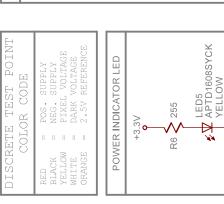
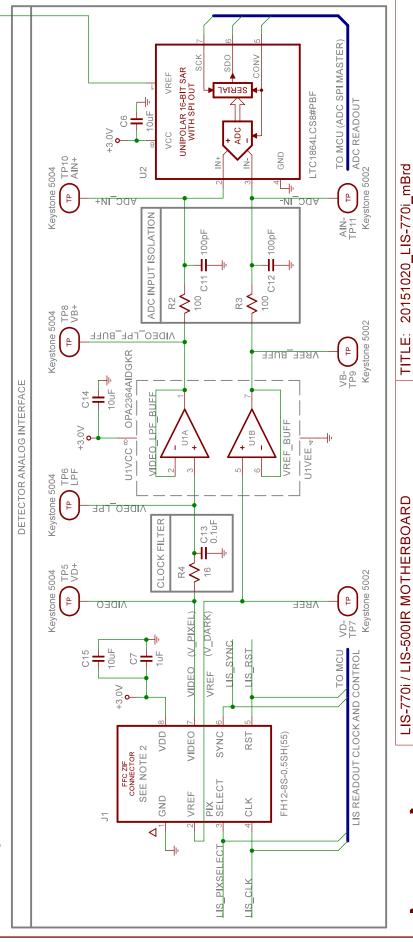
PCB LAYOUT NOTES:

- 1. Split the ground plane below the voltage regulator to isolate return signals for input and output. See the ground plane layout sketch "LDO voltage regulator ground plane layout.pdf".
- 2. Pin 1 on the motherboard ZIF maps to pin 8 on the daughterboard ZIF: M1->D8, M2->D7, M3 -> D6, M4 -> D5, etc. See sketch in "LIS-770i dBrd and mBrd cable.pdf"



5VREF C5 110uF TP4 2.5V Keystone 5003 ₽ TRIM/NR TEMP REF5025AIDGKR VOUT 2.5V REF VOLTAGE REGULATOR AND REFERENCE GND 03 TP1 GND ₩ 100F 10uF Keystone 5001 +3.0\ 且 C3 04 1uF 3.0V Keystone 5000 +3.0V ₽ C2 SEE NOTE 1 NC-GND TLV70030DDCR LDO 3.0V 200mA 3.3V 05 Keystone 5000 _ ₽ 10uF +3.3V \overline{c}

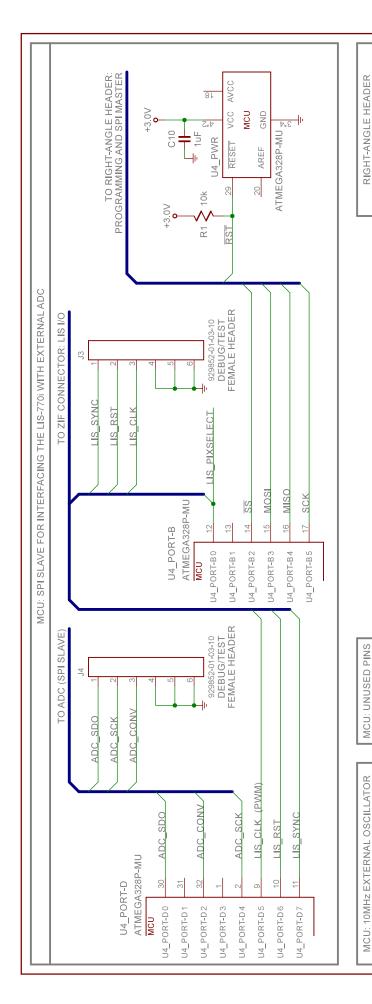


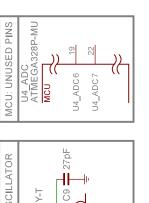


LIS-770i / LIS-500IR MOTHERBOARD
LIS READOUT CIRCUIT (ANALOG)

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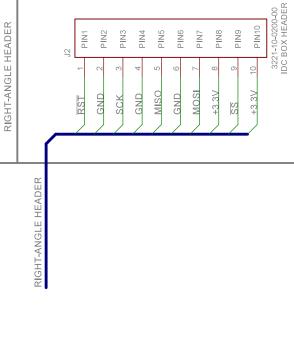
((xtal1 xtal2 ((Atmega328P-mu U4_xtal_pins

MCU [®]

27pF

80

ABM3C-10.000MHZ-D4Y-T





LIS-770i / LIS-500IR MOTHERBOARD

MICROCONTROLLER: ADC, LIS, SPI

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