ATmega328 USART in Master SPI Mode (MSPIM)

UMSELn1:0 bits = [1 1] — enables SPI mode

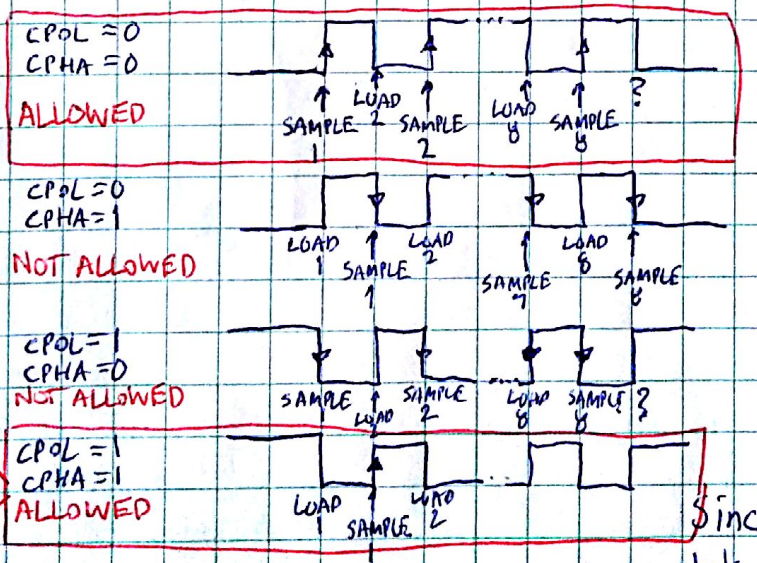
DDR_XCKn = 1 — XCK is an output
this is set before USART in MSPIM is enabled

TXENn = 1 RXENn = 1 — USART in MSPIM is enabled.

$$\text{BAUD RATE} = \frac{f_{osc}}{2(UBRRn+1)} \qquad UBRRn = \frac{f_{osc}}{2 \cdot \text{BAUD RATE}} - 1$$

Baud Rate is bits per second
UBRR is a ~~16~~ 12-bit register

ADC SPI: bits are loaded onto SDO on SCK falling edge. } CPOL=0 CPHA=0 OR CPOL=1 CPHA=1
SPI master samples SDO on SCK rising edge. }
~~This seems OK with either clock polarity~~ phase polarity
No, the clock will have to idle high.
This is why the datasheet specifies the setup time between ADC CONV ↓ and ADC SCK ↓...
we will have some delay between ADC CONV ↓ and running the USART to generate the first SCK ↓.
The safe approach is CPOL=1, so for sample on rising edges, then CPHA=1



Pick this one

SAMPLE FIRST: PHASE=0
LOAD FIRST: PHASE=1
FIRST EDGE IS RISING: POLARITY=0
FIRST EDGE IS FALLING: POLARITY=1
So, sample on a rising and shift on a falling could be
CPOL=0, CPHA=0 or
CPOL=1, CPHA=1

Since we know how long instructions take (at least 100ns) and setup is 60ns, either clock polarity is fine.
CPOL=1 & CPHA=1

UCPOLn = 1 UCPHAn = 1
UDORDn = — MSB first

First poll for UDREn to go high in UCSRnA → Write two bytes to UDRn for a 16-bit transfer. A UART transmit complete interrupt signals that the 16-bit value was shifted out (and a 16-bit value was shifted in). Or you can poll for RXCn in UCSRnA to go high.