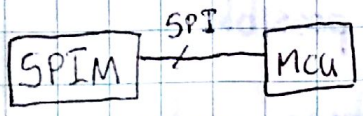
① Frame Request



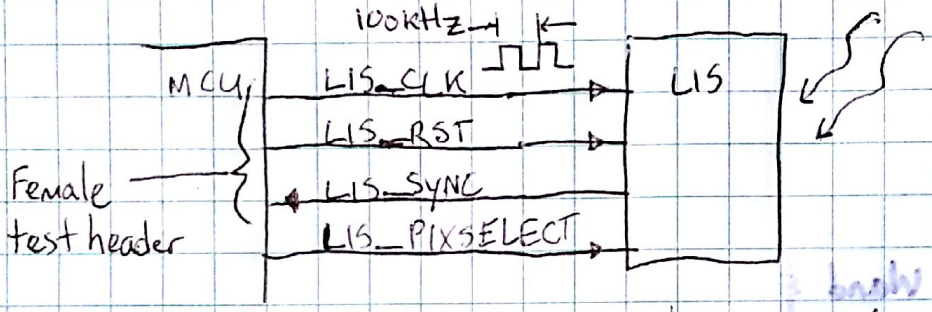
④ Frame Transmit

MISO ↓, $\overline{SS}$ ↓, SPIM clocks MCU, MCU loads frame into SPI transmit buffer.

No test points (maybe put test points on Sim PCB)

$\overline{SS}$	$\overline{SS}$ ↓, SPIM clocks MCU, MCU receives message.
MOSI	
MISO	$\overline{SS}$ ↑, SPIM polls MISO.
SCK	

② Integration



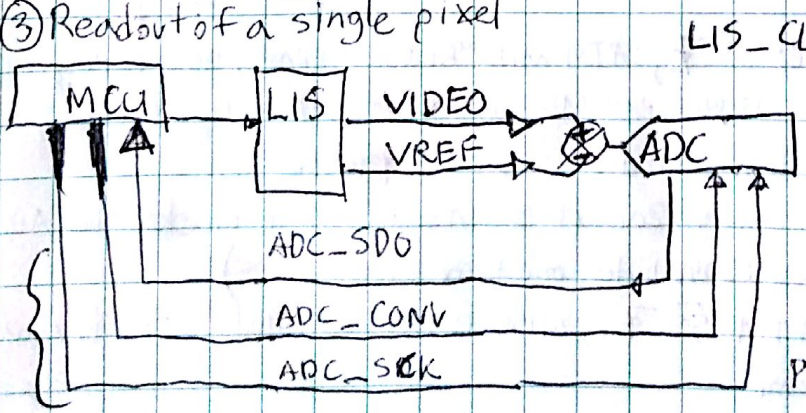
LIS_CLK always runs for evaluation. It is 100kHz.
In production, LIS_CLK will be low and off.
When a frame request comes in, MCU starts LIS_CLK. One cycle is sufficient for recovery (verify this by looking at V_{REF} and V_{out} -- recovery depends on capacitive loading of these pins.)
LIS_RST is low when entering this state.

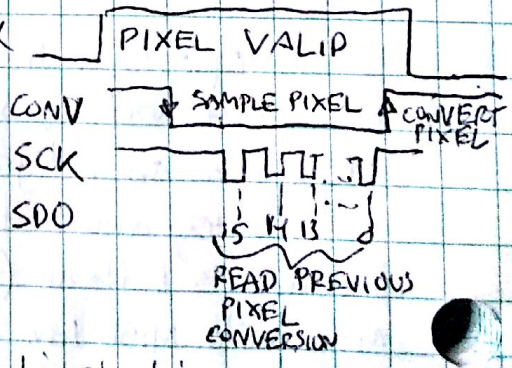
LIS_RST ↑, int. pd. begins. LIS_RST ↓, int. pd. ends

LIS_SYNC ⎍ output by LIS.

readout starts on next LIS_CLK ↑, pixels valid while LIS_CLK is high.

③ Readout of a single pixel





Pixel is stored in memory.

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