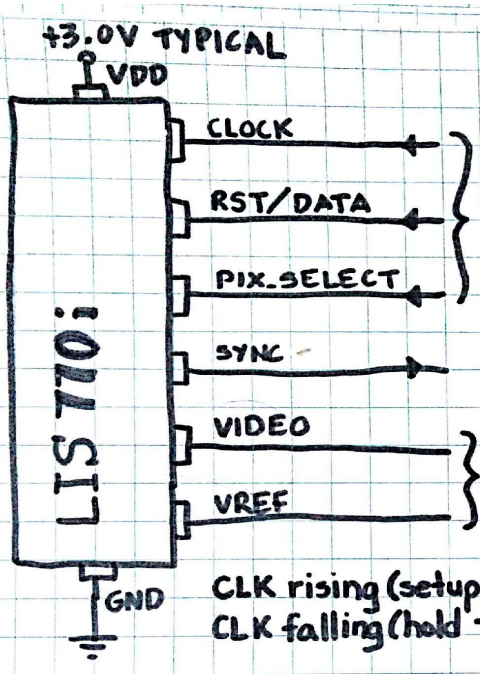
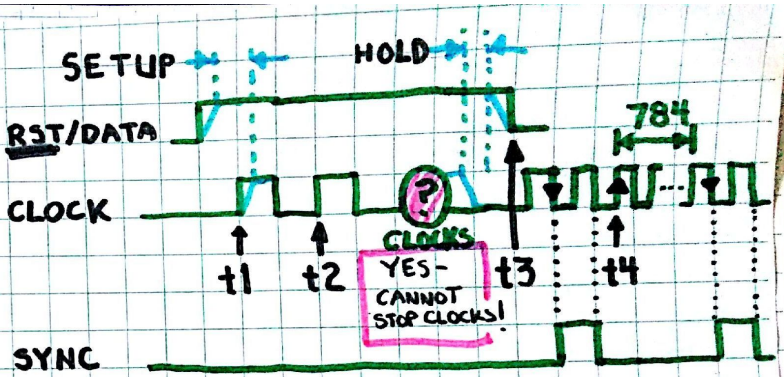
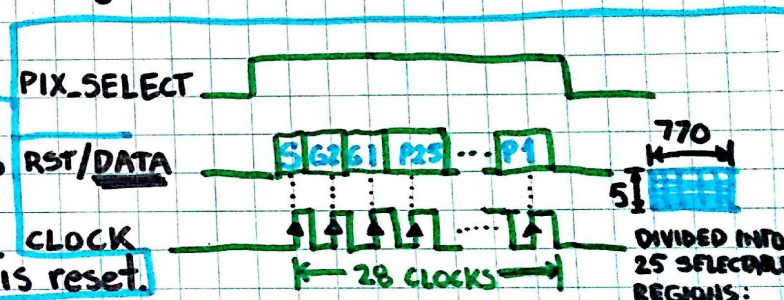


CLK rising (setup time): 10.0ns
CLK falling (hold time): 10.0ns



Integration and Readout



t1: Internal logic is reset and pixel charge is reset.

t2: Integration period begins.

t3: Integration period ends.

Programmable Setup

DATA is shifted in on rising edges of CLOCK.

S=0 → 784 pixels S=1 → 392 pixels (pixels added)

G[2:1]=00 → A_V=1 01 → A_V=2.5 10 → A_V=4 11 → A_V=5

t4: Pixel readout begins. Sample data anywhere from the CLOCK rising edge until the clock falling edge:

Readout begins as soon as integration ends; there is no "hold" functionality.