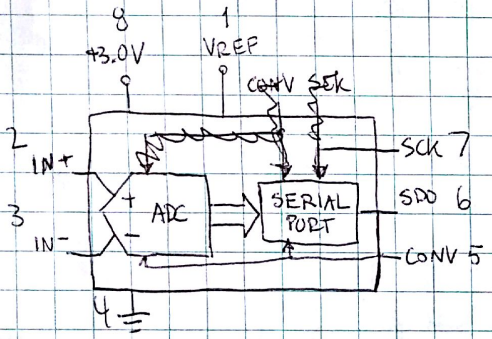
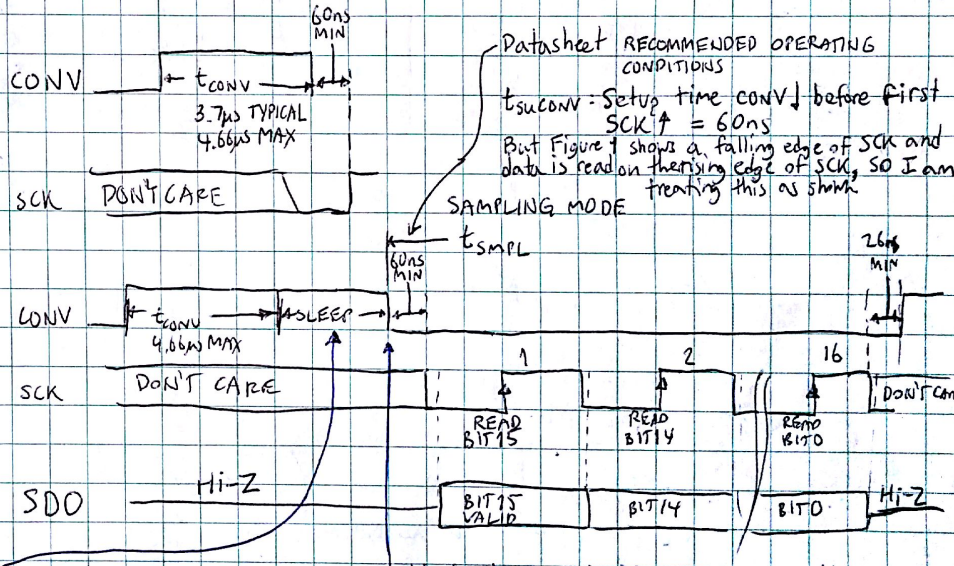
CONV: Convert Input – A logic high on this input starts the A/D conversion process.
A logic low on this input enables the SDO pin, allowing the data to be shifted out.

SDO: Digital Data Output – The A/D conversions are shifted out on this pin.

SCK: Shift Clock Input – This clock synchronizes the serial data transfer. Duty cycle needs to be close to 50%.





Datasheet RECOMMENDED OPERATING CONDITIONS
t_{SUCONV}: Setup time CONV↓ before first SCK↑ = 60ns
But Figure 1 shows a falling edge of SCK and data is read on the rising edge of SCK, so I am treating this as shown.

Wait for the pixel voltage to stabilize before ADC CONV↓

This is the beginning of reading a pixel voltage. 16 SCK + t_{CONV} LATER, the pixel voltage is read while the next pixel is sampled.

"...take care to ensure the transients ~~settle~~ caused by the [capacitive switching input] current spikes settle completely before the conversion begins." Does this mean the "conversion" or the "sampling"? Conversion.