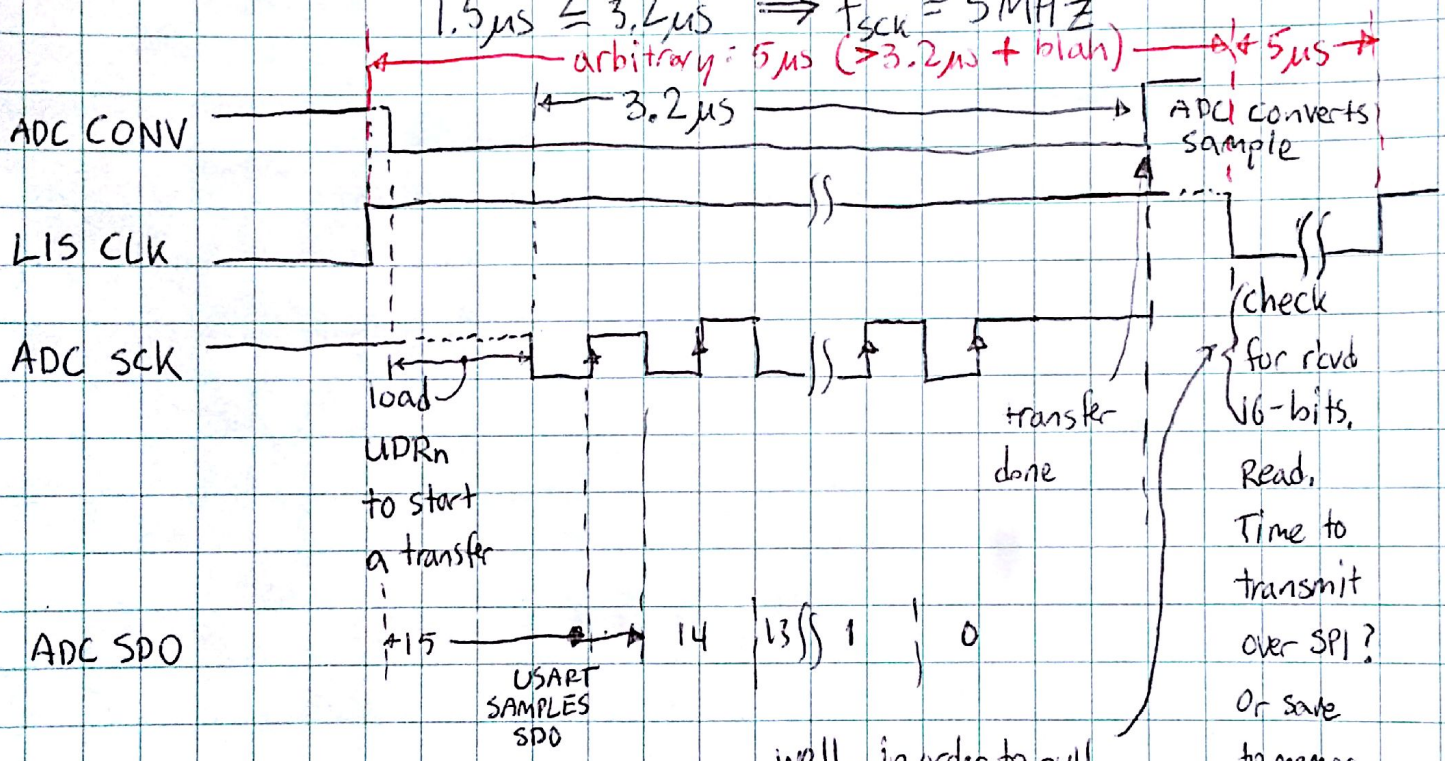
The op amp settles to 0.01% (6.5 LSB) in 1.5 µs.
The RC filter settles to 0.01% in 10 τ, $\tau = 10ns$, $10\tau = 100ns$.
The fastest we can clock the ADC with the USART XCK on a 10MHz ATmega328 is 5MHz.
Sampling lasts for 16 SCK. $16 \cdot \frac{1}{5MHz} = 3.2\mu s$.

The only open question: what effect does ADC sampling cap have on settling time?

If we ignore this: We already have $T_{SETTLE} \leq 16 T_{SCK}$:

$1.5\mu s \leq 3.2\mu s \Rightarrow f_{SCK} = 5MHz$



5µs high + 5µs low = 10µs period is no problem assuming there is enough time to transmit data or write to memory. And assuming capacitive loading is not a problem... that is the purpose of the isolation cap after all.

well... in order to pull ADC CONV high, we already knew the USART transmission finished.

6.4µs SPI xfr + ~2µs wait for slave to load byte

100kHz LIS CLK

784 pixels × 10µs

784 pix × 2 $\frac{byte}{pix}$ × 8.4µs

At 100kHz: frame rate = integration time + 7.84ms readout time + 13.2ms transmit time
= Int. Pd. + 21ms