

I2C Controller Implementation Using FPGA and Applying it to 8-Bit ADC

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Abstract: This paper describes the I2C communication controller implementation. The project aims to solve the communication problem between the FPGA and electronic devices, which are I2C compatible devices. The I2C controller design is implemented as a finite state machine. I2C protocol is implemented with Verilog language on XILINX. After simulation the design is synthesized to generate the RTL circuit and program it onto the FPGA Spartan 6 using Xilinx Platform cable. Finally, the design is validated by interfacing an ADC to FPGA which acts as the I2C controller. The data from ADC is read through I2C bus and displayed on LED.

Keywords: I2C, FPGA, Verilog, ADC, Serial communication, System-On-Chip.

1. Introduction

I2C [1], [2] mainly uses either the open-drain or open-collector type of input buffer along the same line, where it allows a single data line to be used for bidirectional data flow and the synchronous 8-bits oriented serial bus for the communication between integrated circuits which are installed one after the other. Philips has Created this in the late 1980s, which is a two wires bus and with five standardized [3] types of speed modes, known by the standard 100 kbps, fast 400 kbps, fast plus 1Mbps, High Speed 3.4 Mbps and Ultra-fast 5 Mbps, which is a SDA line Cable and a SCL cable. FPGA is the digital IC. Where we can program the function of working within chip. It is suitable for circuit design and the chip design, the problem that occurred in the interface of hardware of the FPGA with Pin GPIO connection [4], [5]. Made them unable to connect the electronic devices, like sensors, ADC, EEPROM, etc. where most are the serial connections such as the I2C and SPI. So, to communicate we need to solve the problem of connection, hence we offer the I2C controller. In I2C controller implementation of FPGA, we have implemented it on the XILINX FPGA Spartan 6 [6]-[10]. Therefore, this paper explains how we have designed an I2C controller using Finite State Machine and the I2C controller is being tested by decode and displayed it on 7 segment display through four digits and using which we have compared ADC step input readings on the DMM.

The general structure of an I2C bus is as shown in Fig.3.1. It mainly consists of two wires Known by SCL (serial clock) and SDA (serial data), where number of slave units can be interconnected to master unit. For the Proper functioning of system, we also have a common ground wire. Example of IC family nowadays fabricated with I2C support are also shown in the Fig.3.1, which can include microcontrollers, ADC and DAC converters, also RTC circuits, sensors like temperature sensing, and accelerometers, the SCL here is unidirectional, usually master generates it always, whereas SDA transmission is in bidirectional. As SCL and SDA are open-drain lines, the external pull-up resistor has to be connected between the wires and power supply. The 7 bits of address can be shared through same bus for number of devices. More than one master is allowed, in case the I2C protocol provides bus arbitration. Other advanced features include clock stretching, general call, reset by software, and others.

2. Literature Survey

The I2C Bus is a two-wire, low to medium speed, communication bus developed by Philips Semiconductors in the early 1980s. I2C was created to reduce the manufacturing costs of electronic products. powerful, chip-to-chip communication link within these products [1].

The I2C bus is a very popular and powerful bus used for communication between a master and a single or multiple slave device [2].

Field Programmable Gate Arrays (FPGAs) and Complex Programmable Logic Devices (CPLDs) can be used in virtually any digital logic system. Over 35 million Xilinx components have been used in a wide variety of end-equipment applications, ranging from supercomputers to hand-held instruments, and from missile guidance systems to guitar synthesizers [7].

The modern era of electronics started with the invention of the transistor by William Shockley, John Bardeen, and Walter Brattain at Bell Laboratories in 1947. A partial picture of the original experiment, and a popular commercial package, made out of plastic and called TO-92. Before that, electronic circuits were constructed with vacuum tubes, which were large, slow,

and required high voltage and high power [8].

Field Programmable Gate Arrays have emerged as an attractive means of implementing logic circuits, providing instant manufacturing turnaround and negligible prototype costs. They hold the promise of replacing much of the VLSI market now held by mask-programmed gate arrays [9].

FPGA designs, methodologies, and design techniques. When mentoring new FPGA design engineers, I draw my suggestions and recommendations from this experience. Up until now, many of these recommendations have referenced specific white papers and application notes that discuss specific practical aspects of FPGA design [10].

VHDL is a formal notation intend for use in all of the phases of creation of electronics system. Because of its both machine readability as well human readable, it is being supporting the development, verifying, synthetization, and to test the hardware design [11].

3. Objective

The objective here is to solve the communication problem between FPGA and embedded electronic devices, which are communicated by I2C. I2C is implemented by state machine and simulation is done to performed to check the error. After the process of synthesis RTL circuits is generated and program it to FPGA Spartan 6 using the Xilinx Platform cable. Two experimental boards are required to implement; first development board is FPGA. electronic device that has the I2Ccommunication include 8-bits ADC, 8-bits DAC, etc. is the Second the board.

A. I2C controller design

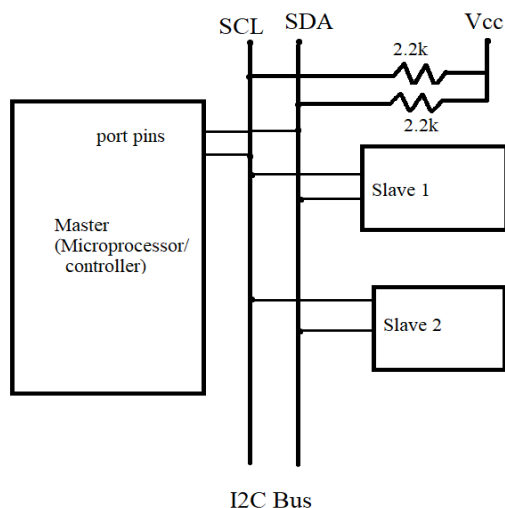


Fig. 1. I2C communication structure

4. Methodology

The setup for experiment is as shown in fig. 2, which consists of Master block and a Slave block. The Master block implements I2C Controller on FPGA. The Slave block consists

of ADC. The output is divided into two sections, the one section contains Serial Clock Line and Serial Data Line, the other section is for testing the circuit, which consists of a display on seven-segment four digits the data read from Analog to Digital Converter.

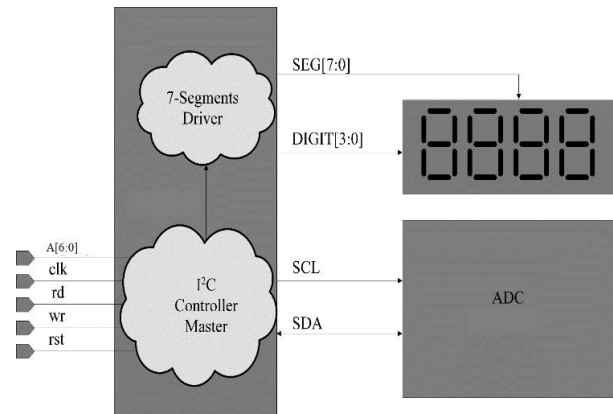


Fig. 2. Block diagram

The Master block consists of Address line, clock (clk), read(rd), write(wr), reset(rst) which are at the input side as shown in the figure above and Serial clock Line and Serial Data Line are connected with the ADC block and the output is displayed on seven segment LED block.

5. Results

In fig. 3, the simulation results where it has the output of serial data line, serial clock line, system clock, reset, 8 states, 7-bit address and 8-bit data.

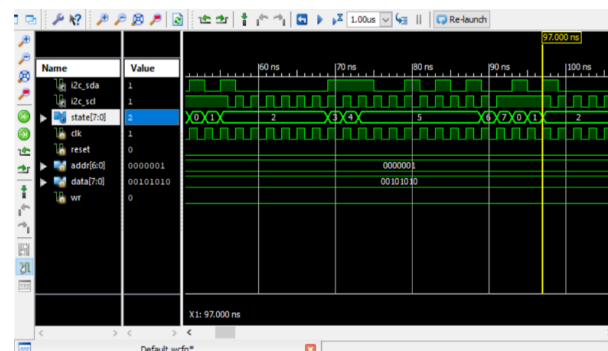


Fig. 3. Simulation result

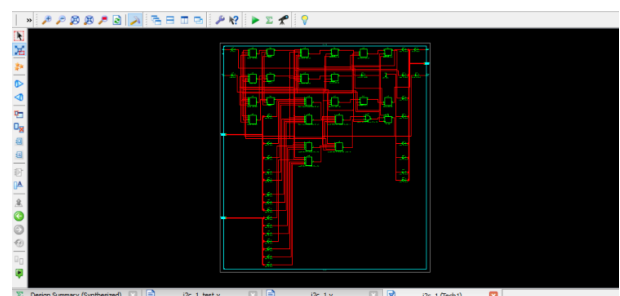


Fig. 4. Technology schematic

In fig. 4, it is the Technology Schematic after the Verilog synthesis phase which represents the pre optimized design in term of generic symbols.

In fig. 5, is the RTL Schematic i.e. Register Transfer Level Schematic which opens an NGR file to view as the gate level schematic which also represents the pre optimized design in term of generic symbols.

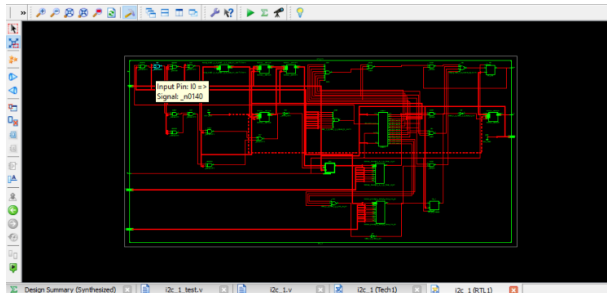


Fig. 5. RTL schematic

6. Conclusion

The project is designed using ISE Design tool version 12.1 and is able to provide an accurate simulation result of an I2C controller along with RTL and Technology Schematic.

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