ECG Pre-Lab

Sunday, April 23, 2023 1:27 PM

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Original Design:

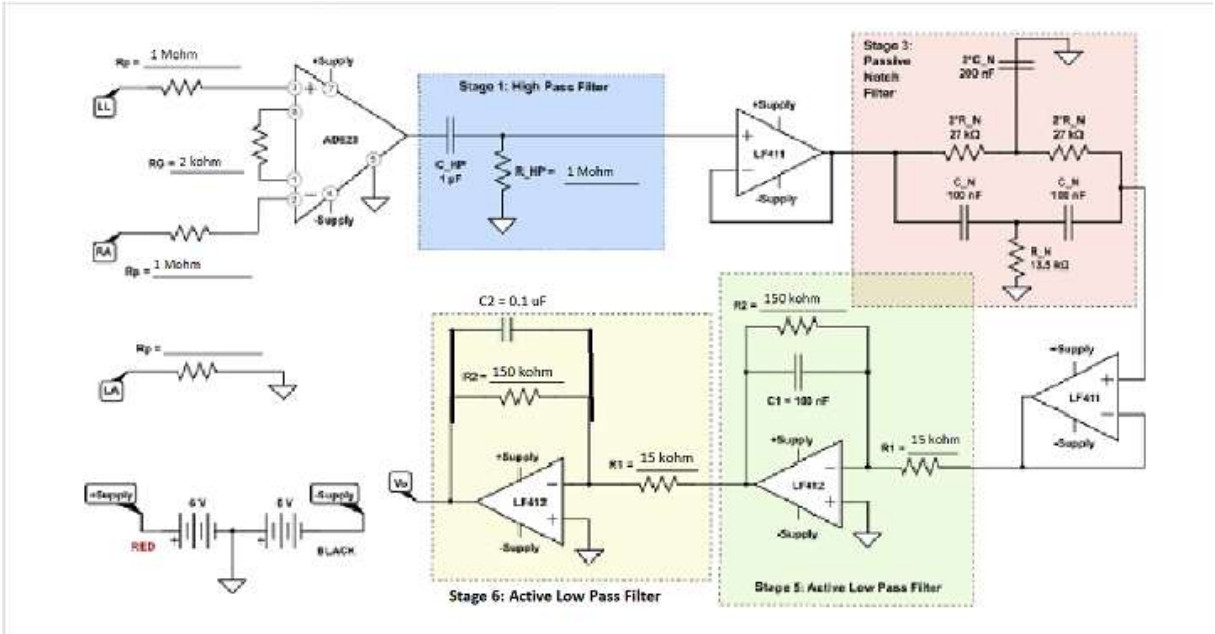


Figure 1: Circuit schematic of Electrocardiogram circuit from EECE 244: Electrocardiogram Circuit Lab handout from

To provide an additional layer of safety, we will include resistors to limit the maximum current flowing from our circuit to the electrodes. We will employ a factor of safety of 1000; therefore, **the maximum current will be limited to 10 µA**. Given a supply voltage of **5V** calculate the value of the resistors to achieve a current of 10 µA.

R = 500 kΩ

Round this up to the next resistor available (100kΩ, 150kΩ, 200kΩ, or 1MΩ)

R_P = 1 MΩ

Measurement with an Instrumentation Op Amp

The first stage of amplification uses an AD623 instrumentation amplifier. Locate the formula for setting the gain in the datasheet (https://www.analog.com/media/en/technical-documentation/data-sheets/ad623.pdf) and write it below:

$$Gain\ Formula = 1 + \frac{100\,k}{R_g}$$

The gain should be between 40 and 60. This will be adjusted later during the tuning phase. Determine an appropriate value for the gain resistor R_G in the circuit shown above.

Stage 1 Gain Resistor R_G = 2k Ω (1.7k ⇒ 2.6k) Ω

Gain: 51

Passive High Pass Filter Design (Stage 1)

We will use a high pass filter to eliminate baseline (DC) drift (e.g. low frequency noise). Generally, the heart rate is above 60 beats per minute (BPM), so we will want to design filter with a fc below 1 Hz. Given f_c = 0.16 Hz and a capacitor C_{HP} = 1 µF, calculate the appropriate resistor value for the first-order analog filter used in the ECG circuit.

Formula for Cutoff Frequency: $f_c = \frac{1}{2\pi R_{HP} C_{HP}}$

Given:

C_{HP} = 1 µF

High Pass Frequency (f_c) = 0.16Hz

Find:

R_{HP} = 994718 Ω

Passive Notch Filter Design (Stage 3)

In the second stage or buffer amplifier, we remove 60 Hz noise in stage 3. 60 Hz noise is a particular issue in our electronics lab. This design follows the Twin-T notch topology. Since this design is particularly sensitive to tolerances in component values, you should measure resistances carefully and trim values. The corner frequency (f_C) is found by:

$$f_C = \frac{1}{4\pi R_N C_N}$$

Verify that for the circuit components given in figure 1 that fc ≈ 60 Hz. Again, measure component values carefully in this design and match them as well as possible.

Find:

f_c = 58.95 Hz

Active Low Pass Filter Designs (Stage 5)

Following another buffer (stage 4), is a 1st order active low pass filter. In this design, we want a gain of 10-15 and a low-pass cutoff frequency (f_C) that removes 60 Hz noise and does not overly affect our ECG measurement. Recall that a lower cutoff frequency will provide greater 60 Hz noise attenuation, but too aggressive of a cut-off could lead to signal distortion. Write the formula for the inverting gain and cutoff frequencies (see *Design with Operational Amplifiers and Analog Integrated Circuits* by Sergio Franco, Section 3.2 First Order Active Filters). To design for the gain in the passband, assume that the contributions of the capacitor are negligible (i.e.- the jωC term goes to 0).

$$Gain = -R_2/R_1$$

$$f_C = \frac{1}{2\pi R_2 C_1}$$

Assume the magnitude of the gain is 10 and fc = 10.6 Hz. Use these formulas to select components knowing we'll use: **C_1 = 0.1 µF**. Find R_1 and R_2.

Given:

|Gain| = 10 V/V

f_c = 10.6 Hz

Find:

R_1 = 15 kΩ

R_2 = 150 kΩ

For Stage 6, stage 5 is repeated to further increase the gain of the circuit

Figure 2: EECE 244: Electrocardiogram Circuit Lab handout

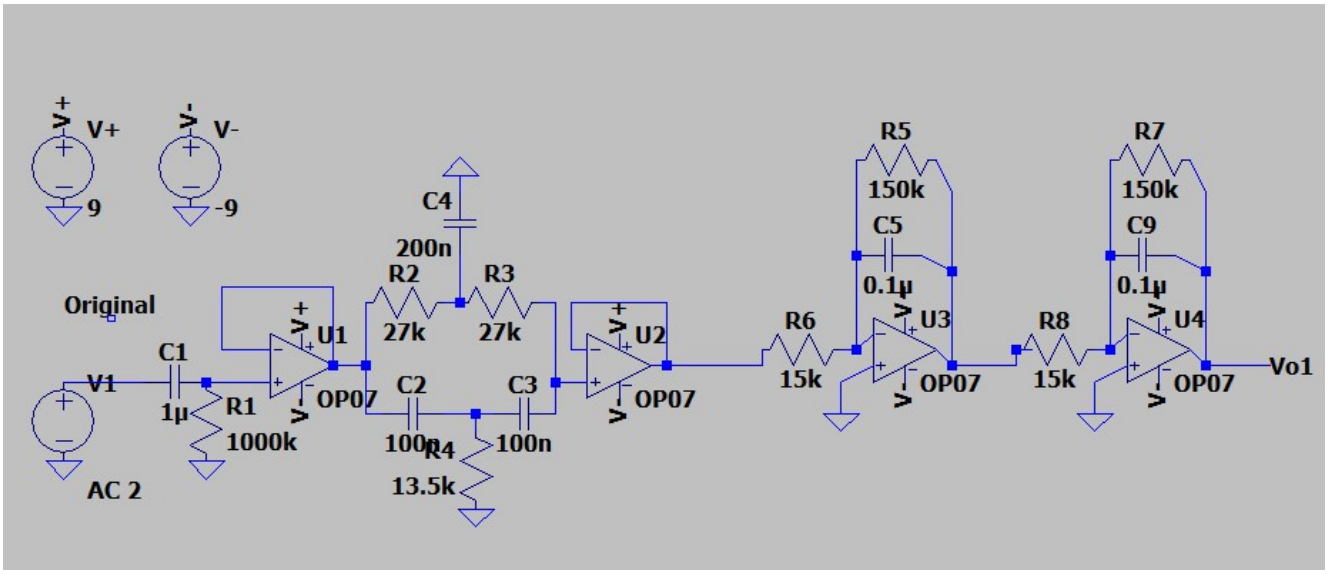


Figure 3: LTSpice Circuit Schematic of stages 1-6 from Figure 1

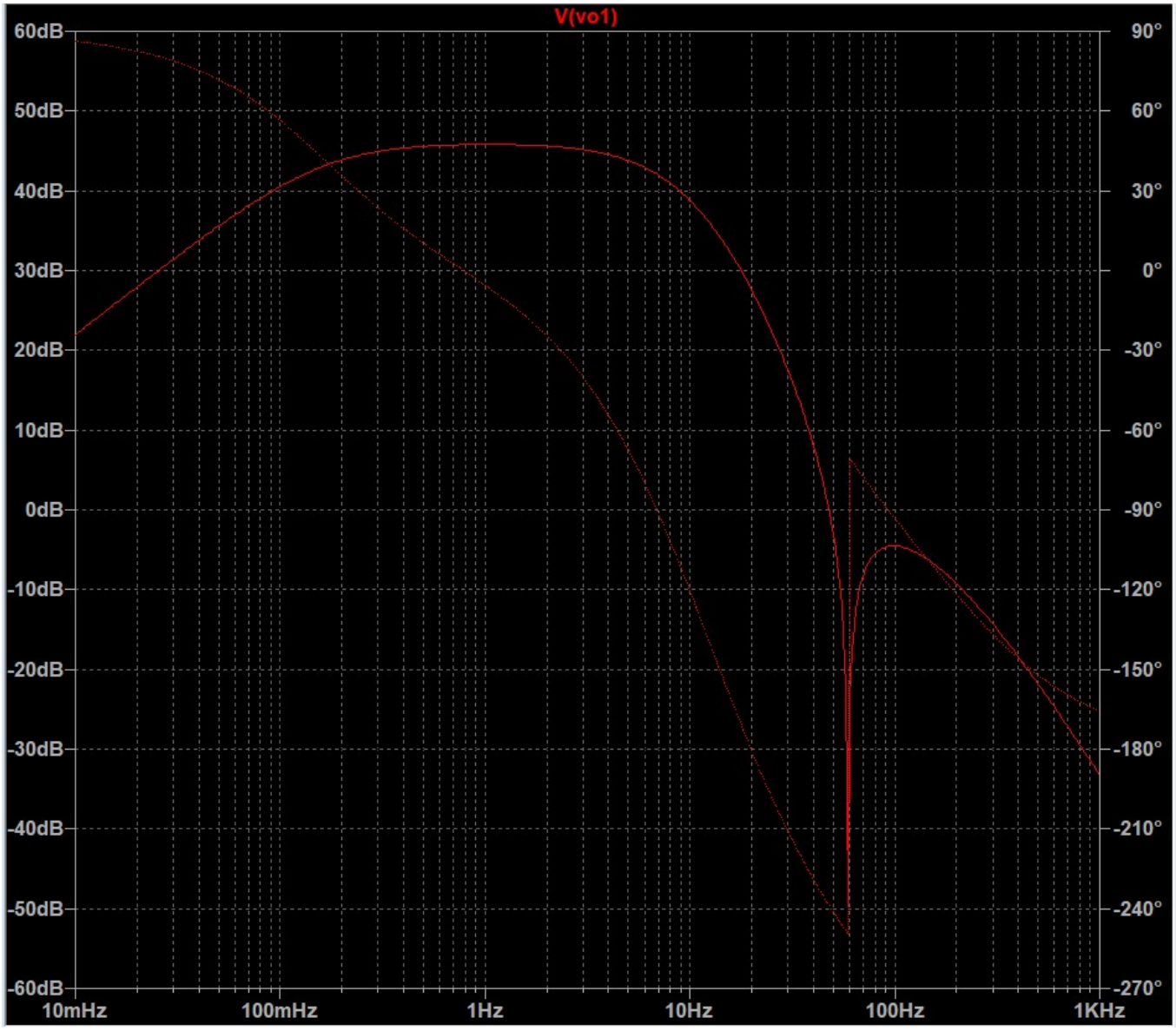


Figure 4: Frequency response of Figure 3 from 0.01Hz to 1KHz at 2 Vpp

Simplified Design:

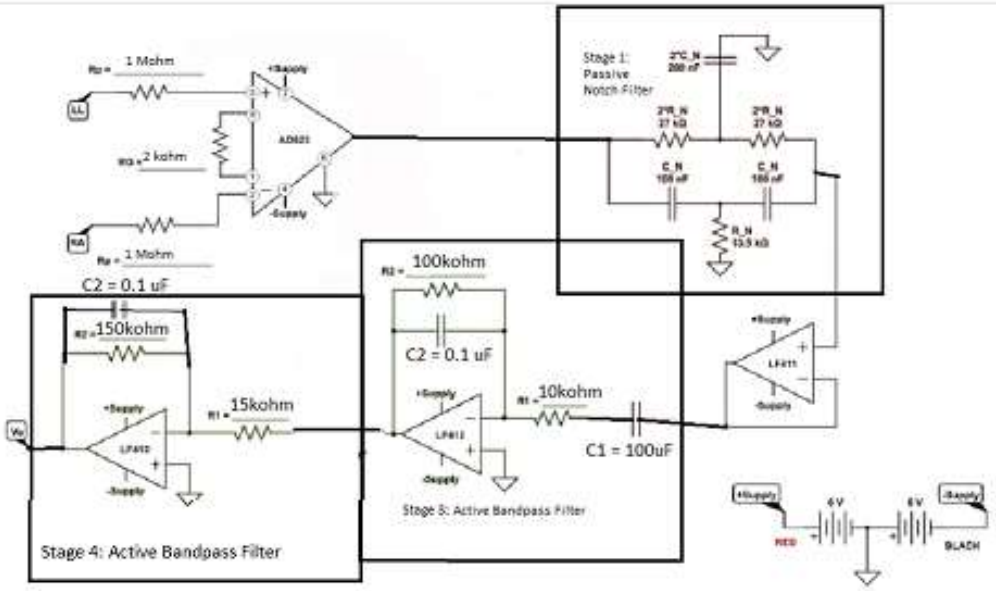


Figure 5: Circuit schematic of Simplified Electrocardiogram circuit

Passive Notch Filter Design (Stage 1)

In the first stage or buffer amplifier, we remove 60 Hz noise in stage 3. 60 Hz noise is a particular issue in our electronics lab. This design follows the Twin-T notch topology. Since this design is particularly sensitive to tolerances in component values, you should measure resistances carefully and trim values. The corner frequency (f_C) is found by:

$$f_C = \frac{1}{4\pi R_N C_N}$$

Verify that for the circuit components given in figure 1 that fc ≈ 60 Hz. Again, measure component values carefully in this design and match them as well as possible.

Find:

f_c = 58.95 Hz

Active Band Pass Filter Designs (Stage 3)

In the third stage, we will use an active bandpass filter to eliminate baseline DC drift (e.g. low frequency noise) and 60 Hz noise that does not overly affect our ECG measurement. Generally, the heart rate is above 60 beats per minute (BPM), so we will want to design filter with a fc1 below 1 Hz. Recall that a lower cutoff frequency will provide greater 60 Hz noise attenuation, but too aggressive of a cut-off could lead to signal distortion so assume fc2 is 10.6 Hz.

Design Equations:

$$f_{c_1} = \frac{1}{2\pi R_1 C_1} \qquad f_{c_2} = \frac{1}{2\pi R_2 C_2}$$

$$\text{Gain} = \frac{-R_2}{R_1}$$

Given;

$|\text{Gain}| = 10 \frac{V}{V}$

$f_{c_1} = 0.16\ \text{Hz}$

$f_{c_2} = 10.6\ \text{Hz}$

$C_1 = 10\ \mu\text{F}$

$C_2 = 15\ \mu\text{F}$

Find

$R_1 =$ 100 kΩ

$R_2 =$ 1 mΩ

Using a 1M ohm resistor outside of the instrumentation op amp is not recommended. We also want to try to reduce the capacitor values to maximize slew rate.
To start, R1 will be 100k ohms

For more realistic values:

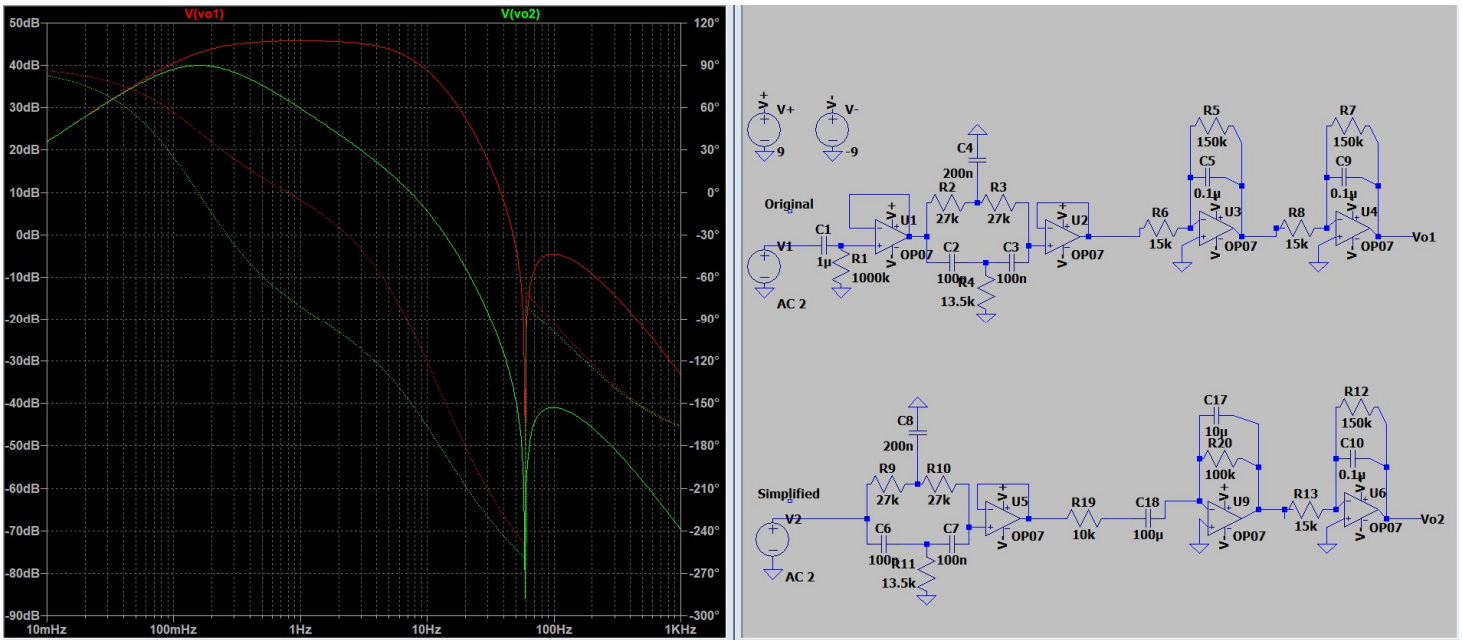
$R_1 = 10\ \text{k}\Omega$

$C_1 = 99\ \mu\text{F}$ (ideal) $= 100\ \mu\text{F}$ (standard)

$R_2 = 100\ \text{k}\Omega$

$C_2 = 15\ \mu\text{F}$ (ideal) $= 10\ \mu\text{F}$ (standard)

From the calculations above, the bandwidth of the passband is not as large as the bandwidth of the pass band in the original circuit.



To fix this, we will set C2 = 0.1uF

Active Low Pass Filter Designs (Stage 4)

Following another buffer (stage 4), is a 1st order active low pass filter. In this design, we want a gain of 10-15 and a low-pass cutoff frequency (f_c) that removes 60 Hz noise and does not overly affect our ECG measurement. Recall that a lower cutoff frequency will provide greater 60 Hz noise attenuation, but too aggressive of a cut-off could lead to signal distortion. Write the formula for the inverting gain and cutoff frequencies (see *Design with Operational Amplifiers and Analog Integrated Circuits* by Sergio Franco, Section 3.2 First Order Active Filters). To design for the gain in the passband, assume that the contributions of the capacitor are negligible (i.e.- the jωC term goes to 0).

$$Gain = -R_2/R_1$$

$$f_C = \frac{1}{2\pi R_2 C_1}$$

Assume the magnitude of the gain is 10 and fc = 10.6 Hz. Use these formulas to select components knowing we'll use: **C_1 = 0.1 µF**. Find R_1 and R_2.

Given:

|Gain| = 10 V/V

f_c = 10.6 Hz

Find:

R_1 = 15 kΩ

R_2 = 150 kΩ

Figure 6: Design specifications and calculations referring to Figure 5

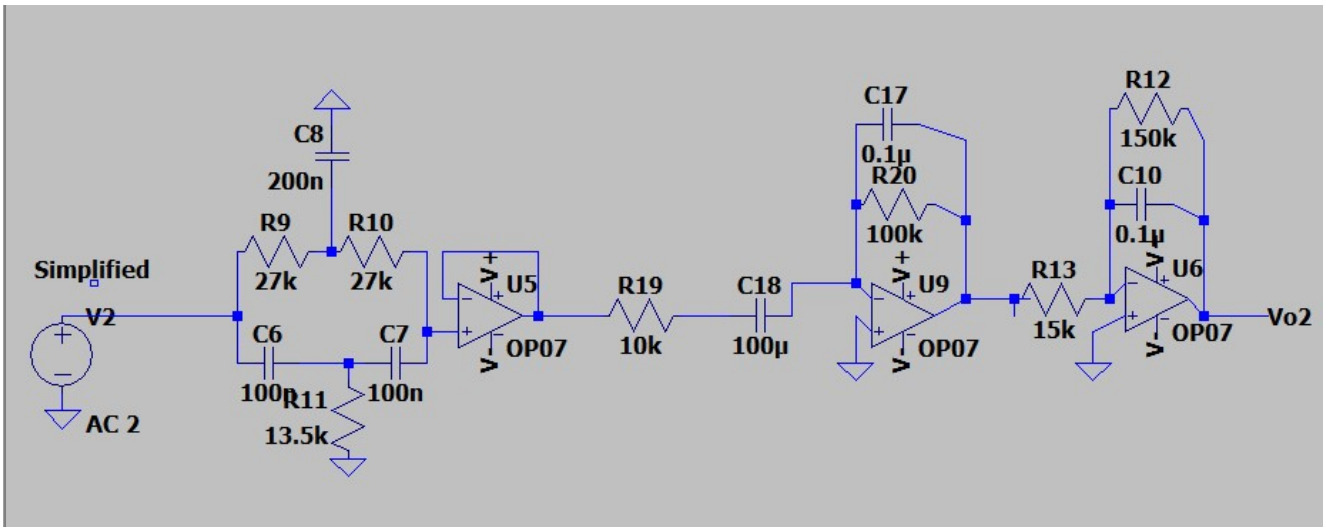


Figure 7: LTSpice Circuit Schematic of stages 1-4 from Figure 5

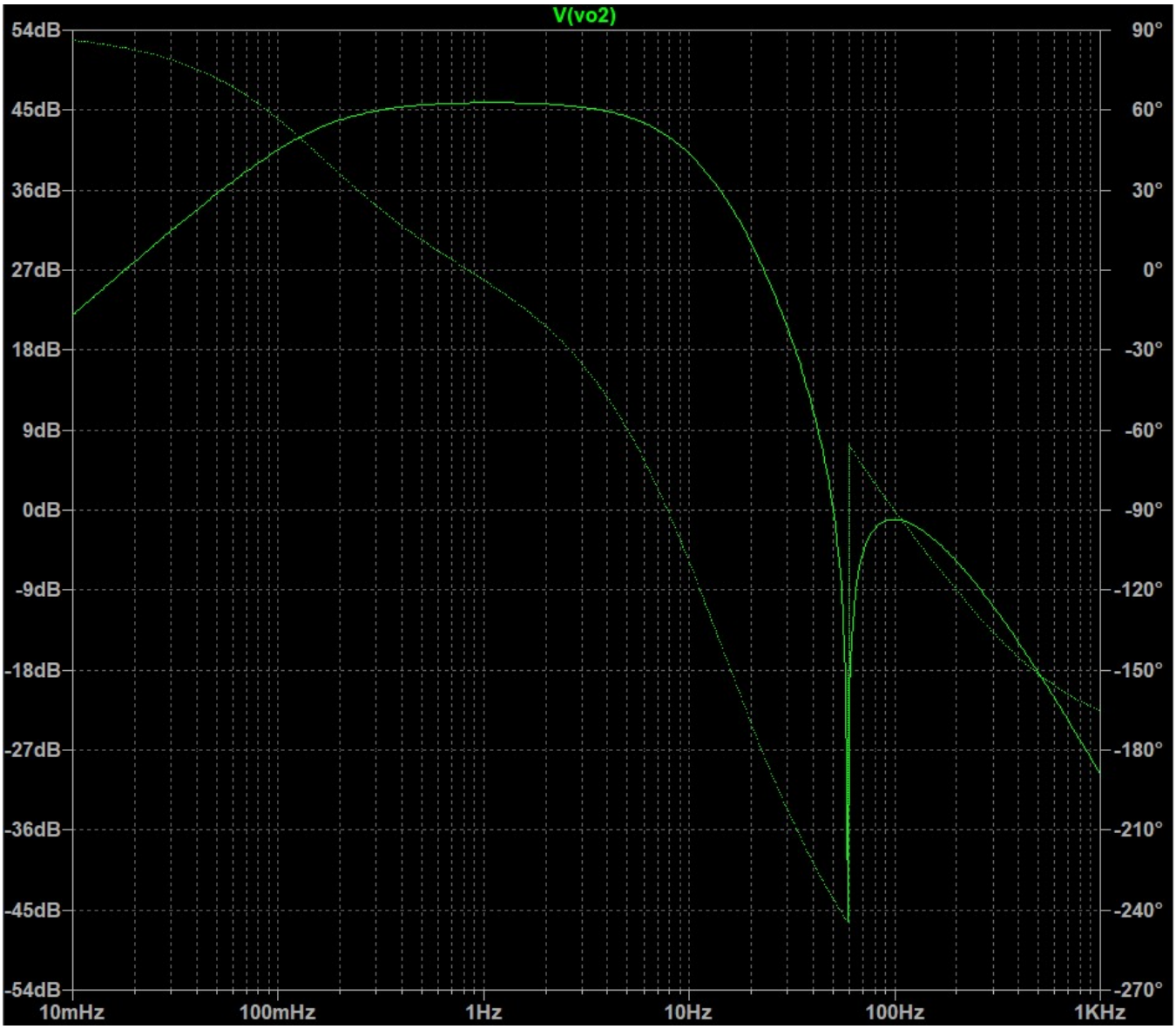


Figure 8: Frequency response of Figure 7 from 0.01Hz to 1KHz at 2 Vpp

Comparison:

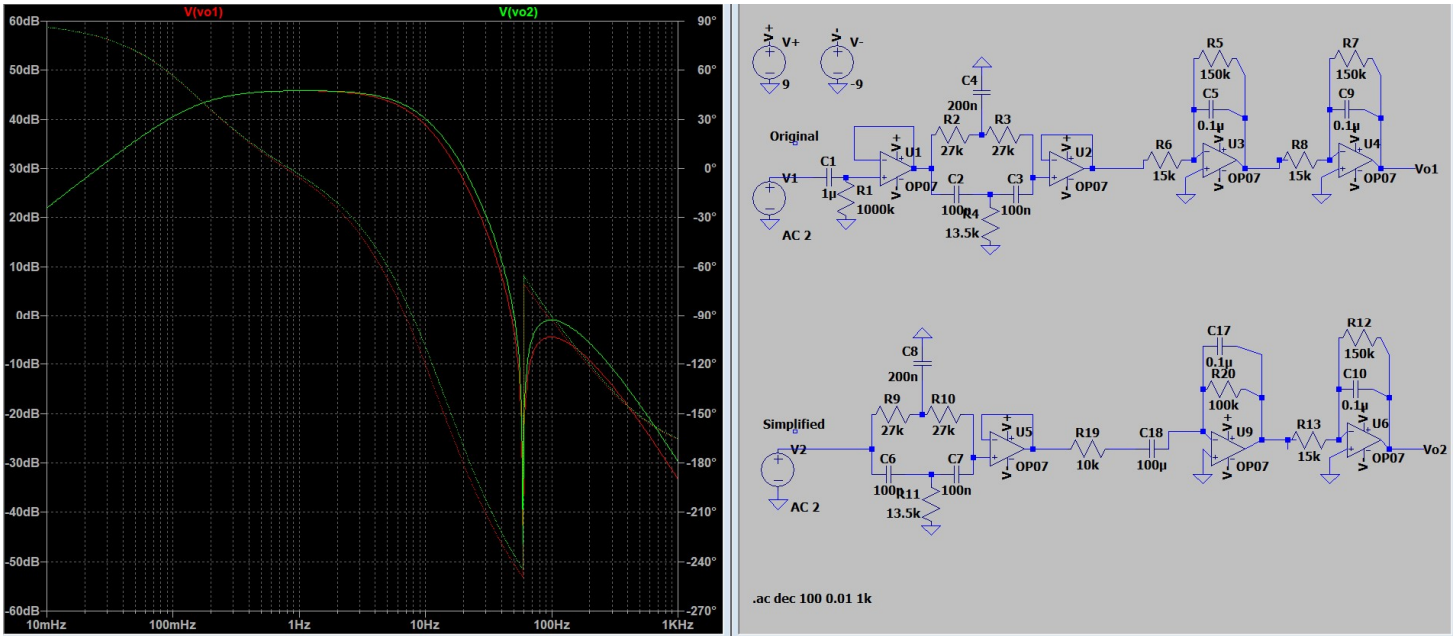


Figure 9: Frequency response comparison of Figure 1 and Figure 7 from 0.01 to 1KHz at 2Vpp

Max Gain = 45.84 dB = 195.9 V/V