

Gildin Ilia

Electronics engineer, looking for a position in PCB Design, RT/ED, FPGA and Solidworks

ID number : 309068278

Born on October 16th, 1989

Address : Bney Akiva 2/16, Ashkelon

Phone : +972-53-423-03-13

Mail : ilia178@gmail.com

Education

- 2010 - 2014** SCE - SHAMOON COLLEGE OF ENGINEERING
B.Sc. in Electrical Engineering, with specialization in communications.
▷ *Specialized in DSP, random signals, image processing.*
▷ *Final-year project : use of compressive sensing methods for the analysis of spectrometric data.*
- 2020** FPGAXPERT - LOGTEL
▷ *LVDS, BRAM, LUT6, DSP, Distributed Memory, BUFG, BUFR, IBUFDS, ISERDES, OSERDES, AXI.*
▷ *Clock Inter/Intra effects.*
▷ *Writing Test-bench Simulation.*
▷ *CHIP-SCOPE.*

Work Experience

- 2020-** GENERAL COVID WORKS
▷ *Mostly cleaning offices.*
- 2017 - 2020** SENSORITY
▷ *Digital Board Design.*
▷ *Micro-controllers programming in C embedded.*
▷ *Worked with UART, SPI, I²C protocols.*
- 2014 - 2017** IPU INDUSTRIES
▷ *Digital Board Design.*
▷ *Micro-controllers programming in Assembler language and C embedded.*
▷ *Worked with UART, SPI, I²C protocols.*
▷ *Programming computer screens in C++ and C#.*

Electronics knowledge

- ▷ *Board Design.*
▷ *High Speed Board Design.*
▷ *FPGA.*

Computer Skills

- PROGRAMMING LANGUAGES
▷ *VHDL, C / C++, Matlab, Assembler, Verilog.*
- ENVIRONMENTS
▷ *Vivado, IAR, Keil, MPLAB X, Qt5, Linux, OpenCV, Caffé, OpenVino, TensorFlow.*
- OTHER
▷ *Solidworks.*

Foreign languages

- ▷ *Hebrew (mother tongue).*
▷ *Russian (mother tongue).*
▷ *Fluent English.*

Publications

- ▷ *T. Trigano, I. Gildin and Y. Sepulcre, "Pileup correction algorithm using an iterated sparse reconstruction method", IEEE Signal Processing Letters, Volume : 22, Issue : 9.*