
Logic Design Course

Arithmetic Unit Project

Team 15's Documentation

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I. Names

- Mahmoud Adas
 B.N 23
- Khaled Sabry
 B.N 21
- Mahmoud Youssri
 B.N 24
- Loai Ali
 B.N 13

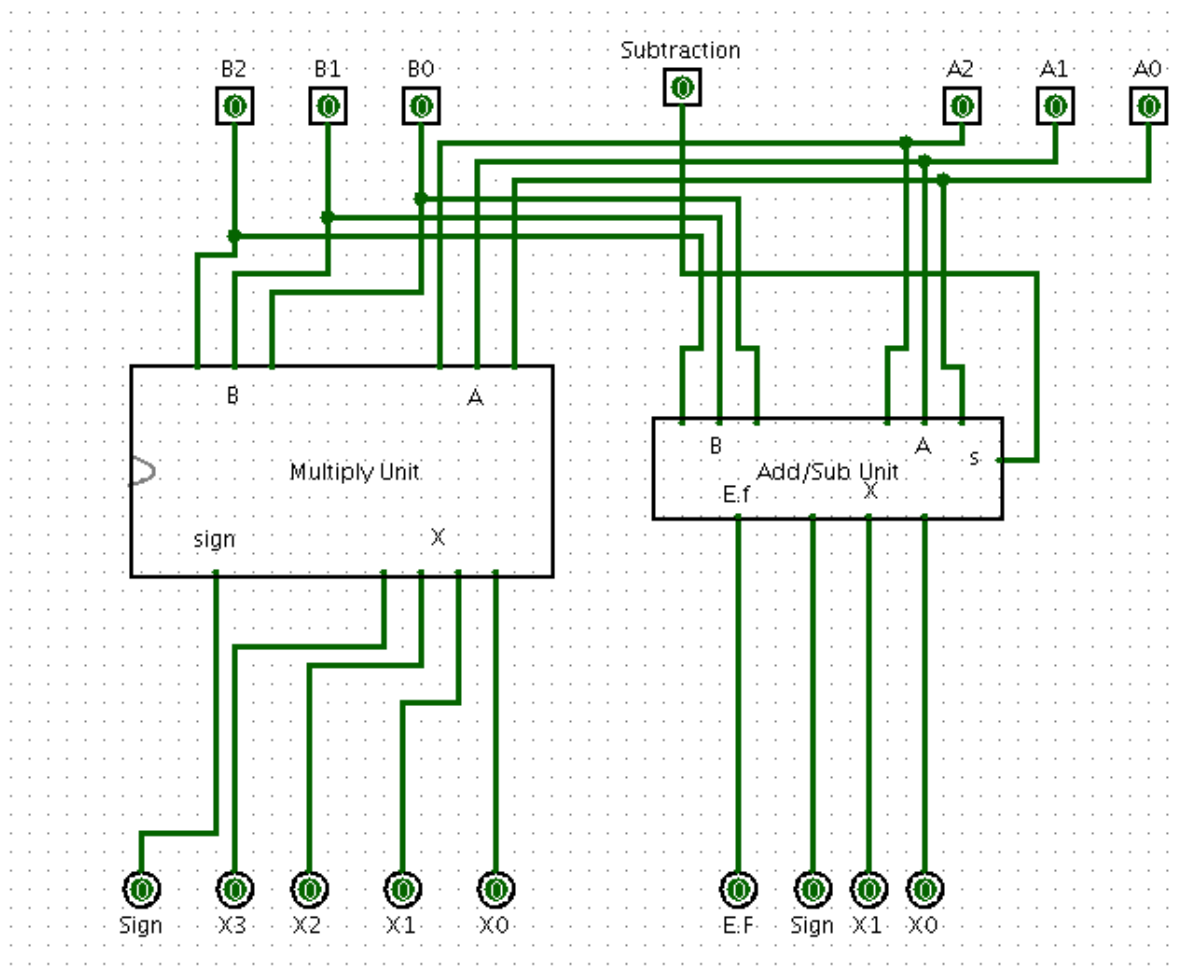
II. Tasks

- Design the Adder/Subtractor
 - All
- Design the Multiplier
 - Loai
 - Mahmoud Adas
- Design the converter
 - Mahmoud Adas
- Design Error Flag
 - Mahmoud Youssri
 - Mahmoud Adas
- Simulate the design in logisim
 - Mahmoud Adas
- Get the tools
 - Mahmoud Youssri
 - Khaled Sabry
- Build Multiplier
 - Mahmoud Youssri
 - Khaled Sabry
 - Mahmoud Adas
- Build Adder/Subtractor
 - Mahmoud Adas
 - Loai
- Build Converters

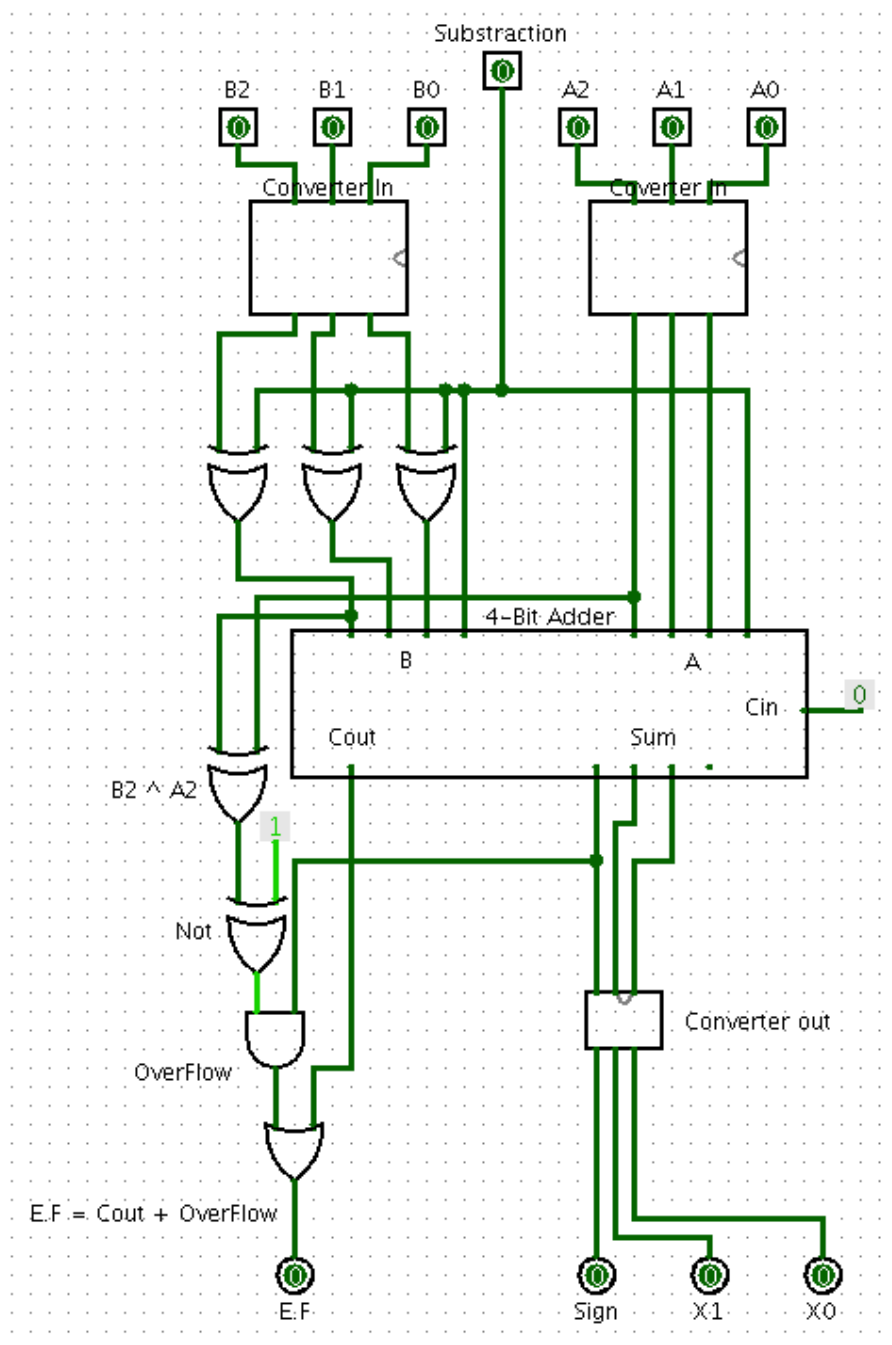
- Mahmoud Youssri
- Khaled Sabry
- Build Error Flag
 - Mahmoud Youssri
 - Mahmoud Adas
- Test
 - All
- Write documentation
 - Mahmoud Adas

III. Logic Diagrams

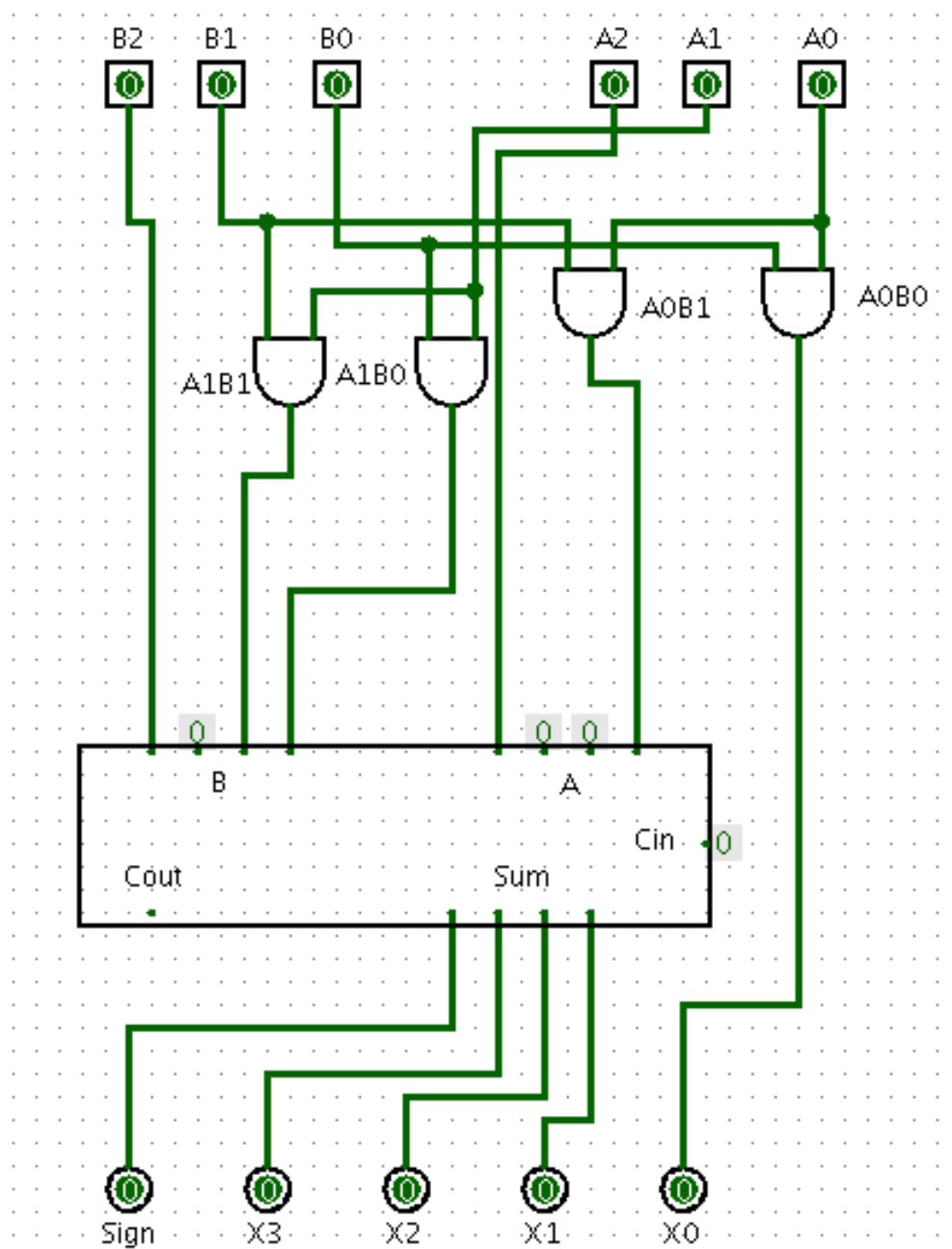
Main



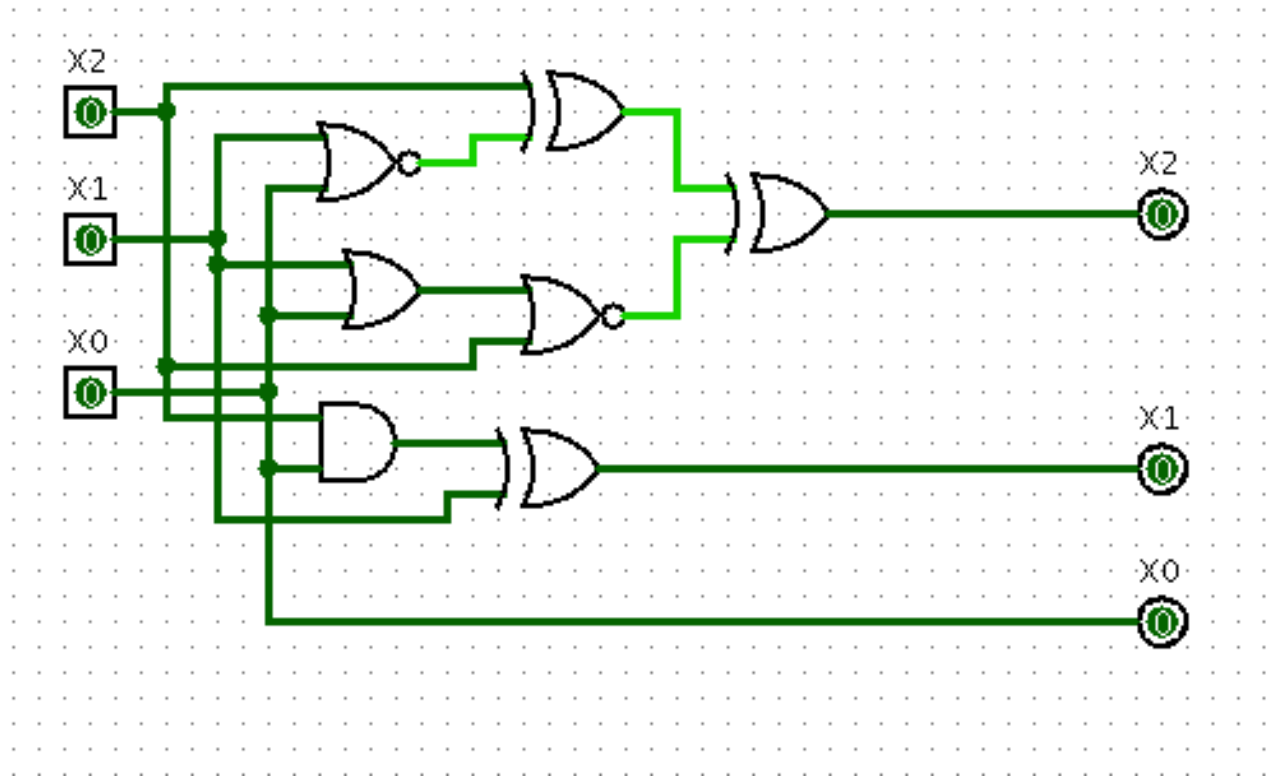
Add/Subtraction Unit



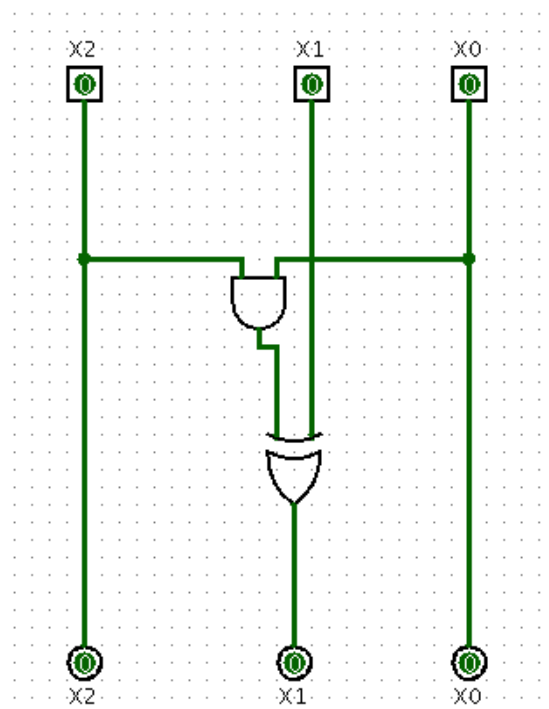
Multiplication Unit



Converter In



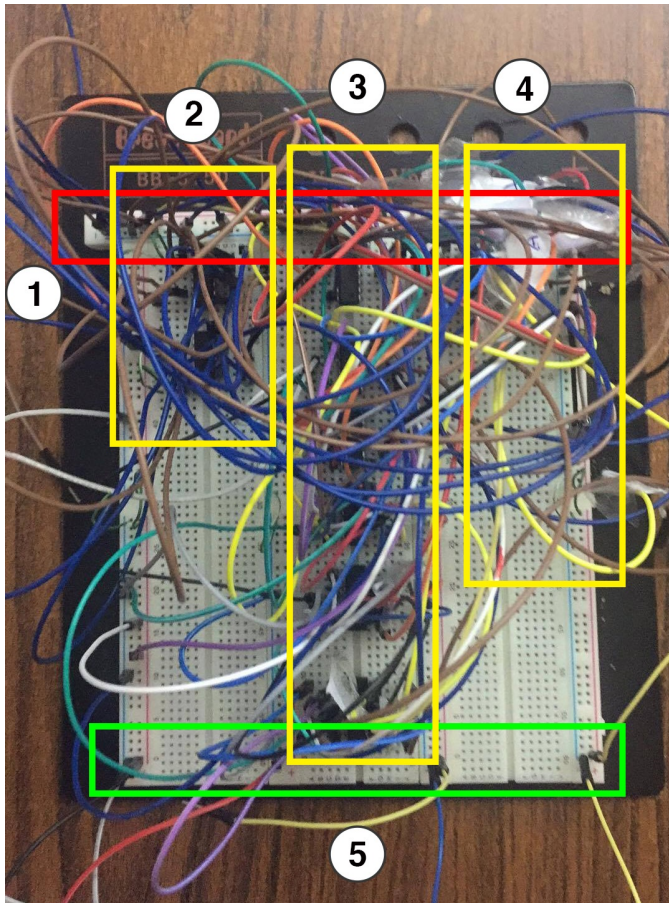
Converter Out



IV. Design Description

Project is divided into 2 main units: the Add/Sub and the Multiplication Unit

- In Multiplication Unit
 - we ANDed all input bits -except signs- and sent them to a 4-bit adder
 - Ignored Error Flag and Carry-out; it is useless
- In Add/Sub Unit
 - Inputs are converted from magnitude to the 2nd complement (if negative)
 - input B is XORed with the Subtraction selector, to flip them in case of subtraction or pass it otherwise
 - both inputs (after converting) are inserted in 4-bit adder in gates 2:4 leaving the first one for the subtraction selector and ignoring the C-In (always 0)
 - *we decided that so we can get the C-out. In case we inserted the numbers from 1:3, we would leave the last gate then lose the C-out
 - the output then is Converted from the 2nd complement to the magnitude using the Converter-Out (lightweight copy of converter-in)
 - Error Flag
 - is the OverFlow ORed with C-out
 - $E.F = O.F + C.out$
 - OverFlow
 - happens when both signs are 1 or 0 and the result sign is different than them
 - $O.F = \sim(B2 \wedge A2) . X2$
- Converters:
 - we have two types of converters: Converter-in and Converter-out
 - both of them can convert from magnitude to 2nd complement and vice-versa
 - Converter-in prevents -0 from entering to the adder to avoid errors, as adder will handle it as if it was -4.
 - Converter-out is simpler, as there will be no -0 in output to convert, it has only two gates to convert from 2nd complement to magnitude
 - Both two inputs A and B are converted.
- Input-Output
 - There is one selector “Subtraction Selector” or S0
 - to add numbers S0=0, to toggle to subtraction S0=1 so B is flipped
 - both Multiplication and Add/Sub Units run at the same time



•Output is 9 leds, only one is for E.F of Add/Sub

This Picture Shows different parts of the AU

- 1- POWER**
- 2- MULTIPLICATION UNIT**
- 3- CONVERTERS**
- 4- ADD/SUB UNIT**
- 5- INPUT**

V. Components

- 2 units of 4-Bit Adder sn74s283
- 3 XOR 7486ls
- 2 AND 7408
- 1 NOR 7402
- 1 OR 7432

Total number of IC's is 9

Total Cost (including used and un-used wires + breadboard) is 310 EGP

VI. Power

we used the provided kit to avoid the problems of power

VII. Test Cases

Every time we finish a unit we test it against all possible cases