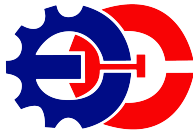


Hysteresis on Comparator

TE201414 - Rangkaian Elektronik 2

Program Studi Teknik Elektro

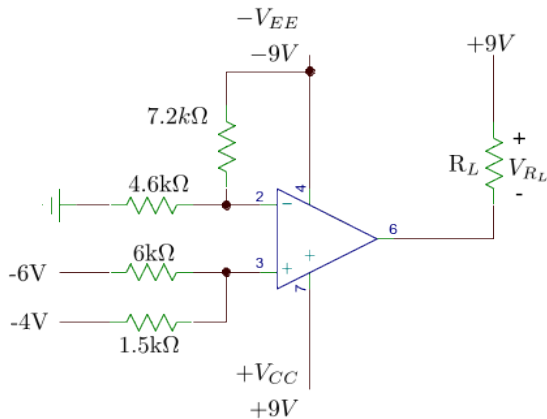


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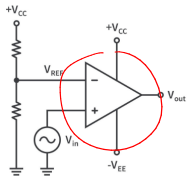
February 24, 2025

Posttest

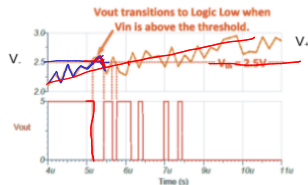
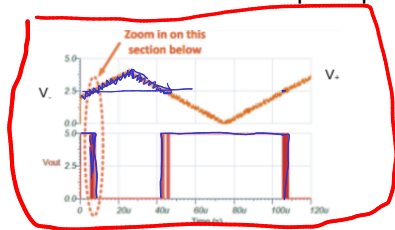
Find the voltage on Load Resistor V_{R_L}



Hysteresis



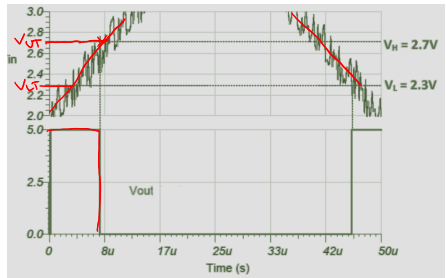
what if noise occurred on input op-amp?



it will result unwanted output voltage signal

Hysteresis

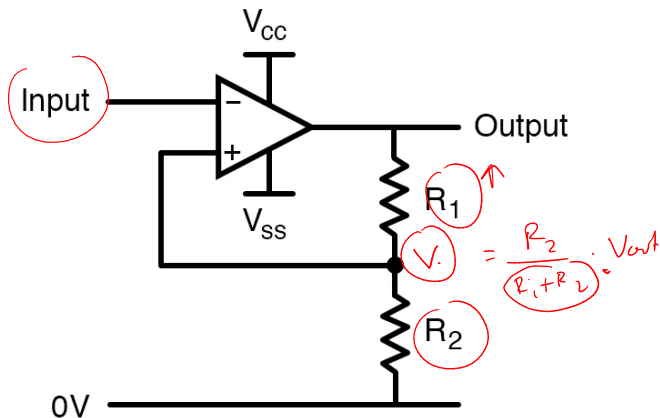
How to overcome this problem? by defining 2 threshold (Lower Threshold and Upper Threshold) the unwanted signal can be eliminated.



then, how is the circuit?

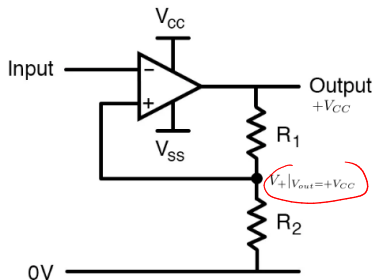
Hysteresis on op-amp

by adding a connection between output and non-inverting input. the comparator circuit has 2 threshold.



Hysteresis on op-amp

while $V_{out} = +V_{CC}$, then



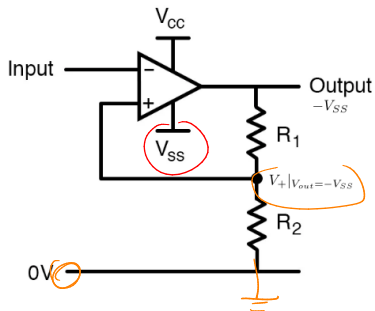
$$V_+|_{V_{out}=+V_{CC}} = \frac{R_2}{R_1 + R_2} (+V_{CC})$$

$V_+|_{V_{out}=+V_{CC}}$ is the upper threshold voltage V_{UT} , thus

$$V_{UT} = \frac{R_2}{R_1 + R_2} (+V_{CC})$$

Hysteresis on op-amp

while $V_{out} = -V_{SS}$, then

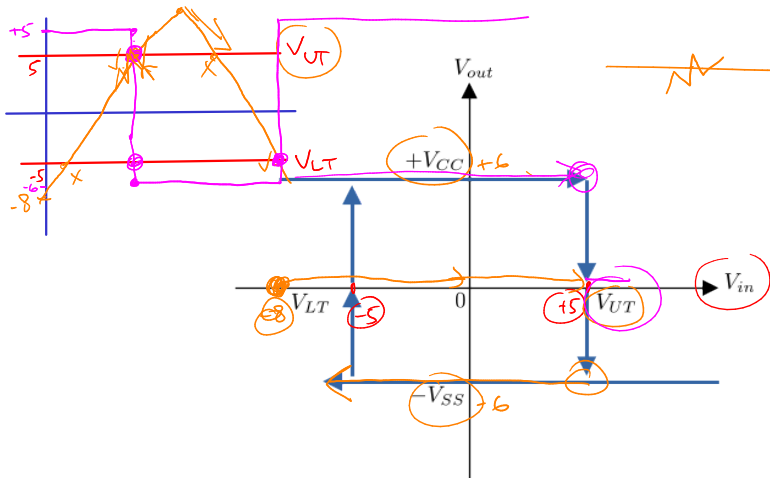


$$V_+|_{V_{out}=-V_{SS}} = \frac{R_2}{R_1 + R_2}(-V_{SS})$$

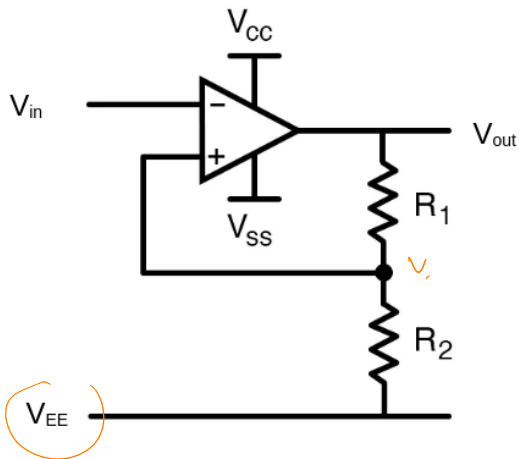
$V_+|_{V_{out}=-V_{SS}}$ is the lower threshold V_{LT} , thus

$$V_{LT} = \frac{R_2}{R_1 + R_2}(-V_{SS})$$

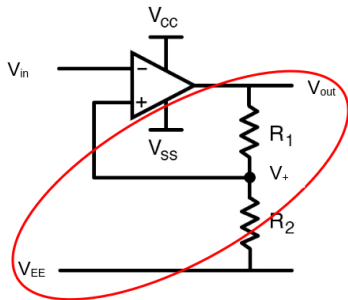
Hysteresis diagram



Hysteresis on op-amp

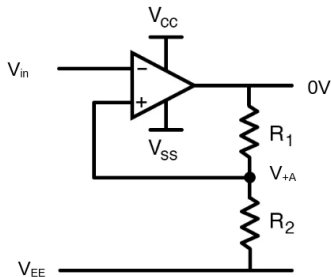


Hysteresis on op-amp



Superposition theorem is used to solve circuit problem with more than 1 sources.

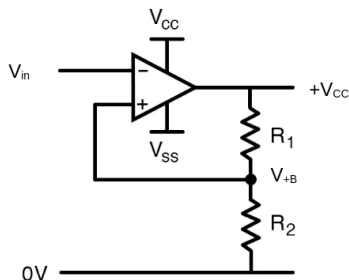
Hysteresis on op-amp



Sumber tegangan V_{out} dimatikan, sehingga:

$$V_{+A} = \frac{R_1}{R_1 + R_2} V_{EE}$$

Hysteresis on op-amp



Sumber tegangan V_{EE} dimatikan,
ketika $V_{out} = +V_{CC}$:

$$V_{+B} = \frac{R_2}{R_1 + R_2} (+V_{CC})$$

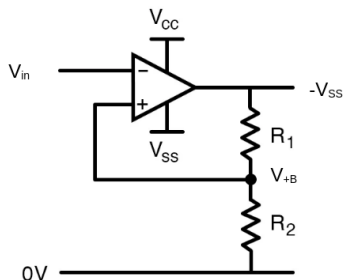
Ambang batas atas V_{UT} :

$$V_{UT} = V_{+A} + V_{+B}$$

$$V_{UT} = \frac{R_1}{R_1 + R_2} (V_{EE}) + \frac{R_2}{R_1 + R_2} (+V_{CC})$$

$$V_{UT} = \frac{R_1(V_{EE}) + R_2(+V_{CC})}{R_1 + R_2}$$

Hysteresis on op-amp



Sumber tegangan V_{EE} dimatikan,
ketika $V_{out} = -V_{SS}$:

$$V_{+B} = \frac{R_2}{R_1 + R_2}(-V_{SS})$$

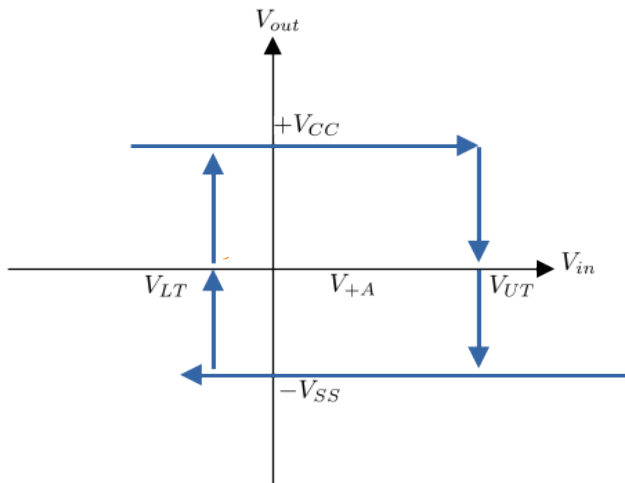
Ambang batas bawah V_{LT} :

$$V_{LT} = V_{+A} + V_{+B}$$

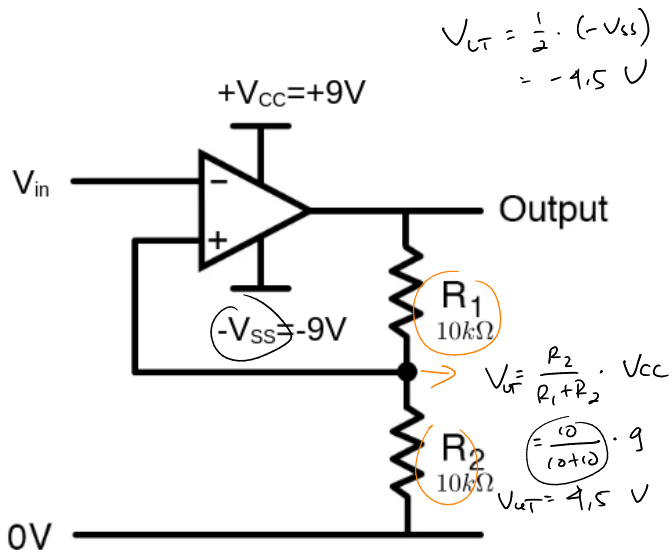
$$V_{LT} = \frac{R_1}{R_1 + R_2}(V_{EE}) + \frac{R_2}{R_1 + R_2}(-V_{SS})$$

$$V_{LT} = \frac{R_1(V_{EE}) + R_2(-V_{SS})}{R_1 + R_2}$$

Diagram Histerisis



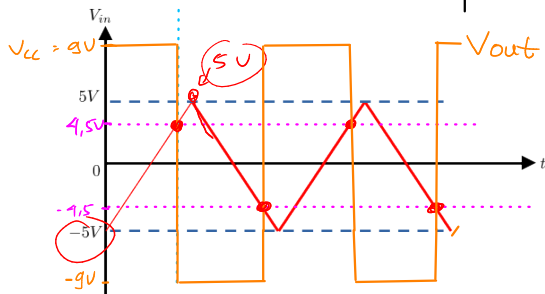
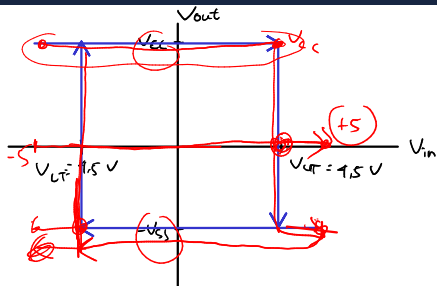
Contoh



Contoh

Tentukan:

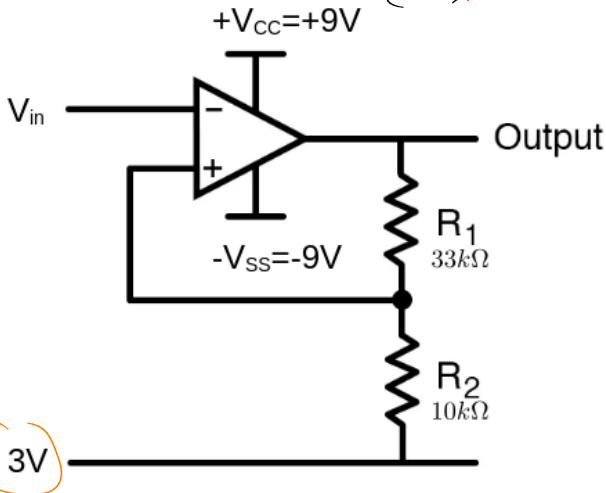
- ✓ • $V_{UT} = 4,5$
- ✓ • $V_{LT} = -4,5$
- ✓ • diagram histerisis
- V_{out} apabila diberikan V_{in}



Contoh

$$V_{UT} = \frac{R_1(V_{EE}) + R_2(+V_{CC})}{R_1 + R_2} = \frac{33k(3) + 10k(9)}{33k + 10k} = \frac{[33(3) + 10(9)]}{(33+10)} = 4.4V$$

V_{LT}



$$V_{LT} = \frac{R_1(V_{EE}) + R_2(-V_{SS})}{R_1 + R_2} = \frac{33k(3) + 10k(-9)}{33k + 10k} = 0.2V$$

Contoh

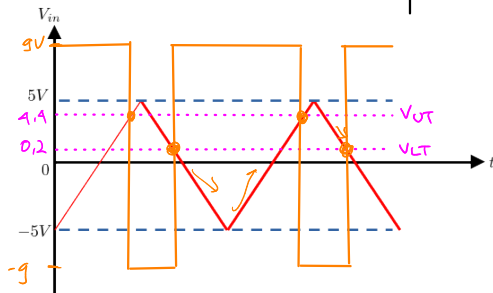
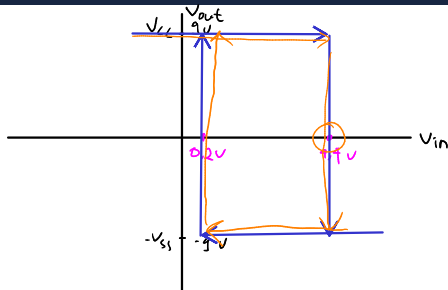
Tentukan:

✓ • $V_{UT} = 4,9 \text{ V}$

✓ • $V_{LT} = 0,2 \text{ V}$

✓ • diagram histerisis

○ • V_{out} apabila diberikan V_{in}



References

Boylestad, R. L., Nashelsky, L., Electronic Devices and Circuit Theory, Pearson, 2014.

Malvino, A., Bates, D., Electronic Principles, McGraw-Hill Education, 2016.

Terima Kasih