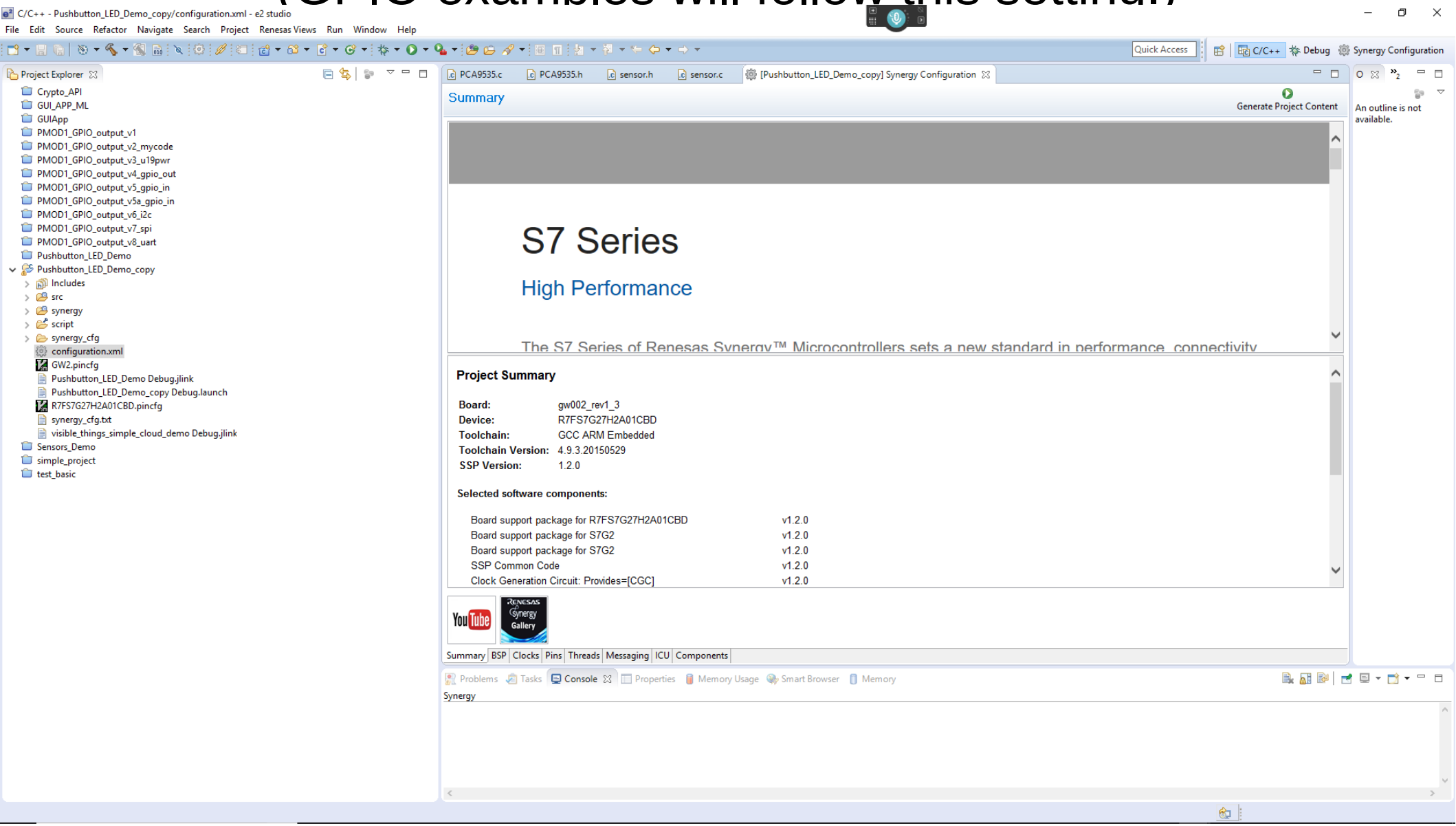
Purpose : Determine why the RTOS version of the GPIO example is hard to build

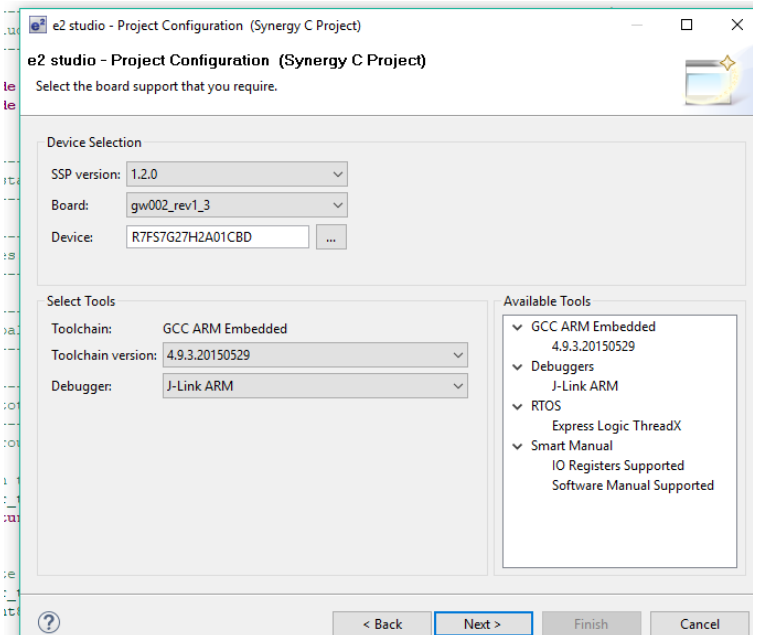
By Michael Li
03/28/2018

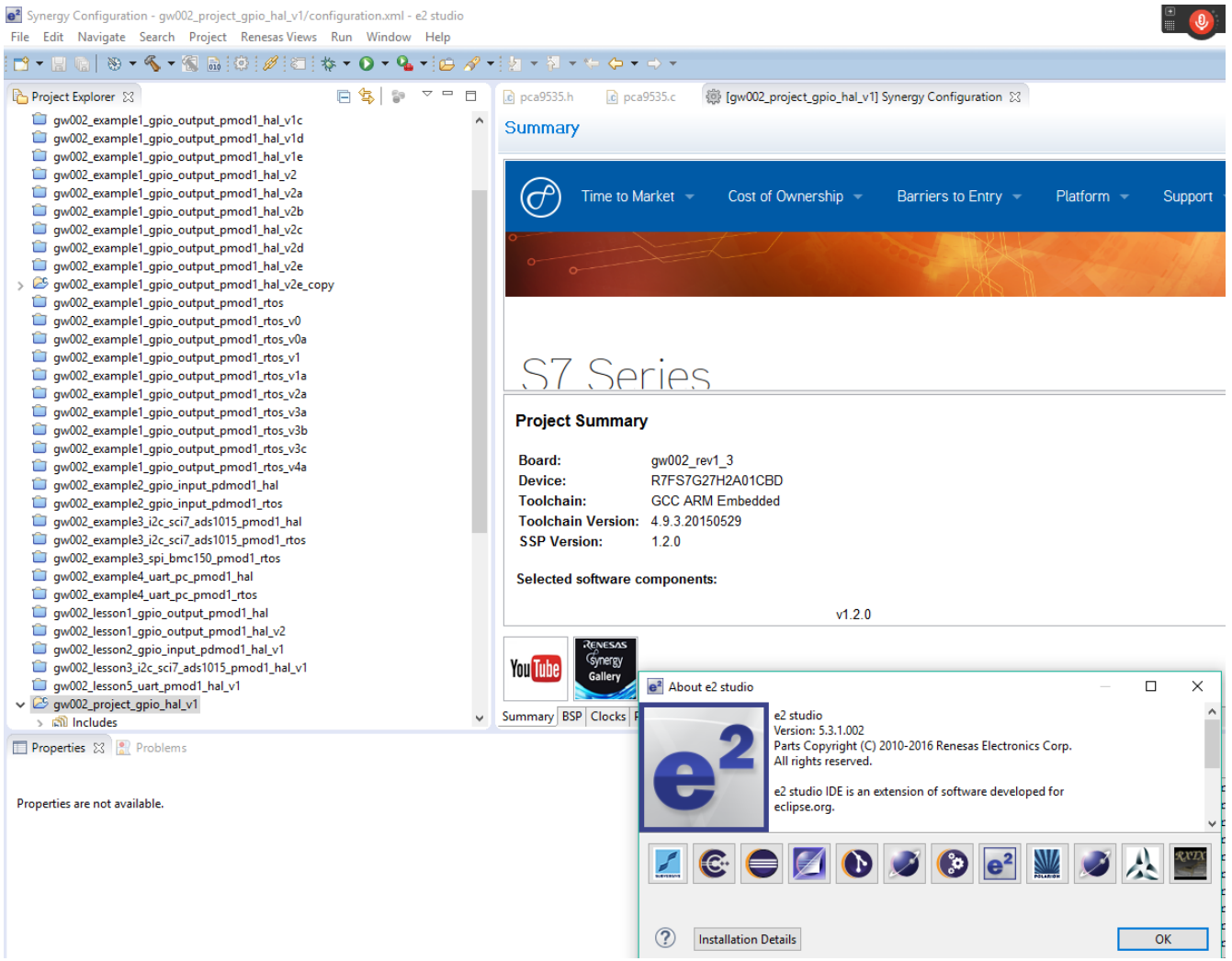
Demo Project Setting

(GPIO examples will follow this setting.)

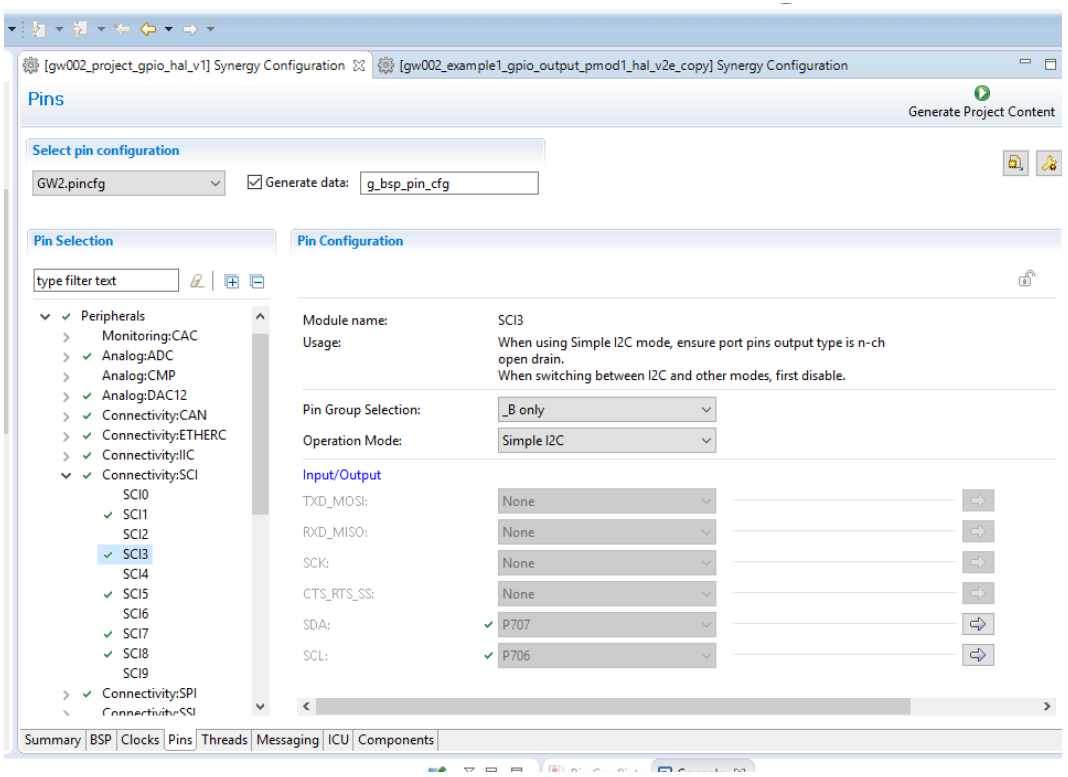


HAL

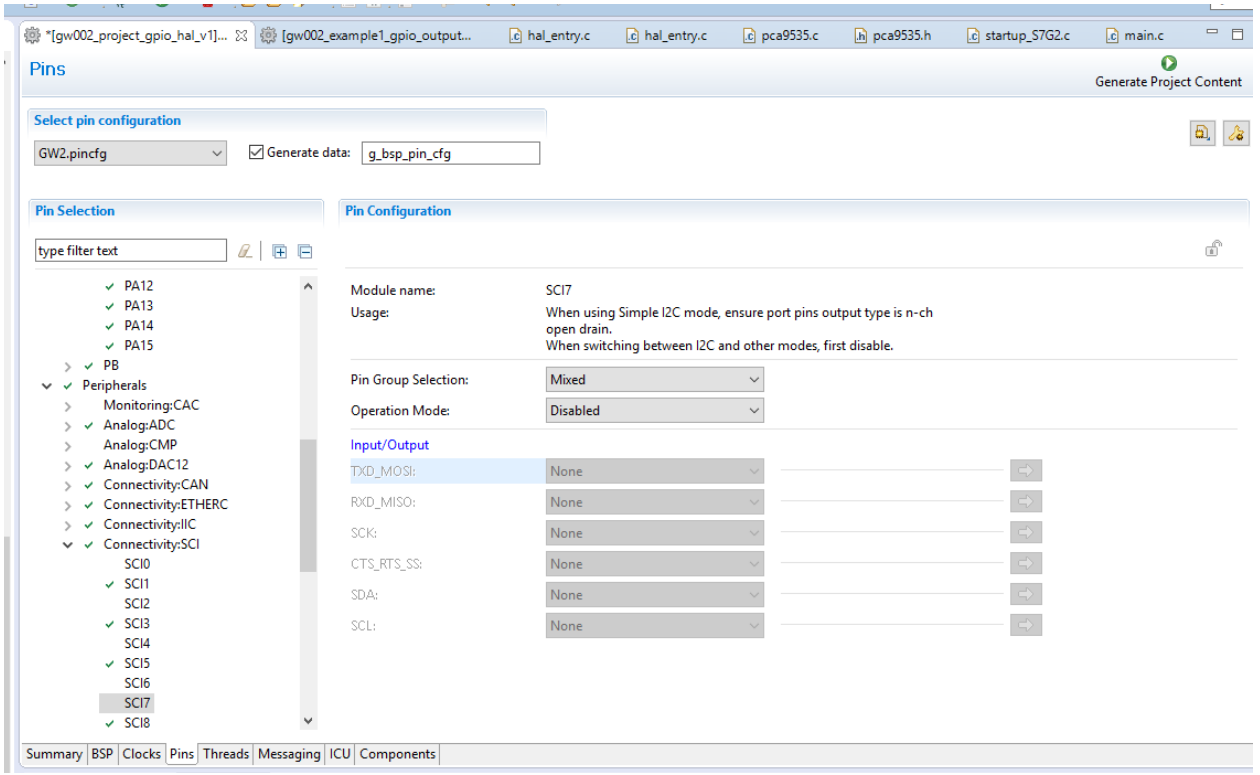

e2 studio - Project Configuration (Synergy C Project)
e2 studio - Project Configuration (Synergy C Project)
Select the board support that you require.
Device Selection
SSP version: 1.2.0
Board: gw002_rev1_3
Device: R7FS7G27H2A01CBD
...
Select Tools
Toolchain: GCC ARM Embedded
Toolchain version: 4.9.3.20150529
Debugger: J-Link ARM
Available Tools
GCC ARM Embedded
4.9.3.20150529
Debuggers
J-Link ARM
RTOS
Express Logic ThreadX
Smart Manual
IO Registers Supported
Software Manual Supported
< Back
Next >
Finish
Cancel


Synergy Configuration - gw002_project_gpio_hal_v1/configuration.xml - e2 studio
File Edit Navigate Search Project Renesas Views Run Window Help
Project Explorer
gw002_example1_gpio_output_pmod1_hal_v1c
gw002_example1_gpio_output_pmod1_hal_v1d
gw002_example1_gpio_output_pmod1_hal_v1e
gw002_example1_gpio_output_pmod1_hal_v2
gw002_example1_gpio_output_pmod1_hal_v2a
gw002_example1_gpio_output_pmod1_hal_v2b
gw002_example1_gpio_output_pmod1_hal_v2c
gw002_example1_gpio_output_pmod1_hal_v2d
gw002_example1_gpio_output_pmod1_hal_v2e
gw002_example1_gpio_output_pmod1_hal_v2e_copy
gw002_example1_gpio_output_pmod1_rtos
gw002_example1_gpio_output_pmod1_rtos_v0
gw002_example1_gpio_output_pmod1_rtos_v0a
gw002_example1_gpio_output_pmod1_rtos_v1
gw002_example1_gpio_output_pmod1_rtos_v1a
gw002_example1_gpio_output_pmod1_rtos_v2a
gw002_example1_gpio_output_pmod1_rtos_v3a
gw002_example1_gpio_output_pmod1_rtos_v3b
gw002_example1_gpio_output_pmod1_rtos_v3c
gw002_example1_gpio_output_pmod1_rtos_v4a
gw002_example2_gpio_input_pdmod1_hal
gw002_example2_gpio_input_pdmod1_rtos
gw002_example3_i2c_sci7_ads1015_pmod1_hal
gw002_example3_i2c_sci7_ads1015_pmod1_rtos
gw002_example3_spi_bmc150_pmod1_rtos
gw002_example4_uart_pc_pmod1_hal
gw002_example4_uart_pc_pmod1_rtos
gw002_lesson1_gpio_output_pmod1_hal
gw002_lesson1_gpio_output_pmod1_hal_v2
gw002_lesson2_gpio_input_pdmod1_hal_v1
gw002_lesson3_i2c_sci7_ads1015_pmod1_hal_v1
gw002_lesson5_uart_pmod1_hal_v1
gw002_project_gpio_hal_v1
Includes
Properties
Problems
Properties are not available.
pca9535.h
pca9535.c
[gw002_project_gpio_hal_v1] Synergy Configuration
Summary
Time to Market
Cost of Ownership
Barriers to Entry
Platform
Support
S7 Series
Project Summary
Board: gw002_rev1_3
Device: R7FS7G27H2A01CBD
Toolchain: GCC ARM Embedded
Toolchain Version: 4.9.3.20150529
SSP Version: 1.2.0
Selected software components:
v1.2.0
Summary
BSP
Clocks
About e2 studio
e2 studio
Version: 5.3.1.002
Parts Copyright (C) 2010-2016 Renesas Electronics Corp.
All rights reserved.
e2 studio IDE is an extension of software developed for eclipse.org.
Installation Details
OK

Pin Configuration



Disable SCI7



PMOD1: PA05/4/3/2, P400 GPIO Output Mode

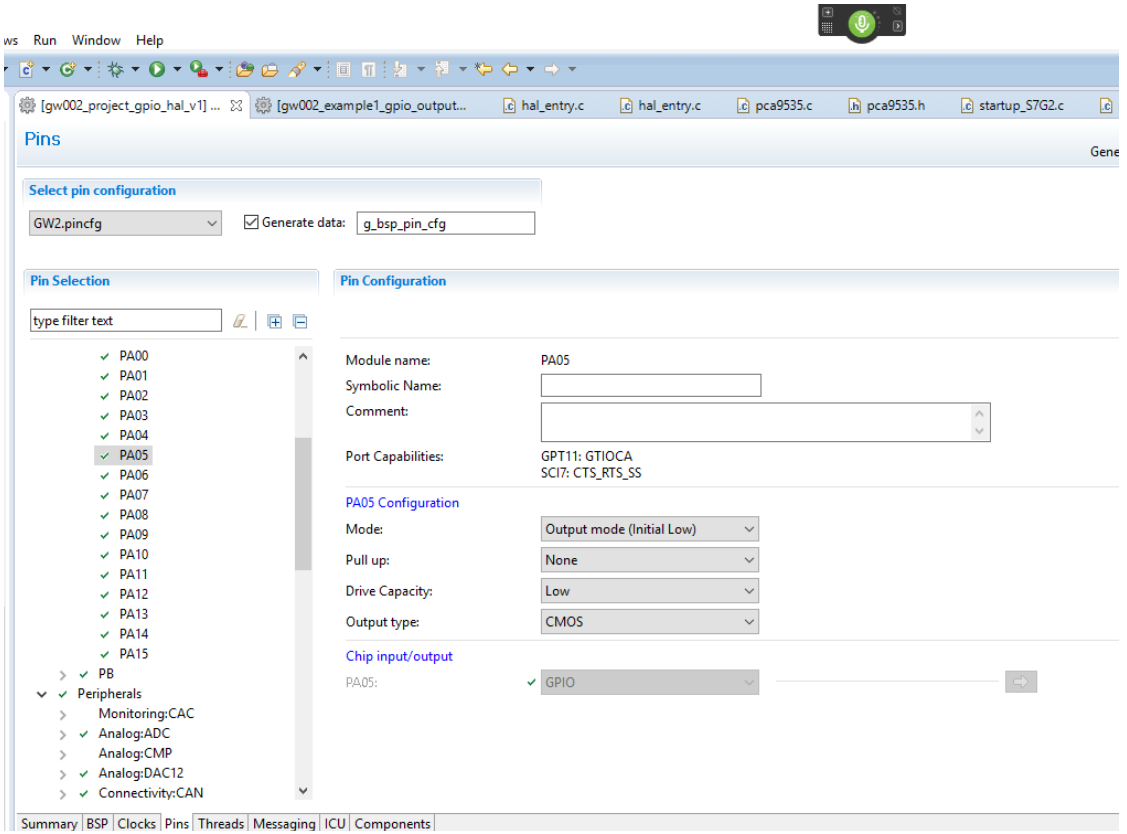


Table 6 – Pmod1 UART Type 4A and SPI Type 2A Pin Connections

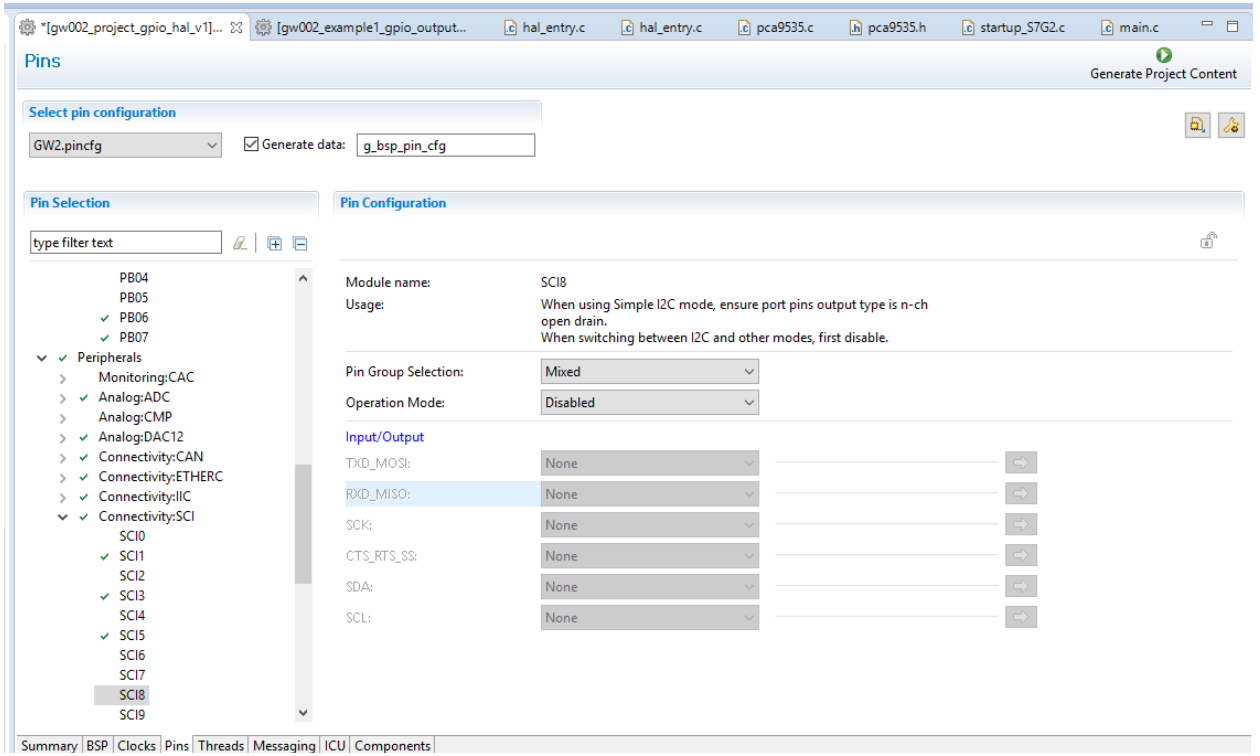
GPIO Type 1 Pmods

If clearance is not an issue, two GPIO Type 1 standard Pmods can be used together when the connector is configured in UART/SPI Comms Mode. **Do not turn a second Type 1 Pmod upside down to get it to fit! Damage may occur as a result of inserting a Pmod upside down!**

	Pmod		S7G2	
	Pin	Pin Function	Port Pin	Pin Function
Upper Row	1	GPIO	PA05	GPIO
	2	GPIO	PA02	GPIO
	3	GPIO	PA03	GPIO
	4	GPIO	PA04	GPIO
	5	GND	GND	GND
	6	VCC (3.3V)	VCC (3.3V)	VCC (3.3V)
Lower Row	1	GPIO	P400	GPIO
	2	GPIO	I/O Expander	GPIO
	3	GPIO	I/O Expander	GPIO
	4	GPIO	I/O Expander	GPIO
	5	GND	GND	GND
	6	VCC (3.3V)	VCC (3.3V)	VCC (3.3V)

Table 7 – Pmod1 GPIO Type 1 Pin Connections (UART/SPI Mode)

Disable SCI8



PMOD2:
PB05/4/3/2, GPIO Output Mode.
P001 : GPIO Input Mode (Output Mode is not available)

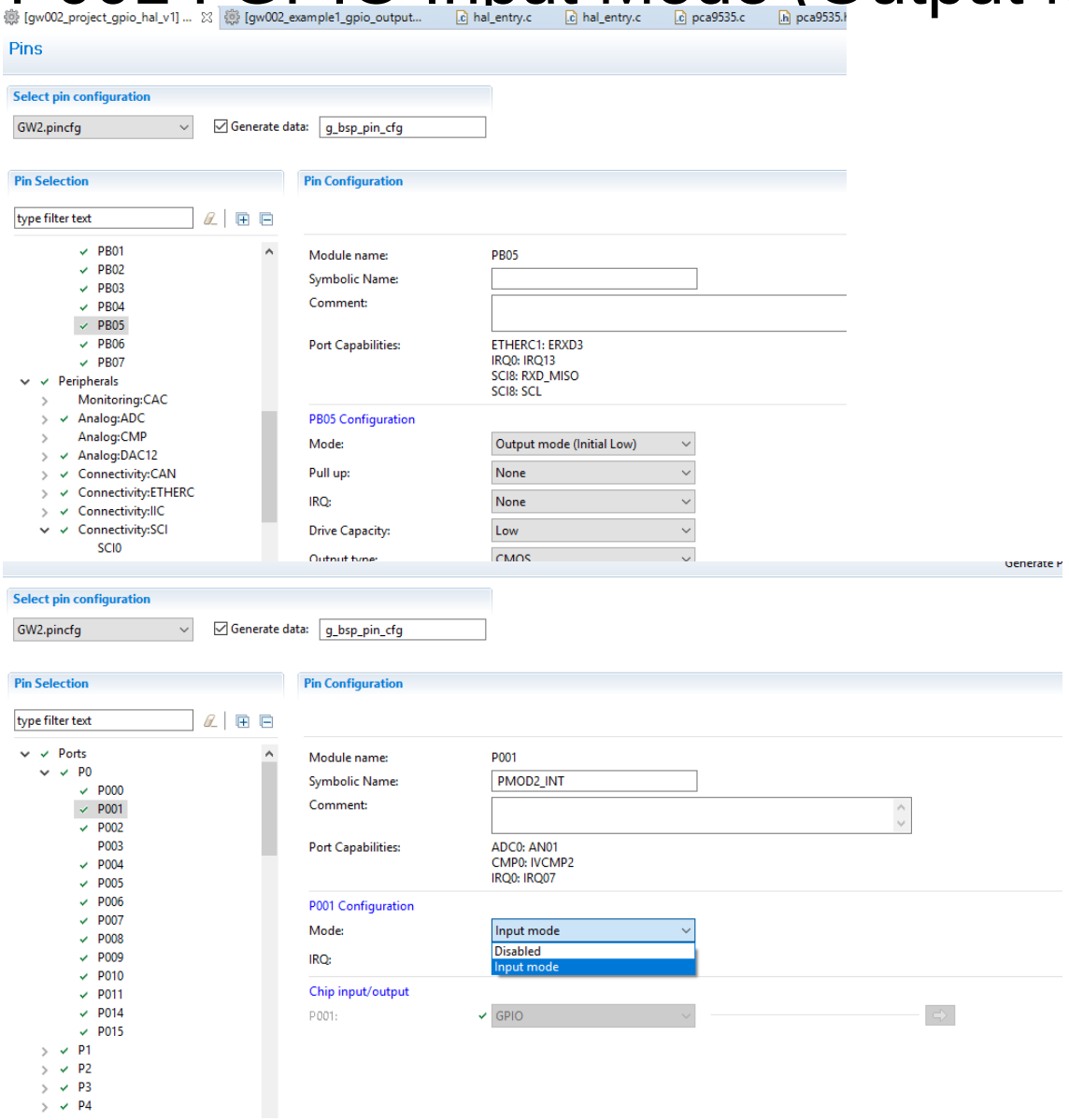


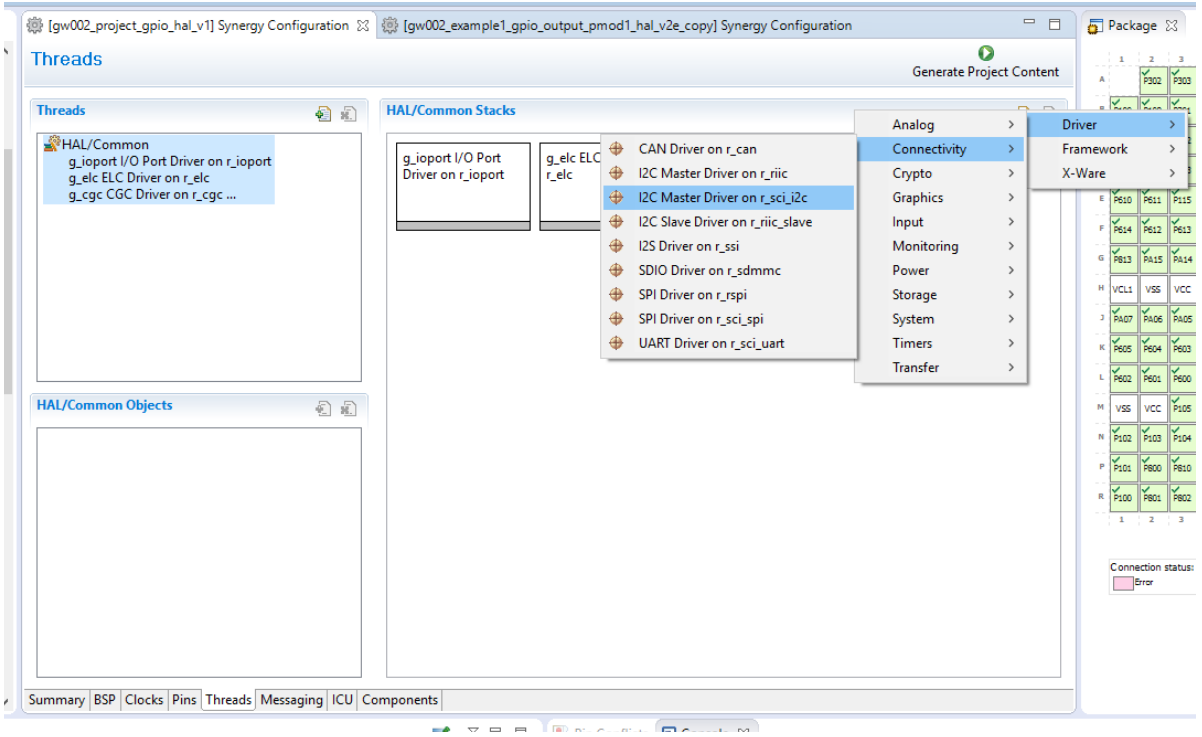
Table 13 – Pmod2 UART Type 4A and SPI Type 2A Pin Connections

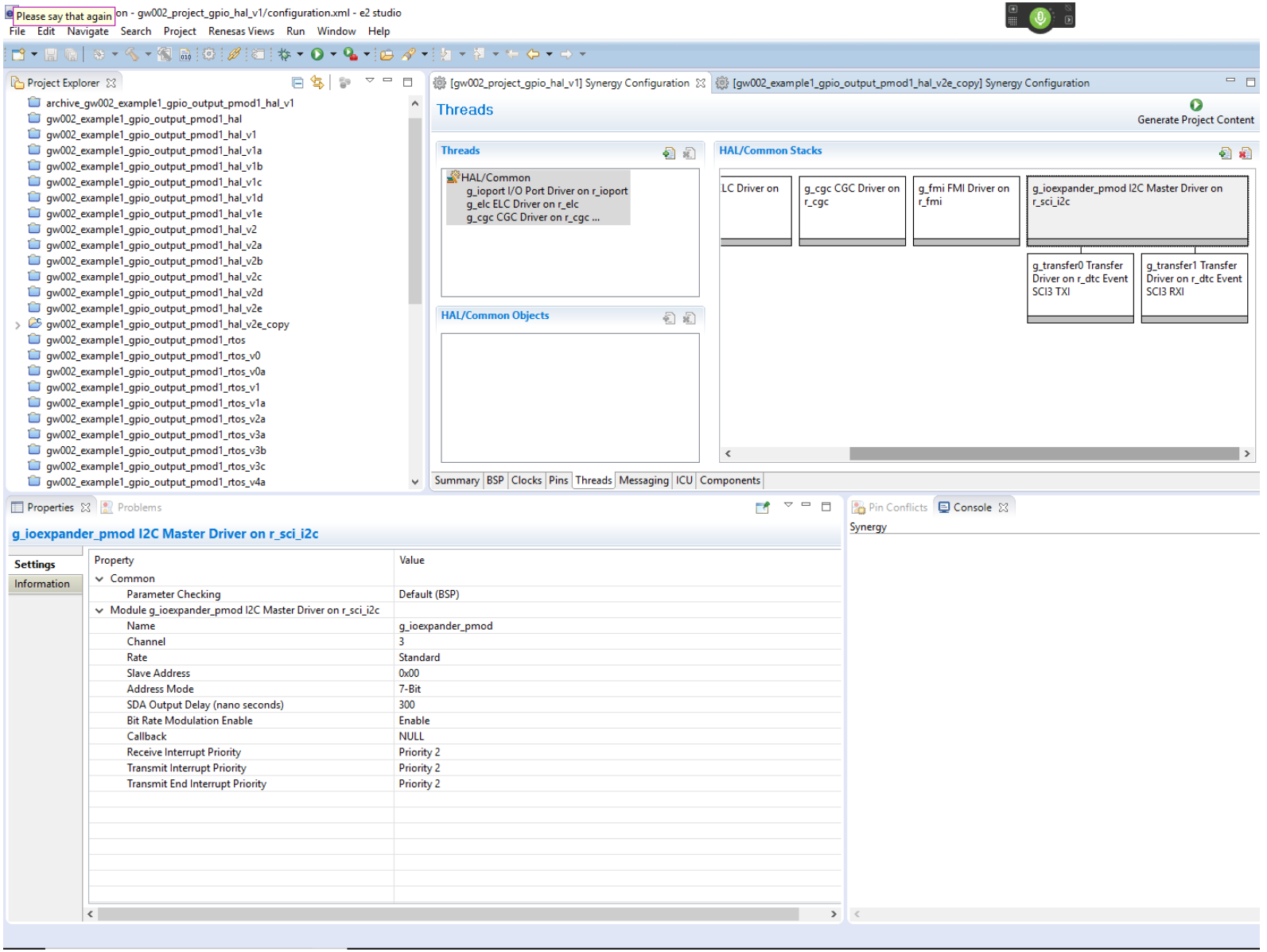
GPIO Type 1 Pmods

If clearance is not an issue, two GPIO Type 1 standard Pmods can be used together when the connector is configured in UART/SPI Comms Mode. **Do not turn a second Type 1 Pmod upside down to get it to fit! Damage may occur as a result of inserting a Pmod upside down!**

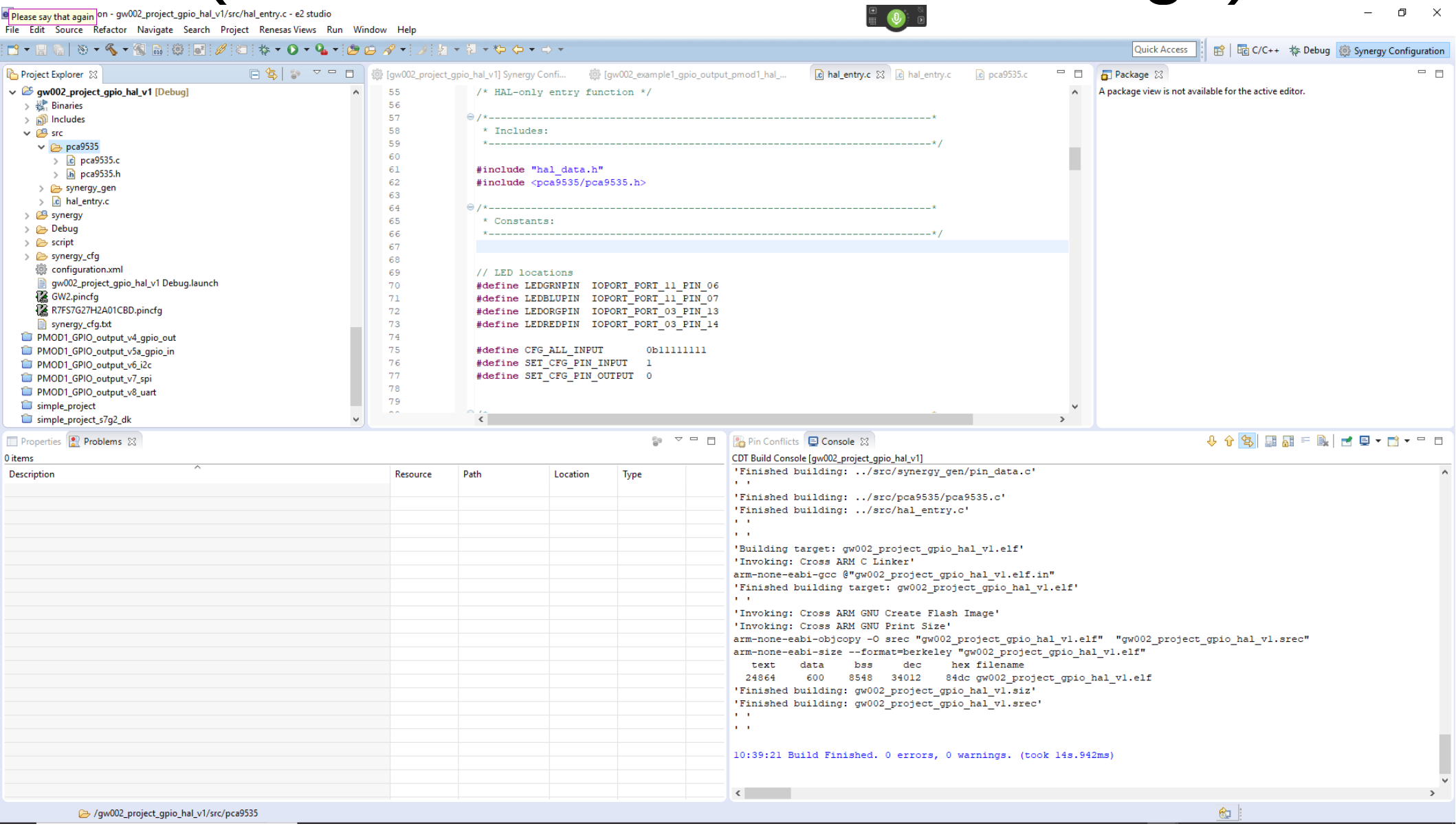
	Pmod		S7G2	
	Pin	Pin Function	Port Pin	Pin Function
Upper Row	1	GPIO	PB02	GPIO
	2	GPIO	PB04	GPIO
	3	GPIO	PB05	GPIO
	4	GPIO	PB03	GPIO
	5	GND	GND	GND
	6	VCC (3.3V)	VCC (3.3V)	VCC (3.3V)
Lower Row	1	GPIO	P001	GPIO
	2	GPIO	I/O Expander	GPIO
	3	GPIO	I/O Expander	GPIO
	4	GPIO	I/O Expander	GPIO
	5	GND	GND	GND
	6	VCC (3.3V)	VCC (3.3V)	VCC (3.3V)

Table 14 – Pmod2 GPIO Type 1 Pin Connections (SPI/UART Mode)

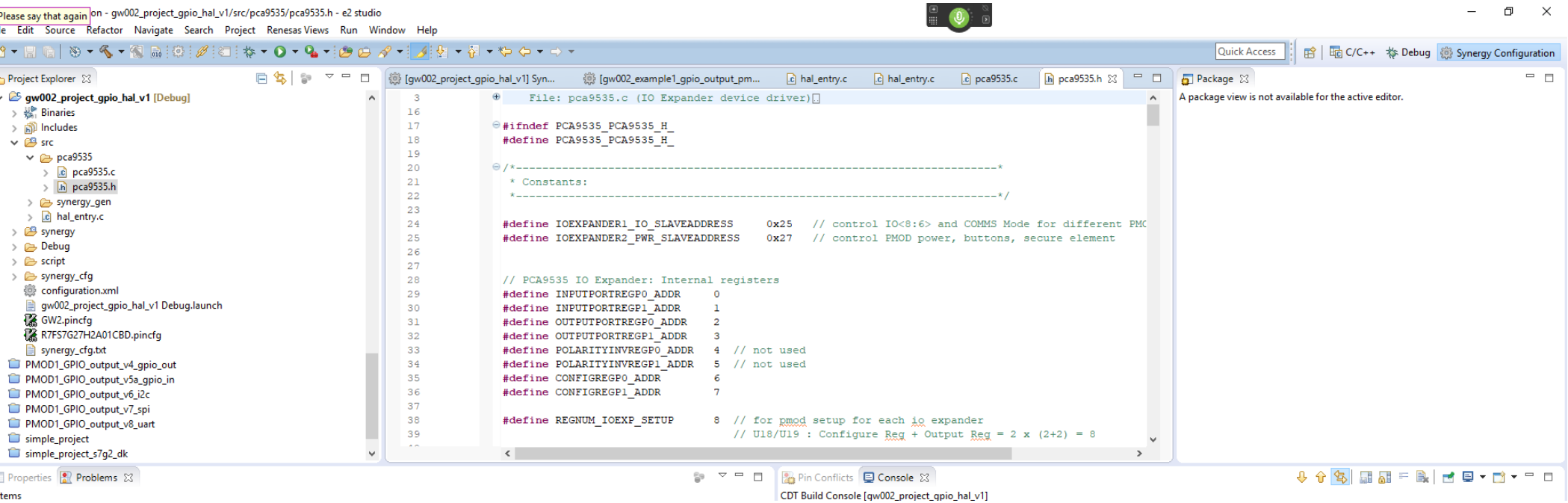

[gw002_project_gpio_hal_v1] Synergy Configuration
[gw002_example1_gpio_output_pmod1_hal_v2e_copy] Synergy Configuration
Package
Threads
Generate Project Content
Threads
HAL/Common
g_ioport I/O Port Driver on r_ioport
g_elc ELC Driver on r_elc
g_cgc CGC Driver on r_cgc ...
HAL/Common Stacks
g_ioport I/O Port Driver on r_ioport
g_elc ELC r_elc
HAL/Common Objects
CAN Driver on r_can
I2C Master Driver on r_riic
I2C Master Driver on r_sci_i2c
I2C Slave Driver on r_riic_slave
I2S Driver on r_ssi
SDIO Driver on r_sdmmc
SPI Driver on r_rspi
SPI Driver on r_sci_spi
UART Driver on r_sci_uart
Analog
Connectivity
Crypto
Graphics
Input
Monitoring
Power
Storage
System
Timers
Transfer
Driver
Framework
X-Ware
Summary
BSP
Clocks
Pins
Threads
Messaging
ICU
Components
Connection status:
Error

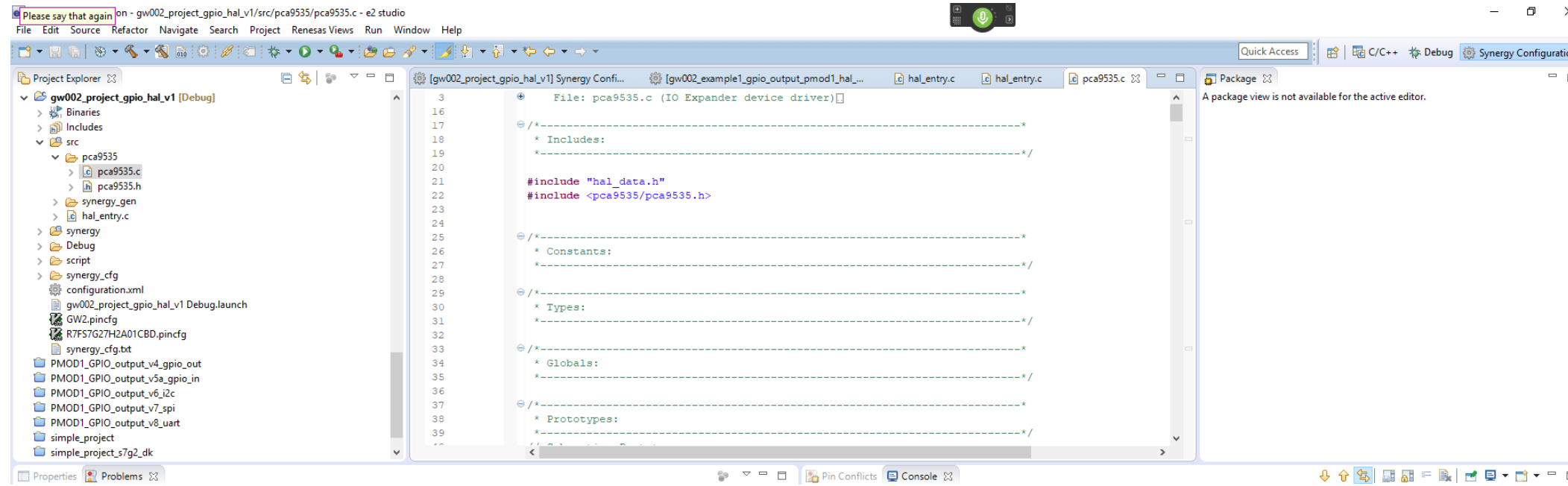

Please say that again
on - gw002_project_gpio_hal_v1/configuration.xml - e2 studio
File Edit Navigate Search Project Renesas Views Run Window Help
Project Explorer
archive_gw002_example1_gpio_output_pmod1_hal_v1
gw002_example1_gpio_output_pmod1_hal
gw002_example1_gpio_output_pmod1_hal_v1
gw002_example1_gpio_output_pmod1_hal_v1a
gw002_example1_gpio_output_pmod1_hal_v1b
gw002_example1_gpio_output_pmod1_hal_v1c
gw002_example1_gpio_output_pmod1_hal_v1d
gw002_example1_gpio_output_pmod1_hal_v1e
gw002_example1_gpio_output_pmod1_hal_v2
gw002_example1_gpio_output_pmod1_hal_v2a
gw002_example1_gpio_output_pmod1_hal_v2b
gw002_example1_gpio_output_pmod1_hal_v2c
gw002_example1_gpio_output_pmod1_hal_v2d
gw002_example1_gpio_output_pmod1_hal_v2e
gw002_example1_gpio_output_pmod1_hal_v2e_copy
gw002_example1_gpio_output_pmod1_rtos
gw002_example1_gpio_output_pmod1_rtos_v0
gw002_example1_gpio_output_pmod1_rtos_v0a
gw002_example1_gpio_output_pmod1_rtos_v1
gw002_example1_gpio_output_pmod1_rtos_v1a
gw002_example1_gpio_output_pmod1_rtos_v2a
gw002_example1_gpio_output_pmod1_rtos_v3a
gw002_example1_gpio_output_pmod1_rtos_v3b
gw002_example1_gpio_output_pmod1_rtos_v3c
gw002_example1_gpio_output_pmod1_rtos_v4a
[gw002_project_gpio_hal_v1] Synergy Configuration
[gw002_example1_gpio_output_pmod1_hal_v2e_copy] Synergy Configuration
Threads
Generate Project Content
Threads
HAL/Common
g_ioport I/O Port Driver on r_ioport
g_elc ELC Driver on r_elc
g_cgc CGC Driver on r_cgc ...
HAL/Common Objects
HAL/Common Stacks
LC Driver on
g_cgc CGC Driver on r_cgc
g_fmi FMI Driver on r_fmi
g_ioexpander_pmod I2C Master Driver on r_sci_i2c
g_transfer0 Transfer Driver on r_dtc Event SCI3 TXI
g_transfer1 Transfer Driver on r_dtc Event SCI3 RXI
Summary BSP Clocks Pins Threads Messaging ICU Components
Properties
Problems
g_ioexpander_pmod I2C Master Driver on r_sci_i2c
Settings
Information
Property
Value
Common
Parameter Checking
Default (BSP)
Module g_ioexpander_pmod I2C Master Driver on r_sci_i2c
Name
g_ioexpander_pmod
Channel
3
Rate
Standard
Slave Address
0x00
Address Mode
7-Bit
SDA Output Delay (nano seconds)
300
Bit Rate Modulation Enable
Enable
Callback
NULL
Receive Interrupt Priority
Priority 2
Transmit Interrupt Priority
Priority 2
Transmit End Interrupt Priority
Priority 2
Pin Conflicts
Console
Synergy

hal_entry.c
(Build: No errors or warnings)

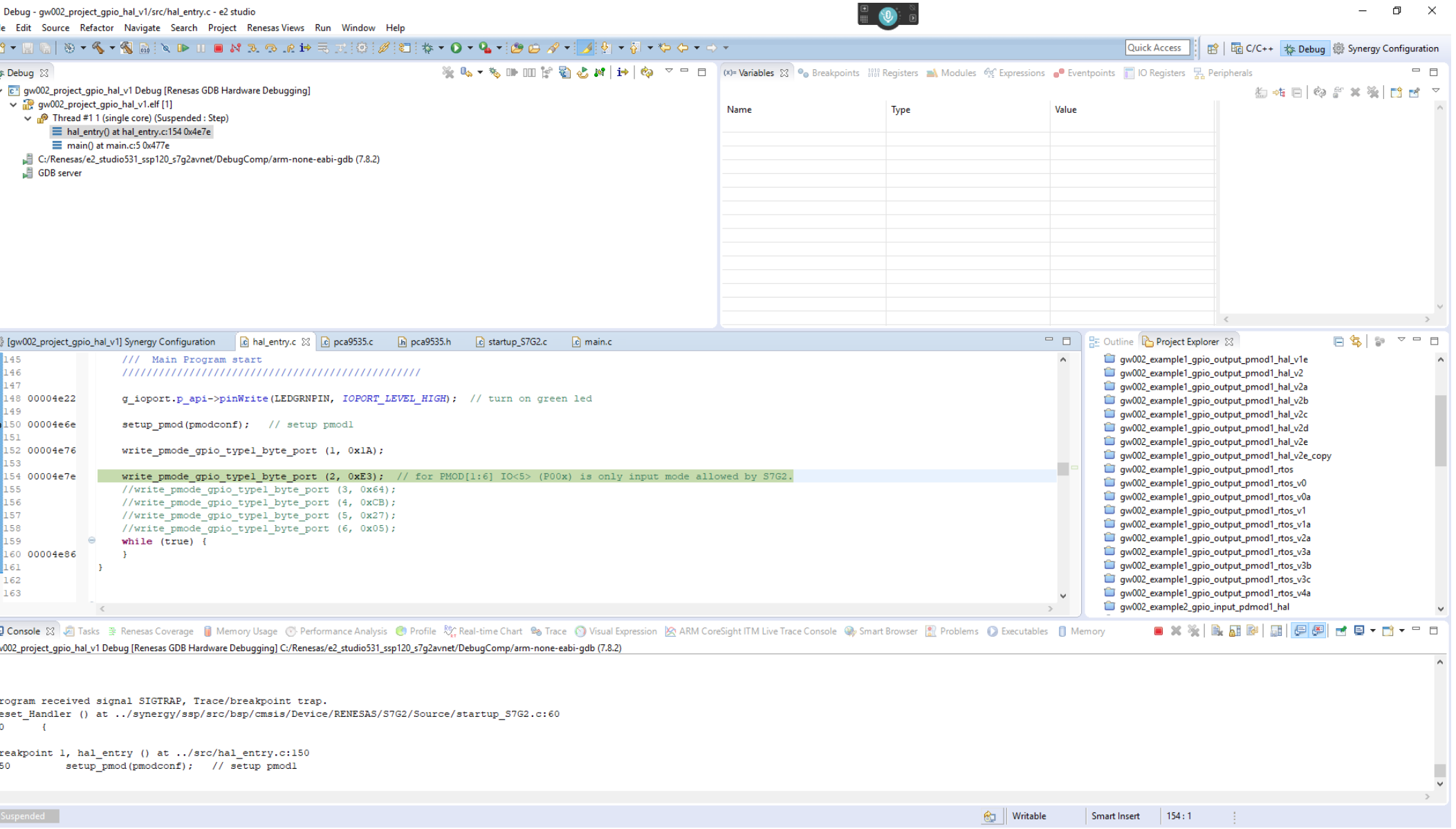


Pca9535.h/c

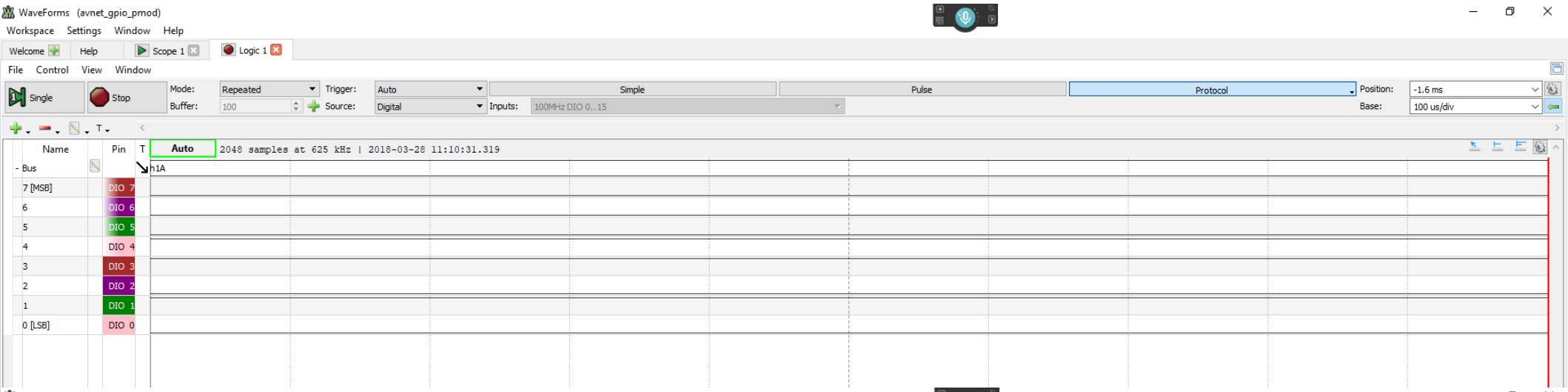

Please say that again
on - gw002_project_gpio_hal_v1/src/pca9535/pca9535.h - e2 studio
e Edit Source Refactor Navigate Search Project Renesas Views Run Window Help
Quick Access
C/C++
Debug
Synergy Configuration
Project Explorer
gw002_project_gpio_hal_v1 [Debug]
Binaries
Includes
src
pca9535
pca9535.c
pca9535.h
synergy_gen
hal_entry.c
synergy
Debug
script
synergy_cfg
configuration.xml
gw002_project_gpio_hal_v1 Debug.launch
GW2.pincfg
R7FS7G27H2A01CBD.pincfg
synergy_cfg.txt
PMOD1_GPIO_output_v4_gpio_out
PMOD1_GPIO_output_v5a_gpio_in
PMOD1_GPIO_output_v6_i2c
PMOD1_GPIO_output_v7_spi
PMOD1_GPIO_output_v8_uart
simple_project
simple_project_s7g2_dk
[gw002_project_gpio_hal_v1] Syn...
[gw002_example1_gpio_output_pm...
hal_entry.c
hal_entry.c
pca9535.c
pca9535.h
3 File: pca9535.c (IO Expander device driver)
16
17 #ifndef PCA9535_PCA9535_H_
18 #define PCA9535_PCA9535_H_
19
20 /*----------*
21 * Constants:
22 *----------*/
23
24 #define IOEXPANDER1_IO_SLAVEADDRESS 0x25 // control IO<8:6> and COMMS Mode for different PMC
25 #define IOEXPANDER2_PWR_SLAVEADDRESS 0x27 // control PMOD power, buttons, secure element
26
27
28 // PCA9535 IO Expander: Internal registers
29 #define INPUTPORTREGP0_ADDR 0
30 #define INPUTPORTREGP1_ADDR 1
31 #define OUTPUTPORTREGP0_ADDR 2
32 #define OUTPUTPORTREGP1_ADDR 3
33 #define POLARITYINVREGP0_ADDR 4 // not used
34 #define POLARITYINVREGP1_ADDR 5 // not used
35 #define CONFIGREGP0_ADDR 6
36 #define CONFIGREGP1_ADDR 7
37
38 #define REGNUM_IOEXP_SETUP 8 // for pmod setup for each io expander
39 // U18/U19 : Configure Reg + Output Reg = 2 x (2+2) = 8
Package
A package view is not available for the active editor.
Properties
Problems
Pin Conflicts
Console
CDT Build Console [gw002_project_gpio_hal_v1]

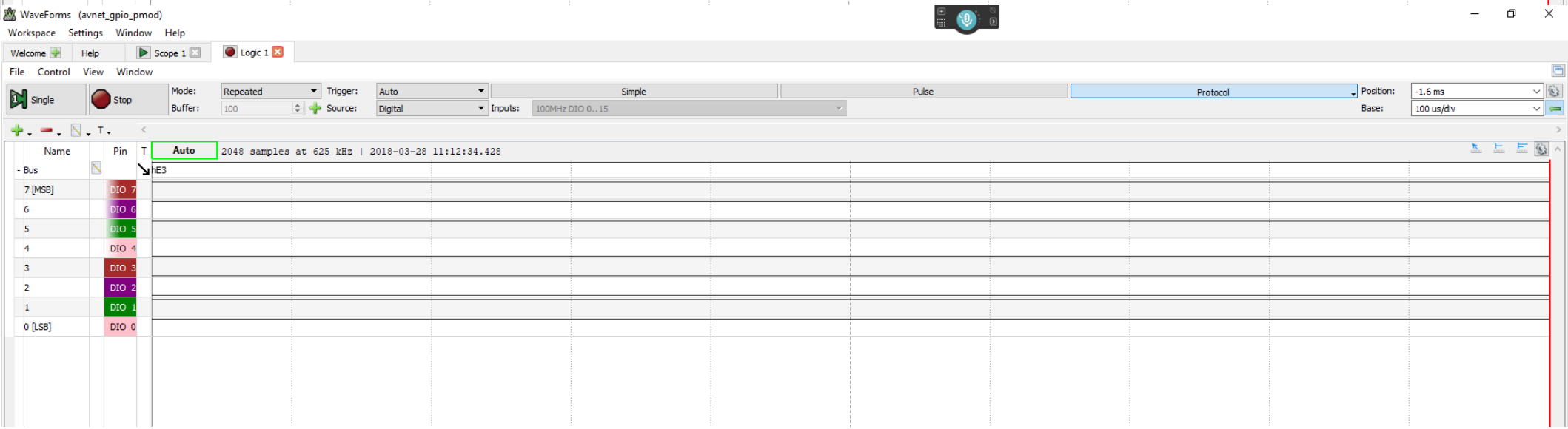

Please say that again
on - gw002_project_gpio_hal_v1/src/pca9535/pca9535.c - e2 studio
File Edit Source Refactor Navigate Search Project Renesas Views Run Window Help
Quick Access
C/C++
Debug
Synergy Configuration
Project Explorer
gw002_project_gpio_hal_v1 [Debug]
Binaries
Includes
src
pca9535
pca9535.c
pca9535.h
synergy_gen
hal_entry.c
synergy
Debug
script
synergy_cfg
configuration.xml
gw002_project_gpio_hal_v1 Debug.launch
GW2.pincfg
R7FS7G27H2A01CBD.pincfg
synergy_cfg.txt
PMOD1_GPIO_output_v4_gpio_out
PMOD1_GPIO_output_v5a_gpio_in
PMOD1_GPIO_output_v6_i2c
PMOD1_GPIO_output_v7_spi
PMOD1_GPIO_output_v8_uart
simple_project
simple_project_s7g2_dk
[gw002_project_gpio_hal_v1] Synergy Confi...
[gw002_example1_gpio_output_pmod1_hal_...
hal_entry.c
hal_entry.c
pca9535.c
3 File: pca9535.c (IO Expander device driver)
16
17 /*----------*
18 * Includes:
19 *----------*/
20
21 #include "hal_data.h"
22 #include <pca9535/pca9535.h>
23
24
25 /*----------*
26 * Constants:
27 *----------*/
28
29 /*----------*
30 * Types:
31 *----------*/
32
33 /*----------*
34 * Globals:
35 *----------*/
36
37 /*----------*
38 * Prototypes:
39 *----------*/
Package
A package view is not available for the active editor.
Properties
Problems
Pin Conflicts
Console

Run

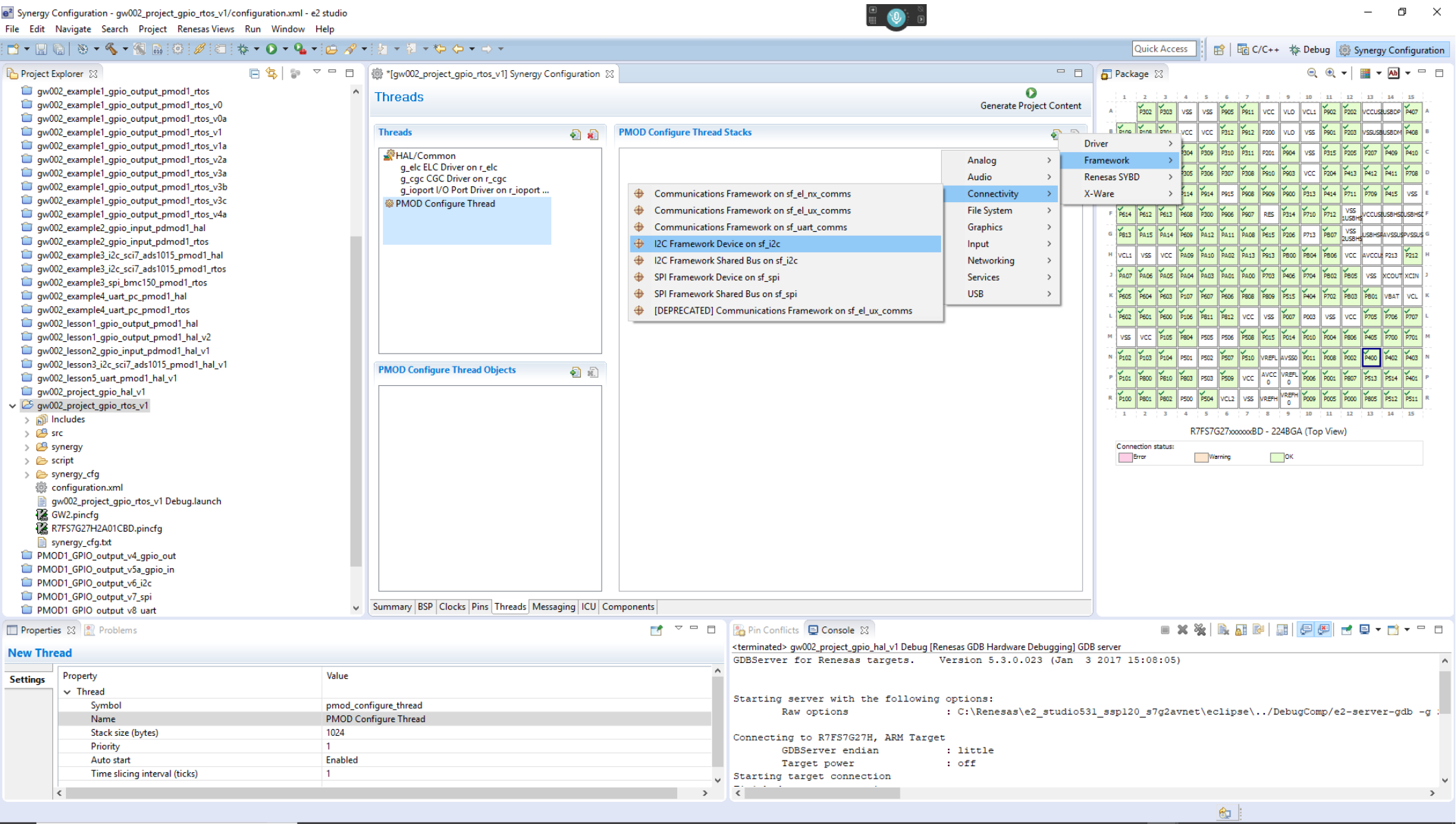

Debug - gw002_project_gpio_hal_v1/src/hal_entry.c - e2 studio
Edit Source Refactor Navigate Search Project Renesas Views Run Window Help
Quick Access
C/C++ Debug Synergy Configuration
Debug
gw002_project_gpio_hal_v1 Debug [Renesas GDB Hardware Debugging]
gw002_project_gpio_hal_v1.elf [1]
Thread #1 1 (single core) (Suspended : Step)
hal_entry() at hal_entry.c:154 0x4e7e
main() at main.c:5 0x477e
C:/Renesas/e2_studio531_ssp120_s7g2avnet/DebugComp/arm-none-eabi-gdb (7.8.2)
GDB server
Variables Breakpoints Registers Modules Expressions Eventpoints IO Registers Peripherals
Name Type Value
[gw002_project_gpio_hal_v1] Synergy Configuration
hal_entry.c
pca9535.c
pca9535.h
startup_S7G2.c
main.c
/// Main Program start
00004e22 g_ioport.p_api->pinWrite(LEDGRNPIN, IOPORT_LEVEL_HIGH); // turn on green led
00004e6e setup_pmod(pmodconf); // setup pmod1
00004e76 write_pmode_gpio_typeI_byte_port (1, 0x1A);
00004e7e write_pmode_gpio_typeI_byte_port (2, 0xE3); // for PMOD[1:6] IO<5> (P00x) is only input mode allowed by S7G2.
//write_pmode_gpio_typeI_byte_port (3, 0x64);
//write_pmode_gpio_typeI_byte_port (4, 0xCB);
//write_pmode_gpio_typeI_byte_port (5, 0x27);
//write_pmode_gpio_typeI_byte_port (6, 0x05);
while (true) {
00004e86 }
}
Outline Project Explorer
gw002_example1_gpio_output_pmod1_hal_v1e
gw002_example1_gpio_output_pmod1_hal_v2
gw002_example1_gpio_output_pmod1_hal_v2a
gw002_example1_gpio_output_pmod1_hal_v2b
gw002_example1_gpio_output_pmod1_hal_v2c
gw002_example1_gpio_output_pmod1_hal_v2d
gw002_example1_gpio_output_pmod1_hal_v2e
gw002_example1_gpio_output_pmod1_hal_v2e_copy
gw002_example1_gpio_output_pmod1_rtos
gw002_example1_gpio_output_pmod1_rtos_v0
gw002_example1_gpio_output_pmod1_rtos_v0a
gw002_example1_gpio_output_pmod1_rtos_v1
gw002_example1_gpio_output_pmod1_rtos_v1a
gw002_example1_gpio_output_pmod1_rtos_v2a
gw002_example1_gpio_output_pmod1_rtos_v3a
gw002_example1_gpio_output_pmod1_rtos_v3b
gw002_example1_gpio_output_pmod1_rtos_v3c
gw002_example1_gpio_output_pmod1_rtos_v4a
gw002_example2_gpio_input_pdmod1_hal
Console Tasks Renesas Coverage Memory Usage Performance Analysis Profile Real-time Chart Trace Visual Expression ARM CoreSight ITM Live Trace Console Smart Browser Problems Executables Memory
v002_project_gpio_hal_v1 Debug [Renesas GDB Hardware Debugging] C:/Renesas/e2_studio531_ssp120_s7g2avnet/DebugComp/arm-none-eabi-gdb (7.8.2)
rogram received signal SIGTRAP, Trace/breakpoint trap.
eset_Handler () at ../synergy/ssp/src/bsp/cmsis/Device/RENESAS/S7G2/Source/startup_S7G2.c:60
0 {
reakpoint 1, hal_entry () at ../src/hal_entry.c:150
50 setup_pmod(pmodconf); // setup pmod1
Suspended
Writable
Smart Insert
154 : 1

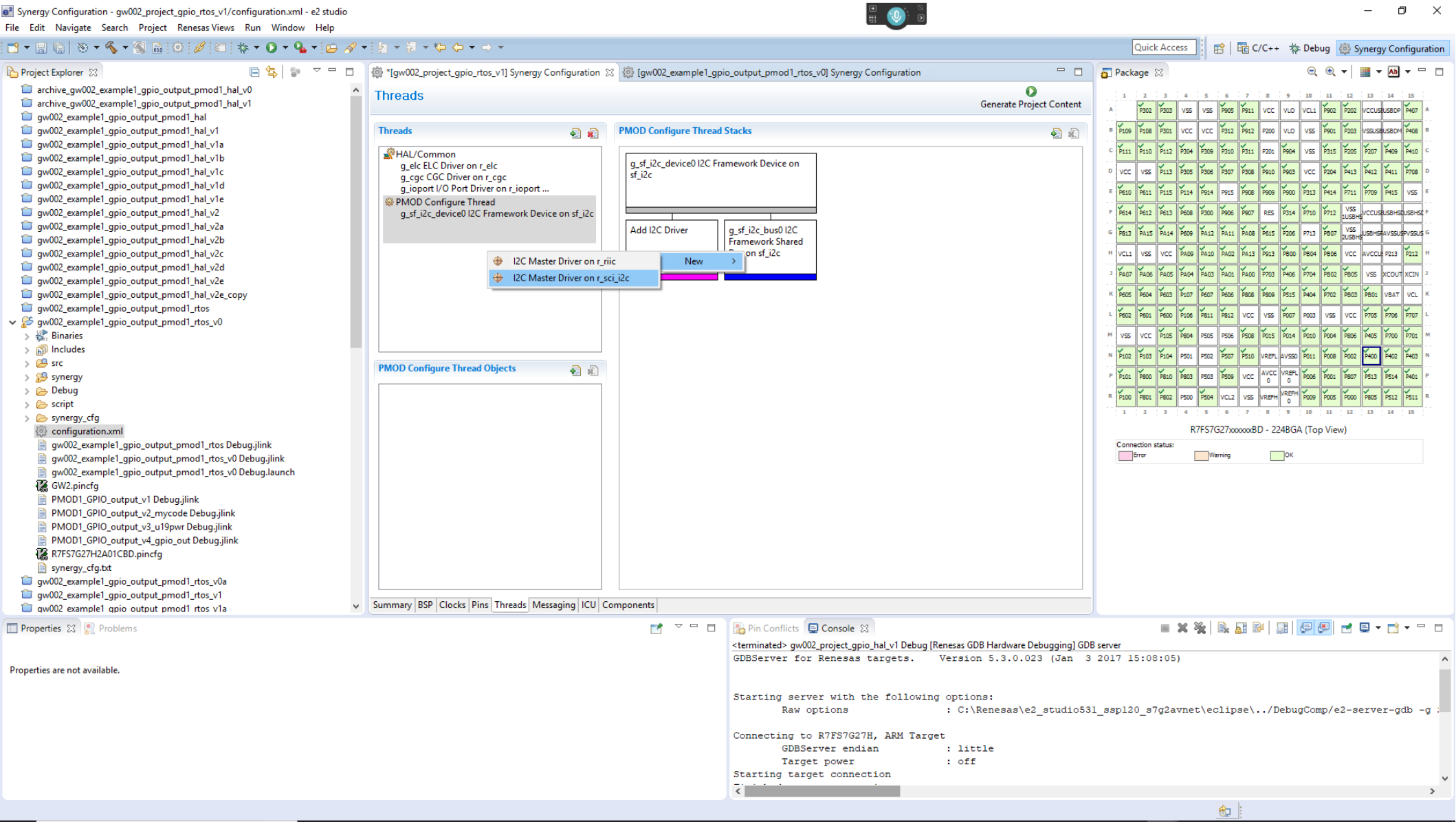
Scope Probing



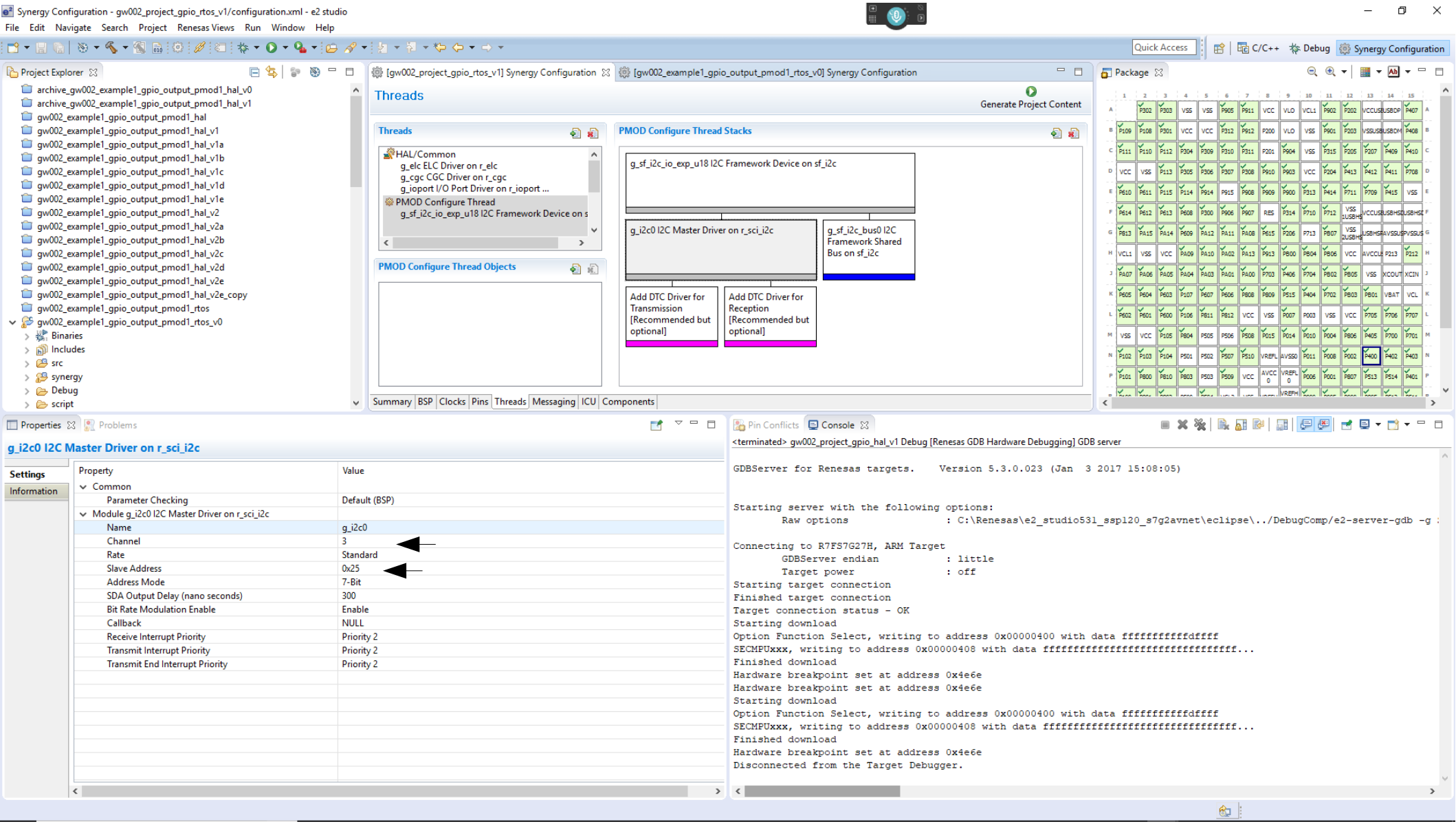


RTOS

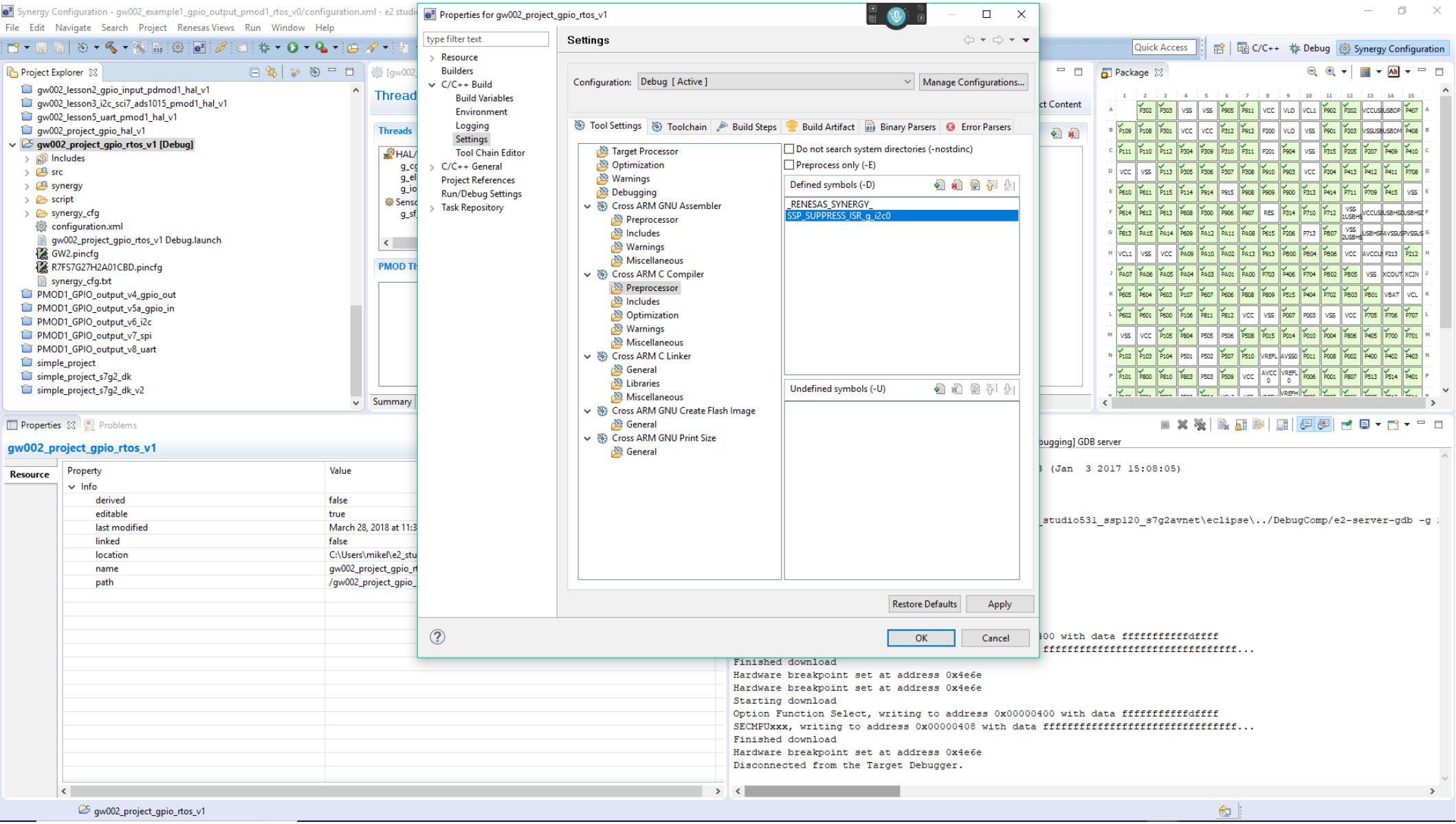

Synergy Configuration - gw002_project_gpio_rtos_v1/configuration.xml - e2 studio
File Edit Navigate Search Project Renesas Views Run Window Help
Quick Access
C/C++ Debug Synergy Configuration
Project Explorer
gw002_example1_gpio_output_pmod1_rtos
gw002_example1_gpio_output_pmod1_rtos_v0
gw002_example1_gpio_output_pmod1_rtos_v0a
gw002_example1_gpio_output_pmod1_rtos_v1
gw002_example1_gpio_output_pmod1_rtos_v1a
gw002_example1_gpio_output_pmod1_rtos_v2a
gw002_example1_gpio_output_pmod1_rtos_v3a
gw002_example1_gpio_output_pmod1_rtos_v3b
gw002_example1_gpio_output_pmod1_rtos_v3c
gw002_example1_gpio_output_pmod1_rtos_v4a
gw002_example2_gpio_input_pdmod1_hal
gw002_example2_gpio_input_pdmod1_rtos
gw002_example3_i2c_sci7_ads1015_pmod1_hal
gw002_example3_i2c_sci7_ads1015_pmod1_rtos
gw002_example3_spi_bmc150_pmod1_rtos
gw002_example4_uart_pc_pmod1_hal
gw002_example4_uart_pc_pmod1_rtos
gw002_lesson1_gpio_output_pmod1_hal
gw002_lesson1_gpio_output_pmod1_hal_v2
gw002_lesson2_gpio_input_pdmod1_hal_v1
gw002_lesson3_i2c_sci7_ads1015_pmod1_hal_v1
gw002_lesson5_uart_pmod1_hal_v1
gw002_project_gpio_hal_v1
gw002_project_gpio_rtos_v1
Includes
src
synergy
script
synergy_cfg
configuration.xml
gw002_project_gpio_rtos_v1 Debug.launch
GW2.pincfg
R7FS7G27H2A01CBD.pincfg
synergy_cfg.txt
PMOD1_GPIO_output_v4_gpio_out
PMOD1_GPIO_output_v5a_gpio_in
PMOD1_GPIO_output_v6_i2c
PMOD1_GPIO_output_v7_spi
PMOD1 GPIO output v8 uart
*[gw002_project_gpio_rtos_v1] Synergy Configuration
Threads
Generate Project Content
Threads
HAL/Common
g_elc ELC Driver on r_elc
g_cgc CGC Driver on r_cgc
g_ioport I/O Port Driver on r_ioport ...
PMOD Configure Thread
PMOD Configure Thread Objects
PMOD Configure Thread Stacks
Driver
Framework
Renesas SYBD
X-Ware
Analog
Audio
Connectivity
File System
Graphics
Input
Networking
Services
USB
Communications Framework on sf_el_nx_comms
Communications Framework on sf_el_ux_comms
Communications Framework on sf_uart_comms
I2C Framework Device on sf_i2c
I2C Framework Shared Bus on sf_i2c
SPI Framework Device on sf_spi
SPI Framework Shared Bus on sf_spi
[DEPRECATED] Communications Framework on sf_el_ux_comms
Summary BSP Clocks Pins Threads Messaging ICU Components
Package
R7FS7G27xxxxxxBD - 224BGA (Top View)
Connection status:
Error
Warning
OK
Properties
Problems
New Thread
Settings
Property
Value
Thread
Symbol
pmod_configure_thread
Name
PMOD Configure Thread
Stack size (bytes)
1024
Priority
1
Auto start
Enabled
Time slicing interval (ticks)
1
Pin Conflicts
Console
<terminated> gw002_project_gpio_hal_v1 Debug [Renesas GDB Hardware Debugging] GDB server
GDBServer for Renesas targets. Version 5.3.0.023 (Jan 3 2017 15:08:05)
Starting server with the following options:
Raw options : C:\Renesas\e2_studio531_ssp120_s7g2avnet\eclipse\../DebugComp/e2-server-gdb -g
Connecting to R7FS7G27H, ARM Target
GDBServer endian : little
Target power : off
Starting target connection

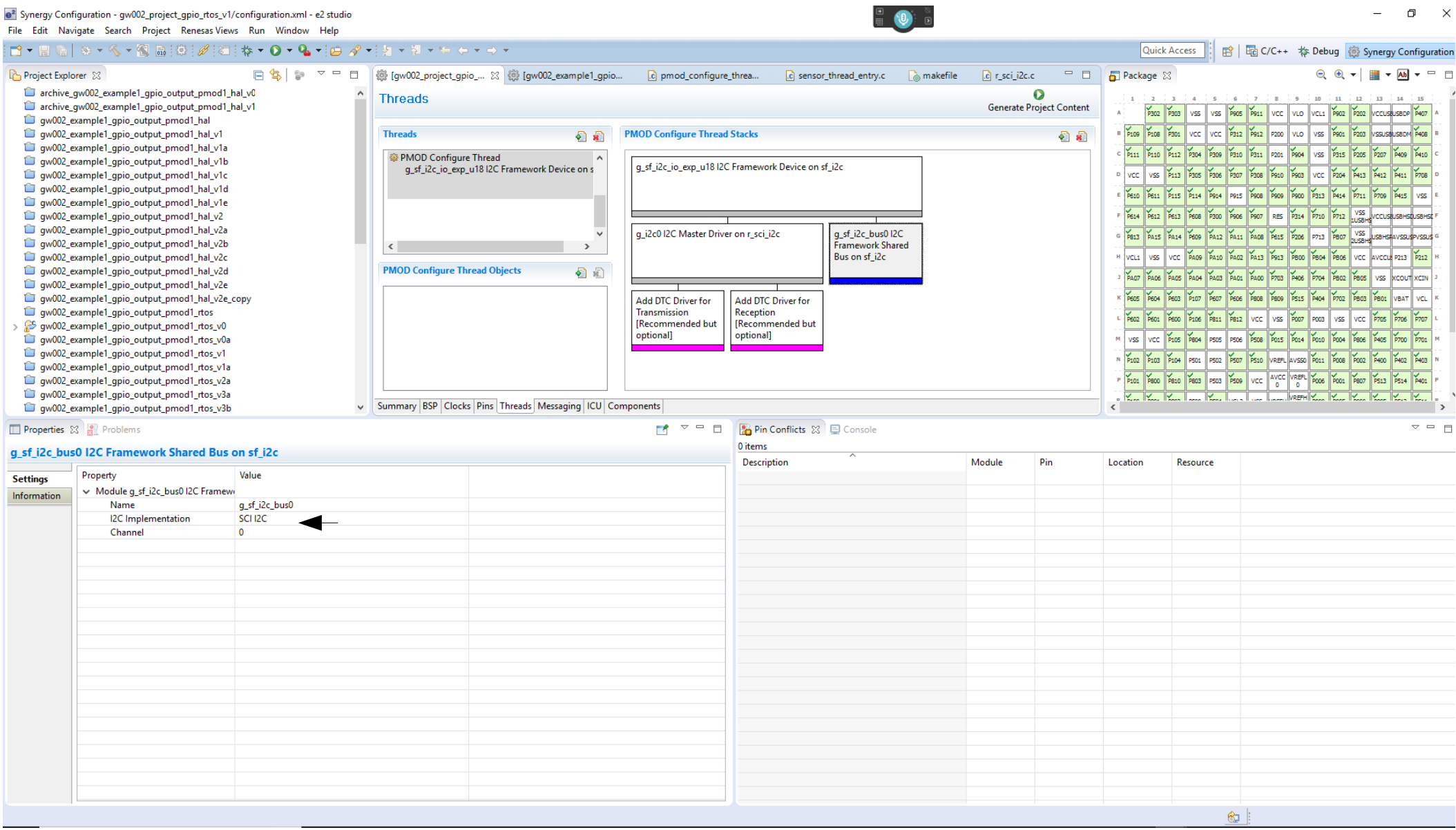

Synergy Configuration - gw002_project_gpio_rtos_v1/configuration.xml - e2 studio
File Edit Navigate Search Project Renesas Views Run Window Help
Quick Access
C/C++
Debug
Synergy Configuration
Project Explorer
archive_gw002_example1_gpio_output_pmod1_hal_v0
archive_gw002_example1_gpio_output_pmod1_hal_v1
gw002_example1_gpio_output_pmod1_hal
gw002_example1_gpio_output_pmod1_hal_v1
gw002_example1_gpio_output_pmod1_hal_v1a
gw002_example1_gpio_output_pmod1_hal_v1b
gw002_example1_gpio_output_pmod1_hal_v1c
gw002_example1_gpio_output_pmod1_hal_v1d
gw002_example1_gpio_output_pmod1_hal_v1e
gw002_example1_gpio_output_pmod1_hal_v2
gw002_example1_gpio_output_pmod1_hal_v2a
gw002_example1_gpio_output_pmod1_hal_v2b
gw002_example1_gpio_output_pmod1_hal_v2c
gw002_example1_gpio_output_pmod1_hal_v2d
gw002_example1_gpio_output_pmod1_hal_v2e
gw002_example1_gpio_output_pmod1_hal_v2e_copy
gw002_example1_gpio_output_pmod1_rtos
gw002_example1_gpio_output_pmod1_rtos_v0
Binaries
Includes
src
synergy
Debug
script
synergy_cfg
configuration.xml
gw002_example1_gpio_output_pmod1_rtos Debug.jlink
gw002_example1_gpio_output_pmod1_rtos_v0 Debug.jlink
gw002_example1_gpio_output_pmod1_rtos_v0 Debug.launch
GW2.pincfg
PMOD1_GPIO_output_v1 Debug.jlink
PMOD1_GPIO_output_v2_mycode Debug.jlink
PMOD1_GPIO_output_v3_u19pwr Debug.jlink
PMOD1_GPIO_output_v4_gpio_out Debug.jlink
R7FS7G27H2A01CBD.pincfg
synergy_cfg.txt
gw002_example1_gpio_output_pmod1_rtos_v0a
gw002_example1_gpio_output_pmod1_rtos_v1
gw002_example1_gpio_output_pmod1_rtos_v1a
*[gw002_project_gpio_rtos_v1] Synergy Configuration
[gw002_example1_gpio_output_pmod1_rtos_v0] Synergy Configuration
Threads
Generate Project Content
Threads
HAL/Common
g_elc ELC Driver on r_elc
g_cgc CGC Driver on r_cgc
g_ioport I/O Port Driver on r_ioport ...
PMOD Configure Thread
g_sf_i2c_device0 I2C Framework Device on sf_i2c
PMOD Configure Thread Stacks
g_sf_i2c_device0 I2C Framework Device on sf_i2c
Add I2C Driver
g_sf_i2c_bus0 I2C Framework Shared
New
I2C Master Driver on r_riic
I2C Master Driver on r_sci_i2c
PMOD Configure Thread Objects
Summary BSP Clocks Pins Threads Messaging ICU Components
Package
R7FS7G27xxxxxxBD - 224BGA (Top View)
Connection status:
Error
Warning
OK
Properties
Problems
Properties are not available.
Pin Conflicts
Console
<terminated> gw002_project_gpio_hal_v1 Debug [Renesas GDB Hardware Debugging] GDB server
GDBServer for Renesas targets. Version 5.3.0.023 (Jan 3 2017 15:08:05)
Starting server with the following options:
Raw options : C:\Renesas\e2_studio531_ssp120_s7g2avnet\eclipse\../DebugComp/e2-server-gdb -g
Connecting to R7FS7G27H, ARM Target
GDBServer endian : little
Target power : off
Starting target connection

Add framework driver for U18

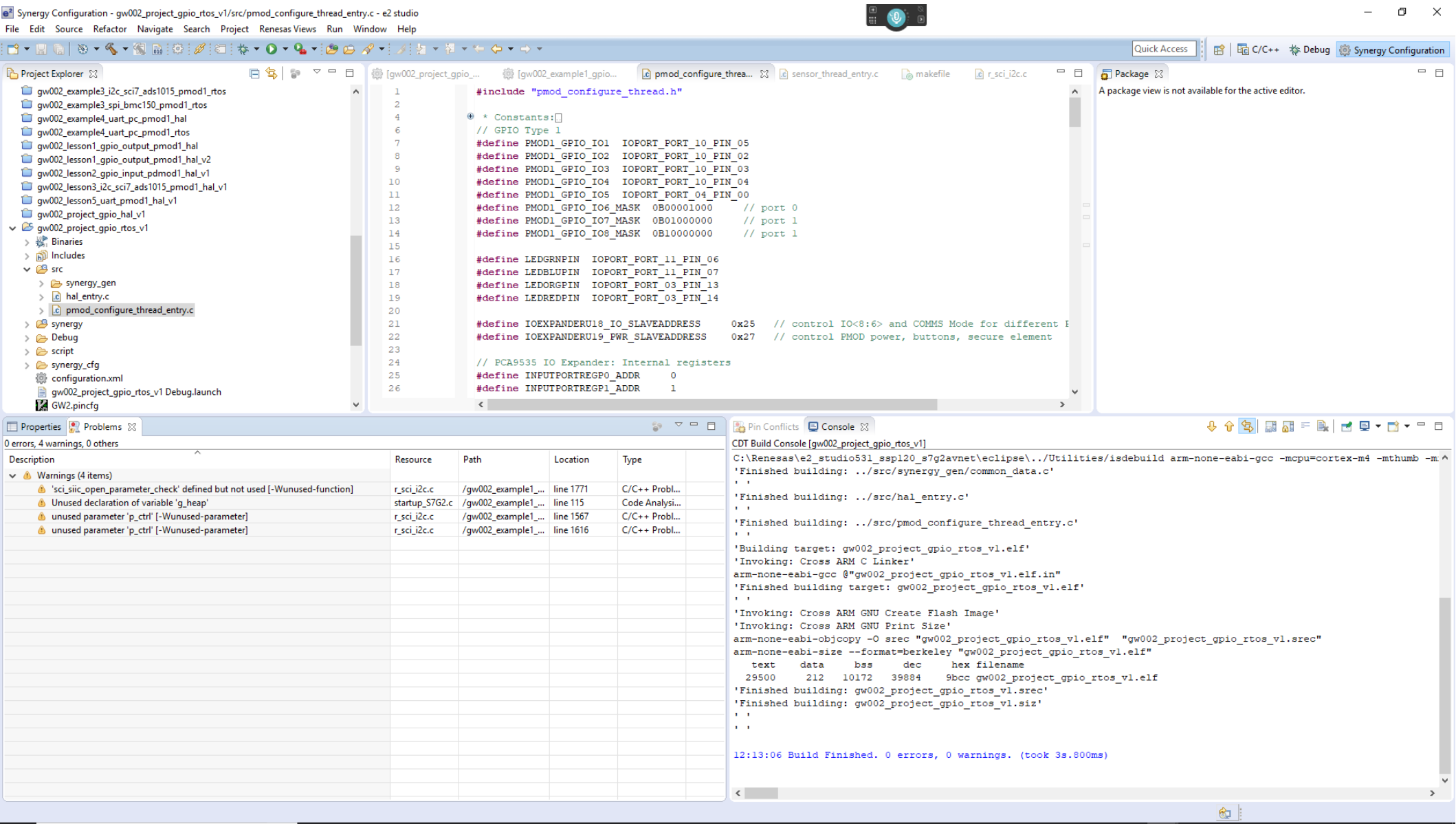


Suppress errors.




Synergy Configuration - gw002_project_gpio_rtos_v1/configuration.xml - e2 studio
File Edit Navigate Search Project Renesas Views Run Window Help
Quick Access
C/C++ Debug Synergy Configuration
Project Explorer
archive_gw002_example1_gpio_output_pmod1_hal_v0
archive_gw002_example1_gpio_output_pmod1_hal_v1
gw002_example1_gpio_output_pmod1_hal
gw002_example1_gpio_output_pmod1_hal_v1
gw002_example1_gpio_output_pmod1_hal_v1a
gw002_example1_gpio_output_pmod1_hal_v1b
gw002_example1_gpio_output_pmod1_hal_v1c
gw002_example1_gpio_output_pmod1_hal_v1d
gw002_example1_gpio_output_pmod1_hal_v1e
gw002_example1_gpio_output_pmod1_hal_v2
gw002_example1_gpio_output_pmod1_hal_v2a
gw002_example1_gpio_output_pmod1_hal_v2b
gw002_example1_gpio_output_pmod1_hal_v2c
gw002_example1_gpio_output_pmod1_hal_v2d
gw002_example1_gpio_output_pmod1_hal_v2e
gw002_example1_gpio_output_pmod1_hal_v2e_copy
gw002_example1_gpio_output_pmod1_rtos
gw002_example1_gpio_output_pmod1_rtos_v0
gw002_example1_gpio_output_pmod1_rtos_v0a
gw002_example1_gpio_output_pmod1_rtos_v1
gw002_example1_gpio_output_pmod1_rtos_v1a
gw002_example1_gpio_output_pmod1_rtos_v2a
gw002_example1_gpio_output_pmod1_rtos_v3a
gw002_example1_gpio_output_pmod1_rtos_v3b
[gw002_project_gpio_...
[gw002_example1_gpio...
pmod_configure_threa...
sensor_thread_entry.c
makefile
r_sci_i2c.c
Threads
Generate Project Content
Threads
PMOD Configure Thread
g_sf_i2c_io_exp_u18 I2C Framework Device on s
PMOD Configure Thread Stacks
g_sf_i2c_io_exp_u18 I2C Framework Device on sf_i2c
g_i2c0 I2C Master Driver on r_sci_i2c
g_sf_i2c_bus0 I2C Framework Shared Bus on sf_i2c
Add DTC Driver for Transmission [Recommended but optional]
Add DTC Driver for Reception [Recommended but optional]
PMOD Configure Thread Objects
Summary BSP Clocks Pins Threads Messaging ICU Components
Package
Properties
Problems
g_sf_i2c_bus0 I2C Framework Shared Bus on sf_i2c
Settings
Information
Property
Value
Module g_sf_i2c_bus0 I2C Framew
Name
g_sf_i2c_bus0
I2C Implementation
SCI I2C
Channel
0
Pin Conflicts
Console
0 items
Description
Module
Pin
Location
Resource

Clean Build


Synergy Configuration - gw002_project_gpio_rtos_v1/src/pmod_configure_thread_entry.c - e2 studio
File Edit Source Refactor Navigate Search Project Renesas Views Run Window Help
Quick Access
C/C++
Debug
Synergy Configuration
Project Explorer
gw002_example3_i2c_sci7_ads1015_pmod1_rtos
gw002_example3_spi_bmc150_pmod1_rtos
gw002_example4_uart_pc_pmod1_hal
gw002_example4_uart_pc_pmod1_rtos
gw002_lesson1_gpio_output_pmod1_hal
gw002_lesson1_gpio_output_pmod1_hal_v2
gw002_lesson2_gpio_input_pdmod1_hal_v1
gw002_lesson3_i2c_sci7_ads1015_pmod1_hal_v1
gw002_lesson5_uart_pmod1_hal_v1
gw002_project_gpio_hal_v1
gw002_project_gpio_rtos_v1
Binaries
Includes
src
synergy_gen
hal_entry.c
pmod_configure_thread_entry.c
synergy
Debug
script
synergy_cfg
configuration.xml
gw002_project_gpio_rtos_v1 Debug.launch
GW2.pincfg
pmod_configure_threa...
sensor_thread_entry.c
makefile
r_sci_i2c.c
#include "pmod_configure_thread.h"
* Constants:
// GPIO Type 1
#define PMOD1_GPIO_IO1 IOPORT_PORT_10_PIN_05
#define PMOD1_GPIO_IO2 IOPORT_PORT_10_PIN_02
#define PMOD1_GPIO_IO3 IOPORT_PORT_10_PIN_03
#define PMOD1_GPIO_IO4 IOPORT_PORT_10_PIN_04
#define PMOD1_GPIO_IO5 IOPORT_PORT_04_PIN_00
#define PMOD1_GPIO_IO6_MASK 0B00001000 // port 0
#define PMOD1_GPIO_IO7_MASK 0B01000000 // port 1
#define PMOD1_GPIO_IO8_MASK 0B10000000 // port 1
#define LEDGRNPIN IOPORT_PORT_11_PIN_06
#define LEDBLUPIN IOPORT_PORT_11_PIN_07
#define LEDORGPIN IOPORT_PORT_03_PIN_13
#define LEDREDPIN IOPORT_PORT_03_PIN_14
#define IOEXPANDERU18_IO_SLAVEADDRESS 0x25 // control IO<8:6> and COMMS Mode for different
#define IOEXPANDERU19_PWR_SLAVEADDRESS 0x27 // control PMOD power, buttons, secure element
// PCA9535 IO Expander: Internal registers
#define INPUTPORTREGP0_ADDR 0
#define INPUTPORTREGP1_ADDR 1
Package
A package view is not available for the active editor.
Properties
Problems
0 errors, 4 warnings, 0 others
Description
Resource
Path
Location
Type
Warnings (4 items)
'sci_siic_open_parameter_check' defined but not used [-Wunused-function]
r_sci_i2c.c
/gw002_example1_...
line 1771
C/C++ Probl...
Unused declaration of variable 'g_heap'
startup_S7G2.c
/gw002_example1_...
line 115
Code Analysi...
unused parameter 'p_ctrl' [-Wunused-parameter]
r_sci_i2c.c
/gw002_example1_...
line 1567
C/C++ Probl...
unused parameter 'p_ctrl' [-Wunused-parameter]
r_sci_i2c.c
/gw002_example1_...
line 1616
C/C++ Probl...
Pin Conflicts
Console
CDT Build Console [gw002_project_gpio_rtos_v1]
C:\Renesas\e2_studio531_ssp120_s7g2avnet\eclipse\../Utilities/isdebuild arm-none-eabi-gcc -mcpu=cortex-m4 -mthumb -m
'Finished building: ../src/synergy_gen/common_data.c'
' '
'Finished building: ../src/hal_entry.c'
' '
'Finished building: ../src/pmod_configure_thread_entry.c'
' '
'Building target: gw002_project_gpio_rtos_v1.elf'
'Invoking: Cross ARM C Linker'
arm-none-eabi-gcc @"gw002_project_gpio_rtos_v1.elf.in"
'Finished building target: gw002_project_gpio_rtos_v1.elf'
' '
'Invoking: Cross ARM GNU Create Flash Image'
'Invoking: Cross ARM GNU Print Size'
arm-none-eabi-objcopy -O srec "gw002_project_gpio_rtos_v1.elf" "gw002_project_gpio_rtos_v1.srec"
arm-none-eabi-size --format=berkeley "gw002_project_gpio_rtos_v1.elf"
text data bss dec hex filename
29500 212 10172 39884 9bcc gw002_project_gpio_rtos_v1.elf
'Finished building: gw002_project_gpio_rtos_v1.srec'
'Finished building: gw002_project_gpio_rtos_v1.siz'
' '
' '
12:13:06 Build Finished. 0 errors, 0 warnings. (took 3s.800ms)

SSP_ERR_IRQ_BSP_DISABLED