

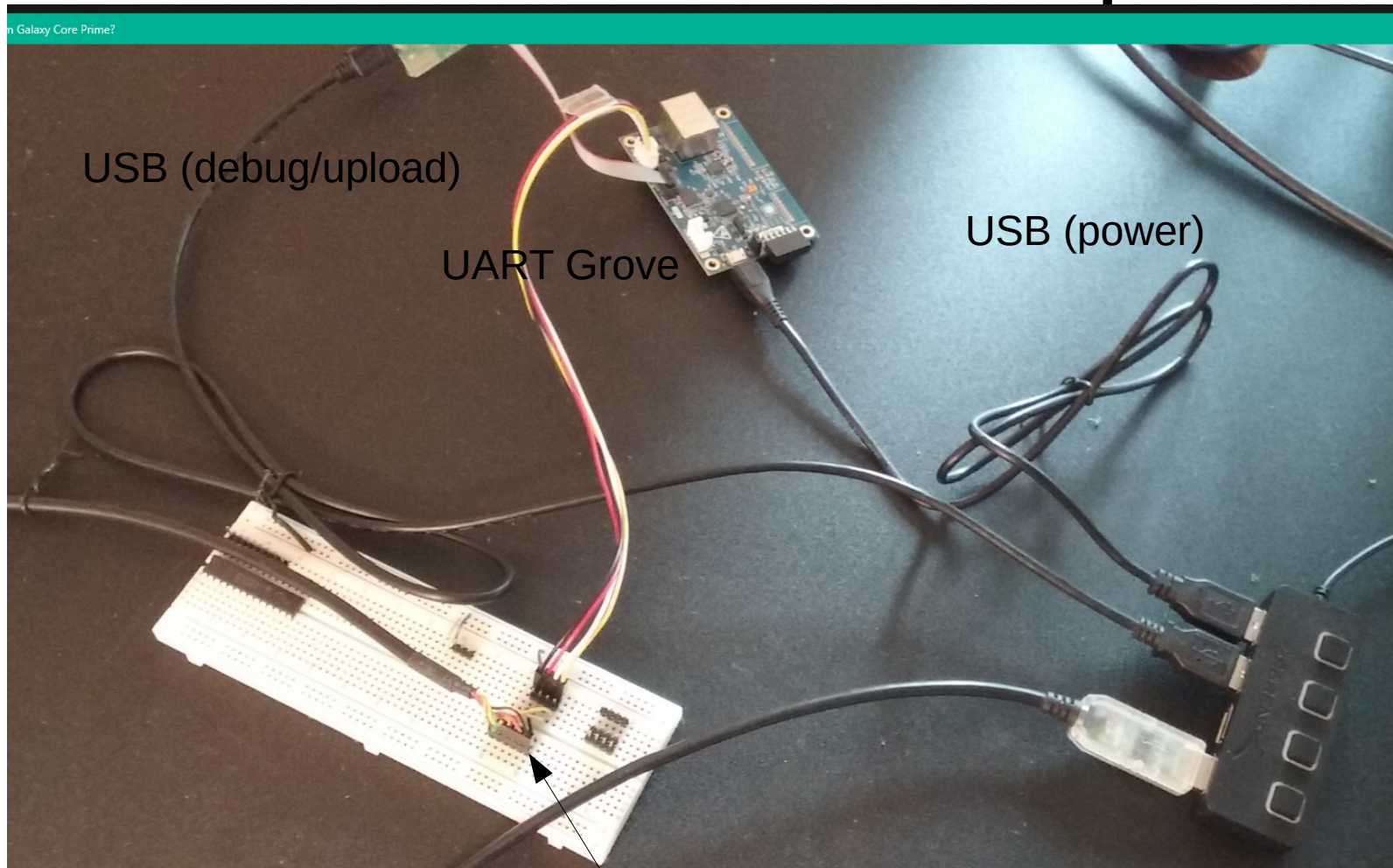
S5D9 UART Bus Example (Framework Version with ThreadX RTOS)

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E2 Studio 5.4.0.023
SSP 1.3.0

Hardware Setup



USB (debug/upload)

UART Grove

USB (power)

UART to USB FDTI Cable (Adafruit)

Color code (see next page)

Connection

Connections

Grove A J3: UART to FTDI USB-to-UART Cable

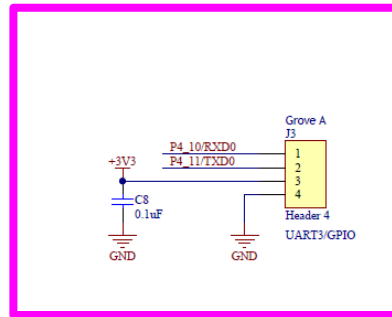
Pin 1: Yellow RXD → Pin 4 Orange TXD

Pin 2: White TXD → Pin 5 Yellow RXD

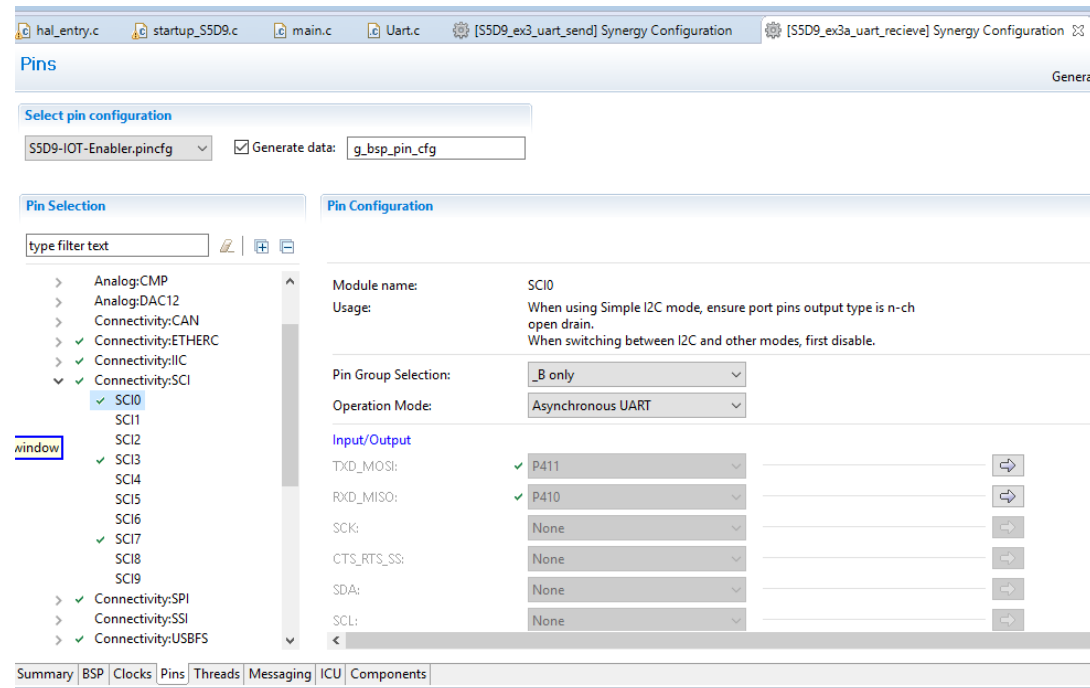
Pin 3: Red 3V (No Connect)

Pin 4: Black GND → Pin 1 Black GND

Grove (UART)



Pin Configuration (SCI0 Asy UART)



Create Thread and Fill in the properties

The screenshot shows the Synergy IDE interface with the 'Threads' and 'UART Thread Objects' panels. The 'Threads' panel lists the following threads:

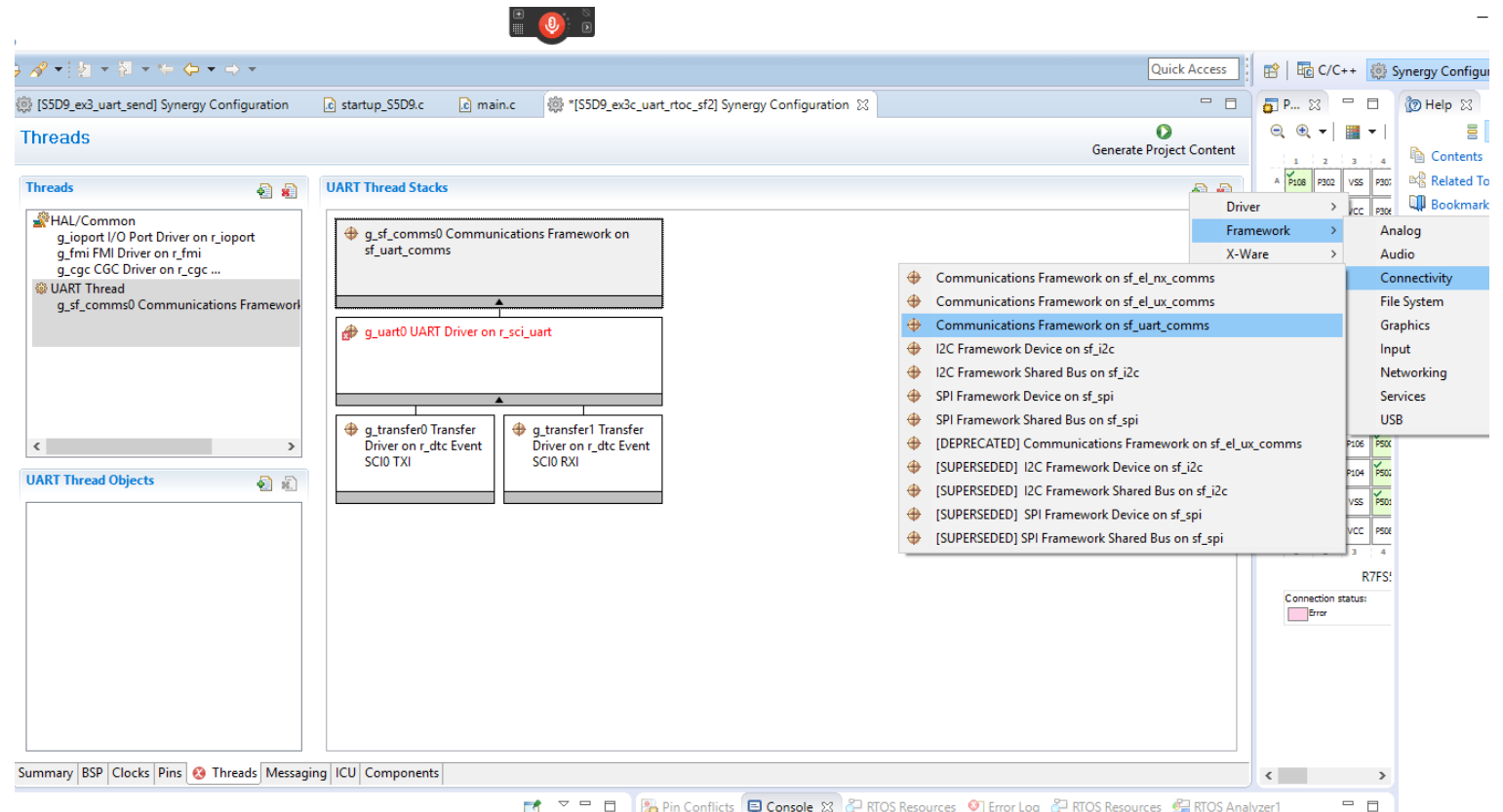
- HAL/Common
 - g_ioport I/O Port Driver on r_ioport
 - g_fmi FMI Driver on r_fmi
 - g_cgc CGC Driver on r_cgc ...
- UART Thread
 - g_sf_comms0 Communications Framework

The 'UART Thread Objects' panel is empty.

The 'UART Thread' properties are shown in the bottom panel:

| Property | Value |
|-------------------------------|-------------|
| Symbol | uart_thread |
| Name | UART Thread |
| Stack size (bytes) | 1024 |
| Priority | 15 |
| Auto start | Enabled |
| Time slicing interval (ticks) | 1 |

Select UART Framework



The screenshot displays the Synergy Configuration tool interface. The top toolbar includes buttons for 'Generate Project Content', 'Find', and 'All'. The main workspace is divided into several panes:

- Threads:** Lists HAL/Common components (g_ioport I/O Port Driver on r_ioport, g_fmi FMI Driver on r_fmi, g_cgc CGC Driver on r_cgc ...) and the UART Thread.
- UART Thread Objects:** A list of objects associated with the UART thread.
- UART Thread Stacks:** A hierarchical diagram showing the stack of components for the UART thread. It includes:
 - g_sf_comms0 Communications Framework on sf_uart_comms
 - g_uart0 UART Driver on r_sci_uart
 - g_transfer0 Transfer Driver on r_dtc Event SCI0 TXI
 - g_transfer1 Transfer Driver on r_dtc Event SCI0 RXI

Below the main workspace, there is a tabbed interface with 'Summary', 'BSP', 'Clocks', 'Pins', 'Threads', 'Messaging', 'ICU', and 'Components'. The 'Threads' tab is selected, and the 'Console' sub-tab is active. An arrow points from the 'Console' sub-tab to the 'Properties' pane.

The 'Properties' pane shows the configuration for the **g_sf_comms0 Communications Framework on sf_uart_comms** module. It includes a 'Settings' section with 'Information' expanded, displaying the following properties:

| Property | Value |
|--|----------------|
| Common | |
| Parameter Checking | Default (BSP) |
| Read Input Queue Size (4-Byte Words) | 15 |
| Module g_sf_comms0 Communications Framework on sf_uart_co | |
| Name | g_sf_comms0 |
| Name of generated initialization function | sf_comms_init0 |
| Auto Initialization | Enable |

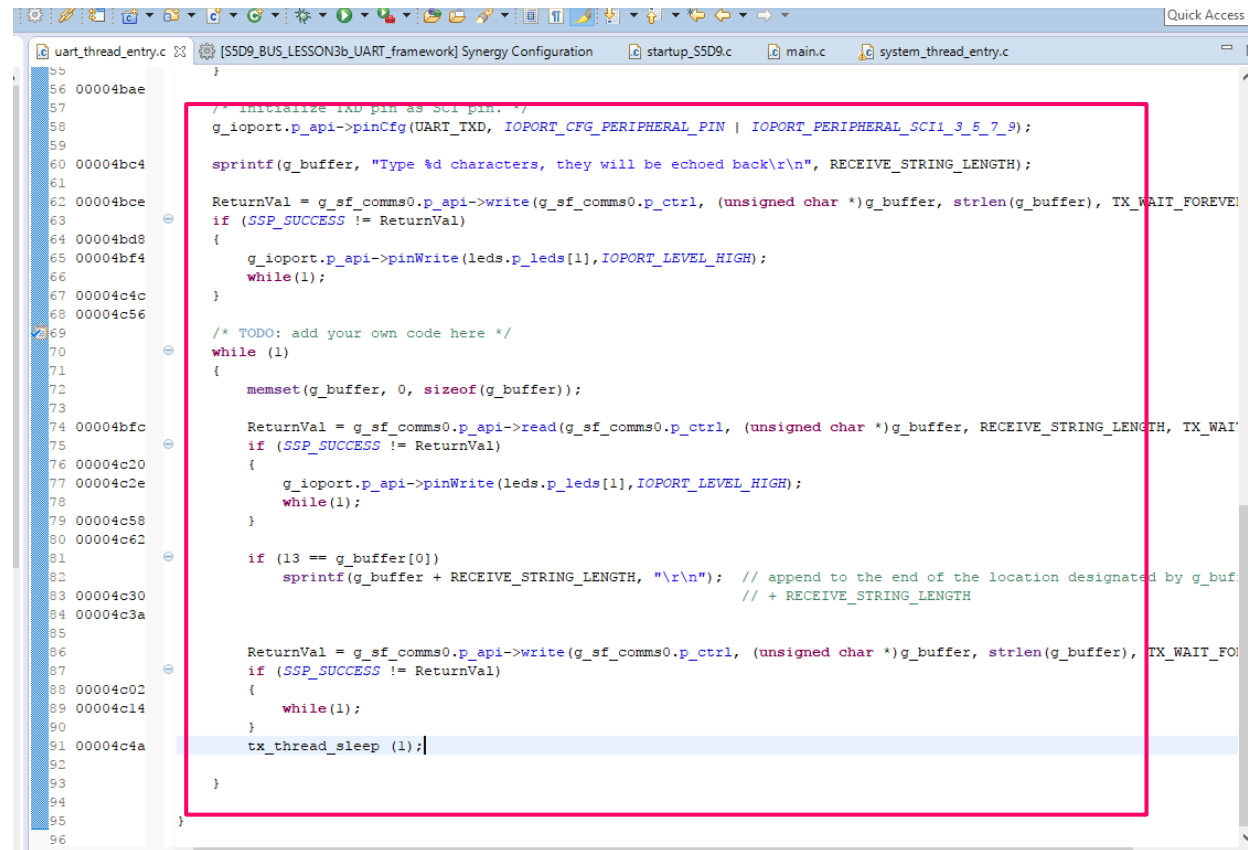
Set Priority 6 for Interrupt Priority. Channel is 0 (SCI0)

The screenshot shows the Synergy Configuration interface for a project named [SSD9_ex3c_uart_rtoc_sf2]. The top section displays the 'Threads' and 'UART Thread Stacks' hierarchy. The 'UART Thread Stacks' section shows a stack of components: g_sf_comms0 Communications Framework on sf_uart_comms, g_uart0 UART Driver on r_sci_uart, and two transfer drivers (g_transfer0 and g_transfer1) on r_dtc Event SCI0 TXI. Below this, the 'g_uart0 UART Driver on r_sci_uart' settings are shown. The 'Settings' tab is active, and the 'Information' sub-tab is selected. The settings table is as follows:

| Property | Value |
|---|--|
| Common | |
| External RTS Operation | Disable |
| Reception | Enable |
| Transmission | Enable |
| Parameter Checking | Default (BSP) |
| Module g_uart0 UART Driver on r_sci_uart | |
| Name | g_uart0 |
| Channel | 0 |
| Baud Rate | 9600 |
| Data Bits | 8bits |
| Parity | None |
| Stop Bits | 1bit |
| CTS/RTS Selection | RTS (CTS is disabled) |
| Name of UART callback function to be defined by user | NULL |
| Name of UART callback function for the RTS external pin contr | NULL |
| Clock Source | Internal Clock |
| Baudrate Clock Output from SCK pin | Disable |
| Start bit detection | Falling Edge |
| Noise Cancel | Disable |
| Bit Rate Modulation Enable | Enable |
| Receive FIFO Trigger Level | Max |
| Receive Interrupt Priority | Priority 6 (CM4: valid, CM0+: invalid) |
| Transmit Interrupt Priority | Priority 6 (CM4: valid, CM0+: invalid) |
| Transmit End Interrupt Priority | Priority 6 (CM4: valid, CM0+: invalid) |
| Error Interrupt Priority | Priority 6 (CM4: valid, CM0+: invalid) |

Channel is 0 because SC0 is used.

Source Code



```
55
56 00004bae /* Initialize I/O pin as SCI pin. */
57 g_ioport.p_api->pinCfg(UART_TXD, IOPORT_CFG_PERIPHERAL_PIN | IOPORT_PERIPHERAL_SCI1_3_5_7_9);
58
59
60 00004bc4 sprintf(g_buffer, "Type %d characters, they will be echoed back\r\n", RECEIVE_STRING_LENGTH);
61
62 00004bce ReturnVal = g_sf_comms0.p_api->write(g_sf_comms0.p_ctrl, (unsigned char *)g_buffer, strlen(g_buffer), TX_WAIT_FOREVER);
63 if (SSP_SUCCESS != ReturnVal)
64 {
65 00004bd8 g_ioport.p_api->pinWrite(leds.p_leds[1], IOPORT_LEVEL_HIGH);
66 00004bf4 while(1);
67 }
68 00004c4c
69 00004c56
70 /* TODO: add your own code here */
71 while (1)
72 {
73
74 00004bfc memset(g_buffer, 0, sizeof(g_buffer));
75
76 00004c20 ReturnVal = g_sf_comms0.p_api->read(g_sf_comms0.p_ctrl, (unsigned char *)g_buffer, RECEIVE_STRING_LENGTH, TX_WAIT_FOREVER);
77 00004c2e if (SSP_SUCCESS != ReturnVal)
78 {
79 00004c58 g_ioport.p_api->pinWrite(leds.p_leds[1], IOPORT_LEVEL_HIGH);
80 00004c62 while(1);
81 }
82
83 00004c30 if (13 == g_buffer[0])
84 00004c3a sprintf(g_buffer + RECEIVE_STRING_LENGTH, "\r\n"); // append to the end of the location designated by g_buffer
85 // + RECEIVE_STRING_LENGTH
86
87 ReturnVal = g_sf_comms0.p_api->write(g_sf_comms0.p_ctrl, (unsigned char *)g_buffer, strlen(g_buffer), TX_WAIT_FOREVER);
88 if (SSP_SUCCESS != ReturnVal)
89 {
90 00004c02 while(1);
91 00004c4a tx_thread_sleep (1);
92 }
93
94
95
96 }
```

Use Device Manager for the COM port #.

