# S5D9 ADS1015 I2C Bus Examples (Both IIC and SCI Drivers) By Michael Li (3/2/2018) https://www.miketechuniverse.com

E2 Studio 5.4.0.023 SSP 1.3.0 This is a set of examples that show how to add the ADC capability to the S5D9 IOT board.

This board has two grove headers. Grove B is an IIC port while grove A is an SCI port. You creates r\_iic driver for the IIC por and r\_sci\_i2c for the SCI port.

6 examples are included in this tutorial.

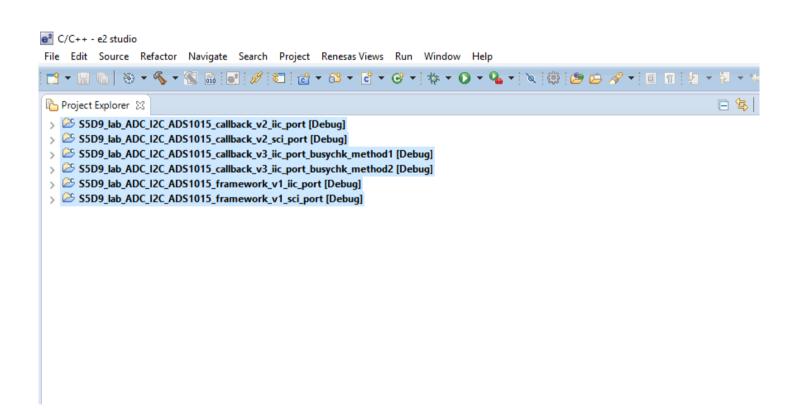
```
Grove B / r_iic driver (only for the fast speed mode) *
Grove B / framework with r_iic driver
Grove A / r_sci_i2c driver
Grove A / framework with r_sci_i2c driver
```

\*Because r\_iic has some issue for standard speed mode. Two possible workaround examples are included.

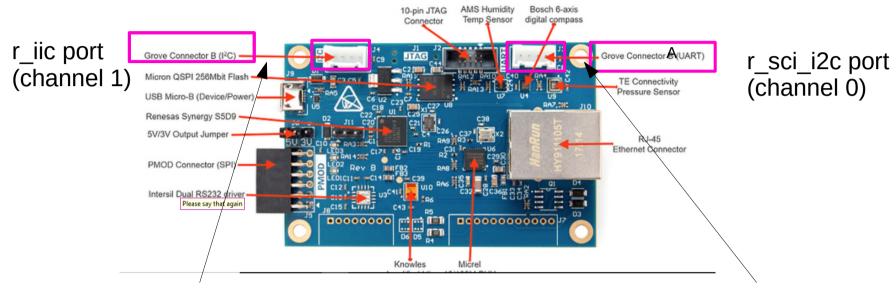
Grove B / r\_iic driver / method 1 with busy bit check Grove B / r\_iic driver / method 2 with busy bit check

Both checks for the hardware busy bit before the code starts the next i2c transmission. The above examples are are done with limited testing. At this point, this ADC component seem to work well with these workaround solutions.

#### **Project List**



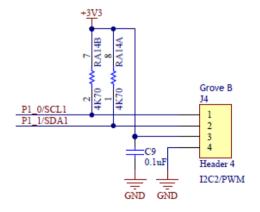
#### Two I2C Bus Ports' Location



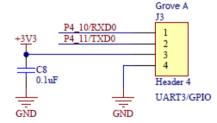
I2C Grove B J4 (P1 0/1)

iic1 Driver

I2C Grove A J3 (P4\_10/11) sci0 Driver



Need to add external 4.7K pull up resistors for P4\_10/11



Reconfigure this port as I2C instead of UART port.

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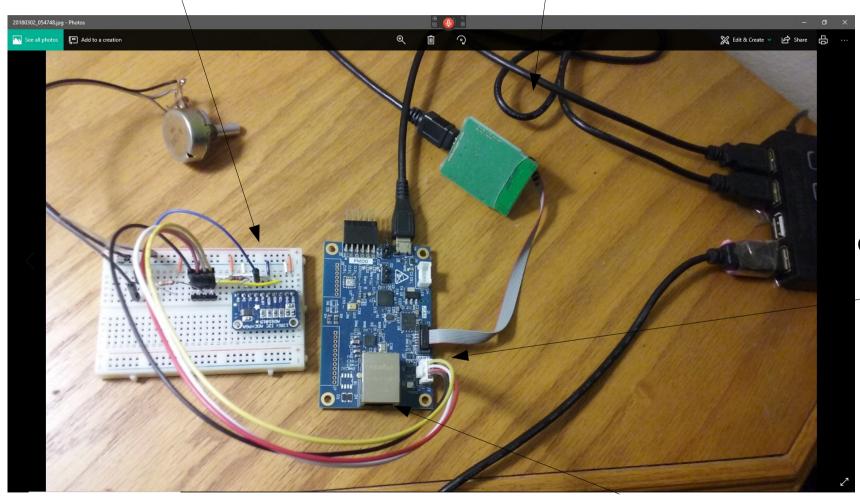
# Adafruit TI ADS1015 ADC Hardware setup I2C bus (Grove B r\_iic port) (ADC part and Potentiometer)

Grove B r\_iic port

S5D9 IOT board

#### Adafruit TI ADS1015 ADC

#### Hardware setup I2C bus (Grove A r\_sci\_i2c port) (ADC part and Potentiometer)

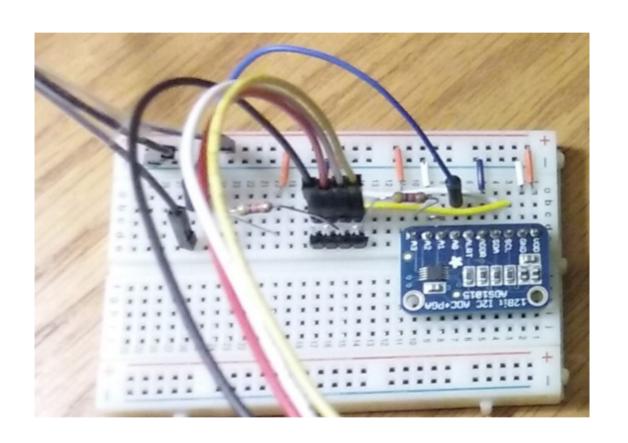


Grove B r\_sci\_i2c port

S5D9 IOT board

Michael C. Li

#### **ADC** connection



VCC = VCC

GND = GND

SCL = SCL

SDA = SDA

ADDR = GND

ALRT = NC

A0 = Potentiometer

A1/2/3 = GND (not used)

#### **ADC Slave Address**

#### I<sup>2</sup>C ADDRESS SELECTION

The ADS1013/4/5 have one address pin, ADDR, that sets the  $I^2C$  address. This pin can be connected to ground, VDD, SDA, or SCL, allowing four addresses to be selected with one pin as shown in Table 5. The state of the address pin ADDR is sampled continuously.

Table 5. ADDR Pin Connection and Corresponding Slave Address

ADDR PIN	SLAVE ADDRESS
Ground	1001000
VDD	1001001
SDA	1001010
SCL	1001011

**Example: Configuration Register Read** 

Step 1: Slave address (48h) +  $w \rightarrow Register$  address (01h)

Step 2: Slave address (48h) +  $r \rightarrow 2$  bytes of data read (8583h)

xample: Configuration Register Write and initiate one shot ADC conversion.

Step 1: Slave address (48h) + w → Register address (01h) + 2 bytes of data write (C383h)

Table 8. Conversion Register (Read-Only)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0

Voltage level =  $D[11:0] / 2048 \times 4.096V$  (using +/-4096 FSR)

**Example: Conversion Register Read** 

Step 1: Slave address (48h) + w → Register address (00h)

Step 2: Slave address (48h) +  $r \rightarrow 2$  bytes of data read (16 bits)

POINTER REGISTER

The four registers are accessed by writing to the Pointer register byte; see Figure 16. Table 6 and Table 7 indicate the Pointer register byte map.

Table 6. Register Address

BIT 1	BIT 0	REGISTER
0	0	Conversion register
0	1	Config register
1	0	Lo_thresh register
1	1	Hi_thresh register

#### Default = 8583h (Config Register)

Table 9. Config Register (Read/Write)

BIT	15	14	13	12	11	10	9	8
NAME	os	MUX2	MUX1	MUX0	PGA2	PGA1	PGA0	MODE
BIT	7	6	5	4	3	2	1	0
NAME	DR2	DR1	DR0	COMP_MODE	COMP_POL	COMP_LAT	COMP_QUE1	COMP_QUE0

Default = 8583h.

Bit [15]

#### OS: Operational status/single-shot conversion start

This bit determines the operational status of the device. This bit can only be written when in power-down mode.

For a write status:

0 : No effect

1 : Begin a single conversion (when in power-down mode)

For a read status:

D : Device is currently performing a conversion
 Device is not currently performing a conversion

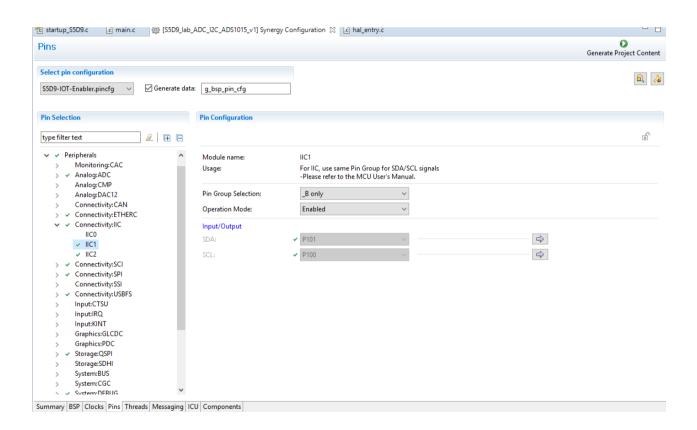
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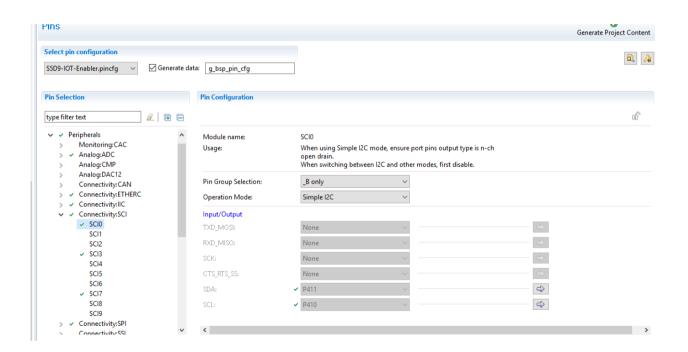
15

Product Folder Link(s): ADS1013 ADS1014 ADS1015

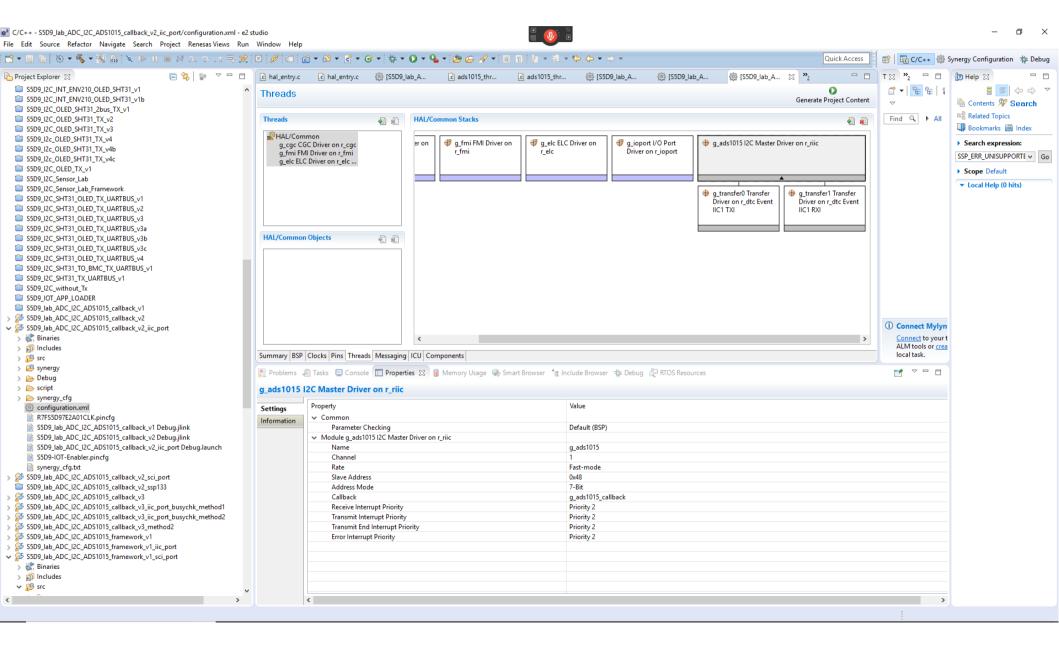
#### IIC Channel 1



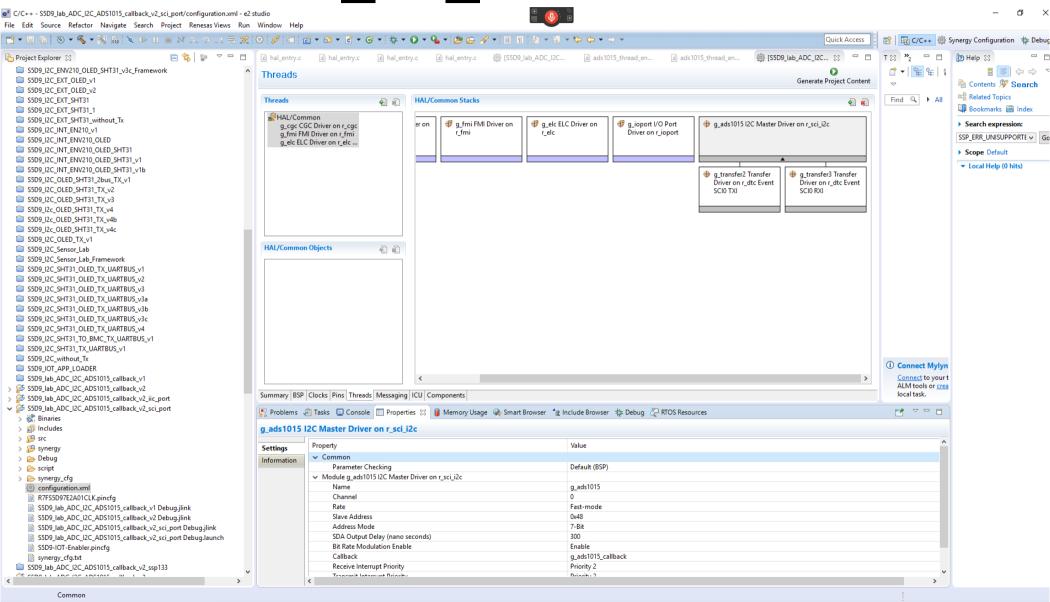
#### SCI Channel 0



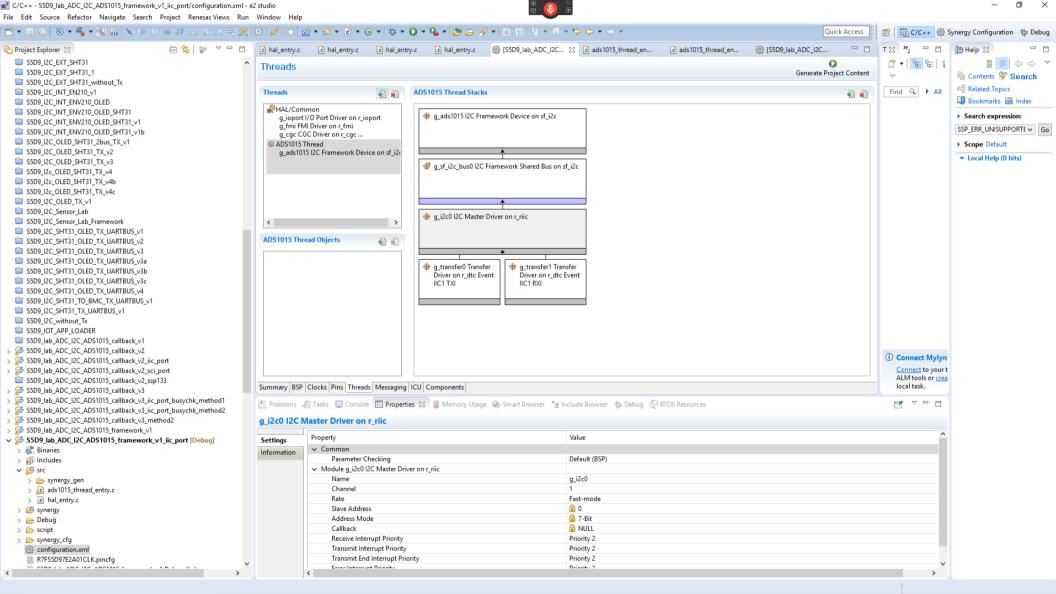
#### r\_iic driver



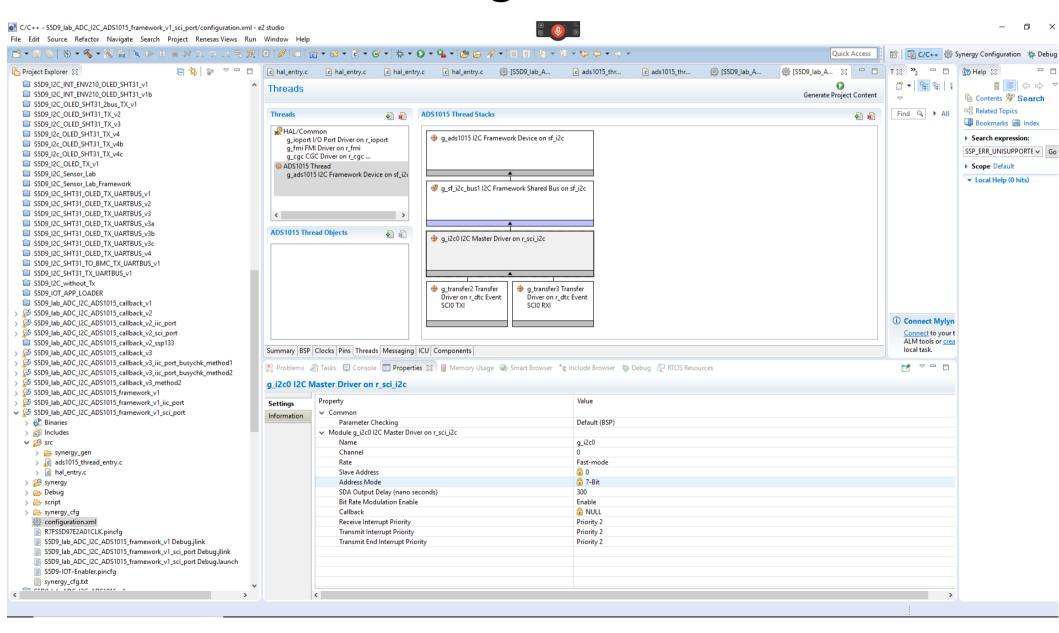
#### r\_sci\_i2c driver



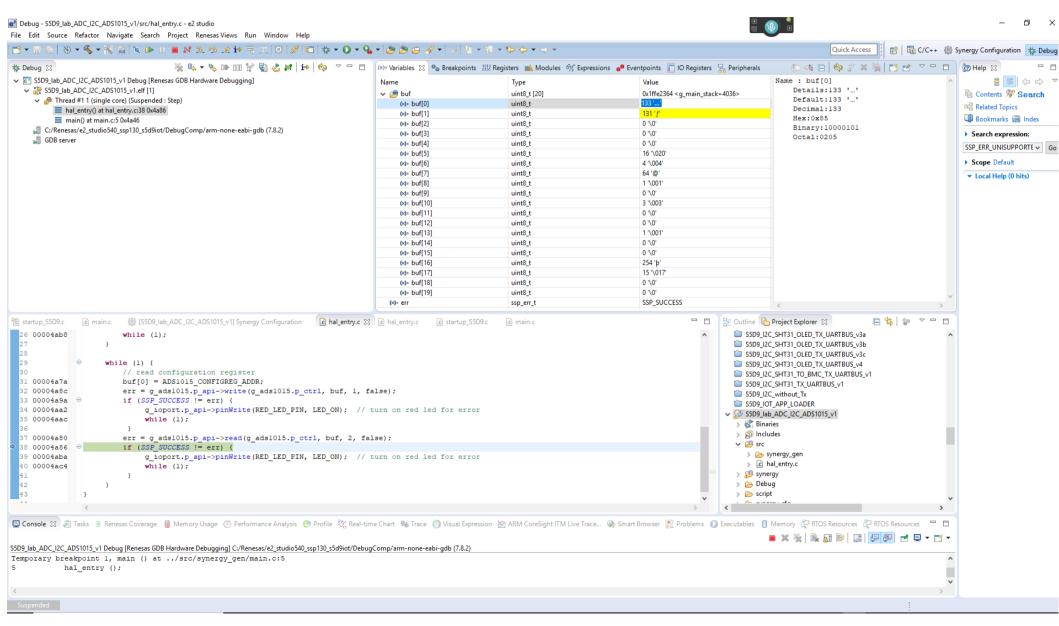
### Framework with the r\_iic driver configuration



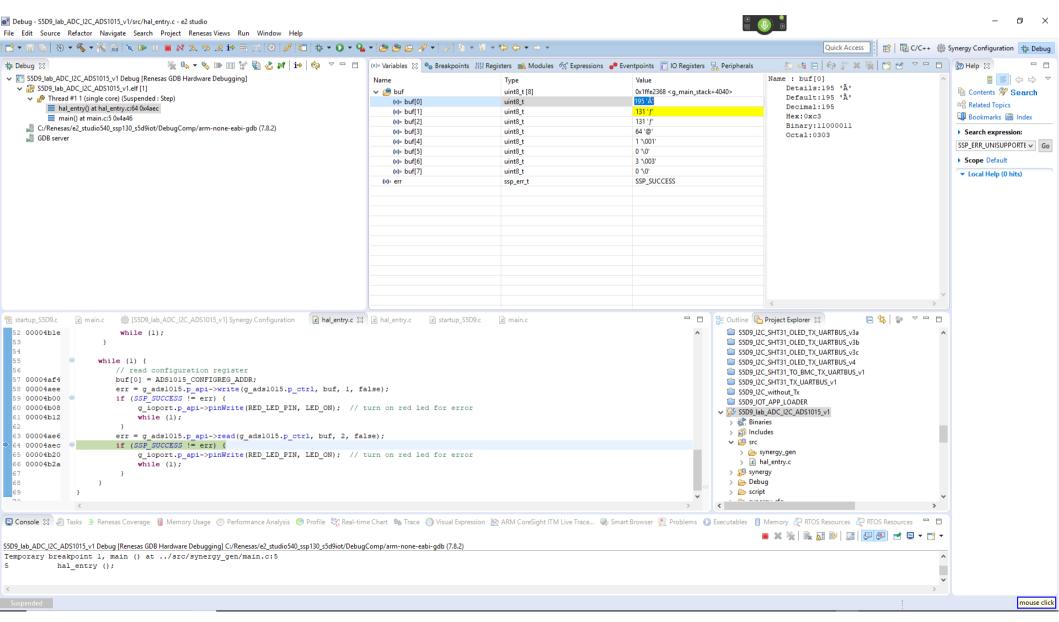
## Framework with the r\_sci\_i2c driver configuration



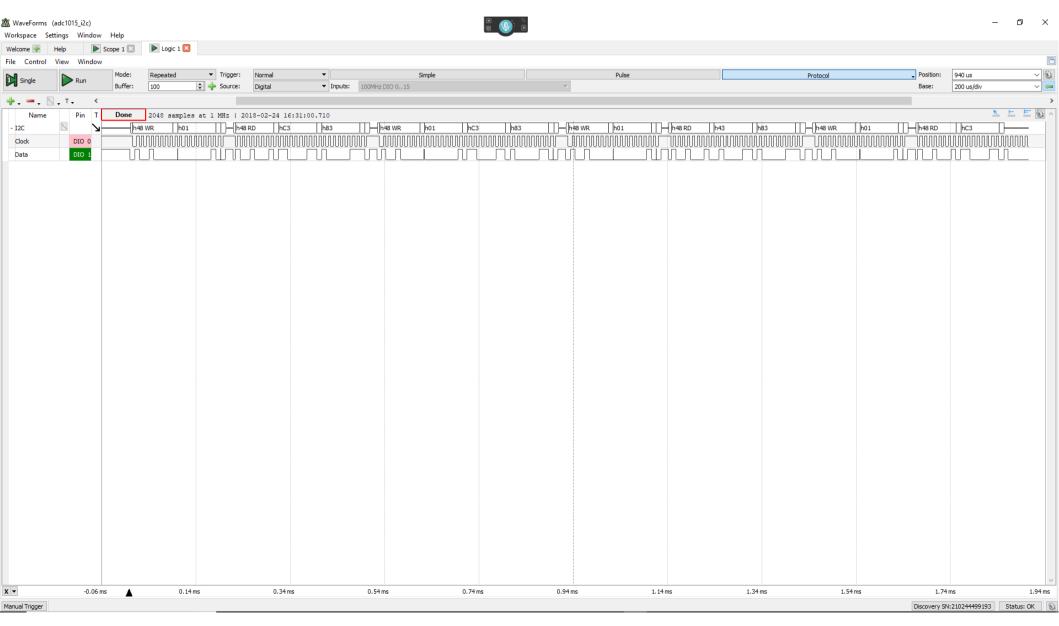
#### Configuration Register read Buf[0] = 85h and Buf[1] = 83h



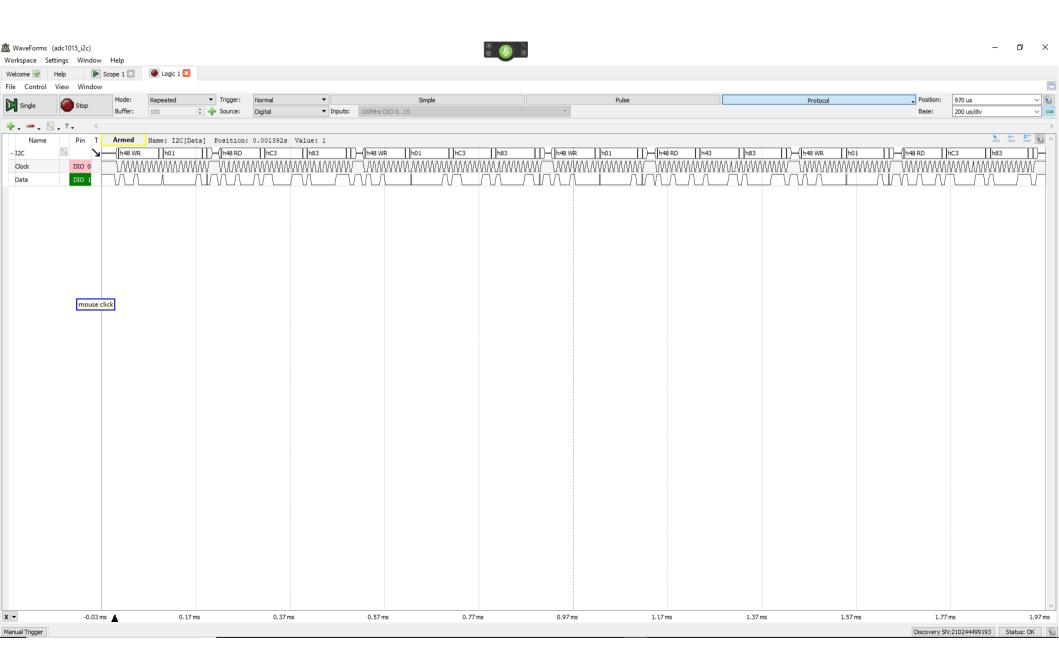
#### Configuration Register write/read Buf[0] = C3h and Buf[1] = 83h



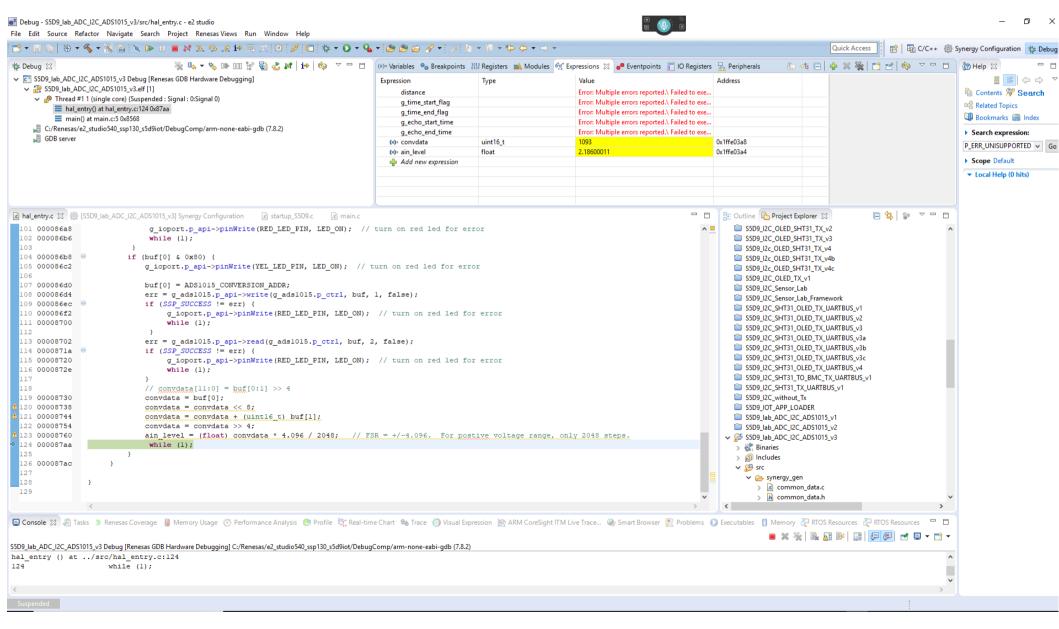
#### C3 (1100\_0011) $\rightarrow$ 43 (0100\_0011) good WR OS bit $\rightarrow$ RD OS bit (0=busy)

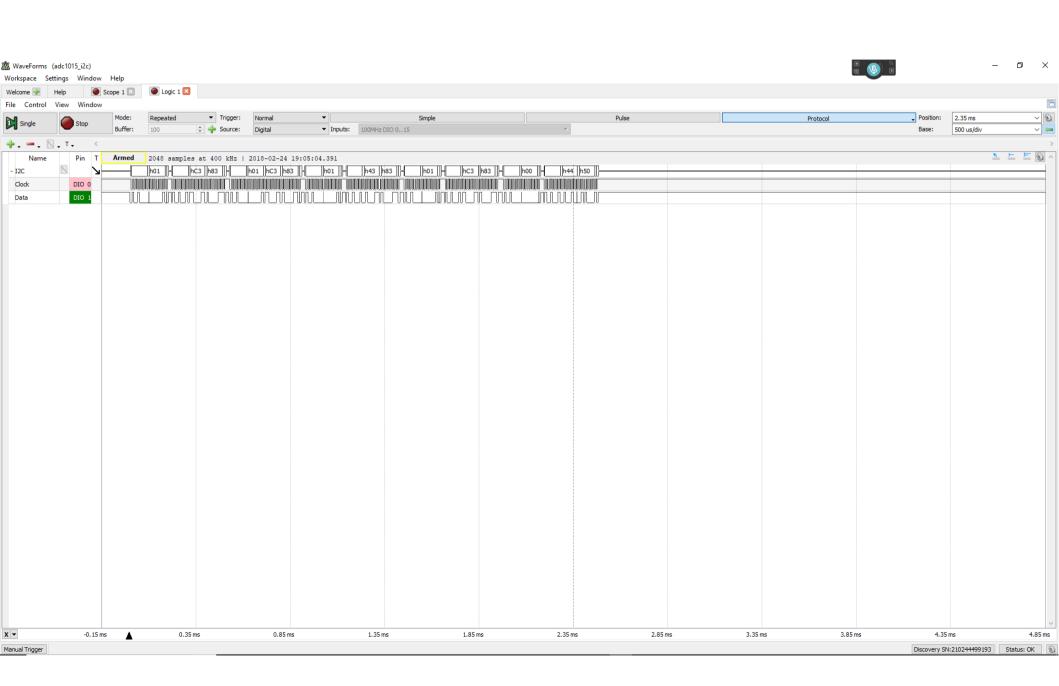


#### Stop when OS bit = 1



#### $0x4450 \rightarrow 0x445 \text{ or } 1093$ $1093 / 2048 \times 4.096 = 2.186V$ FSR +/- 4.096 and only positive side use 2048





#### 0.379 Khz (fast mode)

