S5D9 ADS1015 I2C Bus Examples (Both IIC and SCI Drivers)

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https://www.miketechuniverse.com

E2 Studio 5.4.0.023
SSP 1.3.0

This is a set of examples that show how to add the ADC capability to the S5D9 IOT board.

This board has two grove headers. Grove B is an IIC port while grove A is an SCI port. You creates r_iic driver for the IIC por and r_sci_i2c for the SCI port.

6 examples are included in this tutorial.

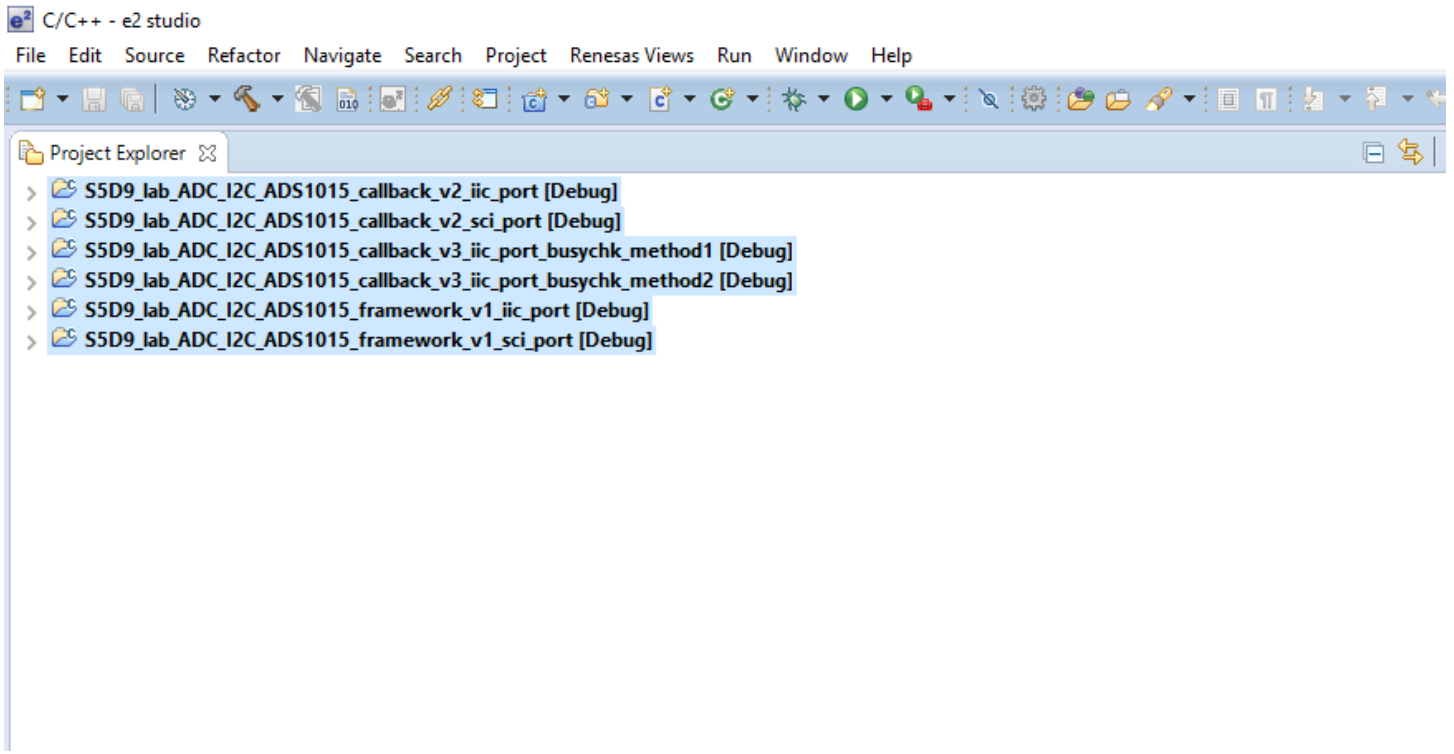
Grove B / r_iic driver (only for the fast speed mode) *
Grove B / framework with r_iic driver
Grove A / r_sci_i2c driver
Grove A / framework with r_sci_i2c driver

*Because r_iic has some issue for standard speed mode. Two possible workaround examples are included.

Grove B / r_iic driver / method 1 with busy bit check
Grove B / r_iic driver / method 2 with busy bit check

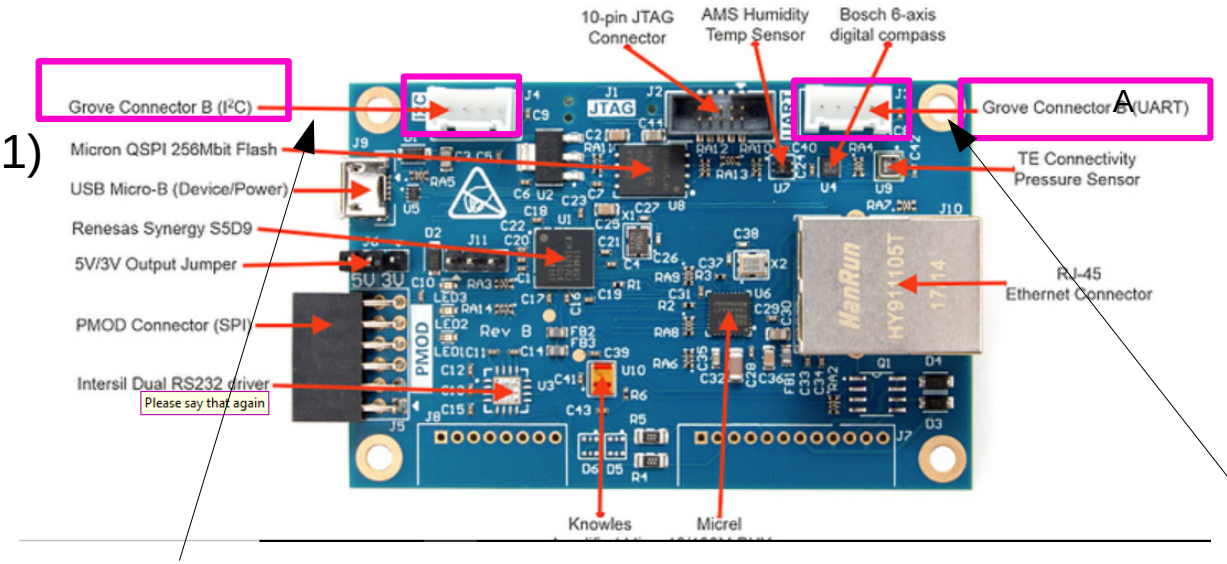
Both checks for the hardware busy bit before the code starts the next i2c transmission. The above examples are are done with limited testing. At this point, this ADC component seem to work well with these workaround solutions.

Project List



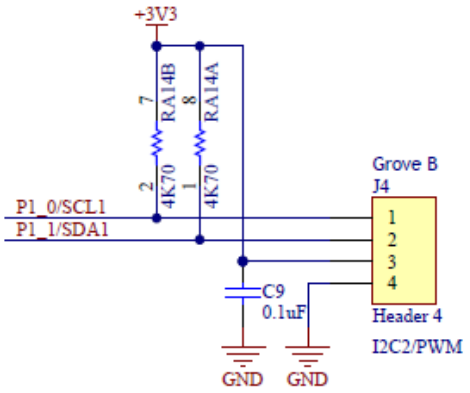
Two I2C Bus Ports' Location

r_iic port (channel 1)



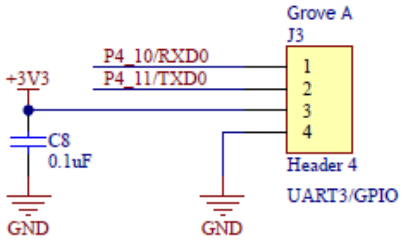
r_sci_i2c port (channel 0)

I2C Grove B J4 (P1_0/1) iic1 Driver



I2C Grove A J3 (P4_10/11) sci0 Driver

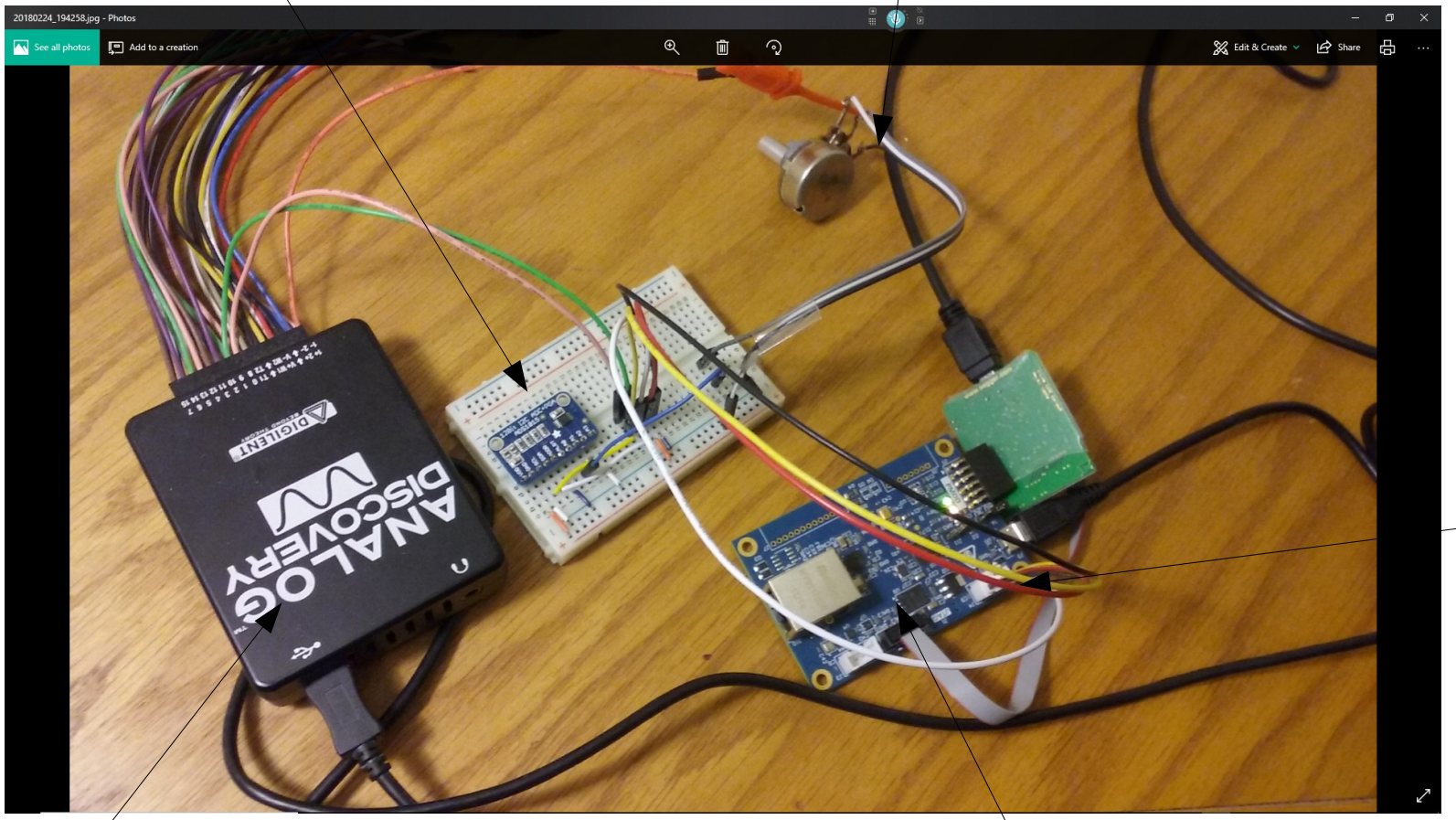
Need to add external 4.7K pull up resistors for P4_10/11



Reconfigure this port as I2C instead of UART port.

Adafruit TI ADS1015 ADC

Hardware setup I2C bus
(Grove B r_iic port)
(ADC part and Potentiometer)



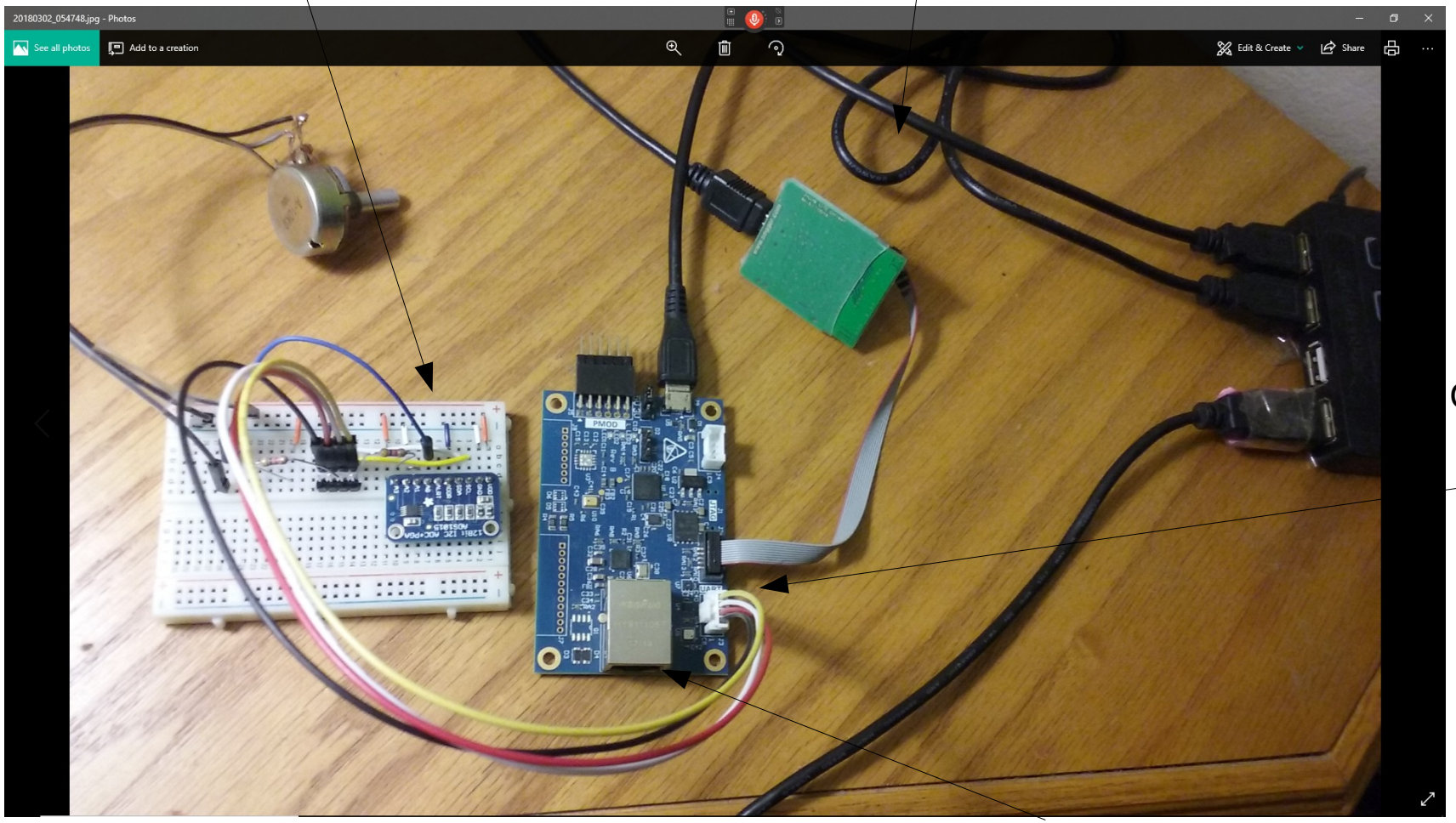
Grove B r_iic port

S5D9 IOT board

Scope

Adafruit TI ADS1015 ADC

Hardware setup I2C bus
(Grove A r_sci_i2c port)
(ADC part and Potentiometer)



Grove B r_sci_i2c port

S5D9 IOT board

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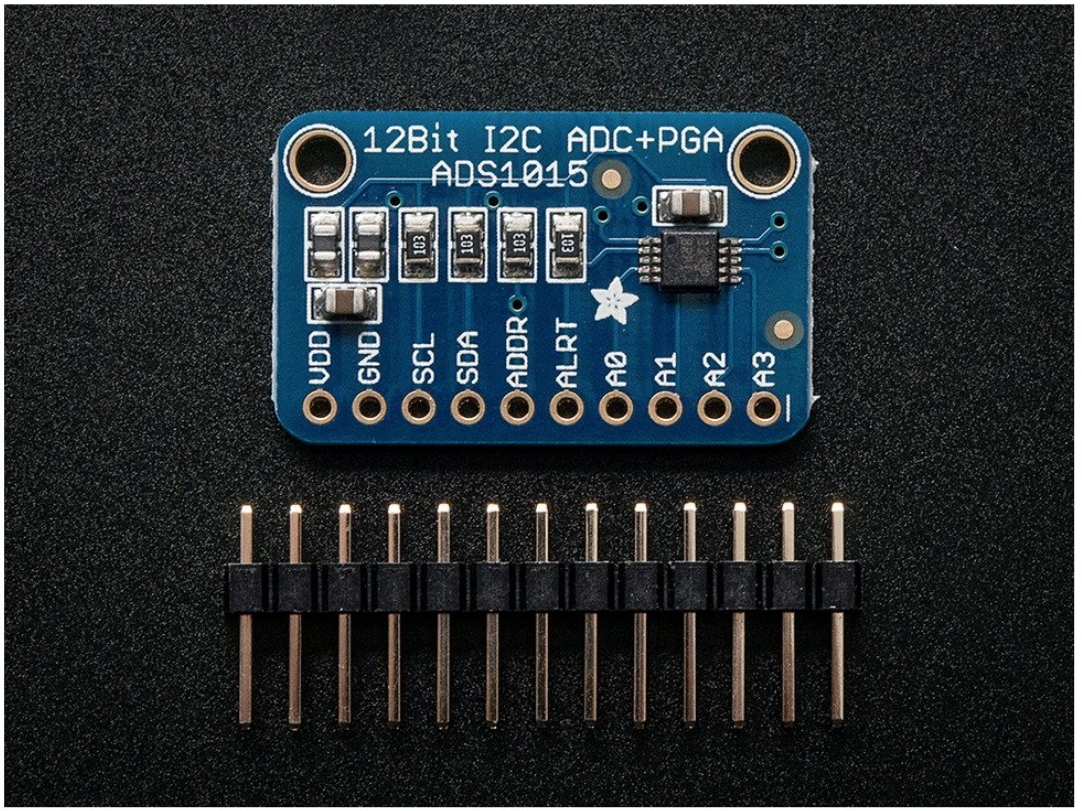
BREAKOUT BOARDS / ADS1015 12-BIT ADC - 4 CHANNEL WITH PROGRAMMABLE GAIN AMPLIFIER



ADS1015 12-Bit ADC - 4 Channel with Programmable Gain Amplifier

PRODUCT ID: 1083

$9.95

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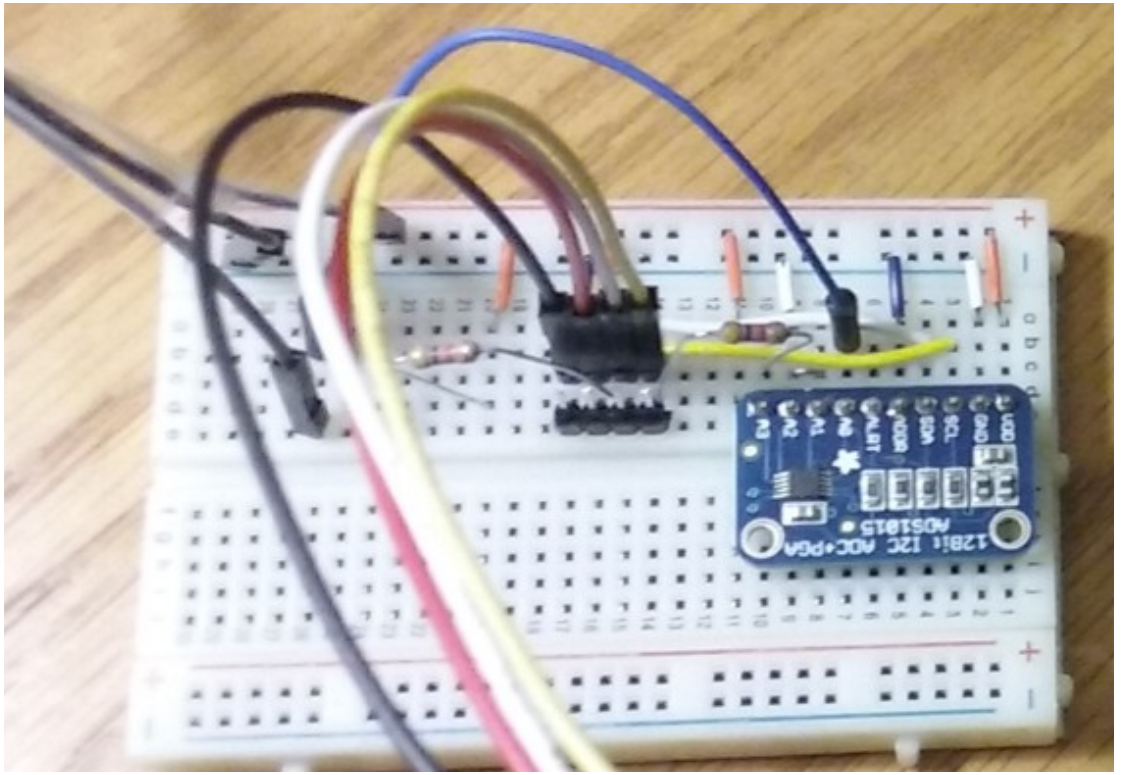
ADC connection



VCC = VCC
GND = GND
SCL = SCL
SDA = SDA
ADDR = GND
ALRT = NC
A0 = Potentiometer
A1/2/3 = GND (not used)

ADC Slave Address

I²C ADDRESS SELECTION

The ADS1013/4/5 have one address pin, ADDR, that sets the I²C address. This pin can be connected to ground, VDD, SDA, or SCL, allowing four addresses to be selected with one pin as shown in Table 5. The state of the address pin ADDR is sampled continuously.

Table 5. ADDR Pin Connection and Corresponding Slave Address

ADDR PIN	SLAVE ADDRESS
Ground	1001000
VDD	1001001
SDA	1001010
SCL	1001011

POINTER REGISTER

The four registers are accessed by writing to the Pointer register byte; see Figure 16. Table 6 and Table 7 indicate the Pointer register byte map.

Table 6. Register Address

BIT 1	BIT 0	REGISTER
0	0	Conversion register
0	1	Config register
1	0	Lo_thresh register
1	1	Hi_thresh register

Example: Configuration Register Read

Step 1: Slave address (48h) + w → Register address (01h)
Step 2: Slave address (48h) + r → 2 bytes of data read (8583h)

xample: Configuration Register Write and initiate one shot ADC conversion.

Step 1: Slave address (48h) + w → Register address (01h) + 2 bytes of data write (C383h)

Table 8. Conversion Register (Read-Only)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0

Voltage level = D[11:0] / 2048 x 4.096V (using +/-4096 FSR)

Example: Conversion Register Read

Step 1: Slave address (48h) + w → Register address (00h)
Step 2: Slave address (48h) + r → 2 bytes of data read (16 bits)

Default = 8583h (Config Register)

Table 9. Config Register (Read/Write)

BIT	15	14	13	12	11	10	9	8
NAME	OS	MUX2	MUX1	MUX0	PGA2	PGA1	PGA0	MODE
BIT	7	6	5	4	3	2	1	0
NAME	DR2	DR1	DR0	COMP_MODE	COMP_POL	COMP_LAT	COMP_QUE1	COMP_QUE0

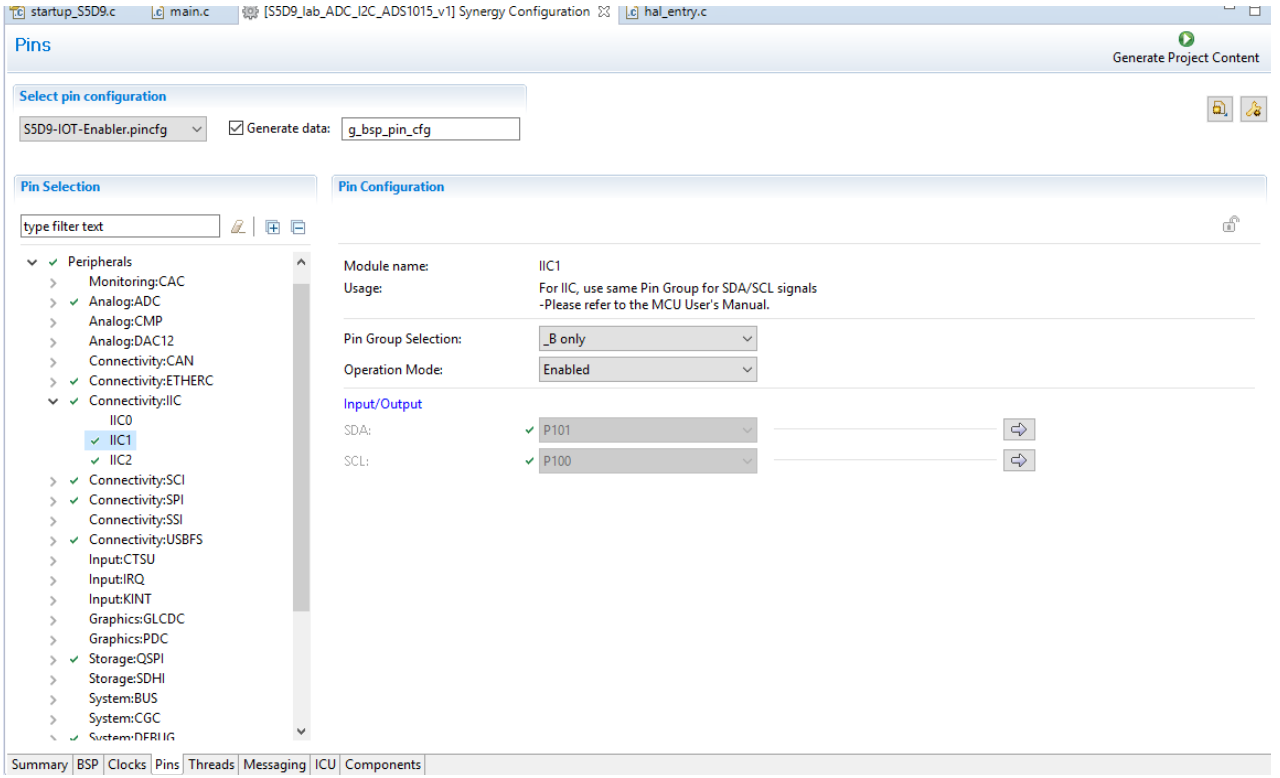
Default = 8583h.

Bit [15] **OS: Operational status/single-shot conversion start**

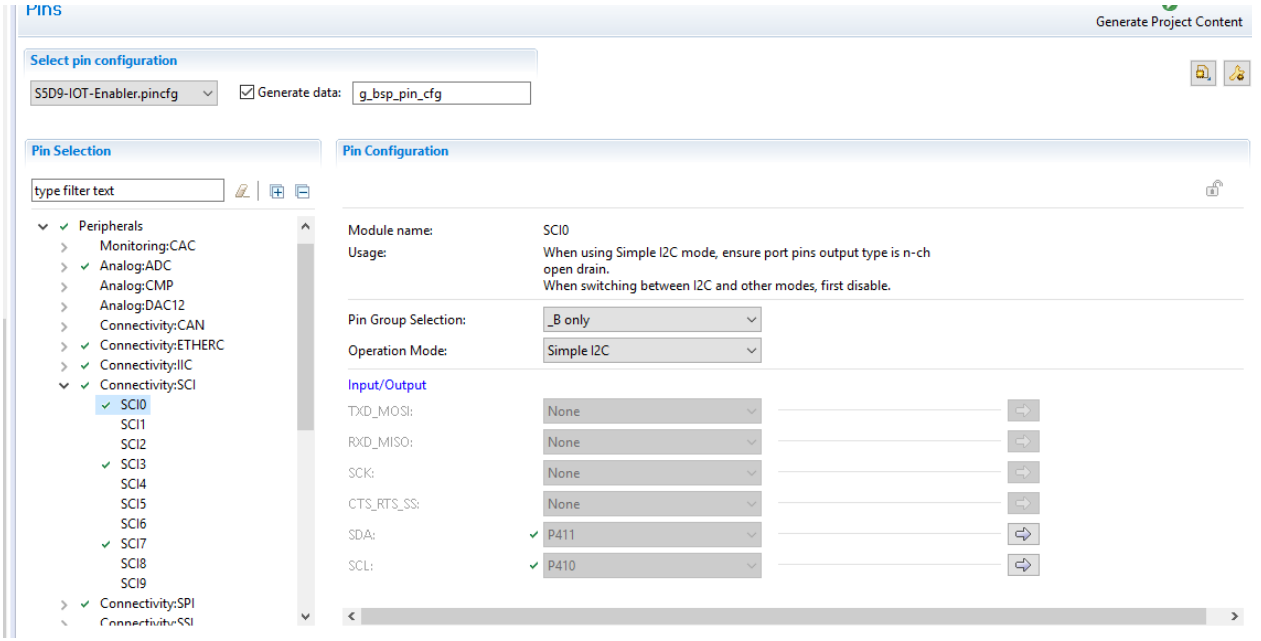
This bit determines the operational status of the device.
This bit can only be written when in power-down mode.

For a write status:
0 : No effect
1 : Begin a single conversion (when in power-down mode)
For a read status:
0 : Device is currently performing a conversion
1 : Device is not currently performing a conversion

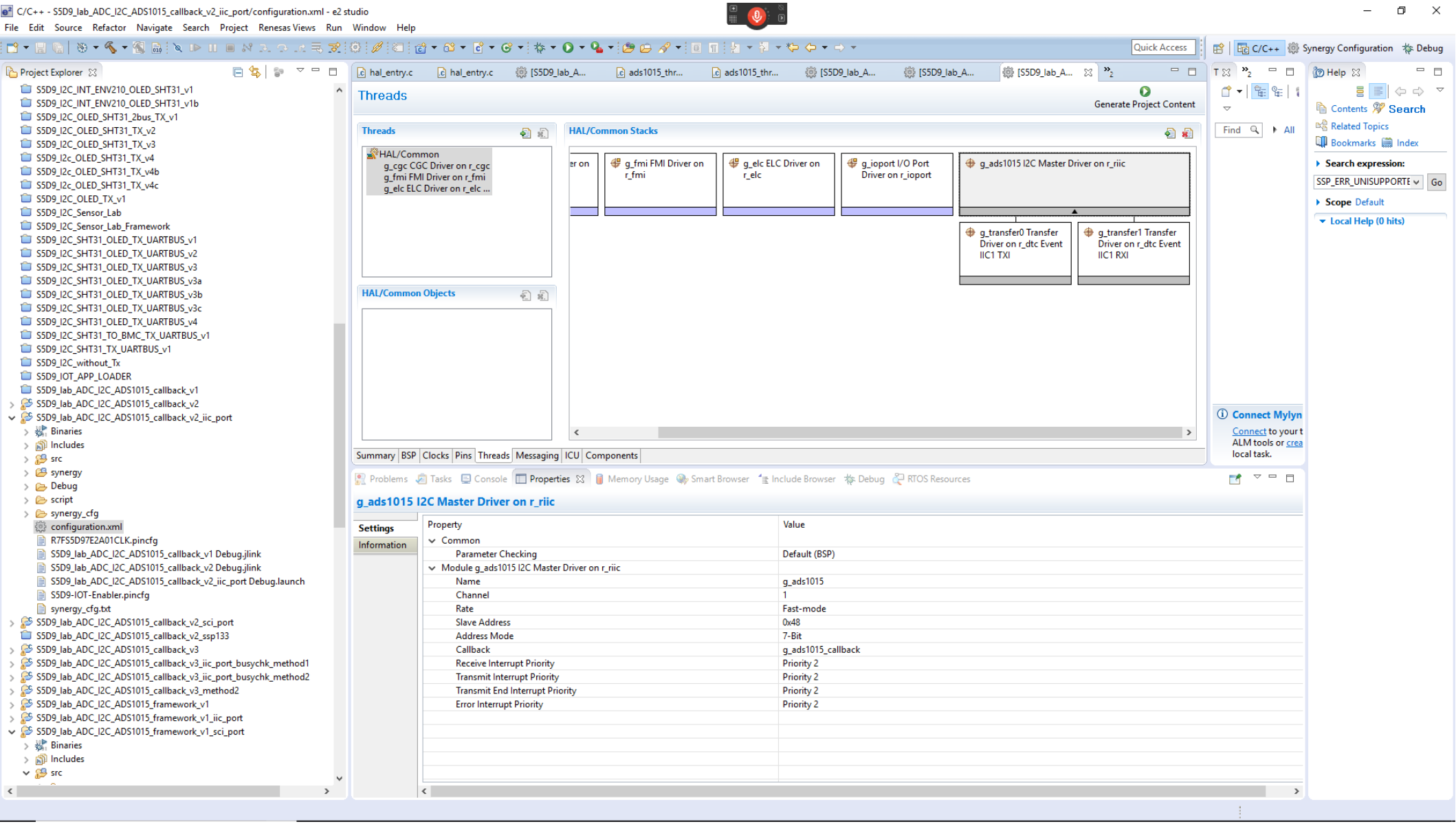
IIC Channel 1



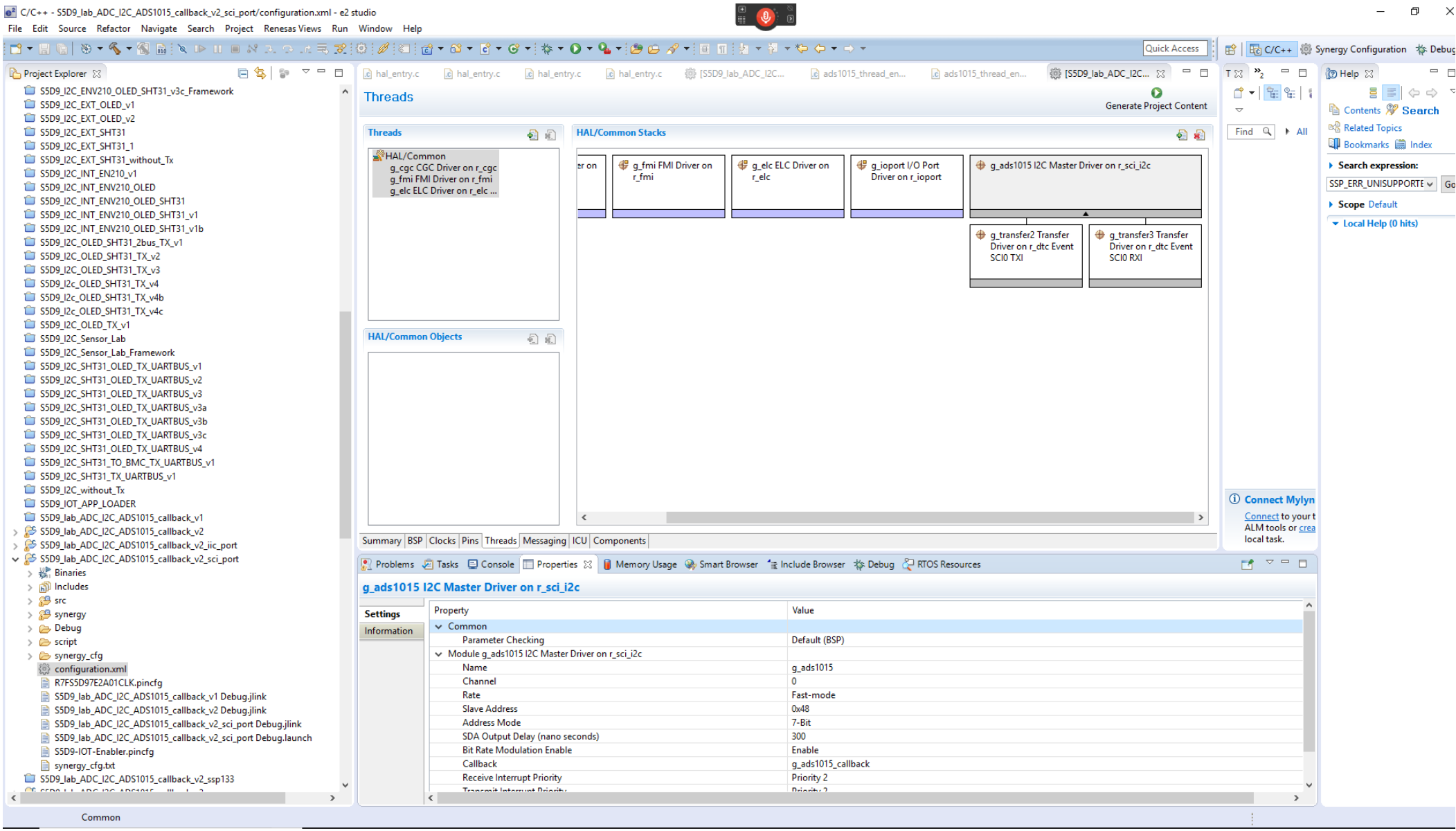
SCI Channel 0



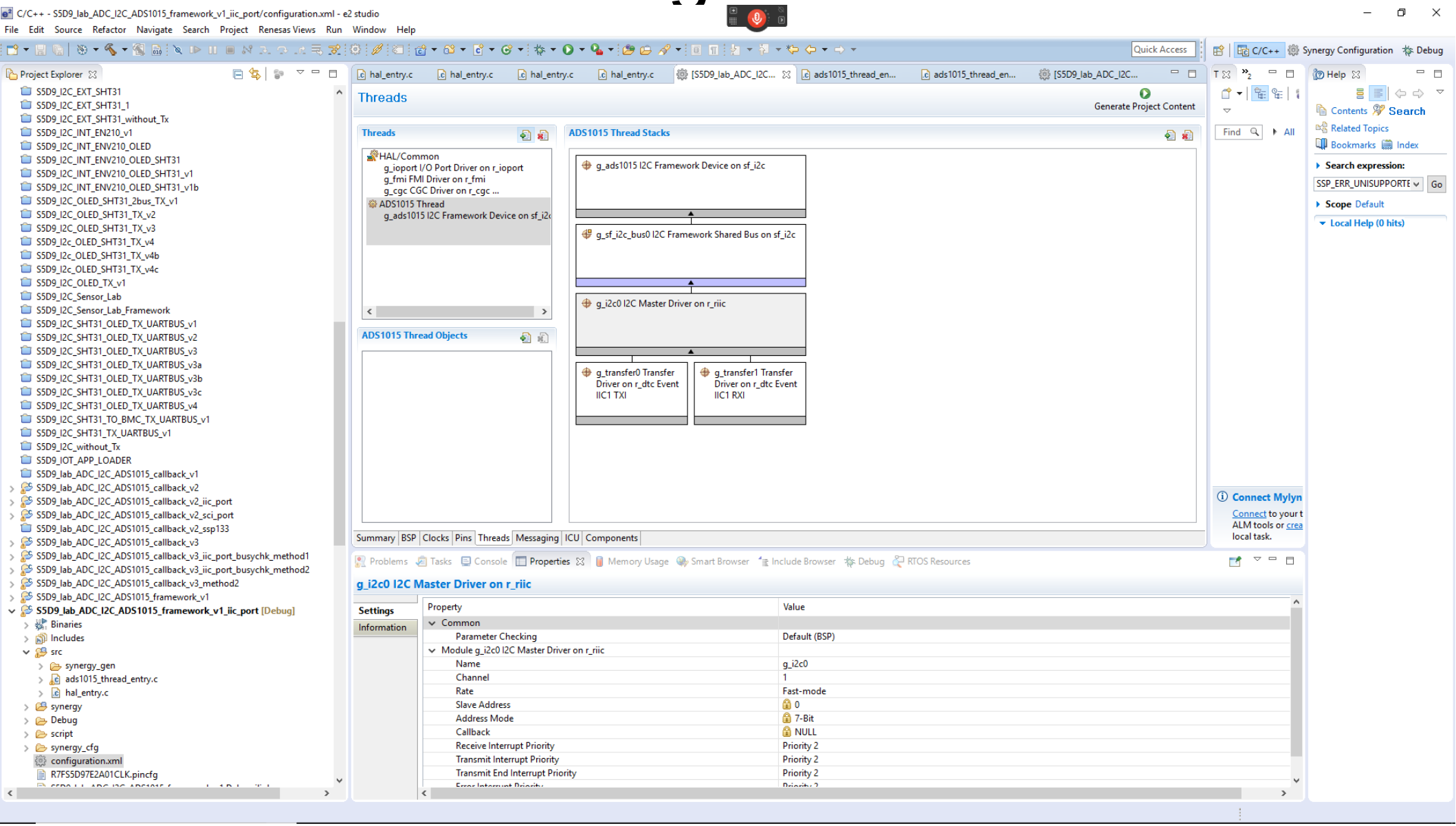
r_iic driver


C/C++ - S5D9_lab_ADC_I2C_ADS1015_callback_v2_iic_port/configuration.xml - e2 studio
File Edit Source Refactor Navigate Search Project Renesas Views Run Window Help
Project Explorer
S5D9_I2C_INT_ENV210_OLED_SHT31_v1
S5D9_I2C_INT_ENV210_OLED_SHT31_v1b
S5D9_I2C_OLED_SHT31_2bus_TX_v1
S5D9_I2C_OLED_SHT31_TX_v2
S5D9_I2C_OLED_SHT31_TX_v3
S5D9_I2c_OLED_SHT31_TX_v4
S5D9_I2c_OLED_SHT31_TX_v4b
S5D9_I2c_OLED_SHT31_TX_v4c
S5D9_I2C_OLED_TX_v1
S5D9_I2C_Sensor_Lab
S5D9_I2C_Sensor_Lab_Framework
S5D9_I2C_SHT31_OLED_TX_UARTBUS_v1
S5D9_I2C_SHT31_OLED_TX_UARTBUS_v2
S5D9_I2C_SHT31_OLED_TX_UARTBUS_v3
S5D9_I2C_SHT31_OLED_TX_UARTBUS_v3a
S5D9_I2C_SHT31_OLED_TX_UARTBUS_v3b
S5D9_I2C_SHT31_OLED_TX_UARTBUS_v3c
S5D9_I2C_SHT31_OLED_TX_UARTBUS_v4
S5D9_I2C_SHT31_TO_BMC_TX_UARTBUS_v1
S5D9_I2C_SHT31_TX_UARTBUS_v1
S5D9_I2C_without_Tx
S5D9_IOT_APP_LOADER
S5D9_lab_ADC_I2C_ADS1015_callback_v1
S5D9_lab_ADC_I2C_ADS1015_callback_v2
S5D9_lab_ADC_I2C_ADS1015_callback_v2_iic_port
Binaries
Includes
src
synergy
Debug
script
synergy_cfg
configuration.xml
R7FS5D97E2A01CLK.pincfg
S5D9_lab_ADC_I2C_ADS1015_callback_v1 Debug.jlink
S5D9_lab_ADC_I2C_ADS1015_callback_v2 Debug.jlink
S5D9_lab_ADC_I2C_ADS1015_callback_v2_iic_port Debug.launch
S5D9-IOT-Enabler.pincfg
synergy_cfg.txt
S5D9_lab_ADC_I2C_ADS1015_callback_v2_sci_port
S5D9_lab_ADC_I2C_ADS1015_callback_v2_ssp133
S5D9_lab_ADC_I2C_ADS1015_callback_v3
S5D9_lab_ADC_I2C_ADS1015_callback_v3_iic_port_busychk_method1
S5D9_lab_ADC_I2C_ADS1015_callback_v3_iic_port_busychk_method2
S5D9_lab_ADC_I2C_ADS1015_callback_v3_method2
S5D9_lab_ADC_I2C_ADS1015_framework_v1
S5D9_lab_ADC_I2C_ADS1015_framework_v1_iic_port
S5D9_lab_ADC_I2C_ADS1015_framework_v1_sci_port
Binaries
Includes
src
Quick Access
C/C++
Synergy Configuration
Debug
hal_entry.c
hal_entry.c
[S5D9_lab_A...
ads1015_thr...
ads1015_thr...
[S5D9_lab_A...
[S5D9_lab_A...
[S5D9_lab_A...
Threads
Generate Project Content
Threads
HAL/Common
g_cgc CGC Driver on r_cgc
g_fmi FMI Driver on r_fmi
g_elc ELC Driver on r_elc ...
HAL/Common Objects
HAL/Common Stacks
g_fmi FMI Driver on r_fmi
g_elc ELC Driver on r_elc
g_ioport I/O Port Driver on r_ioport
g_ads1015 I2C Master Driver on r_riic
g_transfer0 Transfer Driver on r_dtc Event IIC1 TXI
g_transfer1 Transfer Driver on r_dtc Event IIC1 RXI
Summary BSP Clocks Pins Threads Messaging ICU Components
Problems Tasks Console Properties Memory Usage Smart Browser Include Browser Debug RTOS Resources
g_ads1015 I2C Master Driver on r_riic
Settings
Information
Property
Value
Common
Parameter Checking
Default (BSP)
Module g_ads1015 I2C Master Driver on r_riic
Name
g_ads1015
Channel
1
Rate
Fast-mode
Slave Address
0x48
Address Mode
7-Bit
Callback
g_ads1015_callback
Receive Interrupt Priority
Priority 2
Transmit Interrupt Priority
Priority 2
Transmit End Interrupt Priority
Priority 2
Error Interrupt Priority
Priority 2
Find
All
Connect Mylyn
Connect to your t
ALM tools or crea
local task.
Help
Contents
Search
Related Topics
Bookmarks
Index
Search expression:
SSP_ERR_UNISUPPORTE
Go
Scope Default
Local Help (0 hits)

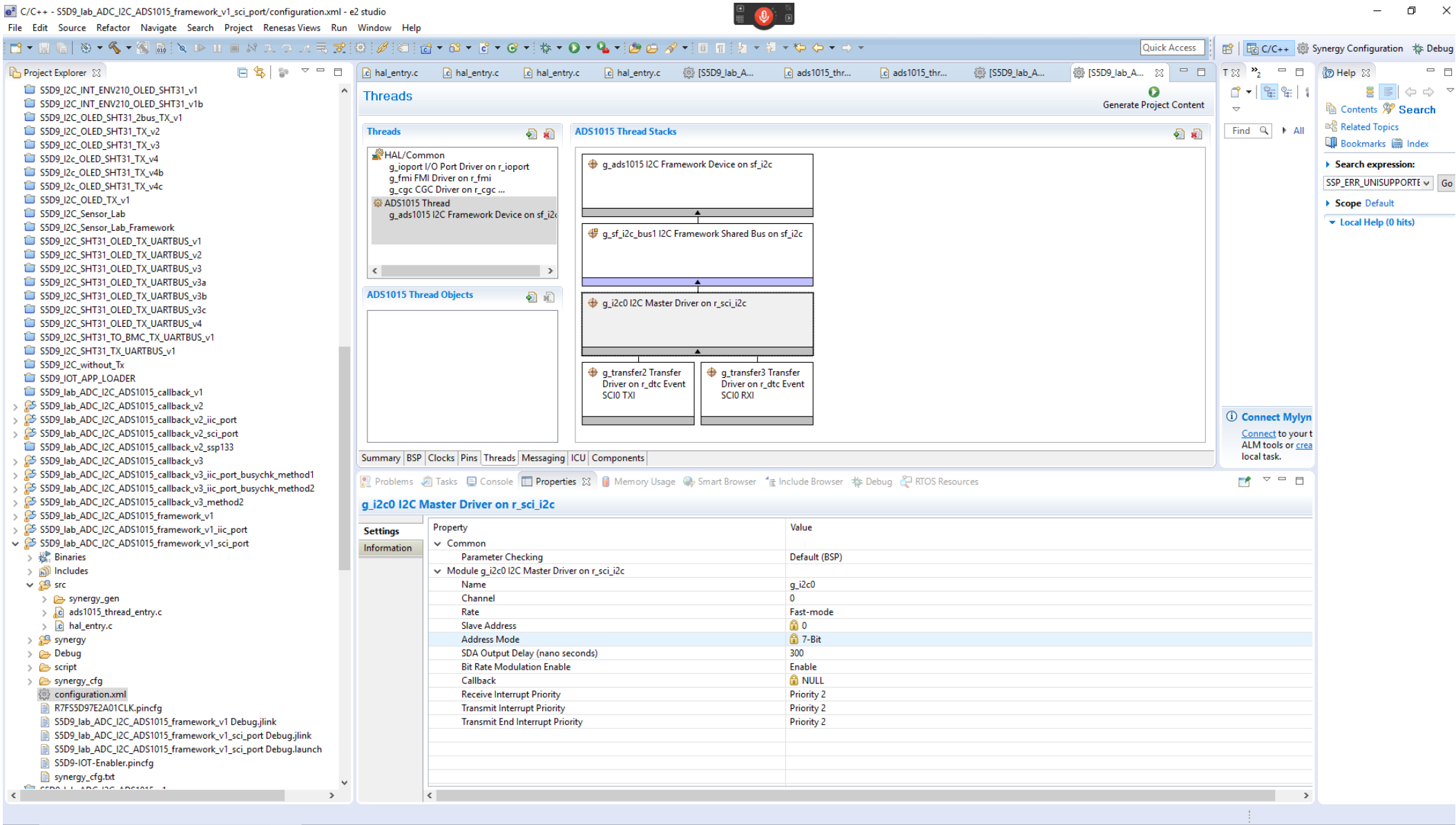
r_sci_i2c driver



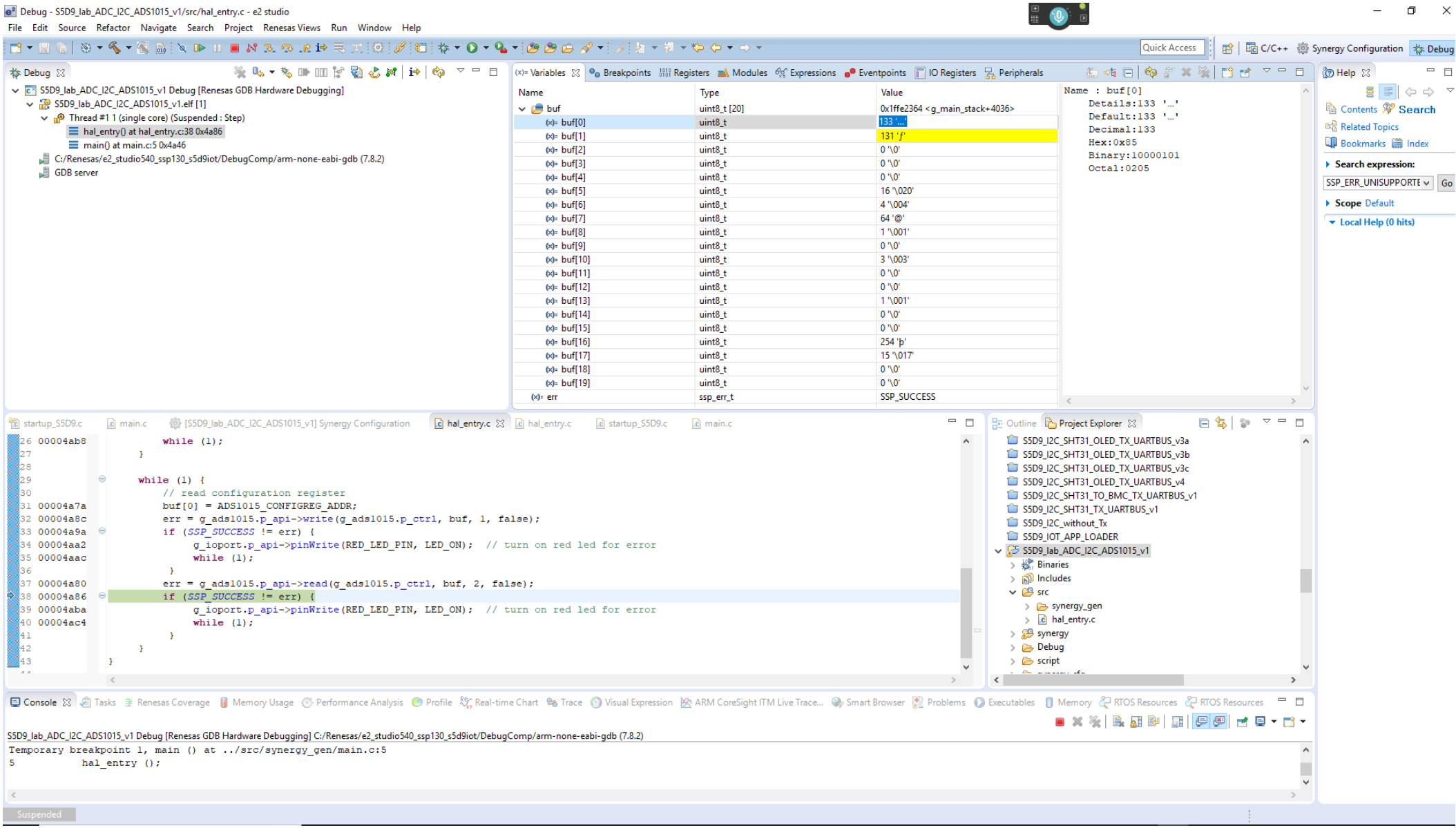
Framework with the r_iic driver configuration



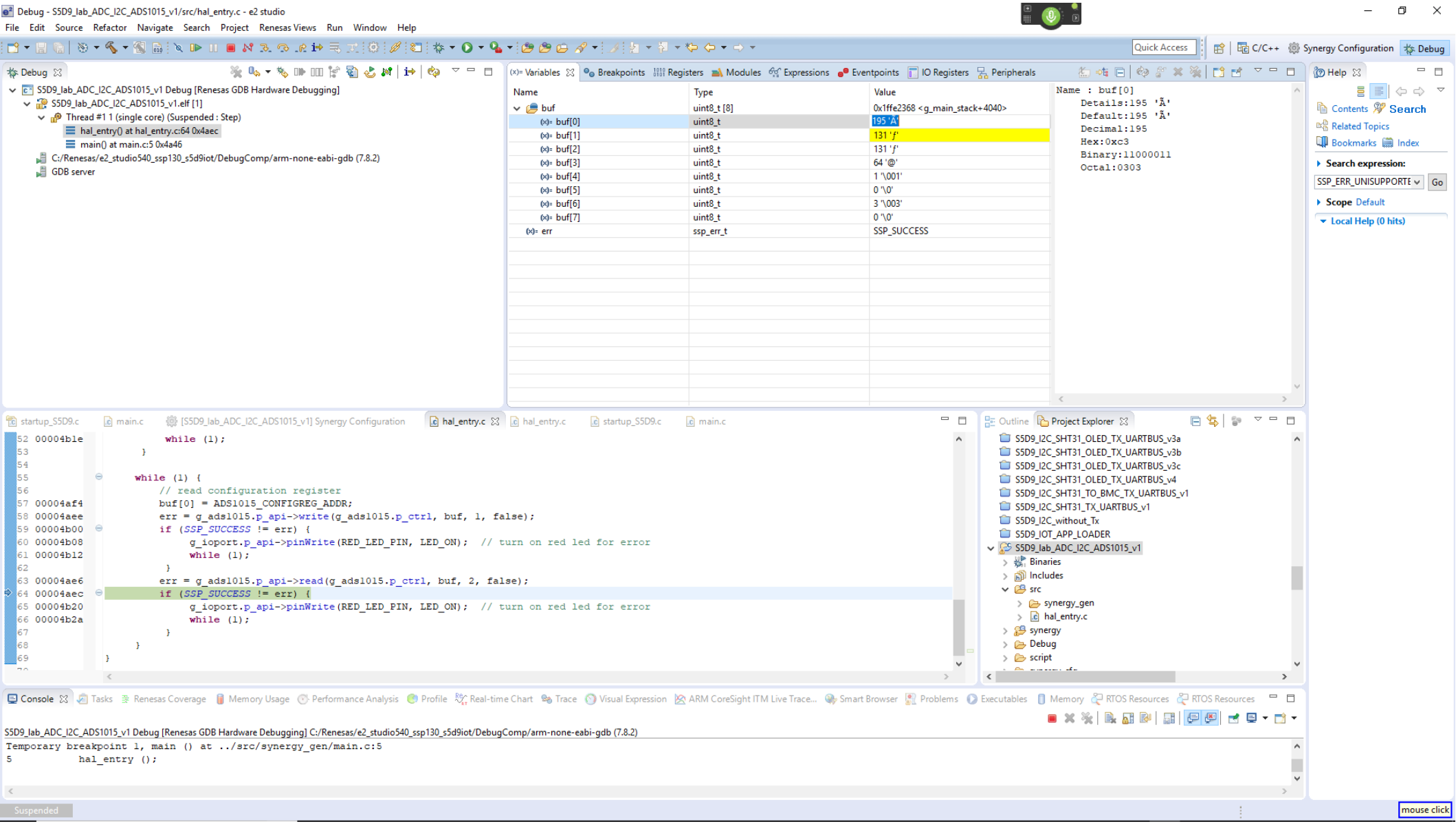
Framework with the r_sci_i2c driver configuration



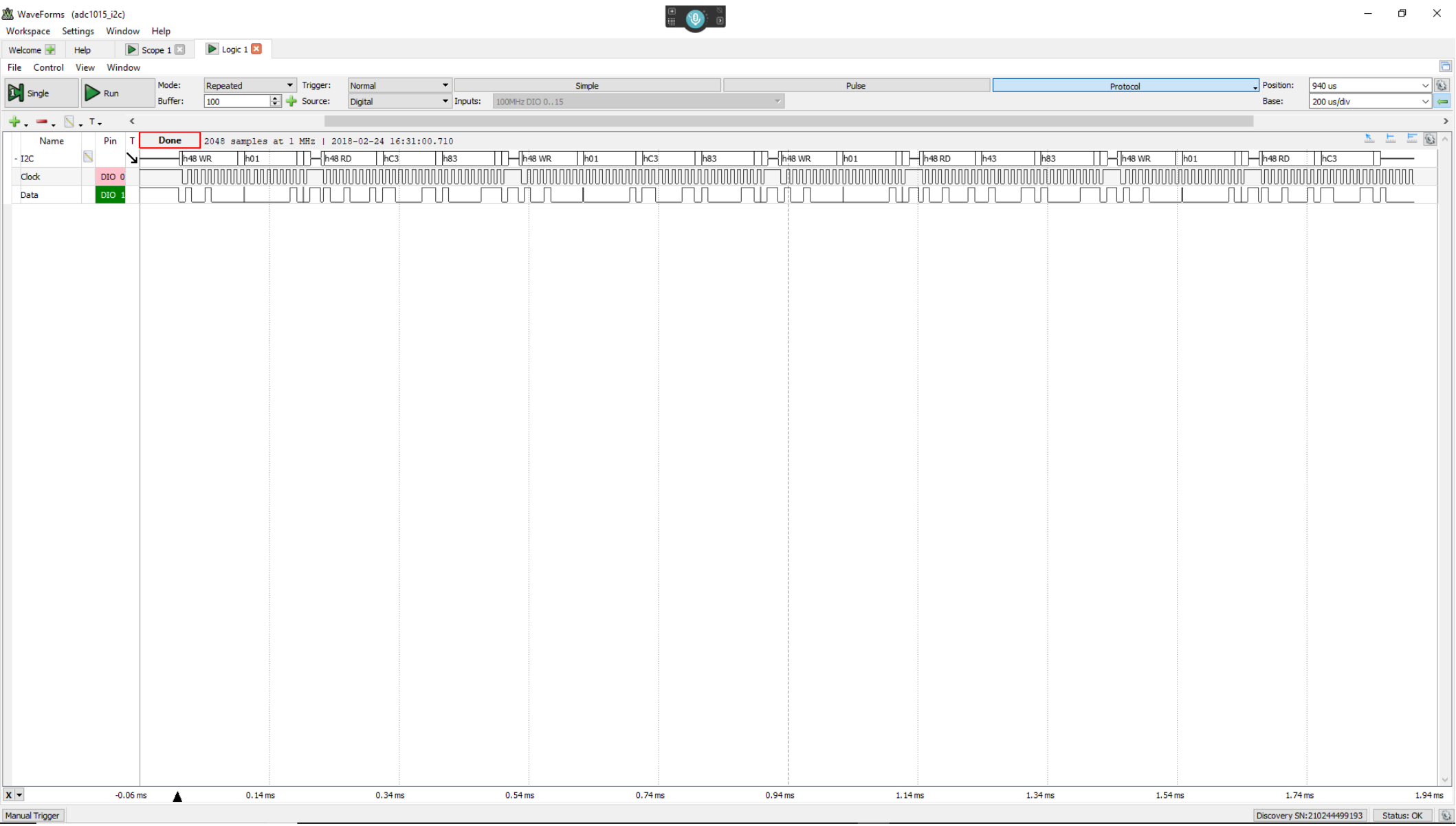
Configuration Register read
Buf[0] = 85h and Buf[1] = 83h



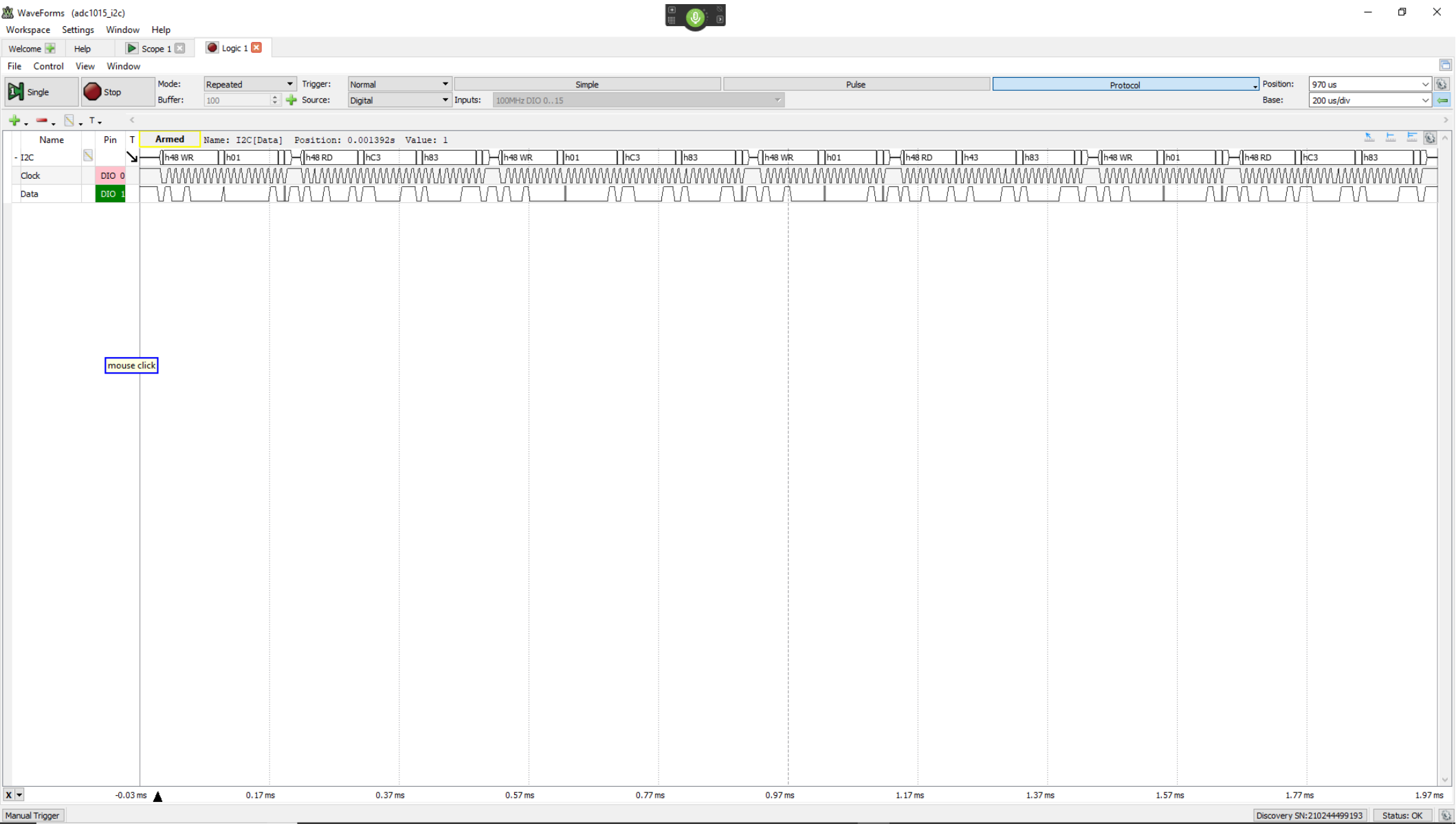
Configuration Register write/read Buf[0] = C3h and Buf[1] = 83h



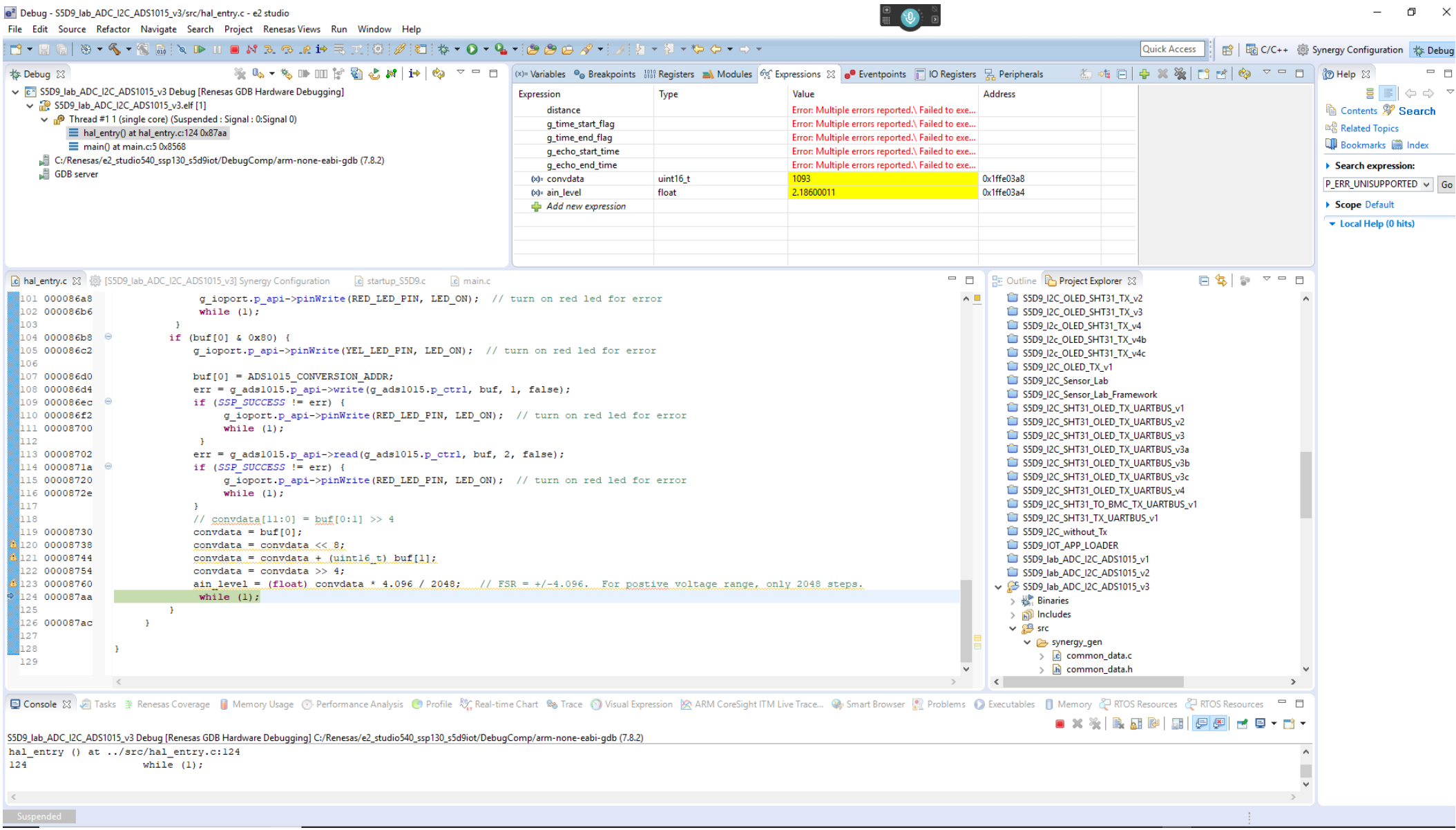
C3 (1100_0011) → 43 (0100_0011) good
WR OS bit → RD OS bit (0=busy)

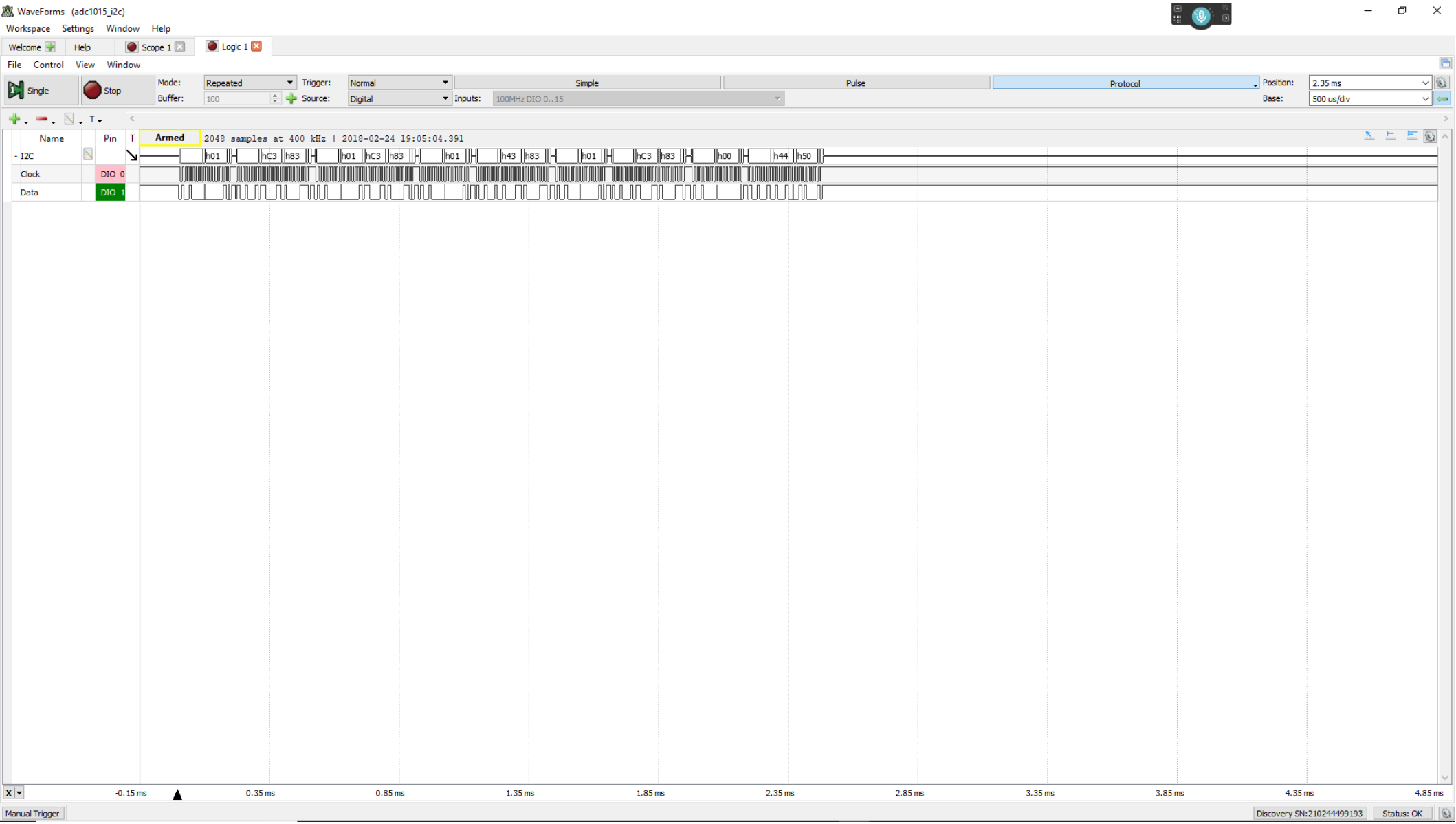


Stop when OS bit = 1



0x4450 → 0x445 or 1093
1093 / 2048 x 4.096 = 2.186V
FSR +/- 4.096 and only positive side use 2048




WaveForms (adc1015_i2c)
Workspace Settings Window Help
Welcome Help Scope 1 Logic 1
File Control View Window
Single Stop
Mode: Repeated Trigger: Normal Simple Pulse Protocol Position: 2.35 ms
Buffer: 100 Source: Digital Inputs: 100MHz DIO 0..15 Base: 500 us/div
Name Pin T Armed 2048 samples at 400 kHz | 2018-02-24 19:05:04.391
I2C
Clock DIO 0
Data DIO 1
h01 hC3 h83 h01 hC3 h83 h01 h43 h83 h01 hC3 h83 h00 h44 h50
-0.15 ms 0.35 ms 0.85 ms 1.35 ms 1.85 ms 2.35 ms 2.85 ms 3.35 ms 3.85 ms 4.35 ms 4.85 ms
Manual Trigger
Discovery SN:210244499193
Status: OK

0.379 Khz (fast mode)