Radiation-Hardened FPGA Implementation of an Adaptive Symbol Mapper for 6G Satellite Communications: A Simulation-Based Study

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I. EXTENDED ABSTRACT

The emergence of 6G satellite communication systems, particularly those leveraging Low Earth Orbit (LEO) and Very Low Earth Orbit (VLEO) constellations, marks a transformative step toward achieving seamless, high-capacity, and ultra-reliable global connectivity [1]. In this sense, the deployment of so-called non-terrestrial networks (NTNs) has become increasingly important in ensuring the connectivity and performance characteristics that define the 6G paradigm. The concept of Non-Terrestrial Network (NTN) integration was initially proposed by the Third Generation Partnership Project (3GPP) for 5G mobile networks. According to the definition established by 3GPP, NTN refers to any network or network segment that uses an aircraft or spacecraft to access a transmission equipment relay node or base station [2].

The NTN systems are expected to enable global connectivity, supporting a wide range of applications, from massive machine-type communications to ultra-low-latency services. To achieve this, there is a need for new fault-tolerant Physical Layer (PHY) technologies capable of withstanding the harsh space environment. One of the main functions of the PHY layer is modulation, a method for converting digital data into a form suitable for transmission over a communication channel. To guarantee the enhanced reliability demanded by the 6G standard, the modulation process must ensure an acceptable BER (bit error rate) level. **In this sense, the adaptive modulation plays a pivotal role in meeting these requirements by dynamically adjusting the modulation scheme based on real-time channel conditions [3]-[4]. A higher-order modulation scheme increases the data rate in good channel conditions, for example, when the signal-to-noise ratio (SNR) is high. Conversely, in poor channel conditions (low SNR), a lower-order modulation scheme is used to ensure a**

**more robust and reliable link.** A further challenge in space-based communication systems is their operation in a harsh

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environment exposed to high-energy particles that can cause the well-known Single Event Effects (SEEs). SEEs are associated with the impact of a single particle, which can lead to data corruption or malfunction, also known as Single Event Transient (SET) and Single Event Upset (SEU) [5]. To counteract these undesired effects, dedicated radiation-hardening techniques must be implemented. In this context, this paper presents a case study to evaluate the fault tolerance of an adaptive symbol mapper in the presence of radiation-induced effects.

Previous studies have analyzed radiation effects in various components of wireless communication systems, like encoders/decoders [6]-[7] and analogue RF elements, such as Low Noise Amplifiers (LNAs) [8]. To the best of our knowledge, there is no comprehensive analysis of the radiation effects on digital symbol mappers.

As presented in Table 1, the modulation schemes selected for this study are Phase Shift Keying (PSK), Quadrature Amplitude Modulation (QAM), and Amplitude Phase Shift Keying (APSK), each supporting multiple modulation orders with varying constellation sizes.

TABLE I

Selected modulation schemes

|  |  |  |
| --- | --- | --- |
| **Type of modulation** | **Modulation Scheme** | **Bits per symbol** |
| *Phase Shift Keying* | ***BPSK*** | ***1*** |
| ***QPSK*** | ***2*** |
| ***Quadrature Amplitude Modulation*** | ***16-QAM*** | ***4*** |
| ***32-QAM*** | ***5*** |
| ***64-QAM*** | ***6*** |
| ***Amplitude and Phase Shift Keying*** | ***16-APSK*** | ***4*** |
| ***32-APSK*** | ***5*** |
| ***64-APSK*** | ***6*** |

The symbol mapper was designed in VHDL using the Xilinx Vivado design suite and integrated into a single-carrier baseband transmitter, whose block diagram is illustrated in Figure 1. For functional validation, the transmitter was synthesized and implemented on an FPGA

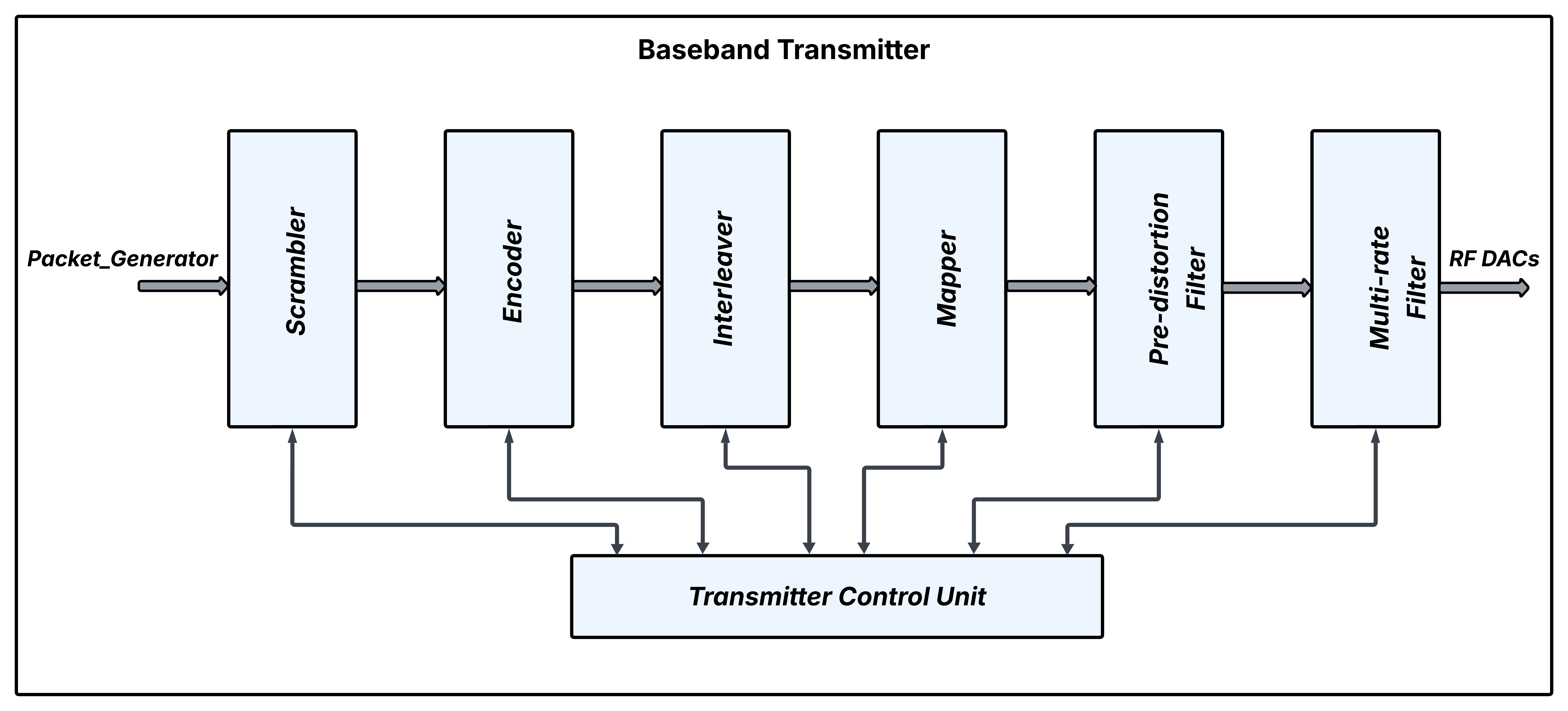
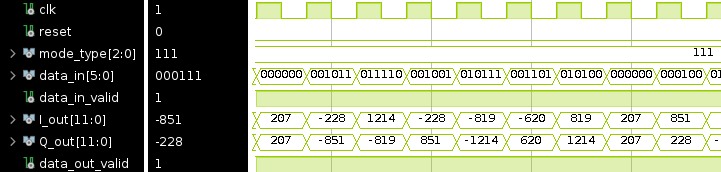


Fig. 1. Baseband transmitter block diagram.

platform. A digital symbol mapper translates the input bits into complex symbols, where each symbol is uniquely defined by its In-Phase (I) and Quadrature (Q) coordinates within a constellation diagram. The output simulation waveforms depicted in Figures 2 and 3 present two examples of symbol mapping processing, respectively for 64-APSK and 64-QAM modulations, with each complex symbol expressed as a signed decimal value.

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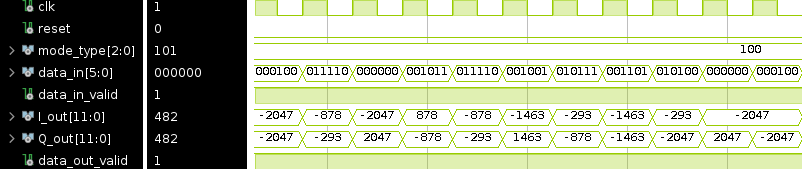
 Fig. 2. 64-APSK modulation waveform.

Fig. 3. 64-QAM modulation waveform.

The fault injection analysis will be conducted at the register-transfer level (RTL) using Cadence Xcelium simulator to characterize the system´s behaviour under fault conditions. As radiation hardening techniques are closely tied to the characteristics of the target hardware platform, this work focuses on Radiation Hardening by Design (RHBD) approaches typical of FPGAs [9]. Such systems are generally protected through redundant logic structures, including Triple Module Redundancy (TMR) and Error Correction Codes (ECCs), which enhance fault tolerance against radiation-induced effects. The final results are expected to identify the most vulnerable element of the symbol mapper and suggest potential mitigation strategies.

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