TL1963A-xx 1.5-A Low-Noise Fast-Transient-Response Low-Dropout Regulator

1 Features

- Optimized for Fast Transient Response
- Output Current: 1.5 A
- Dropout Voltage: 340 mV
- Low Noise: 40 μV_{RMS} (10 Hz to 100 kHz)
- 1-mA Quiescent Current
- No Protection Diodes Needed
- Controlled Quiescent Current in Dropout
- Fixed Output Voltages: 1.5 V, 1.8 V, 2.5 V, 3.3 V
- Adjustable Output from 1.21 V to 20 V (TL1963A Only)
- Less Than 1-µA Quiescent Current in Shutdown
- Stable With 10-µF Ceramic Output Capacitor
- Reverse-Battery Protection
- Reverse-Current Protection

2 Applications

- Industrial
- Wireless Infrastructure
- Radio-Frequency Systems
- 3.3-V to 2.5-V Logic Power Supplies
- Post Regulator for Switching Supplies

3 Description

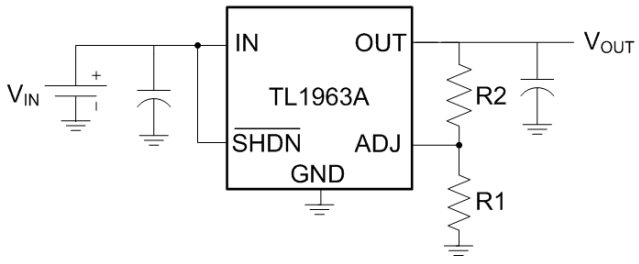
The TL1963A-xx devices are low-dropout (LDO) regulators optimized for fast transient response. The device can supply 1.5 A of output current with a dropout voltage of 340 mV. Operating quiescent current is 1 mA, dropping to less than 1 µA in shutdown. Quiescent current is well controlled; it does not rise in dropout as with many other regulators. In addition to fast transient response, the TL1963A-xx regulators have very low output noise, which makes them ideal for sensitive RF supply applications.

Device Information(1)

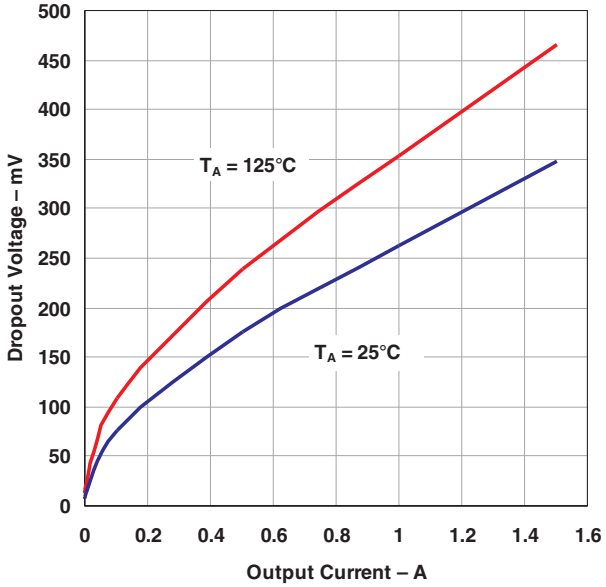
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TL1963A	SOT (6)	6.50 mm × 3.50 mm
	TO-263 (5)	10.16 mm × 8.42 mm
TL1963A-15	SOT (6)	6.50 mm × 3.50 mm
	SOT (4)	
	TO-263 (5)	10.16 mm × 8.42 mm
TL1963A-18	SOT (6)	6.50 mm × 3.50 mm
	SOT (4)	
	TO-263 (5)	10.16 mm × 8.42 mm
TL1963A-25	SOT (6)	6.50 mm × 3.50 mm
	SOT (4)	
	TO-263 (5)	10.16 mm × 8.42 mm
TL1963A-33	SOT (6)	6.50 mm × 3.50 mm
	SOT (4)	
	TO-263 (5)	10.16 mm × 8.42 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Dropout Voltage vs Output Current



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4 Revision History

Changes from Revision F (January 2014) to Revision G **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Description (continued)

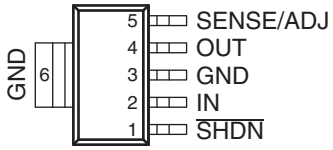
Output voltage range is from 1.21 V to 20 V. The TL1963A-xx regulators are stable with output capacitance as low as 10 µF. Small ceramic capacitors can be used without the necessary addition of ESR as is common with other regulators. Internal protection circuitry includes reverse-battery protection, current limiting, thermal limiting, and reverse-current protection. The devices are available in fixed output voltages of 1.5 V, 1.8 V, 2.5 V, 3.3 V, and as an adjustable device with a 1.21-V reference voltage.

6 Device Comparison Table

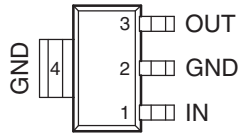
DEVICE	OUTPUT VOLTAGE	PIN 5 (DCQ AND KTT ONLY)
TL1963A	Adjustable	ADJ
TL1963A-15	1.5 V	SENSE
TL1963A-18	1.8 V	SENSE
TL1963A-25	2.5 V	SENSE
TL1963A-33	3.3 V	SENSE

7 Pin Configuration and Functions

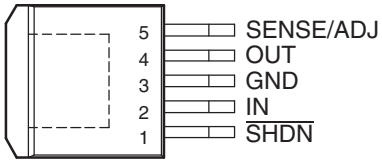
DCQ PACKAGE
(TOP VIEW)



DCY PACKAGE
(TOP VIEW)



KTT PACKAGE
(TOP VIEW)



Pin Functions

PIN				I/O	DESCRIPTION
NAME	DCQ	DCY	KTT		
ADJ	5	—	5	I	Adjust. For the adjustable TL1963A, this is the input to the error amplifier. This pin is clamped internally to ±7 V. It has a bias current of 3 µA that flows into the pin. The ADJ pin voltage is 1.21 V referenced to ground, and the output voltage range is 1.21 V to 20 V.
GND	3, 6	2, 4	3	—	Ground
IN	2	1	2	I	Input. Power is supplied to the device through the IN pin. A bypass capacitor is required on this pin if the device is more than six inches away from the main input filter capacitor. In general, the output impedance of a battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor (ceramic) in the range of 1 µF to 10 µF is sufficient. The TL1963A-xx regulators are designed to withstand reverse voltages on the IN pin with respect to ground and the OUT pin. In the case of a reverse input, which can happen if a battery is plugged in backwards, the device acts as if there is a diode in series with its input. There is no reverse-current flow into the regulator, and no reverse voltage appears at the load. The device protects both itself and the load.
OUT	4	3	4	O	Output. The output supplies power to the load. A minimum output capacitor (ceramic) of 10 µF is required to prevent oscillations. Larger output capacitors are required for applications with large transient loads to limit peak voltage transients.
SENSE	5	—	5	I	Sense. For fixed voltage versions of the TL1963A-xx (TL1963A-1.5, TL1963A-1.8, TL1963A-2.5, and TL1963A-3.3), the SENSE pin is the input to the error amplifier. Optimum regulation is obtained at the point where the SENSE pin is connected to the OUT pin of the regulator. In critical applications, small voltage drops are caused by the resistance (R_P) of PC traces between the regulator and the load. These may be eliminated by connecting the SENSE pin to the output at the load as shown in Figure 32. Note that the voltage drop across the external PCB traces adds to the dropout voltage of the regulator. The SENSE pin bias current is 600 µA at the rated output voltage. The SENSE pin can be pulled below ground (as in a dual supply system in which the regulator load is returned to a negative supply) and still allow the device to start and operate.
$\overline{\text{SHDN}}$	1	—	1	I	Shutdown. The $\overline{\text{SHDN}}$ pin is used to put the TL1963A-xx regulators into a low-power shutdown state. The output is off when the $\overline{\text{SHDN}}$ pin is pulled low. The $\overline{\text{SHDN}}$ pin can be driven either by 5-V logic or open-collector logic with a pullup resistor. The pullup resistor is required to supply the pullup current of the open-collector gate, normally several microamperes, and the $\overline{\text{SHDN}}$ pin current, typically 3 µA. If unused, the $\overline{\text{SHDN}}$ pin must be connected to V_{IN}. The device is in the low-power shutdown state if the $\overline{\text{SHDN}}$ pin is not connected.
Thermal Pad	—	—	—	—	For the KTT package, the exposed thermal pad is connected to ground and must be soldered to the PCB for rated thermal performance.

8 Specifications

8.1 Absolute Maximum Ratings

over operating virtual-junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage, V_{IN}	IN	–20	20	V
	OUT	–20	20	
	Input-to-output differential (2)	–20	20	
	SENSE	–20	20	
	ADJ	–7	7	
	$\overline{SHDN}$	–20	20	
Output short-circuit duration, t_{short}			Indefinite	
Maximum lead temperature (10-s soldering time), T_{lead}			300	°C
Maximum junction temperature, T_{JMAX}			125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to conditions beyond the recommended operating maximum for extended periods may affect device reliability.
(2) Absolute maximum input-to-output differential voltage cannot be achieved with all combinations of rated IN pin and OUT pin voltages. With the IN pin at 20 V, the OUT pin may not be pulled below 0 V. The total measured voltage from IN to OUT can not exceed ±20 V.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage range (1)	V_{OUT} + V_{DO}	20	V
V_{IH}	SHDN High-Level Input Voltage	2	20	V
V_{IL}	SHDN Low-Level Input Voltage		0.25	V
T_J	Recommended operating junction temperature range	–40	125	°C

(1) TL1963A, TL1963A-15, and TL1963A-18 may require a higher minimum input voltage under some output voltage/load conditions as indicated under *Electrical Characteristics*.

8.4 Thermal Information

THERMAL METRIC (1)(2)		TL1963A-xx			UNIT
		KTT	DCQ	DCY	
		5 PINS	6 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.9	50.5	57.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.6	31.1	38.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	18.9	5.1	7.1	
ψ_{JT}	Junction-to-top characterization parameter	5.7	1.0	1.7	
ψ_{JB}	Junction-to-board characterization parameter	17.3	5.0	7.0	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.0	—	—	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

8.5 Electrical Characteristics

Over recommended operating temperature range T_J = –40 to 125 °C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_J	MIN	TYP(2)	MAX	UNIT
V_{IN}	Minimum input voltage(3)(4)	I_{LOAD} = 0.5 A		25°C		1.9		V
		I_{LOAD} = 1.5 A		Full range		2.1	2.5	
V_{OUT}	Regulated output voltage(5)	TL1963A-15	V_{IN} = 2.21 V, I_{LOAD} = 1 mA	25°C	1.477	1.5	1.523	V
			V_{IN} = 2.5 V to 20 V, I_{LOAD} = 1 mA to 1.5 A	Full range	1.447	1.5	1.545	
		TL1963A-18	V_{IN} = 2.3 V, I_{LOAD} = 1 mA	25°C	1.773	1.8	1.827	
			V_{IN} = 2.8 V to 20 V, I_{LOAD} = 1 mA to 1.5 A	Full range	1.737	1.8	1.854	
		TL1963A-25	V_{IN} = 3 V, I_{LOAD} = 1 mA	25°C	2.462	2.5	2.538	
			V_{IN} = 3.5 V to 20 V, I_{LOAD} = 1 mA to 1.5 A	Full range	2.412	2.5	2.575	
		TL1963A-33	V_{IN} = 3.8 V, I_{LOAD} = 1 mA	25°C	3.25	3.3	3.35	
			V_{IN} = 4.3 V to 20 V, I_{LOAD} = 1 mA to 1.5 A	Full range	3.2	3.3	3.4	
V_{ADJ}	ADJ pin voltage(3)(5)	TL1963A	V_{IN} = 2.21 V, I_{LOAD} = 1 mA	25°C	1.192	1.21	1.228	V
			V_{IN} = 2.5 V to 20 V, I_{LOAD} = 1 mA to 1.5 A	Full range	1.174	1.21	1.246	
	Line regulation	TL1963A-15	ΔV_{IN} = 2.21 V to 20 V, I_{LOAD} = 1 mA	Full range		2	6	mV
		TL1963A-18	ΔV_{IN} = 2.3 V to 20 V, I_{LOAD} = 1 mA	Full range		2.5	7	
		TL1963A-25	ΔV_{IN} = 3 V to 20 V, I_{LOAD} = 1 mA	Full range		3	10	
		TL1963A-33	ΔV_{IN} = 3.8 V to 20 V, I_{LOAD} = 1 mA	Full range		3.5	10	
		TL1963A(3)	ΔV_{IN} = 2.21 V to 20 V, I_{LOAD} = 1 mA	Full range		1.5	5	
	Load regulation	TL1963A-15	V_{IN} = 2.5 V, ΔI_{LOAD} = 1 mA to 1.5 A	25°C		2	9	mV
				Full range			18	
		TL1963A-18	V_{IN} = 2.8 V, ΔI_{LOAD} = 1 mA to 1.5 A	25°C		2	10	
				Full range			20	
		TL1963A-25	V_{IN} = 3.5 V, ΔI_{LOAD} = 1 mA to 1.5 A	25°C		2.5	15	
				Full range			30	
		TL1963A-33	V_{IN} = 4.3 V, ΔI_{LOAD} = 1 mA to 1.5 A	25°C		3	20	
				Full range			70	
		TL1963A(3)	V_{IN} = 2.5 V, ΔI_{LOAD} = 1 mA to 1.5 A	25°C		2	8	
				Full range			18	

(1) The TL1963A-xx regulators are tested and specified under pulse load conditions such that $T_J \neq T_A$. They are fully tested at T_A = 25°C. Performance at –40 and 125°C is specified by design, characterization, and correlation with statistical process controls.
(2) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
(3) The TL1963A is tested and specified for these conditions with the ADJ pin connected to the OUT pin.
(4) For the TL1963A, TL1963A-15 and TL1963A-18, dropout voltages are limited by the minimum input voltage specification under some output voltage/load conditions.
(5) Operating conditions are limited by maximum junction temperature. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.

Electrical Characteristics (continued)

Over recommended operating temperature range T_J = –40 to 125 °C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_J	MIN	TYP(2)	MAX	UNIT
V_{DO}	Dropout voltage(4)(6)(7) $V_{IN} = V_{OUT(NOMINAL)}$	I_{LOAD} = 1 mA		25°C		0.02	0.06	V
				Full range			0.1	
		I_{LOAD} = 100 mA		25°C		0.1	0.17	
				Full range			0.22	
		I_{LOAD} = 500 mA		25°C		0.19	0.27	
				Full range			0.35	
		I_{LOAD} = 1.5 A		25°C		0.34	0.45	
				Full range			0.55	
I_{GND}	GND pin current(7)(8) $V_{IN} = V_{OUT(NOMINAL)}$ + 1	I_{LOAD} = 0 mA		Full range		1	1.5	mA
		I_{LOAD} = 1 mA		Full range		1.1	1.6	
		I_{LOAD} = 100 mA		Full range		3.8	5.5	
		I_{LOAD} = 500 mA		Full range		15	25	
		I_{LOAD} = 1.5 A		Full range		80	120	
e_N	Output voltage noise	C_{OUT} = 10 µF, I_{LOAD} = 1.5 A, B_W = 10 Hz to 100 kHz		25°C		40		μV_{RMS}
I_{ADJ}	ADJ pin bias current(3)(9)			25°C		3	10	µA
	Shutdown threshold	V_{OUT} = OFF to ON		Full range		0.9	2	V
		V_{OUT} = ON to OFF		Full range	0.25	0.75		
$I_{\overline{SHDN}}$	$\overline{SHDN}$ pin current	$V_{\overline{SHDN}}$ = 0 V		25°C		0.01	1	µA
		$V_{\overline{SHDN}}$ = 20 V		25°C		3	30	
	Quiescent current in shutdown	V_{IN} = 6 V, $V_{\overline{SHDN}}$ = 0 V		25°C		0.01	1	µA
	Ripple rejection	$V_{IN} – V_{OUT}$ = 1.5 V (avg), V_{RIPPLE} = 0.5 V_{P-P}, f_{RIPPLE} = 120 Hz, I_{LOAD} = 0.75 A		25°C	55	63		dB
I_{LIMIT}	Current limit	V_{IN} = 7 V, V_{OUT} = 0 V		25°C		2		A
		$V_{IN} = V_{OUT(NOMINAL)}$ + 1		Full range	1.6			
I_{IL}	Input reverse leakage current	V_{IN} = –20 V, V_{OUT} = 0 V		Full range			1	µA
I_{RO}	Reverse output current(10)	TL1963A-15	V_{OUT} = 1.5 V, V_{IN} < 1.5 V	25°C		600	1200	µA
		TL1963A-18	V_{OUT} = 1.8 V, V_{IN} < 1.8 V	25°C		600	1200	
		TL1963A-25	V_{OUT} = 2.5 V, V_{IN} < 2.5 V	25°C		600	1200	
		TL1963A-33	V_{OUT} = 3.3 V, V_{IN} < 3.3 V	25°C		600	1200	
		TL1963A	V_{OUT} = 1.21 V, V_{IN} < 1.21 V	25°C		300	600	

(6) Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage is equal to: $V_{IN} – V_{DROPOUT}$.
(7) To satisfy requirements for minimum input voltage, the TL1963A is tested and specified for these conditions with an external resistor divider (two 4.12-kΩ resistors) for an output voltage of 2.4 V. The external resistor divider adds a 300-µA DC load on the output.
(8) GND pin current is tested with V_{IN} = ($V_{OUT(NOMINAL)}$ + 1 V) and a current source load. The GND pin current decreases at higher input voltages.
(9) ADJ pin bias current flows into the ADJ pin.
(10) Reverse output current is tested with the IN pin grounded and the OUT pin forced to the rated output voltage. This current flows into the OUT pin and out the GND pin.

8.6 Typical Characteristics

Typical characteristics apply to all TL1963A-xx devices unless otherwise noted.

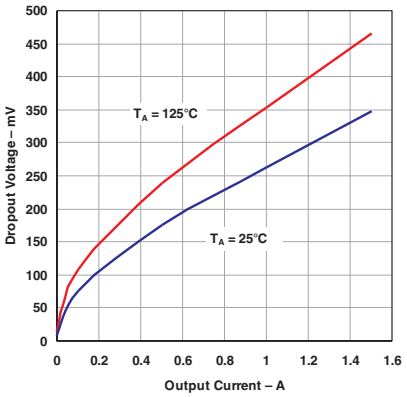


Figure 1. Dropout Voltage vs Output Current

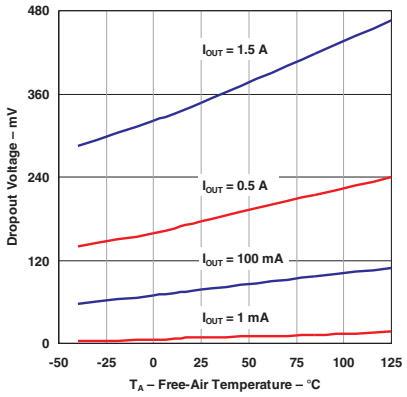
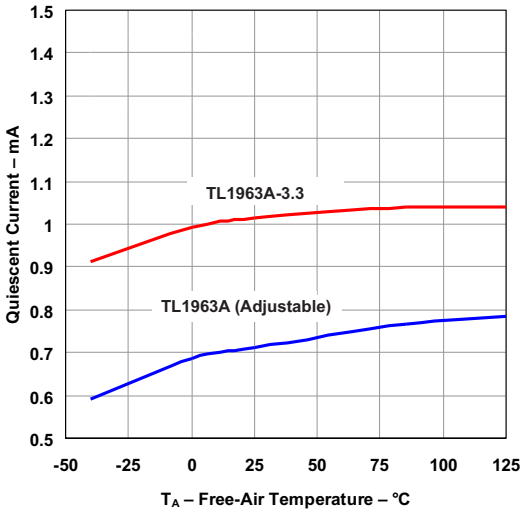
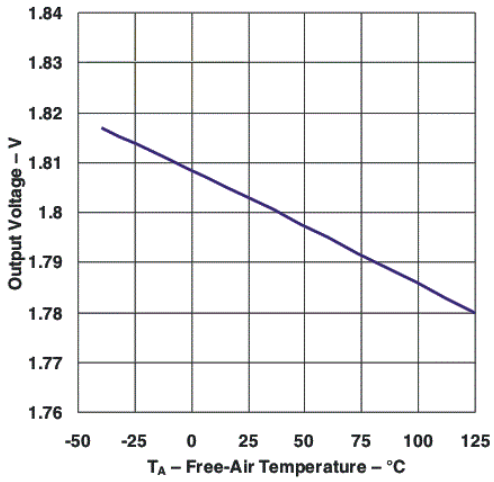


Figure 2. Dropout Voltage vs Temperature



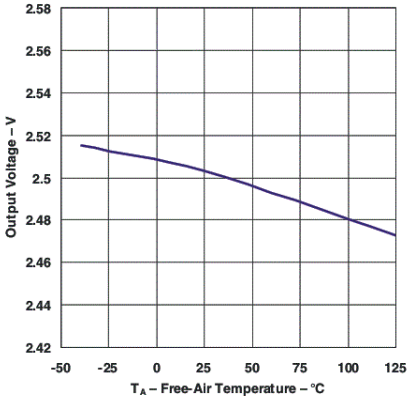
V_{IN} = 6 V I_{OUT} = 0 A V_{SHDN} = VIN

Figure 3. Quiescent Current vs Temperature



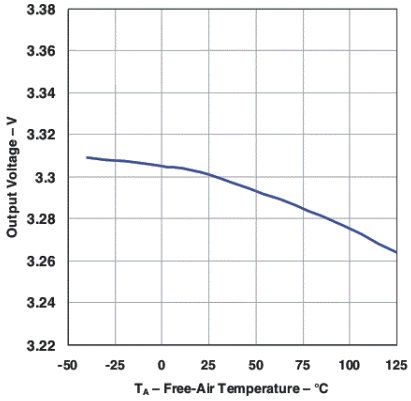
I_{OUT} = 1 mA TL1963A-18

Figure 4. TL1963A-18 Output Voltage vs Temperature



I_{OUT} = 1 mA TL1963A-25

Figure 5. TL1963A-25 Output Voltage vs Temperature

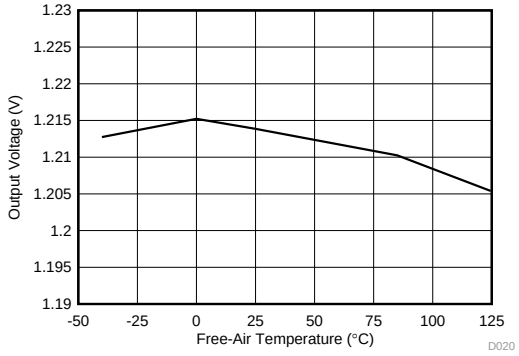


I_{OUT} = 1 mA TL1963A-33

Figure 6. TL1963A-33 Output Voltage vs Temperature

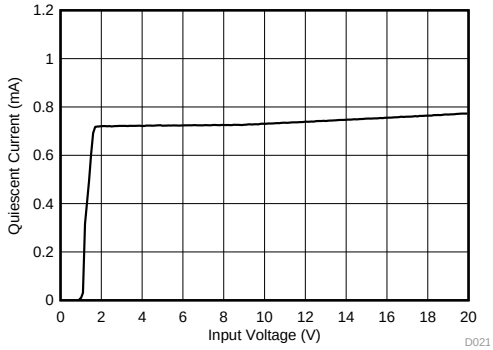
Typical Characteristics (continued)

Typical characteristics apply to all TL1963A-xx devices unless otherwise noted.



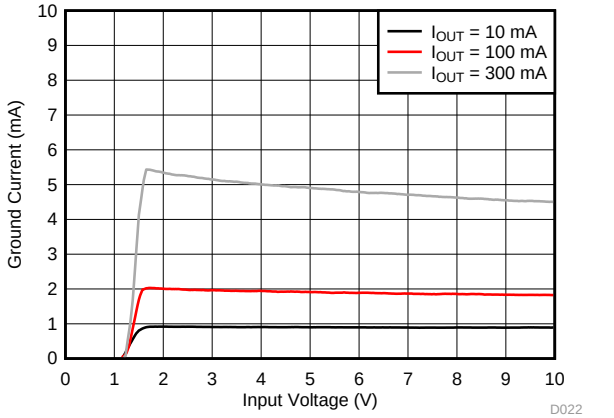
I_{OUT} = 1 mA V_{IN} = 6 V

Figure 7. TL1963A Output Voltage vs Temperature



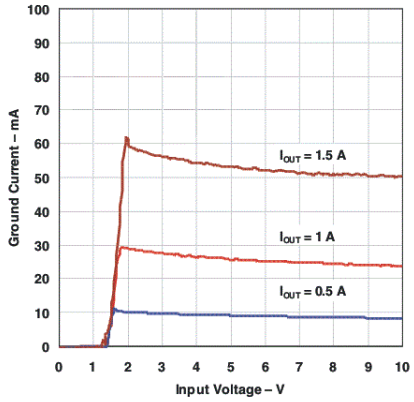
T_J = 25 °C R_{OUT} = 4.3kΩ V_{SHDN} = V_{IN}

Figure 8. Quiescent Current vs Input Voltage



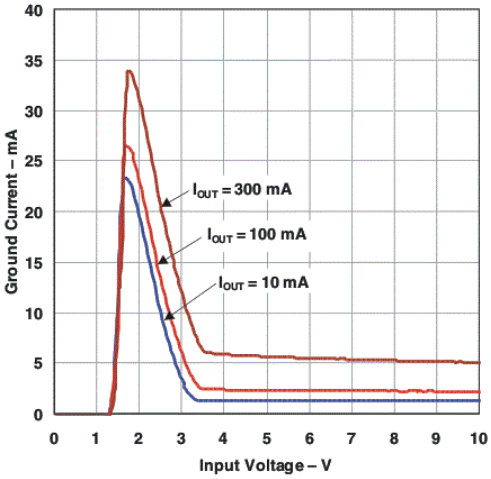
T_J = 25 °C V_{OUT} = 1.21 V V_{SHDN} = V_{IN}

Figure 9. TL1963A Ground Current vs Input Voltage



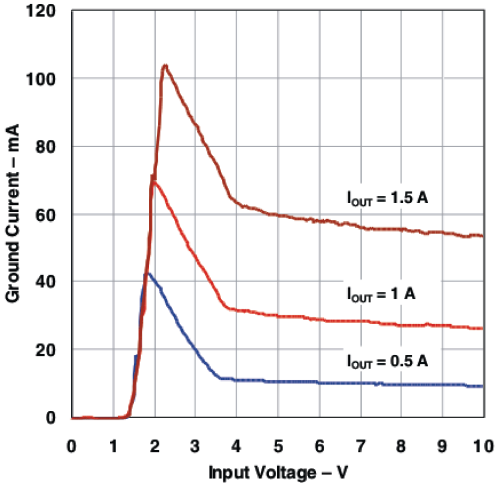
T_J = 25 °C V_{OUT} = 1.21 V V_{SHDN} = V_{IN}

Figure 10. TL1963A Ground Current vs Input Voltage



T_J = 25 °C V_{SHDN} = V_{IN}

Figure 11. TL1963A-33 Ground Current vs Input Voltage

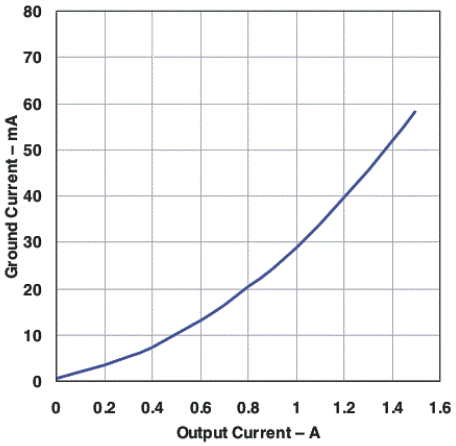


T_J = 25 °C V_{SHDN} = V_{IN}

Figure 12. TL1963A-33 Ground Current vs Input Voltage

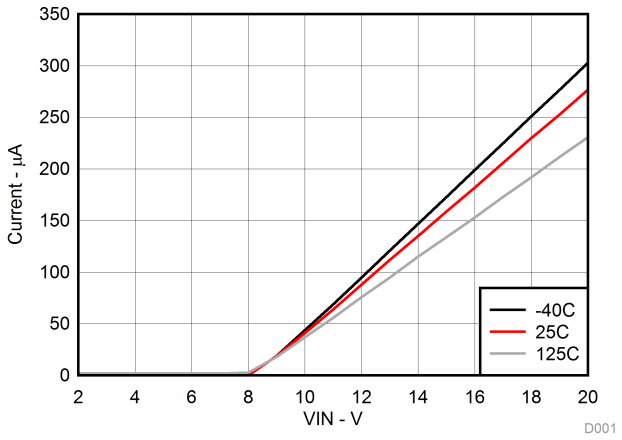
Typical Characteristics (continued)

Typical characteristics apply to all TL1963A-xx devices unless otherwise noted.



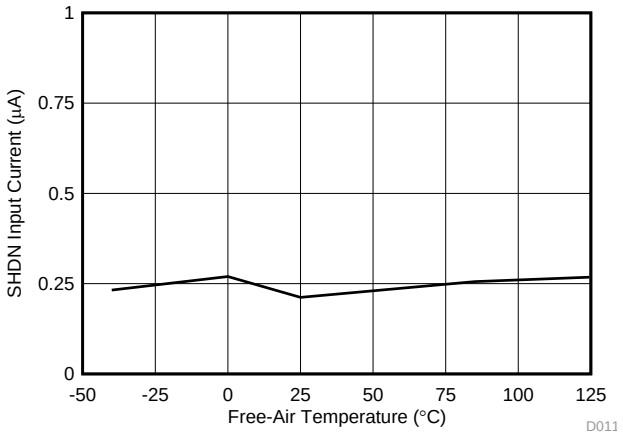
$V_{IN} = V_{OUT}(nom) + 1$

Figure 13. Ground Current vs Output Current



$V_{SHDN} = 0$ V

Figure 14. Quiescent Current in Shutdown vs Input Voltage



$V_{SHON} = 0$ V

Figure 15. $\overline{SHDN}$ Pin Current (I_{SHDN}) vs Temperature

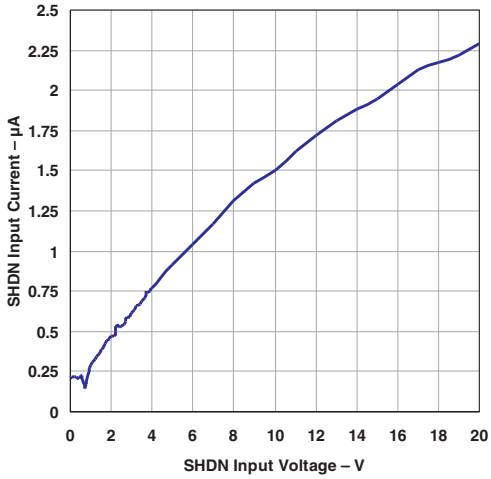
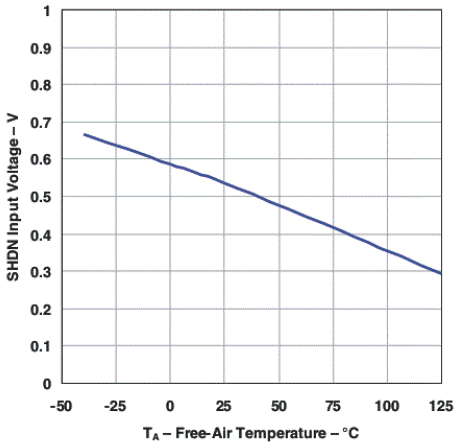
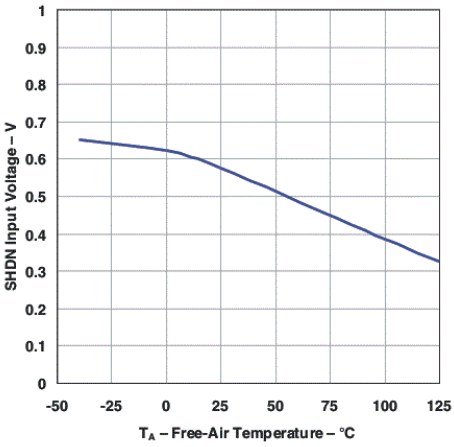


Figure 16. $\overline{SHDN}$ Pin Current (I_{SHDN}) vs $\overline{SHDN}$ Input Voltage



$I_{OUT} = 1$ mA

Figure 17. $\overline{SHDN}$ Threshold (OFF to ON) vs Temperature



$I_{OUT} = 1$ mA

Figure 18. $\overline{SHDN}$ Threshold (ON to OFF) vs Temperature

Typical Characteristics (continued)

Typical characteristics apply to all TL1963A-xx devices unless otherwise noted.

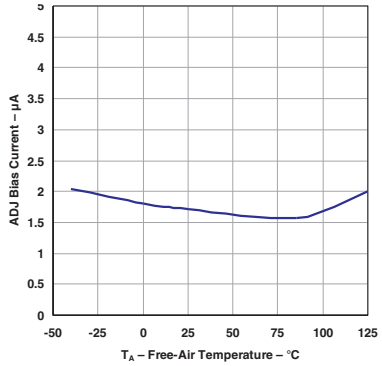
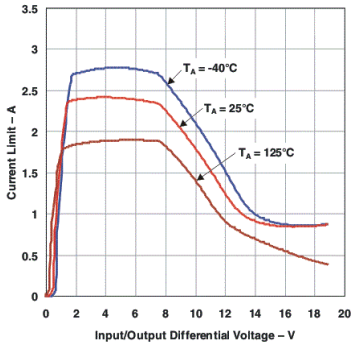
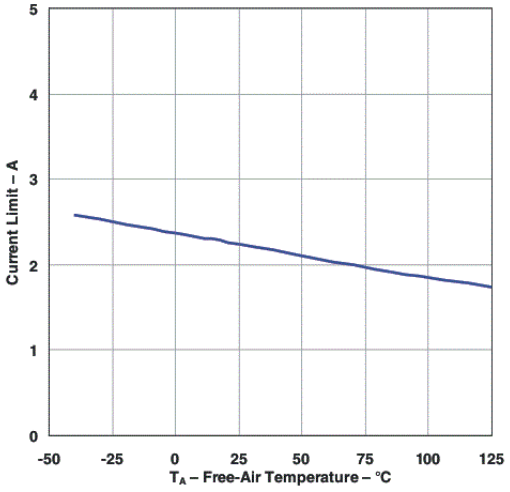


Figure 19. ADJ Bias Current vs Temperature



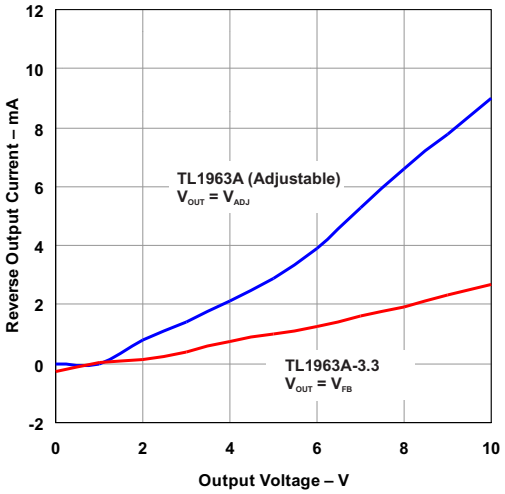
ΔV_{OUT} = 100 mV

Figure 20. Current Limit vs Input-to-Output Differential Voltage



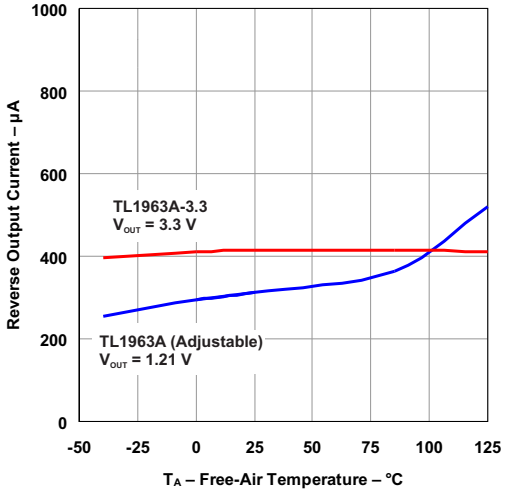
V_{IN} = 7 V V_{OUT} = 0 V

Figure 21. Current Limit vs Temperature



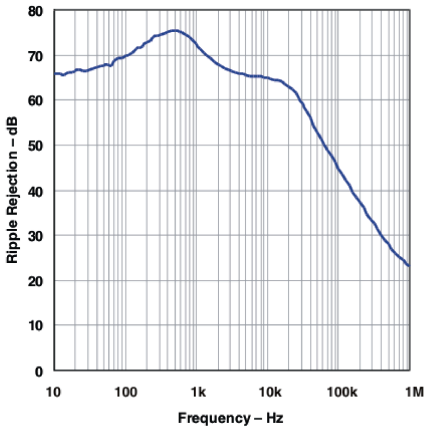
T_J = 25 °C V_{IN} = 0 V
Current flows into OUT pin

Figure 22. Reverse Output Current vs Output Voltage



V_{IN} = 0 V

Figure 23. Reverse Output Current vs Temperature

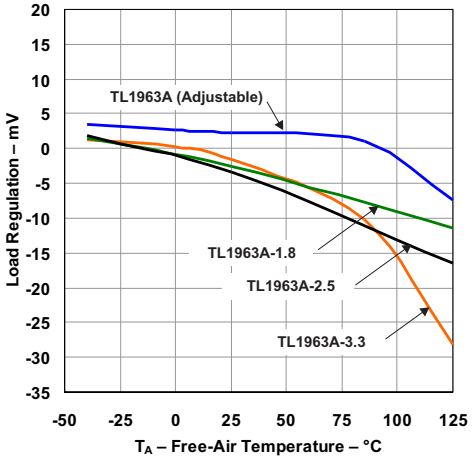


V_{RIPPLE} = 0.05 V_{PP} C_{IN} = 0 T_A = 25 °C
V_{IN} = 2.7 V C_{OUT} = 10 µF (ceramic)

Figure 24. Ripple Rejection vs Frequency

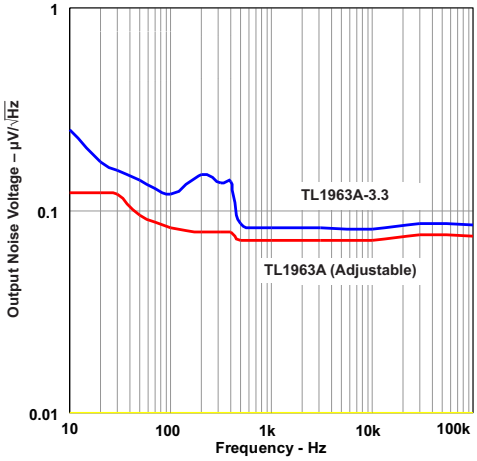
Typical Characteristics (continued)

Typical characteristics apply to all TL1963A-xx devices unless otherwise noted.



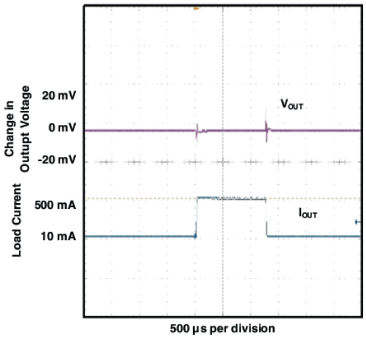
I_{OUT} = 1 mA to 1.5 A

Figure 25. Load Regulation vs Temperature



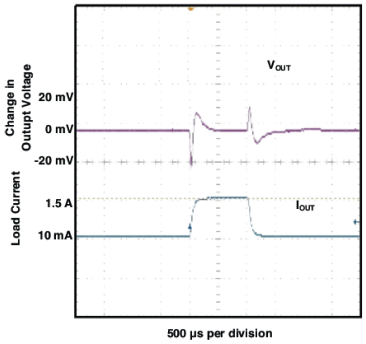
C_{OUT} = 10 µF (ceramic) I_{OUT} = 1.5 A

Figure 26. Output Noise Voltage vs Frequency



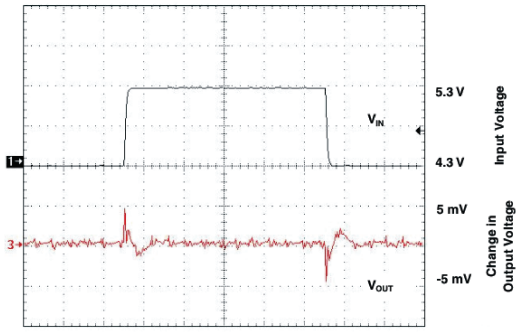
V_{IN} = 4.3 V C_{IN} = 10 µF
C_{OUT} = 10 µF (ceramic)

Figure 27. Load Transient Response



V_{IN} = 4.3 V C_{IN} = 10 µF
C_{OUT} = 10 µF (ceramic)

Figure 28. Load Transient Response



I_{OUT} = 1.5 A C_{IN} = 10 µF
C_{OUT} = 10 µF (ceramic)

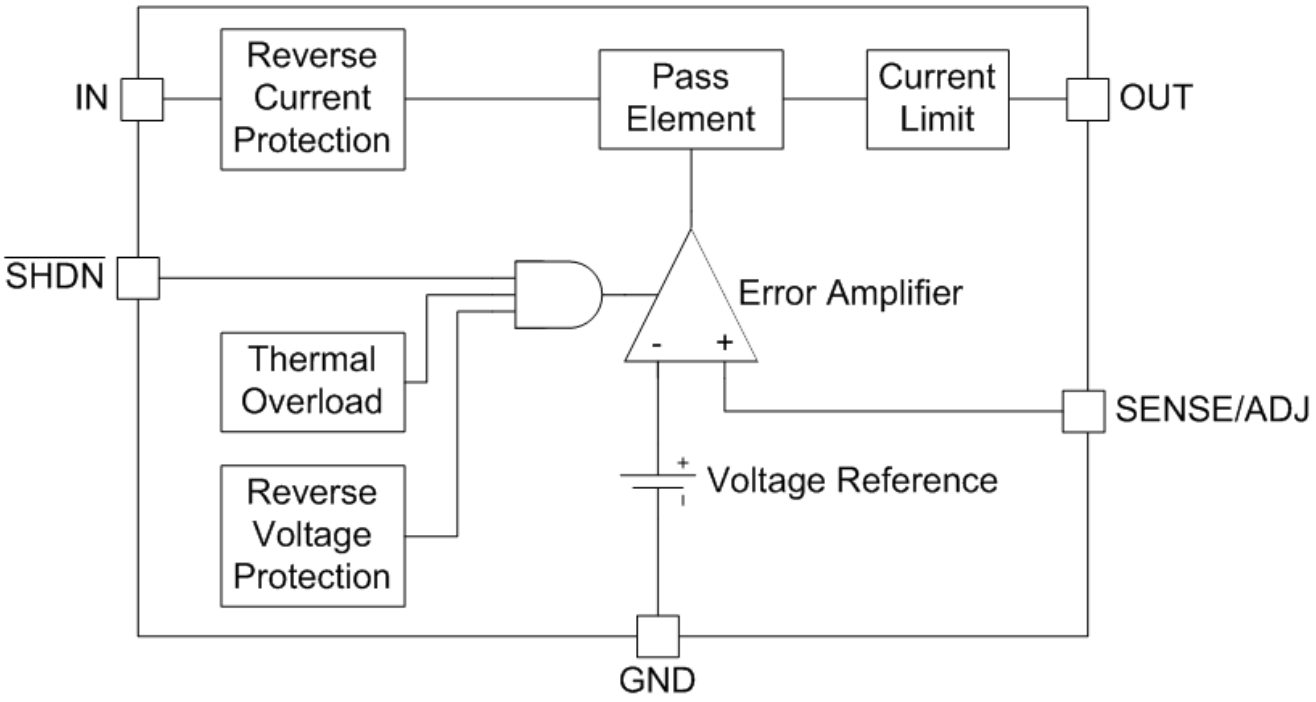
Figure 29. Line Transient response

9 Detailed Description

9.1 Overview

The TL1963A-xx series are 1.5-A low-dropout regulators optimized for fast transient response. The devices can supply 1.5 A at a dropout voltage of 340 mV. The low operating quiescent current (1 mA) drops to less than 1 µA in shutdown. In addition to the low quiescent current, the TL1963A-xx regulators incorporate several protection features that make them ideal for use in battery-powered systems. The devices are protected against both reverse input and reverse output voltages. In battery-backup applications where the output can be held up by a backup battery when the input is pulled to ground, the TL1963A-xx acts as if it has a diode in series with its output and prevents reverse-current flow. Additionally, in dual-supply applications where the regulator load is returned to a negative supply, the output can be pulled below ground by as much as (20 V – VIN) and still allow the device to start and operate.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Overload Recovery

Like many IC power regulators, the TL1963A-xx has safe operating area protection. The safe area protection decreases the current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The protection is designed to provide some output current at all values of input-to-output voltage up to the device breakdown.

When power is first turned on, as the input voltage rises, the output follows the input, allowing the regulator to start up into very heavy loads. During start-up, as the input voltage is rising, the input-to-output voltage differential is small, allowing the regulator to supply large output currents. With a high input voltage, a problem can occur wherein removal of an output short does not allow the output voltage to recover. Other regulators also exhibit this phenomenon, so it is not unique to the TL1963A-xx.

Feature Description (continued)

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations occur immediately after the removal of a short circuit or when the shutdown pin is pulled high after the input voltage has already been turned on. The load line for such a load may intersect the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the input power supply may need to be cycled down to zero and brought up again to make the output recover.

9.3.2 Output Voltage Noise

The TL1963A-xx regulators have been designed to provide low output voltage noise over the 10-Hz to 100-kHz bandwidth while operating at full load. Output voltage noise is typically 35 nV/√Hz over this frequency bandwidth for the TL1963A (adjustable version). For higher output voltages (generated by using a resistor divider), the output voltage noise is gained up accordingly. This results in RMS noise over the 10-Hz to 100-kHz bandwidth of 14 μV_{RMS} for the TL1963A, increasing to 38 μV_{RMS} for the TL1963A-33.

Higher values of output voltage noise may be measured when care is not exercised with regard to circuit layout and testing. Crosstalk from nearby traces can induce unwanted noise onto the output of the TL1963A-xx. Power-supply ripple rejection must also be considered; the TL1963A-xx regulators do not have unlimited power-supply rejection and pass a small portion of the input noise through to the output.

9.3.3 Protection Features

The TL1963A-xx regulators incorporate several protection features which make them ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the devices are protected against reverse input voltages, reverse output voltages and reverse voltages from output to input.

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature should not exceed 125°C.

The input of the device withstands reverse voltages of 20 V. Current flow into the device is limited to less than 1 mA (typically less than 100 µA), and no negative voltage appears at the output. The device protects both itself and the load. This provides protection against batteries that can be plugged in backward.

The output of the TL1963A-xx can be pulled below ground without damaging the device. If the input is left open circuit or grounded, the output can be pulled below ground by 20 V. For fixed voltage versions, the output acts like a large resistor, typically 5 kΩ or higher, limiting current flow to typically less than 600 µA. For adjustable versions, the output acts like an open circuit; no current flows out of the pin. If the input is powered by a voltage source, the output sources the short-circuit current of the device and protects itself by thermal limiting. In this case, grounding the $\overline{\text{SHDN}}$ pin turns off the device and stops the output from sourcing the short-circuit current.

The ADJ pin of the adjustable device can be pulled above or below ground by as much as 7 V without damaging the device. If the input is left open circuit or grounded, the ADJ pin acts like an open circuit when pulled below ground and like a large resistor (typically 5 kΩ) in series with a diode when pulled above ground.

In situations where the ADJ pin is connected to a resistor divider that would pull the ADJ pin above its 7-V clamp voltage if the output is pulled high, the ADJ pin input current must be limited to less than 5 mA. For example, a resistor divider is used to provide a regulated 1.5-V output from the 1.21-V reference when the output is forced to 20 V. The top resistor of the resistor divider must be chosen to limit the current into the ADJ pin to less than 5 mA when the ADJ pin is at 7 V. The 13-V difference between OUT and ADJ divided by the 5-mA maximum current into the ADJ pin yields a minimum top resistor value of 2.6 kΩ.

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage, or is left open circuit.

When the IN pin of the TL1963A-xx is forced below the OUT pin or the OUT pin is pulled above the IN pin, input current typically drops to less than 2 µA. This can happen if the input of the device is connected to a discharged (low voltage) battery and the output is held up by either a backup battery or a second regulator circuit. The state of the $\overline{\text{SHDN}}$ pin has no effect on the reverse output current when the output is pulled above the input.

9.4 Device Functional Modes

Table 1. Device States

SHDN	DEVICE STATE
H	Regulated Voltage
L	Shutdown

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

This section will highlight some of the design considerations when implementing this device in various applications.

10.1.1 Output Capacitance and Transient Response

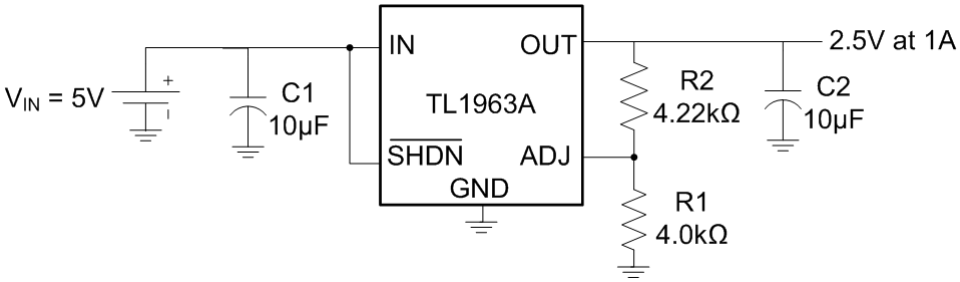
The TL1963A-xx regulators are designed to be stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. A minimum output capacitor of 10 µF with an ESR of 3 Ω or less is recommended to prevent oscillations. Larger values of output capacitance can decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the TL1963A-xx, increase the effective output capacitor value.

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. The most common dielectrics used are Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but exhibit strong voltage and temperature coefficients. When used with a 5-V regulator, a 10-µF Y5V capacitor can exhibit an effective value as low as 1 µF to 2 µF over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients.

10.2 Typical Applications

10.2.1 Adjustable Output Operation



NOTE: All capacitors are ceramic.

Figure 30. Adjustable Output Voltage Operation

Typical Applications (continued)

10.2.1.1 Design Requirements

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage (V_{IN})	5.0 V
Output Voltage (V_{OUT})	2.5 V
Output Current (I_{OUT})	0 A to 1 A
Load Regulation	1%

10.2.1.2 Detailed Design Procedure

The TL1963A has an adjustable output voltage range of 1.21 V to 20 V. The output voltage is set by the ratio of two external resistors R1 and R2 as shown in Figure 30. The device maintains the voltage at the ADJ pin at 1.21 V referenced to ground. The current in R1 is then equal to (1.21 V/R1), and the current in R2 is the current in R1 plus the ADJ pin bias current. The ADJ pin bias current, 3 µA at 25°C, flows through R2 into the ADJ pin. The output voltage can be calculated using Equation 1.

$$V_{OUT} = 1.21V(1+\frac{R2}{R1}) + I_{ADJ} \times R2 \quad (1)$$

The value of R1 should be less than 4.17 kΩ to minimize errors in the output voltage caused by the ADJ pin bias current. Note that in shutdown the output is turned off, and the divider current is zero. For an output voltage of 2.50 V, R1 will be set to 4.0 kΩ. R2 is then found to be 4.22 kΩ using the equation above.

$$V_{OUT} = 1.21V(1+\frac{4.22k\Omega}{4.0k\Omega}) + 3\mu A \times 4.22k\Omega \quad (2)$$

$$V_{OUT} = 2.50\ V \quad (3)$$

The adjustable device is tested and specified with the ADJ pin tied to the OUT pin for an output voltage of 1.21 V. Specifications for output voltages greater than 1.21 V are proportional to the ratio of the desired output voltage to 1.21 V: V_{OUT}/1.21 V. For example, load regulation for an output current change of 1 mA to 1.5 A is –2 mV (typ) at V_{OUT} = 1.21 V. At V_{OUT} = 2.50 V, the typical load regulation is:

(2.50 V/1.21 V)(–2 mV) = –4.13 mV (4)

Figure 33 shows the actual change in output is ~3 mV for a 1A load step. The maximum load regulation at 25 °C is –8 mV. At V_{OUT} = 2.50 V, the maximum load regulation is:

(2.50 V/1.21 V)(–8 mV) = –16.53 mV (5)

Since 16.53 mV is only 0.7% of the 2.5 V output voltage, the load regulation will meet the design requirements.

10.2.1.2.1 Fixed Operation

The TL1963A-xx can be used in a fixed voltage configuration. The SENSE/ADJ pin should be connected to OUT for proper operation. An example of this is shown in Figure 31. The TL1963A can also be used in this configuration for a fixed output voltage of 1.21 V.

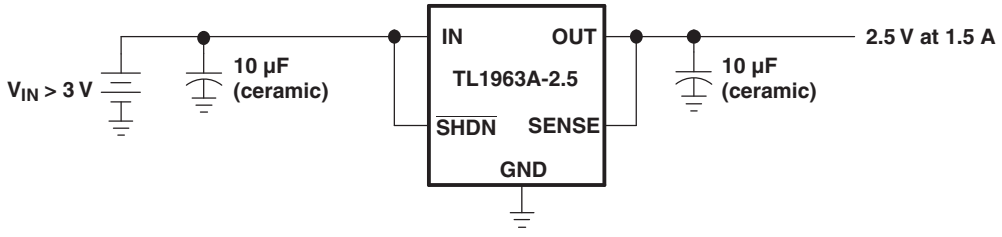


Figure 31. 3.3-V to 2.5-V Regulator

During fixed voltage operation, the SENSE/ADJ pin can be used for a Kelvin connection if routed separately to the load. This allows the regulator to compensate for voltage drop across parasitic resistances (RP) between the output and the load. This becomes more crucial with higher load currents.

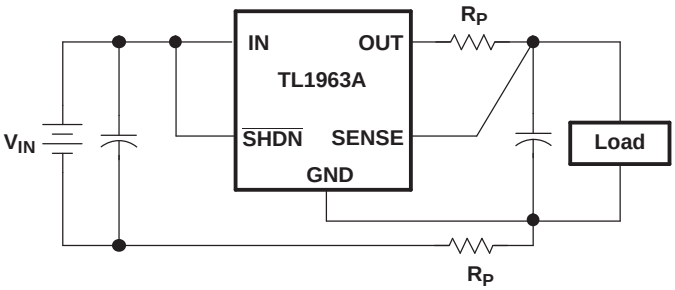


Figure 32. Kelvin Sense Connection

10.2.1.3 Application Curve

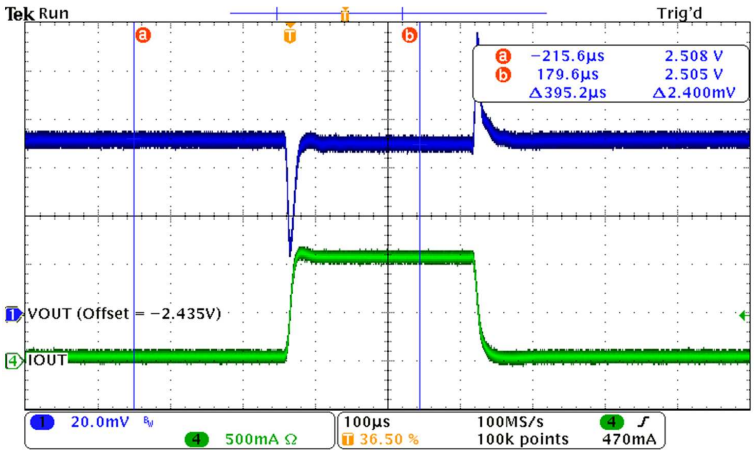
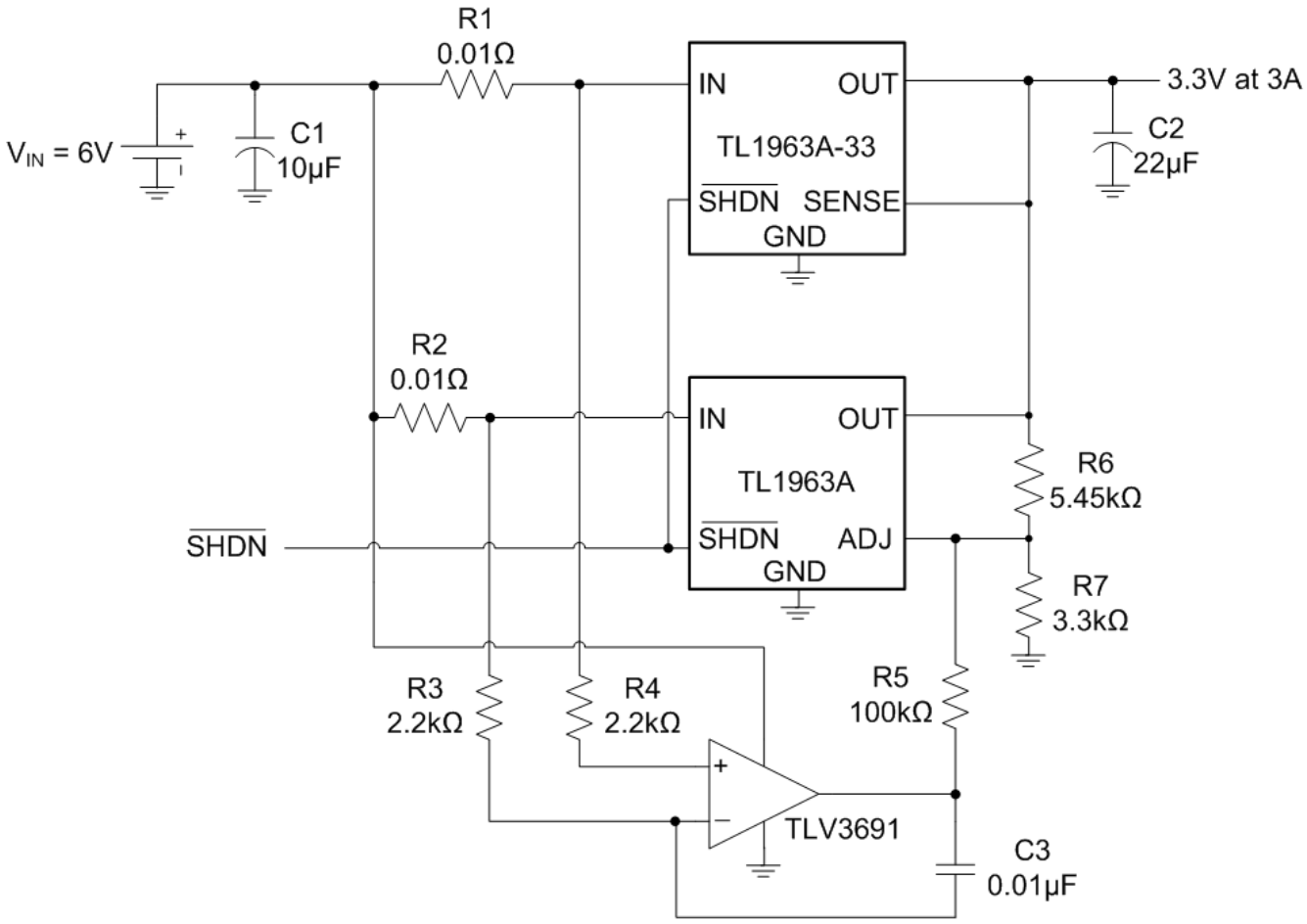


Figure 33. 1-A Load Transient Response (C_{OUT} = 10 uF)

10.2.2 Paralleling Regulators for Higher Output Current



NOTE: All capacitors are ceramic.

Figure 34. Paralleling Regulators For Higher Output Current

10.2.2.1 Design Requirements

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage (V_{IN})	6.0 V
Output Voltage (V_{OUT})	3.3 V
Output Current (I_{OUT})	3.0 A

10.2.2.2 Detailed Design Procedure

In an application requiring higher output current, an adjustable output regular can be placed in parallel with a fixed output regulator to increase the current capacity. Two sense resistors and a comparator can be used to control the feedback loop of the adjustable regulator in order to balance the current between the two regulators.

In Figure 34 resistors R1 and R2 are used to sense the current flowing into each regulator and should have a very low resistance to avoid unnecessary power loss. R1 and R2 should have the same value and a tolerance of 1% or better so the current is shared equally between the regulators. For this example, a value of 0.01 Ω will be used.

The TLV3691 rail-to-rail nanopower comparator output will alternate between VIN and GND depending on the currents flowing into each of the two regulators. To design this control circuit, begin by looking at the case where the two output currents are approximately equal and the comparator output is low. In this case, the output of the TL1963A should be set the same as the fixed voltage regulator. The TL1963A-33 has a 3.3 V fixed output, so this will be the set point for the adjustable regulator. Begin by selecting a R7 value less than 4.17 kΩ. In this example, 3.3 kΩ will be used. R5 will need to have a high resistance to satisfy Equation 10, for this example 100 kΩ was chosen. Then find the parallel resistance of R5 and R7 since they are both connected from the ADJ pin to GND using Equation 6.

$$(R5 \,||\, R7) = \frac{R5 \times R7}{R5 + R7} = 3.19k\Omega \tag{6}$$

Once the R5 and R7 parallel resistance in calculated, the value for R6 can be found using Equation 7.

$$R6 = \frac{V_{OUT}}{1.22V}(R5 \,||\, R7) - (R5 \,||\, R7) \tag{7}$$

$$R6 = \frac{3.3V}{1.22V}\left(3.19k\Omega\right) - \left(3.19k\Omega\right) \tag{8}$$

$$R6 = 5.45\ k\Omega \tag{9}$$

In the case where the TL1963A-33 is sourcing more current than TL1963A, the comparator output will go high. This will lower the voltage at the ADJ pin causing the TL1963A to try and raise the output voltage by sourcing more current. The TL1963A-33 will then react by sourcing less current to try and keep the output from rising. When the current through the TL1963A-33 becomes less than the TL1963A, the comparator output will return to GND. In order for this to happen, Equation 10 must be satisfied:

$$V_{IN}\left(\frac{R7}{R5 + R7}\right) + \left(V_{IN} - V_{OUT}\right)\left(\frac{R6}{R5 + R6}\right) < Vref \tag{10}$$

$$6V\left(\frac{3.3k\Omega}{100k\Omega + 3.3k\Omega}\right) + (2.7V)\left(\frac{5.45k\Omega}{100k\Omega + 5.45k\Omega}\right) < 1.21V \tag{11}$$

$$0.19\ V + 0.14\ V < 1.21\ V \tag{12}$$

$$0.33\ V < 1.21\ V \tag{13}$$

10.2.2.3 Application Curve

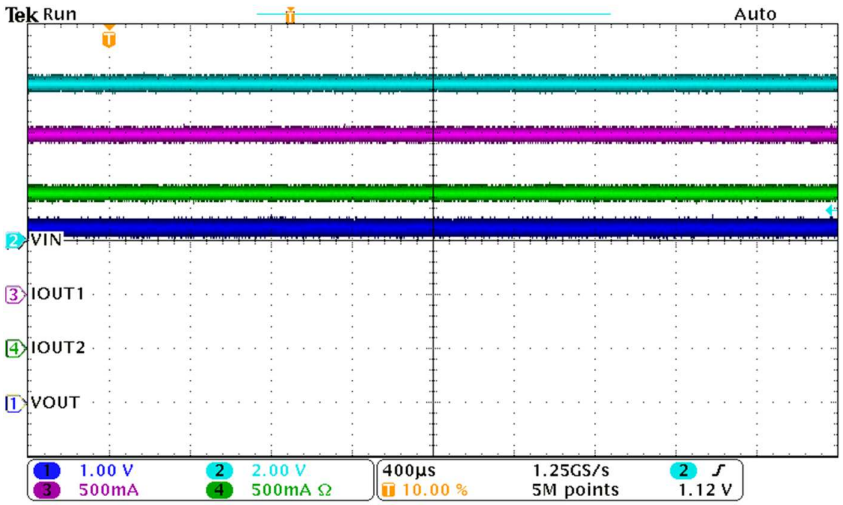


Figure 35. Parallel Regulators Sharing Load Current

11 Power Supply Recommendations

The device is designed to operate with an input voltage supply up to 20 V. The minimum input voltage should provide adequate headroom greater than the dropout voltage in order for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

12 Layout

12.1 Layout Guidelines

- For best performance, all traces should be as short as possible.
- Use wide traces for IN, OUT, and GND to minimize the parasitic electrical effects.
- A minimum output capacitor of 10 µF with an ESR of 3 Ω or less is recommended to prevent oscillations. X5R and X7R dielectrics are preferred.
- Place the Output Capacitor as close as possible to the OUT pin of the device.
- The tab of the DCQ package should be connected to ground.
- The exposed thermal pad of the KTT package should be connected to a wide ground plane for effective heat dissipation.

12.2 Layout Example

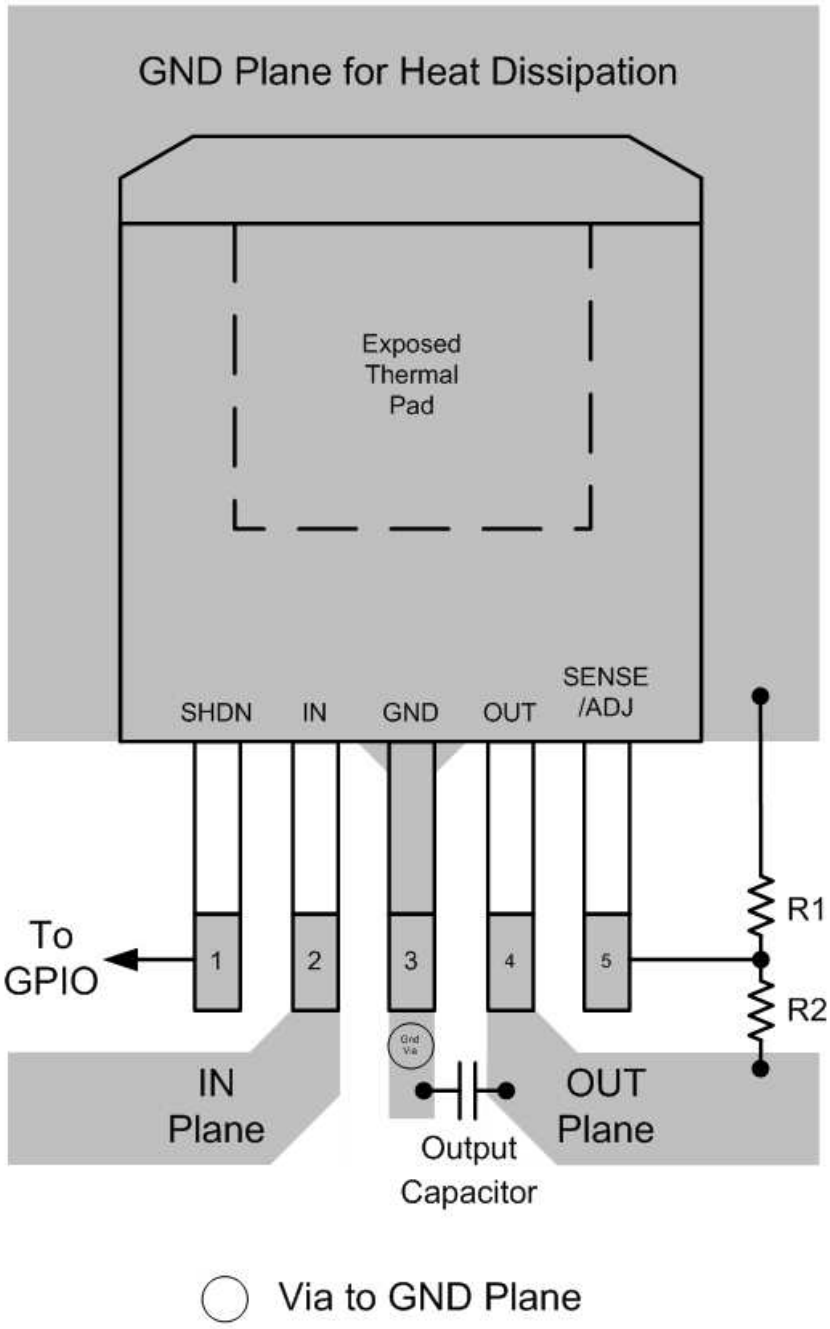


Figure 36. TO-263 Layout Example (KTT)

Layout Example (continued)

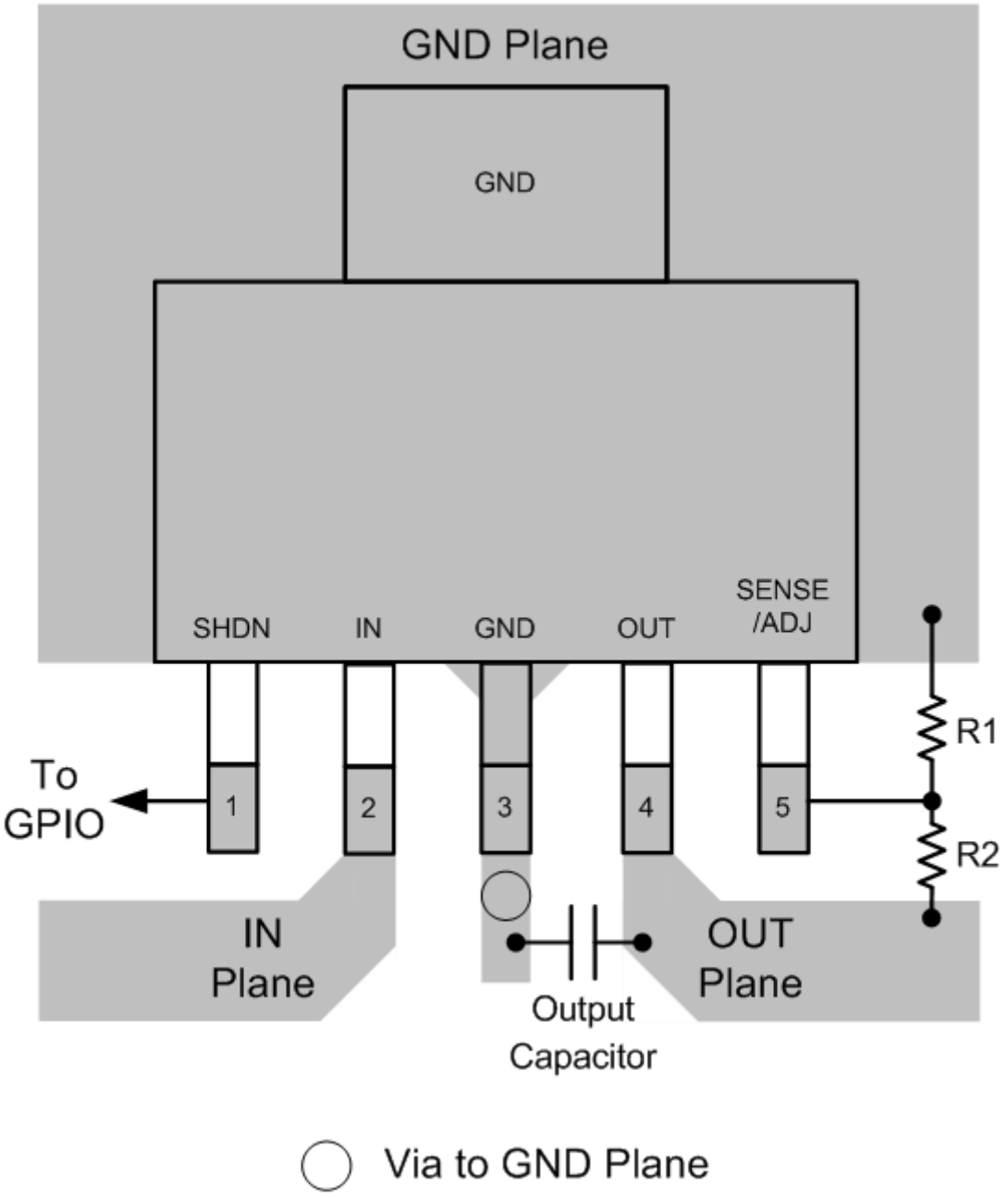


Figure 37. 6SOT-223 Layout Example (DCQ)

Layout Example (continued)

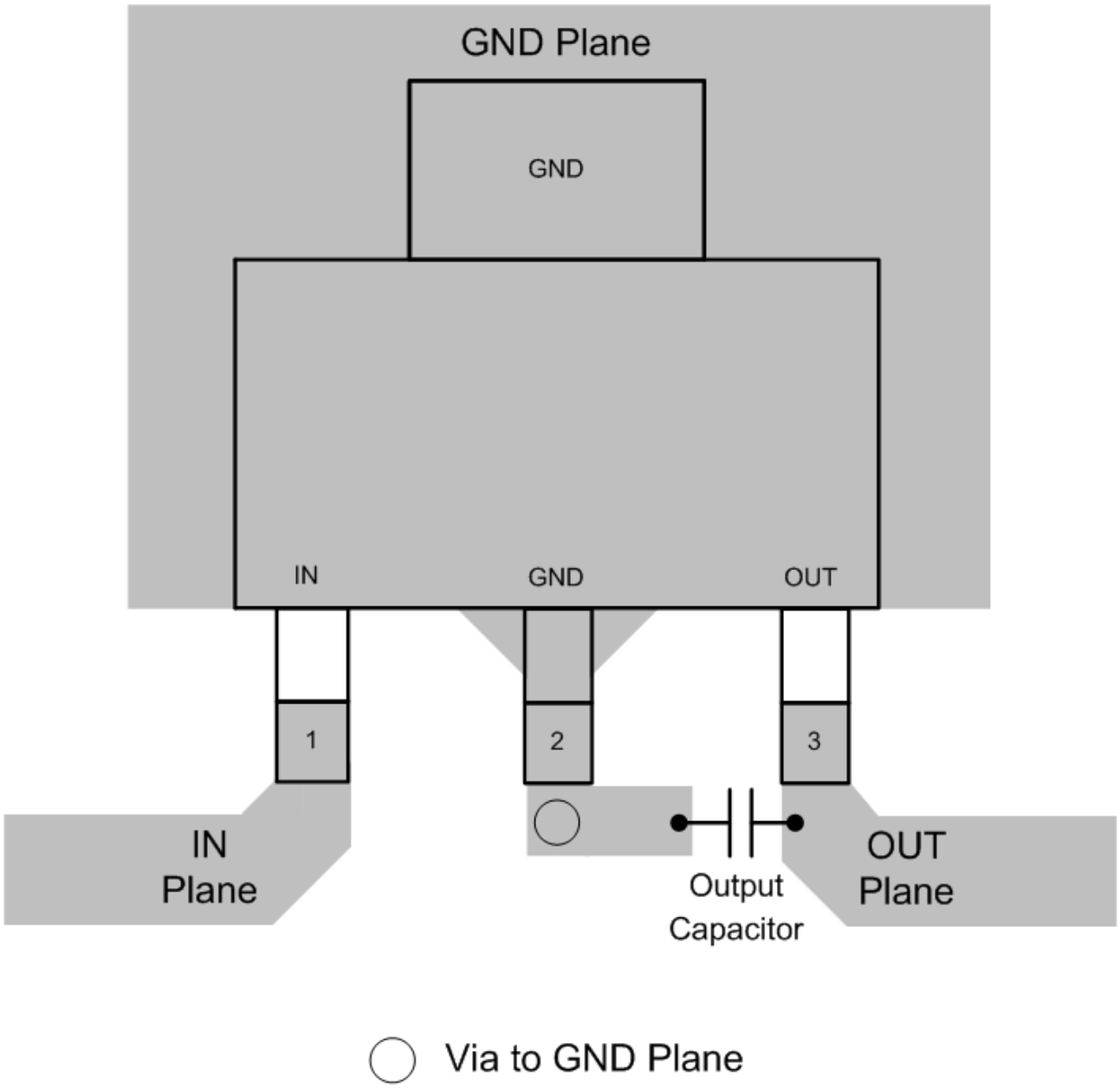


Figure 38. 4SOT-223 Layout Example (DCY)

12.3 Thermal Considerations

The power handling capability of the device is limited by the recommended maximum operating junction temperature (125°C). The power dissipated by the device is made up of two components:

- Output current multiplied by the input/output voltage differential: $I_{OUT}(V_{IN} – V_{OUT})$
- GND pin current multiplied by the input voltage: $I_{GND}V_{IN}$

The GND pin current can be found using the GND Pin Current graphs in *Typical Characteristics*. Power dissipation is equal to the sum of the two components listed above.

Thermal Considerations (continued)

The TL1963A-xx series regulators have internal thermal limiting designed to protect the device during overload conditions. For continuous normal conditions, the recommended maximum operating junction temperature is 125 °C. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

For surface-mount devices, heat sinking is accomplished by using the heat-spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

Table 4 lists thermal resistance for several different board sizes and copper areas. All measurements were taken in still air on 1/16" FR-4 board with 1-oz copper.

Table 4. Thermal Data for KTT Package (5-Pin TO-263)

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION TO AMBIENT)
TOPSIDE(1)	BACKSIDE		
2500 mm^2	2500 mm^2	2500 mm^2	23°C/W
1000 mm^2	2500 mm^2	2500 mm^2	25°C/W
125 mm^2	2500 mm^2	2500 mm^2	33°C/W

(1) Device is mounted on topside.

12.3.1 Calculating Junction Temperature

Example: Given an output voltage of 3.3 V, an input voltage range of 4 V to 6 V, an output current range of 0 mA to 500 mA, and a maximum ambient temperature of 50°C, what is the operating junction temperature?

The power dissipated by the device is equal to:

$$I_{OUT(MAX)}(V_{IN(MAX)} - V_{OUT}) + I_{GND}(V_{IN(MAX)})$$

where

- $I_{OUT(MAX)}$ = 500 mA
- $V_{IN(MAX)}$ = 6 V
- I_{GND} at (I_{OUT} = 500 mA, V_{IN} = 6 V) = 10 mA (14)

So,

$$P = 500\ mA \times (6\ V - 3.3\ V) + 10\ mA \times 6\ V = 1.41\ W \quad (15)$$

Using a KTT package, the thermal resistance is in the range of 23°C/W to 33°C/W, depending on the copper area. So the junction temperature rise above ambient is approximately equal to:

$$1.41\ W \times 28°C/W = 39.5°C \quad (16)$$

The junction temperature rise can then be added to the maximum ambient temperature to find the operating junction temperature (T_J):

$$T_J = 50°C + 39.5°C = 89.5°C \quad (17)$$

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TL1963A	Click here	Click here	Click here	Click here	Click here
TL1963A-15	Click here	Click here	Click here	Click here	Click here
TL1963A-18	Click here	Click here	Click here	Click here	Click here
TL1963A-25	Click here	Click here	Click here	Click here	Click here
TL1963A-33	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL1963A-15DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1963A-15	Samples
TL1963A-15DCQT	ACTIVE	SOT-223	DCQ	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		1963A-15	Samples
TL1963A-15DCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TF	Samples
TL1963A-15DCYT	ACTIVE	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TF	Samples
TL1963A-15KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TL1963A-15	Samples
TL1963A-15KTTT	PREVIEW	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI	-40 to 125		
TL1963A-18DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1963A-18	Samples
TL1963A-18DCQT	ACTIVE	SOT-223	DCQ	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		1963A-18	Samples
TL1963A-18DCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TG	Samples
TL1963A-18KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TL1963A-18	Samples
TL1963A-18KTTT	PREVIEW	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI	-40 to 125		
TL1963A-25DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1963A-25	Samples
TL1963A-25DCQT	ACTIVE	SOT-223	DCQ	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1963A-25	Samples
TL1963A-25DCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TH	Samples
TL1963A-25DCYT	ACTIVE	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TH	Samples
TL1963A-25KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TL1963A-25	Samples
TL1963A-25KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TL1963A-25	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL1963A-25KTTT	PREVIEW	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI	-40 to 125		
TL1963A-33DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1963A-33	Samples
TL1963A-33DCQT	ACTIVE	SOT-223	DCQ	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		1963A-33	Samples
TL1963A-33DCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TJ	Samples
TL1963A-33DCYT	PREVIEW	SOT-223	DCY	4	250	TBD	Call TI	Call TI	-40 to 125	TJ	
TL1963A-33KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TL1963A-33	Samples
TL1963A-33KTTT	PREVIEW	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI	-40 to 125		
TL1963ADCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		TL1963A	Samples
TL1963ADCQT	ACTIVE	SOT-223	DCQ	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		TL1963A	Samples
TL1963AKTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TL1963A	Samples
TL1963AKTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TL1963A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TL1963A :

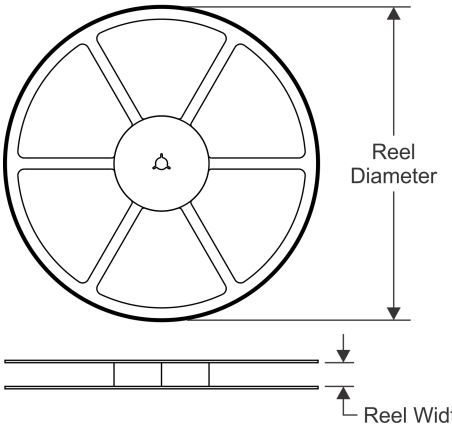
- Automotive: TL1963A-Q1

NOTE: Qualified Version Definitions:

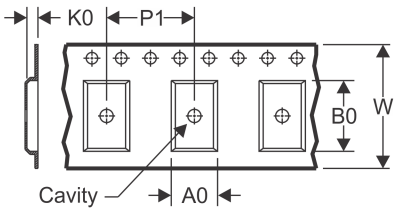
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

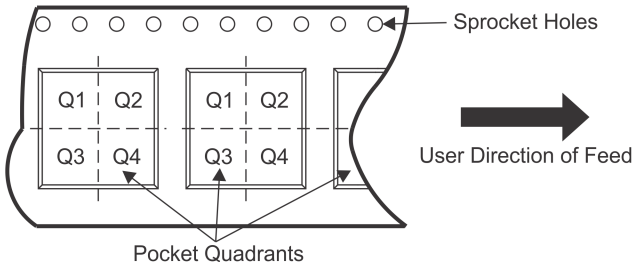


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

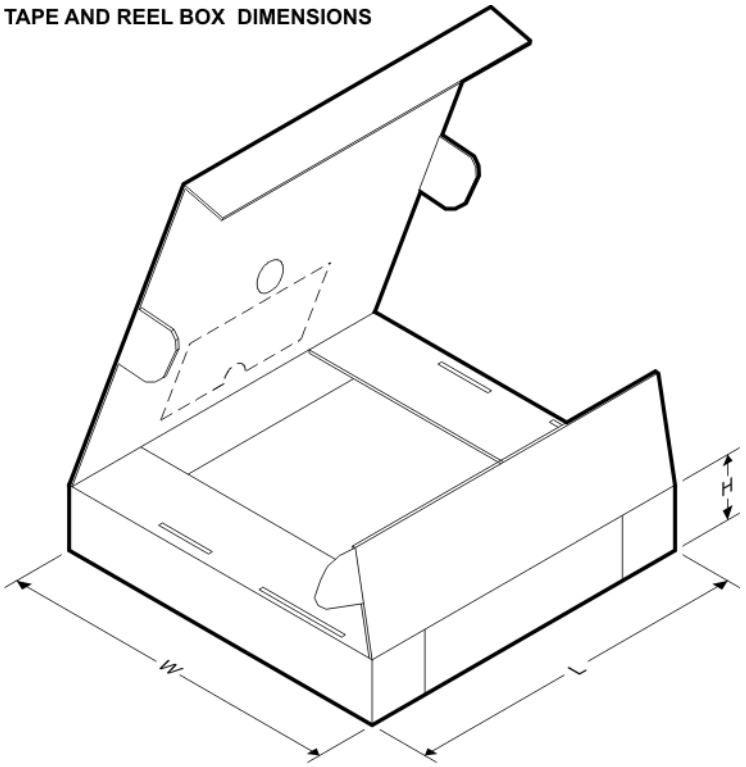


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL1963A-15DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TL1963A-15DCQT	SOT-223	DCQ	6	250	177.8	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TL1963A-15DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TL1963A-15DCYT	SOT-223	DCY	4	250	180.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TL1963A-15KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
TL1963A-18DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TL1963A-18DCQT	SOT-223	DCQ	6	250	177.8	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TL1963A-18DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TL1963A-18KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
TL1963A-25DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TL1963A-25DCQT	SOT-223	DCQ	6	250	177.8	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TL1963A-25DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TL1963A-25DCYT	SOT-223	DCY	4	250	180.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TL1963A-25KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
TL1963A-33DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TL1963A-33DCQT	SOT-223	DCQ	6	250	177.8	12.4	7.1	7.45	1.88	8.0	12.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL1963A-33DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TL1963A-33KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
TL1963ADCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TL1963ADCQT	SOT-223	DCQ	6	250	177.8	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TL1963AKTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



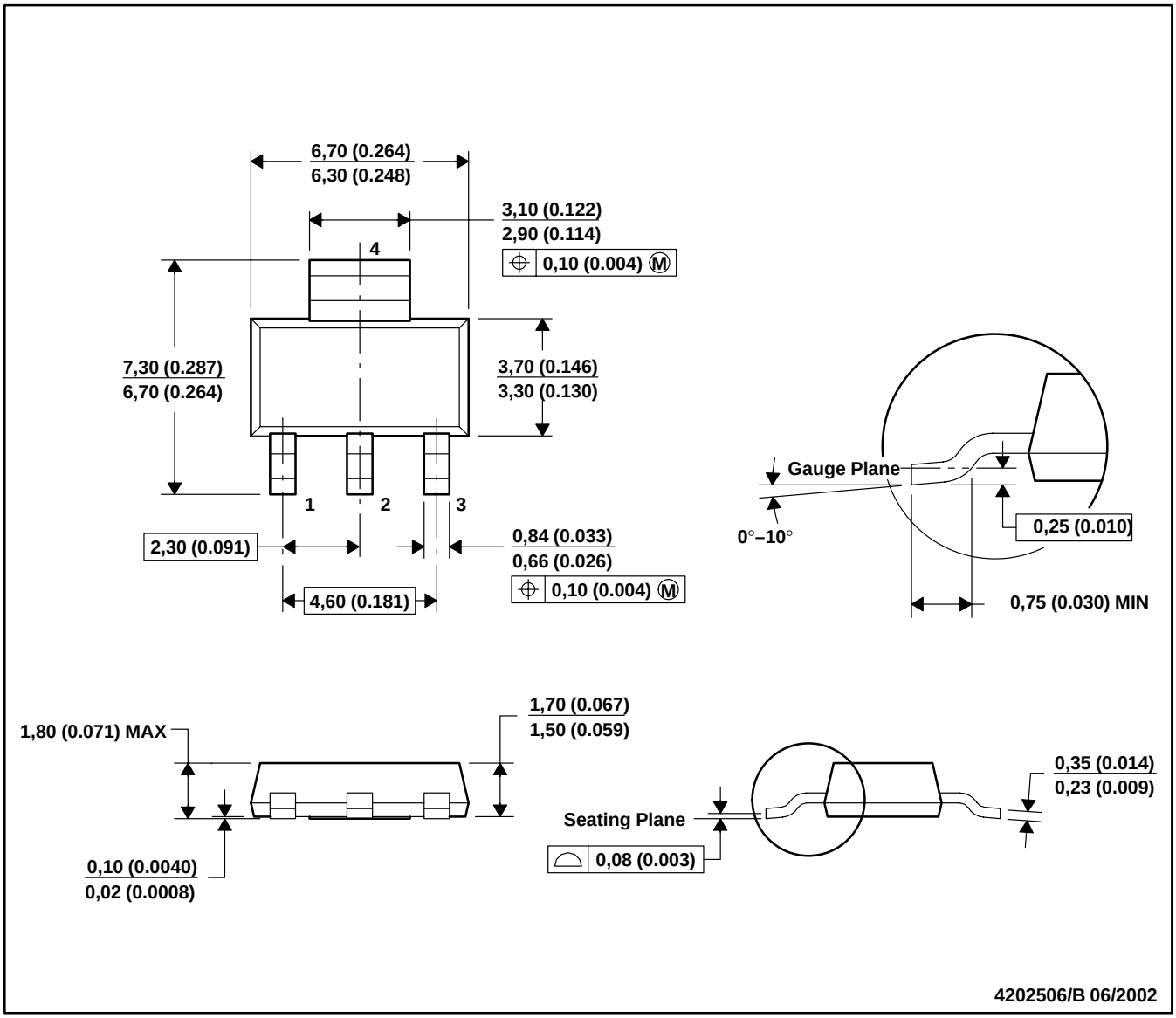
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL1963A-15DCQR	SOT-223	DCQ	6	2500	406.0	348.0	63.0
TL1963A-15DCQT	SOT-223	DCQ	6	250	180.0	180.0	85.0
TL1963A-15DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TL1963A-15DCYT	SOT-223	DCY	4	250	190.0	190.0	30.0
TL1963A-15KTTR	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TL1963A-18DCQR	SOT-223	DCQ	6	2500	406.0	348.0	63.0
TL1963A-18DCQT	SOT-223	DCQ	6	250	180.0	180.0	85.0
TL1963A-18DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TL1963A-18KTTR	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TL1963A-25DCQR	SOT-223	DCQ	6	2500	406.0	348.0	63.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL1963A-25DCQT	SOT-223	DCQ	6	250	180.0	180.0	85.0
TL1963A-25DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TL1963A-25DCYT	SOT-223	DCY	4	250	190.0	190.0	30.0
TL1963A-25KTTR	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TL1963A-33DCQR	SOT-223	DCQ	6	2500	406.0	348.0	63.0
TL1963A-33DCQT	SOT-223	DCQ	6	250	180.0	180.0	85.0
TL1963A-33DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
TL1963A-33KTTR	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TL1963ADCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TL1963ADCQT	SOT-223	DCQ	6	250	180.0	180.0	85.0
TL1963AKTTR	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0

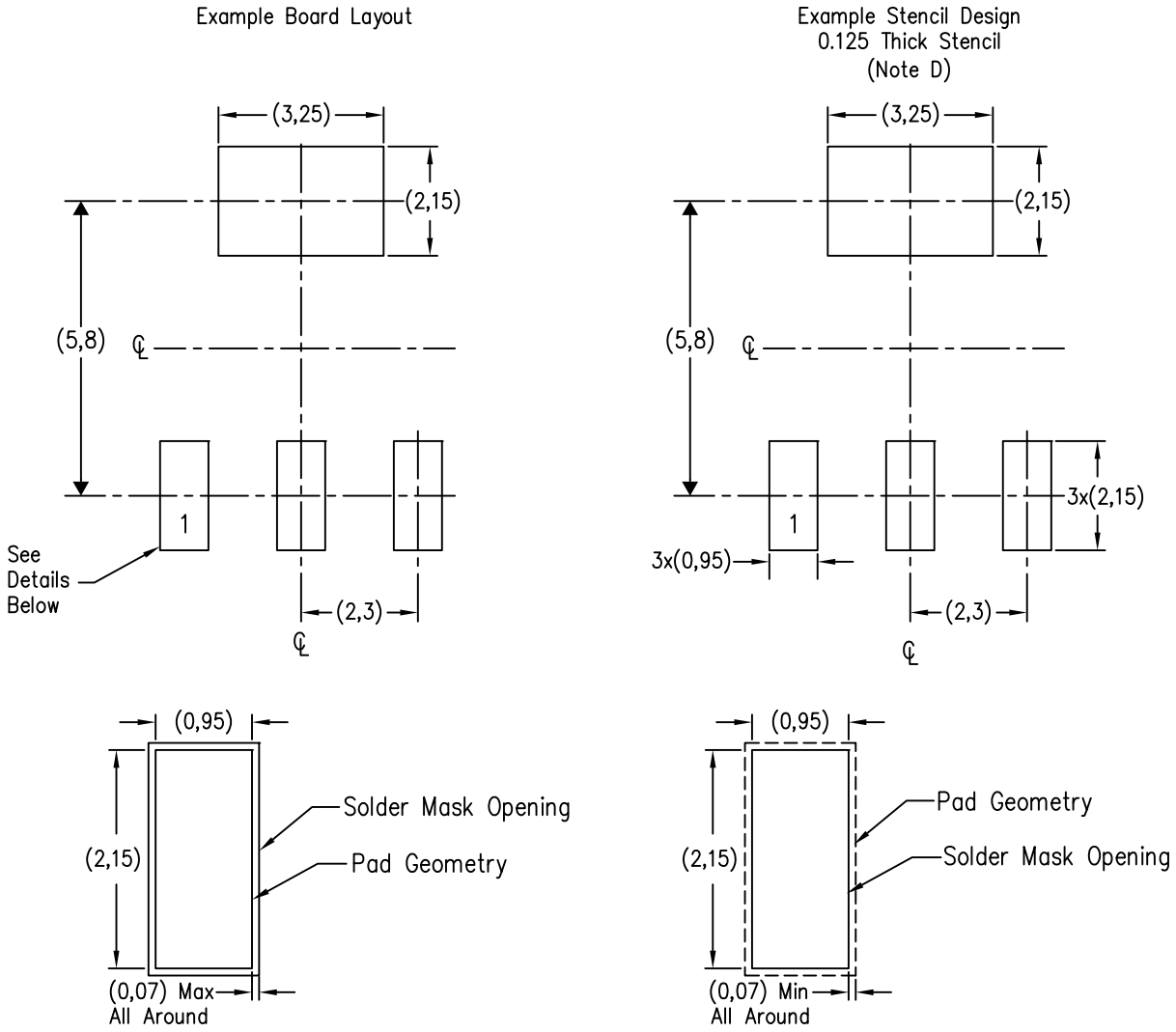
MPDS094A – APRIL 2001 – REVISED JUNE 2002

DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC TO-261 Variation AA.

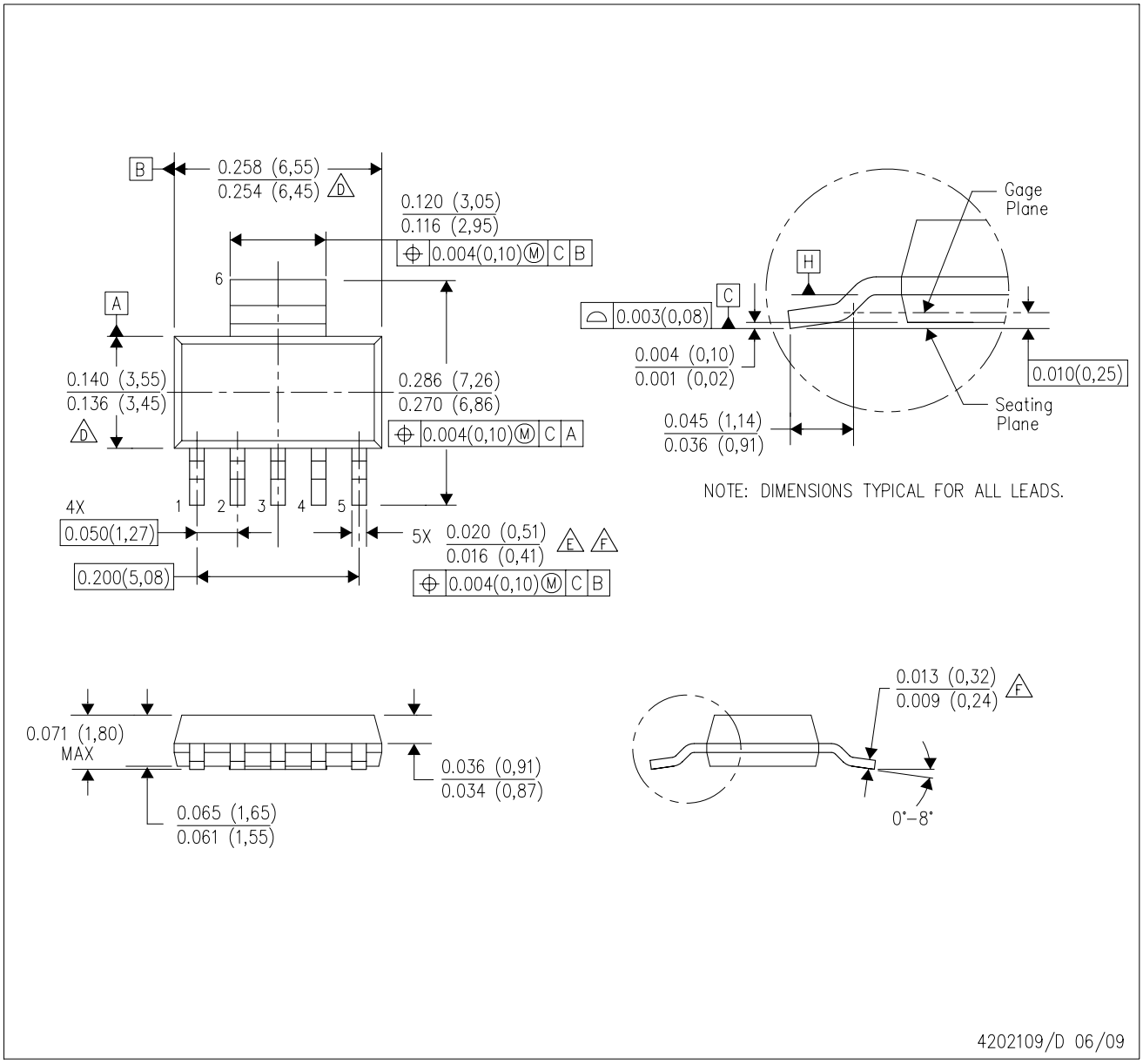
DCY (R–PDSO–G4) PLASTIC SMALL OUTLINE



NOTES:

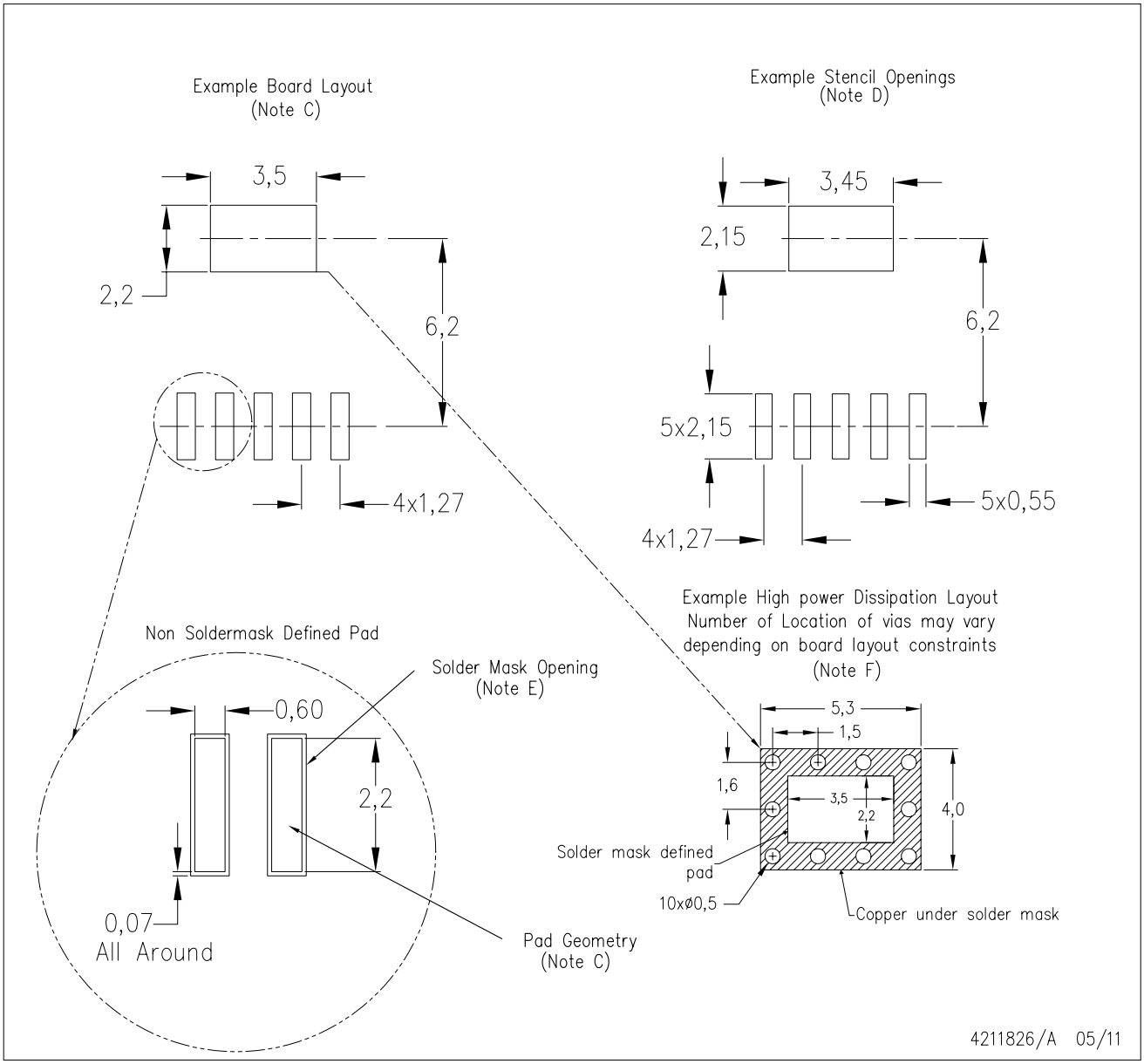
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil recommendations. Refer to IPC 7525 for stencil design considerations.

DCQ (R–PDSO–G6) PLASTIC SMALL–OUTLINE



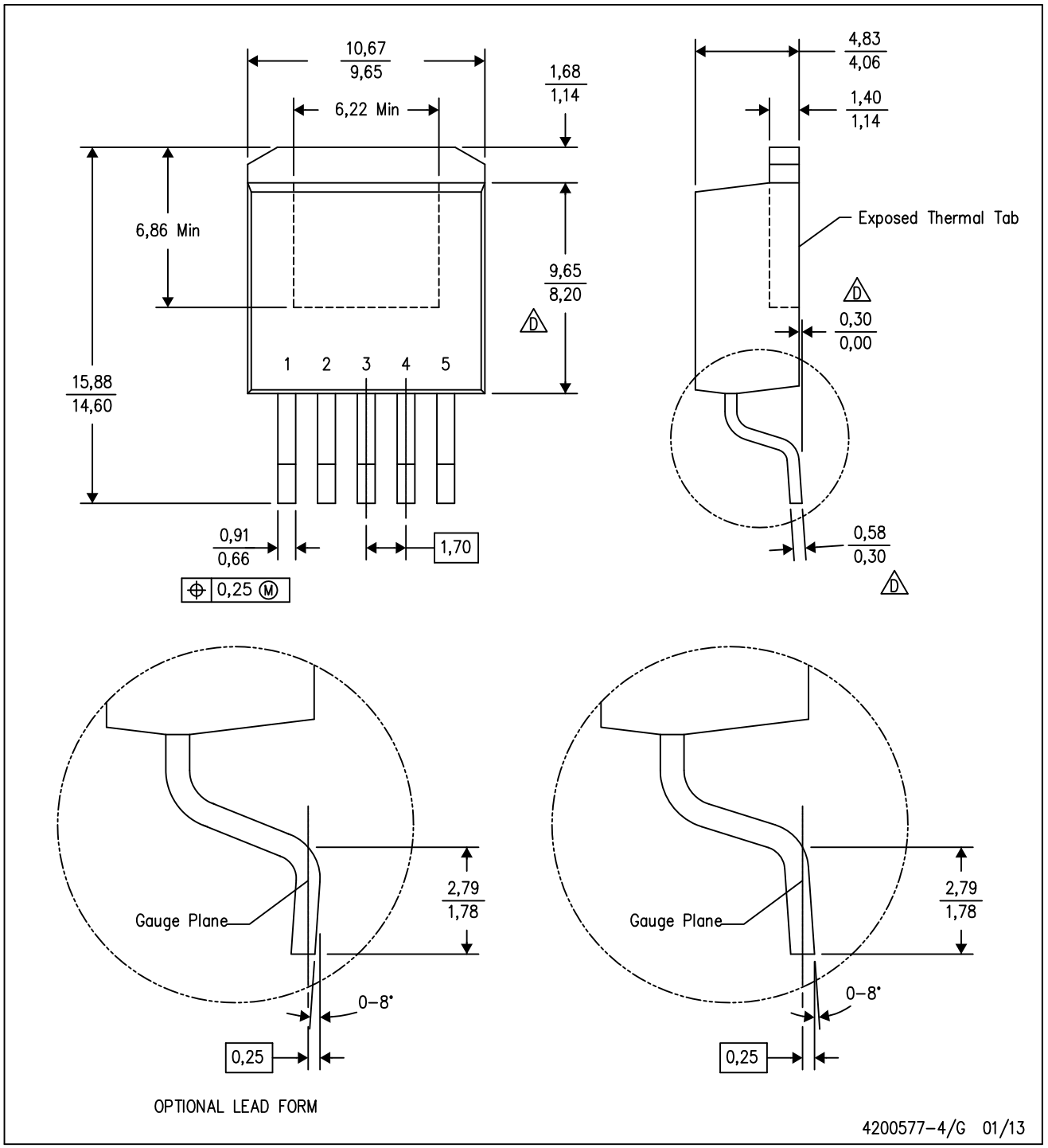
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Controlling dimension in inches.
- D. Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
- E. Lead width dimension does not include dambar protrusion.
- F. Lead width and thickness dimensions apply to solder plated leads.
- G. Interlead flash allow 0.008 inch max.
- H. Gate burr/protrusion max. 0.006 inch.
- I. Datums A and B are to be determined at Datum H.

DCQ (R–PDSO–G6) PLASTIC SMALL OUTLINE



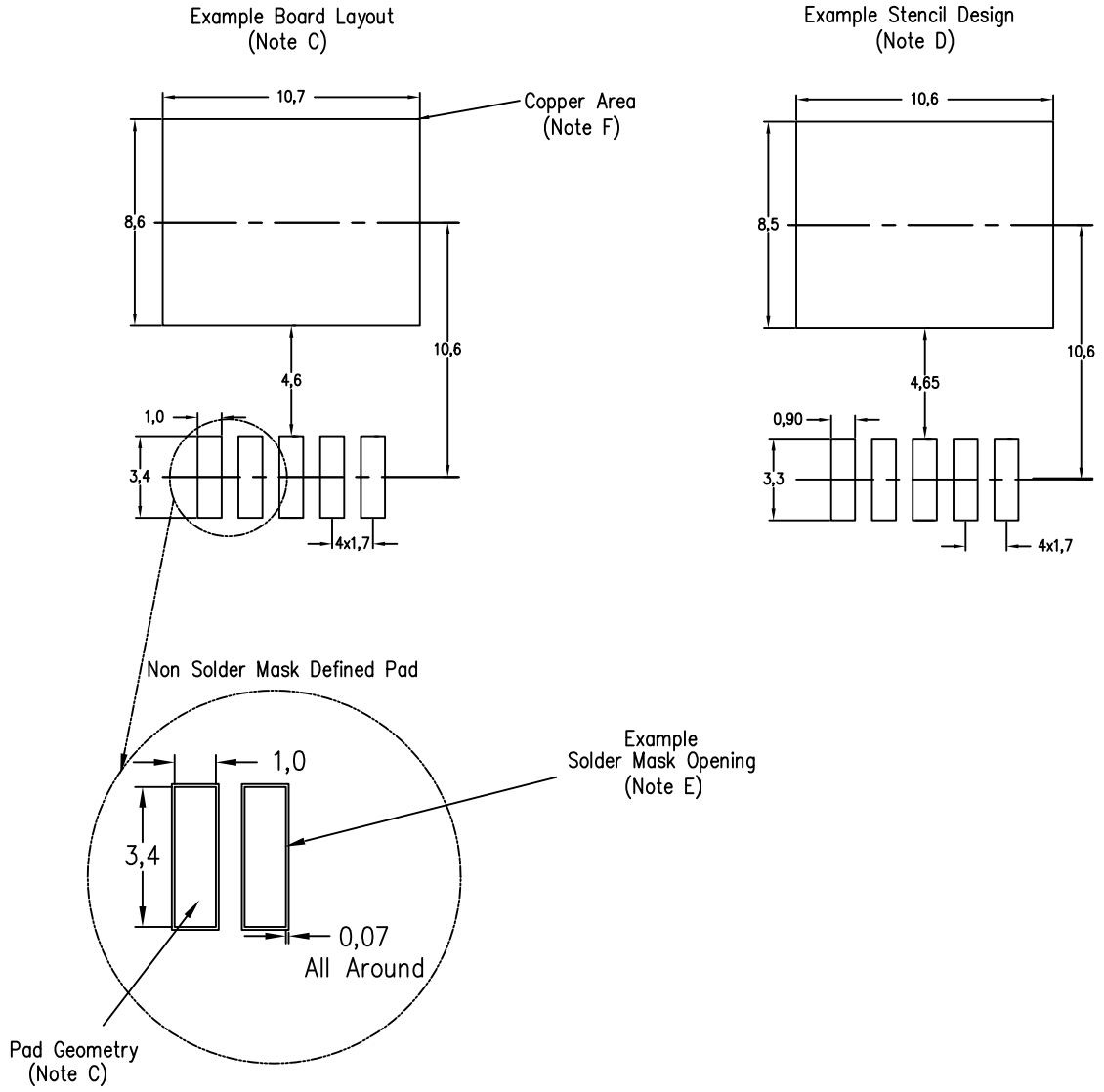
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. Please refer to the product data sheet for specific via and thermal dissipation requirements.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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