TÉCNICO LISBOA

Lab 4: Audio Amplifier

Circuit Theory and Electronics Fundamentals

Mestrado Integrado Engenharia Física Tecnológica, Técnico, University of Lisbon

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Contents

1 Introduction

The objective of this laboratory assignment is to build an Audio Amplifier using a transistor based circuit with a gain stage and an output stage. The circuit can be seen in Figure 1.

In Section 2, the circuit was built ,tested and adjusted to give the expected results. In Section 3, it was used the transistor large signal Ebbers-Moll model to study the DC component and the transistor small signal model for the AC component. The results are compared to the simulation results obtained in Section 2. The conclusions of this study are outlined in Section 9.

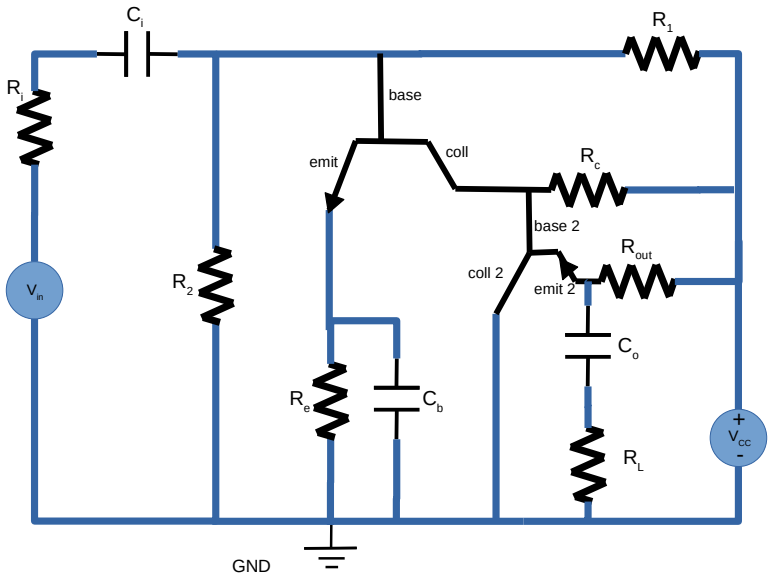

Figure 1: Audio Amplifier

2 Simulation Analysis

2.1 Operating Point Analysis

Table 1 shows the simulated operating point results for the circuit under analysis.

Name	Value [A or V]
@cb[i]	0.000000e+00
@ci[i]	0.000000e+00
@co[i]	0.000000e+00
@q1[ib]	5.415187e-05
@q1[ic]	9.700371e-03
@q1[ie]	-9.75452e-03
@q1[is]	8.305429e-12
@q2[ib]	4.797253e-04
@q2[ic]	7.149508e-02
@q2[ie]	-7.19748e-02
@q2[is]	-8.31222e-12
@r1[i]	1.384448e-04
@r2[i]	8.429297e-05
@rc[i]	9.220646e-03
@re[i]	9.754523e-03
@rin[i]	0.000000e+00
@rl[i]	0.000000e+00
@rout[i]	-7.19748e-02
base	1.685859e+00
coll	8.311742e+00
emit	9.754523e-01
emit2	9.121008e+00
in	0.000000e+00
in2	0.000000e+00
out	0.000000e+00
vcc	1.200000e+01

Table 1: Operating point. A variable preceded by @ is of type *current* and expressed in Ampere; other variables are of type *voltage* and expressed in Volt.

2.2 Transient Analysis

Figures 2, 3 and 4 show the simulated transient analysis results for the circuit under analysis.

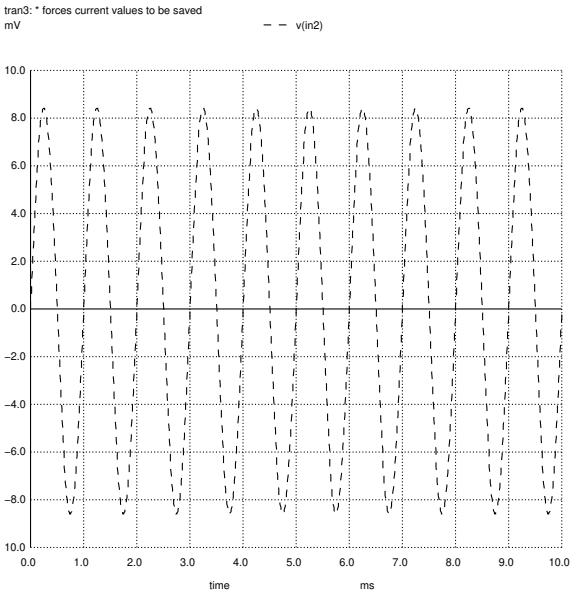

Figure 2: Transient input voltage

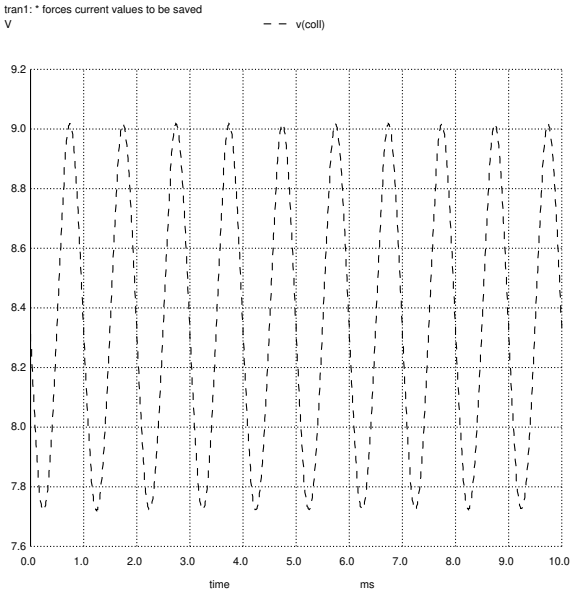

Figure 3: Transient output voltage, Gain Stage

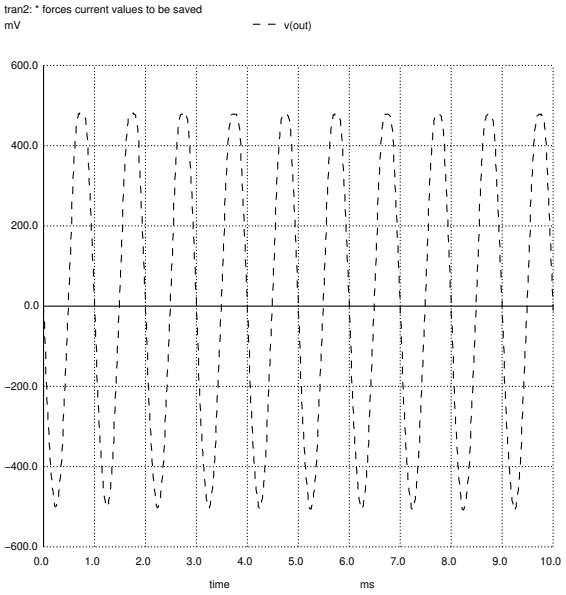

Figure 4: Transient output voltage

2.3 Frequency Analysis

2.3.1 Magnitude Response

Figures 5 and 6 show the magnitude of the frequency response for the circuit under analysis.

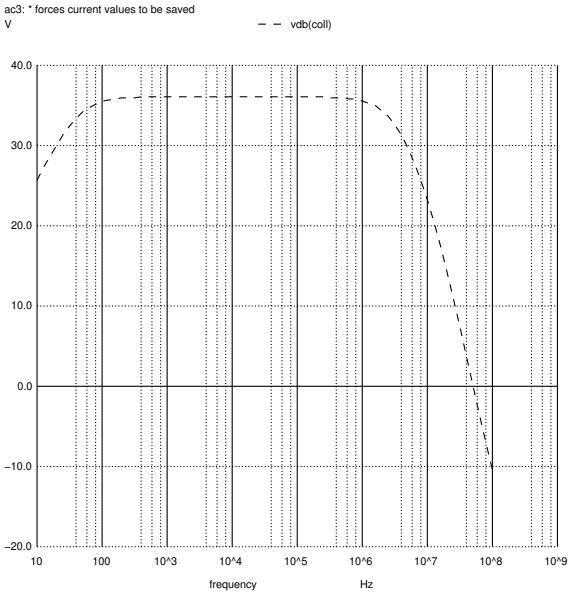

Figure 5: Magnitude response, Gain Stage

The maximum gain for the Output is of 34.60573dB.

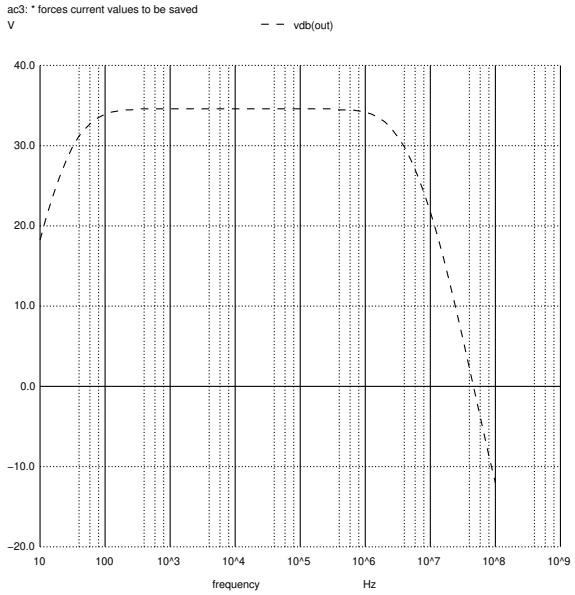

Figure 6: Magnitude response, Output Stage

2.3.2 Input Impedance

The simulation gives an input impedance of 555.9097Ω which is very good compared to $R_{in} = 100\Omega$.

2.3.3 Output Impedance

The simulation gives an output impedance of 4.2725Ω which is reasonable compared to $R_L = 8\Omega$.

3 Theoretical Analysis

In this section, the eletrical device shown in Figure 1 is analysed theoretically to predict the output of the Gain Stage and Output Stage circuits.

4 Operating Point

4.1 Gain Stage

The DC Analysis corresponds to a frequency of zero Hz which means that the capacitors are equivalent to an open circuit. For the bias circuit, it was considered the Thévenin's equivalent with $R_{eq1} = R_1||R_2$ and $V_{eq1} = \frac{R_2}{R_1+R_2} \times V_{CC}$ Using KVL we get:

$$V_{eq1} + R_{eq} \times I_{B1} + V_{BEON} + R_E \times I_{E1} = 0 \tag{1}$$

From the transistor model:

$$I_{E1} = (1 + \beta_F) \times I_{B1} \tag{2}$$

$$I_{C1} = \beta_F \times I_{B1} \tag{3}$$

Using the ohm's law and the KVL in the other loop we get the voltages:
Comparing the theoretical values with the simulation, they are satisfyingly close.

Operating Point	Value (V/A)
I_{B1}	0.000054529800057
I_{C1}	0.009744475270257
I_{E1}	0.009799005070315
V_{E1}	0.979900507031474
V_{O1}	8.102209891897063
V_{CE}	7.122309384865589

Table 2: Solutions to Node Analysis Method

4.2 Output Stage

Using the same methods:

$$V_{I2} - V_{CC} + V_{EBON} + R_E \times I_E = 0 \tag{4}$$

$$V_O = V_{CC} - R_E \times I_E \tag{5}$$

We get the following results:

Operating Point	Value (V/A)
V_{I2}	8.102209891897063
I_{E2}	0.079944752702573
I_{C2}	0.079594578577726
V_{E2}	8.802209891897062

Table 3: Solutions to Node Analysis Method

Comparing the theoretical values with the simulation, they are pleasantly close.

5 Gain

In the these and the following setions we are going to use the incremental model for the transistors and having in mind that the capacitors operate as approximately a short circuit for higher frequencies.

5.1 Gain Stage

Using another Thévenin's equivalent for the source signal and the bias circuit, we get $R_{eq2} = R_{eq1}||R_S$ and $v_{eq2} = \frac{R_{eq1}}{R_{eq1}+R_S} \times v_I$. Keeping in mind that the incremental parameters are given by $R_{\pi 1} = \frac{\beta_F}{g_{m1}}$, $g_{m1} = \frac{I_C}{V_T}$ and $R_{o1} \approx \frac{V_A}{I_C}$

And doing mesh analysis and making $R_E = 0$(because of the bypass capacitor), the gain is given by:

$$AV_1 = \frac{R_{eq1}}{R_{eq1} + R_S} \times R_C \times \frac{R_E - g_{m1}R_{\pi 1}R_{o1}}{(R_{o1} + R_C + R_E) \times (R_{eq2} + R_{\pi 1} + R_E) + g_{m1}R_E R_{\pi 1} R_{o1} - R_E^2} = 41.626dB \tag{6}$$

5.2 Output Stage

Aplying KCl, we get directly:

$$AV_2 = \frac{g_{m2}}{g_{\pi 2} + g_{out} + g_{o2} + g_{m2}} = 0.98724 \tag{7}$$

Where $g_{\pi 2} = \frac{1}{R_{\pi}2}$, $g_{out} = \frac{1}{R_{out}}$ and $g_{o2} = \frac{1}{R_{o2}}$

5.3 Total Circuit

In this calculation the whole circuit is taken into consideration, simplifying the Gain Stage.

$$AV = \frac{g_B + \frac{g_{m2} * g_B}{g_{\pi 2}}}{g_B + g_{out} + g_{o2} + \frac{g_{m2} * g_B}{g_{\pi 2}}} \times AV_1 = 41.173 \tag{8}$$

6 Input impedance

This is calculated by imposing a voltage in the imput terminals and measuring the current through it we get the imput impedance by dividing them $Z_I = \frac{v_i}{I}$.

6.1 Gain Stage

Doing mesh analysis and solving for the wanted current, we get($R_E = 0$):

$$Z_{I1} = \frac{1}{(\frac{1}{R_B} + \frac{1}{((((r_{o1}+R_{C1}+R_E)*(r_{\pi 1}+R_E)+g_{m1}*R_E*r_{o1}*r_{\pi 1}-R_E^2)/(r_{o1}+R_{C1}+R_E)))})} = 445.51\Omega \tag{9}$$

This value is sort of compatible because Z_{I1} is 4.5x greater than R_S.

6.2 Output Stage

Using the gain expression and doin a simple ohm's law, we get

$$Z_{I2} = \frac{(g_{m2} + g_{\pi 2} + g_{o2} + g_{out})}{(g_{\pi 2})(g_{\pi 2} + g_{o2} + g_{e2})} = 5595.5\Omega \tag{10}$$

6.3 Total Circuit

We considered it equal to $Z_I = Z_{I1} = 445.51\Omega$.

7 Output impedance

This is calculated by shutting off the imput source and imposing a voltage in the output terminals and measuring the current through it, we get the output impedance by dividing them $Z_O = \frac{v_O}{I}$

7.1 Gain Stage

Looking at the circuit we notice that $v_{\pi 1} = 0$ which means that the impedance seen by the test source is simply:

$$Z_{O1} = \frac{1}{\frac{1}{R_{o1}} + \frac{1}{R_C}} = 378.82\Omega \tag{11}$$

This value is compatible with Z_{I2} because Z_{I2} is much greater.

7.2 Output Stage

Applying KCL and noticing that $v_{\pi 2} = -v_o$:

$$Z_{O2} = \frac{1}{(g_{m2} + g_{\pi 2} + g_{o2} + g_{out})} = 0.31008\Omega \tag{12}$$

7.3 Total Circuit

$$Z_O = \frac{1}{g_{o2} + \frac{g_{m2} * g_B}{g_{\pi 2}} + g_{out} + g_B} = 1.8718\Omega \tag{13}$$

The total output impedance is compatible enough to connect to an 8Ω load.

8 Frequency response

Using the complete incremental model for the circuit (with the capacitors on), applying the node method and solving ($AV = \frac{V_o}{V_i}$) for a $10Hz$ frquency up to $100MHz$, we get the following results:

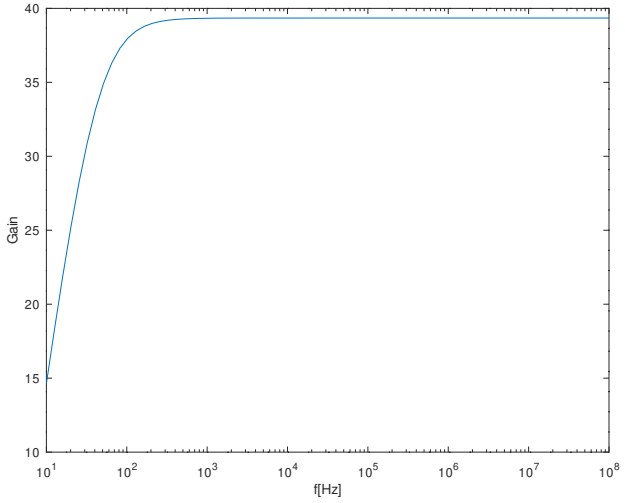

Figure 7: Frequency Response

9 Conclusion

In this laboratory assignment the objective of building an Audio Amplifier has been achieved. The output analyses has been performed both theoretically using the Octave maths tool and by circuit simulation using the Ngspice tool. The simulation results differed from the theoretical

results as was expected because of the non-linear components used. The final merit was of 1194.911322 with a cost of 3095.24 MU, for the simulation the Voltage gain, bandwith and lower cut off frequency were of 57.09831355, $2864235.782Hz$ and $44.2183Hz$, respectively. The diferences in the gain, input and output impedances between the theoretical and simulation analysis are explained by the difference in simplicity between the incremental model and all the approximations used in the theoretical analyse and the very complex model used by ngspice.