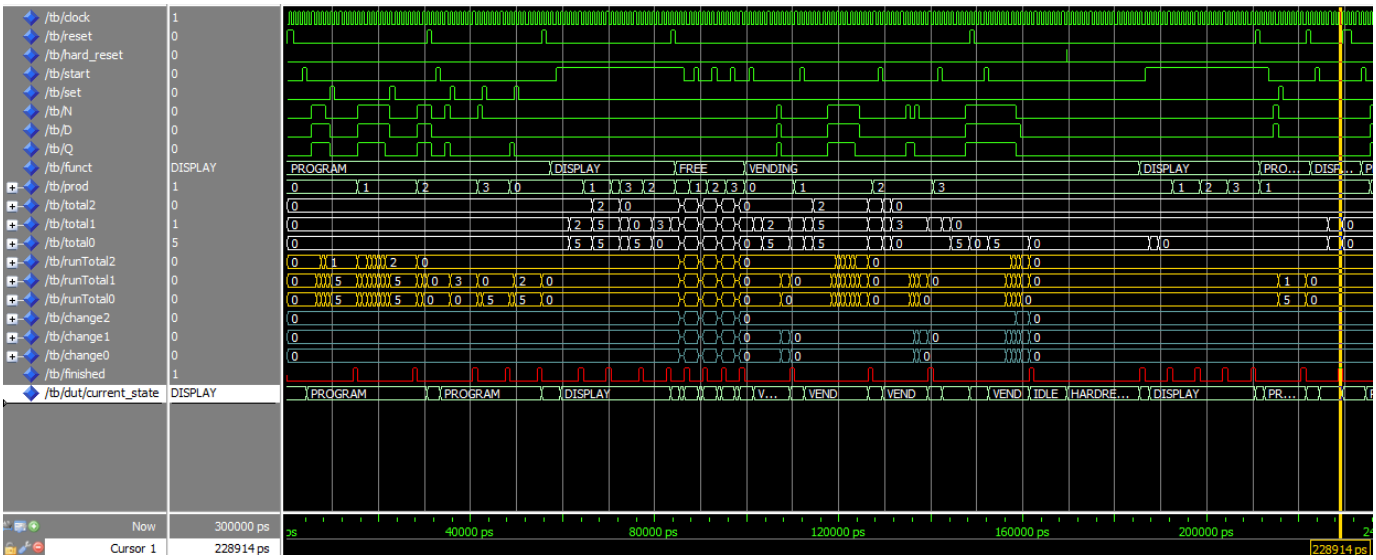
VENDING MACHINE

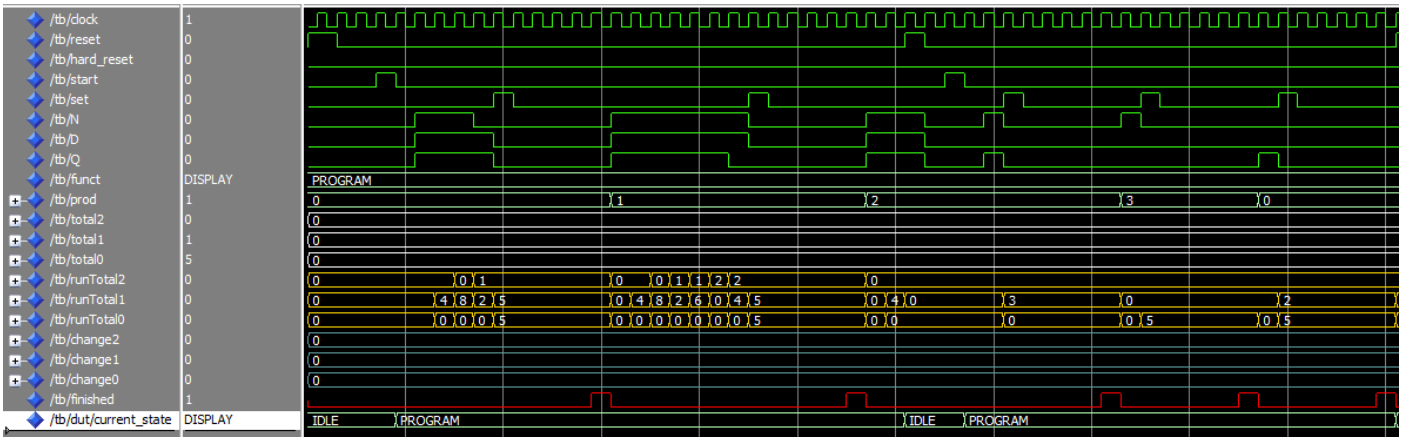
Test



Complete test waveform

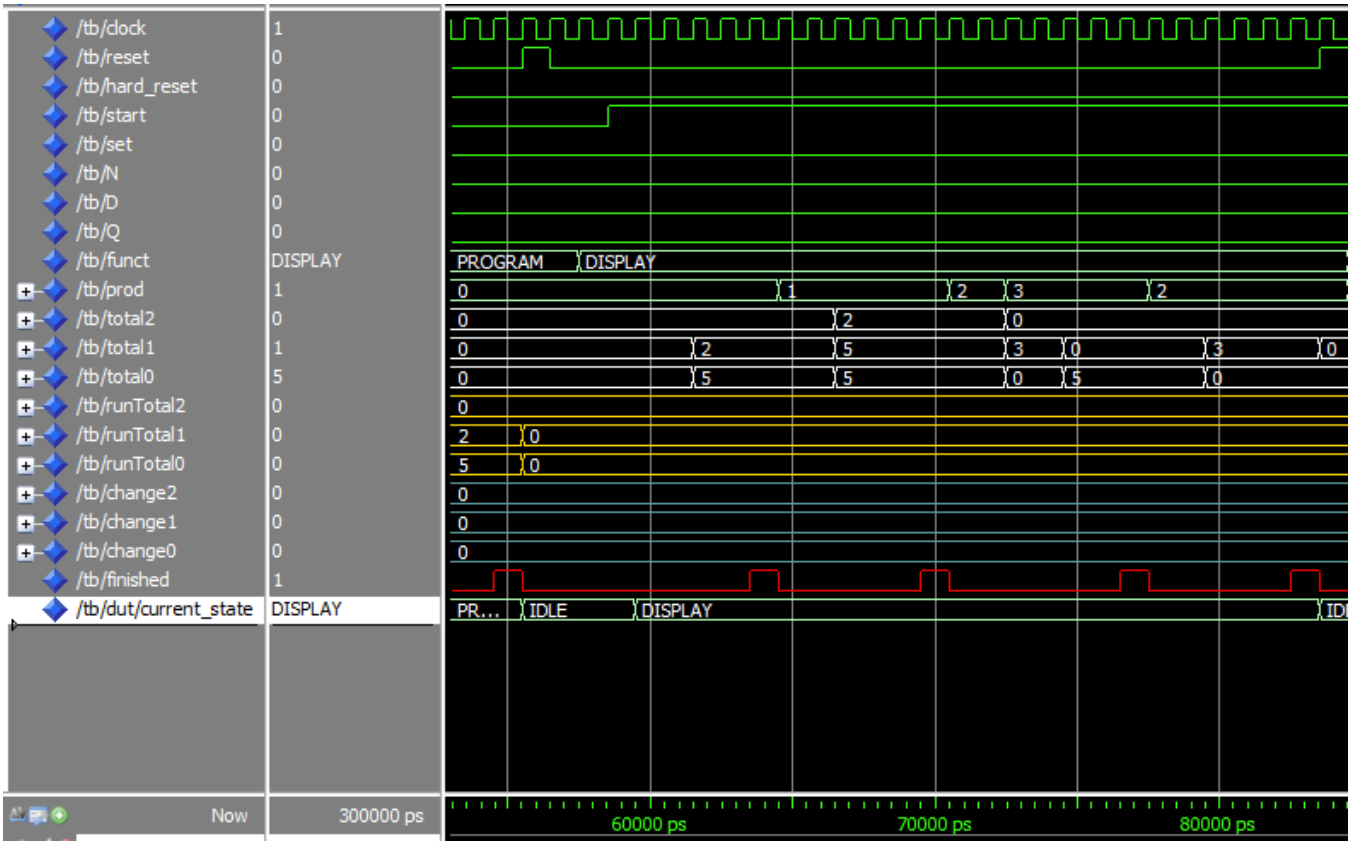
In the test bench all the modes of operation are tested in the following order

1. Program
    a. Program prod 0 = 155
    b. Program prod 1 = 255
    c. Program prod 2 = 40 (abort with reset)
    d. Program prod 2 = 30
    e. Program prod 3 = 5
    f. Re-program pro 0 = 25



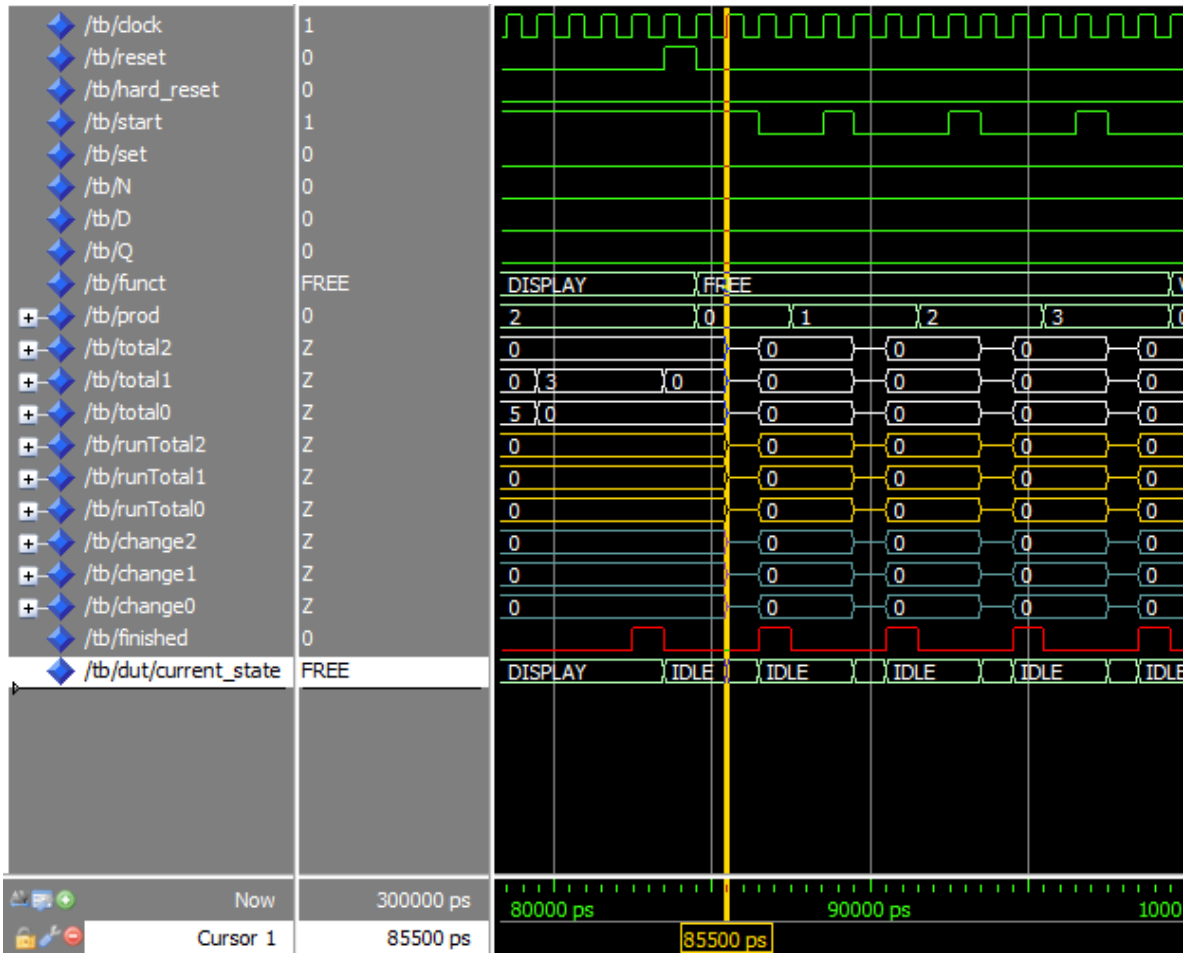
2. Display
    a. Display prod 0 = 25
    b. Display prod 1 = 255
    c. Display prod 2 = 30 (abort with reset, finished is not asserted

d. Display prod 3 = 5
e. Display prod 2 = 30

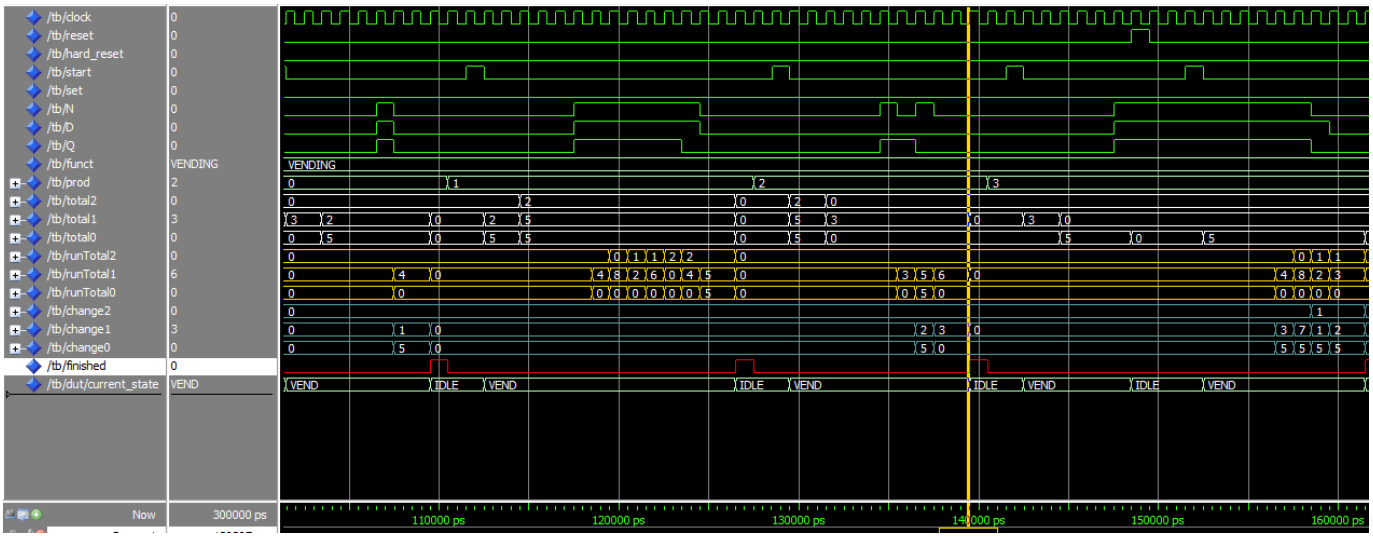


3. FREE MODE
    a. Free prod 0
    b. Free prod 1
    c. Free prod 2
    d. Free prod 3

Outputs set to floating while system is in FREE state, after 1 cycle finished is asserted and system returns to IDLE

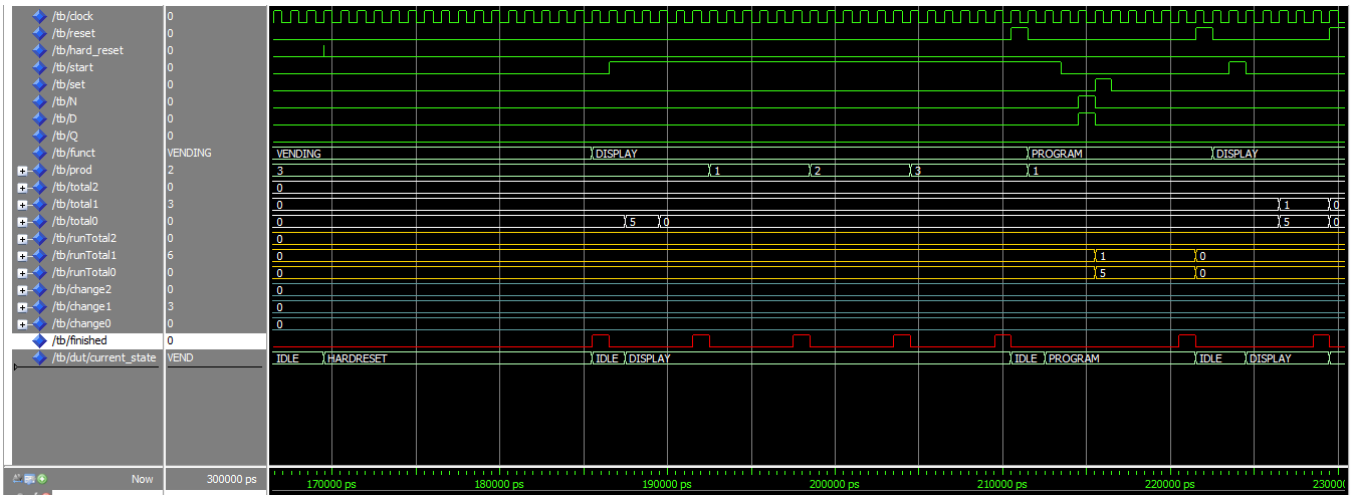


4. Vending
    a. Buy prod 0 with extra cash
        i. Cost = 25, cash = 40, change = 15
    b. Buy prod 1 with exact cash
        i. Cost = 255, cash = 255, change = 0
    c. Buy prod 2 introducing extra cash for 2 cycles
        i. Cost = 30, cash = 60, change = 30
    d. Buy prod 3 with a reset aborting 1 time the operation



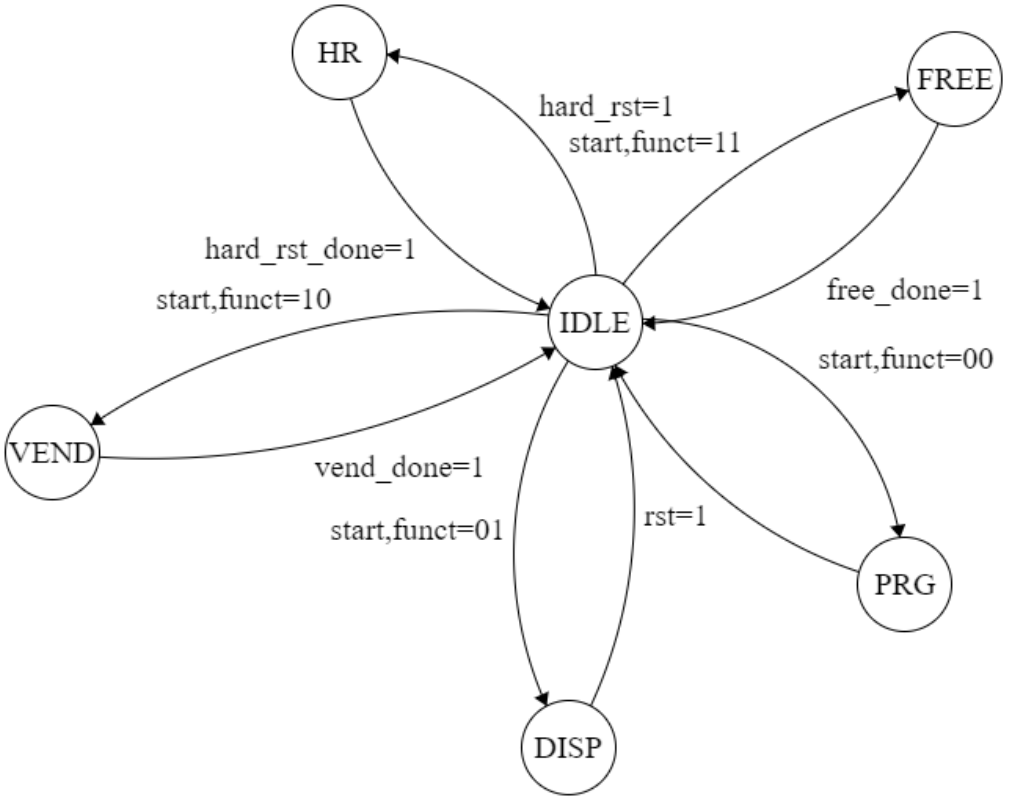
5. HARD RESET
    a. HARD reset and flush memory
    b. Display all prods = 0
    c. Program prod1 = 15
    d. Display prod1 = 15

The Hard Reset is implented inside the program module adding 1 state to the state machine to use the same Hardware to write 0 to all memory

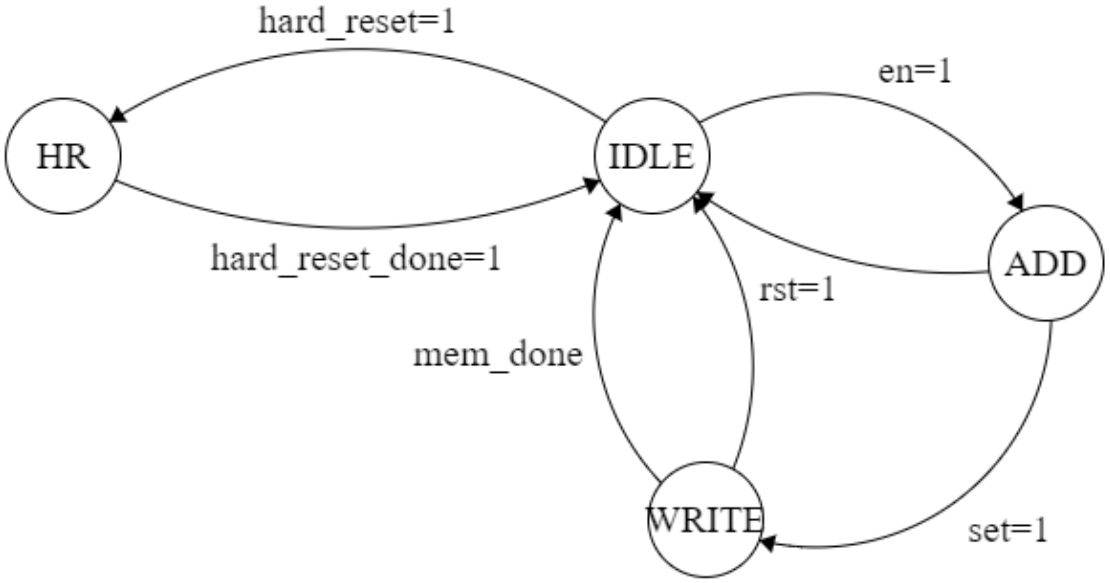


STATE MACHINE

VMC



Program FSM


hard_reset=1
HR
IDLE
en=1
ADD
hard_reset_done=1
rst=1
mem_done
WRITE
set=1