MODELING THE RC-INTERCONNECT EFFECTS IN A HIERARCHICAL TIMING ANALYZER[1]

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Abstract

An approach for accurately modeling the RC-interconnect delay and gate-loading effects in a hierarchical timing analyzer is presented. The change in gate-loading due to interconnect resistance is considered by an "effective capacitance" approximation. The RC-interconnect path delays are precharacterized in terms of an interpolating polynomial function.

Introduction

For today's VLSI designs, circuit size often dictates that timing analysis is performed hierarchically. The hierarchical nature of the analyzer allows a path to be modeled from the cell level to the gate level or some combination thereof. For efficiency, gate (or cell) delays and output transition times are often modeled as an empirical function of the input signal transition time and total gate-load capacitance. The empirical model approximates the *waveform response*, hence the delay, at the output of the gate, or the driving point of the interconnect. For the total delay to the fanout points of interest, this "gate delay" is then added to the RC-delay along the interconnect paths. It is desirable that the RC-interconnect be precharacterized to avoid its repeated analysis during the timing evaluation [1-5].

To understand the hierarchical timing analysis approach, consider the simple example in Fig. 1(a). In this example, each block is a gate or complete logic cell. In general, function F_1 in Fig. 1(b) predicts the delay(t_d) for block 1 in terms of input transition time (t_t) and total output net capacitance (C_{tot}). A similar function, F_2(Fig. 1(b)), predicts the output transition time(t_x) in terms of the same parameters. The delay, t_d, is the difference between the 50% point on the input and the 50% point on the output while the transition time, t_x, is the 0% to 100% transition time of the output signal.

Given C_{tot} and t_t, the block delay (t_d) and the output transition time(t_x) are evaluated as shown in Fig. 1(b). Next, this signal is driven into an RC model for the interconnect of the driver (Fig. 1(c)). Often a lumped RC tree is used for the interconnect circuit model to approximate the delay from the driver to each fanout point of interest.

One difficulty with this empirical modeling approach is the total net capacitance is often an overestimate of the capacitance "seen by" the gate. In other words, the total net capacitance always over-estimates the driving-point admittance of the RC-interconnect to some degree. But in particular, for high-frequency signals or long metal lines, the interconnect resistance "shields" some of the load capacitance, thus making the delay approximation significantly pessimistic[5,6]. A higher order circuit model can be used to approximate driving-point admittance[5,10], however, such models are not compatible with the empirical modeling schemes.

In this paper, we first present an *effective capacitance* approximation for reducing the pessimistic delay estimates of empirical models. Then, with an accurate driving-point waveform approximation, the RC-interconnect delays and transition times are precharacterized using interpolated piecewise functions. The overall result is an efficient, yet accurate, characterization of the RC effects of metal interconnect for high-speed circuits.

Interconnect Resistance Effects

The resistance of the interconnect tends to "shield" some of the load capacitance from the driver, particularly on long interconnects such as clock or bus lines. Thus, the total capacitance (C_{tot}) will always cause the gate delay to be overestimated. In many cases this overestimate will be slight and can be ignored, but for high-speed switching it can be quite large. This shielding effect can be modeled using a higher order driving point admittance model [5,10] such as the π-model in Fig. 2(d).

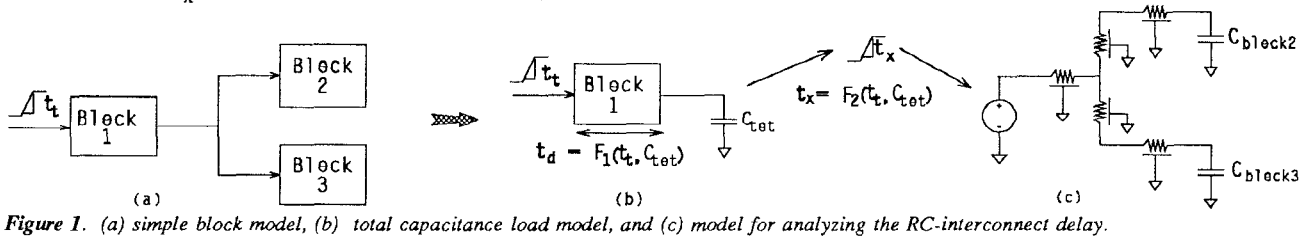

Figure 1. *(a) simple block model, (b) total capacitance load model, and (c) model for analyzing the RC-interconnect delay.*

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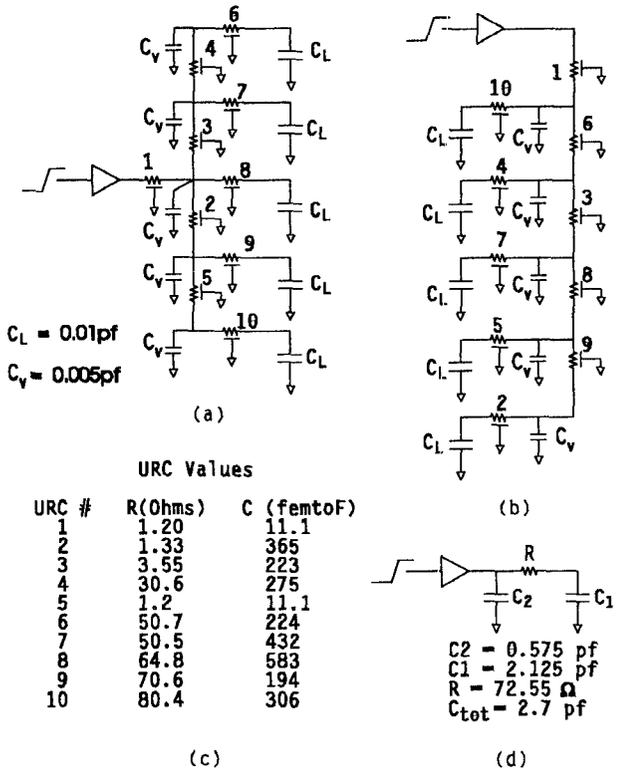

URC Values

URC #	R(Ohms)	C (femtoF)
1	1.20	11.1
2	1.33	365
3	3.55	223
4	30.6	275
5	1.2	11.1
6	50.7	224
7	50.5	432
8	64.8	583
9	70.6	194
10	80.4	306

Figure 2. Two different layouts with the same amount of metal and metal capacitance. The π-model in (d) is needed to model the shielding in (b).

To illustrate the resistance shielding effect, consider the two interconnects in Fig. 2 which consist of the same amount of metal and the same loads and drivers. Only the placement of the uniform RC segments (URC's) has been changed. The plots of two PSPICE[7] transient simulations in Fig. 3 reveal that for the circuit in Fig. 2(a), C_{tot} reasonably approximates the driving point admittance of the interconnect and loads.

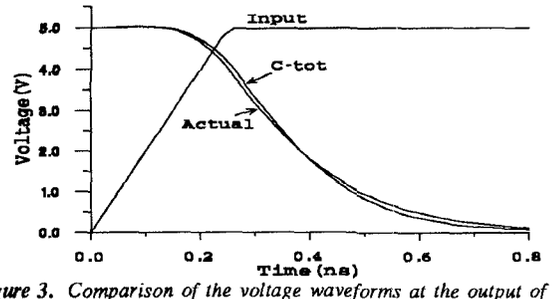

Figure 3. Comparison of the voltage waveforms at the output of the gate in Fig. 2(a) when driving the actual net and just a C_{tot} load.

In Fig. 4, however, a large error is revealed when the same comparison is attempted for the net in Fig. 2(b). Here, C_{tot} causes the delay to be overestimated by a large percentage. This indicates that delay is not only dependent on the area of interconnect, but also the specific layout. Moreover, the π-model of Fig. 2(d) matches the actual loading very well in Fig. 4.

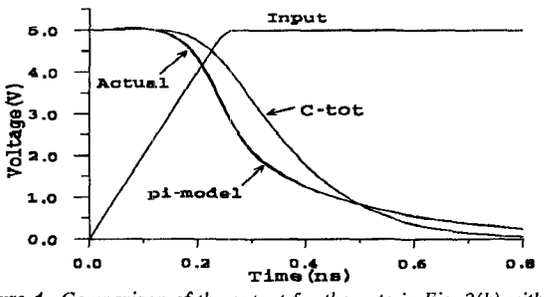

Figure 4. Comparison of the output for the gate in Fig. 2(b) with the same gate driving the total capacitance, C_{tot} ,and the π-model.

Modeling the Effective Gate-Loading

The total capacitance of the net can be shown to be the first moment of the driving point admittance. This first-order approximation is valid whenever the signal-frequencies at the gate-output are low enough so that resistance shielding is not a factor. The validity of the empirical delay model approximation using C_{tot} can be tested by considering the waveform approximation given by F_1 and F_2 to be the voltage waveform on the driving point of the π-model, as shown in Fig. 5. Note that if the signal frequencies at the driving point are low enough, which is dependent upon the relative values of t_x and the π-model resistance, then C_{tot} is a valid assumption.

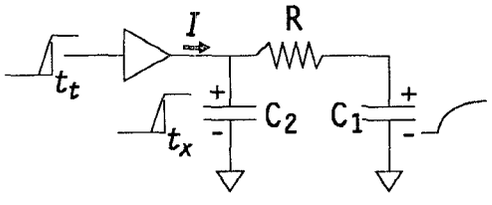

Figure 5. An inverter driving a π-model.

From Fig. 5 one may conclude that the C_{tot} assumption is valid if the total current out of the gate, *I*, is the same for both the C_{tot} and the π-model loads. The current, *I*, during the output transition, is simply $V_{DD}C_{tot}/t_x$, for the idealized waveform model in Fig. 1. For the π-model, the total current is $V_{DD}C_2/t_x$ plus the current into capacitor C_1. The voltage waveform on C_1 is an exponential function, therefore, its current is not readily known.

In order to compare the C_{tot} and π-model currents, the current into C_1 can be averaged for the time range of interest. First, the current in C_1 can be solved for by evaluating the single RC circuit (RC_1) with C_2's voltage as the forcing function. The simplest forcing function would be a single saturate-ramp, as shown in Fig. 5, however, the average current in C_1 is very sensitive to the voltage wave shape at C_2. Therefore, a more accurate wave shape model is to consider the voltage at C_2 to be a quadratic wave-shape up to the 20% point, and a ramp from the 20 to 50% point. These waveform points are obtainable from the empirical equations for t_d and t_x[6]. The resulting current-waveform at C_1 is then aver-

aged over this time range of interest (see Fig. 5)[6].

But along with verifying the accuracy of the C_{tot} assumption, determining an "effective loading capacitor" value is even more desirable. From the sum of the average current in C_1 and C_2, there is a unique effective capacitance value which has the same average current over the time range of interest[6]:

$$C_{eff} = C_2 + \frac{C_1}{t_d}\left[t_d - RC_1\left(3 - e^{-\frac{0.3t_x}{RC_1}}\right) + \frac{2R^2C_1^2}{t_d - 0.3t_x}\left(1 - e^{-\frac{t_d - 0.3t_x}{RC_1}}\right)\right] \quad (1)$$

If the relative values of the transition time and the π-model are such that C_{tot} is a valid assumption, the C_{eff} value from equation (1) will be very close to C_{tot}. This is easily realized since in the limit as R approaches zero, C_{eff} approaches C_1+C_2, which is equal to C_{tot}[5,6,10]. Similarly, in the limit as R tends toward infinity (maximum shielding), the C_{eff} value approaches that of the first capacitor in the π-model, C_2.

A plot of Eq. (1) as a function of t_d (for a single value of t_x) is shown in Fig. 6. Eq. (1) displays an exponential form which starts at a value of C_2 and asymptotically approaches C_{tot} (C_1+C_2). Also shown on this graph are plots of the empirical delay equations for two different driver sizes as a function of load capacitance. Note that for the small buffer the curves intersect at a C_{eff} value which is very close to C_{tot}. For the larger buffer, however, which is characterized by a smaller "effective resistance" and hence higher signal-frequencies at the driving point, the curves intersect at a C_{eff} value much smaller than C_{tot}.

To improve the delay approximation for the larger buffer case, C_{eff} is used to evaluate F_1 and F_2 as was done originally for C_{tot}, resulting in new values for t_d and t_x. These new values are then used in Eq. (1) to determine the accuracy of this C_{eff} value, etc. These iterations are continued until convergence is reached. Note that there is always one unique solution as evidenced by the plot in Fig. 6, and that the C_{eff} curve moves only slightly as a function of t_x, from one iteration to the next. It should be added that the ability to iterate requires that the C_{eff} model approximate both the delay and the transition time to the 50% point accurately, thus the reason for the careful selection of the general voltage wave shapes on C_2 for averaging the current at C_1.

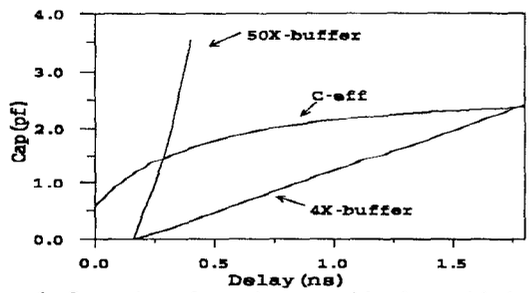

Figure 6. Comparison of capacitance vs. delay for empirical models of 4X and 50X CMOS buffers along with the effective capacitance predicted by Eq. 1.

The plot in Fig. 7 compares the C_{eff} model with the π-model for the example in Fig. 2(b). Note that the curves agree extremely well through the 20% and 50% points. After these points, however, the errors can be quite large, since the C_{eff} expression does not go beyond time t_d in averaging the current at C_1. Eq. (1) could be modified to reach the 80% point, however the overall accuracy up to that point may be compromised.

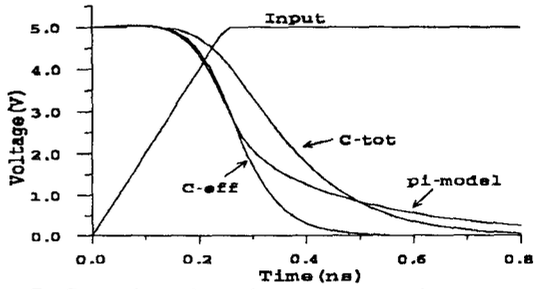

Figure 7. Comparison of actual response versus the response when C_{eff} is used for the circuit in Fig. 2(b).

Further results are revealed in Table 1 for various driver sizes and RC-nets. Both the 20% and 50% delays are shown using the C_{tot}, C_{eff}, and π-model. The most dramatic improvement is seen in the last example which improves from a +500% to a few percent delay error.

Precharacterizing the RC Delay

After t_d and t_x have been determined, the next step is to determine the delay due to the RC interconnect between the gate/cell output and fanout points. The RC fanout is usually modeled with an RC tree or mesh while loads are modeled by linear capacitances.

The RC net is first analyzed by applying Asymptotic Waveform Evaluation (AWE)[8,9] to produce an approximation for the step-response. The general form of the step-response is easily combined via superposition with a saturated input ramp signal to produce the following output waveform expression in terms of t_x:

$$v(t) = \begin{cases} \frac{1}{t_x}\left[t - T_D + \sum_{i=1}^{q}\frac{K_i}{p_i}e^{p_i t}\right] & t \le t_x \\ 1 + \frac{1}{t_x}\sum_{i=1}^{q}\left[\frac{K_i}{p_i}\left(e^{p_i t} - e^{p_i(t-t_x)}\right)\right] & t > t_x \end{cases} \quad (2)$$

In Eq. 2, p_i and k_i are the approximate dominant poles and residues, respectively, of the unit-step response[8]. Eq. 2 can be solved for the delay at any logic threshold by applying Newton-Raphson (N-R) iterations. N-R will usually converge to within 1 percent in 2-3 iterations. This fast convergence is due to a good first guess produced by the equation

$$t_g = rt_x + T_D \ln\left(\frac{1}{1-r}\right) \quad (3)$$

where T_D is the Elmore delay (first moment), r the logic threshold (0.5), and t_x the transition time.

For cases where a given RC net must be analyzed many (perhaps thousands) of times, there is a more efficient method for evaluating the delays from (2). This

Table 1. *Results for various buffer sizes and interconnects. All examples use t_t = 250ps thus the gate delay is obtained by subtracting 125ps from the 50% waveform time points in the table.*

Ckt	20 % waveform point(ps) using:			50 % waveform point(ps) using:			π-Model Parameters			C-eff (pf)	# Iterations
	C-tot	π-model	C-eff	C-tot	π-model	C-eff	C2(pf)	C1(pf)	R(Ω)		
30x-1	253	204	207	347	272	263	1.463	0.245	89.52	0.731	4
30x-2	358	222	241	509	267	285	0.283	3.849	232.0	0.577	4
30x-3	297	212	217	451	286	282	0.454	2.494	105.7	0.957	3
50x-2	262	215	219	350	276	272	0.575	2.125	72.55	1.23	2
200x	4496	1185	1240	10590	2231	2287	125.0	752.2	1618	126	2

involves solving (2) for a few (4-7) values of transition time and then using linear or quadratic interpolation during the actual timing analysis to produce the delay values. The efficiency of this technique is about 10-20 times that of using N-R for each new transition time since the transcendental ramp-response equation(2) is not repeatedly solved. Other interpolation methods such as cubic splines and classical moment-matching to a high-order exponential were also attempted, but interpolation with a linear or quadratic appeared the most attractive.

For example, consider again the interconnect in Fig. 2(b). By solving its ramp-response equation (2) for the delay at several rise times and plotting the results, the graph in Fig. 8 results. *This delay characteristic curve* completely characterizes the delay for the RC net over all possible values of transition-time.

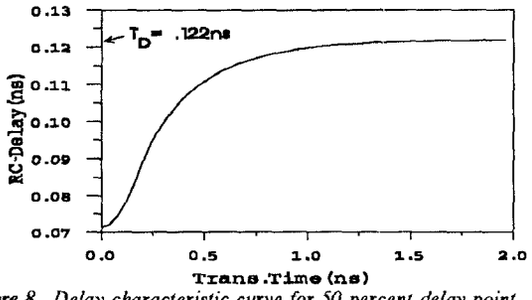

Figure 8. Delay characteristic curve for 50 percent delay point. For RC trees and meshes these curves always saturate to the Elmore delay value, regardless of the logic threshold chosen.

It should also be noted that these curves saturate to a constant value as the output of the RC net begins to *follow* the input, thus resulting in a ramp-follower, as illustrated by Fig. 9. Coincidentally, for RC trees and meshes, this value of delay saturation is the ubiquitous Elmore delay(T_D) which marks the separation distance between the position of the input ramp and the steady-state asymptote for its response[6,8]. Therefore, when the rise/fall time is long compared to the Elmore delay ($>5T_D$), then T_D may be used as the delay value.

Conclusions

A technique has been presented for alleviating the pessimism of empirical gate-delay models by modeling the RC loading by an *effective capacitance* load. In addition, the subsequent RC interconnect delay which is added to the gate-delay is precharacterized in terms of simple piecewise polynomials.

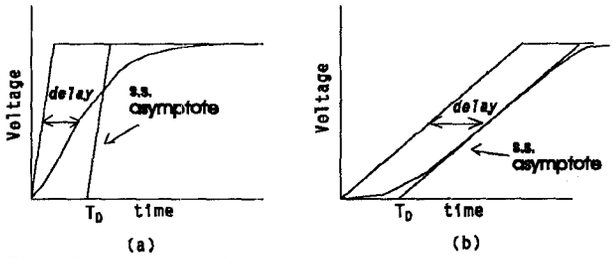

Figure 9. An example of the ramp response and delay using fast (a) and slow signals (b).

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