LECTURE 220 – INTRODUCTION TO OP AMPS

LECTURE OUTLINE

Outline

- Op Amps
- Categorization of Op Amps
- Compensation of Op Amps
- Miller Compensation
- Other Forms of Compensation
- Op Amp Slew Rate
- Summary

***CMOS Analog Circuit Design*, 2nd Edition Reference**

Pages 243-269

OP AMPS

What is an Op Amp?

The op amp (operational amplifier) is a high gain, dc coupled amplifier designed to be used with negative feedback to precisely define a closed loop transfer function.

The basic requirements for an op amp:

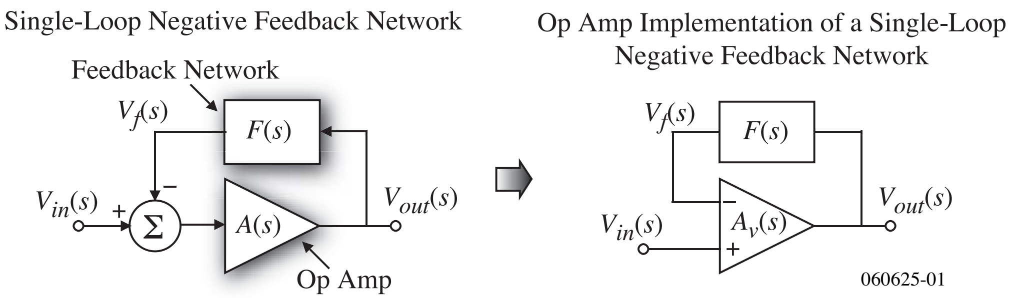
- Sufficiently large gain (the accuracy of the signal processing determines this)
- Differential inputs
- Frequency characteristics that permit stable operation when negative feedback is applied

Other requirements:

- High input impedance
- Low output impedance
- High speed/frequency

Why Op Amps?

The op amp is designed to be used with single-loop, negative feedback to accomplish precision signal processing as illustrated below.



The voltage gain, $\frac{V_{out}(s)}{V_{in}(s)}$, can be shown to be equal to,

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{A_v(s)}{1+A_v(s)F(s)}$$

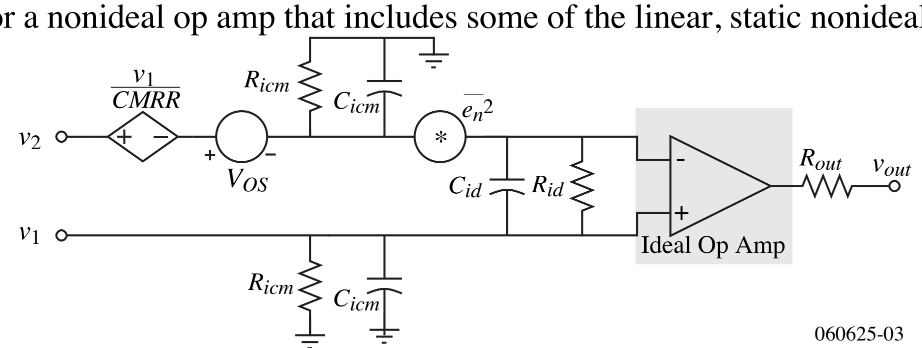
If the product of $A_v(s)F(s)$ is much greater than 1, then the voltage gain becomes,

$$\frac{V_{out}(s)}{V_{in}(s)} \approx \frac{1}{F(s)}$$ ⇨ The precision of the voltage gain is defined by $F(s)$.

OP AMP CHARACTERIZATION

Linear and Static Characterization of the CMOS Op Amp

A model for a nonideal op amp that includes some of the linear, static nonidealities:



where

R_{id} = differential input resistance
C_{id} = differential input capacitance
R_{icm} = common mode input resistance
R_{icm} = common mode input capacitance
V_{OS} = input-offset voltage
$CMRR$ = common-mode rejection ratio (when v_1=v_2 an output results)
$\overline{e_n^2}$ = voltage-noise spectral density (mean-square volts/Hertz)

Linear and Dynamic Characteristics of the Op Amp

Differential and common-mode frequency response:

$$V_{out}(s) = A_v(s)[V_1(s) - V_2(s)] \pm A_c(s)\left(\frac{V_1(s)+V_2(s)}{2}\right)$$

Differential-frequency response:

$$A_v(s) = \frac{A_{v0}}{\left(\frac{s}{p_1}-1\right)\left(\frac{s}{p_2}-1\right)\left(\frac{s}{p_3}-1\right)\cdots} = \frac{A_{v0}\,p_1p_2p_3\cdots}{(s-p_1)(s-p_2)(s-p_3)\cdots}$$

where $p_1, p_2, p_3, \cdots$ are the poles of the differential-frequency response (ignoring zeros).

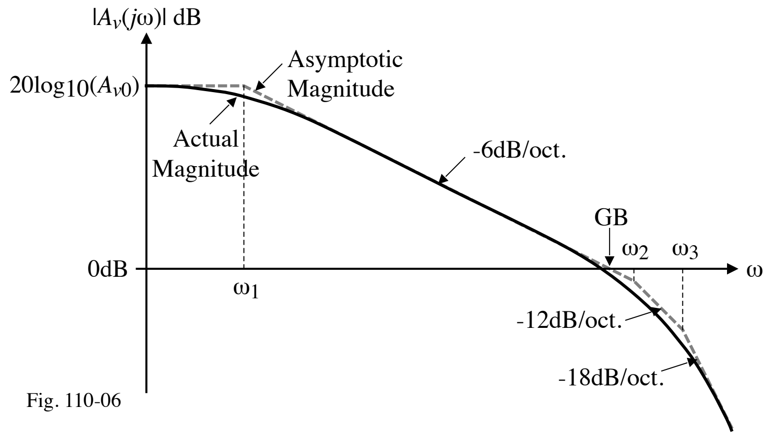


Fig. 110-06

Other Characteristics of the Op Amp

Power supply rejection ratio (*PSRR*):

$$PSRR = \frac{\Delta V_{DD}}{\Delta V_{OUT}} A_v(s) = \frac{V_o/V_{in}\ (V_{dd}=0)}{V_o/V_{dd}\ (V_{in}=0)}$$

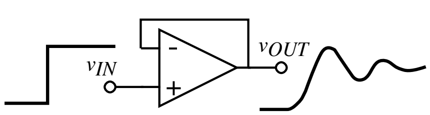
Input common mode range (*ICMR*):

ICMR = the voltage range over which the input common-mode signal can vary without influence the differential performance

Slew rate (*SR*):

SR = output voltage rate limit of the op amp

Settling time (T_s):



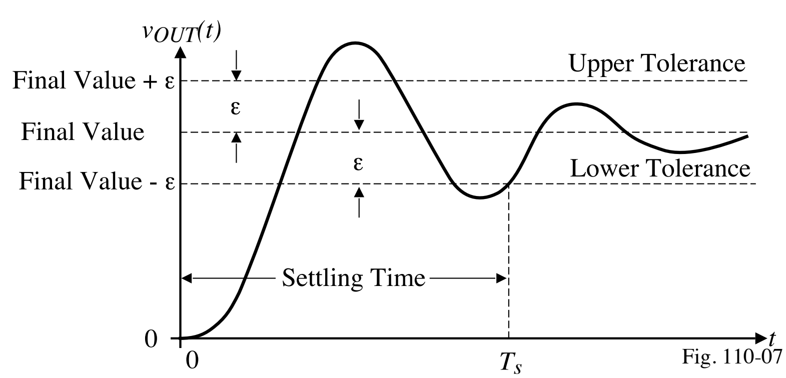


Fig. 110-07

OP AMP CATEGORIZATION

Classification of CMOS Op Amps

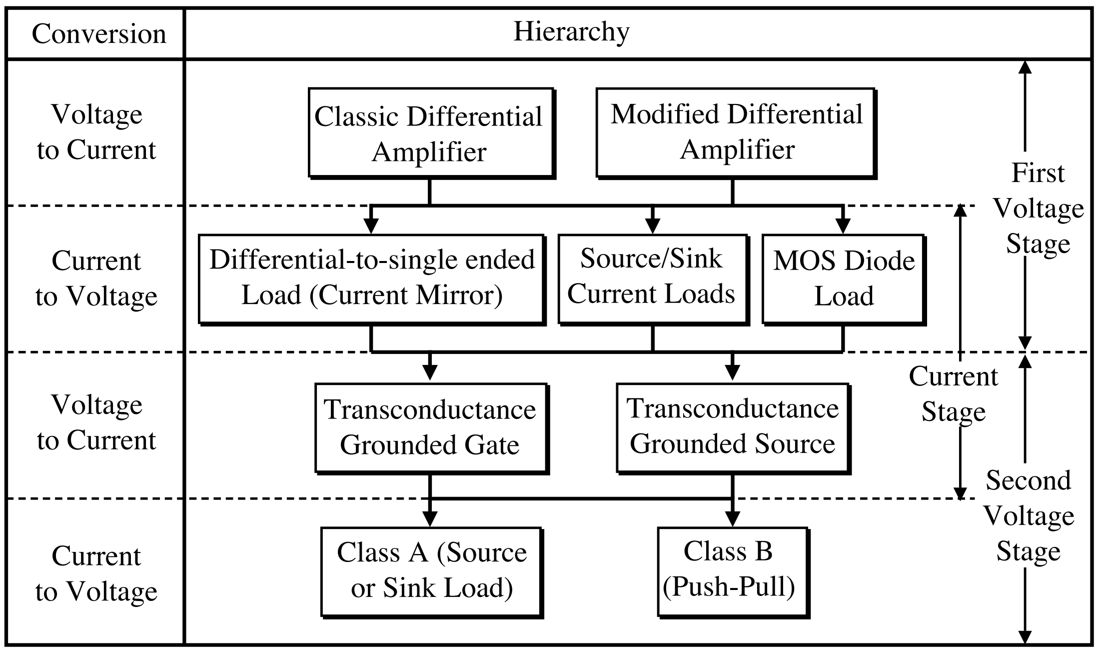


Table 110-01

Two-Stage CMOS Op Amp

Classical two-stage CMOS op amp broken into voltage-to-current and current-to-voltage stages:

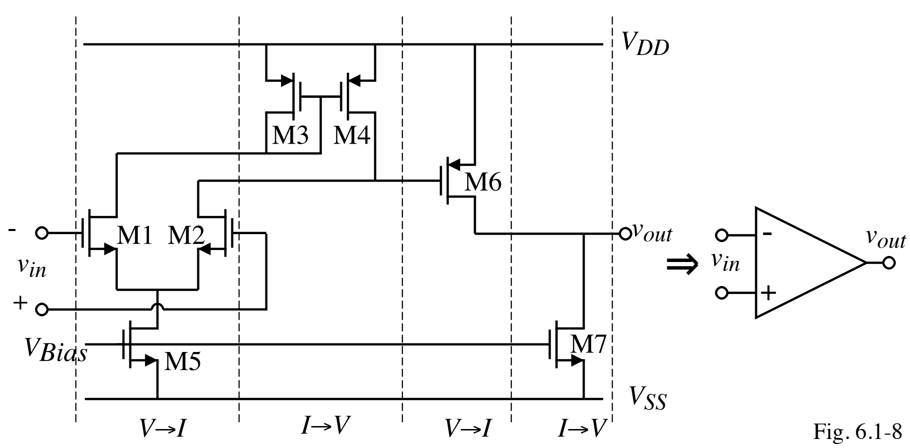
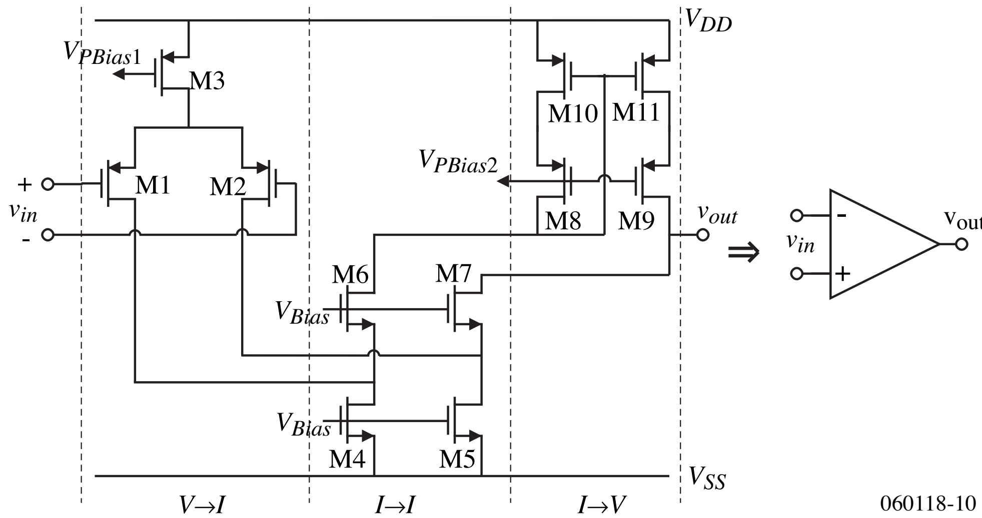


Fig. 6.1-8

Folded Cascode CMOS Op Amp

Folded cascode CMOS op amp broken into stages.



COMPENSATION OF OP AMPS

Compensation

Objective

Objective of compensation is to achieve stable operation when negative feedback is applied around the op amp.

Types of Compensation

1. Miller - Use of a capacitor feeding back around a high-gain, inverting stage.
   - Miller capacitor only
   - Miller capacitor with an unity-gain buffer to block the forward path through the compensation capacitor. Can eliminate the RHP zero.
   - Miller with a nulling resistor. Similar to Miller but with an added series resistance to gain control over the RHP zero.
2. Self compensating - Load capacitor compensates the op amp (later).
3. Feedforward - Bypassing a positive gain amplifier resulting in phase lead. Gain can be less than unity.

Because compensation plays such a strong role in design, it is considered before design.

Single-Loop, Negative Feedback Systems

Block diagram:

$A(s)$ = differential-mode voltage gain of the op amp

$F(s)$ = feedback transfer function from the output of op amp back to the input.

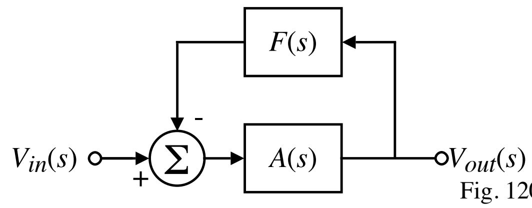


Fig. 120-01

Definitions:

- Open-loop gain = $L(s) = -A(s)F(s)$
- Closed-loop gain = $\dfrac{V_{out}(s)}{V_{in}(s)} = \dfrac{A(s)}{1+A(s)F(s)}$

Stability Requirements:

The requirements for stability for a single-loop, negative feedback system is,

$$|A(j\omega_{360°})F(j\omega_{360°})| = |L(j\omega_{360°})| < 1 \;\_\; |A(j\omega_{0°})F(j\omega_{0°})| = |L(j\omega_{0°})| < 1$$

where $\omega_{360°} = \omega_{0°}$ is defined as

$$\text{Arg}[-A(j\omega_{0°})F(j\omega_{0°})] = \text{Arg}[L(j\omega_{0°})] = 0° = 360°$$

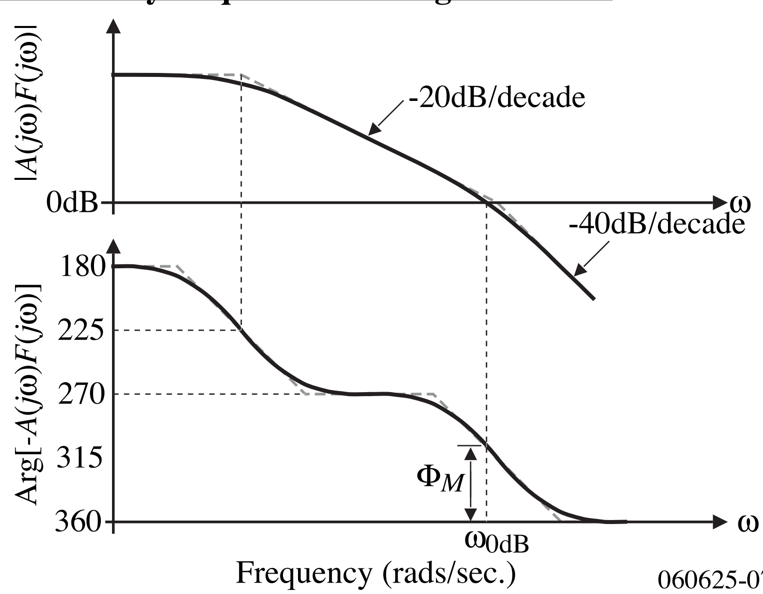
Another convenient way to express this requirement is

$$\text{Arg}[-A(j\omega_{0dB})F(jw_{0dB})] = \text{Arg}[L(j\omega_{0dB})] > 0°$$

where ω_{0dB} is defined as

$$|A(j\omega_{0dB})F(j\omega_{0dB})| = |L(j\omega_{0dB})| = 1$$

Illustration of the Stability Requirement using Bode Plots



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A measure of stability is given by the phase when $|A(j\omega)F(j\omega)| = 1$. This phase is called *phase margin*.

$$\text{Phase margin} = \Phi_M = 360° - \text{Arg}[-A(j\omega_{0dB})F(j\omega_{0dB})] = 360° - \text{Arg}[L(j\omega_{0dB})]$$

Why Do We Want Good Stability?

Consider the step response of second-order system which closely models the closed-loop gain of the op amp connected in unity gain.

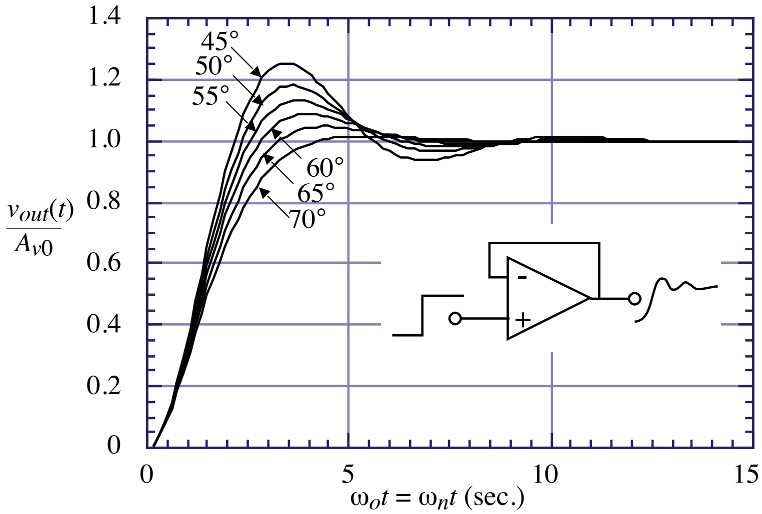


Fig. 120-03

A "good" step response is one that quickly reaches its final value.

Therefore, we see that phase margin should be at least 45° and preferably 60° or larger.

(A rule of thumb for satisfactory stability is that there should be less than three rings.)

Note that good stability is not necessarily the quickest rise time.

Uncompensated Frequency Response of Two-Stage Op Amps

Two-Stage Op Amps:

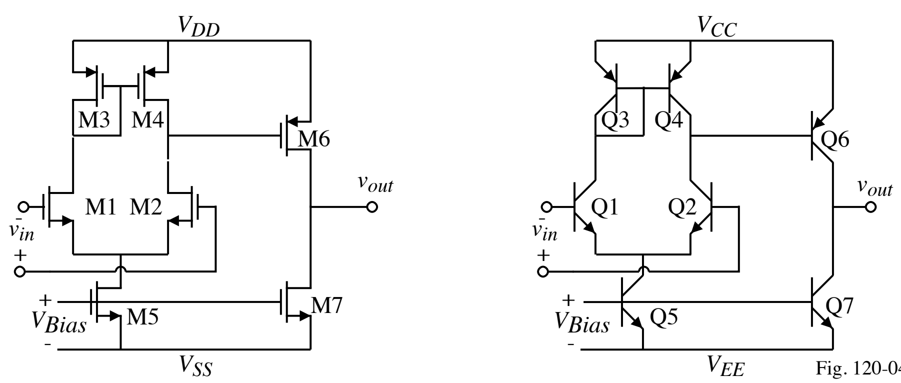


Fig. 120-04

Small-Signal Model:

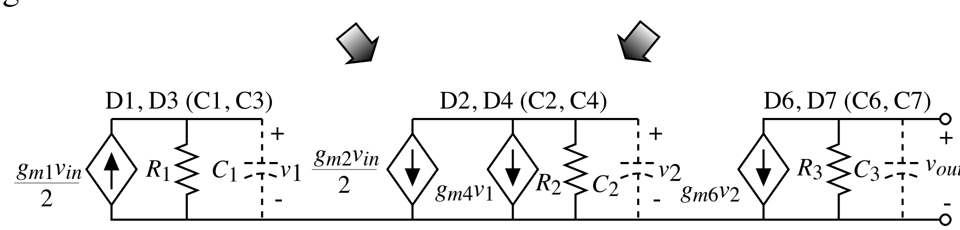


Fig. 120-05

Note that this model neglects the base-collector and gate-drain capacitances for purposes of simplification.

Uncompensated Frequency Response of Two-Stage Op Amps - Continued

For the MOS two-stage op amp:

$$R_1 \approx \frac{1}{g_{m3}} || r_{ds3} || r_{ds1} \approx \frac{1}{g_{m3}} \qquad R_2 = r_{ds2} || r_{ds4} \qquad \text{and} \qquad R_3 = r_{ds6} || r_{ds7}$$

$$C_1 = C_{gs3}+C_{gs4}+C_{bd1}+C_{bd3} \qquad C_2 = C_{gs6}+C_{bd2}+C_{bd4} \qquad \text{and} \quad C_3 = C_L + C_{bd6}+C_{bd7}$$

For the BJT two-stage op amp:

$$R_1 = \frac{1}{g_{m3}} || r_{\pi3} || r_{\pi4} || r_{o1} || r_{o3} \approx \frac{1}{g_{m3}} \quad R_2 = r_{\pi6} || r_{o2} || r_{o4} \approx r_{\pi6} \quad \text{and} \quad R_3 = r_{o6} || r_{o7}$$

$$C_1 = C_{\pi3}+C_{\pi4}+C_{cs1}+C_{cs3} \qquad C_2 = C_{\pi6}+C_{cs2}+C_{cs4} \qquad \text{and} \quad C_3 = C_L+C_{cs6}+C_{cs7}$$

Assuming the pole due to C_1 is much greater than the poles due to C_2 and C_3 gives,

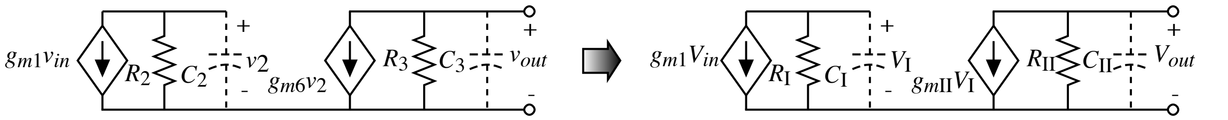


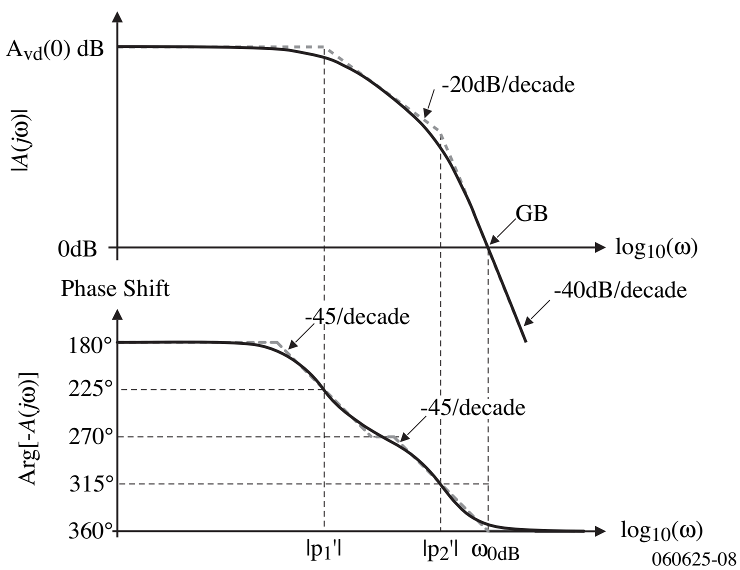
Fig. 120-06

The locations for the two poles are given by the following equations

$$p'_1 = \frac{-1}{R_I C_I} \quad \text{and} \quad p'_2 = \frac{-1}{R_{II} C_{II}}$$

where R_I (R_{II}) is the resistance to ground seen from the output of the first (second) stage and C_I (C_{II}) is the capacitance to ground seen from the output of the first (second) stage.

Uncompensated Frequency Response of an Op Amp ($F(s) = 1$)



If we assume that $F(s) = 1$ (this is the worst case for stability considerations), then the above plot is the same as the loop gain.

Note that the phase margin is much less than 45° (≈ 6°).

Therefore, the op amp must be compensated before using it in a closed-loop configuration.

MILLER COMPENSATION

Miller Compensation of the Two-Stage Op Amp

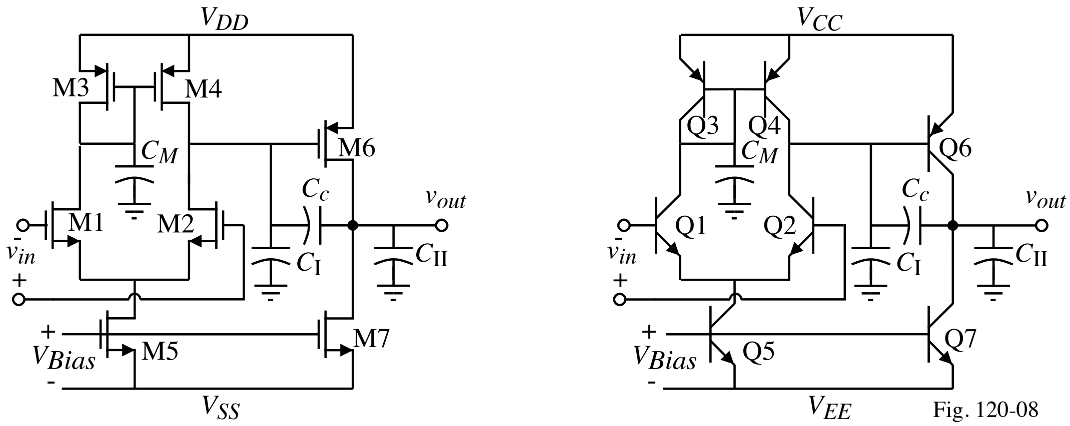


Fig. 120-08

The various capacitors are:

C_c = accomplishes the Miller compensation

C_M = capacitance associated with the first-stage mirror (mirror pole)

C_I = output capacitance to ground of the first-stage

C_{II} = output capacitance to ground of the second-stage

Compensated Two-Stage, Small-Signal Frequency Response Model Simplified

Use the CMOS op amp to illustrate:

1.) Assume that $g_{m3} >> g_{ds3} + g_{ds1}$

2.) Assume that $\frac{g_{m3}}{C_M} >> GB$

Therefore,

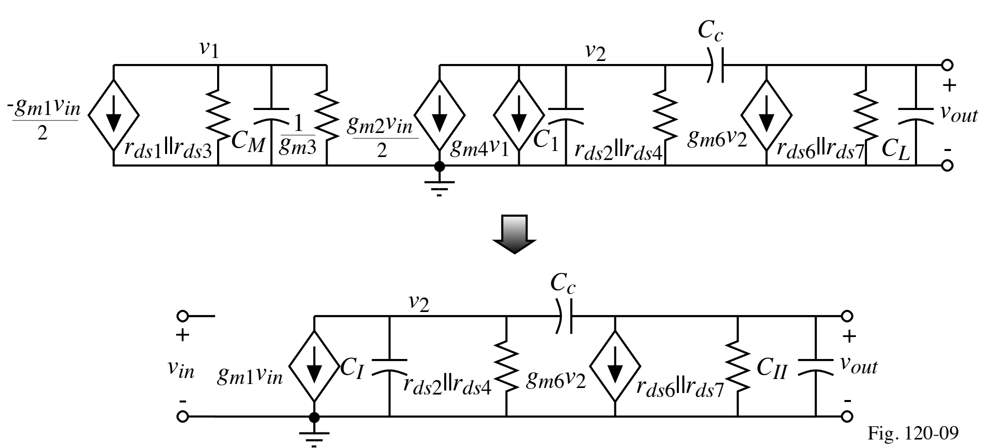


Fig. 120-09

Same circuit holds for the BJT op amp with different component relationships.

General Two-Stage Frequency Response Analysis

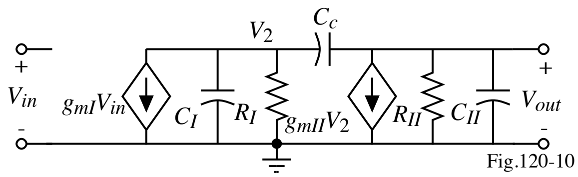


Fig.120-10

where

$$g_{mI} = g_{m1} = g_{m2},\ R_I = r_{ds2}||r_{ds4},\ C_I = C_1$$

and

$$g_{mII} = g_{m6},\ R_{II} = r_{ds6}||r_{ds7},\ C_{II} = C_2 = C_L$$

Nodal Equations:

$$-g_{mI}V_{in} = [G_I + s(C_I + C_c)]V_2 - [sC_c]V_{out} \quad \text{and} \quad 0 = [g_{mII} - sC_c]V_2 + [G_{II} + sC_{II} + sC_c]V_{out}$$

Solving using Cramer's rule gives,

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{g_{mI}(g_{mII} - sC_c)}{G_IG_{II}+s\,[G_{II}(C_I+C_{II})+G_I(C_{II}+C_c)+g_{mII}C_c]+s^2[C_IC_{II}+C_cC_I+C_cC_{II}]}$$

$$= \frac{A_o[1 - s\,(C_c/g_{mII})]}{1+s\,[R_I(C_I+C_{II})+R_{II}(C_2+C_c)+g_{mII}R_1R_{II}C_c]+s^2[R_IR_{II}(C_IC_{II}+C_cC_I+C_cC_{II})]}$$

where, $A_o = g_{mI}g_{mII}R_IR_{II}$

In general, $D(s) = \left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right) = 1-s\left(\frac{1}{p_1}+\frac{1}{p_2}\right)+\frac{s^2}{p_1p_2} \rightarrow D(s) \approx 1-\frac{s}{p_1}+\frac{s^2}{p_1p_2}$, if $|p_2|>>|p_1|$

$$\therefore \quad \boxed{p_1 = \frac{-1}{R_I(C_I+C_{II})+R_{II}(C_{II}+C_c)+g_{mII}R_1R_{II}C_c} \approx \frac{-1}{g_{mII}R_1R_{II}C_c}},\ \boxed{z = \frac{g_{mII}}{C_c}}$$

$$\boxed{p_2 = \frac{-[R_I(C_I+C_{II})+R_{II}(C_{II}+C_c)+g_{mII}R_1R_{II}C_c]}{R_IR_{II}(C_IC_{II}+C_cC_I+C_cC_{II})} \approx \frac{-g_{mII}C_c}{C_IC_{II}+C_cC_I+C_cC_{II}} \approx \frac{-g_{mII}}{C_{II}}},\ C_{II} > C_c > C_I$$

Summary of Results for Miller Compensation of the Two-Stage Op Amp

There are three roots of importance:

1.) Right-half plane zero:

$$z_1 = \frac{g_{mII}}{C_c} = \frac{g_{m6}}{C_c}$$

This root is very undesirable- it boosts the magnitude while decreasing the phase.

2.) Dominant left-half plane pole (the Miller pole):

$$p_1 \approx \frac{-1}{g_{mII}R_IR_{II}C_c} = \frac{-(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})}{g_{m6}C_c}$$

This root accomplishes the desired compensation.

3.) Left-half plane output pole:

$$p_2 \approx \frac{-g_{mII}}{C_{II}} \approx \frac{-g_{m6}}{C_L}$$

p_2 must be ≥ unity-gainbandwidth or satisfactory phase margin will not be achieved.

Root locus plot of the Miller compensation:

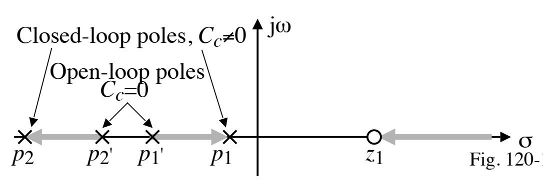
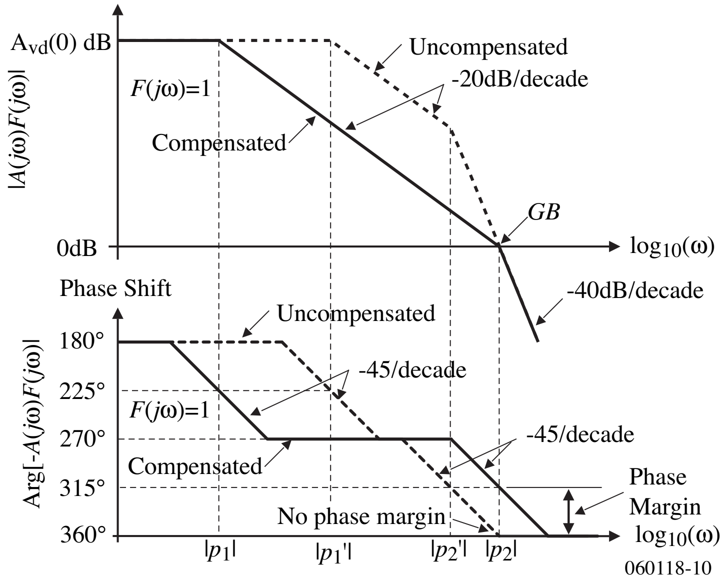


Fig. 120-11

Compensated Open-Loop Frequency Response of the Two-Stage Op Amp



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Note that the unity-gainbandwidth, GB, is

$$GB = A_{vd}(0)\cdot|p_1| = (g_{mI}g_{mII}R_IR_{II})\frac{1}{g_{mII}R_IR_{II}C_c} = \frac{g_{mI}}{C_c} = \frac{g_{m1}}{C_c} = \frac{g_{m2}}{C_c}$$

Conceptually, where do these roots come from?

1.) The Miller pole:

$$|p_1| \approx \frac{1}{R_I(g_{m6}R_{II}C_c)}$$

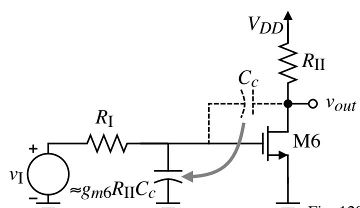


Fig. 120-13

2.) The left-half plane output pole:

$$|p_2| \approx \frac{g_{m6}}{C_{II}}$$

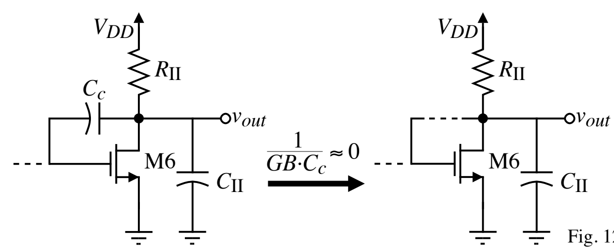


Fig. 120-14

3.) Right-half plane zero (*One source of zeros is from multiple paths from the input to output*):

$$v_{out} = \left(\frac{-g_{m6}R_{II}(1/sC_c)}{R_{II} + 1/sC_c}\right) v' + \left(\frac{R_{II}}{R_{II} + 1/sC_c}\right) v'' = \frac{-R_{II}\left(\frac{g_{m6}}{sC_c} - 1\right)}{R_{II} + 1/sC_c}\, v$$

where $v = v' = v''$.

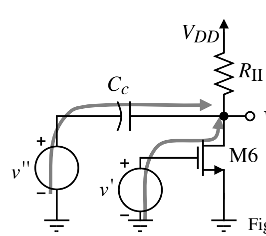
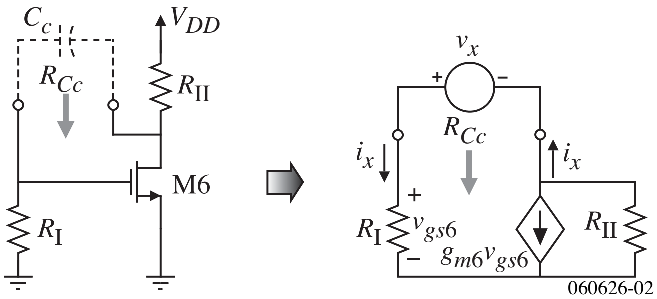


Fig. 120-15

Further Comments on p_2

The previous observations on p_2 can be proved as follows:

Find the resistance R_{Cc} seen by the compensation capacitor, C_c.



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$$v_x = i_xR_I + (i_x + g_{m6}v_{gs6})R_{II} = i_xR_I + (i_x + g_{m6}i_xR_I)R_{II}$$

Therefore,

$$R_{Cc} = \frac{v_x}{i_x} = R_I + (1 + g_{m6}R_I)R_{II} \approx g_{m6}R_IR_{II}$$

The frequency at which C_c begins to become a short is,

$$\frac{1}{\omega C_c} < g_{m6}R_IR_{II} \qquad \text{or} \qquad \omega > \frac{1}{g_{m6}R_IR_{II}\,C_c} \approx |p_1|$$

Thus, at the frequency where C_{II} begins to short the output, C_c is acting as a short.

Influence of the Mirror Pole

Up to this point, we have neglected the influence of the pole, p_3, associated with the current mirror of the input stage. A small-signal model for the input stage that includes C_3 is shown below:

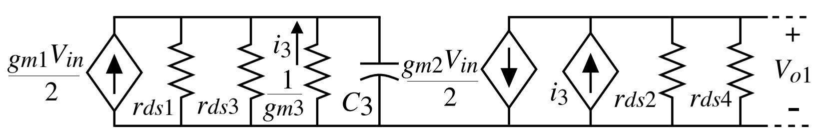

Fig. 120-16

The transfer function from the input to the output voltage of the first stage, $V_{o1}(s)$, can be written as

$$\frac{V_{o1}(s)}{V_{in}(s)} = \frac{-g_{m1}}{2(g_{ds2}+g_{ds4})}\left[\frac{g_{m3}+g_{ds1}+g_{ds3}}{g_{m3}+g_{ds1}+g_{ds3}+sC_3}+1\right] \approx \frac{-g_{m1}}{2(g_{ds2}+g_{ds4})}\left[\frac{sC_3+2g_{m3}}{sC_3+g_{m3}}\right]$$

We see that there is a pole and a zero given as

$$p_3 = -\frac{g_{m3}}{C_3} \quad \text{and} \quad z_3 = -\frac{2g_{m3}}{C_3}$$

Summary of the Conditions for Stability of the Two-Stage Op Amp

• Unity-gainbandwith is given as:

$$GB = A_v(0)\cdot|p_1| = (g_{mI}g_{mII}R_IR_{II})\cdot\left(\frac{1}{g_{mII}R_IR_{II}C_c}\right) = \frac{g_{mI}}{C_c} = (g_{m1}g_{m2}R_1R_2)\cdot\left(\frac{1}{g_{m2}R_1R_2C_c}\right) = \frac{g_{m1}}{C_c}$$

• The requirement for 45° phase margin is:

$$\pm180° - \text{Arg[Loop Gain]} = \pm180° - \tan^{-1}\left(\frac{\omega}{|p_1|}\right) - \tan^{-1}\left(\frac{\omega}{|p_2|}\right) - \tan^{-1}\left(\frac{\omega}{z}\right) = 45°$$

Let $\omega = GB$ and assume that $z \geq 10GB$, therefore we get,

$$\pm180° - \tan^{-1}\left(\frac{GB}{|p_1|}\right) - \tan^{-1}\left(\frac{GB}{|p_2|}\right) - \tan^{-1}\left(\frac{GB}{z}\right) = 45°$$

$$135° \approx \tan^{-1}(A_v(0)) + \tan^{-1}\left(\frac{GB}{|p_2|}\right) + \tan^{-1}(0.1) = 90° + \tan^{-1}\left(\frac{GB}{|p_2|}\right) + 5.7°$$

$$39.3° \approx \tan^{-1}\left(\frac{GB}{|p_2|}\right) \Rightarrow \frac{GB}{|p_2|} = 0.818 \Rightarrow \boxed{|p_2| \geq 1.22GB}$$

• The requirement for 60° phase margin:

$$\boxed{|p_2| \geq 2.2GB \text{ if } z \geq 10GB}$$

• If 60° phase margin is required, then the following relationships apply:

$$\frac{g_{m6}}{C_c} > \frac{10g_{m1}}{C_c} \quad\Rightarrow\quad \boxed{g_{m6} > 10g_{m1}} \qquad \text{and} \quad \frac{g_{m6}}{C_2} > \frac{2.2g_{m1}}{C_c} \quad\Rightarrow\quad \boxed{C_c > 0.22C_2}$$

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OTHER FORMS OF COMPENSATION

Feedforward Compensation

Use two parallel paths to achieve a LHP zero for lead compensation purposes.

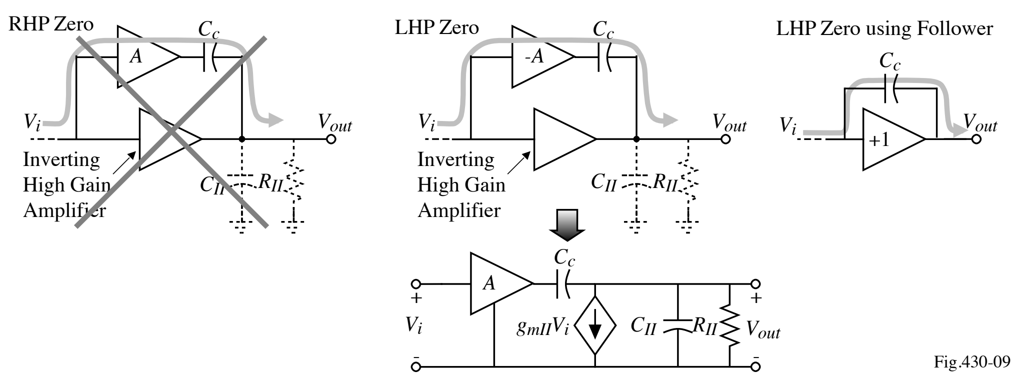

Fig.430-09

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{AC_c}{C_c + C_{II}}\left(\frac{s + g_{mII}/AC_c}{s + 1/[R_{II}(C_c + C_{II})]}\right)$$

To use the LHP zero for compensation, a compromise must be observed.

• Placing the zero below GB will lead to boosting of the loop gain that could deteriorate the phase margin.

• Placing the zero above GB will have less influence on the leading phase caused by the zero.

Note that a source follower is a good candidate for the use of feedforward compensation.

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Self-Compensated Op Amps

Self compensation occurs when the load capacitor is the compensation capacitor (can never be unstable for resistive feedback)

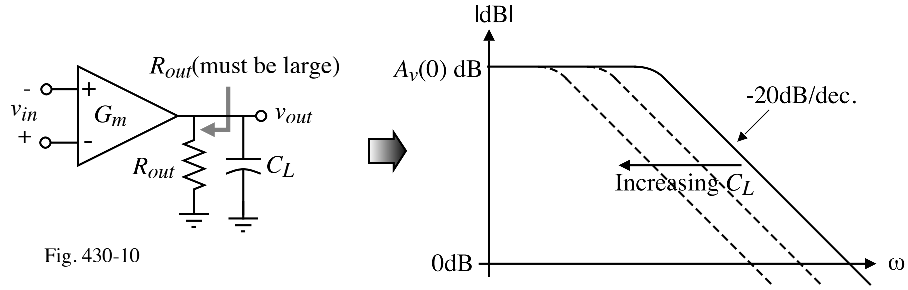


Fig. 430-10

Voltage gain:

$$\frac{v_{out}}{v_{in}} = A_v(0) = G_m R_{out}$$

Dominant pole:

$$p_1 = \frac{-1}{R_{out}C_L}$$

Unity-gainbandwidth:

$$GB = A_v(0)\cdot|p_1| = \frac{G_m}{C_L}$$

Stability:

Large load capacitors simply reduce *GB* but the phase is still 90° at *GB*.

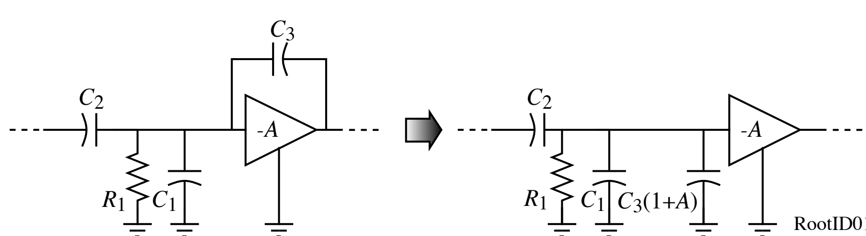
FINDING ROOTS BY INSPECTION

Identification of Poles from a Schematic

1.) Most poles are equal to the reciprocal product of the resistance from a node to ground and the capacitance connected to that node.

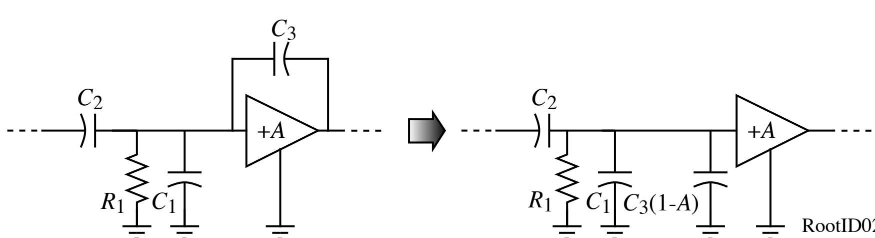
2.) Exceptions (generally due to feedback):

a.) Negative feedback:



RootID01

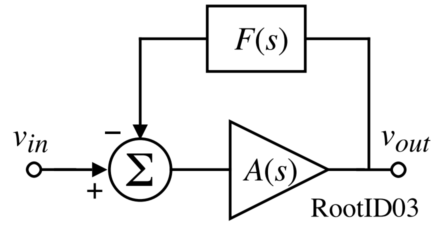
b.) Positive feedback (A<1):



RootID02

Identification of Zeros from a Schematic

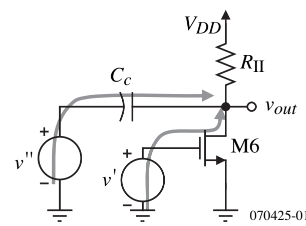
1.) Zeros arise from poles in the feedback path.



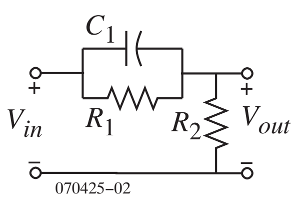
If $F(s) = \dfrac{1}{\dfrac{s}{p_1}+1}$,

then $\dfrac{V_{out}}{V_{in}} = \dfrac{A(s)}{1+A(s)F(s)} = \dfrac{A(s)}{1+A(s)\dfrac{1}{\dfrac{s}{p_1}+1}} = \dfrac{A(s)\left(\dfrac{s}{p_1}+1\right)}{\dfrac{s}{p_1}+1+A(s)}$

2.) Zeros are also created by two paths from the input to the output and one of more of the paths is frequency dependent.



3.) Zeros also come from simple RC networks.



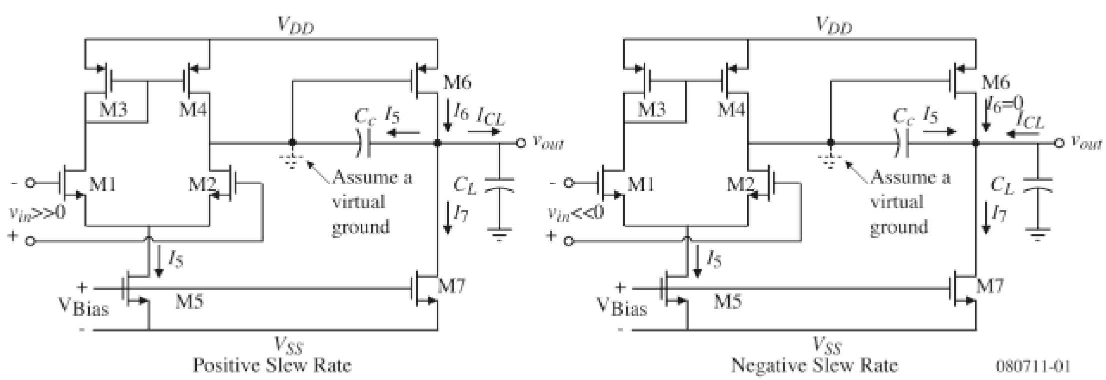
$$\frac{V_{out}}{V_{in}} = \frac{s + 1/(R_1C_1)}{s + 1/(R_1 \| R_2)C_1}$$

CMOS OP AMP SLEW RATE

Slew Rate of a Two-Stage CMOS Op Amp

Remember that slew rate occurs when currents flowing in a capacitor become limited and is given as

$$I_{lim} = C\frac{dv_C}{dt} \quad \text{where } v_C \text{ is the voltage across the capacitor } C.$$



$$SR^+ = \min\left[\frac{I_5}{C_c}, \frac{I_6\text{-}I_5\text{-}I_7}{C_L}\right] = \frac{I_5}{C_c} \text{ because } I_6 >> I_5 \qquad SR^- = \min\left[\frac{I_5}{C_c}, \frac{I_7\text{-}I_5}{C_L}\right] = \frac{I_5}{C_c} \text{ if } I_7 >> I_5.$$

Therefore, if C_L is not too large and if I_7 is significantly greater than I_5, then the slew rate of the two-stage op amp should be, I_5/C_c.

SUMMARY

- Op amps achieve accuracy by using negative feedback
- Compensation is required to insure that the feedback loop is stable
- The degree of stability is measured by phase margin and is necessary to achieve small settling times
- A compensated op amp will have one dominant pole and all other poles will be greater than *GB*
- A two-stage op amp requires some form of Miller compensation
- A high output resistance op amp is compensated by the load capacitor
- Poles of a CMOS circuit are generally equal to the negative reciprocal of the product of the resistance to ground from a node times the sum of the capacitances connected to that node.
- The slew rate of the two-stage op amp is equal to the input differential stage current sink/source divided by the Miller capacitor

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