Circuitos CMOS No Lineales

86.46 Microelectrónica
66.61 Tecnología de Circuitos Integrados
FIUBA

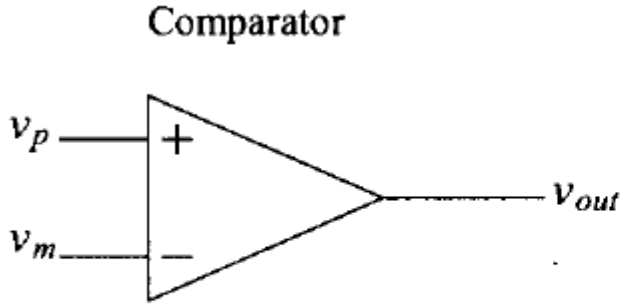
- Comparador
- Schmitt Trigger
- Osciladores
- PLL Digital
- Charge Pump

Presentación Basada en el texto:

R.J. Baker - CMOS Circuit Design, Layout and Simulation
3rd Edition, Wiley – IEEE Press

Comparador

- Operación básica



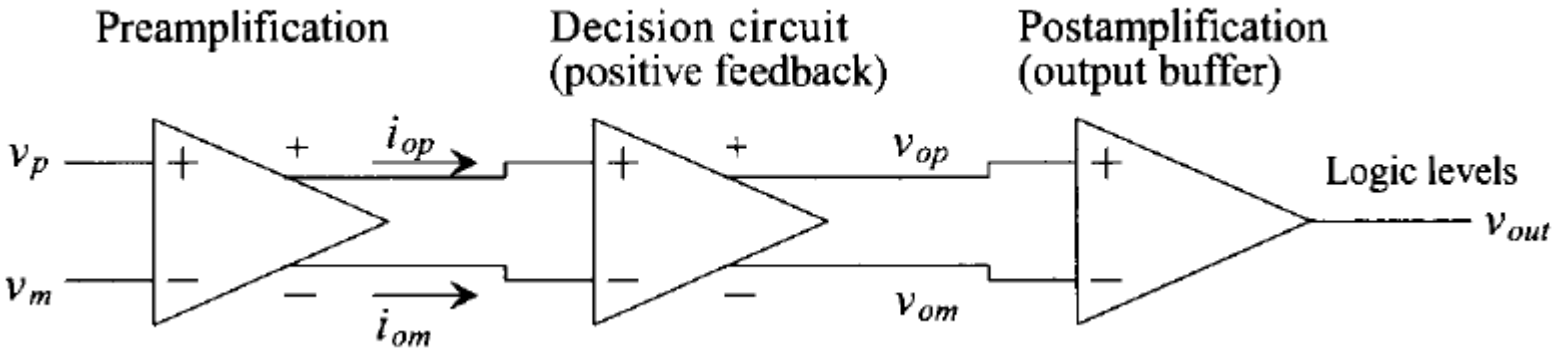
$v_p > v_m$ then $v_{out} = VDD$ = logic 1

$v_p < v_m$ then $v_{out} = 0$ = logic 0

- Características principales:
  - Velocidad
  - Ganancia

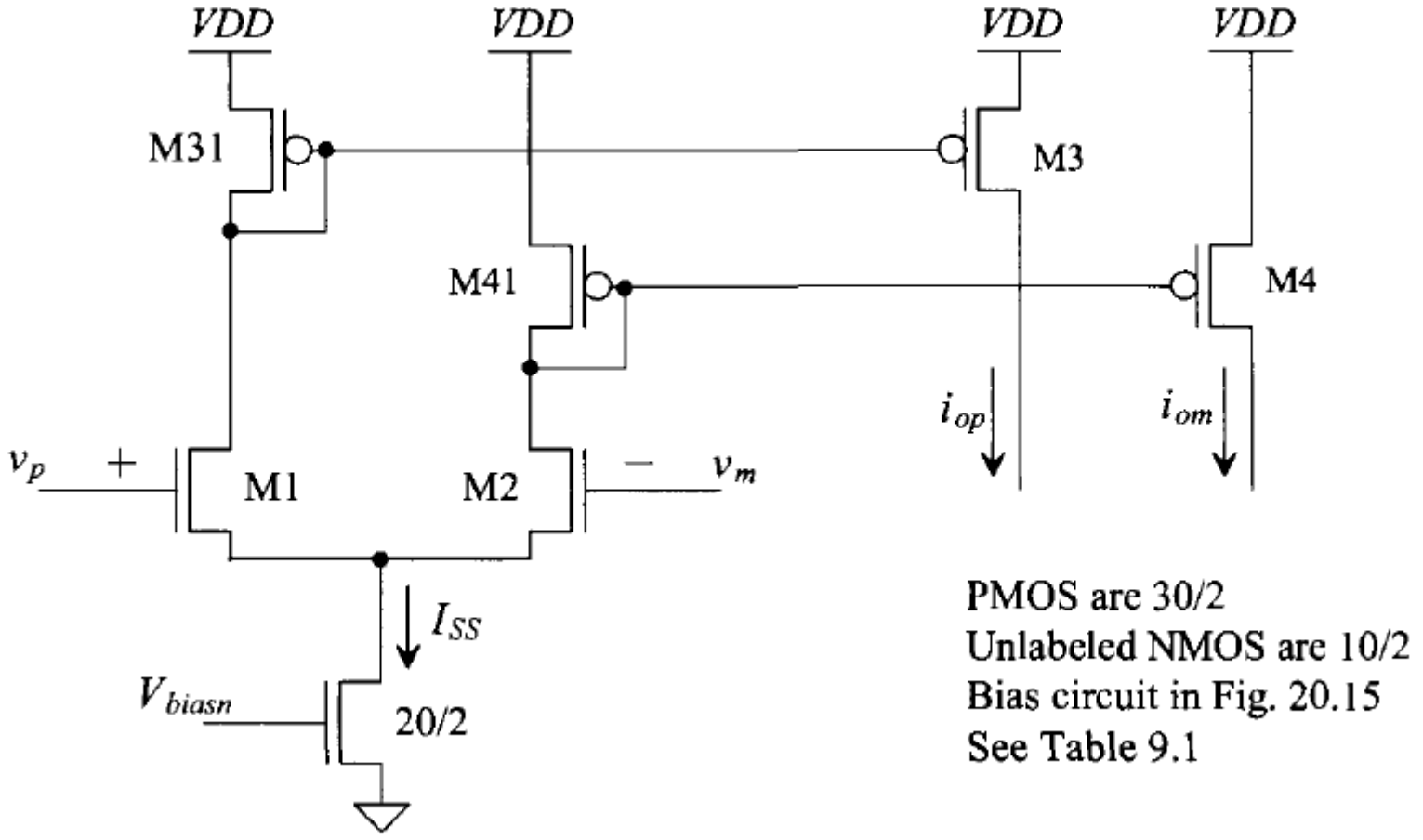
Comparador

- Diagrama en bloques



Comparador

- Preamp

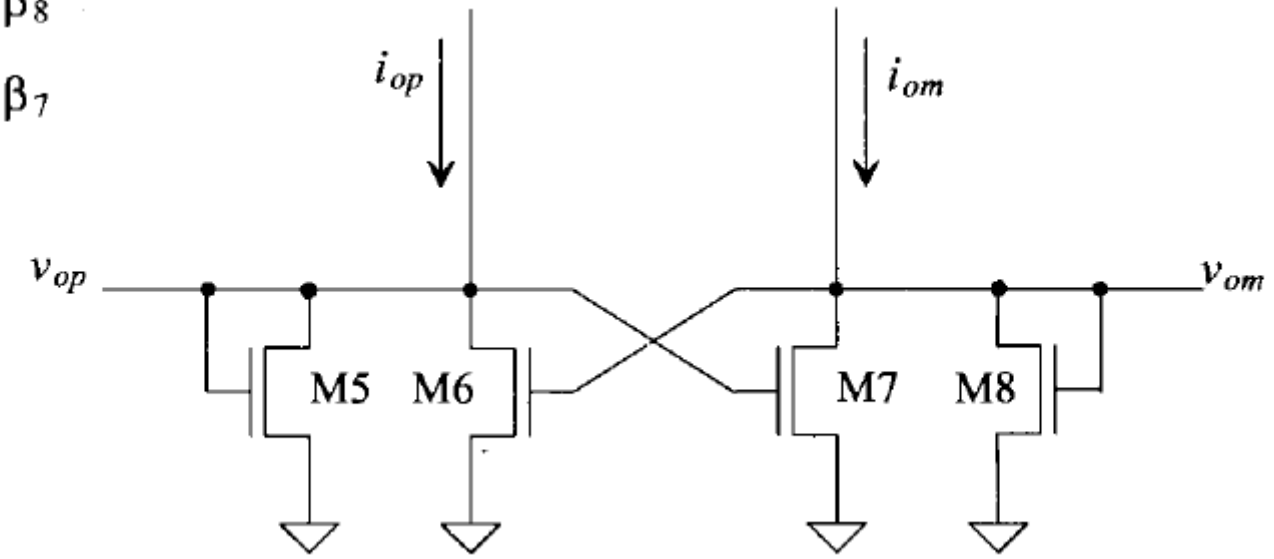


Comparador

- Etapa de decisión: con realimentación positiva

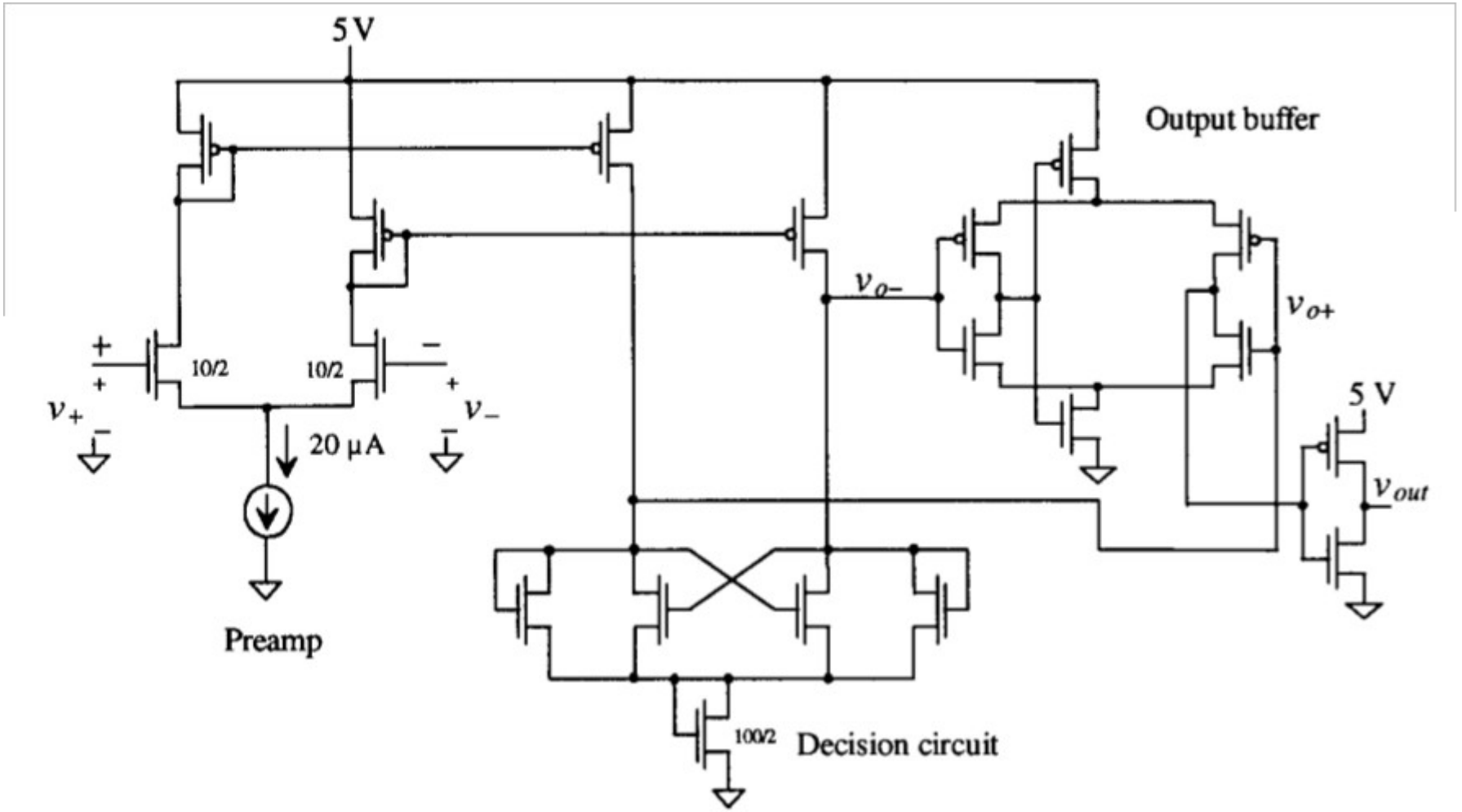
$\beta_A = \beta_5 = \beta_8$

$\beta_B = \beta_6 = \beta_7$



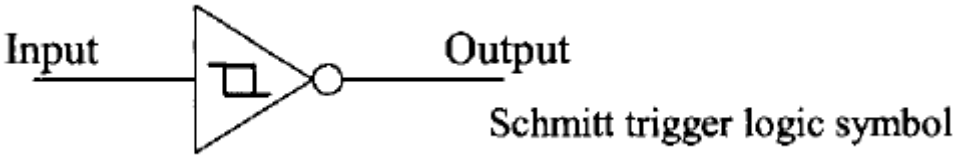
Comparador

- Esquemático completo

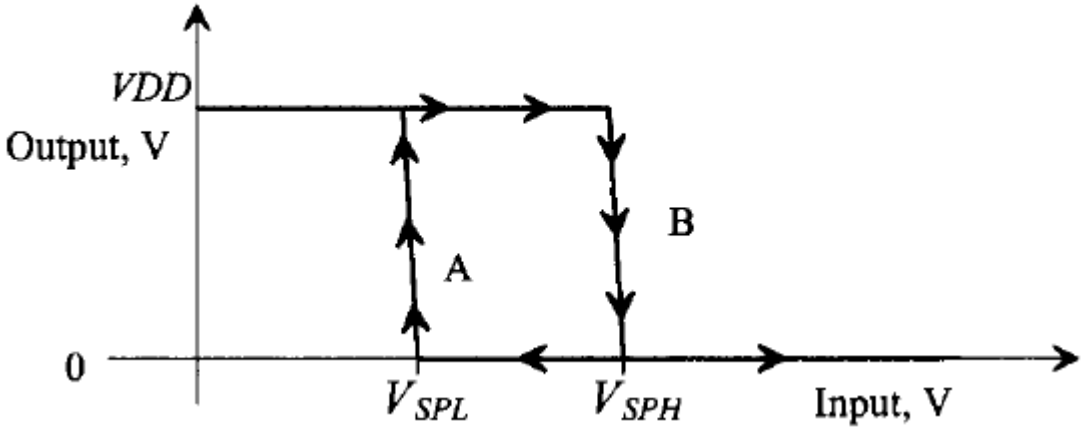


Schmitt Trigger

- Transferencia

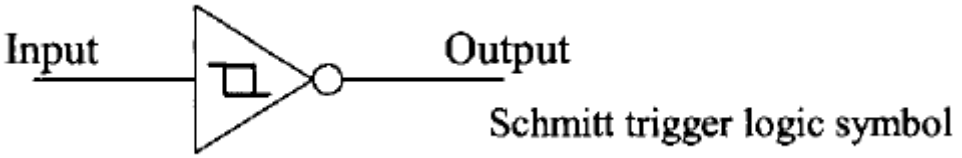


Schmitt trigger logic symbol

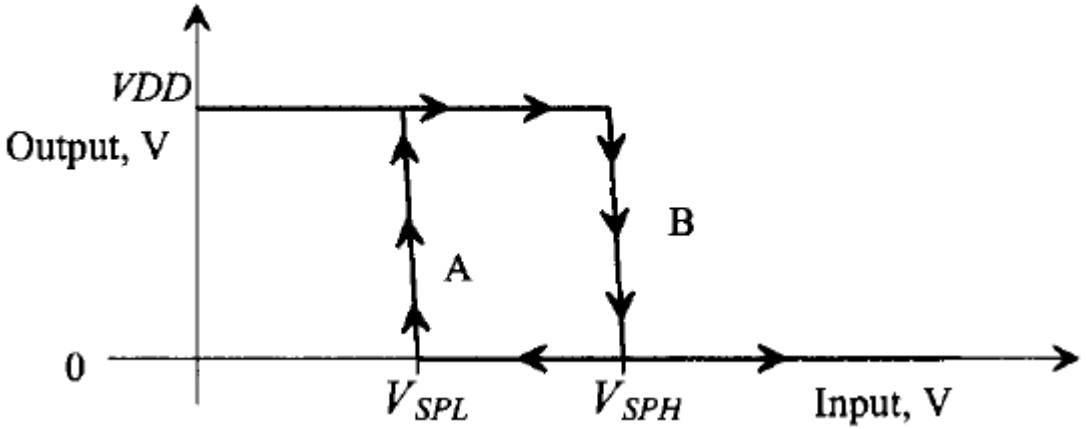


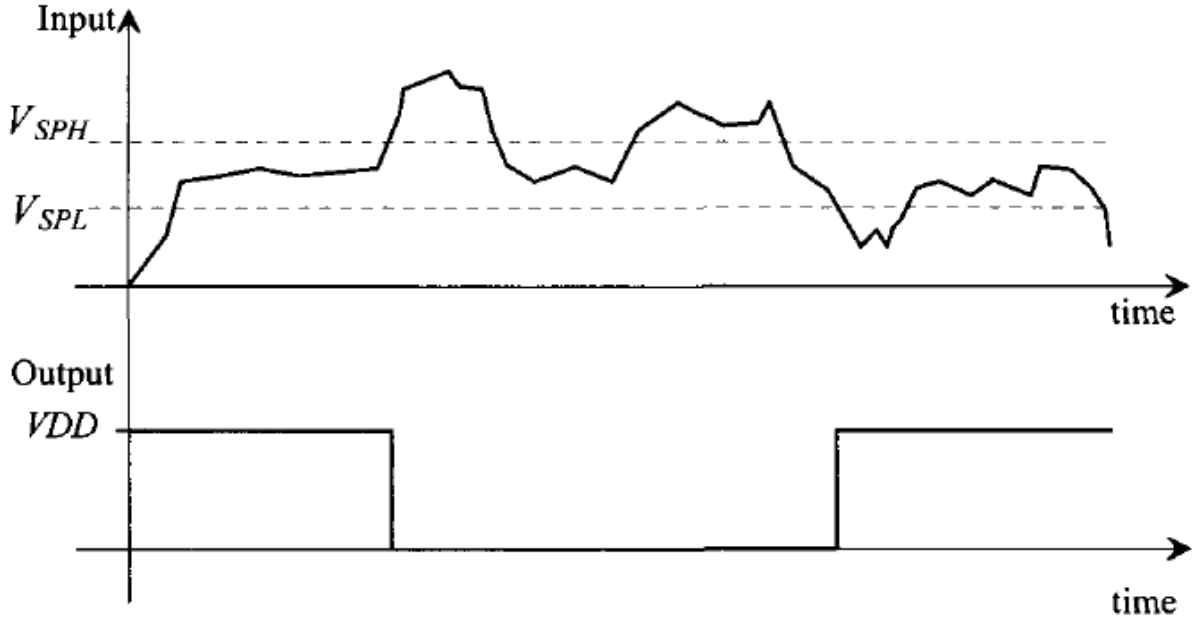
Schmitt Trigger

- Transferencia



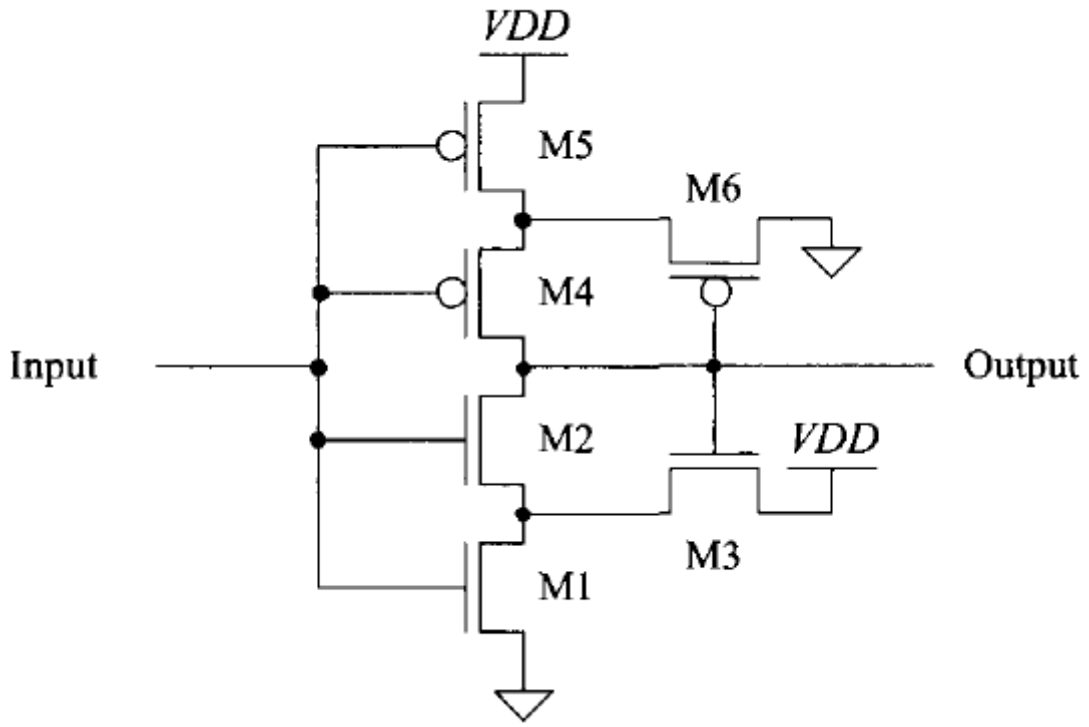
Schmitt trigger logic symbol





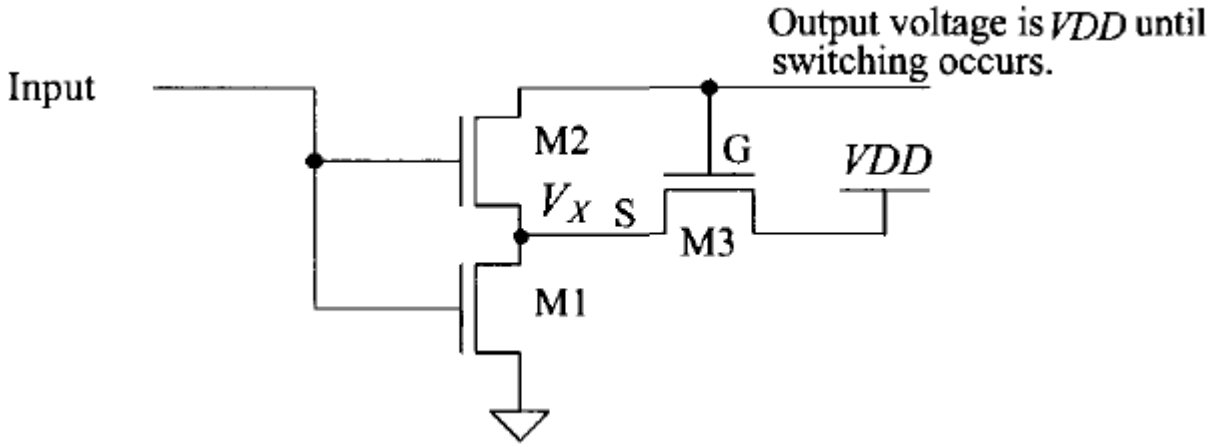
Schmitt Trigger

- Esquemático



Schmitt Trigger

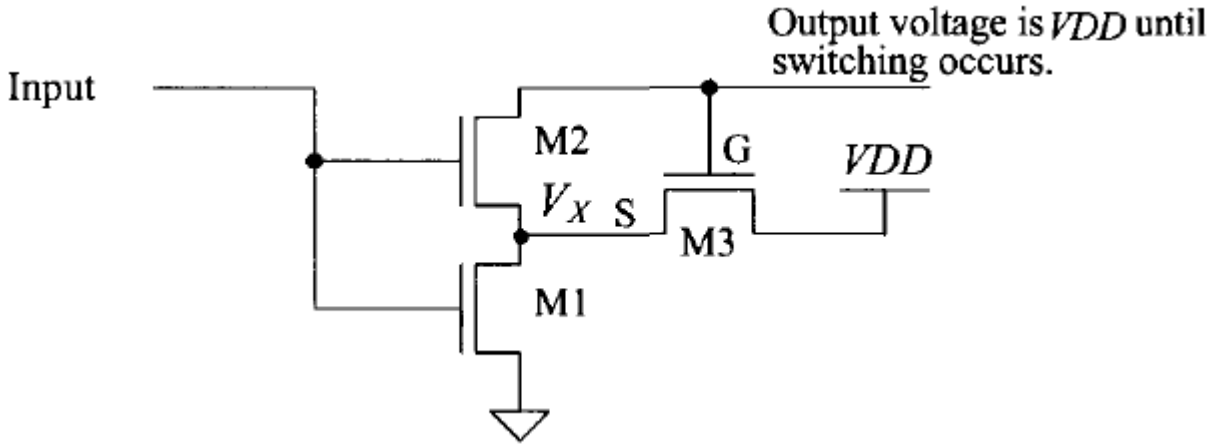
- Umbral de conmutación



$$V_{in} = V_{SPH} = V_{THN2} + V_X$$

Schmitt Trigger

- Umbral de conmutación

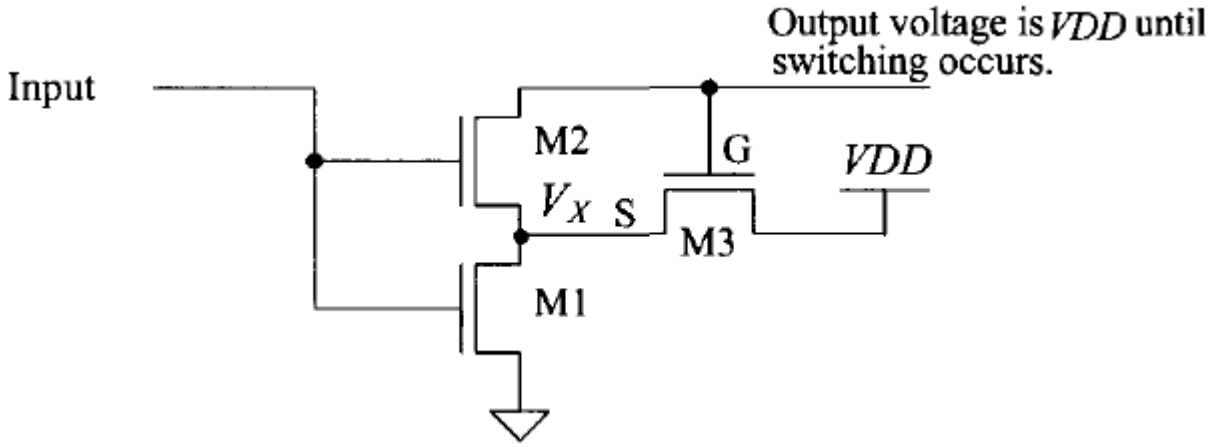


$$V_{in} = V_{SPH} = V_{THN2} + V_X$$

$$\frac{\beta_1}{2}(V_{SPH} - V_{THN})^2 = \frac{\beta_3}{2}(VDD - V_X - V_{THN3})^2$$

Schmitt Trigger

- Umbral de conmutación



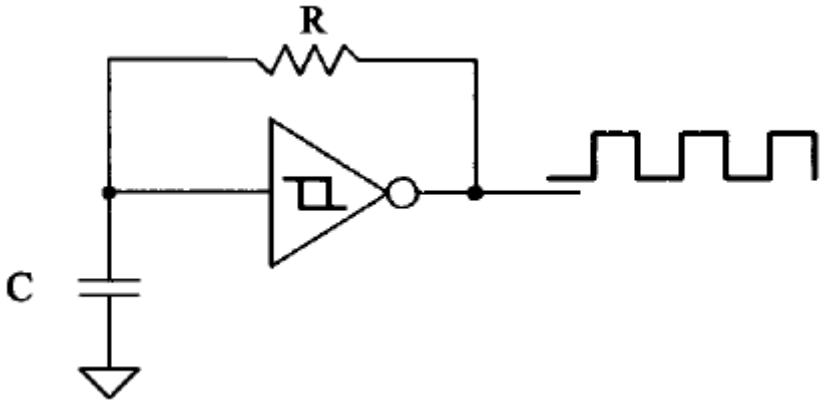
$$V_{in} = V_{SPH} = V_{THN2} + V_X$$

$$\frac{\beta_1}{2}(V_{SPH} - V_{THN})^2 = \frac{\beta_3}{2}(VDD - V_X - V_{THN3})^2$$

$$\frac{\beta_1}{\beta_3} = \frac{W_1 L_3}{L_1 W_3} = \left[\frac{VDD - V_{SPH}}{V_{SPH} - V_{THN}}\right]^2$$

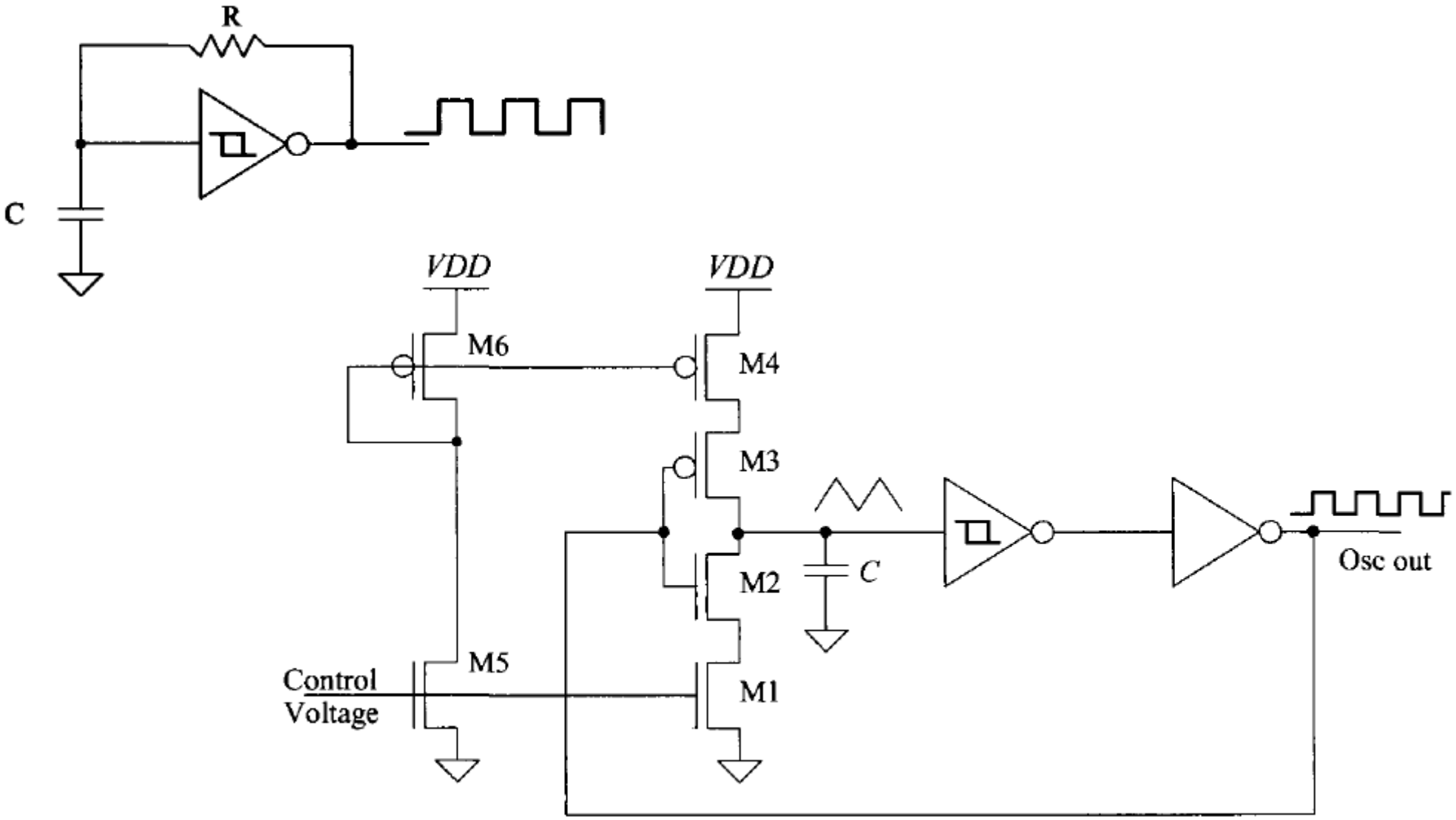
Schmitt Trigger

- Osciladores basados en ST

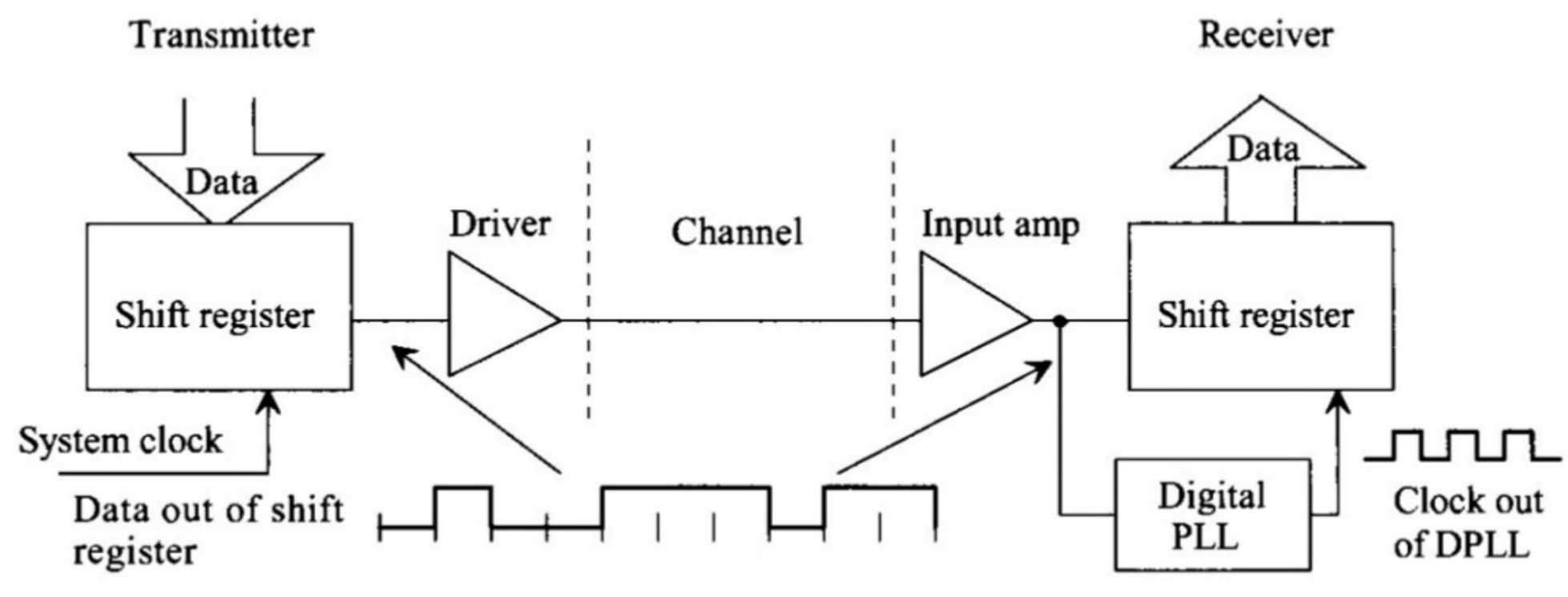


Schmitt Trigger

- Osciladores basados en ST

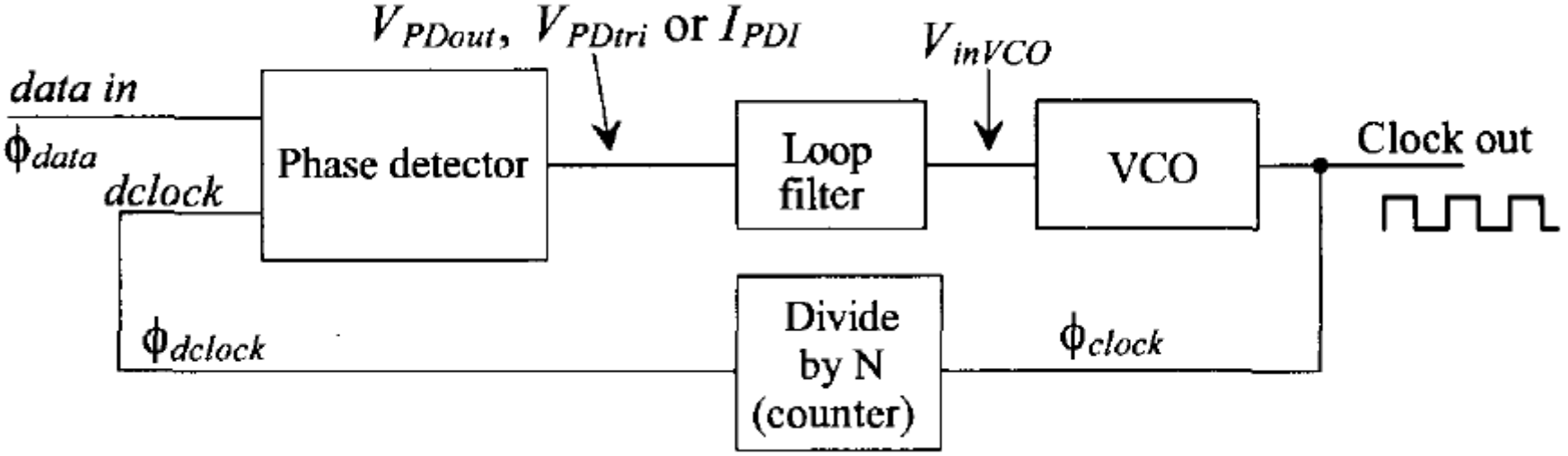


Digital Phase-Locked Loop (DPLL)



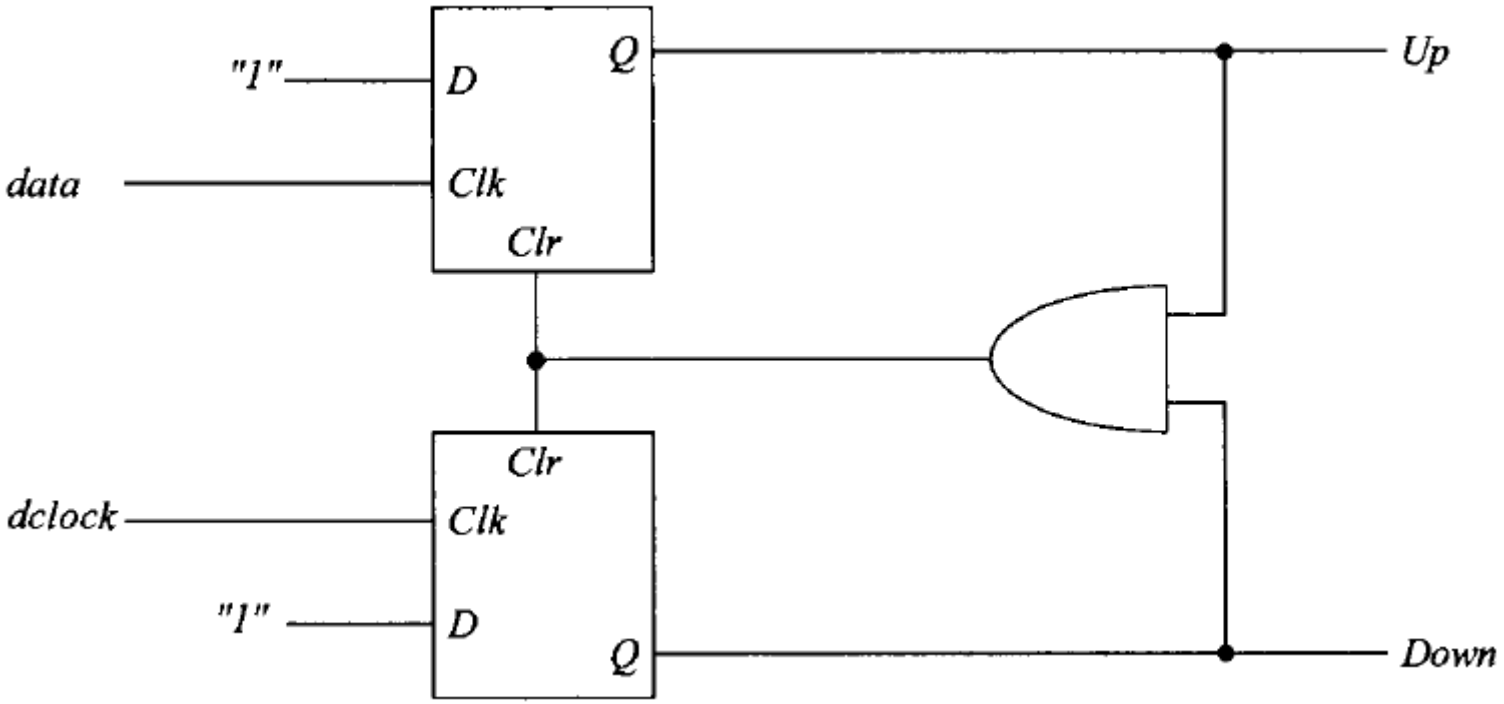
PLL Digital

- Diagrama en bloques

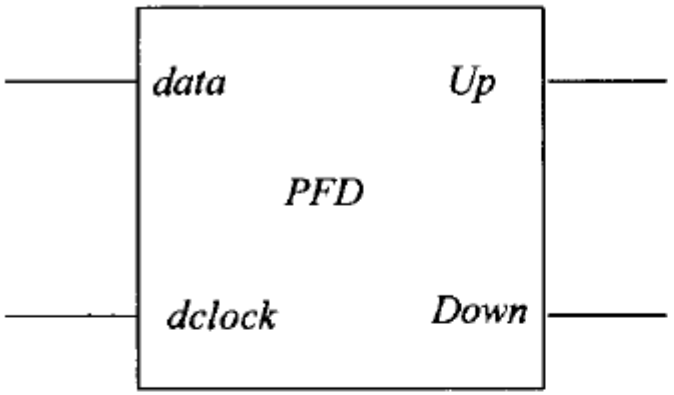


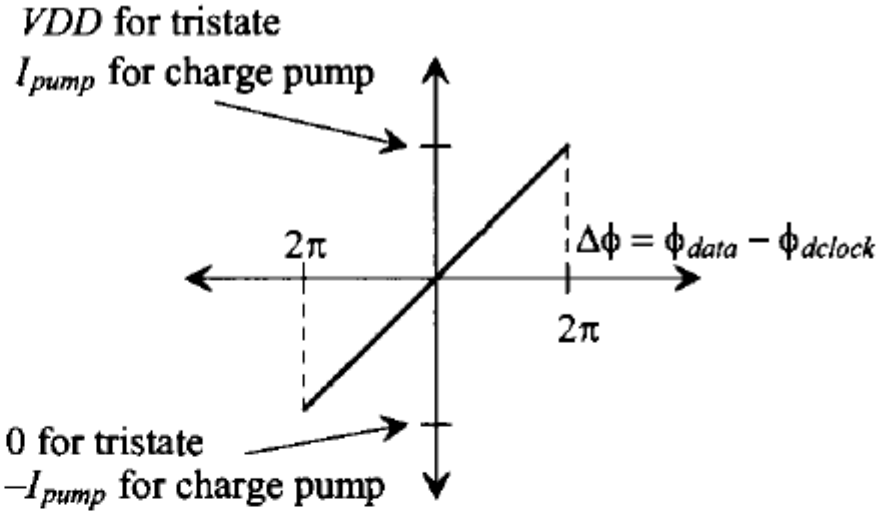
PLL Digital - PFD

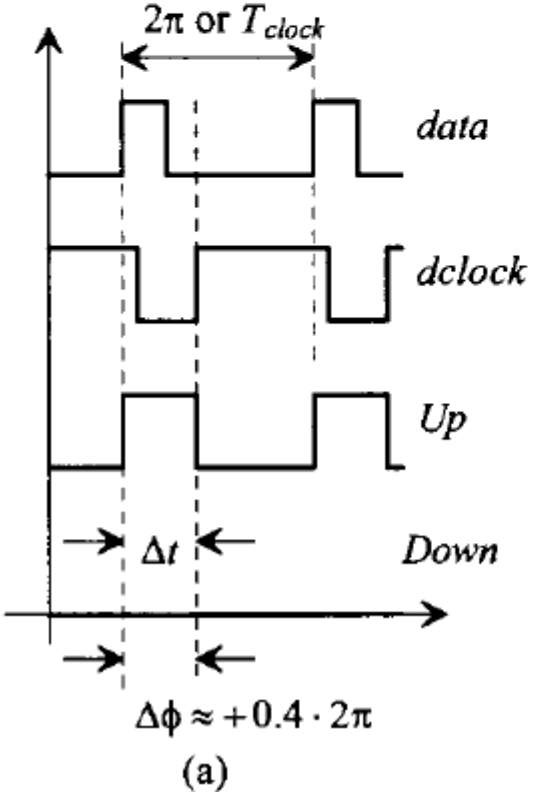
- Phase Frecuency Detector (PFD)

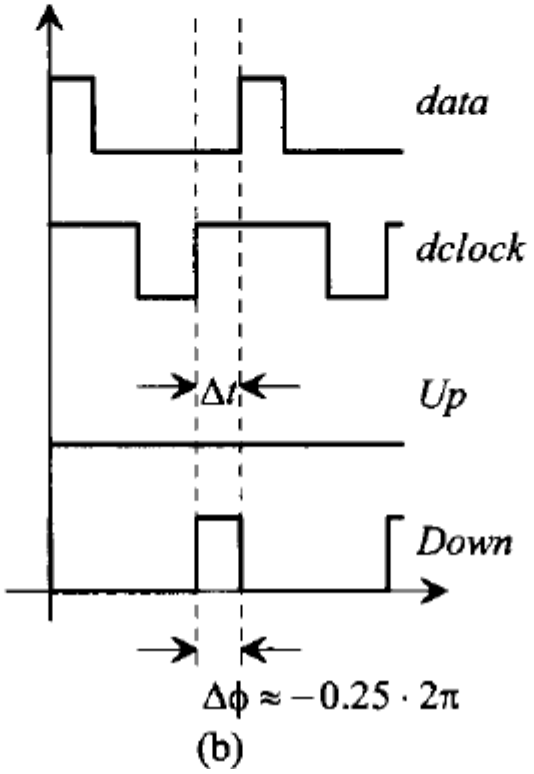


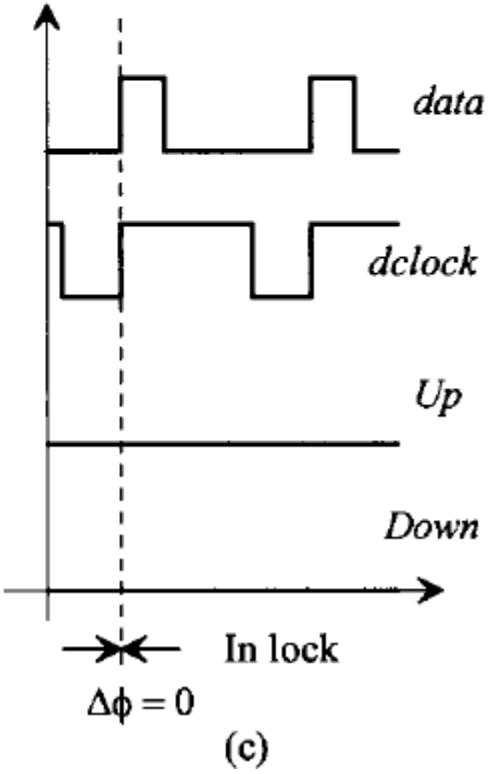
PLL Digital - PFD





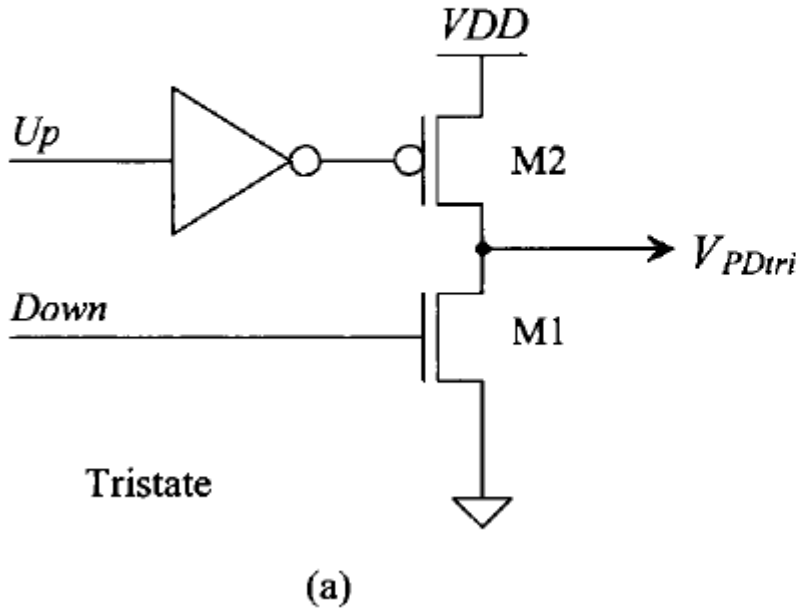


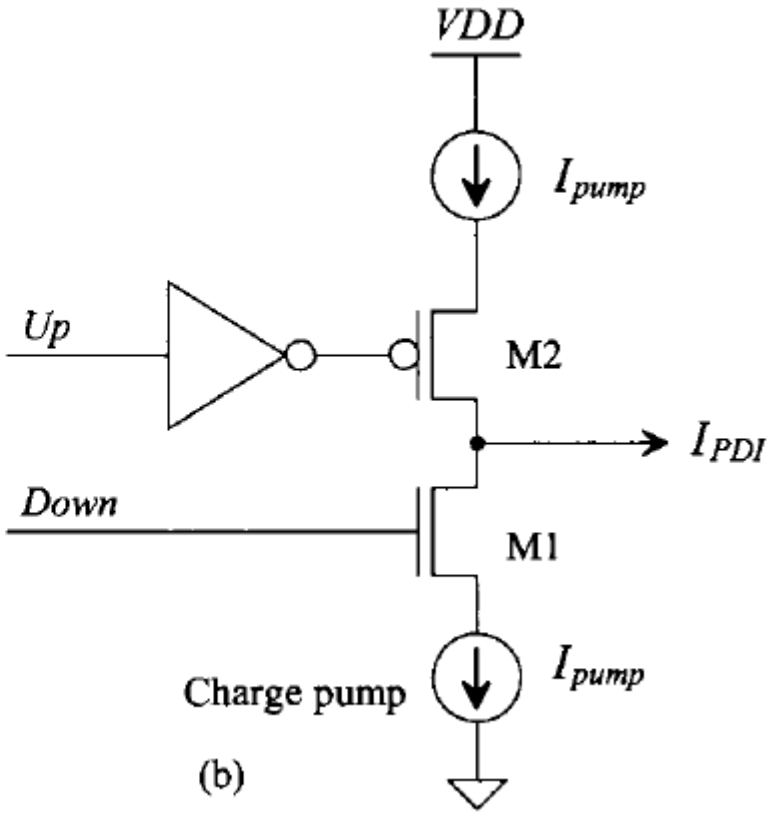




PLL Digital -PFD

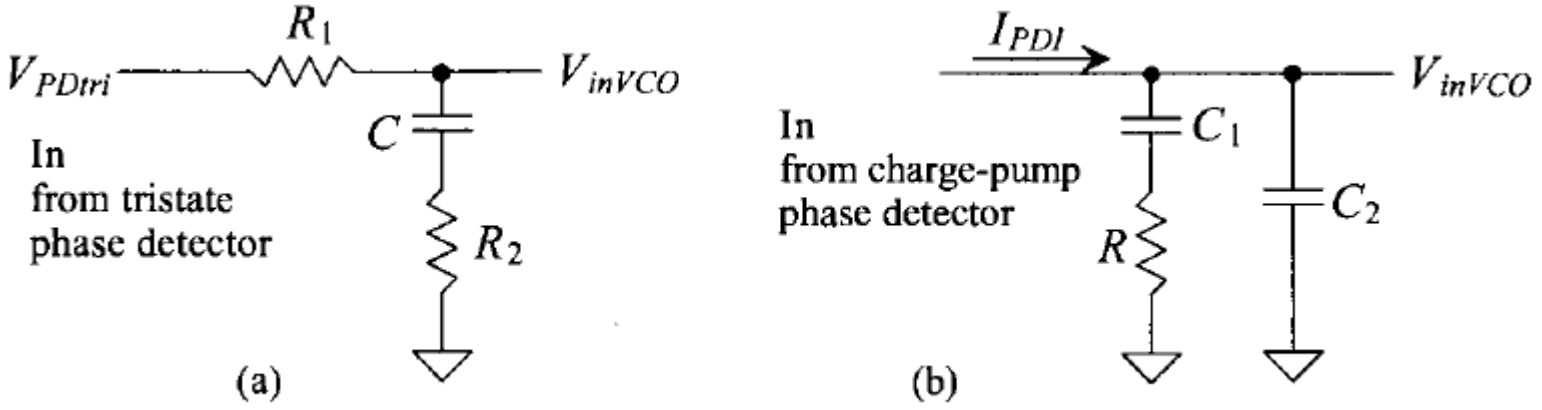
- PFD output buffer





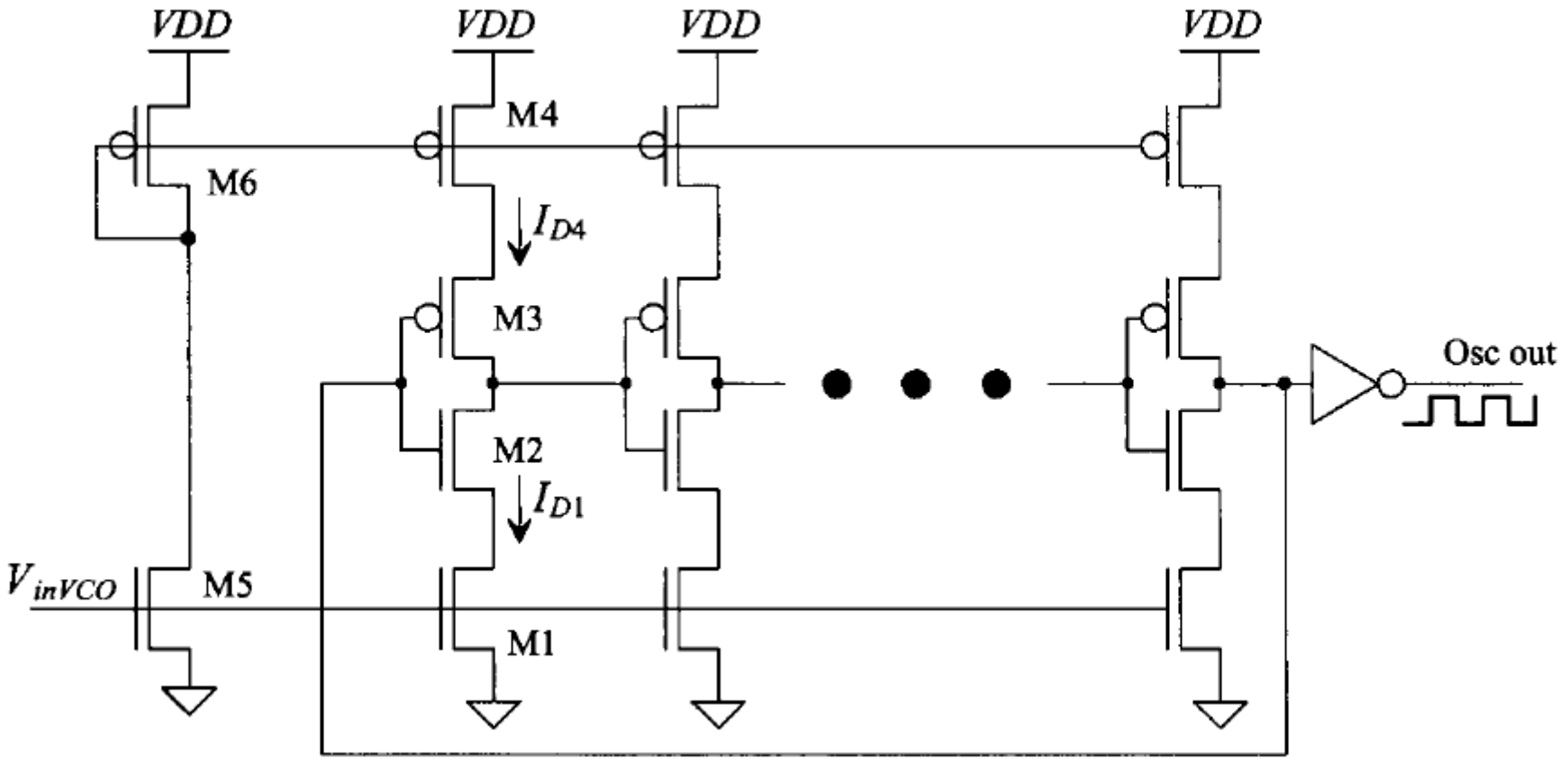
PLL Digital - PFD

- PFD loop filter



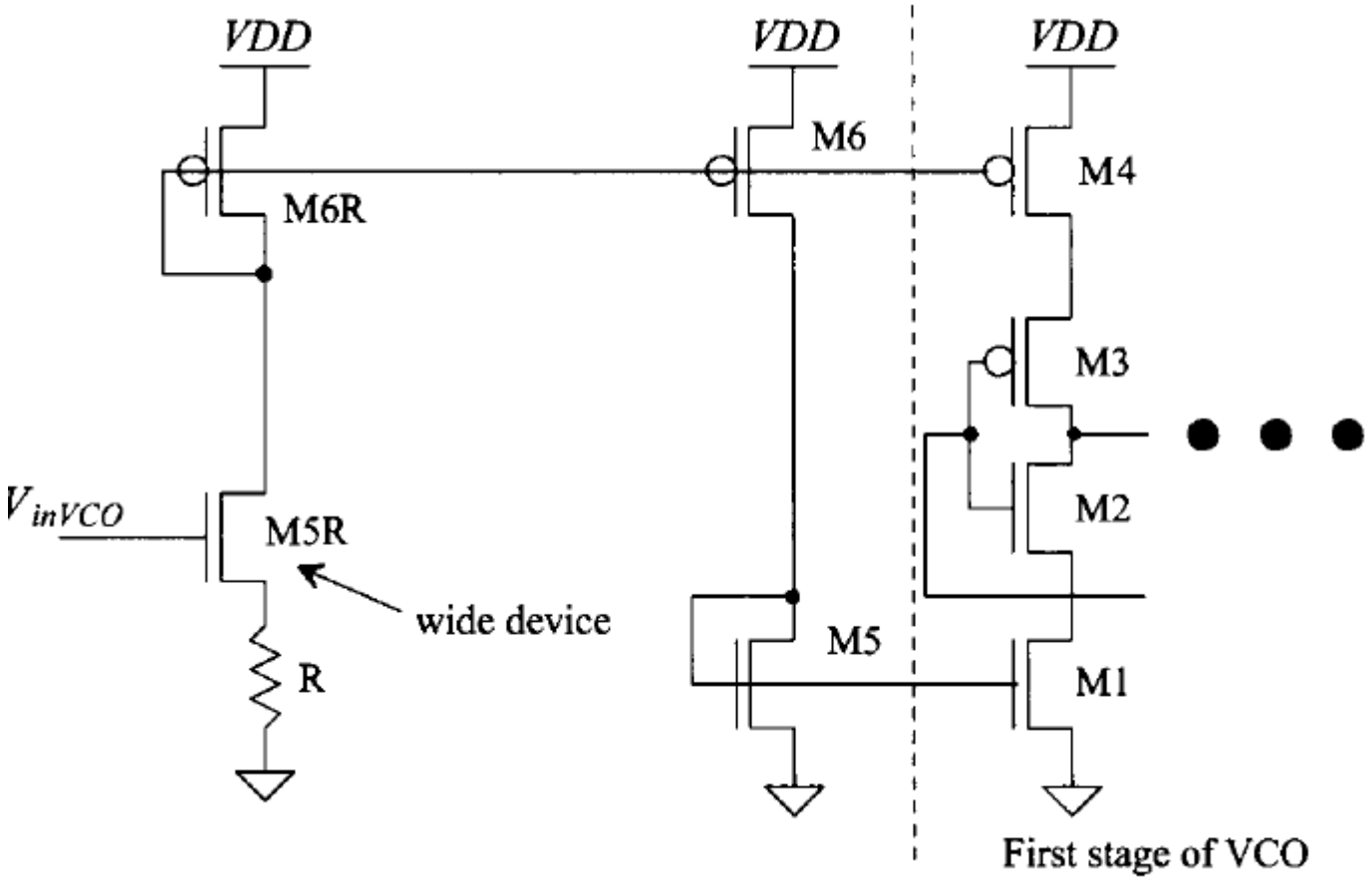
PLL Digital – VCO RO

- Voltage controlled oscilator (VCO) 1: Starved Ring Oscilator



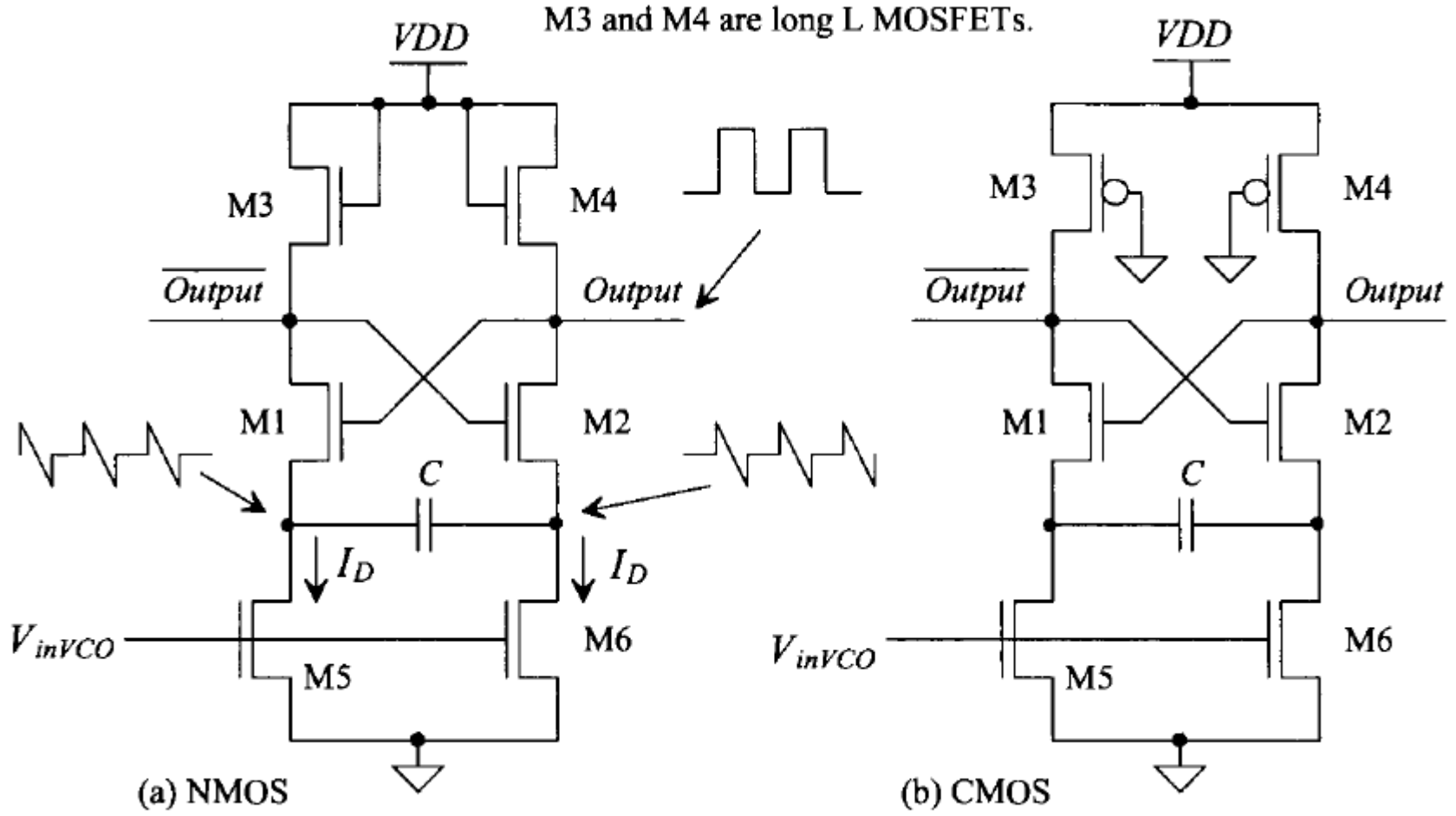
PLL Digital -VCO RO

- Linealización del VCO 1



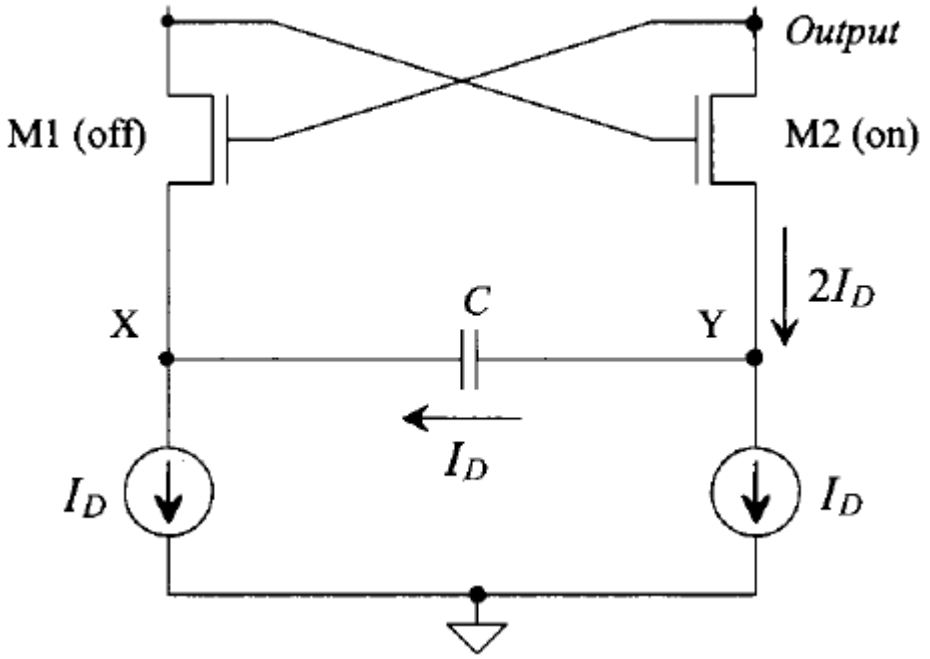
PLL Digital – VCO SC

- VCO 2: Source-Coupled



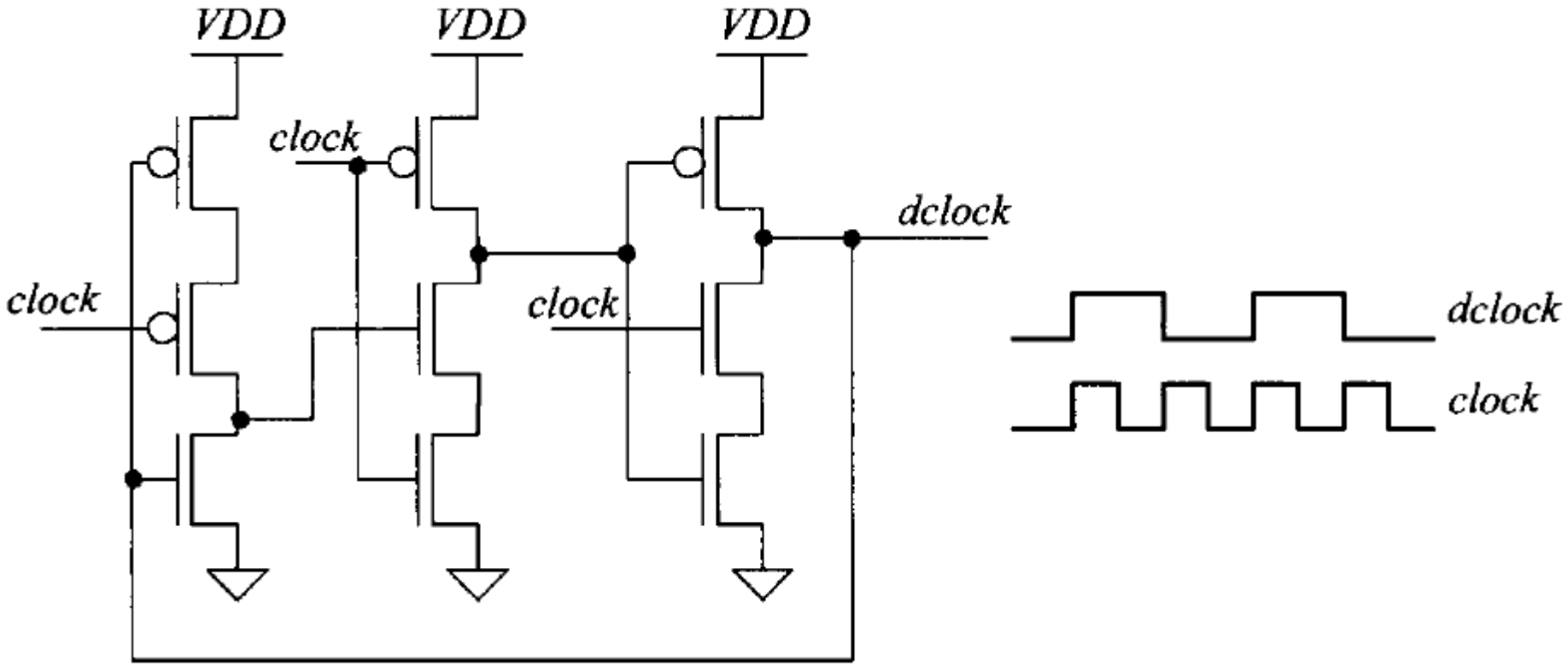
PLL Digital – VCO SC

- VCO 2: Source-Coupled



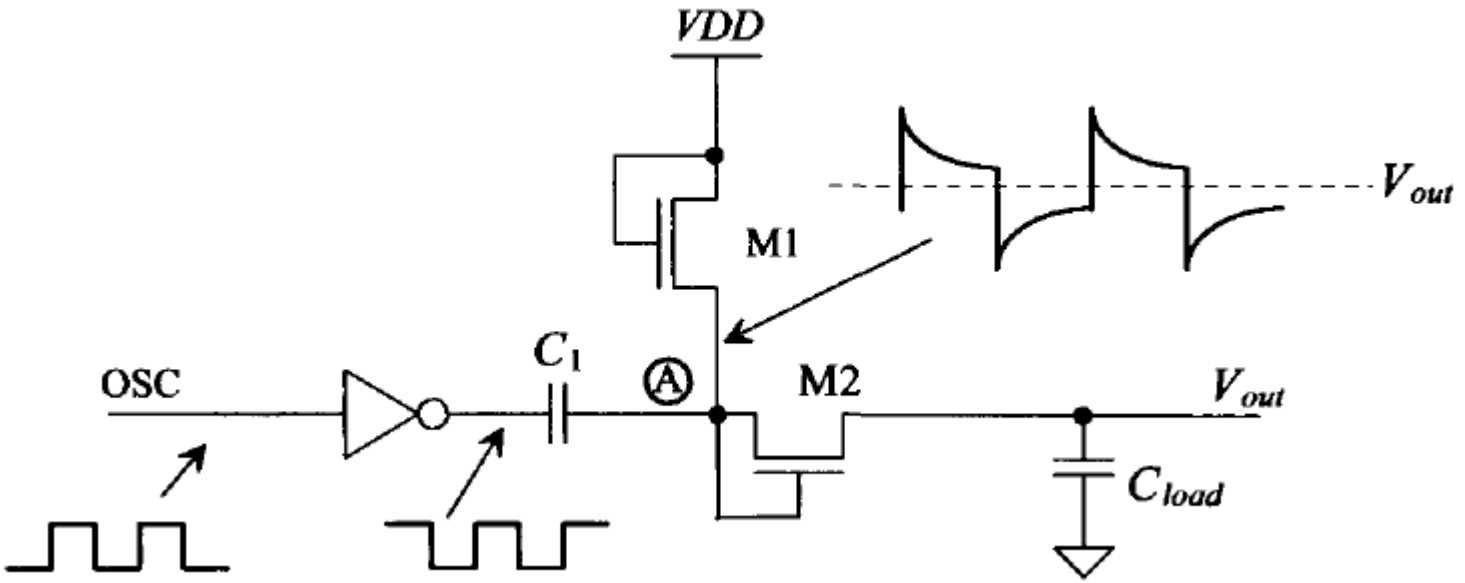
PLL Digital - FD

- Divisor de frecuencia



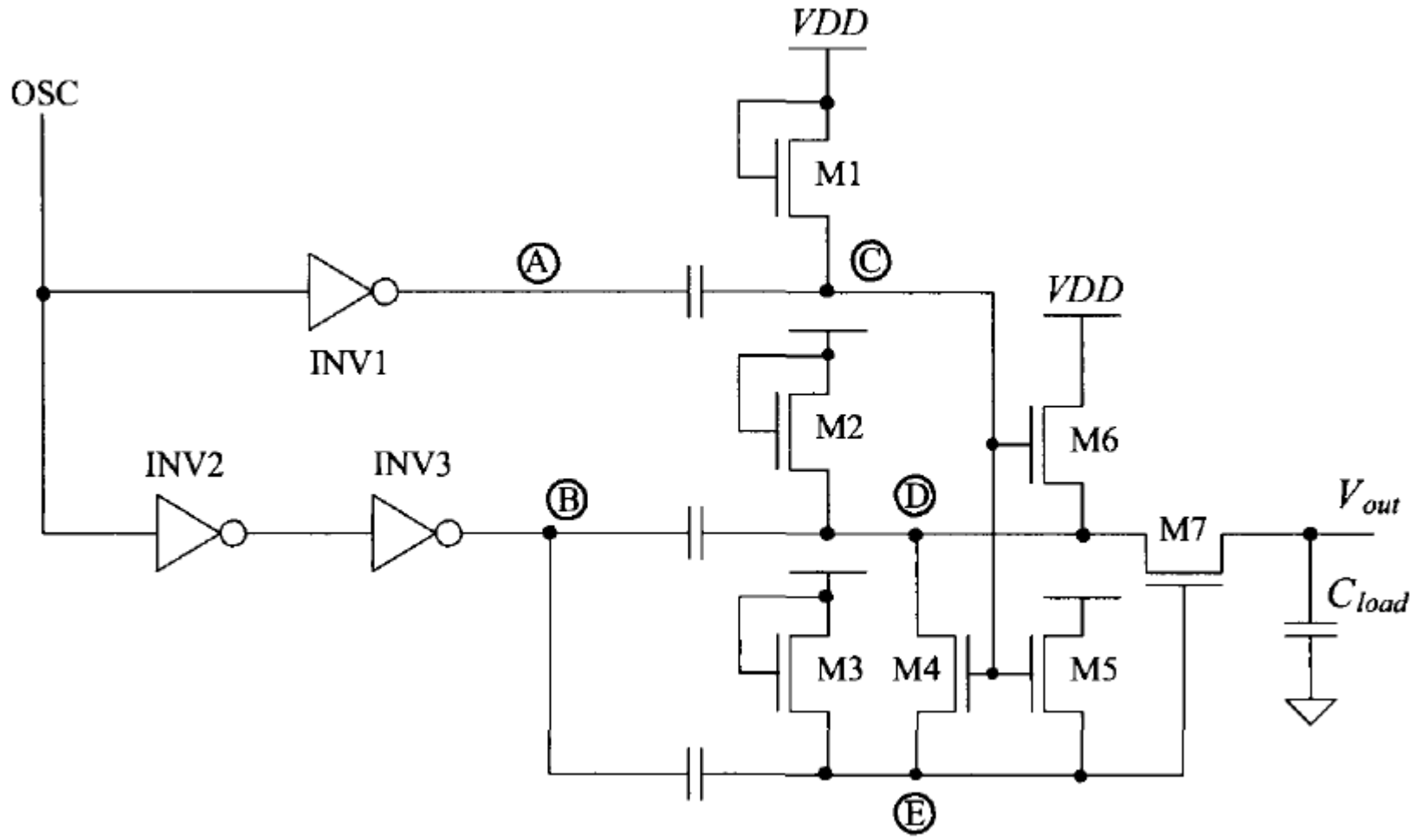
Charge Pump

- Generador de tensión mayor a V_{DD}



Charge Pump

- Dickson CP



Charge Pump

- Dickson CP multistage