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Towards artificial general intelligence with hybrid Tianjic chip architecture

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Abstract



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Extended data figures and tables

Extended Data Fig. 1 Overview of the FCore architecture.

Extended Data Fig. 2 Fabrication of the Tianjic chip and testing boards.

a

b

Extended Data Fig. 3 Throughput-aware unfolded mapping and resource-aware folded mapping.

a

b

Extended Data Fig. 4 Chip measurements in different modes.

a

b

x

c

Extended Data Fig. 5 Performance comparison and routing profiling.

a

b

c

d

e

f

Extended Data Fig. 6 Overheads of the Tianjic chip during the bicycle experiment.

a

b

Extended Data Fig. 7 Neural state machine.

a

b

Extended Data Table 1 A unified description of neural network models

Extended Data Table 2 Comparison of the Tianjic chip with existing specialized platforms

Extended Data Table 3 Model topologies and input/output descriptions for networks applied in the bicycle demonstration

Supplementary information

[41586_2019_1424_MOESM1_ESM.mp4](#)

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