ETHZ

MASTER PROJECT REPORT

Microelectronic circuit design for neural interfaces in 0.18um CMOS technology using an open source VLSI ecosystem

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Abstract

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The Thesis Abstract is written here (and usually kept to just this page). The page is kept centered vertically so can expand into the blank space above the title too...

Acknowledgements

The acknowledgments and the people to thank go here, don't forget to include your project advisor...

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LAH	**L**ist **A**bbreviations **H**ere
WSF	**W**hat (it) **S**tands **F**or

Chapter 1

Introduction

1.1 Overview

The field of integrated circuit (IC) design has traditionally relied on proprietary tools and resources, often posing a barrier to entry for students, researchers, and hobbyists due to their high costs. This project, titled "Microelectronic Circuit Design for Neural Interfaces in 0.18um CMOS Technology Using an Open Source VLSI Ecosystem," seeks to challenge this paradigm by leveraging open-source tools for the design and implementation of a CMOS inverter-based amplifier. The ultimate goal is to demonstrate that high-quality IC designs can be achieved through accessible and collaborative open-source resources, thereby promoting innovation and democratizing technology.

1.2 Significance of Open-Source Tools

Open-source tools are pivotal in democratizing technology and fostering an inclusive environment for technological advancements. They provide a cost-effective platform for exploring and innovating in IC design, making it accessible to a broader audience. This project underscores the potential of open-source tools to reduce development costs, encourage collaboration, and accelerate the pace of technological advancements in the field of microelectronics.

1.3 Project Objectives

The primary objectives of this project are multifaceted:

- **Design and Implementation:** Develop a CMOS inverter-based amplifier that adheres to specific design specifications.
- **Tool Utilization:** Demonstrate the capabilities of various open-source tools throughout the IC design workflow.
- **Educational Resource:** Create a comprehensive guide and resource for future projects and studies in IC design using open-source tools.
- **Community Contribution:** Contribute to the open-source community by documenting the design process and sharing the project files.

1.4 Scope of the Project

This project encompasses the entire IC design workflow, from initial concept to final layout, utilizing open-source tools such as:

- **Xschem:** For schematic capture and design.
- **Ngspice:** For circuit simulation and analysis.
- **Magic:** For layout design and verification.
- **Netgen:** For layout versus schematic (LVS) checks.
- **SkyWater SKY130 PDK:** The process design kit used to ensure the design meets manufacturing standards.

1.5 Amplifier Design Basis

The amplifier designed in this project is inspired by the architecture presented in Figure 3.a of the paper "Extracellular Recording of Entire Neural Networks Using a Dual-Mode Microelectrode Array With 19,584 Electrodes and High SNR." This amplifier is intended to serve as a pixel amplifier in an Active Pixel Sensor (APS) readout circuit on a microelectrode array. The main function of this amplifier is to enhance the signal-to-noise ratio (SNR) for extracellular recordings of neural networks. In the context of a neural interface, the amplifier must reliably amplify the small signals generated by neural activity while maintaining a high SNR to ensure accurate and clear signal readings. This makes the design crucial for high-fidelity neural recordings and subsequent data analysis.

1.6 Structure of the Report

The report is organized into the following chapters:

- **Introduction:** Provides an overview and context for the project.
- **Workflow:** Details the step-by-step design process.
- **Documentation of the Design Process:** Explains how the design process was documented in the wiki, including tools presentation, installation steps, and additional resources.
- **CMOS Inverter-Based Amplifier:** Discusses the design and implementation of the amplifier in detail.
- **Conclusion:** Summarizes the project outcomes and lessons learned.
- **Glossary:** Defines key terms and acronyms.
- **Appendices:** Includes supplementary materials and additional resources.

1.7 Expected Outcomes

By the conclusion of this project, we aim to achieve the following outcomes:

- Successfully design and simulate a CMOS inverter-based amplifier.
- Create a fully functional layout ready for fabrication.
- Validate the design through extensive simulation and verification steps.

- Document the entire design process to serve as a reference for future projects.

In summary, this project not only aims to demonstrate the feasibility of high-quality IC design using open-source tools but also seeks to contribute valuable resources to the open-source community and pave the way for future innovations in the field of microelectronics.

Chapter 2

Workflow

2.1 Overview of Analog IC Design Flow

Analog IC design is a meticulous process that requires extensive manual work and iterative refinement. Unlike digital design, which can be heavily automated, analog design demands close attention to the relationship between the design and the physical device models. While commercial tools have historically dominated this space, recent advancements in open-source software have made it possible to manage the essential tasks of analog IC design effectively.

2.2 Design Flow Schematic

The following schematic illustrates the sequential and iterative process employed in analog IC design using the open-source tools recommended by Efabless. This workflow guides the design from concept to layout, highlighting the stages where iterations are necessary to refine the design and meet specifications.

2.3 Design Stages and Their Purpose

2.3.1 Design Concept (Python)

The initial stage of the design process involves formulating and modeling the idea. This stage leverages mathematical and simulation tools such as Python, along with libraries like NumPy and SciPy, to create preliminary models and validate initial concepts.

2.3.2 Schematic Entry (Xschem)

In this stage, the design specifications are translated into a schematic diagram using tools like Xschem. Xschem is known for its user-friendly interface, which simplifies the process of creating and managing schematic diagrams.

2.3.3 Simulation (ngspice)

Once the schematic is complete, the design is simulated using ngspice. This simulation tool ensures that the design operates correctly within the defined specifications, allowing for the identification and correction of any issues early in the process.

2.3.4 Layout (Magic)

The physical design stage involves drawing the geometries that will form the semiconductor device's layers. Magic is used for this purpose, providing a robust platform for creating the layout while adhering to design rules.

2.3.5 Design Rule Check (DRC) (Magic)

After the layout is complete, Magic provides an interactive design rule check (DRC) to validate that the layout adheres to manufacturing standards. This step is crucial for ensuring that the design can be successfully fabricated.

2.3.6 Layout versus Schematic (LVS) (Netgen)

Netgen is used to compare the layout against the schematic (LVS) to ensure they match perfectly. This verification step is essential to confirm that the physical layout accurately represents the intended circuit design.

2.3.7 Device and Parasitic Extraction (Magic)

Magic also aids in the extraction of parasitic elements that occur during the layout phase. These parasitics can impact the circuit's performance, and their identification allows for further optimization of the design.

2.4 Process Design Kits (PDKs)

Process Design Kits (PDKs) are vital in IC design, providing a collection of manufacturing process-specific rules, tools, and components. For this project, the SkyWater 130nm CMOS sky130 PDK is utilized, offering a comprehensive suite of analog and digital design capabilities.

2.5 Documentation of the Design Process in the Wiki

Throughout this project, extensive documentation was created to aid future designers. The design process, tool presentation, installation steps, and additional resources are thoroughly detailed in the project wiki. This documentation includes:

- Detailed instructions on the installation and use of each tool.
- Step-by-step guides for each stage of the design process.
- Troubleshooting tips and best practices.
- Links to further resources and community contributions.

For more extensive details on each tool's functions, installation, and integration with the Sky130 PDK, please refer to the wiki pages. This supplementary information is designed to provide a deeper understanding of the toolset used throughout the analog IC design process.

In summary, this workflow chapter provides a comprehensive overview of the stages involved in analog IC design using open-source tools. By following this structured process, we aim to achieve a robust and functional CMOS inverter-based amplifier design.

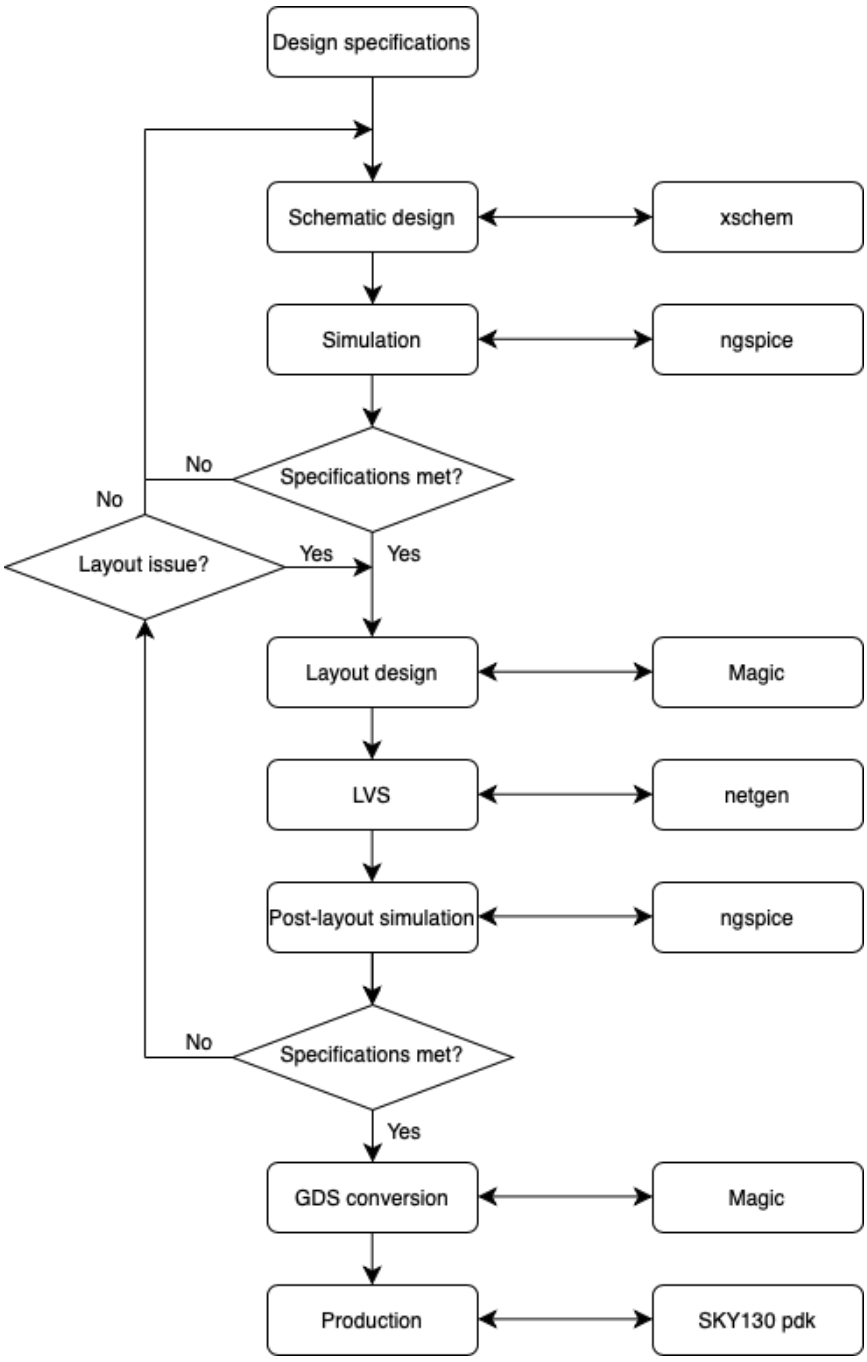

FIGURE 2.1: Analog IC Design Flow Schematic

Appendix A

Frequently Asked Questions

A.1 How do I change the colors of links?

The color of links can be changed to your liking using:

`\hypersetup{urlcolor=red}`, or
`\hypersetup{citecolor=green}`, or
`\hypersetup{allcolor=blue}`.

If you want to completely hide the links, you can use:

`\hypersetup{allcolors=.}`, or even better:
`\hypersetup{hidelinks}`.

If you want to have obvious links in the PDF but not the printed text, use:

`\hypersetup{colorlinks=false}`.

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