

Semester Project Report

Your Name

March 13, 2024

Notes

- Chiplicity = efabless.com methodology for building up complete chips ready for fabrication from component parts pulled from the Efabless IP catalog
- 2 types of IP = Clone Hard IP (open-source), Try Hard IP (proprietary)
- The virtual desktop already provides all tools required for design and verification including the OpenLane design flow, Magic, Klayout, Netgen, Ngspice, and Xschem. These tools do not need to (and can not) be installed in the desktop by users. The desktop also include an installation of the SKY130 pdk.
- Talk about OpenLane.
- Talk about the Skywater 130nm PDK.
- Talk about the Efabless IP catalog.
- There are versions for different supply voltages, ranging from 1.8 up to even 20 V. There's a native NMOS for 3.3 V, but there are also low-threshold variants for 1.8 V power supply. As the main purpose of this paper is to demonstrate a simple, but working, opamp design, we select the transistor capable of working under 3.3 V to work with. This transistor is limited to 500 nm minimum channel length.
- For that supply voltage, we have transfer characteristics in paper <https://doi.org/10.1109/MIEL52794>.

0.1 Installation of Tools

Magic VLSI

MAC:

```
git clone https://github.com/RTimothyEdwards/magic
cd magico
brew install cairo tcl-tk python3
brew install --cask xquartz
```

```
./scripts/configure_mac
```