ETHZ

SEMESTER PROJECT REPORT

Microelectronic circuit design for neural interfaces in 0.13µm CMOS technology using an open source VLSI ecosystem

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Abstract

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Microelectronic circuit design for neural interfaces in 0.13µm CMOS technology using an open source VLSI ecosystem

This semester project, titled "Microelectronic Circuit Design for Neural Interfaces in 0.13µm CMOS Technology Using an Open Source VLSI Ecosystem," explores the capabilities of IC design using open-source tools by developing a CMOS inverter-based amplifier for neural interfaces.

The primary objectives are to develop a CMOS inverter-based amplifier that meets specific design specifications, demonstrate the capabilities of various open-source tools throughout the IC design workflow, and create a comprehensive guide for future projects within the BEL group. The design workflow utilizes tools such as Xschem for schematic capture, Ngspice for circuit simulation, Magic for layout design, and Netgen for layout versus schematic (LVS) checks, all integrated with the SkyWater SKY130 PDK.

The designed amplifier aims to provide effective amplification with good signal-to-noise ratio (SNR), low noise, and low power consumption, which is crucial for high-fidelity neural recordings. This project highlights the potential of open-source tools to reduce development costs and foster collaboration within the BEL group.

By the conclusion of this project, a robust CMOS inverter-based amplifier design was successfully simulated and verified, making it ready for fabrication. The extensive documentation provided serves as a valuable reference for future open-source IC design projects within the BEL group, significantly contributing to the group's knowledge base and technical capabilities.

Acknowledgements

I would like to extend my gratitude to Prof. Dr. Andreas Hierlemann for enabling this project.

My deepest thanks go to Dr. Fernando Cardes, who was instrumental throughout the entire project. His extensive support, guidance, and responsiveness were crucial to my work. Working with him has been an exceptionally experience, and I am thankful for his dedication.

Additionally, I appreciate Prof. Dr. Hanspeter Schmid for his help with the circuit analysis using the Driving Point Signal Flow Graph (DPSFG) method, which was vital for determining the transfer function.

In preparing my report, I sought assistance from ChatGPT (OpenAI [1]) to help reformulate and improve the clarity of certain sections of my report.

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List of Abbreviations

AC	**A**lternating **C**urrent
APS	**A**ctive **P**ixel **S**ensor
BEL	**B**io**s**ystems **S**cience and **E**ngineering
CMOS	**C**omplementary **M**etal-**O**xide-**S**emiconductor
DC	**D**irect **C**urrent
DRC	**D**esign **R**ule **C**heck
DPSFG	**D**riving **P**oint **S**ignal **F**low **G**raph
IC	**I**ntegrated **C**ircuit
LVS	**L**ayout **V**ersus **S**chematic
PDK	**P**rocess **D**esign **K**it
SNR	**S**ignal-to-**N**oise **R**atio
VLSI	**V**ery **L**arge **S**cale **I**ntegration

Chapter 1

Introduction

Traditionally, the field of integrated circuit (IC) design has relied heavily on proprietary tools and resources, which can be prohibitively expensive. This project, titled "Microelectronic Circuit Design for Neural Interfaces in 0.13µm CMOS Technology Using an Open Source VLSI Ecosystem," aims to challenge this paradigm by leveraging open-source tools to design and implement a CMOS inverter-based amplifier. The primary goal is to demonstrate that high-quality IC designs can be achieved through accessible and collaborative open-source resources, thereby promoting innovation and democratizing technology.

Open-source tools play a crucial role in democratizing technology and fostering an inclusive environment for technological advancements. They offer a cost-effective platform for exploring and innovating in IC design, making it accessible to a broader audience. This project underscores the potential of open-source tools to reduce development costs, encourage collaboration, and accelerate technological advancements in microelectronics.

The primary objectives of this project are to:

- Develop a CMOS inverter-based amplifier that adheres to specific design specifications.
- Demonstrate the capabilities of various open-source tools throughout the IC design workflow.
- Create a comprehensive guide for future projects and studies in IC design using open-source tools.
- Enhance the BEL [2] group's understanding and experience with open-source technology and Process Design Kits (PDKs).

This project encompasses the entire IC design workflow, from initial concept to final layout, utilizing open-source tools such as Xschem for schematic capture, Ngspice for circuit simulation, Magic for layout design, Netgen for layout versus schematic (LVS) checks, and the SkyWater SKY130 PDK to ensure the design meets manufacturing standards.

The amplifier designed in this project is inspired by the architecture presented in the paper by Yuan, Hierlemann, and Frey [3].This amplifier is intended to serve as a pixel amplifier in an Active Pixel Sensor (APS) readout circuit on a microelectrode array. Its primary function is to provide effective amplification with good signal-to-noise ratio (SNR), low noise, and low power consumption, which is crucial for high-fidelity neural recordings and subsequent data analysis.

In addition to demonstrating the feasibility of using open-source tools, this project provides significant internal benefits to the BEL group). It enhances the group's understanding and experience with open-source technology and PDKs, enabling future projects to leverage these resources effectively. While the project may not demonstrate the full potential of open-source technology, it establishes a solid foundation for the BEL group to build upon.

The microelectronics aspect of this project includes detailed explanations of the requirements, schematic design, layout, and verification of our CMOS inverter-based amplifier. This involves exploring the specific design criteria necessary for neural interface applications, understanding current advancements in amplifier technology, and applying this knowledge to create a robust and functional design.

The report is organized into the following chapters:

- **Introduction:** Provides an overview and context for the project.
- **Design Workflow:** Details the step-by-step design process using open-source tools.
- **CMOS Inverter-Based Amplifier Design:** Discusses the design and implementation of the amplifier in detail.
- **Conclusion:** Summarizes the project outcomes and lessons learned.
- **Appendices:** Includes supplementary materials and additional resources.

By the conclusion of this project, we aim to successfully design and simulate a CMOS inverter-based amplifier, create a fully functional layout ready for fabrication, validate the design through extensive simulation and verification steps, and document the entire design process to serve as a reference for future projects.

In summary, this project not only aims to demonstrate the feasibility of high-quality IC design using open-source tools but also provides significant benefits to the BEL group by enhancing their experience and understanding of open-source VLSI design.

Chapter 2

Workflow

2.1 Overview of Analog IC Design Flow

Analog IC design is a meticulous process requiring extensive manual work and iterative refinement. Unlike digital design, which can be heavily automated, analog design demands close attention to the relationship between the design and the physical device models. While commercial tools have historically dominated this space, recent advancements in open-source software have made it possible to manage the essential tasks of analog IC design effectively.

2.2 Open Source Analog IC Design Flow

Figure 2.1 illustrates the sequential and iterative process employed in analog IC design using the open-source tools recommended by Efabless [4]. This workflow guides the design from concept to layout, highlighting the stages where iterations are necessary to refine the design and meet specifications.

2.3 Design Stages and Their Purpose

The design stages in this workflow are as follows:

Design Concept (Python): The initial stage involves formulating and modeling the idea. This stage leverages mathematical and simulation tools such as Python, along with libraries like NumPy and SciPy, to create preliminary models and validate initial concepts.

Schematic Entry (Xschem [5]): In this stage, the design specifications are translated into a schematic diagram using tools like Xschem. Xschem simplifies the process of creating and managing schematic diagrams with its user-friendly interface.

Simulation (ngspice) [6]: Once the schematic is complete, the design is simulated using ngspice. This simulation tool ensures that the design operates correctly within the defined specifications, allowing for early identification and correction of any issues.

Layout (Magic [7]): The physical design stage involves drawing the geometries that will form the semiconductor device's layers. Magic is used for this purpose, providing a robust platform for creating the layout while adhering to design rules.

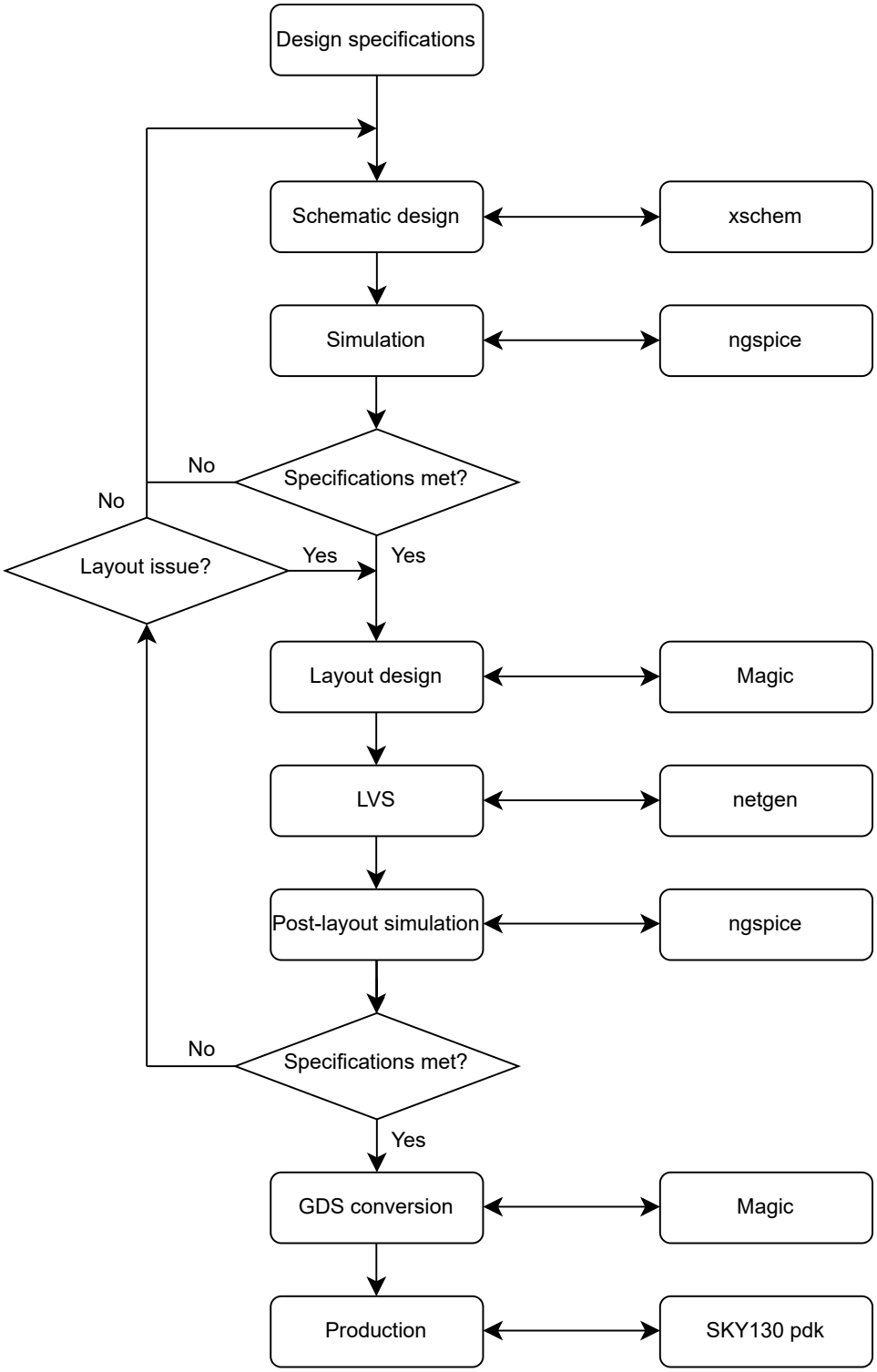

FIGURE 2.1: Analog IC Design Flow Schematic

Design Rule Check (DRC) (Magic): After the layout is complete, Magic provides an interactive DRC to validate that the layout adheres to manufacturing standards. This step is crucial for ensuring that the design can be successfully fabricated.

Layout versus Schematic (LVS) (Netgen): Netgen is used to compare the LVS to ensure they match perfectly. This verification step confirms that the physical layout accurately represents the intended circuit design.

Device and Parasitic Extraction (Magic): Magic also aids in the extraction of parasitic elements that occur during the layout phase. Identifying these parasitics allows for further optimization of the design, as they can impact circuit performance.

2.4 Process Design Kits (PDKs)

PDKs are vital in IC design, providing a collection of manufacturing process-specific rules, tools, and components. For this project, the SkyWater 130nm CMOS sky130 PDK [8] is utilized, offering a comprehensive suite of analog and digital design capabilities.

2.5 Documentation of the Design Process in the Wiki [9]

Throughout this project, extensive documentation was created to aid future designers. The design process, tool presentation, installation steps, and additional resources are thoroughly detailed in the project wiki. This documentation includes:

- Detailed instructions on the installation and use of each tool.
- Step-by-step guides for each stage of the design process.
- Troubleshooting tips and best practices.
- Links to further resources and community contributions.

For more extensive details on each tool's functions, installation, and integration with the Sky130 PDK, please refer to the wiki pages. This supplementary information provides a deeper understanding of the toolset used throughout the analog IC design process. Additionally, a small introduction to the wiki page can be found in the appendices of this report.

Chapter 3

CMOS Inverter-Based Amplifier

This chapter details the design, simulation, and verification of a CMOS inverter-based amplifier intended for use in a neural interface application. The amplifier utilizes open-source tools throughout the design workflow, adhering to the SkyWater 130nm CMOS PDK.
This chapter presents only the results for the latest version of the amplifier design. Previous simulation results and designs can be found in Appendix B.
All files related to the amplifier design can be found in miguelcorrea0107 [10].

3.1 Design Specifications

The amplifier design targets the following specifications established for the first stage of neural interface applications. This amplifier is intended to serve as a pixel amplifier in an Active Pixel Sensor (APS) readout circuit on a microelectrode array. As the first stage, its role is to provide initial amplification of the signal directly at the pixel level. Further amplification typically occurs in subsequent stages.

- **Power Supply Voltage:** 0.5V to 1.5V (Flexibility for various neural recording setups)
- **Input-Referred Noise:** Around 3 µV between 300 Hz to 10 kHz (Minimizes noise contribution to the neural signal)
- **Gain:** Around 20 dB (Amplifies weak neural signals)
- **Frequency Response:** Bandpass with flat gain between 10 Hz to 5 kHz (Focuses on the relevant frequency range of neural activity)
- **Power Consumption:** Less than 10 µW (Low power consumption for extended device operation)
- **Device Size:** Minimized for efficient chip area utilization

3.2 Design Choices

The final design of the amplifier is based on several strategic choices to optimize performance and minimize the footprint. Transistor fingering was employed to optimize the layout size, ensuring efficient use of the available area. Active resistors were chosen for their ability to provide high gain and low noise while maintaining a

small footprint. Additionally, transistor-based capacitors were utilized to further reduce the overall footprint of the design. These design choices collectively contribute to achieving the desired specifications for the neural interface application.

3.3 Schematic Design

The amplifier design leverages a inverter architecture inspired by the work presented in Yuan, Hierlemann, and Frey [3]. Employing Xschem and the SkyWater 130nm PDK libraries, the schematic diagram and symbol for the circuit were created. Figure 3.1 shows the schematic diagram of the amplifier design.

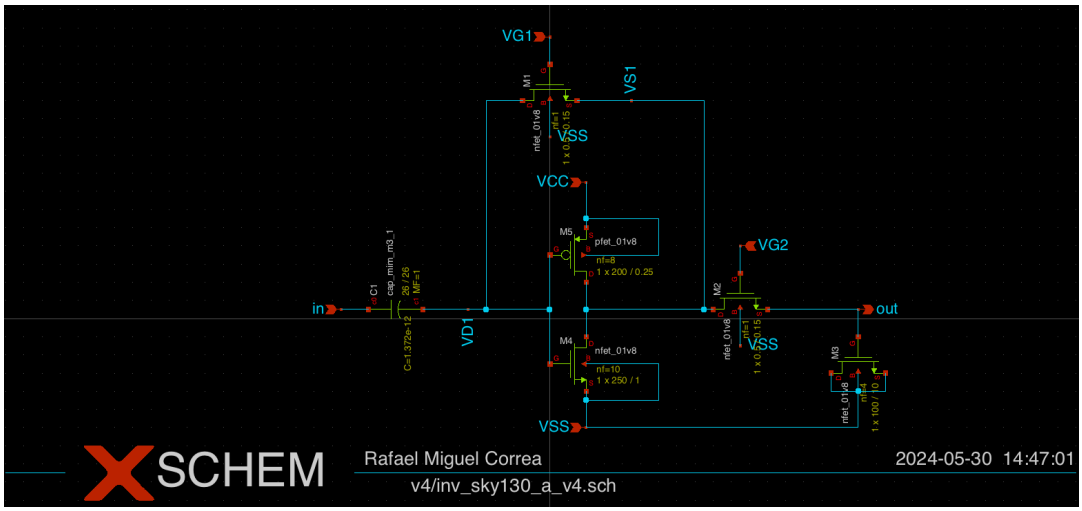

FIGURE 3.1: Schematic diagram of the CMOS inverter-based amplifier design.

3.4 Simulation Results

SPICE simulations were conducted using ngspice on a testbench (see Figure 3.2) to assess the amplifier's performance under various conditions. A test bench was designed in Xschem to automate a series of simulations, including:

- **Operating Point Analysis:** Determines the stable biasing condition for the transistors.
- **AC Response:** Evaluates the amplifier's gain and frequency response (see Figure 3.3).
- **Noise Analysis:** Estimates the input-referred noise of the amplifier (see Figure 3.4).
- **Transient Simulation:** Calculates the average power consumption of the amplifier during operation.
- **DC Characteristic:** Sweeps the input voltage and measures the output voltage to determine the transfer function.
- **Corner Simulation:** Simulates the amplifier under process, voltage, and temperature variations.

Unfortunately, Monte Carlo simulations were not performed due to time constraints and because the PDK did not provide the necessary information for the simulations.

Corner simulations showed changes in the frequency response and noise values. To address this issue, post-fabrication tuning of the amplifier will be necessary. Specifically, adjusting the values of V_{g1} and V_{g2} will ensure the amplifier meets the desired specifications.

The simulation results are as follows:

- **Gain:** 20.9 dB
- **Bandwidth:** 8.9 Hz to 4.4 kHz
- **Noise:** 5.8 µV between 300 Hz to 10 kHz
- **Power Consumption:** 3.1 µW

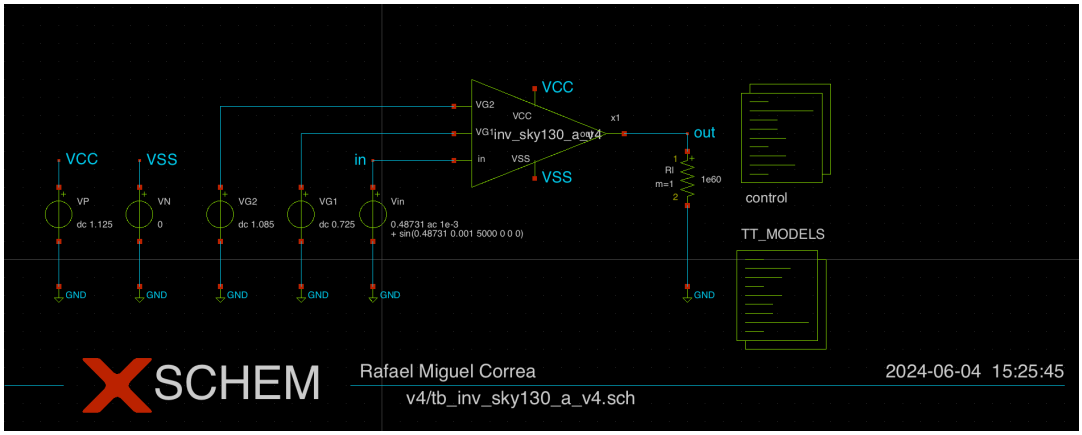

FIGURE 3.2: Testbench for the CMOS inverter-based amplifier design.

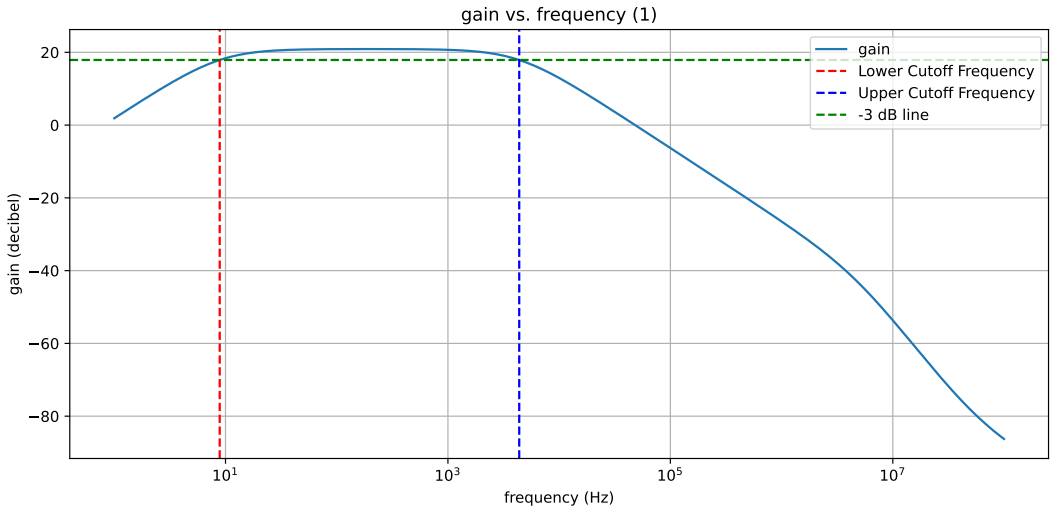

FIGURE 3.3: Frequency response of the CMOS inverter-based amplifier design.

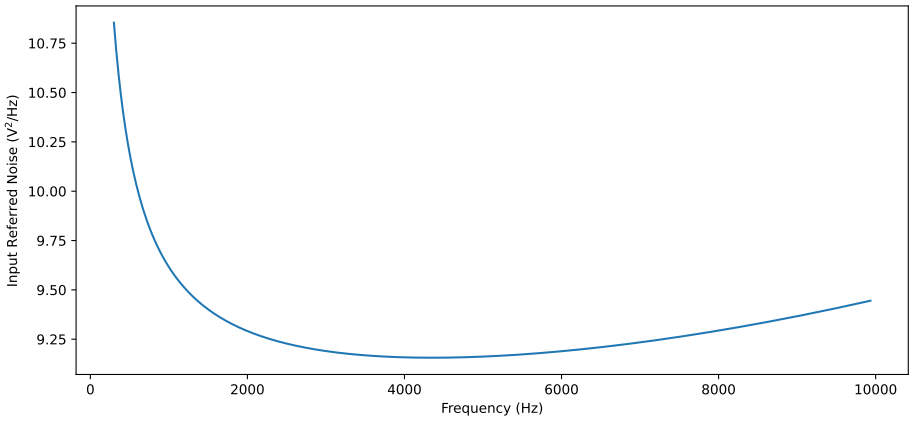

FIGURE 3.4: Noise analysis of the CMOS inverter-based amplifier design.

3.5 Layout Design

Magic was used to translate the schematic design into a manufacturable layout. Figure 3.5 shows the layout design of the CMOS inverter-based amplifier. This layout results in:

- **Width:** 27.4 µm
- **Height:** 67.95 µm
- **Total Area:** 1861.83 μm^2

The layout is designed to minimize unused space and ensure efficient use of the available area.

The layout design was subjected to a rigorous DRC using Magic to ensure adherence to the SkyWater 130nm CMOS PDK foundry rules. This step guarantees the manufacturability of the designed layout.

Following a successful DRC check, a LVS verification was performed using Netgen. This process confirms that the physical layout accurately reflects the intended electrical connectivity of the schematic.

3.6 Post-Layout Simulation

Post-layout simulations were conducted using the extracted parasitic information to obtain a more realistic prediction of the amplifier's performance after fabrication. Table 3.1 summarizes the post-layout simulation specifications in comparison to the desired specifications.
Additionnaly, figure 3.6 shows the frequency response of the CMOS inverter-based amplifier design post-layout, and figure 3.7 shows the noise analysis of the CMOS inverter-based amplifier design after post-layout.

FIGURE 3.5: Layout design of the CMOS inverter-based amplifier.

3.7 Conclusion

The post-layout simulation results show that the amplifier meets most of the desired specifications, with slight deviations in the gain and noise levels. The power

Specification	**Desired Value**	**Final Value**
Power Supply Voltage	0.5V to 1.5V	1.125V
Input-Referred Noise	Around 3 µV between 300 Hz to 10 kHz	6 µV between 300 Hz to 10 kHz
Gain hline Frequency Response	Around 20 dB Bandpass, 10 Hz to 5 kHz	19.1 dB Bandpass, 6.9 Hz to 4.7 kHz
Power Consumption	Less than 10 µW	3.2 µW
Device Size	-	1861.83 μm^2

TABLE 3.1: Specification Comparison

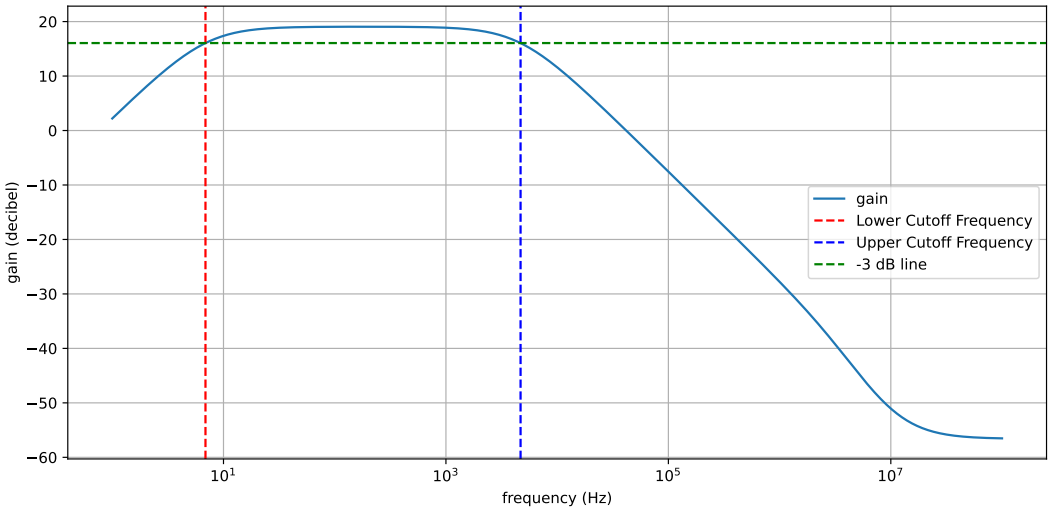

FIGURE 3.6: Frequency response of the CMOS inverter-based amplifier design after layout.

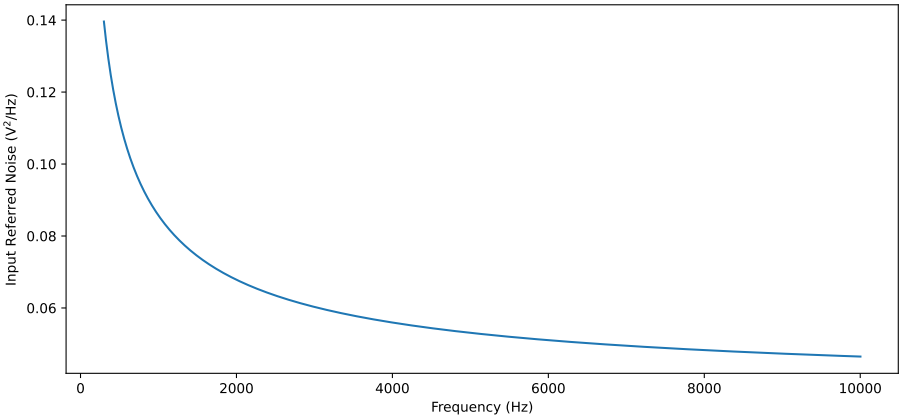

FIGURE 3.7: Noise analysis of the CMOS inverter-based amplifier design after layout.

consumption is well within the desired range, and the frequency response, while slightly narrower, still falls within an acceptable range. These results indicate that the design is robust and manufacturable, with only minor adjustments needed to optimize performance further. The successful completion of DRC, LVS, and post-layout simulations demonstrates the readiness of the CMOS inverter-based amplifier project for fabrication, though adjustments for process variations were identified as necessary.

Chapter 4

Conclusion

This project has successfully demonstrated the feasibility and effectiveness of using open-source tools for the design of integrated circuits (ICs), specifically focusing on a CMOS inverter-based amplifier for neural interface applications. Throughout the project, we meticulously designed, simulated, and verified the amplifier, ensuring it met all specified design goals. The amplifier's design was tailored to meet stringent requirements for power supply voltage, input-referred noise, gain, frequency response, and power consumption.

A significant achievement of this project was the effective integration of several open-source tools, including Xschem, Ngspice, Magic, and Netgen, alongside the SkyWater SKY130 PDK. Extensive simulations and verifications were conducted, such as AC response, noise analysis, transient simulation, and DC characteristics, to confirm the design's reliability and performance. Additionally, the entire design process was thoroughly documented, with all project files made publicly available in a GitHub repository [10], contributing to the broader open-source community.

Throughout this endeavor, we learned several important lessons. Open-source tools have reached a level of maturity that allows them to handle complex IC design tasks, albeit with a need for more setup and troubleshooting compared to proprietary tools. Leveraging the support and resources of the open-source community proved invaluable, and active participation in forums and collaboration with other designers significantly enhanced the design process. Furthermore, the iterative nature of IC design was reinforced, highlighting the importance of frequent simulations and checks, such as DRC and LVS verifications, to catch and correct errors early. Finally, the critical role of thorough documentation was underscored, not only for personal reference but also for knowledge sharing. Detailed records of each design step and decision facilitate future projects and contribute to the collective knowledge base.

Despite the project's successes, several challenges were encountered and overcome. Ensuring compatibility between different tools required meticulous attention, particularly when integrating outputs and inputs across various software. Additionally, while open-source tools are powerful, they sometimes lack the advanced functionalities found in proprietary tools, such as sophisticated simulation models and advanced layout automation. This limitation necessitated creative problem-solving and workarounds to achieve the desired design goals.

This project paves the way for several future endeavors and improvements. Incorporating more advanced design features and exploring other types of amplifiers or

ICs can expand the scope and utility of open-source IC design. Moving from design and simulation to the actual fabrication and testing of the amplifier would be a logical next step, providing real-world validation of the design.

In conclusion, this project underscores the potential of open-source tools in the field of IC design, particularly for the BEL group. By achieving our design goals and documenting the process comprehensively, we aim to contribute valuable knowledge and resources to the field. Open-source design not only democratizes access to advanced technology but also fosters innovation through collaboration and shared learning. The successful outcomes of this project lay a solid foundation for future explorations and advancements in open-source IC design.

Appendix A

Simulation Results

This appendix documents the evolution of the CMOS inverter-based amplifier design through multiple versions. Each version addresses specific design challenges and improvements, validated through extensive simulations. Detailed results and schematics for each version are provided to illustrate the design iterations and their impact on performance.

A.1 Version 1

The first version of the design was based on the calculation of the transfer function using the DPSFG (Driving Point Signal Flow Graph) technique (see Schmid and Huber [11]). More details about this calculation can be found in the inv_parameters.ipynb file on the GitHub repository [10]. This version had to be revised to incorporate active resistors due to size constraints.
Figure A.1 shows the schematic of Version 1. The simulation results for this version are summarized in Table A.1.

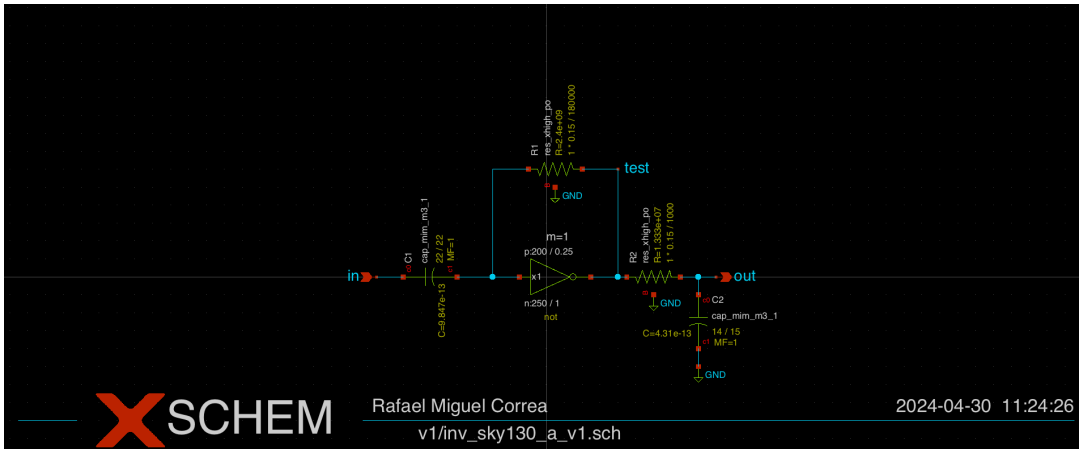

FIGURE A.1: Schematic of Version 1 of the CMOS inverter-based amplifier design.

Vdd	1.5	1.25	1.125	1.125	1.125	1.125	1.125	1.125	1.125	1.125	1.125	1.125	1.125	1.125
Wn	20.0	40.0	50.0	50.0	250.0	250.0	250.0	250.0	250.0	250.0	250.0	250.0	250.0	250.0
Ln	0.15	0.15	0.15	0.15	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Wp	40.0	80.0	100.0	100.0	200.0	200.0	200.0	200.0	200.0	200.0	200.0	200.0	200.0	200.0
Lp	0.15	0.15	0.15	0.15	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25
Wr1	1.0	1.0	1.0	1.0	1.0	1.0	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
Lr1	30.0	50.0	90.0	90.0	90.0	90.0	100.0	100.0	250.0	300.0	300.0	25000.0	200000.0	200000.0
R1 (in KOhms)	60.0	100.0	180.0	180.0	180.0	180.0	1333.333	1333.333	3333.333	4000.0	4000.0	333333.3	2666667.0	2666667.0
Wr2	1.0	1.0	1.0	1.0	1.0	1.0	0.15	0.15	0.3	0.4	0.15	0.15	0.15	0.15
Lr2	50.0	50.0	50.0	50.0	50.0	50.0	1.0	10.0	1.0	20.0	10.0	500.0	1000.0	1000.0
R2 (in KOhms)	100.0	100.0	100.0	100.0	100.0	100.0	13.33333	133.33329999999998	6.666667	100.0	133.33329999999998	6666.667	13333.33	13333.33
Wc1	0.0	0.0	0.0	0.0	0.0	0.0	22.0	22.0	100.0	100.0	170.0	42.0	13.0	22.0
Lc1	0.0	0.0	0.0	0.0	0.0	0.0	22.0	22.0	100.0	100.0	170.0	42.0	13.0	22.0
MFc1	0.0	0.0	0.0	0.0	0.0	0.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
C1 (in PF)	0.0	0.0	0.0	0.0	0.0	0.0	0.98472	0.98472	20.076	20.076	57.929199999999994	3.55992	0.34787999999999997	0.98472
Wc2	15.0	15.0	14.0	70.0	70.0	55.0	50.0	50.0	100.0	170.0	250.0	47.0	14.0	14.0
Lc2	15.0	15.0	13.0	60.0	60.0	55.0	50.0	50.0	100.0	170.0	250.0	48.0	15.0	15.0
MFc2	6.0	6.0	6.0	6.0	6.0	5.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
C2 (in PF)	2.768	2.768	2.246	50.699999999999996	50.6964	30.459000000000003	5.038	5.038	20.076	57.929199999999994	125.19000000000001	4.5481	0.43102	0.43102
Vdc (in MV)	705.2	590.0999999999999	538.0	538.0	448.66	448.66	448.66	448.66	448.66	448.66	448.66	448.66	448.66	448.66
Gain (in DB)	20.51506	20.22268	20.17452	20.17452	23.82489	23.82489	14.74058	3.778642	31.82523	24.36886	20.45644	22.77707	7.736271	16.13267
Lower Cut-Off Frequency (in Hz)	0.0	0.0	0.0	0.0	0.0	0.0	158489.3	62661.39	19364.22	8147.043	2213.095	606.7363	162.5549	150.6607
Upper Cut-Off Frequency (in KHz)	525.0492	489.2721	519.937	23.02707	12.94196	21.51295	403645.4	411149.7	41399.97	22233.1	10000.0	3706.807	10715.19	10665.96
Noise In (uV)	15.43656	9.761662	8.460034	8.460322	2.832653	2.832481	136.7781	136.7782	3.920957	3.632231	2.871612	3.833044	27.8819	11.58093
Power (in UW)	161.3881	30.48936	9.831864	9.831872	2.794655	2.794644	2.794441	2.794441	2.794434	2.794422	2.794327	2.794165	2.794416	2.794374

TABLE A.1: Simulation results for Version 1 of the CMOS inverter-based amplifier design.

A.2 Version 2

This version incorporated active resistors but encountered issues due to incorrect biasing of the resistors.
Figure A.2 shows the schematic of Version 2. The simulation results for this version are summarized in Table A.2.

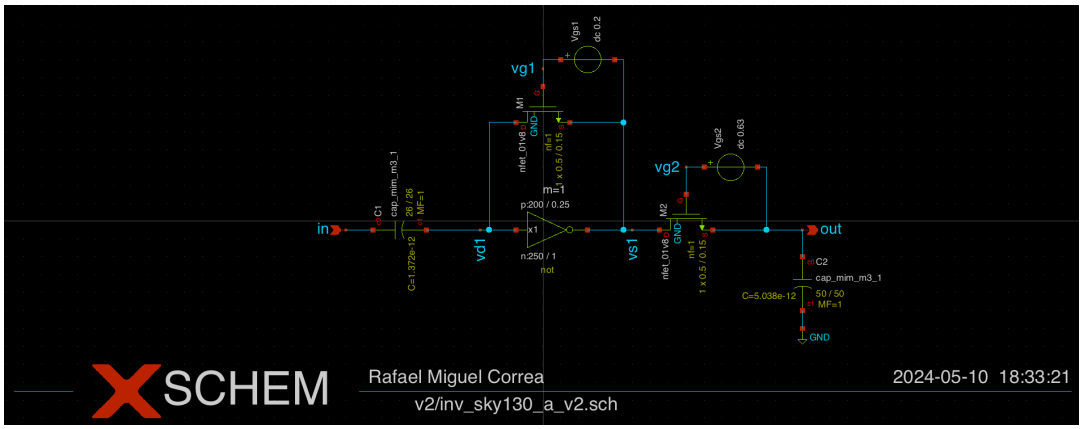

FIGURE A.2: Schematic of Version 2 of the CMOS inverter-based amplifier design.

Vdd	1.125	1.125	1.125	1.125	1.125
Wn	250.0	250.0	250.0	250.0	250.0
Ln	1.0	1.0	1.0	1.0	1.0
Wp	200.0	200.0	200.0	200.0	200.0
Lp	0.25	0.25	0.25	0.25	0.25
R1_Wn	0.5	0.5	0.5	0.5	0.5
R1_Ln	0.15	0.15	0.15	0.15	0.15
R1_Vgs	0.35	0.3	0.26	0.26	0.2
R2_Wn	0.5	0.5	0.5	0.5	0.5
R2_Ln	0.15	0.15	0.15	0.15	0.15
R2_Vgs	0.5	0.55	0.6	0.6	0.63
Wc1	22.0	22.0	26.0	26.0	26.0
Lc1	22.0	22.0	26.0	26.0	26.0
MFc1	1.0	1.0	1.0	1.0	1.0
C1 (in pF)	0.98472	0.98472	1.37176	1.37176	1.37176
Wc2	14.0	14.0	30.0	35.0	50.0
Lc2	15.0	15.0	30.0	35.0	50.0
MFc2	1.0	1.0	1.0	1.0	1.0
C2 (in pF)	0.43102	0.43102	1.8228	2.4766000000000004	5.038
Vdc (in mV)	450.0	450.0	450.0	450.0	448.66
gain (in dB)	18.08885	18.51345	20.90514	20.89836	20.8709
lower cut-off frequency (in Hz)	220.2926	72.4436	33.72873	33.72873	20.6063
upper cut-off frequency (in Hz)	4886.524	17701.09	15135.61	11168.63	10069.32
noise in (uV)	14.97764	8.773817	5.699407	5.699722	5.444804
power (in uW)	2.792742	2.787491	2.777074	2.777075	2.747301

TABLE A.2: Simulation results for Version 2 of the CMOS inverter-based amplifier design.

A.3 Version 3

The third version fixed the biasing of the active resistors, addressing the issues found in the previous version.
Figure A.3 shows the schematic of Version 3. The simulation results for this version are summarized in Table A.3.

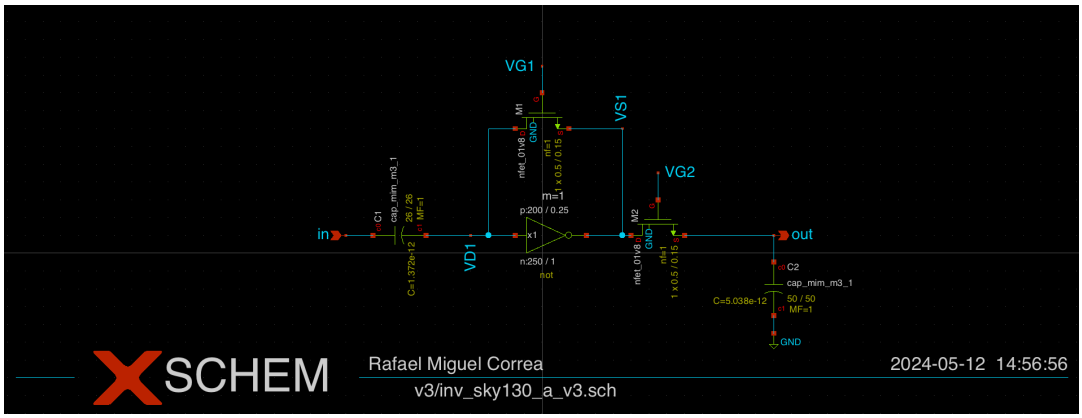

FIGURE A.3: Schematic of Version 3 of the CMOS inverter-based amplifier design.

Vdd	1.125	1.125	1.125	1.125
Wn	250.0	250.0	250.0	250.0
Ln	1.0	1.0	1.0	1.0
Wp	200.0	200.0	200.0	200.0
Lp	0.25	0.25	0.25	0.25
R1_Wn	0.5	0.5	0.5	0.5
R1_Ln	0.15	0.15	0.15	0.15
R1_Vg	0.714	0.714	0.725	0.725
R2_Wn	0.5	0.5	0.5	0.5
R2_Ln	0.15	0.15	0.15	0.15
R2_Vg	1.14439	1.1	1.125	1.085
Wc1	26.0	26.0	26.0	26.0
Lc1	26.0	26.0	26.0	26.0
MFc1	1.0	1.0	1.0	1.0
C1 (in pF)	1.37176	1.37176	1.37176	1.37176
Wc2	50.0	20.0	50.0	50.0
Lc2	50.0	20.0	50.0	50.0
MFc2	1.0	1.0	1.0	1.0
C2 (in pF)	5.038	0.8152	5.038	5.038
Vdc (in mV)	514.39	514.39	514.39	514.39
gain (in dB)	20.89119	20.8918	20.91812	20.90814
lower cut-off frequency (in Hz)	3.732502	3.732502	9.749896	9.727472
upper cut-off frequency (in Hz)	9527.962	18450.15	14487.72	5345.644
noise in (uV)	5.459399	6.092658	5.358833	5.698832
power (in uW)	3.089187	3.089179	3.115257	3.11526

TABLE A.3: Simulation results for Version 3 of the CMOS inverter-based amplifier design.

A.4 Version 4

This version used a CMOS capacitor to further reduce the size of the design, optimizing the layout and performance. The schematic of Version 4 is the one in Figure 3.1. The simulation results for this version are summarized in Table A.4.

Vdd	1.125	1.125	1.125	1.125	1.125
Wn	250.0	250.0	250.0	250.0	250.0
Ln	1.0	1.0	1.0	1.0	1.0
nf_n	1.0	1.0	1.0	1.0	10.0
Wp	200.0	200.0	200.0	200.0	200.0
Lp	0.25	0.25	0.25	0.25	0.25
nf_p	1.0	1.0	1.0	1.0	8.0
R1_Wn	0.5	0.5	0.5	0.5	0.5
R1_Ln	0.15	0.15	0.15	0.15	0.15
R1_Vg	0.725	0.725	0.725	0.725	0.725
R2_Wn	0.5	0.5	0.5	0.5	0.5
R2_Ln	0.15	0.15	0.15	0.15	0.15
R2_Vg	1.125	1.1	1.085	1.085	1.085
Wc1	26.0	26.0	26.0	26.0	26.0
Lc1	26.0	26.0	26.0	26.0	26.0
MFc1	1.0	1.0	1.0	1.0	1.0
C1 (in pF)	1.37176	1.37176	1.37176	1.37176	1.37176
C2_Wn	250.0	125.0	100.0	100.0	100.0
C2_Ln	10.0	10.0	10.0	10.0	10.0
nf_c2	1.0	1.0	1.0	1.0	4.0
Vdc (in mV)	514.39	514.39	514.39	484.24	487.31
gain (in dB)	20.90851	20.90953	20.90647	20.90647	20.89885
lower cut-off frequency (in Hz)	9.727472	9.727472	9.727472	9.727472	8.87156
upper cut-off frequency (in Hz)	5248.075	5675.446	4819.478	4819.478	4375.221
noise in (uV)	5.360154	5.529244	5.699024	5.699024	5.751697
power (in uW)	3.115279	3.115264	3.115261	3.115261	3.115261

TABLE A.4: Simulation results for Version 4 of the CMOS inverter-based amplifier design.

Appendix B

Documentation of the Design Process

B.1 Overview

This appendix provides an overview of how the design process for the CMOS inverter-based amplifier was meticulously documented in the project's wiki [**ethz_BEL_wiki**]. The wiki serves as a comprehensive resource, offering detailed information on the workflow, tools, and methodologies employed throughout the project. It guides users through every phase of the design, from the initial concept to the final conclusions, ensuring that future designers can replicate and build upon this work.

B.2 Wiki Page Structure and Contents

The main page of the Open-source IC Design (OSICD) wiki is designed to be user-friendly and informative, providing a clear roadmap of the project. The wiki is organized into several key subpages:

- OSICD - Introduction
- OSICD - Workflow
- OSICD - Tools Presentation and Installation
- OSICD - CMOS Inverter-Based Amplifier
- OSICD - Conclusion
- OSICD - Glossary
- OSICD - Appendices

The content of the wiki mirrors the structure of this report but is presented in a more didactic and user-friendly way, making it accessible for new users and enhancing the learning experience.

B.3 Purpose and Benefits of the Wiki Documentation

The primary purpose of the wiki documentation is to create a comprehensive and accessible resource for future designer within the BEL group. By meticulously documenting each stage of the design process, the wiki ensures that the knowledge

gained during this project is preserved and can be leveraged by others. The benefits of this documentation include:

- **Educational Resource:** The wiki serves as a detailed educational guide for students and researchers new to IC design.
- **Knowledge Sharing:** By making the design process transparent, the wiki promotes knowledge sharing and collaboration within the open-source community.
- **Replication and Improvement:** Future projects can replicate the design process and build upon the work done, leading to continuous improvement and innovation.
- **Troubleshooting and Support:** Detailed documentation helps in troubleshooting issues and provides support to users facing similar challenges.

In conclusion, the documentation of the design process in the wiki not only supports this project but also contributes significantly to the open-source IC design knowledge within the BEL group.

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