schematic of cell "NOR" design "Non overlapping clock"

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Vdd

Mp2
PMOS25
TW=1.5u
fw=1.5u
l=250n
fingers=1
m=1

A
2.5v

Mp1
PMOS25
TW=1.5u
fw=1.5u
l=250n
fingers=1
m=1

B
2.5v

Out

Mn1
NMOS25
TW=1.5u
fw=1.5u
l=250n
fingers=1
m=1

A
2.5v

gnd

Mn2
NMOS25
TW=1.5u
fw=1.5u
l=250n
fingers=1
m=1

B
2.5v

gnd