Design and Analysis of Two-Stage CMOS Operational Amplifier Using eSim

Mihir Kumar Behera
Dept. of Electronics and Communication Engineering
National Institute of Technology, Rourkela
mihir79kumar@gmail.com

***Abstract*—This paper presents the design and analysis of a two-stage CMOS operational amplifier implemented using the eSim–Ngspice environment at a 1.8 V supply voltage. The circuit ensures all MOSFETs operate in the saturation region to achieve high output impedance, stable transconductance, and enhanced overall gain. The amplifier achieves a DC gain between 90 dB and 100 dB and a phase margin of approximately 60°, meeting the targeted design specifications for stability and bandwidth.**

***Index Terms*—CMOS Op-Amp, Two-Stage Amplifier, Gain Bandwidth Product, Phase Margin**

I. Circuit Design and Analysis

The designed circuit is a two-stage CMOS operational amplifier implemented in eSim–Ngspice with a 1.8 V supply. All MOSFETs are biased in saturation to ensure high output resistance and stable transconductance, which together contribute to high voltage gain. The MOSFETs used as current sources, especially M7 and M8, act as high-impedance loads that enhance the amplifier's gain. The operation of the circuit is governed by trade-offs between gain, bandwidth, and slew rate, adjusted through transistor sizing and bias current.

The first stage consists of transistors M1, M2, M3, M4, and M8, forming a differential amplifier with active load configuration. It converts the differential input into a single-ended output while providing high gain. M1 and M2 constitute the input differential pair and set the input common-mode range. M4 and M5 serve as active loads providing high output resistance, and M8 acts as a tail current source that determines the bias current and minimum input common-mode level. The gain of this stage depends on the transconductance of M1 and M2 and the output resistance of M4 and M5. Increasing the bias current improves the slew rate but reduces gain, as $A_v \approx g_m/\lambda I_D$. Increasing the aspect ratio of M3 and M4 yields higher gain and bandwidth while maintaining saturation.

The second stage, consisting of M3 and M6, forms a PMOS common-source amplifier with active NMOS load. This stage boosts the signal amplitude and output swing. A 600 fF compensation capacitor between stages stabilizes the amplifier and sets the dominant pole. The 2 pF load capacitor models the output load and affects the gain-bandwidth product (GBW). Simulation results show a practical DC gain between 90 dB and 100 dB and a phase margin around 60°, indicating a stable and well-compensated design. The theoretical gain is 70 dB, but channel-length modulation and improved load resistance contribute to higher practical gain.

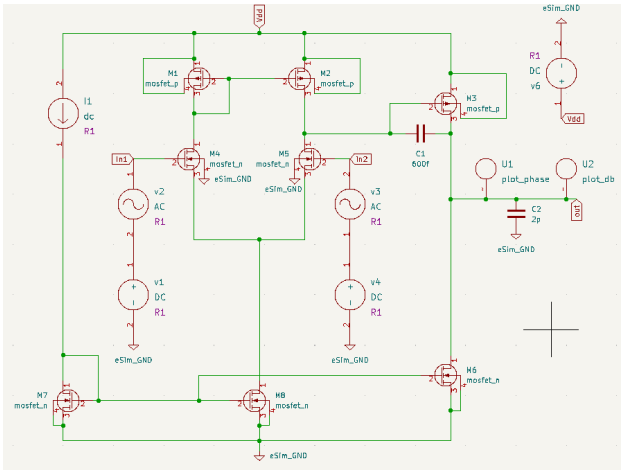

Fig. 1. Implemented two-stage CMOS op-amp circuit schematic.

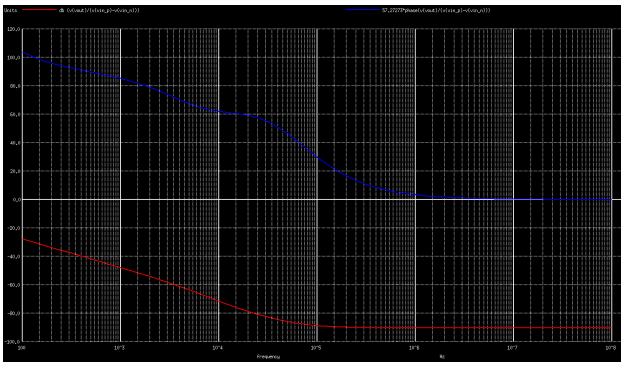

Fig. 2. Simulated output waveform showing op-amp gain and phase response.

Acknowledgment

The author would like to thank the FOSSEE eSim Team, IIT Bombay, for providing the open-source simulation platform and guidance under the FOSSEE Circuit Simulation Project initiative.

References

[1] S. K. M. Goswami, "DC Suppressed High-Gain Active CMOS Instrumentation Amplifier for Biomedical Application," available: *https://ieeexplore.ieee.org/document/5760217*.

[2] "Design of Two-Stage Operational Amplifier," available: *https://youtu.be/dTBUeugPxj0?si=VTuidje-rzb80taF*.