Design of a CMOS Two-Stage Miller-Compensated OTA: Stability and Performance Analysis

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Abstract- Operational Transconductance Amplifiers (OTAs) are fundamental building blocks in analog and mixed-signal systems, used in filters, converters, and sensor interfaces. A common approach for stabilizing two-stage OTAs is Miller compensation, where a capacitor is connected between the first-stage output and the amplifier output. This technique achieves stability through pole-splitting but introduces a right-half-plane zero, which can reduce phase margin and limit speed. In this project, a two-stage CMOS OTA with Miller compensation is designed and simulated. Key performance parameters such as DC gain, unity-gain bandwidth, slew rate, and stability are evaluated under low-voltage operation.

I. CIRCUIT DETAILS

The proposed design is a two-stage CMOS OTA with Miller compensation. In figure [2] the first stage is a differential pair M1–M2 with active loads M3–M4 and current mirror biasing (M5,M8,M7). The second stage uses M6 to provide additional gain and drive capability. A compensation capacitor Cc connects the first-stage output to the amplifier output, ensuring stability through pole-splitting. The OTA drives an external load capacitor C_L, achieving high DC gain, adequate bandwidth, and stable operation under low supply voltage.

The block level schematic of miller compensated is shown in figure [1] . The gm1 and gm2 are input and output stage of the OTA and gmf forms the feed-forward path from input to output node. R1 and R2 represents the node resistances, C1 and CL are the node capacitances of input and output stage, respectively.
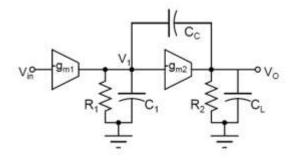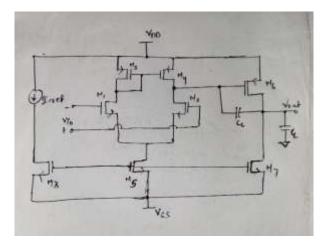

Figure 1 Block Diagram

Figure 2 Circuit Digram

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