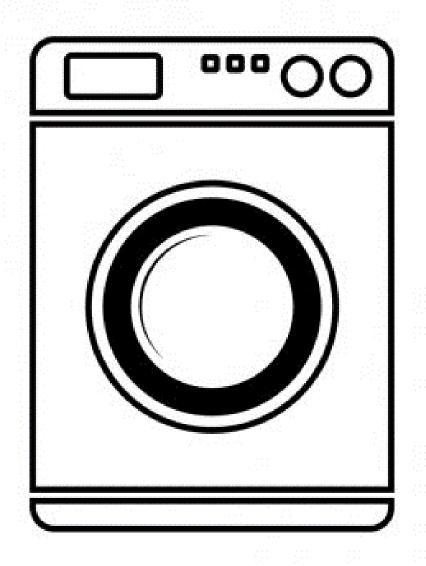
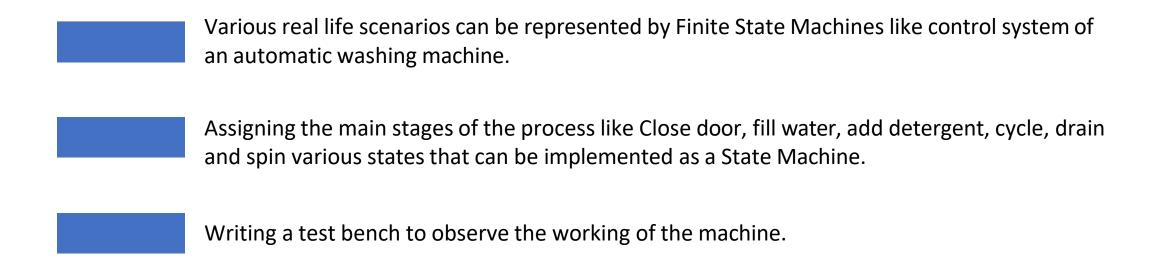
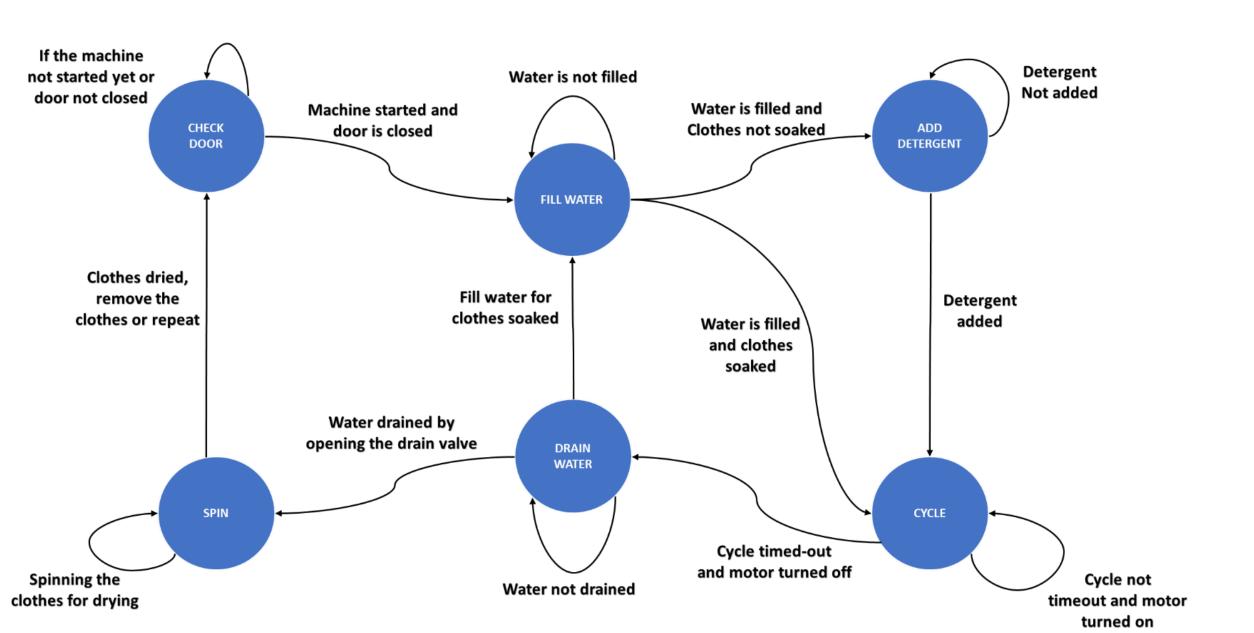
Automatic
Washing Machine
Control System
Using Verilog HDL

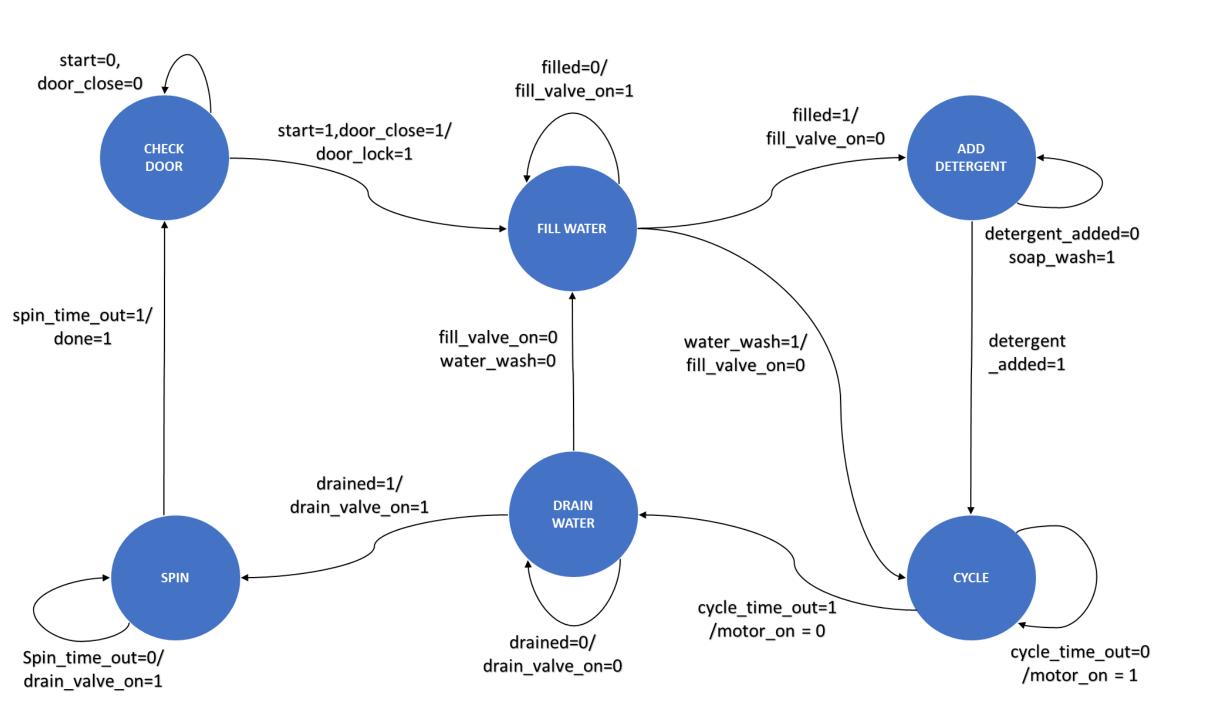


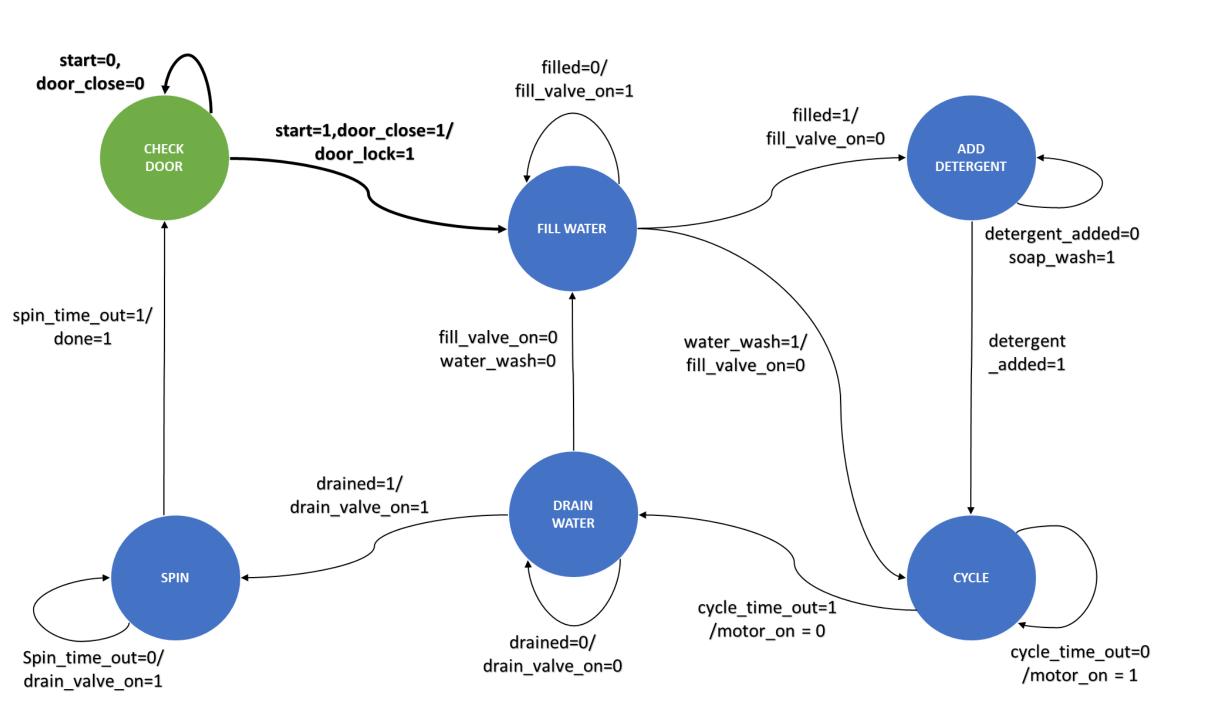
## **INTRODUCTION**

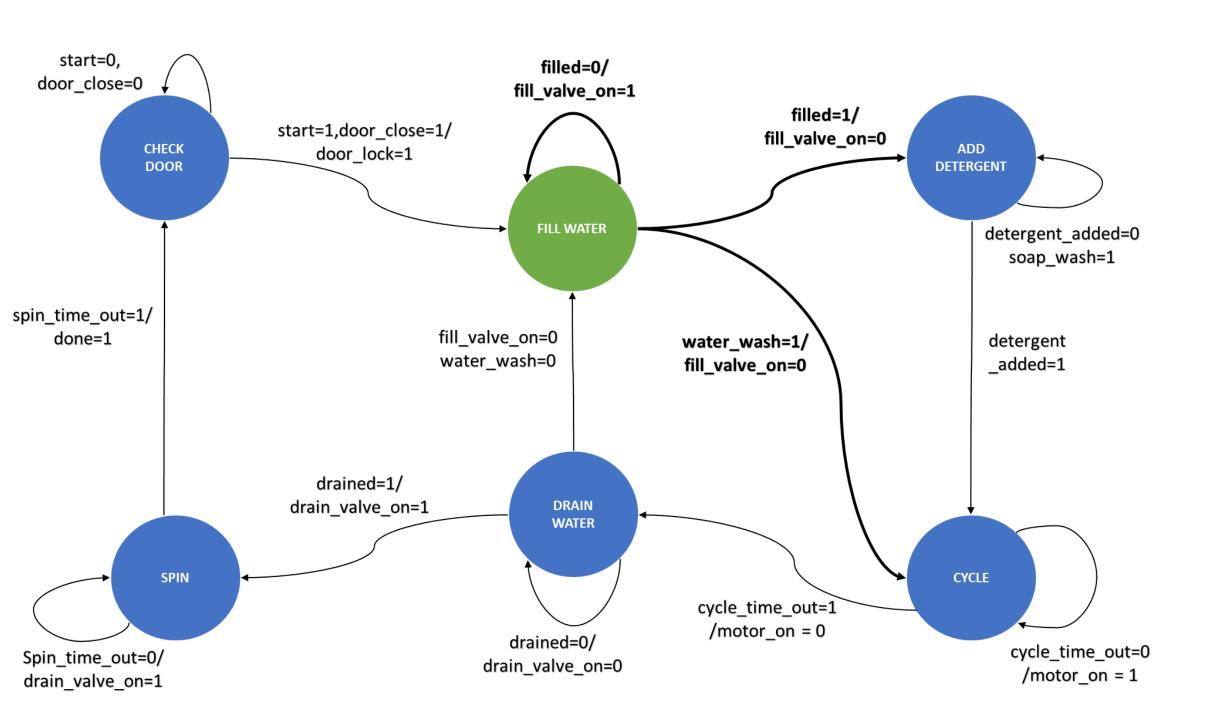


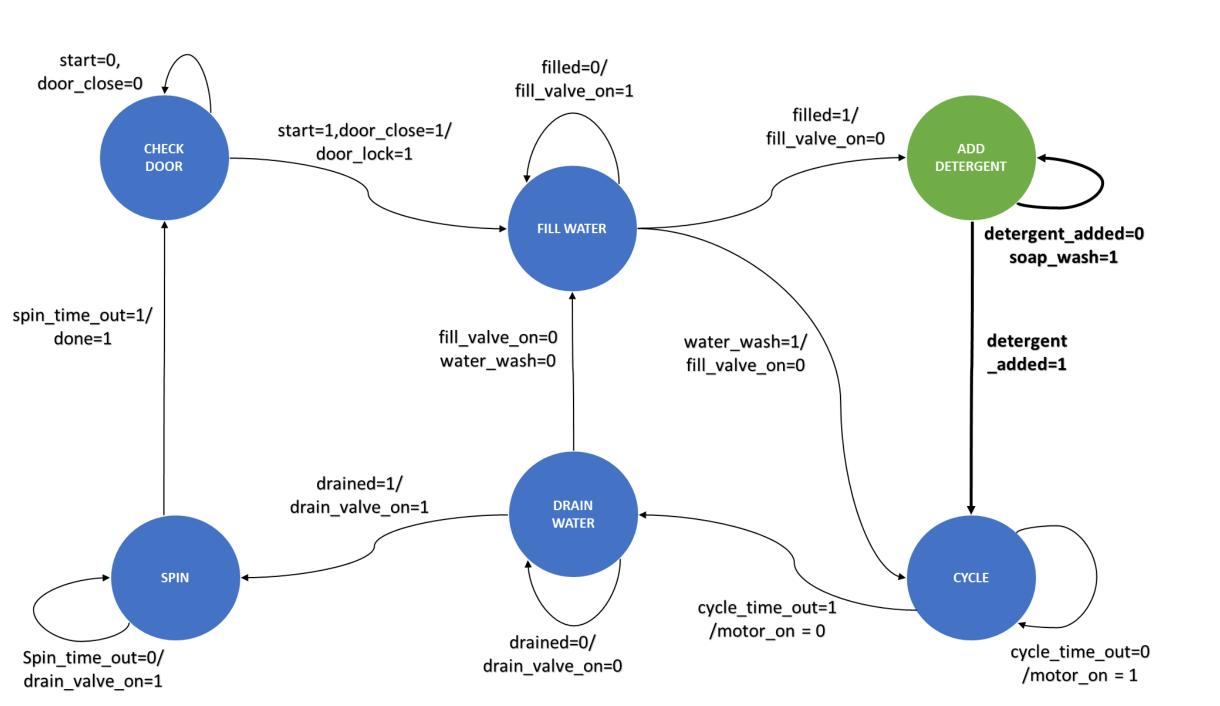
## STATE DIAGRAM

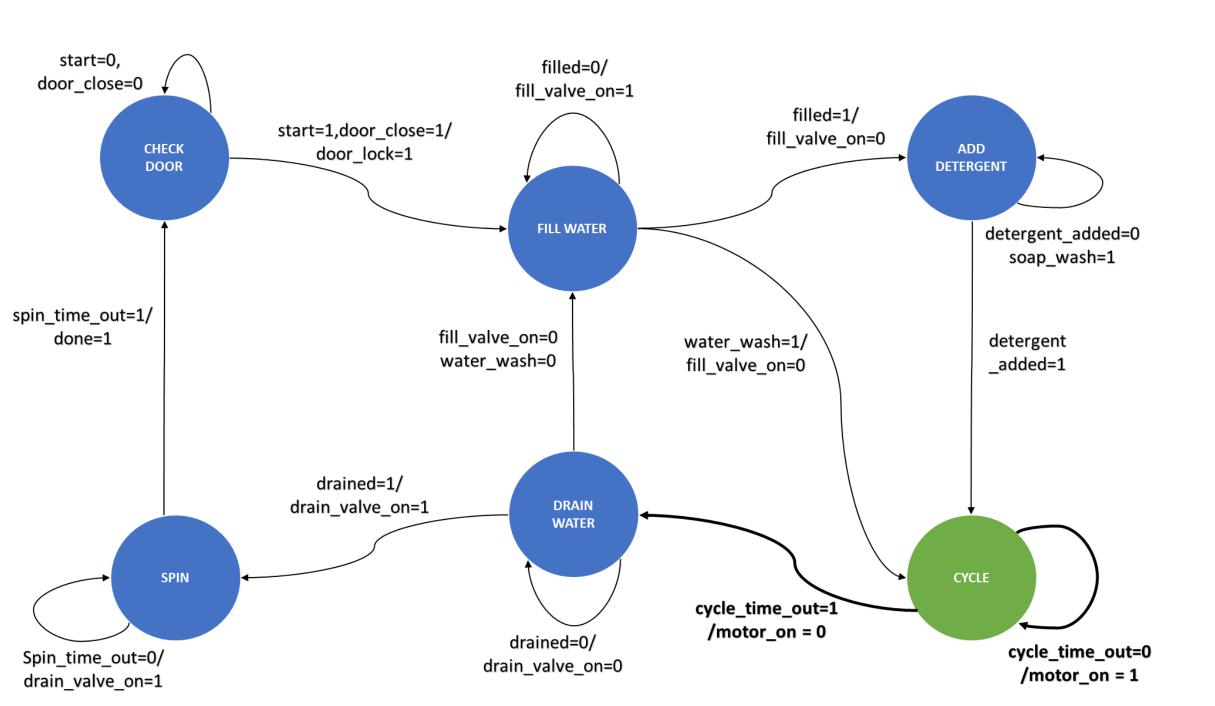


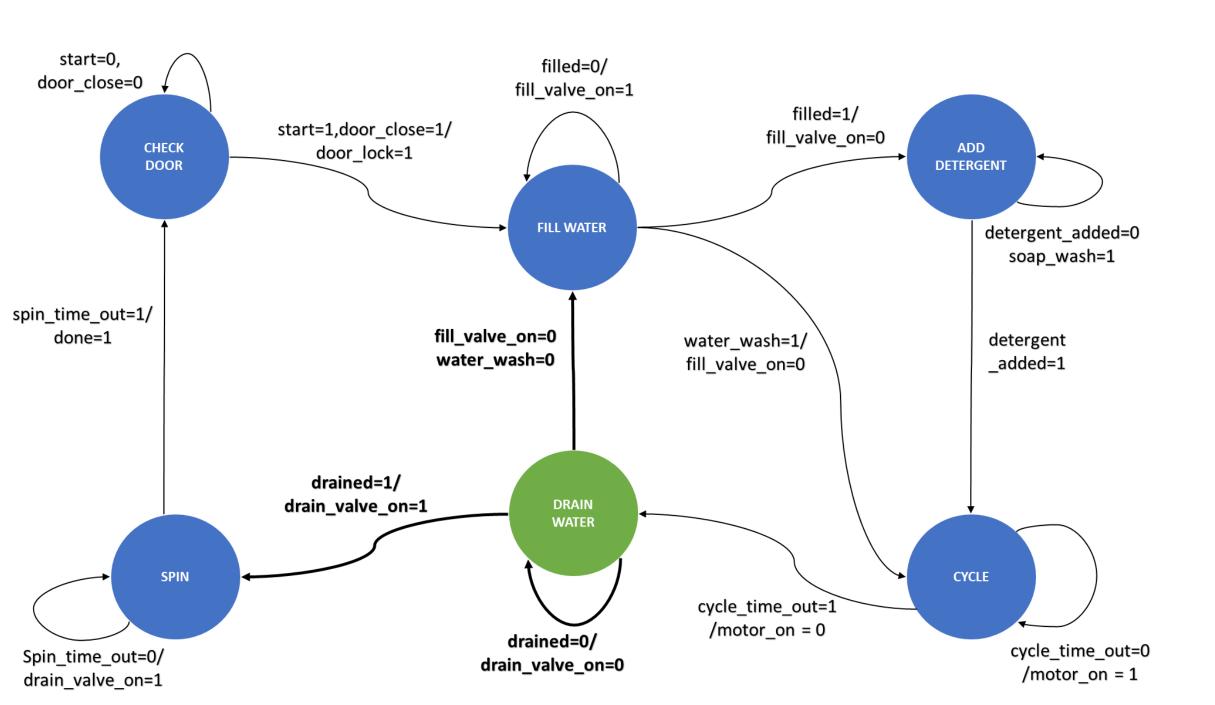


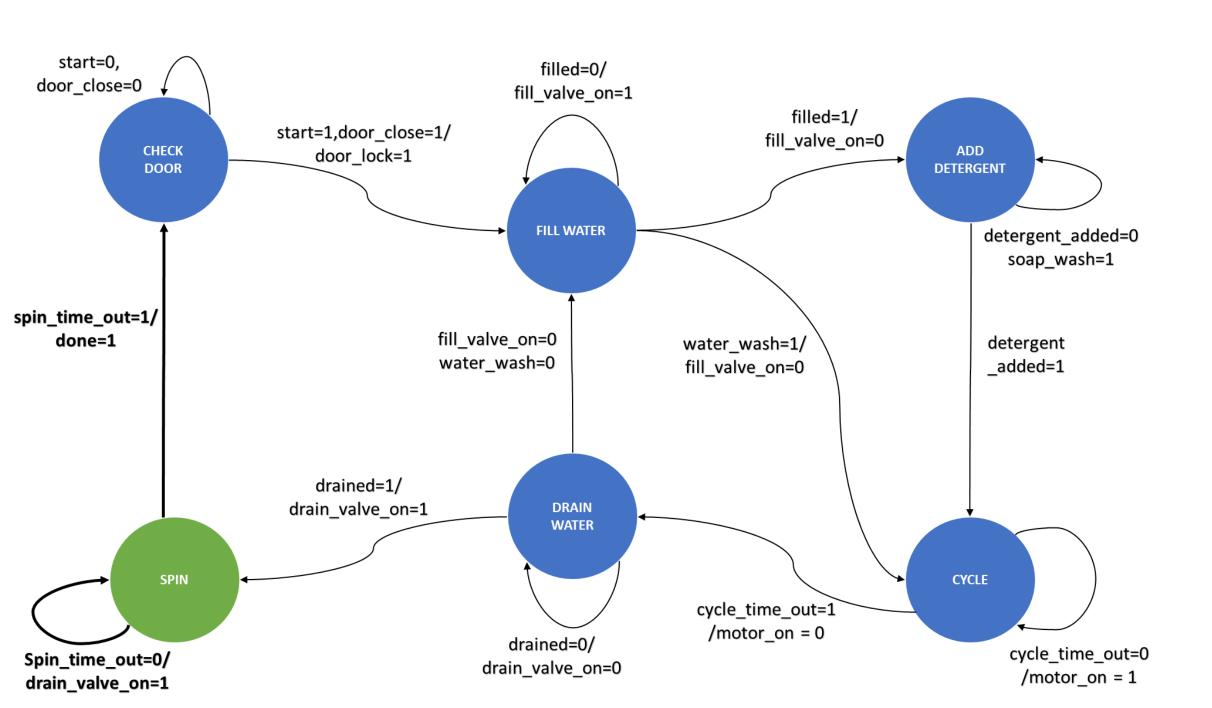












## RESULTS

```
PS D:\VS CODE\Verilog\WASHING MACHINE> iverilog -o test machine.v testbench.v
PS D:\VS CODE\Verilog\WASHING MACHINE> vvp test
VCD info: dumpfile washing machine.vcd opened for output.
Time=0 | State: door lock=0, motor on=0, fill valve=0, drain valve=0, soap=0, water=0, done=0
Time=20 | State: door lock=1, motor on=0, fill valve=0, drain valve=0, soap=0, water=0, done=0
Time=25 | State: door_lock=1, motor_on=0, fill_valve=1, drain_valve=0, soap=0, water=0, done=0
Time=40 | State: door lock=1, motor on=0, fill valve=0, drain valve=0, soap=1, water=0, done=0
Time=65 | State: door lock=1, motor on=1, fill valve=0, drain valve=0, soap=1, water=0, done=0
Time=90 | State: door lock=1, motor on=0, fill valve=0, drain_valve=0, soap=1, water=0, done=0
Time=95 | State: door lock=1, motor on=0, fill valve=0, drain valve=1, soap=1, water=0, done=0
Time=115 | State: door lock=1, motor on=0, fill valve=0, drain valve=0, soap=1, water=1, done=0
Time=145 | State: door lock=1, motor on=0, fill valve=0, drain valve=0, soap=1, water=1, done=1
Time=155
          State: door lock=1, motor on=0, fill valve=0, drain valve=0, soap=0, water=0, done=0
Time=165 | State: door lock=1, motor on=0, fill valve=0, drain valve=0, soap=1, water=0, done=0
Time=205
          State: door lock=1, motor on=0, fill valve=0, drain valve=0, soap=1, water=1, done=0
Time=235 | State: door_lock=1, motor_on=0, fill_valve=0, drain_valve=0, soap=1, water=1, done=1
testbench.v:34: $finish called at 240 (1s)
```

## THANK YOU