PROJECT – 2B

EEE 234

Project 2B

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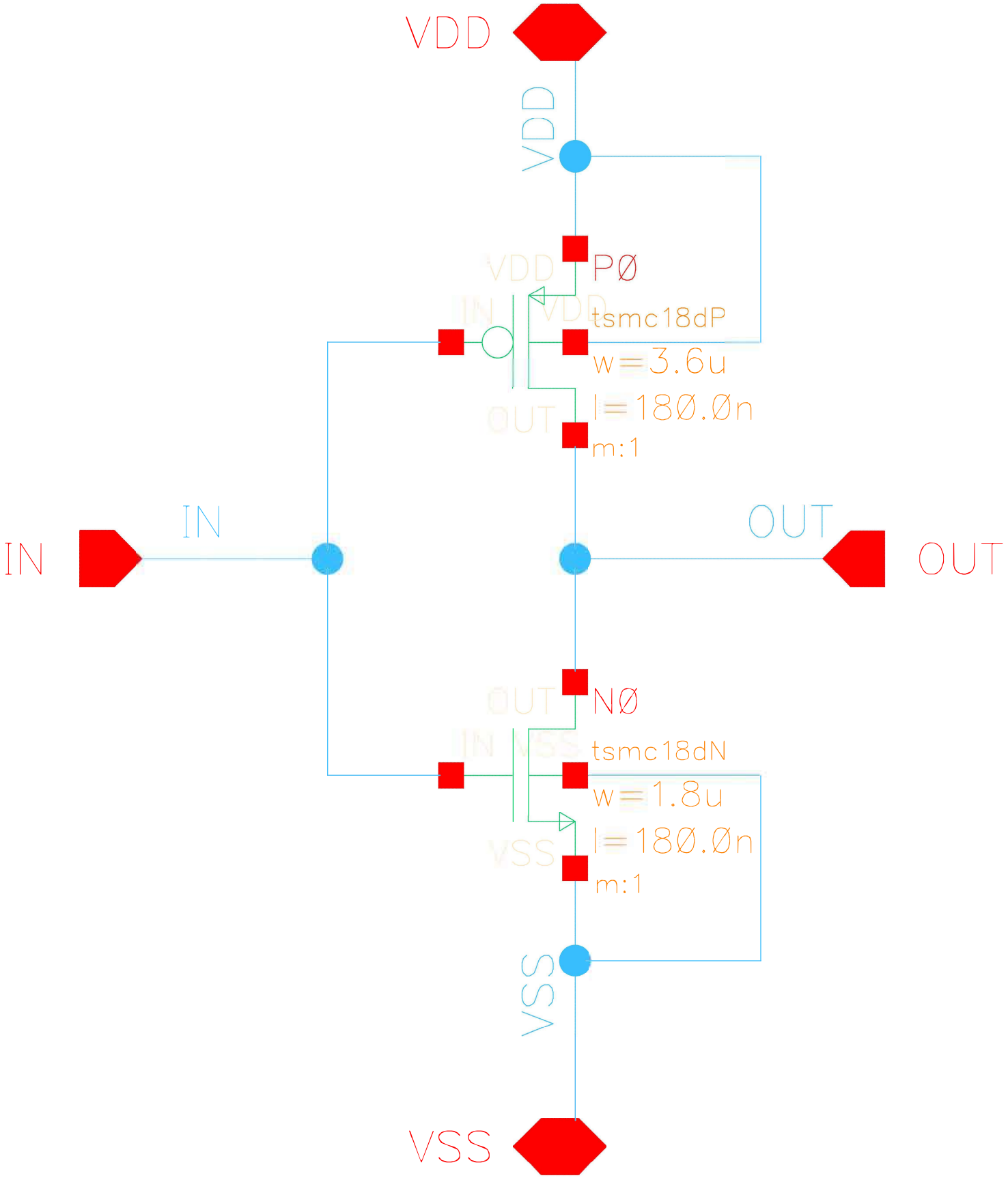
TABLE OF CONTENTS

Inverter

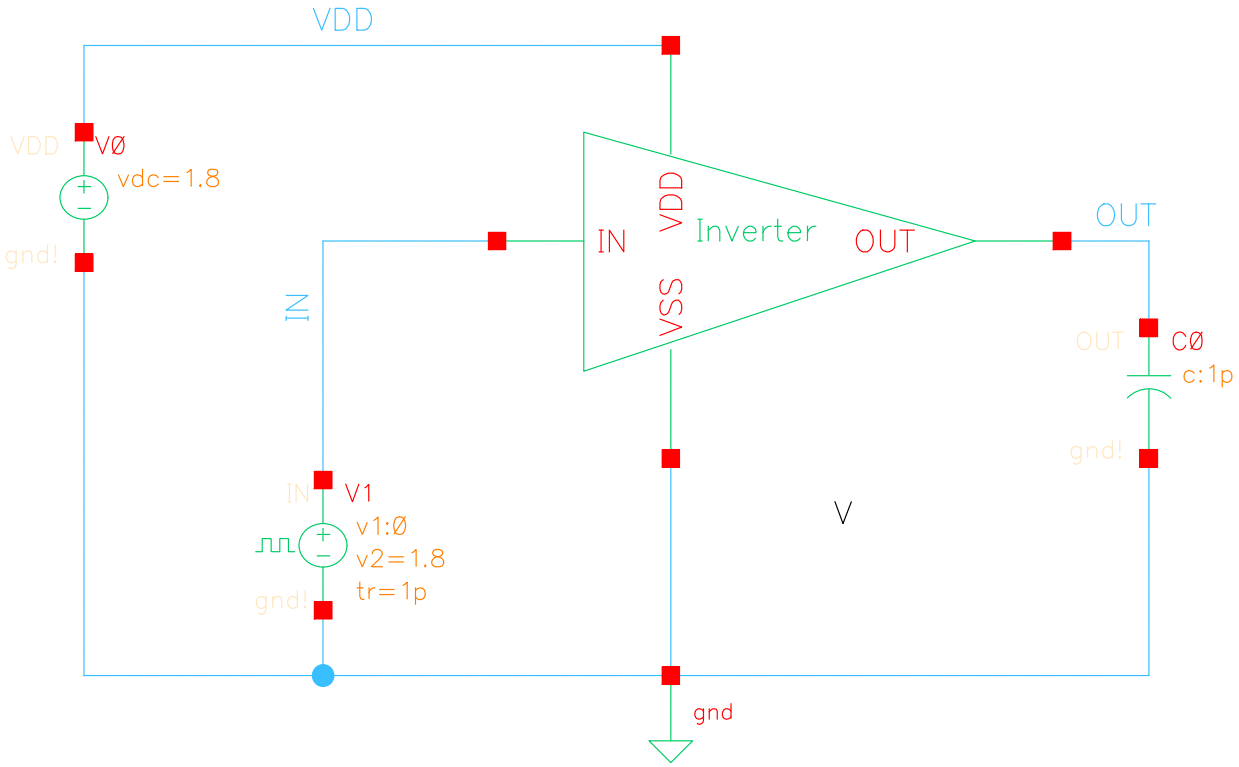
$(W/L)_n = 1.8/0.18$

$(W/L)_p = 3.6/0.18$

Schematic (Inverter)

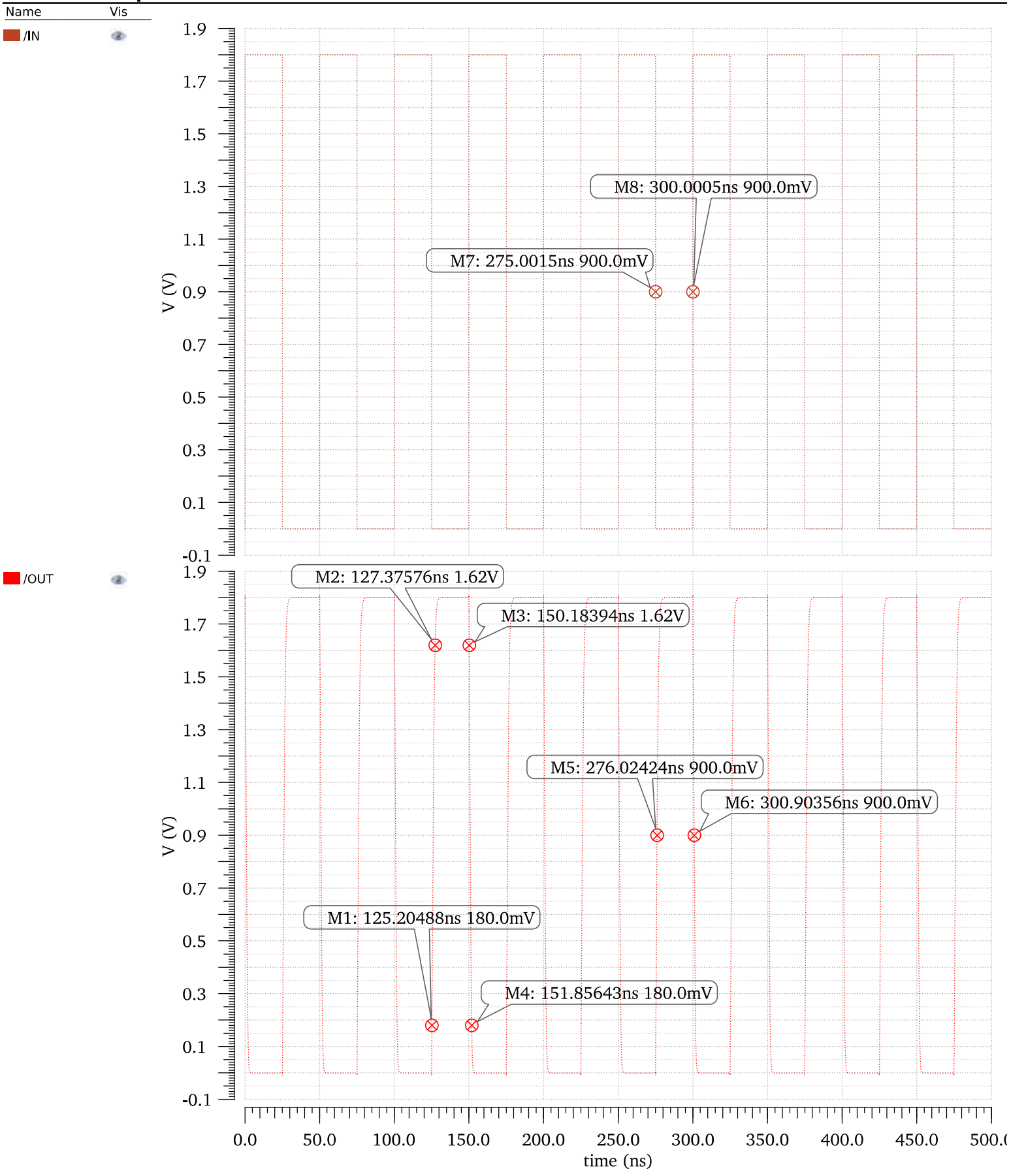


Testbench (Inverter)



Transient Response

Sun Oct 7 20:43:09 2018

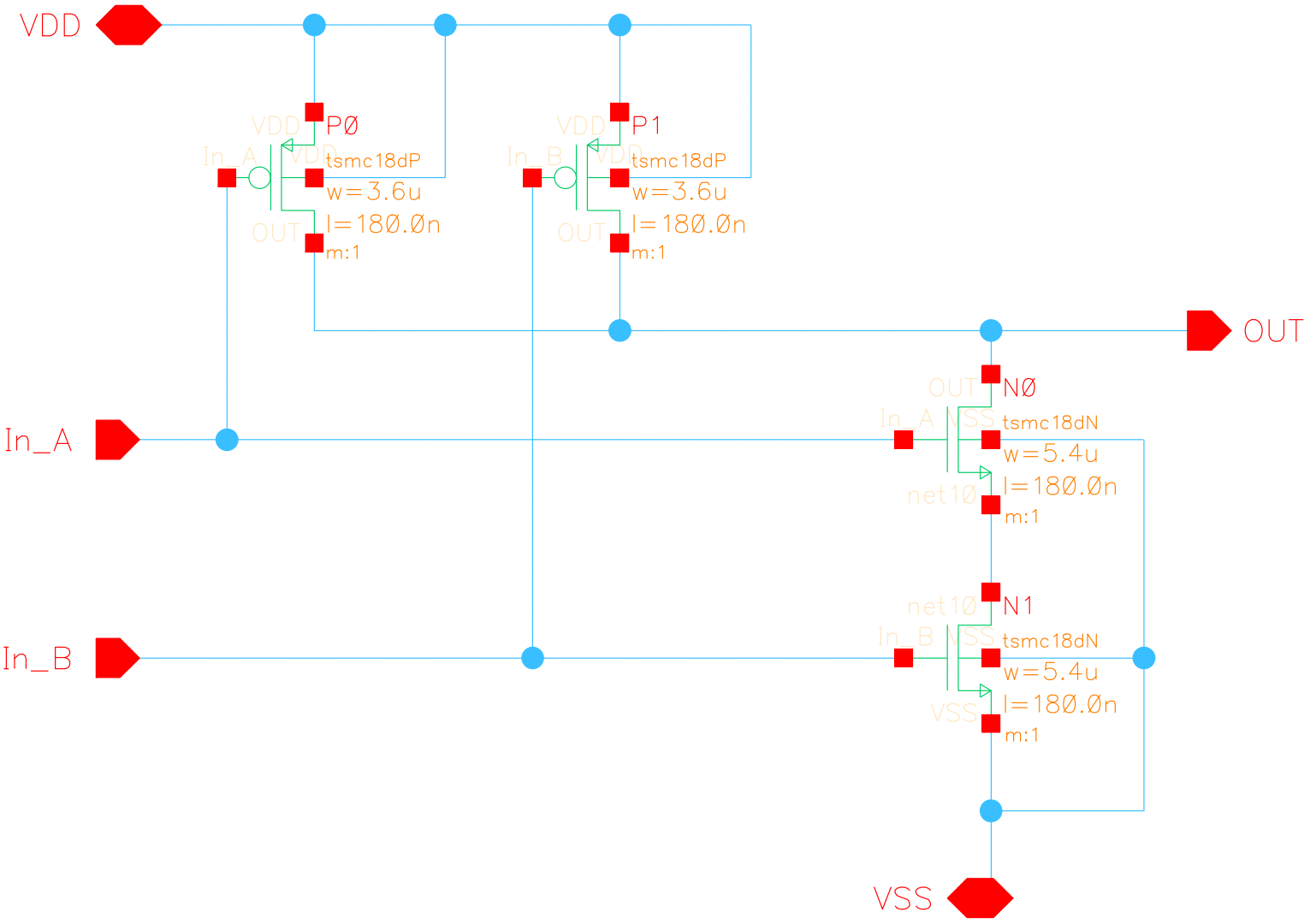


2-input
NAND gate

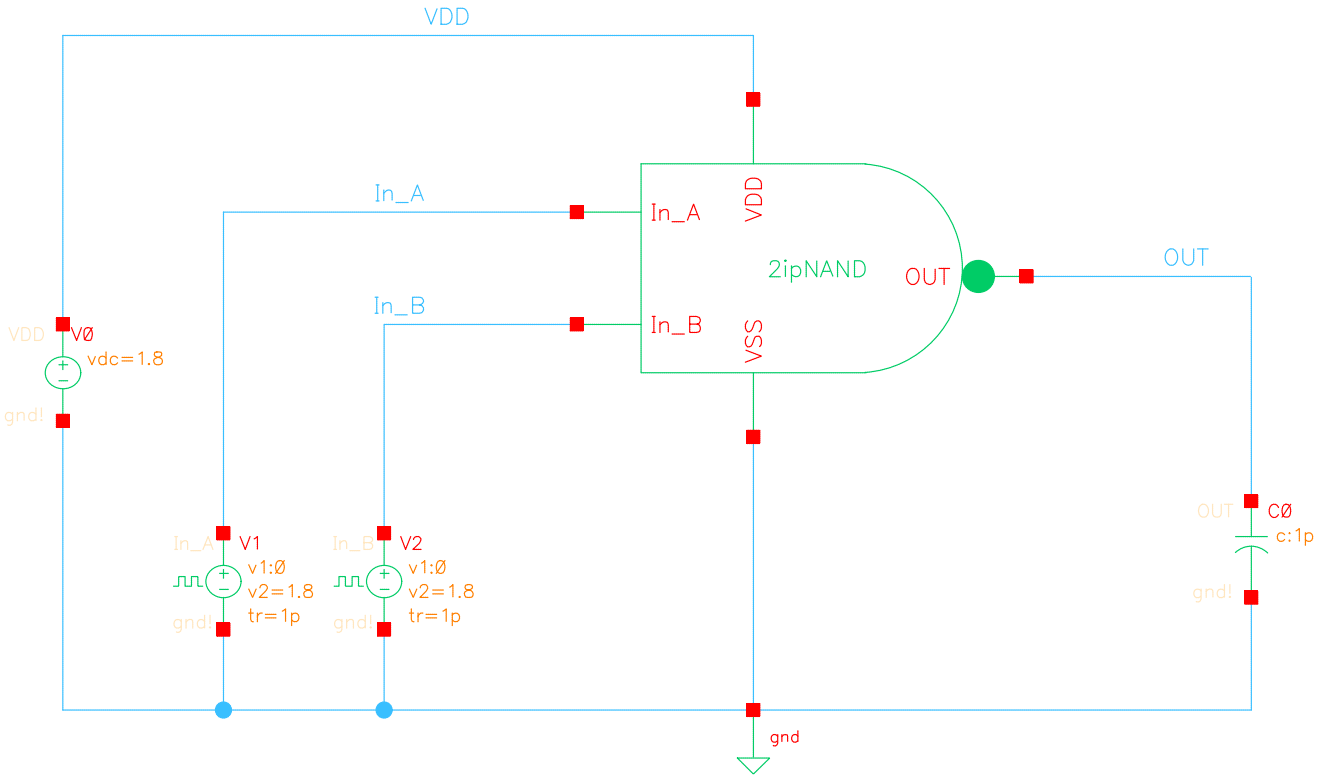
$(W/L)_n = 5.4/0.18$

$(W/L)_p = 3.6/0.18$

Schematic (2-input NAND gate)

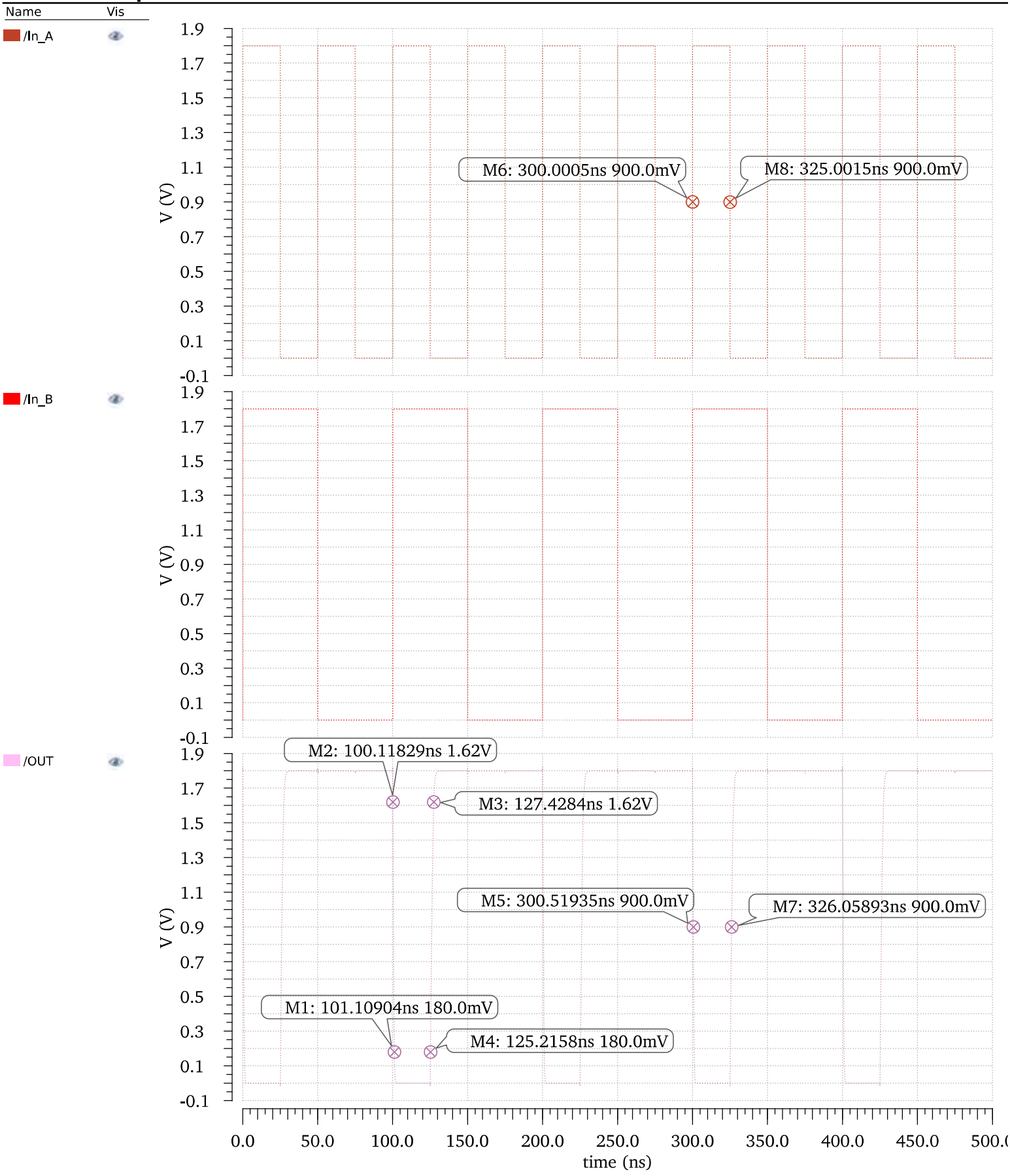


Tesbench (2-input NAND gate)



Transient Response

Sun Oct 7 20:34:47 2018

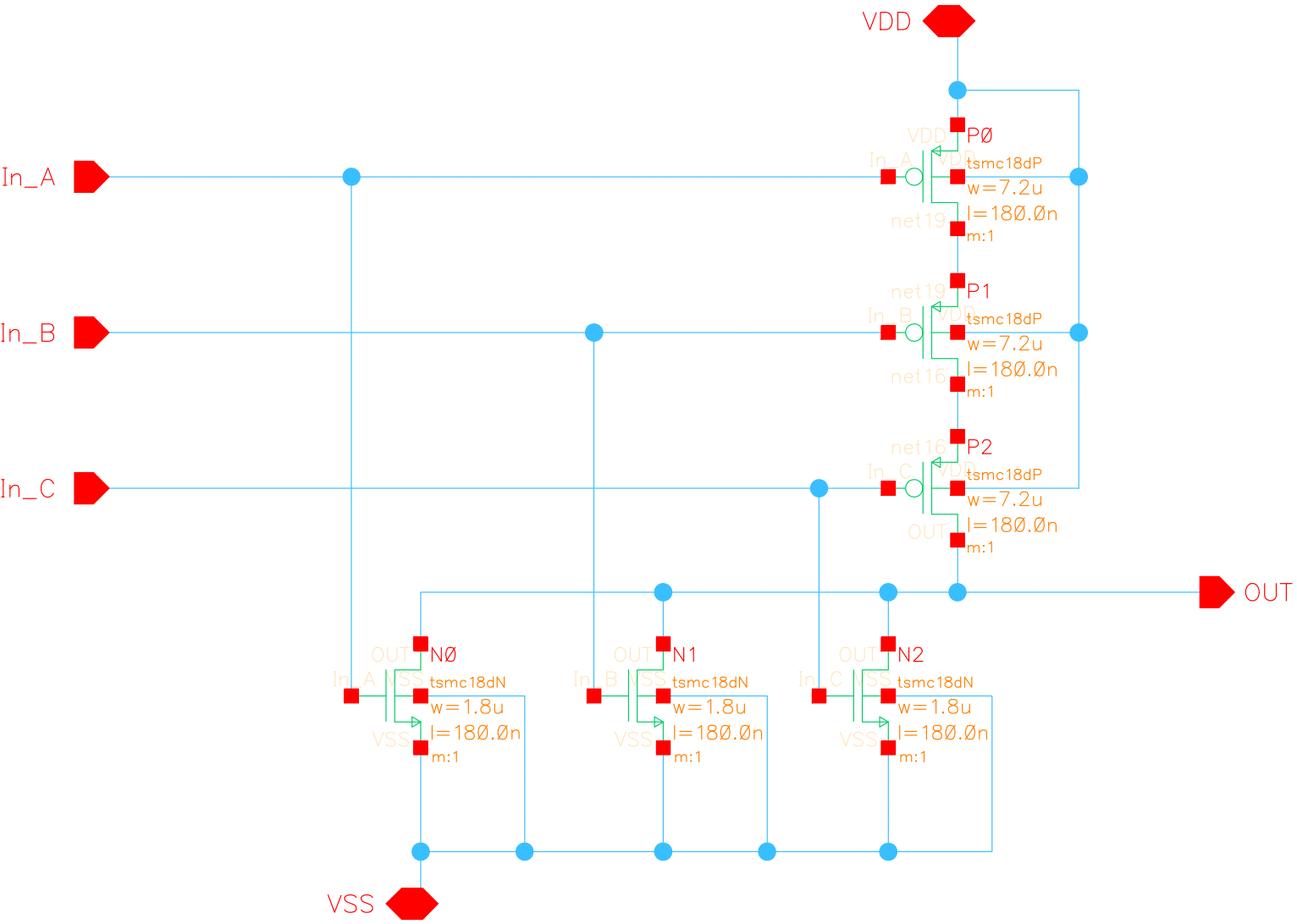


3-input NOR gate

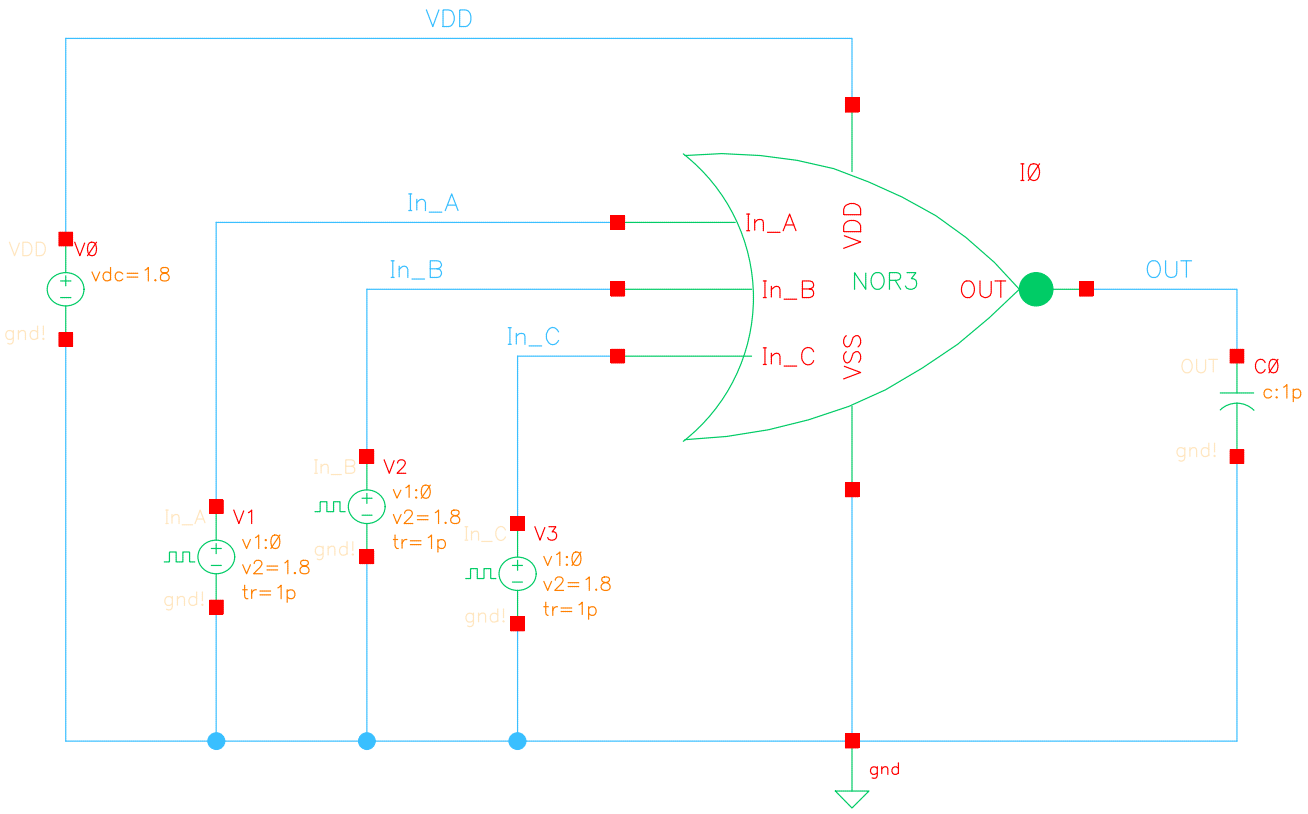
$(W/L)_n = 1.8/0.18$

$(W/L)_p = 7.2/0.18$

Schematic (3-input NOR gate)

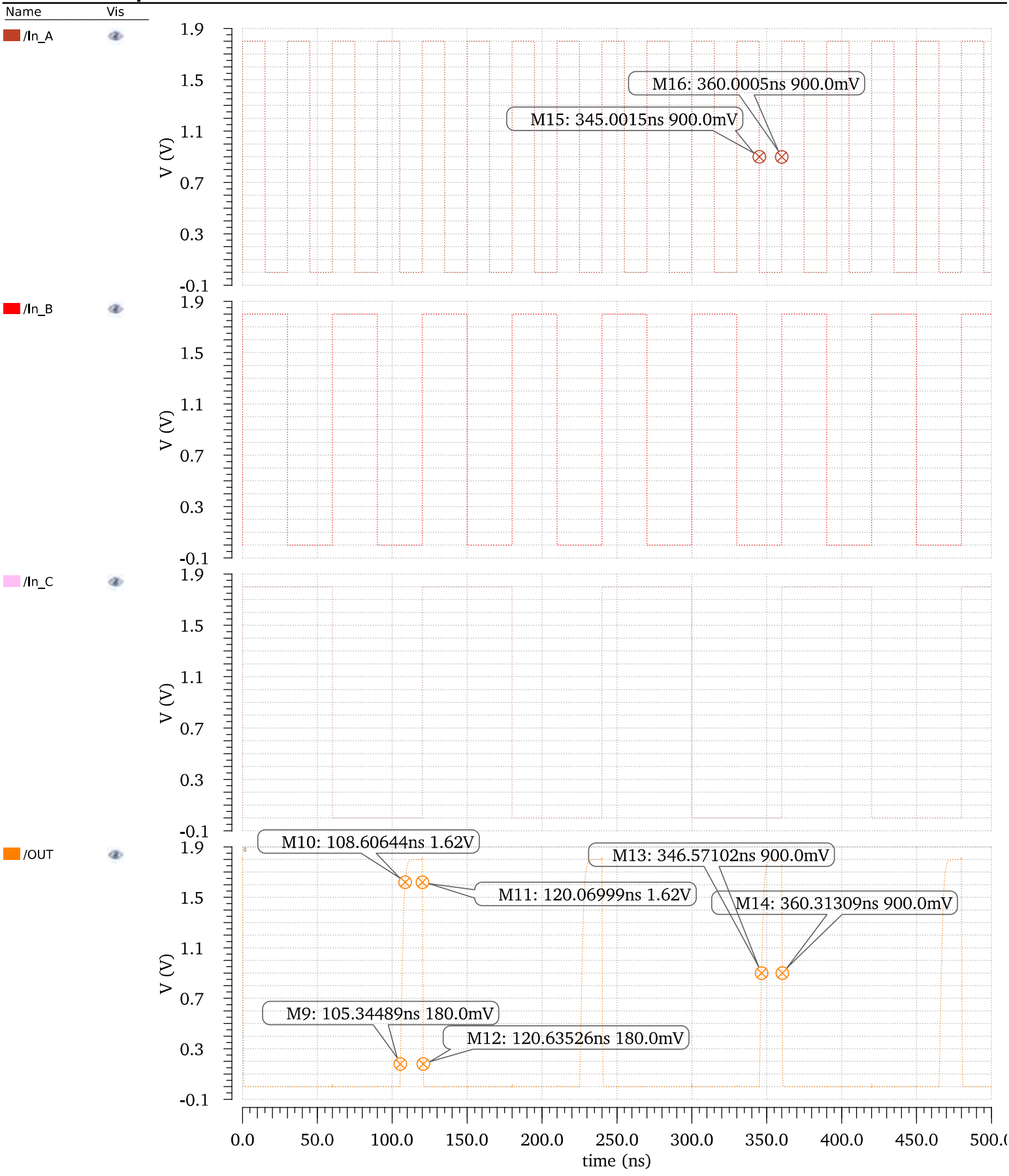


Testbench (3-input NOR gate)



Transient Response

Sun Oct 7 20:24:44 2018

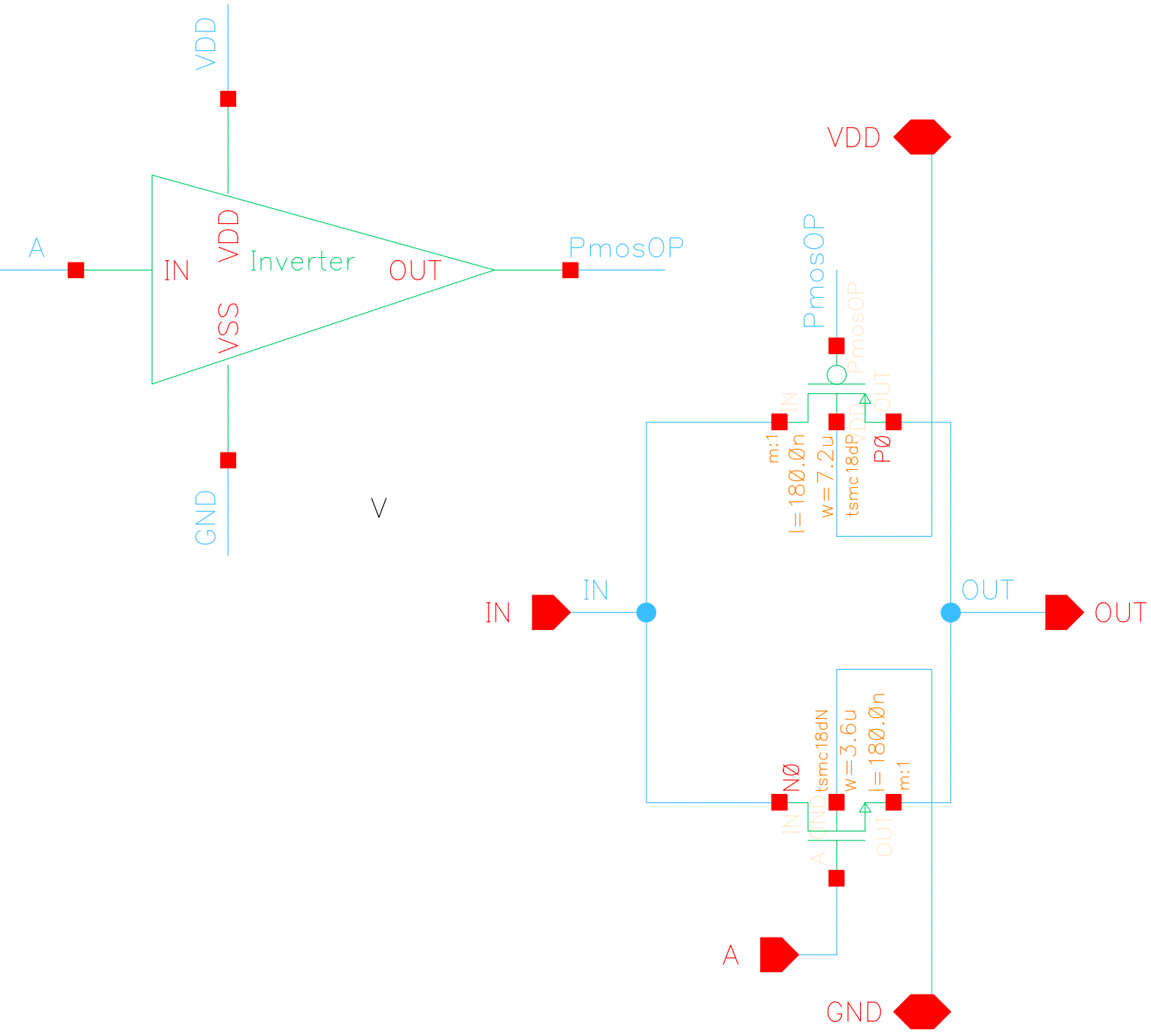


Transmission Gate

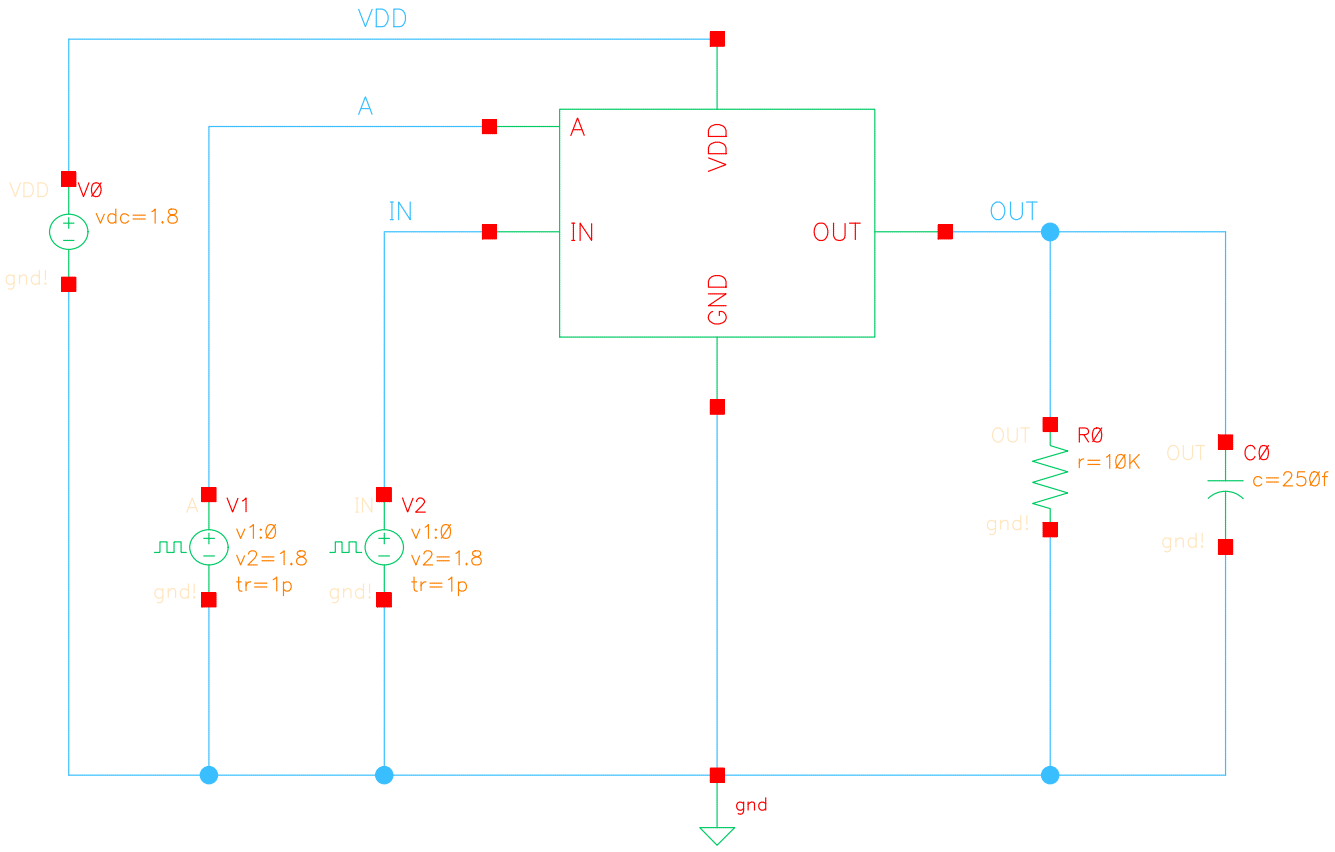
$(W/L)_n = 1.8/0.18$

$(W/L)_p = 3.6/0.18$

Schematic (Transmission Gate)

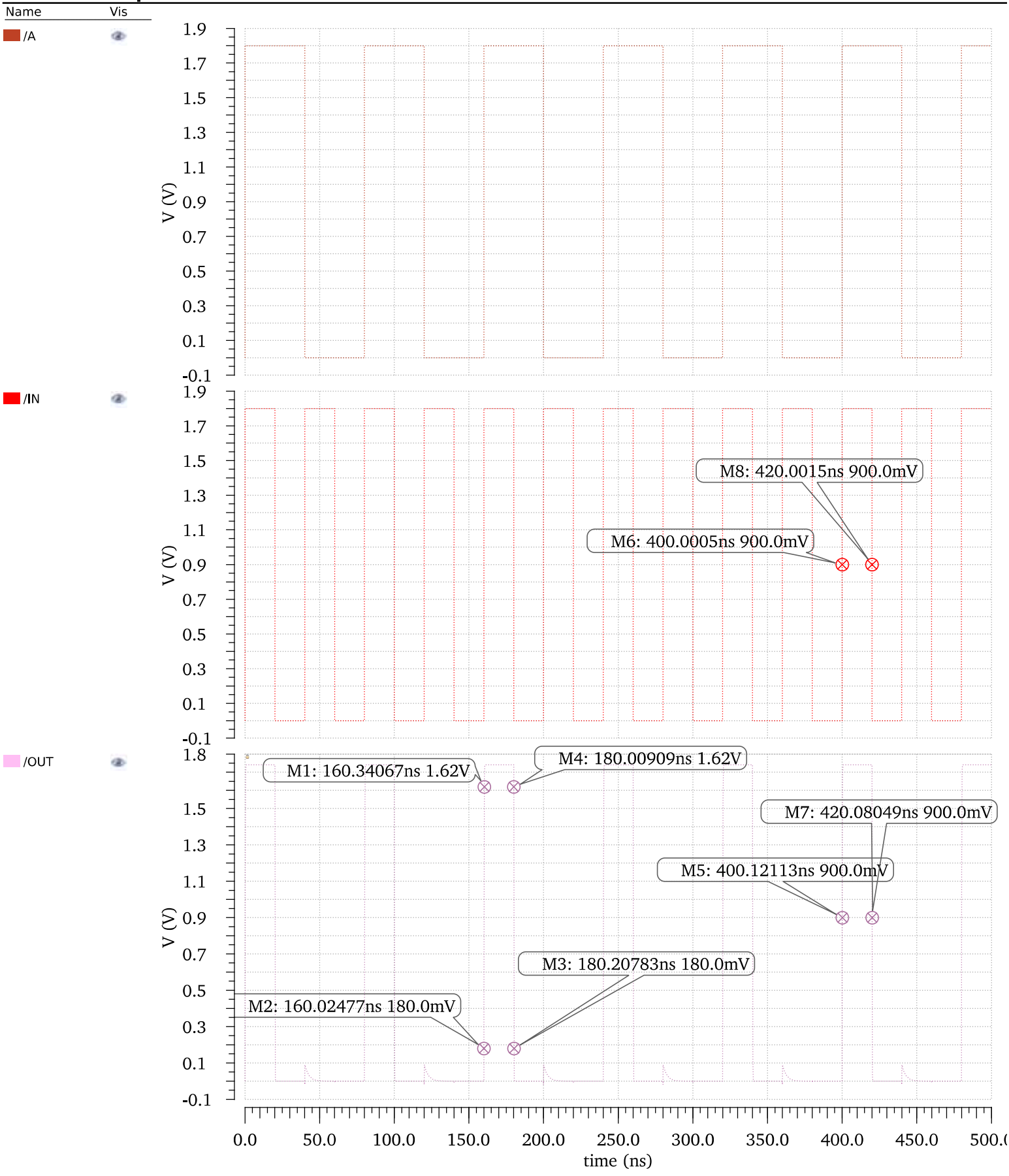


Test bench (Transmission Gate)



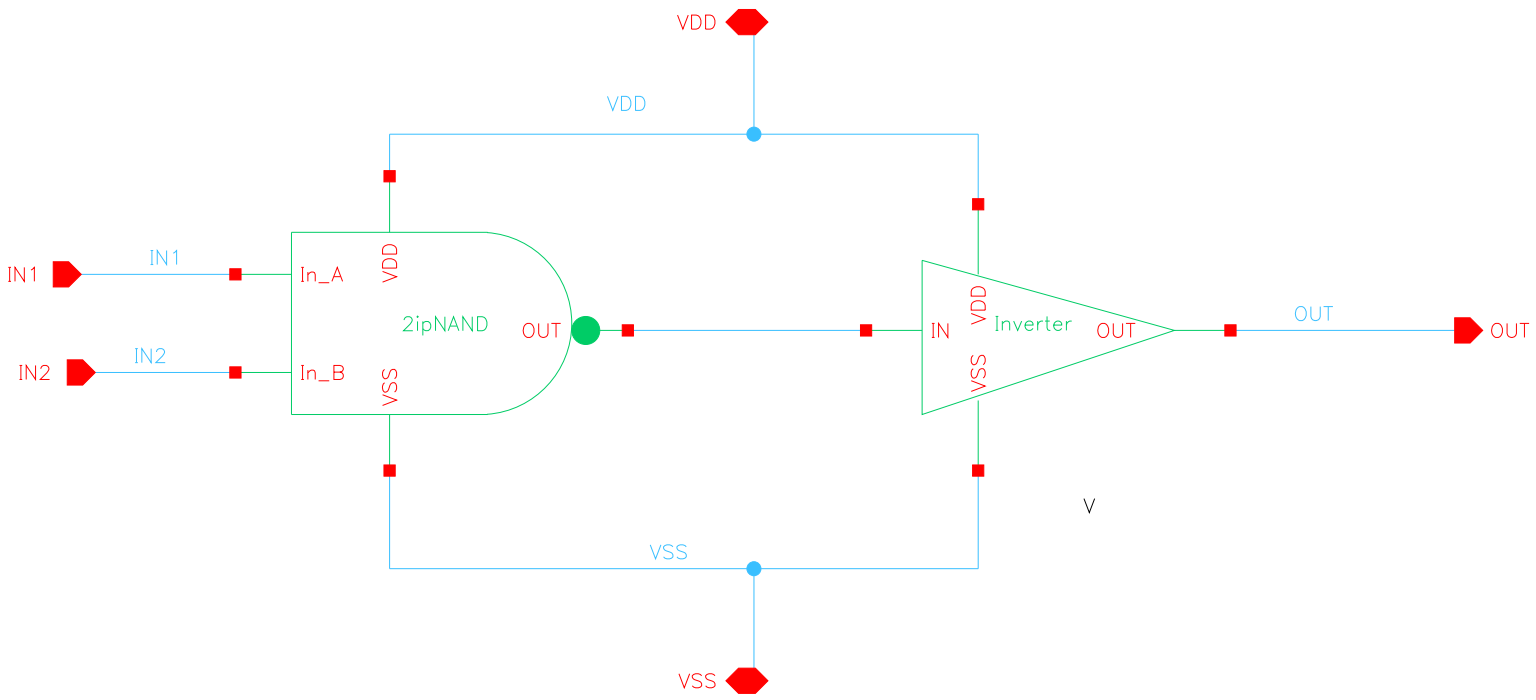
Transient Response

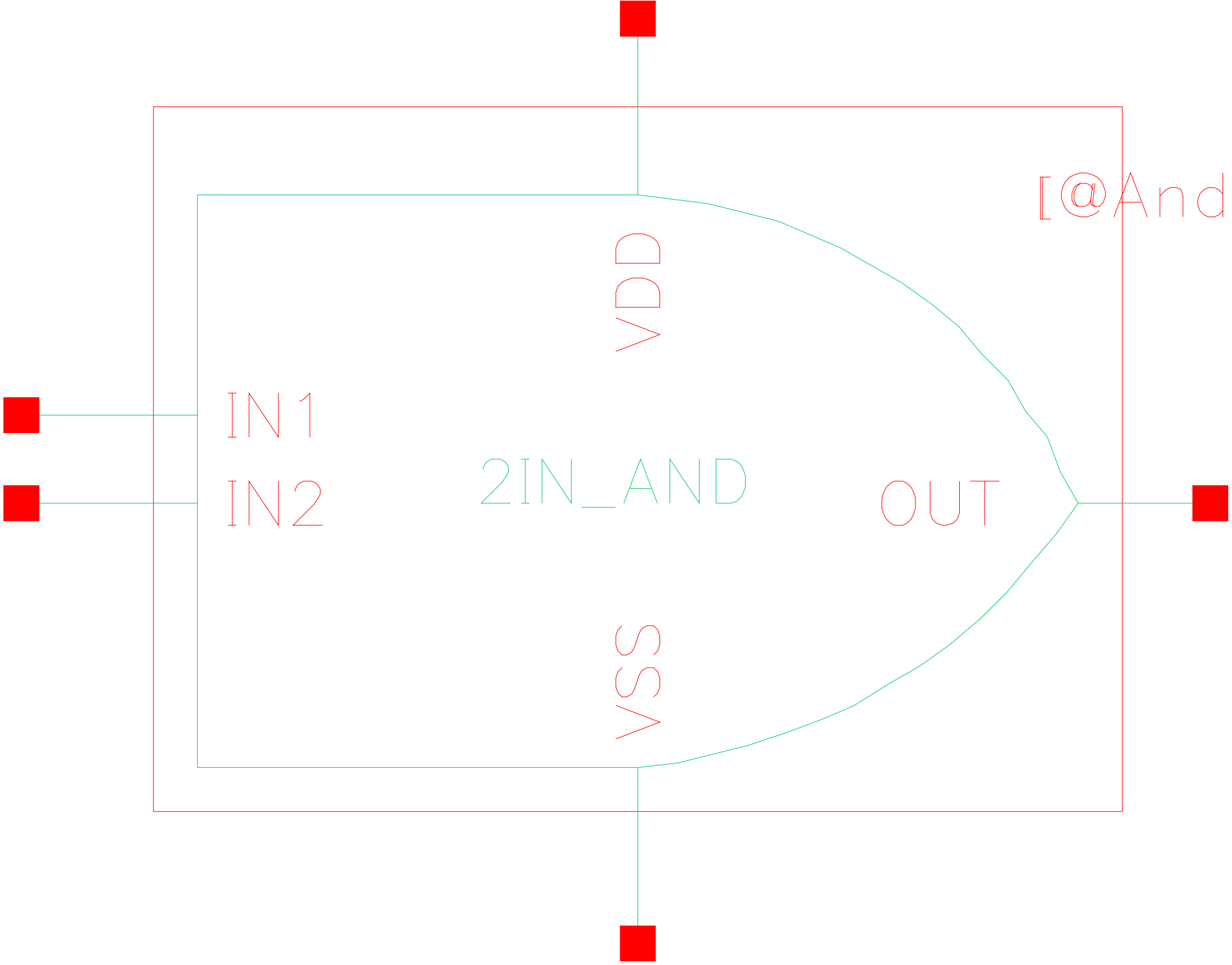
Sun Oct 7 20:11:20 2018

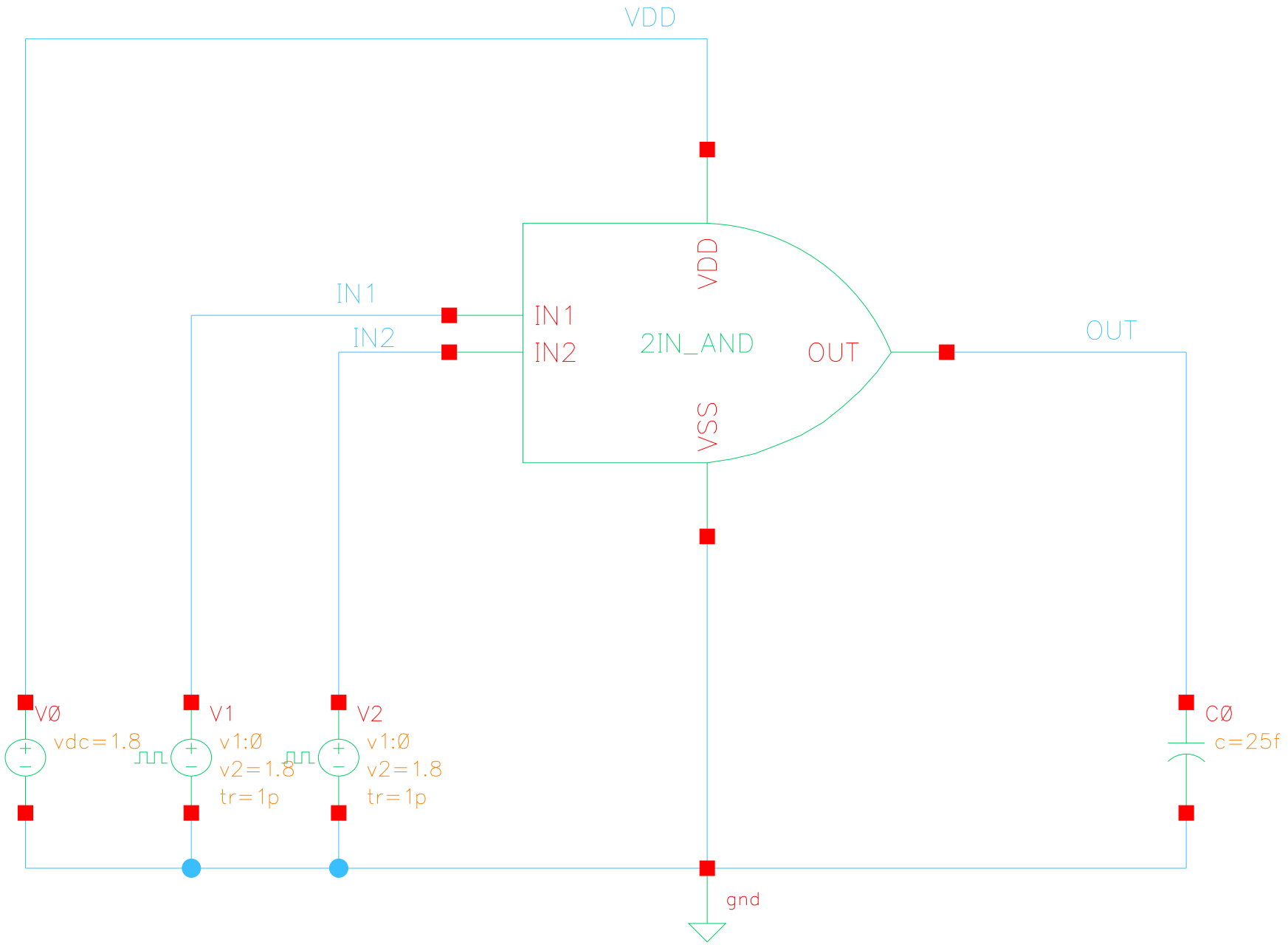


2 Input AND gate

2 Input AND gate schematic

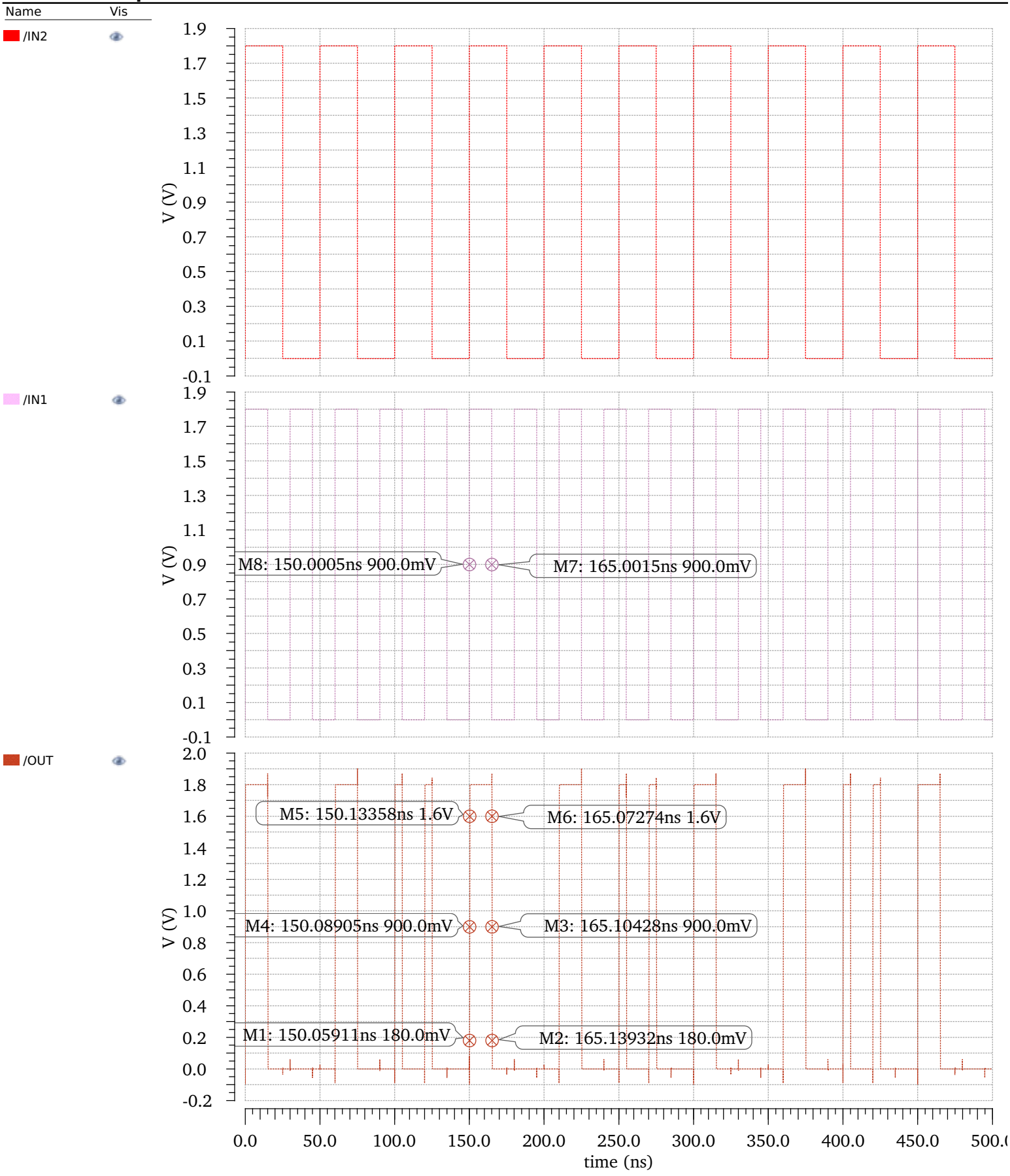



[@And]
VDD
IN1
IN2
2IN_AND
OUT
VSS

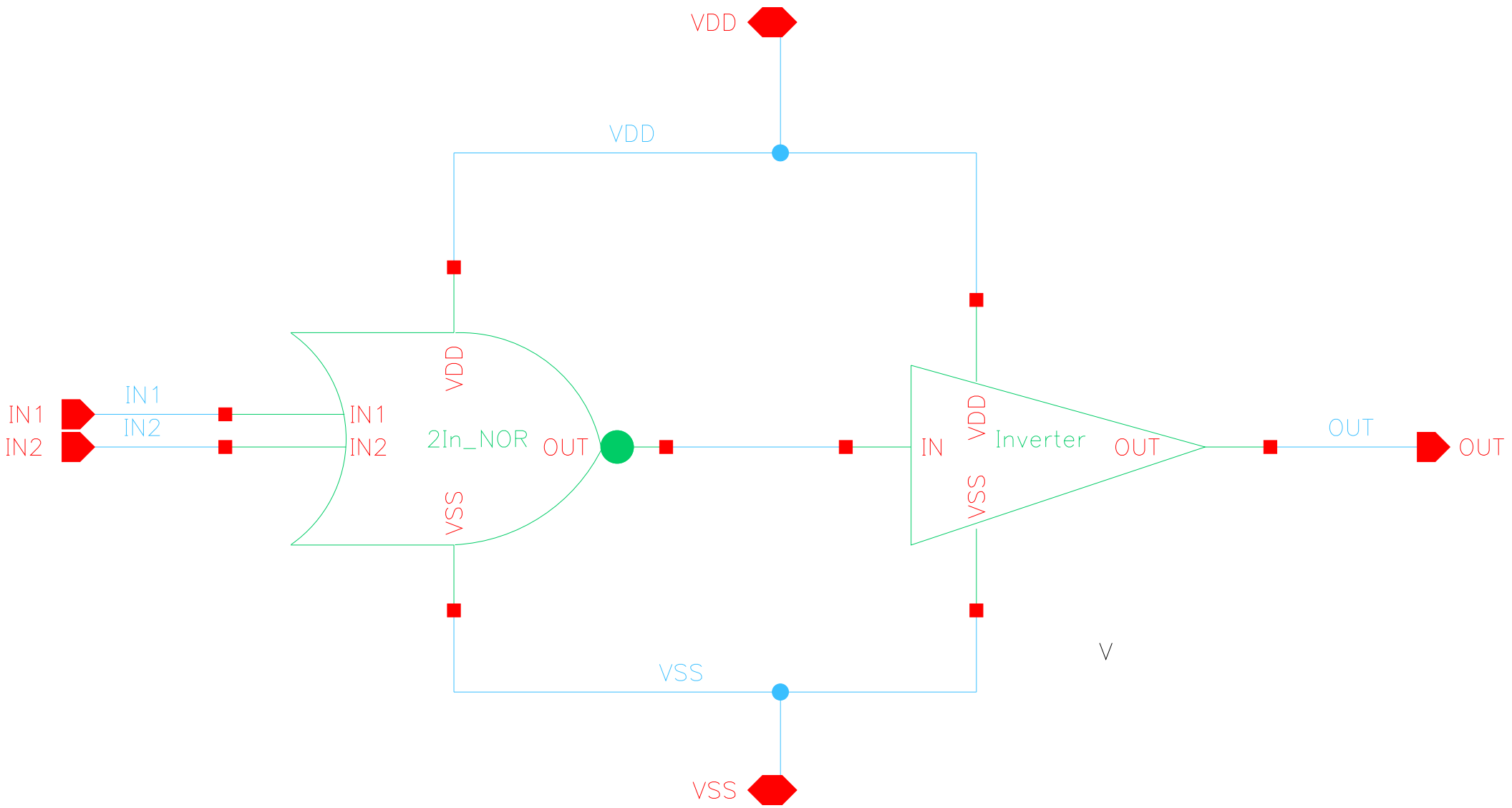

VDD
IN1
IN2
VDD
IN1
IN2
2IN_AND
OUT
VSS
OUT
V0
vdc=1.8
V1
v1:0
v2=1.8
tr=1p
V2
v1:0
v2=1.8
tr=1p
C0
c=25f
gnd

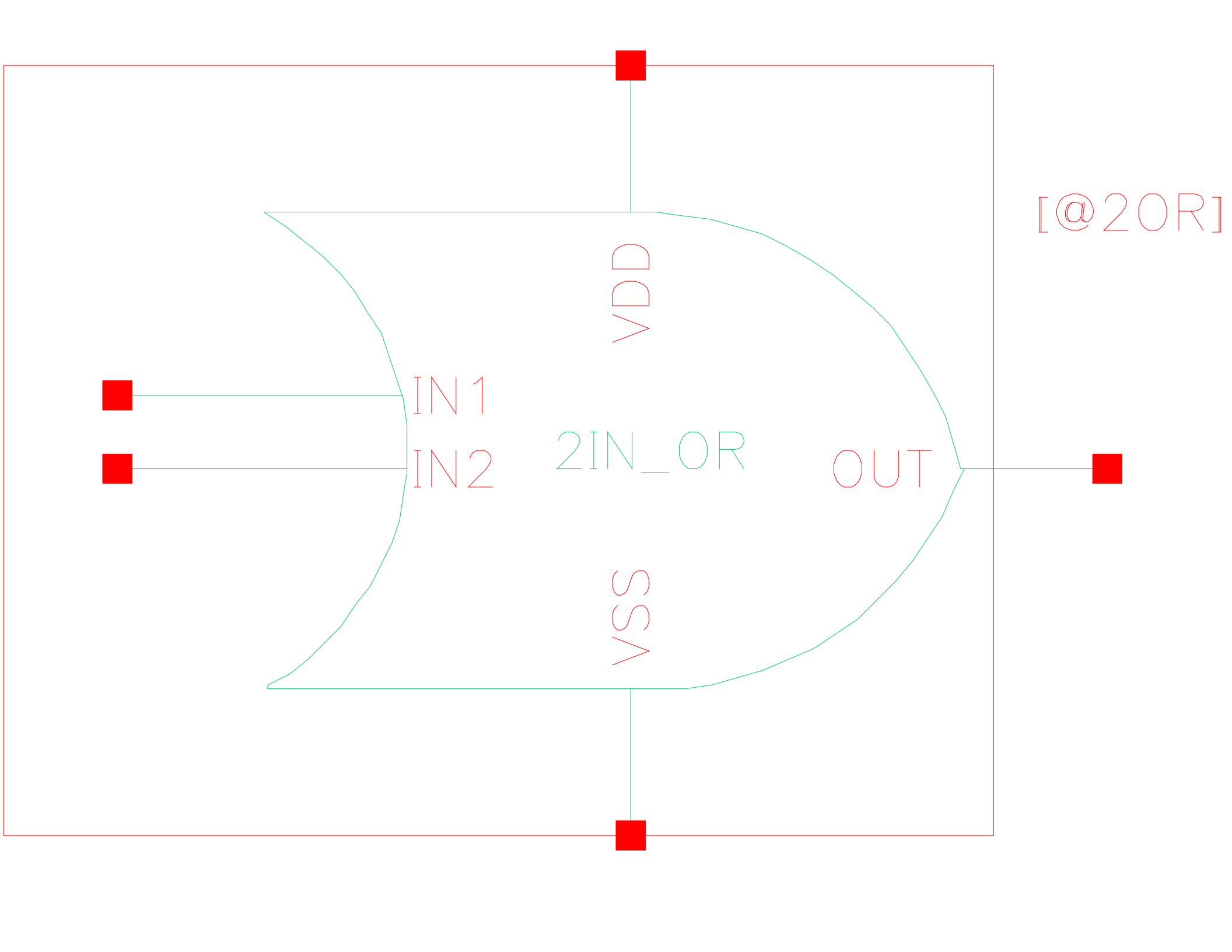
Transient Response

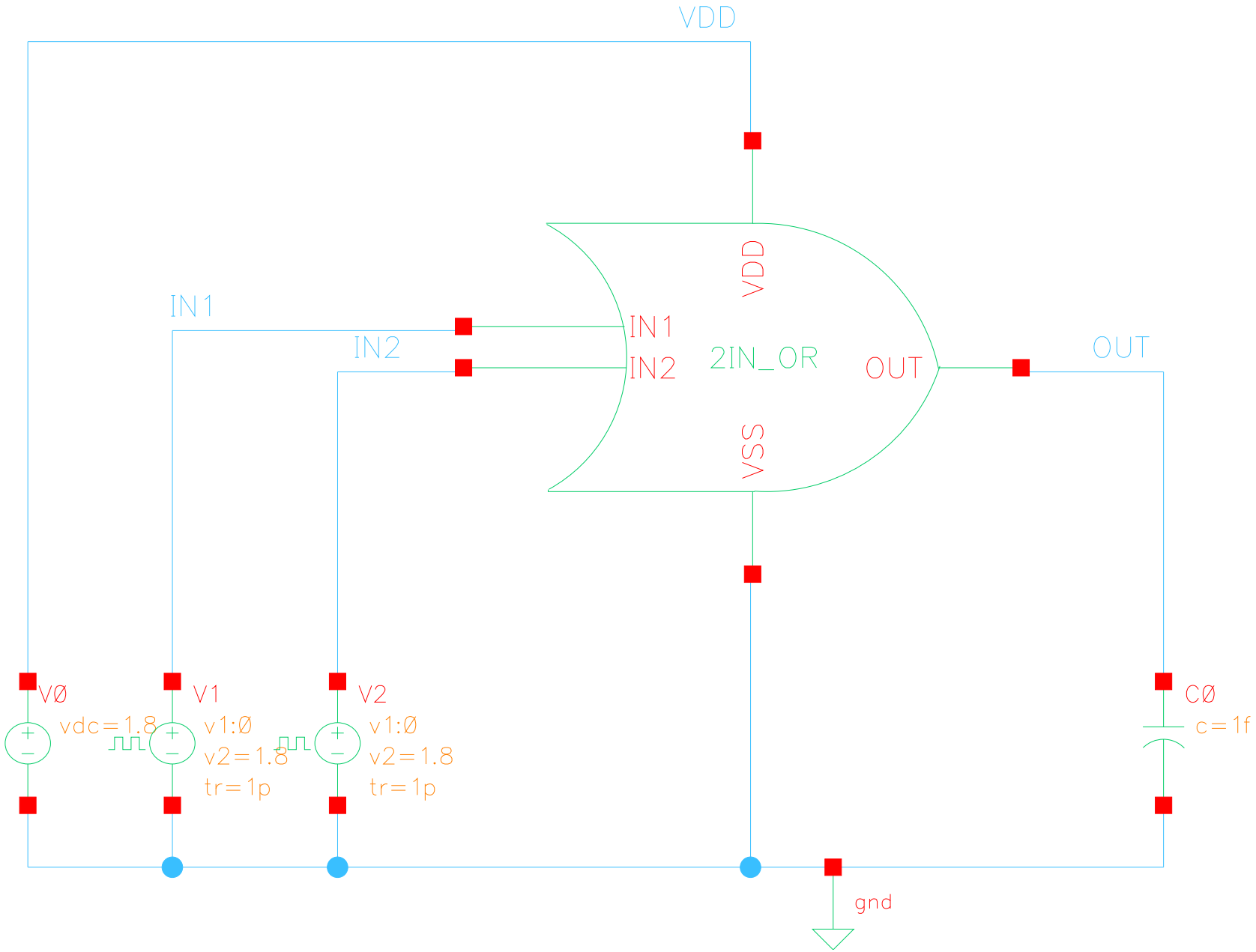
Fri Nov 30 22:32:02 2018



2 Input OR gate


VDD
VDD
IN1
IN2
IN1
IN2
IN1
IN2
VDD
2In_NOR
OUT
VSS
IN
VDD
Inverter
OUT
VSS
OUT
OUT
V
VSS
VSS

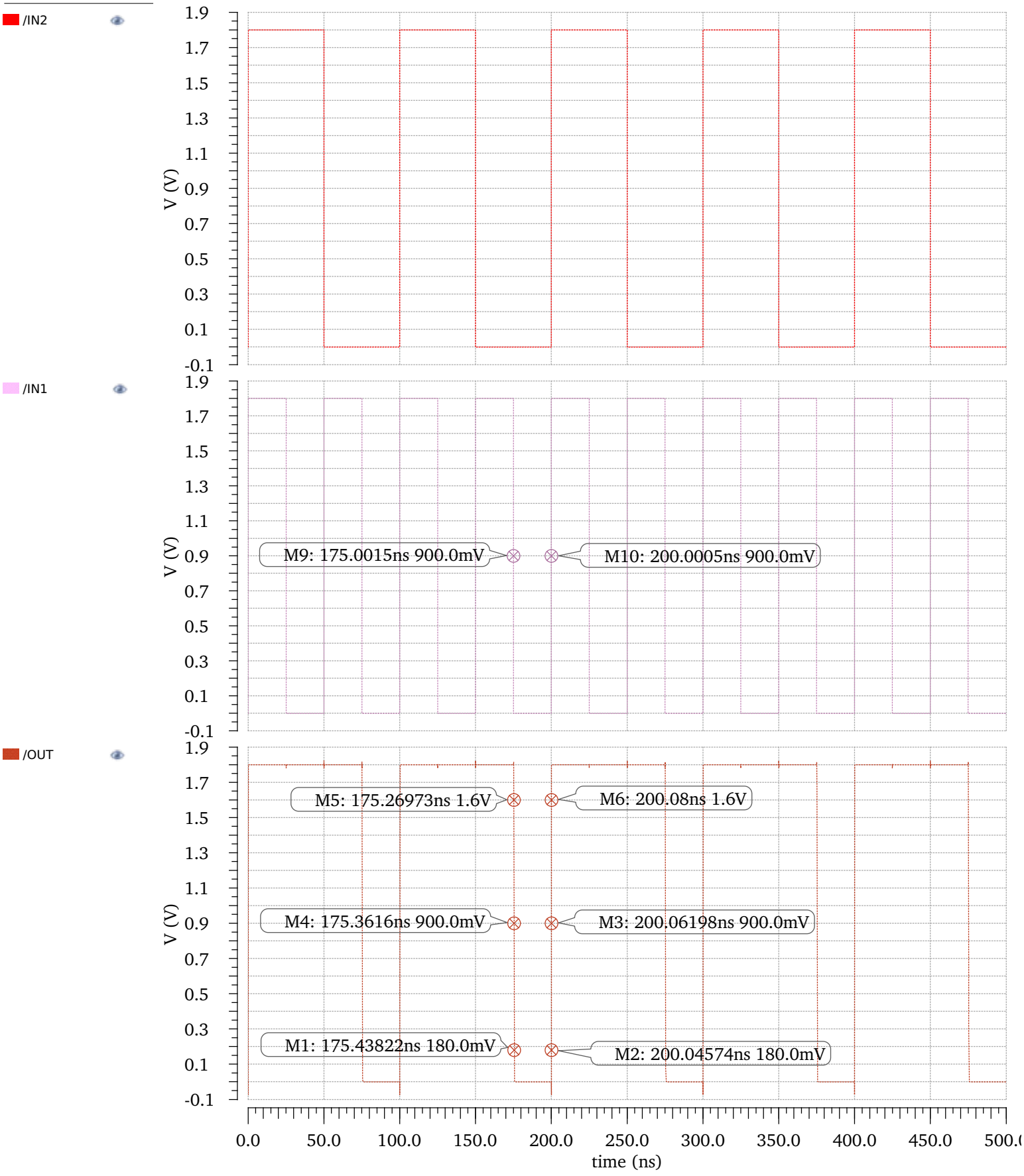

[@2OR]
VDD
IN1
IN2
2IN_OR
OUT
VSS


VDD
IN1
IN2
VDD
IN1
IN2
2IN_OR
OUT
OUT
VSS
VØ
vdc=1.8
V1
v1:Ø
v2=1.8
tr=1p
V2
v1:Ø
v2=1.8
tr=1p
CØ
c=1f
gnd

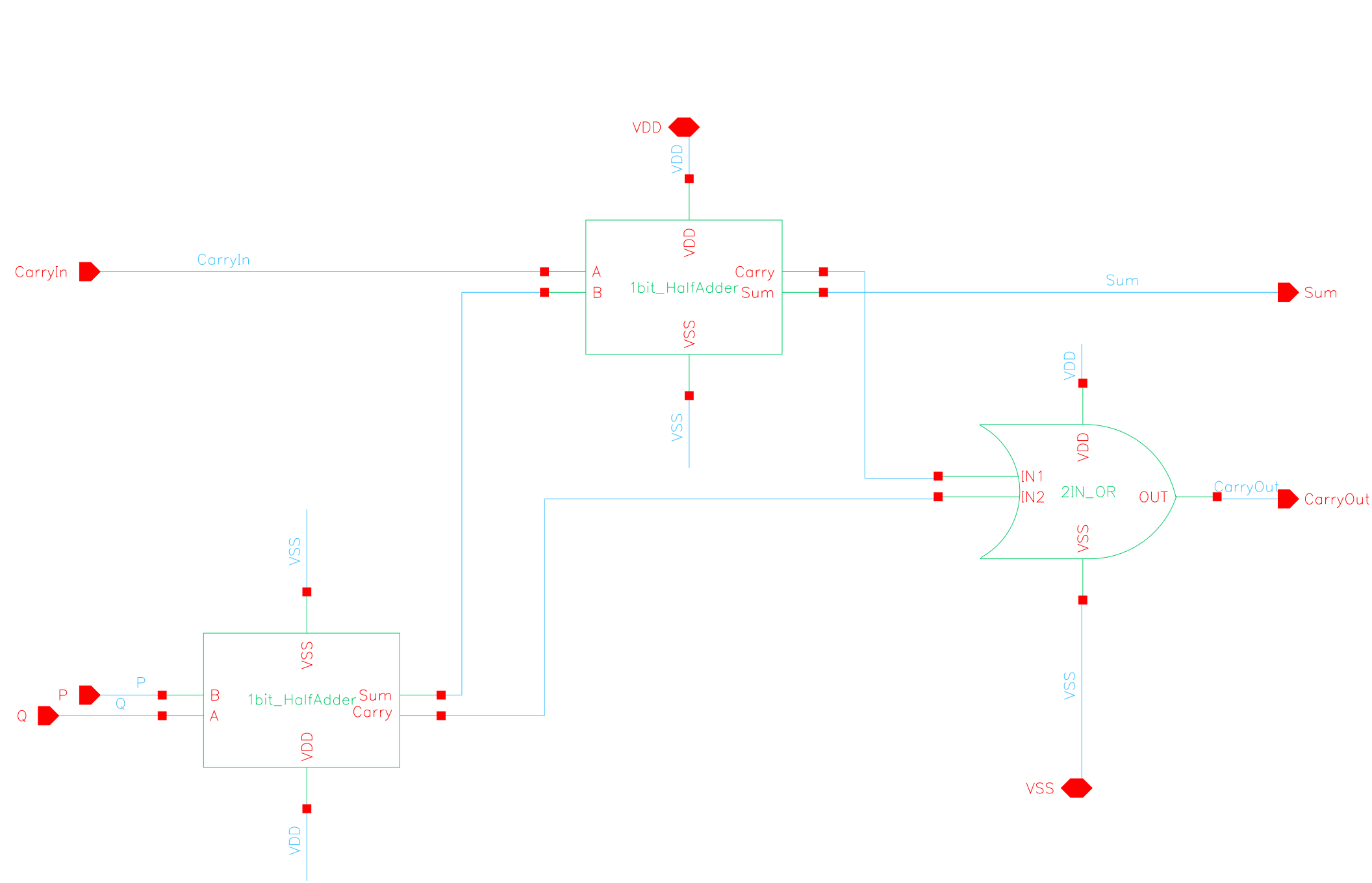
Transient Response

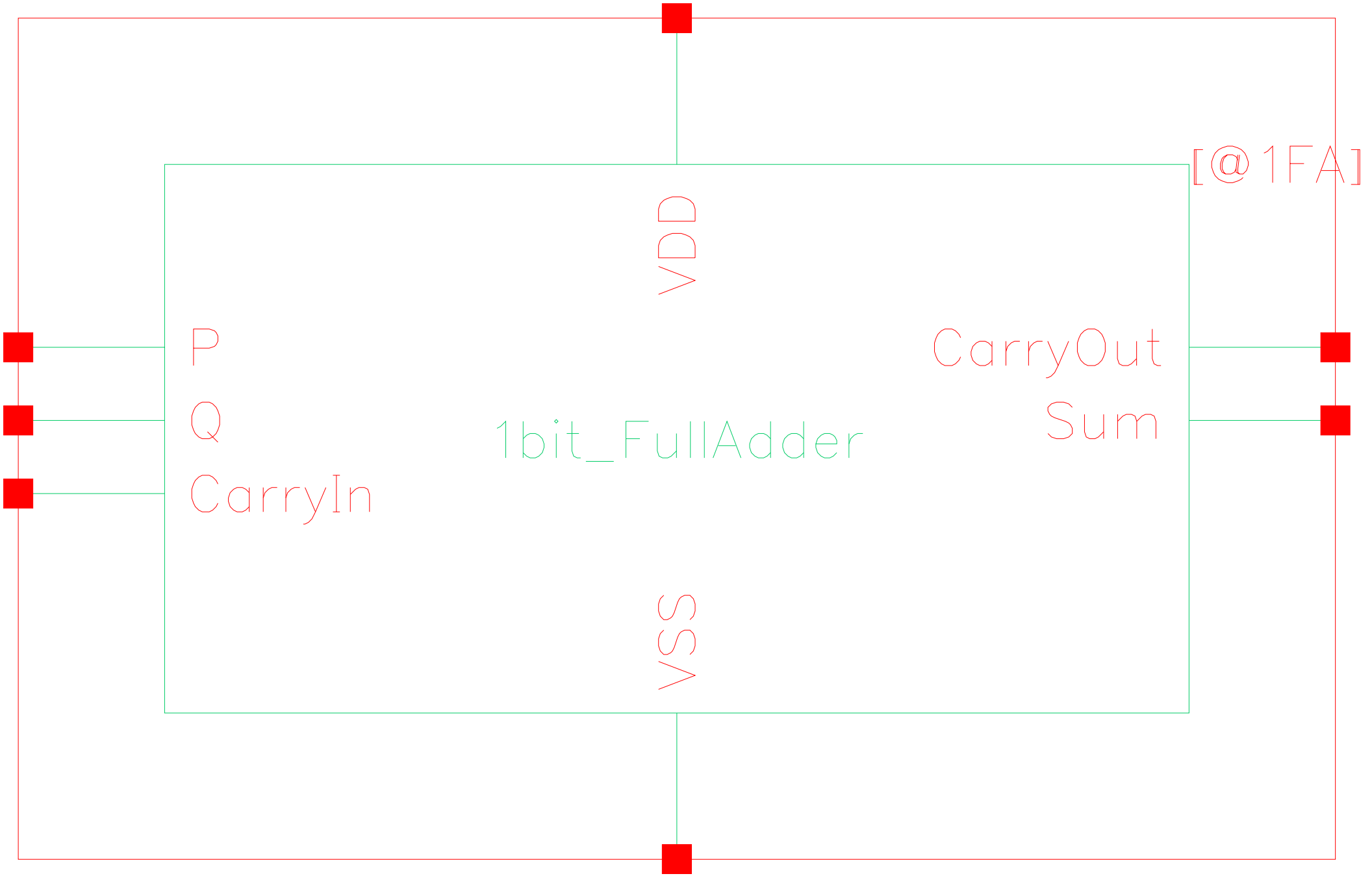
2 Input OR gate

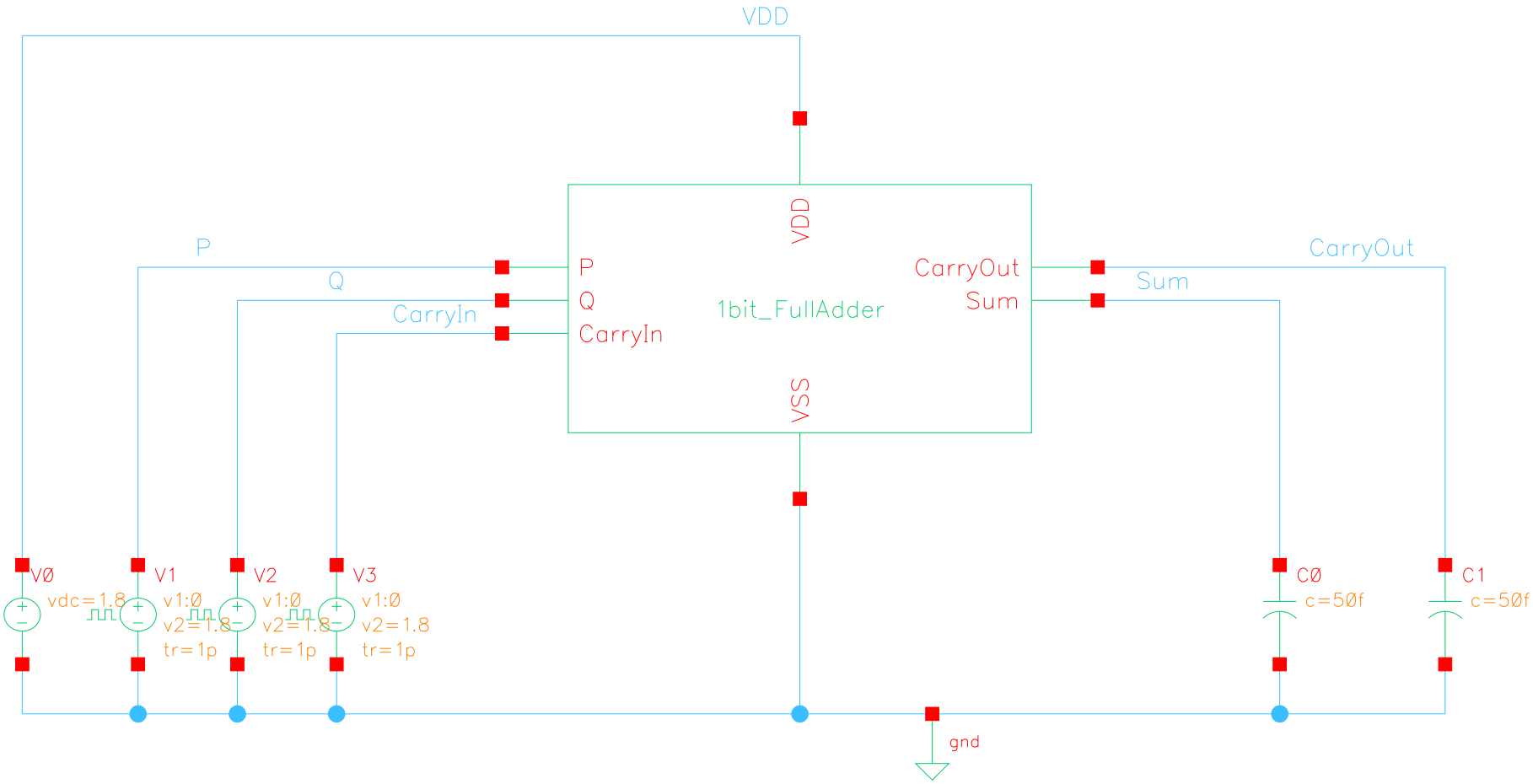
Sat Dec 1 00:53:21 2018



1 Bit Half Adder


VDD
VDD
CarryIn
CarryIn
A
B
1bit_HalfAdder
Carry
Sum
VDD
VSS
VSS
Sum
Sum
VDD
VDD
IN1
IN2
2IN_OR
OUT
CarryOut
CarryOut
VSS
VSS
VSS
P
P
Q
Q
B
A
1bit_HalfAdder
Sum
Carry
VSS
VDD
VDD

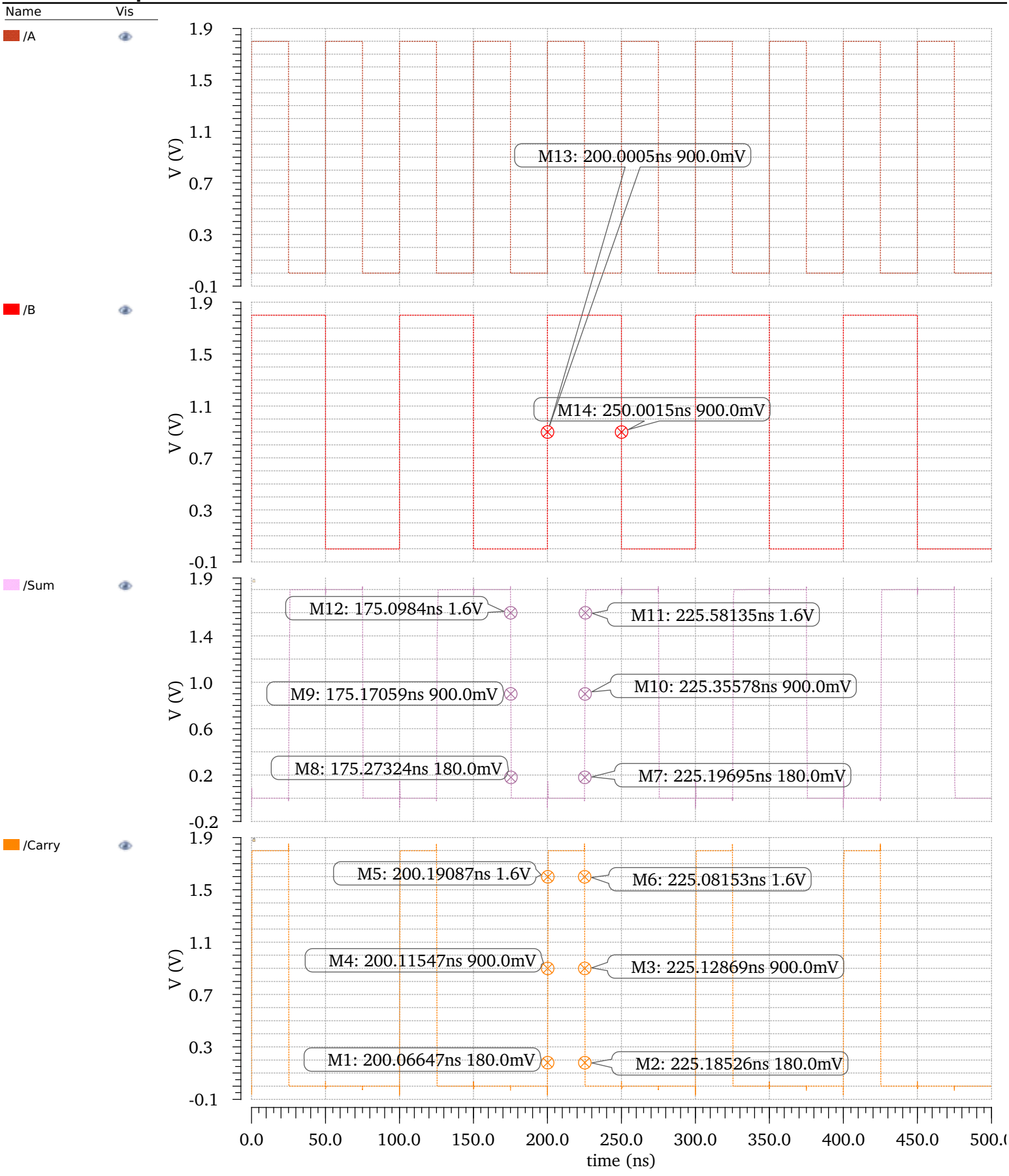

[@1FA]
VDD
P
Q
CarryIn
1bit_FullAdder
CarryOut
Sum
VSS


VDD
P
Q
CarryIn
VDD
P
Q
CarryIn
1bit_FullAdder
CarryOut
Sum
VSS
CarryOut
Sum
V0
vdc=1.8
V1
v1:0
v2=1.8
tr=1p
V2
v1:0
v2=1.8
tr=1p
V3
v1:0
v2=1.8
tr=1p
C0
c=50f
C1
c=50f
gnd

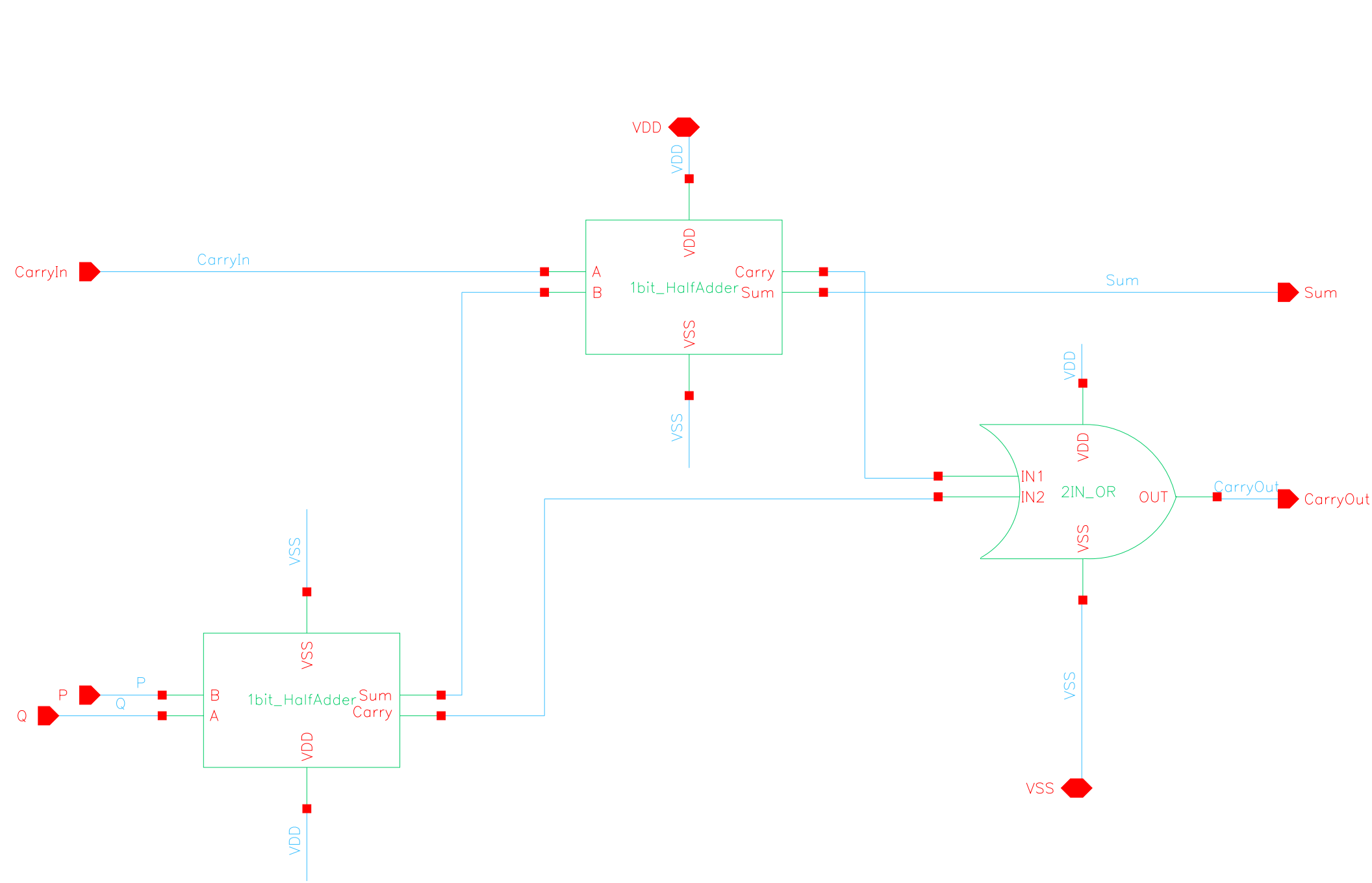
Transient Response

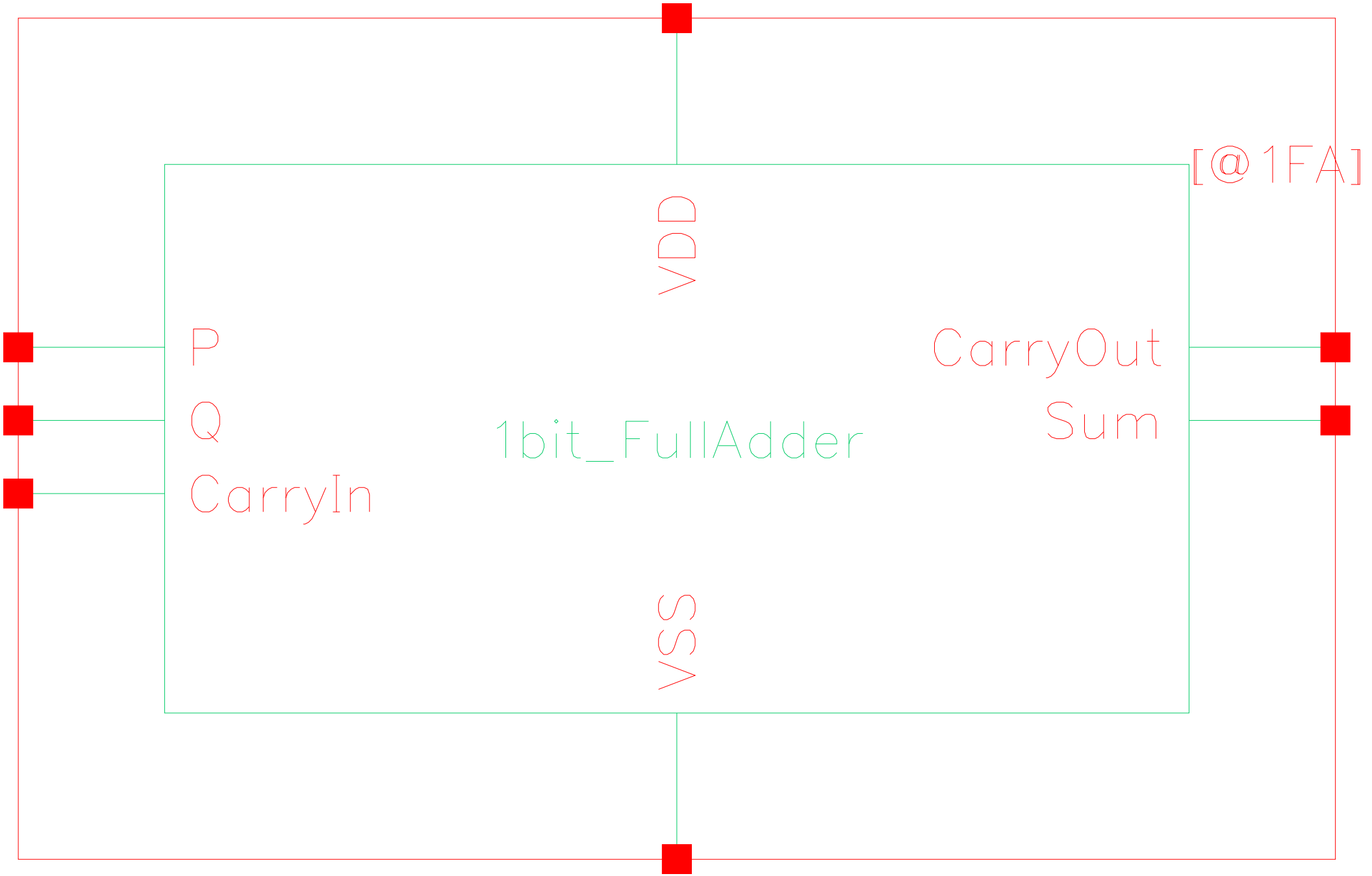
1 Bit Half Adder

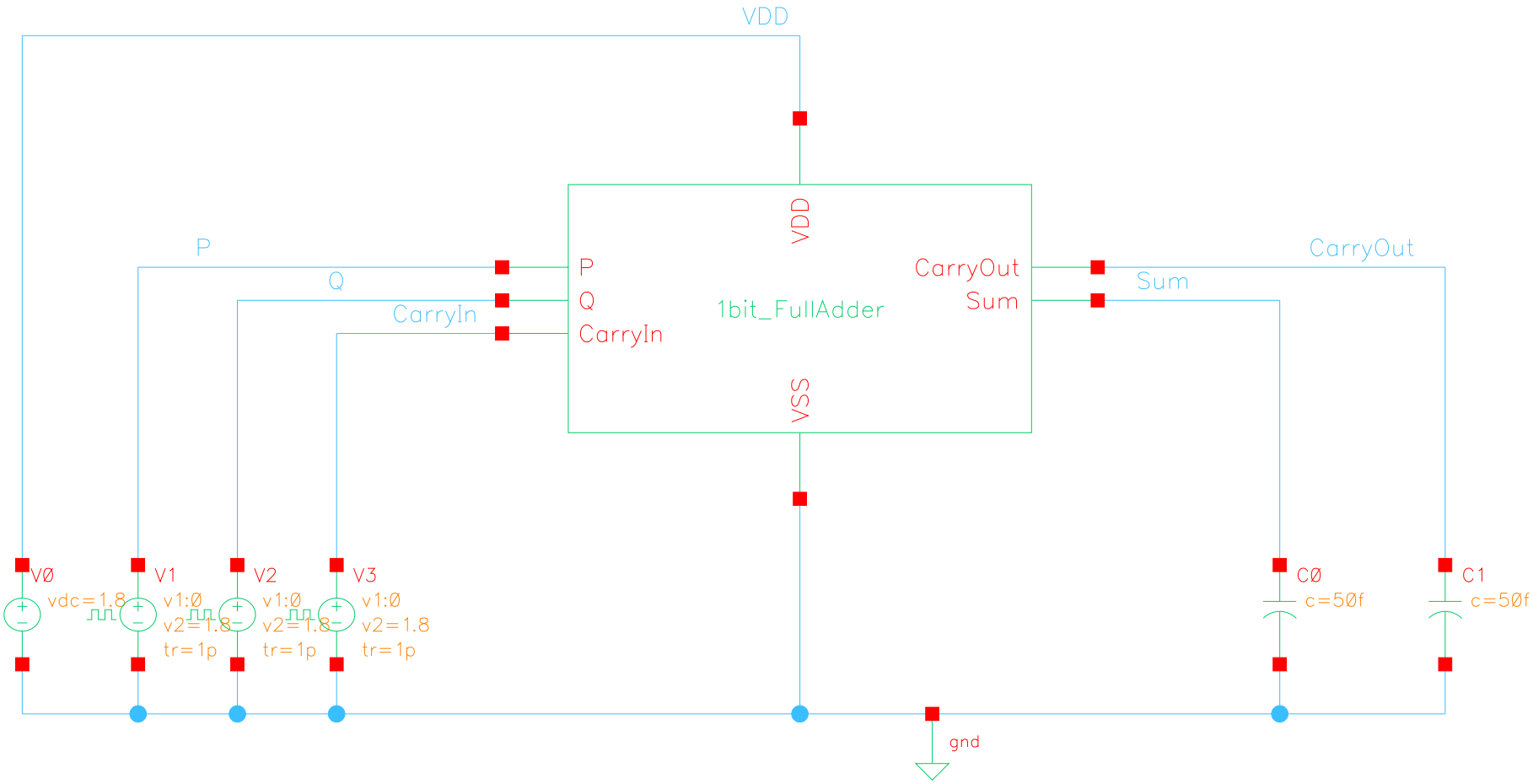
Sat Dec 1 12:10:36 2018



1 Bit Full Adder


VDD
VDD
CarryIn
CarryIn
A
B
1bit_HalfAdder
Carry
Sum
VDD
VSS
VSS
Sum
Sum
VDD
VDD
IN1
IN2
2IN_OR
OUT
CarryOut
CarryOut
VSS
VSS
VSS
P
P
Q
Q
B
A
1bit_HalfAdder
Sum
Carry
VSS
VDD
VDD

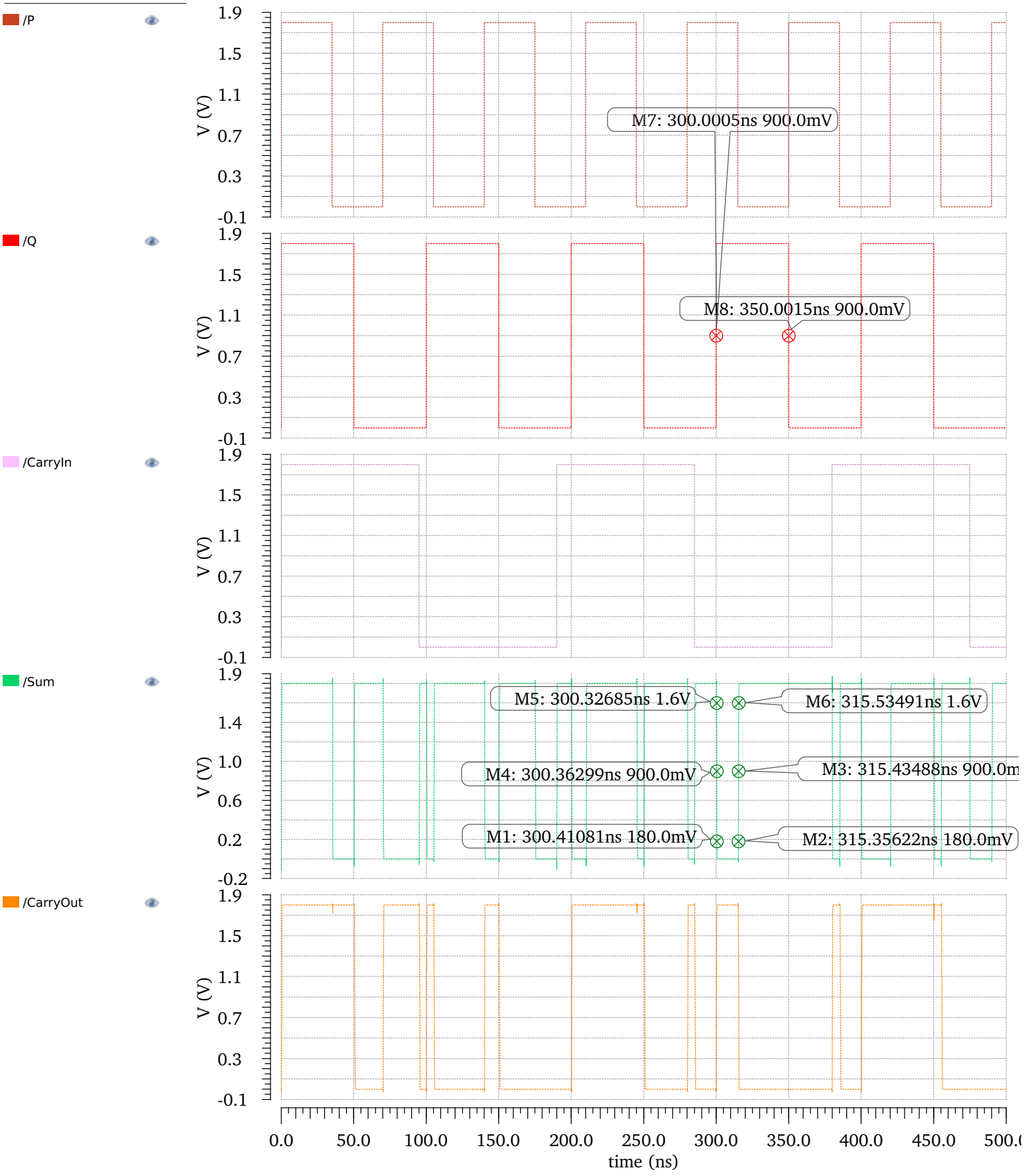

[@1FA]
VDD
P
Q
CarryIn
1bit_FullAdder
CarryOut
Sum
VSS


VDD
P
Q
CarryIn
VDD
P
Q
CarryIn
1bit_FullAdder
CarryOut
Sum
VSS
CarryOut
Sum
V0
vdc=1.8
V1
v1:0
v2=1.8
tr=1p
V2
v1:0
v2=1.8
tr=1p
V3
v1:0
v2=1.8
tr=1p
C0
c=50f
C1
c=50f
gnd

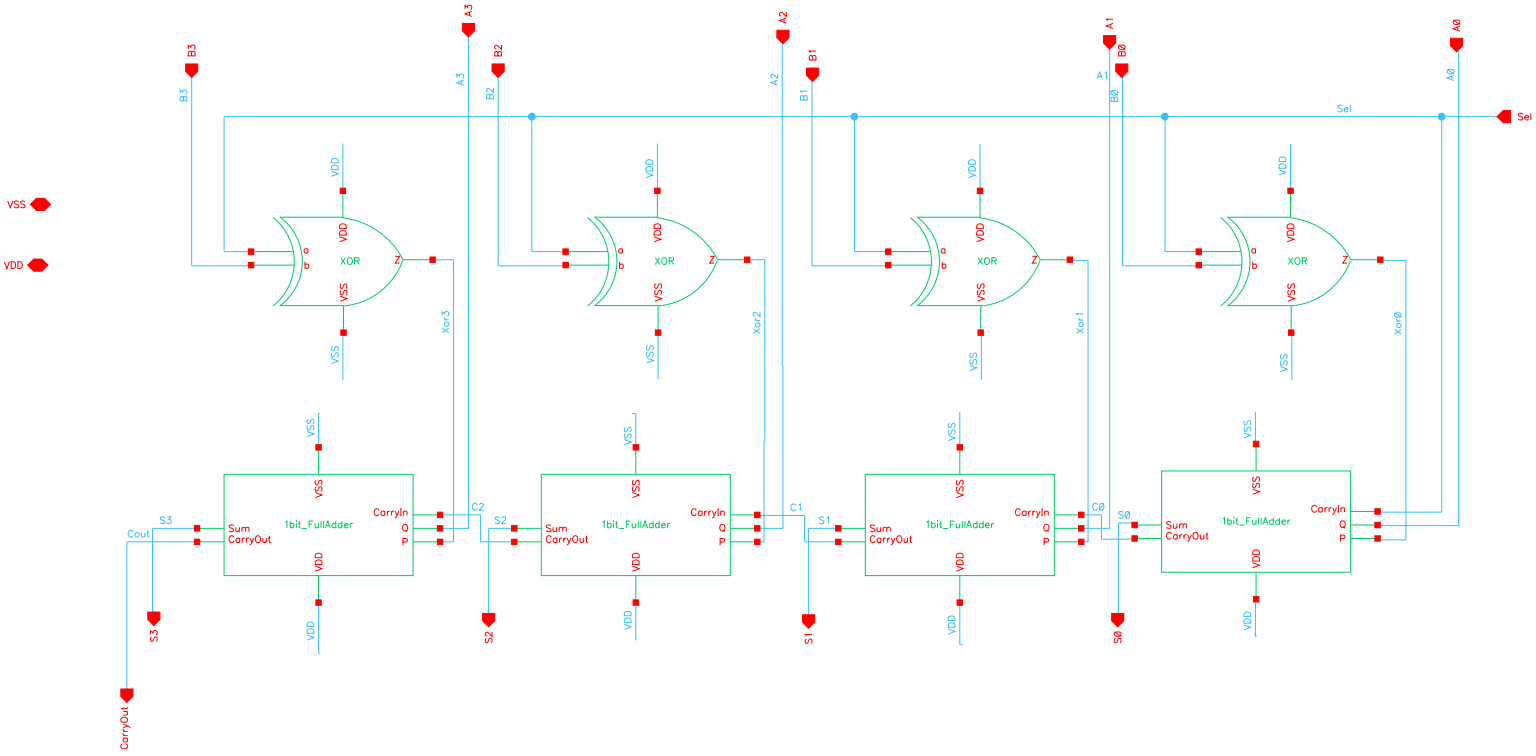
Transient Response

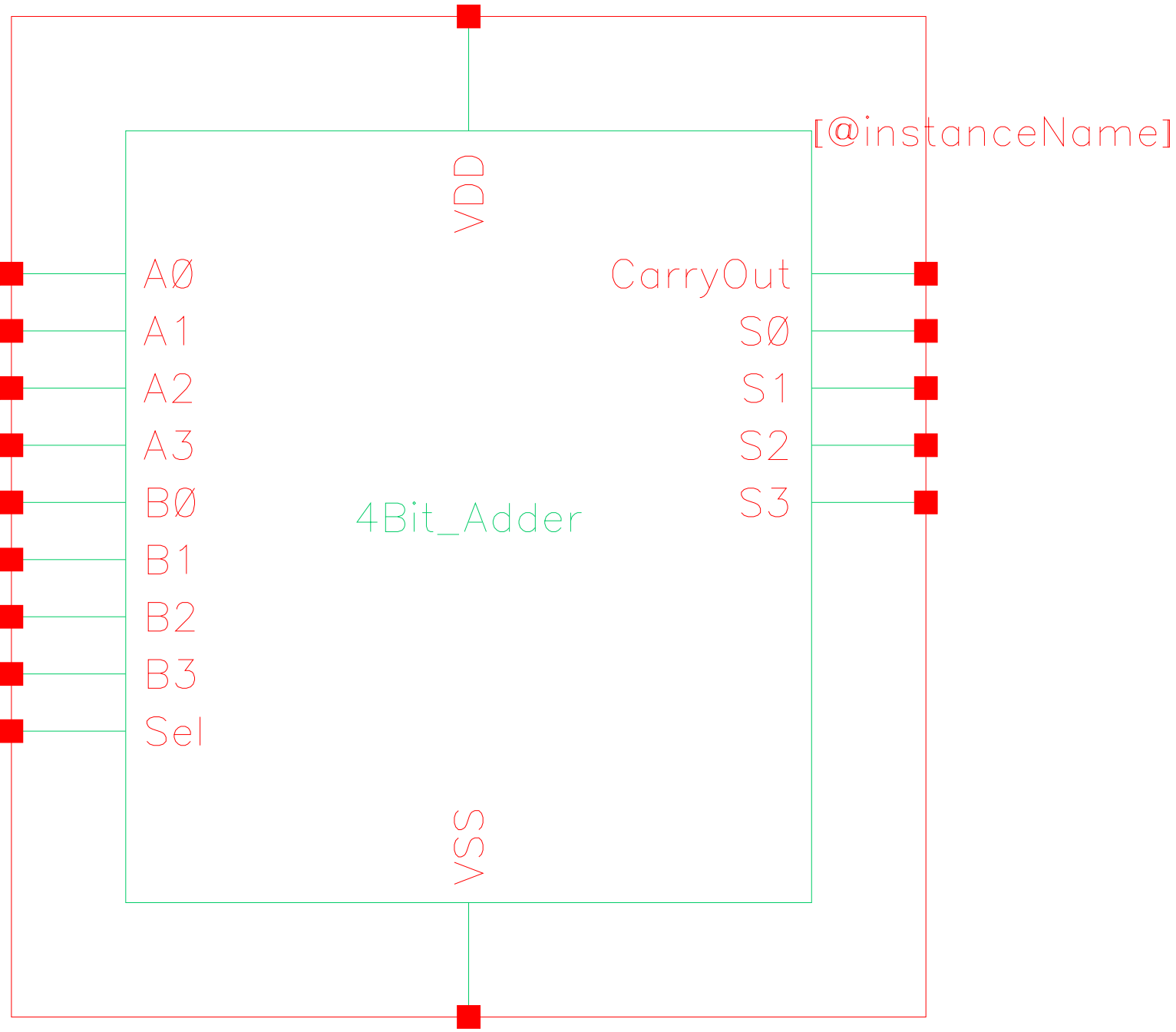
1 Bit Full Adder

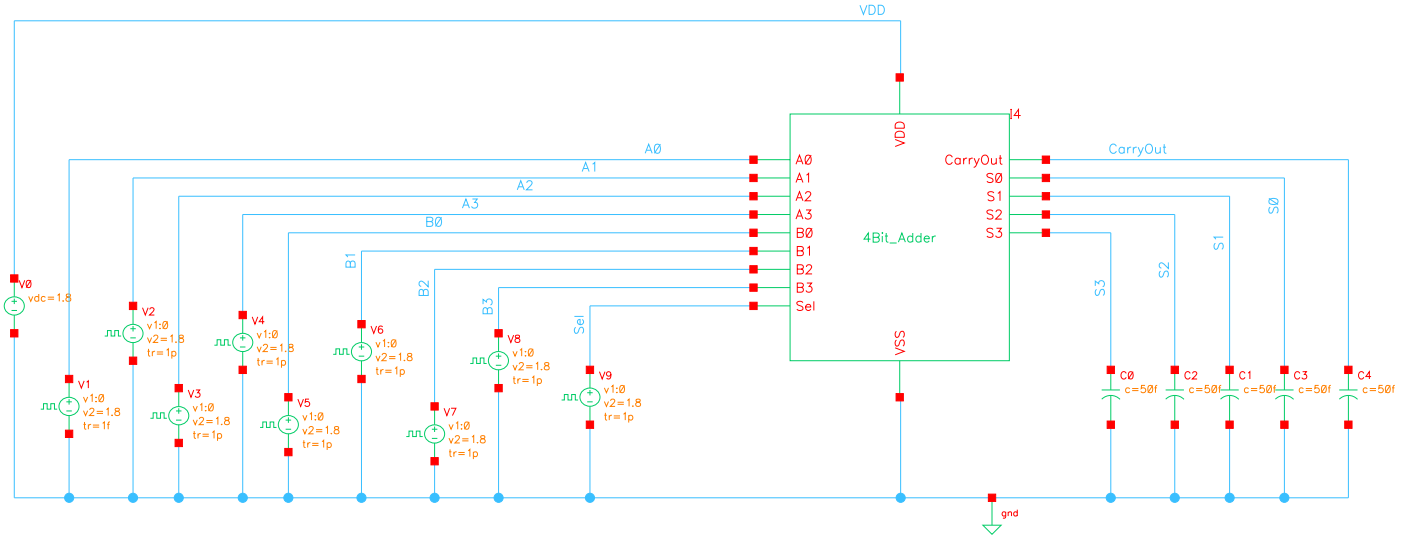
Sat Dec 1 12:33:02 2018



Full Adder

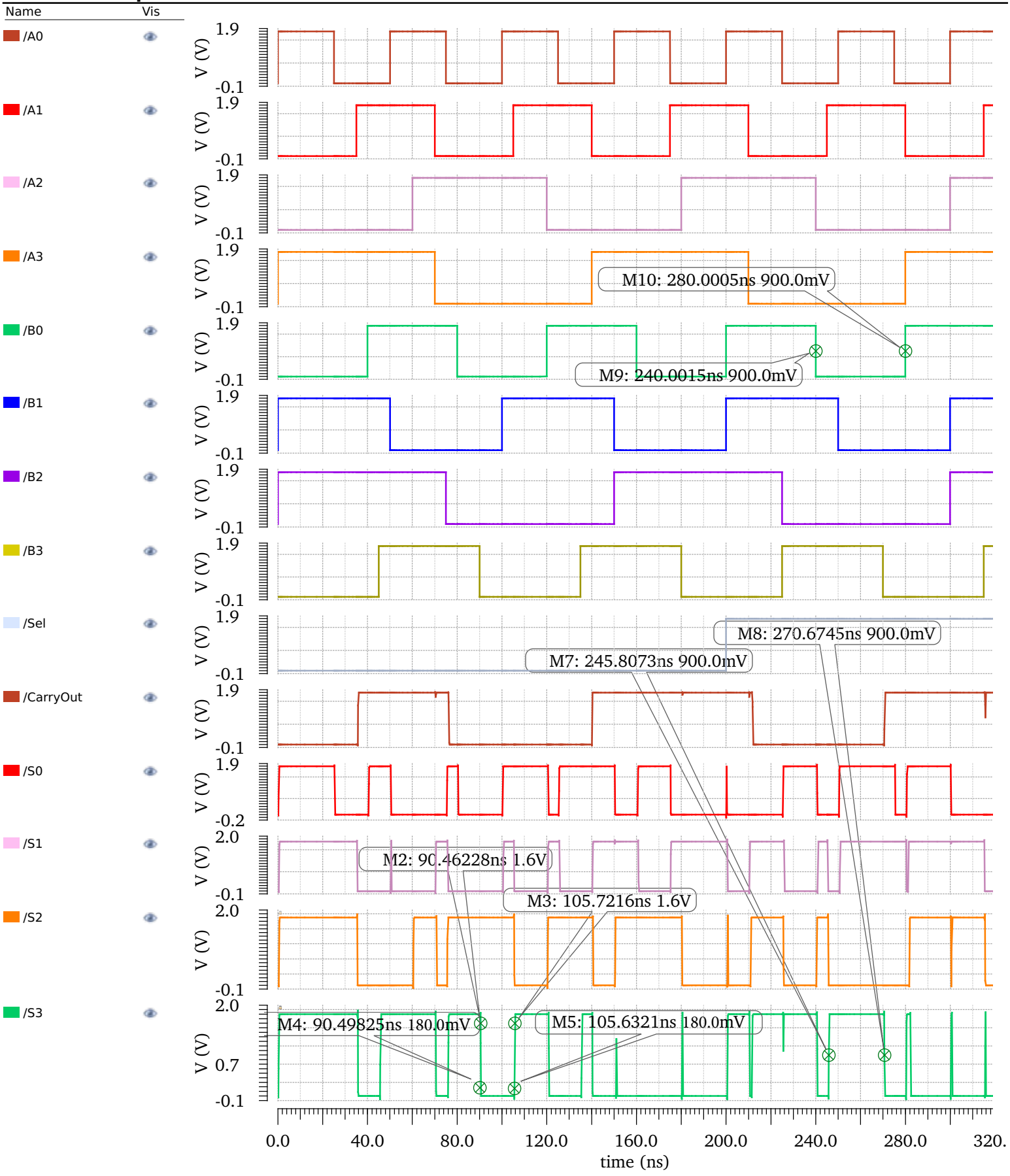

VSS
VDD
B3
A3
B2
A2
B1
A1
B0
A0
Sel
XOR
a
b
Z
VDD
VSS
Xor3
Xor2
Xor1
Xor0
1bit_FullAdder
Sum
CarryOut
CarryIn
Q
P
Cout
S3
S2
S1
S0
C2
C1
C0
CarryOut


[@instanceName]
VDD
A0
A1
A2
A3
B0
B1
B2
B3
Sel
CarryOut
S0
S1
S2
S3
4Bit_Adder
VSS

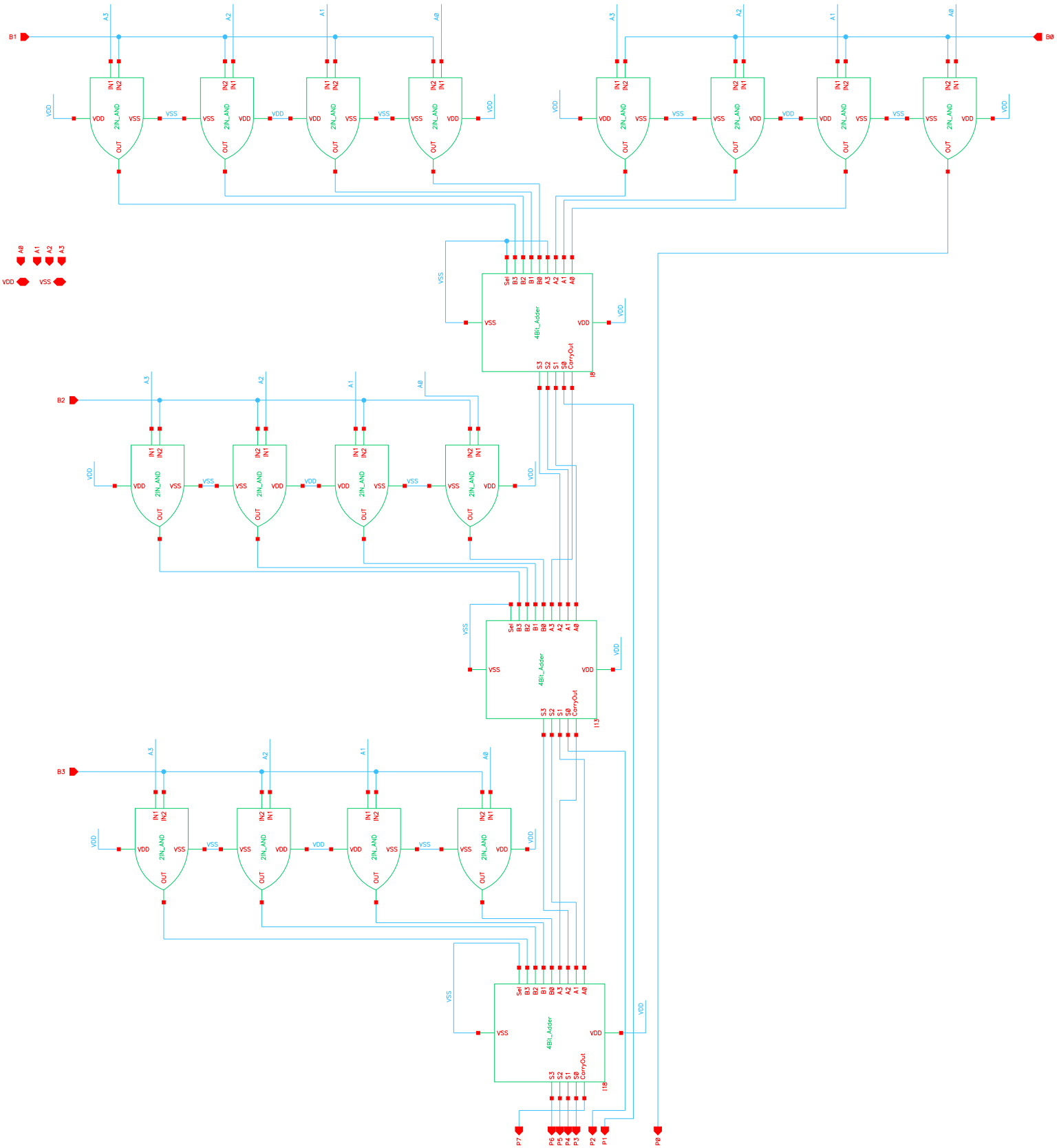

VDD
A0
A1
A2
A3
B0
B1
B2
B3
Sel
VSS
CarryOut
S0
S1
S2
S3
4Bit_Adder
V0
vdc=1.8
V1
v1:0
v2=1.8
tr=1f
V2
v1:0
v2=1.8
tr=1p
V3
v1:0
v2=1.8
tr=1p
V4
v1:0
v2=1.8
tr=1p
V5
v1:0
v2=1.8
tr=1p
V6
v1:0
v2=1.8
tr=1p
V7
v1:0
v2=1.8
tr=1p
V8
v1:0
v2=1.8
tr=1p
V9
v1:0
v2=1.8
tr=1p
C0
c=50f
C2
c=50f
C1
c=50f
C3
c=50f
C4
c=50f
gnd

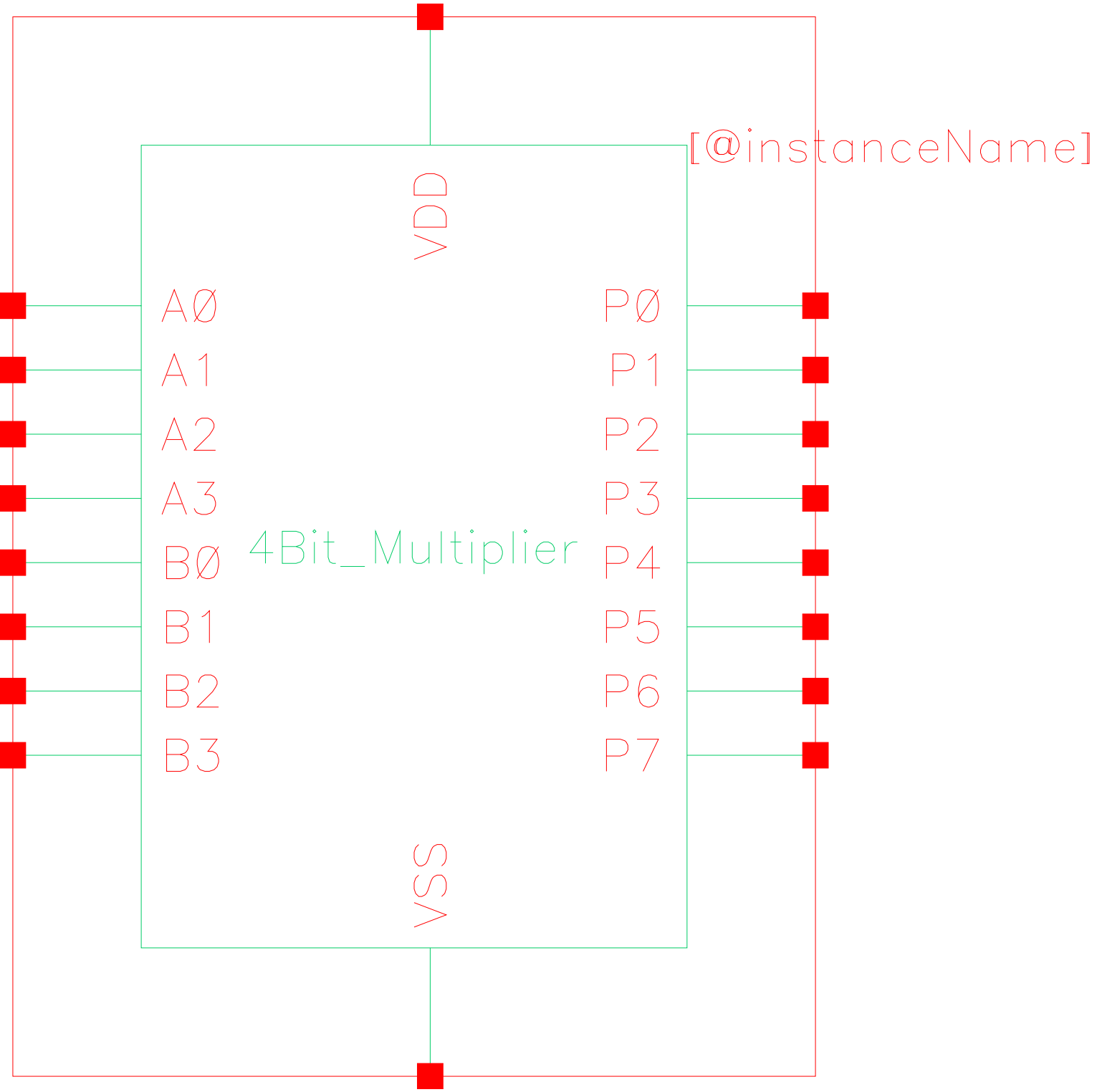
Transient Response

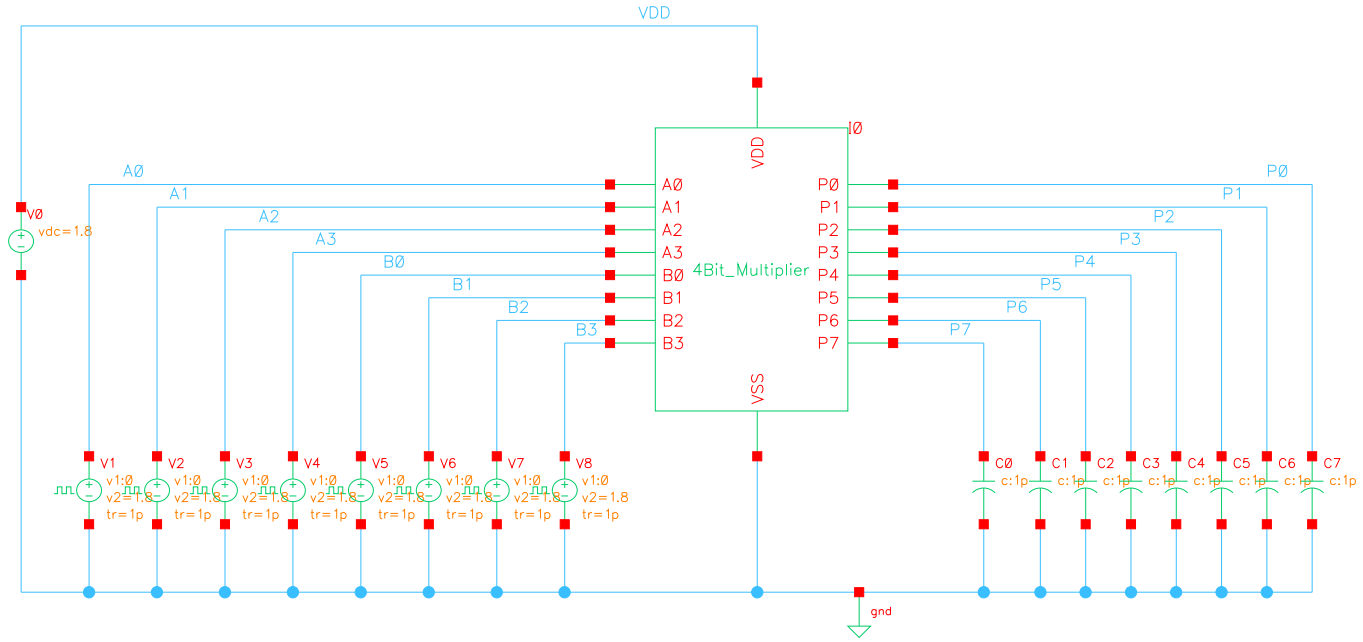
Fri Dec 7 22:04:38 2018



Multiplier

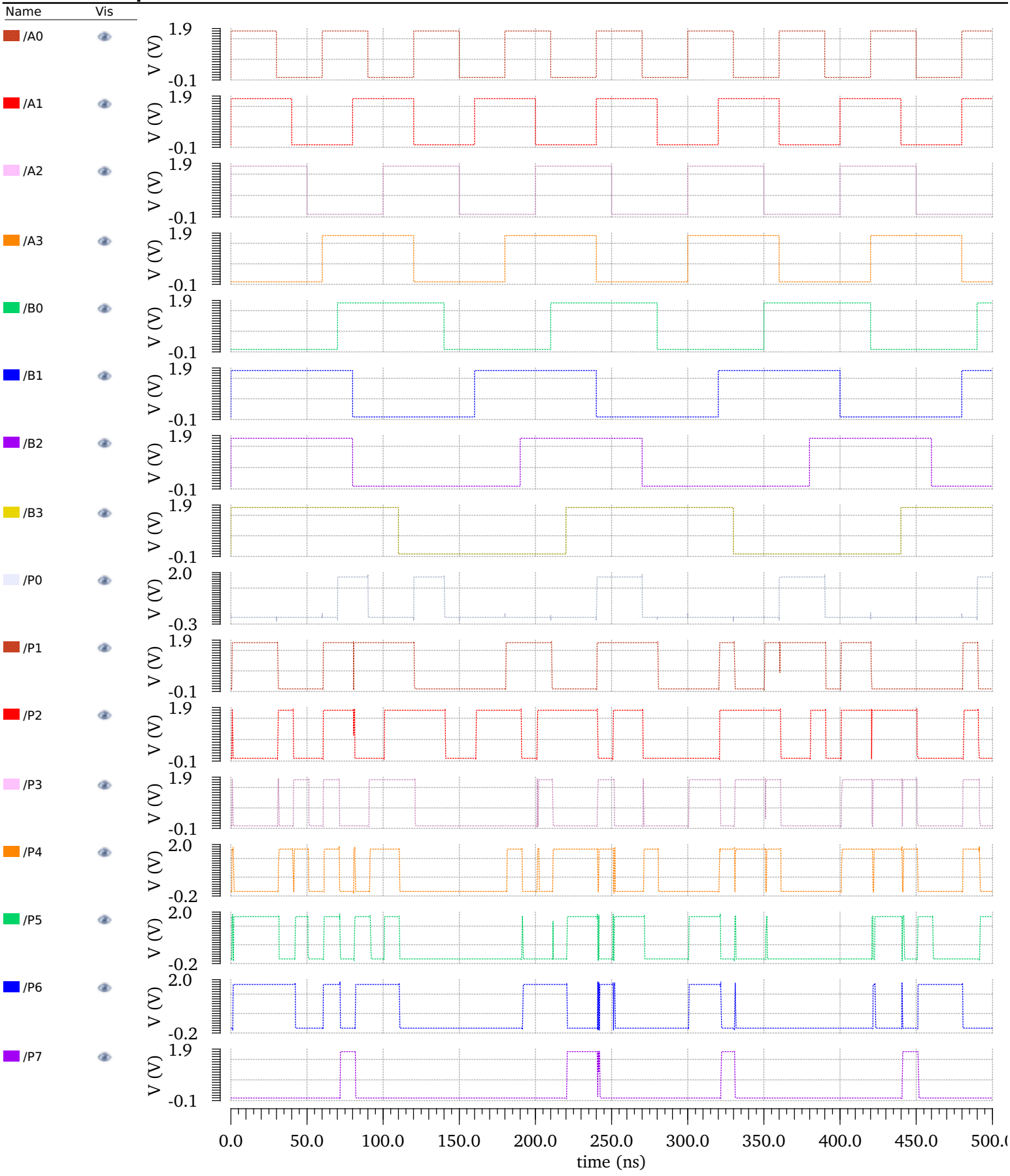

B1
B0
B2
B3
A3
A2
A1
A0
IN1
IN2
2IN_AND
VDD
VSS
OUT
4Bit_Adder
Sel
B3
B2
B1
B0
S3
S2
S1
S0
CarryOut
I8
I13
I18
P7
P6
P5
P4
P3
P2
P1
P0


[@instanceName]
VDD
A0
A1
A2
A3
B0
B1
B2
B3
4Bit_Multiplier
P0
P1
P2
P3
P4
P5
P6
P7
VSS

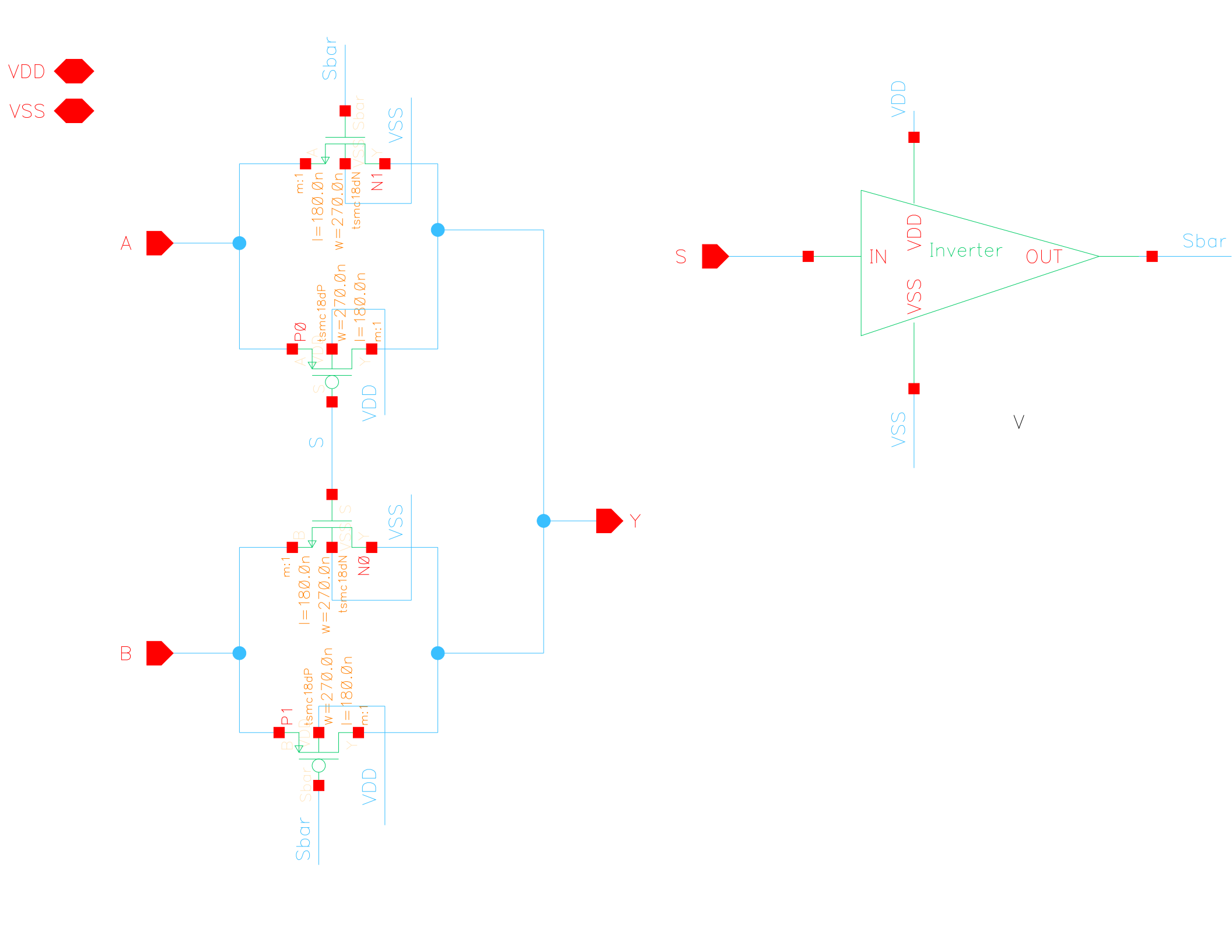

VDD
A0
A1
A2
A3
B0
B1
B2
B3
V0
vdc=1.8
V1
V2
V3
V4
V5
V6
V7
V8
v1:0
v2=1.8
tr=1p
VDD
VSS
4Bit_Multiplier
P0
P1
P2
P3
P4
P5
P6
P7
C0
C1
C2
C3
C4
C5
C6
C7
c:1p
gnd

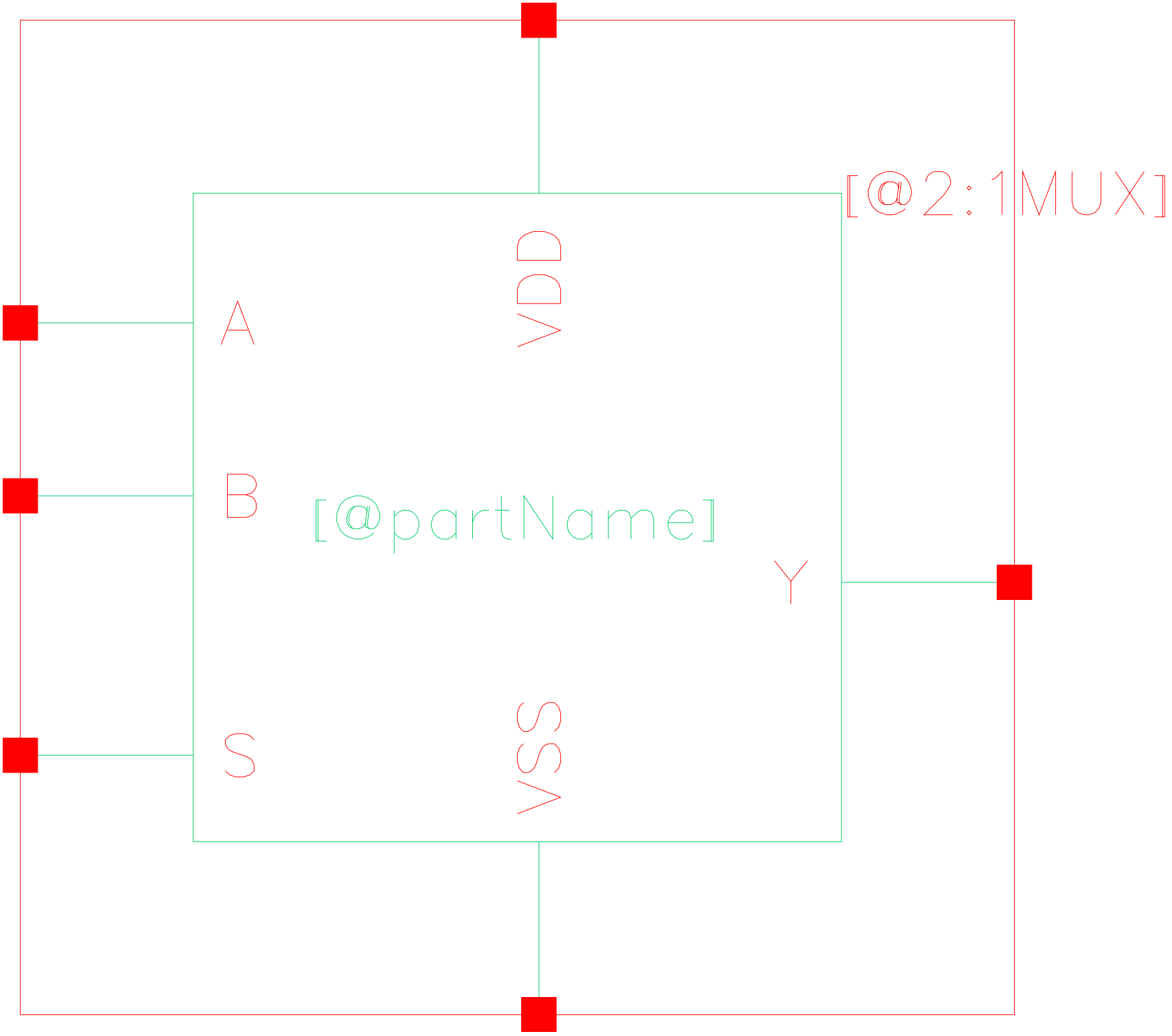
Transient Response

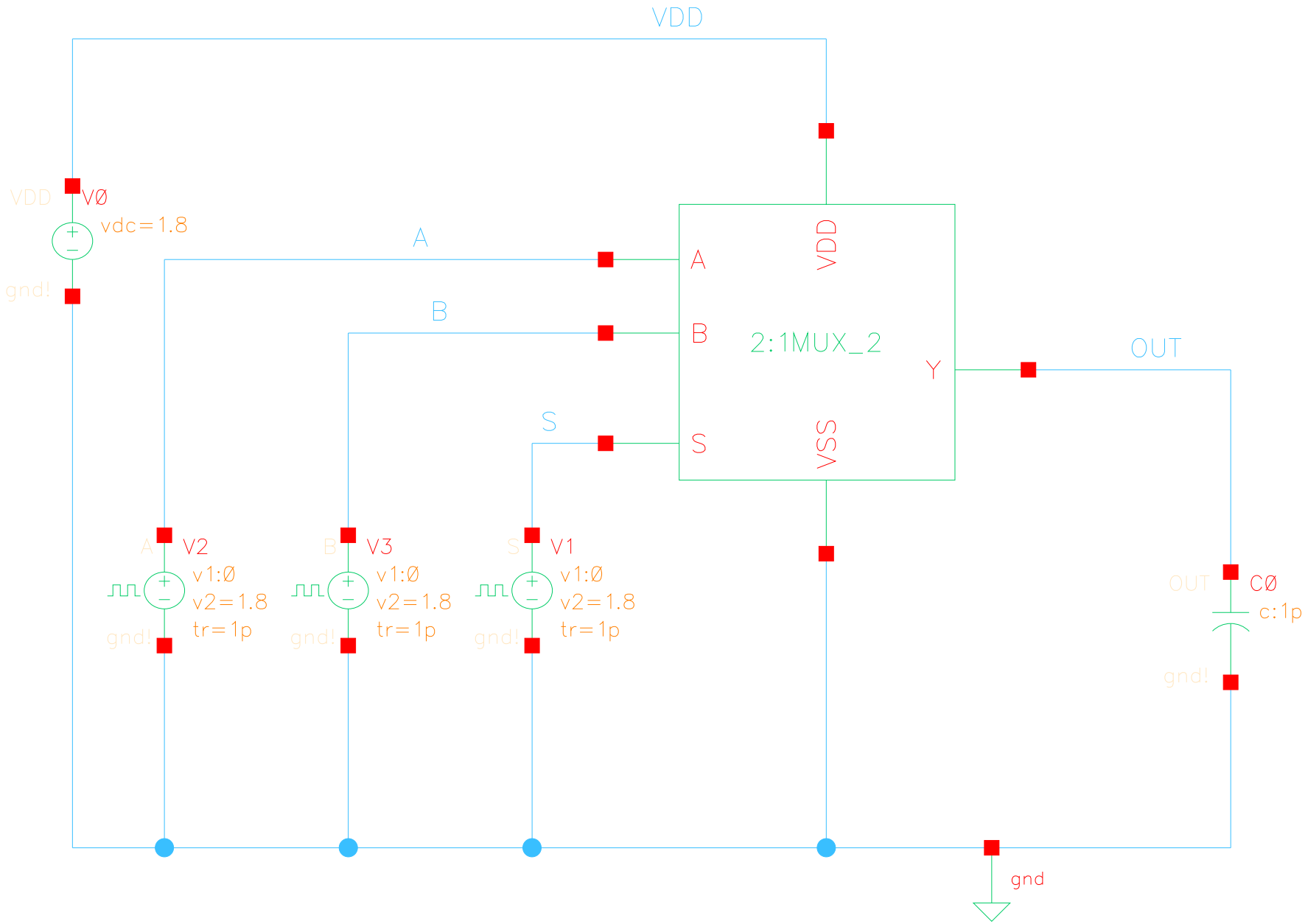
Thu Dec 6 00:32:34 2018



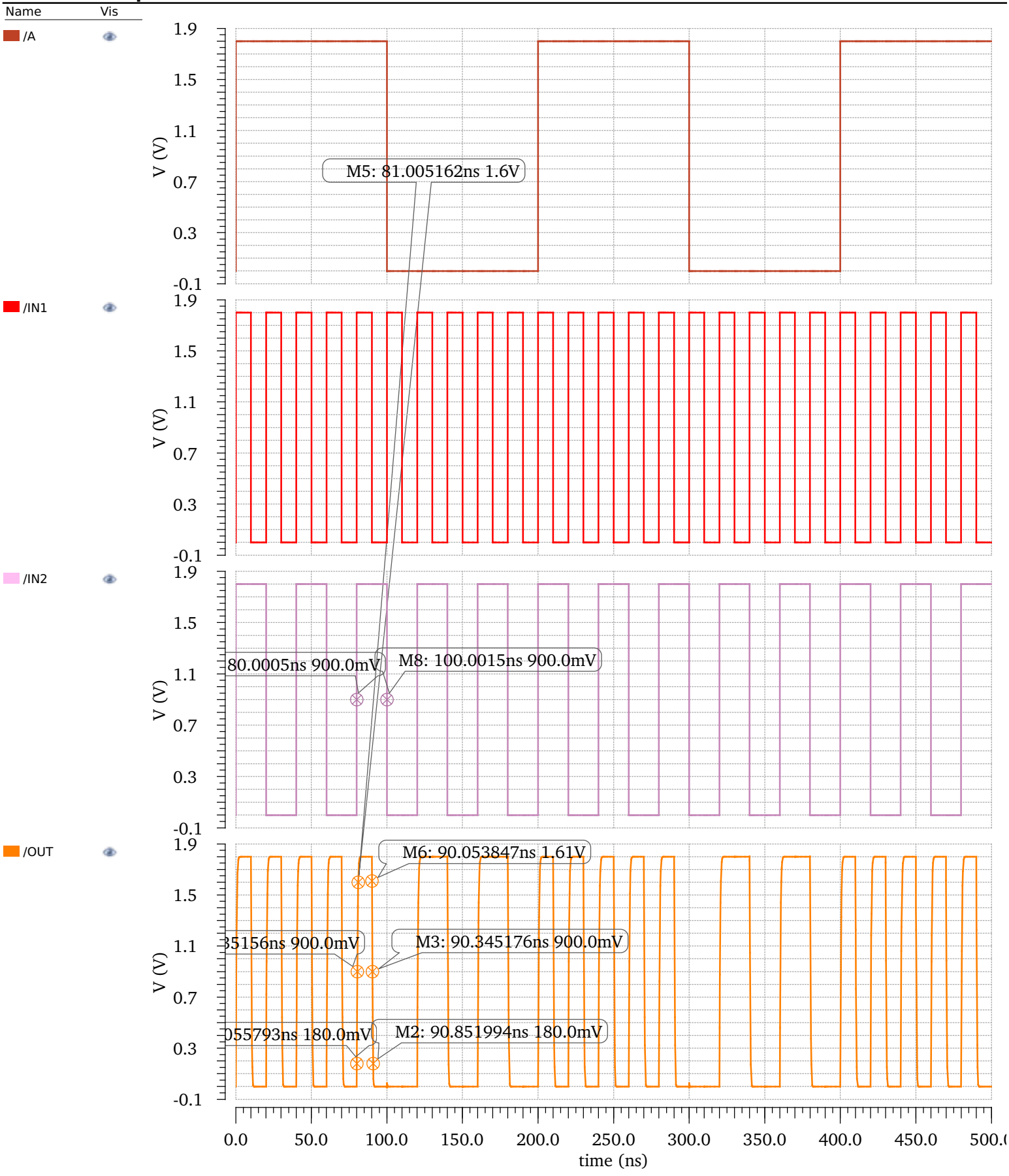
2:1 MUX


VDD
VSS
Sbar
A
B
S
Y
P0
P1
N0
N1
tsmc18dP
tsmc18dN
w=270.0n
l=180.0n
m:1
VDD
VSS
IN
OUT
Inverter
V

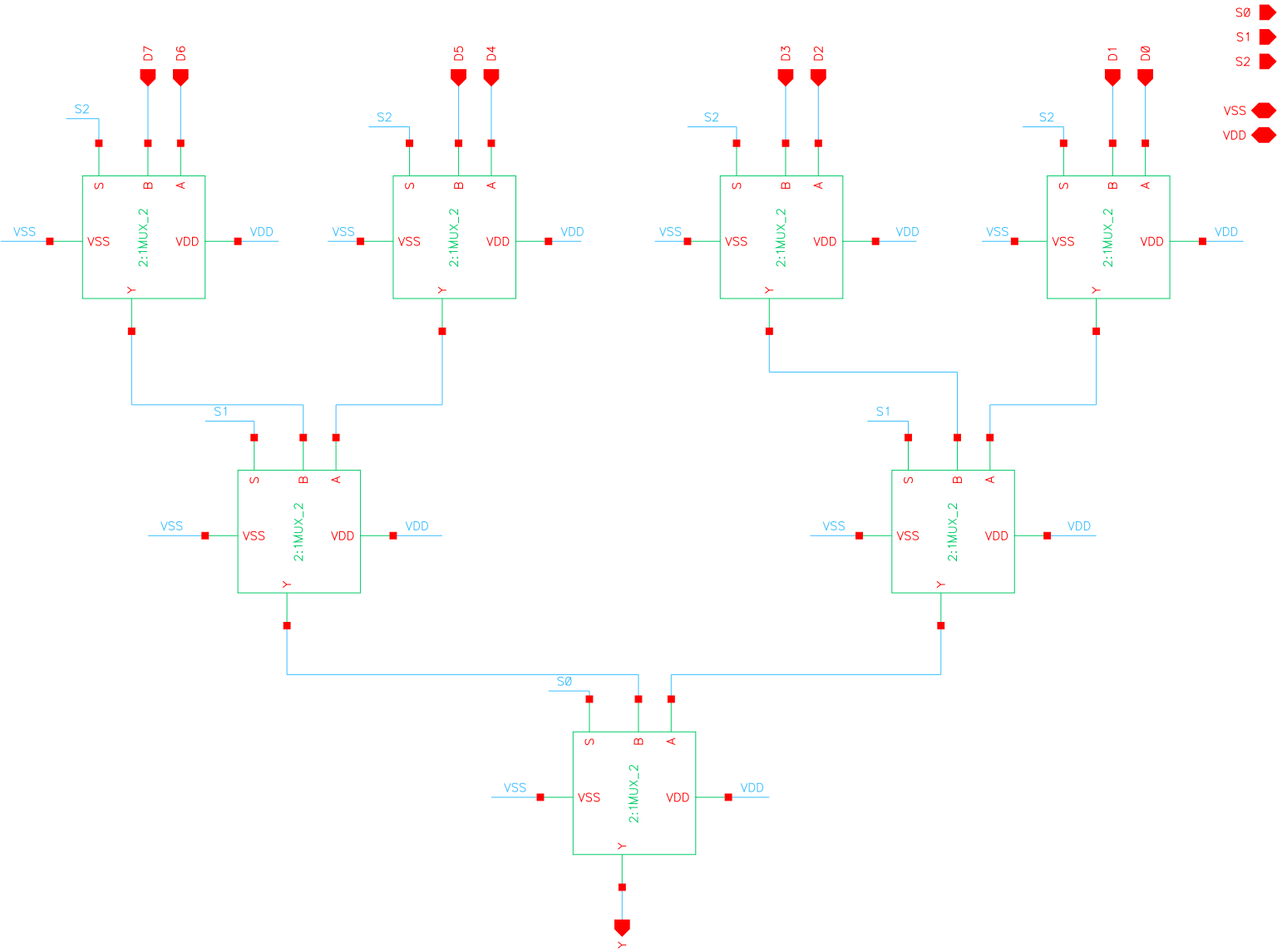

[@2:1MUX]
A
B
S
VDD
VSS
Y
[@partName]

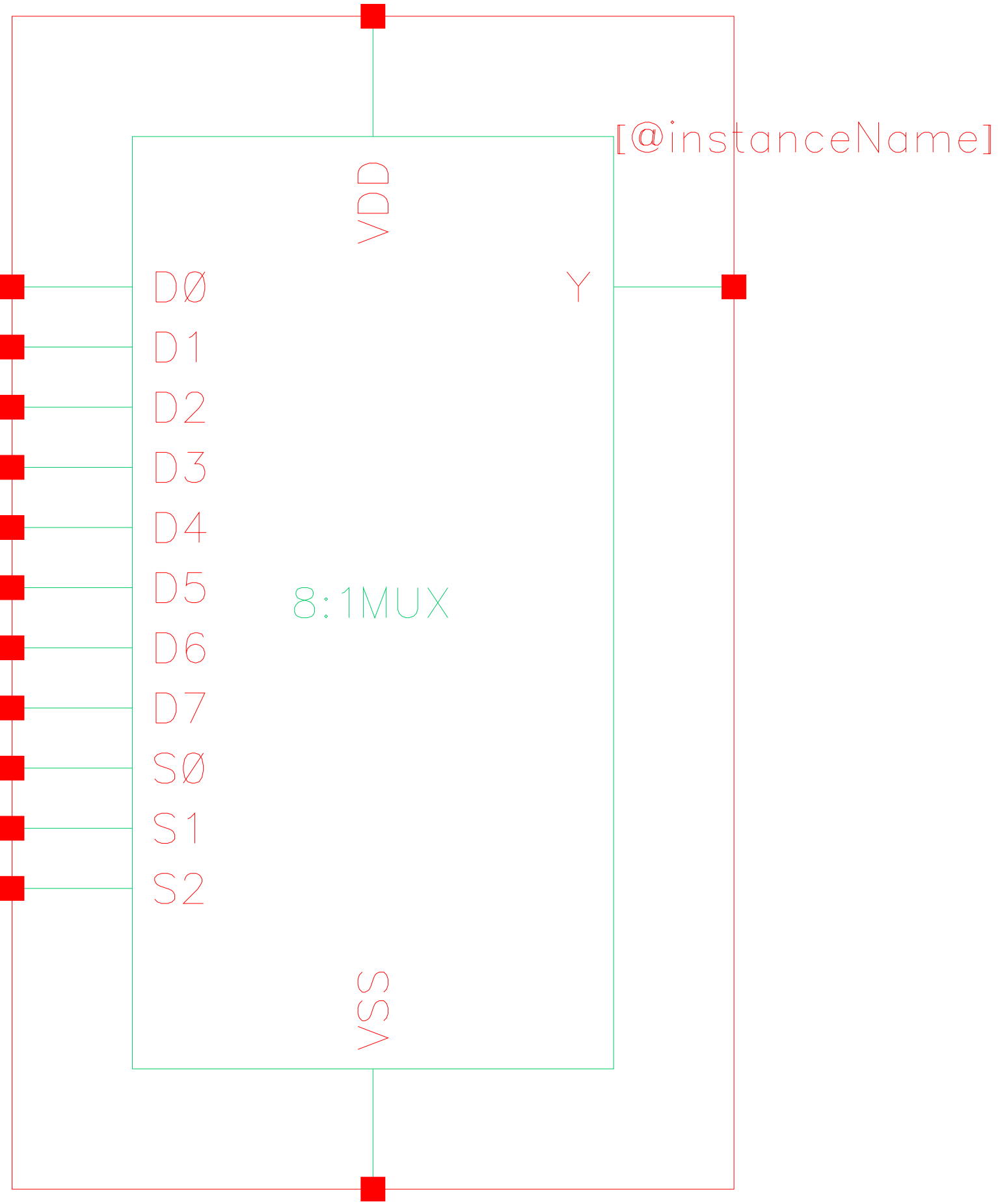

VDD
VDD
VØ
vdc=1.8
gnd!
A
B
S
A
B
S
VDD
VSS
2:1MUX_2
Y
OUT
A
V2
v1:Ø
v2=1.8
tr=1p
gnd!
B
V3
v1:Ø
v2=1.8
tr=1p
gnd!
S
V1
v1:Ø
v2=1.8
tr=1p
gnd!
OUT
CØ
c:1p
gnd!
gnd

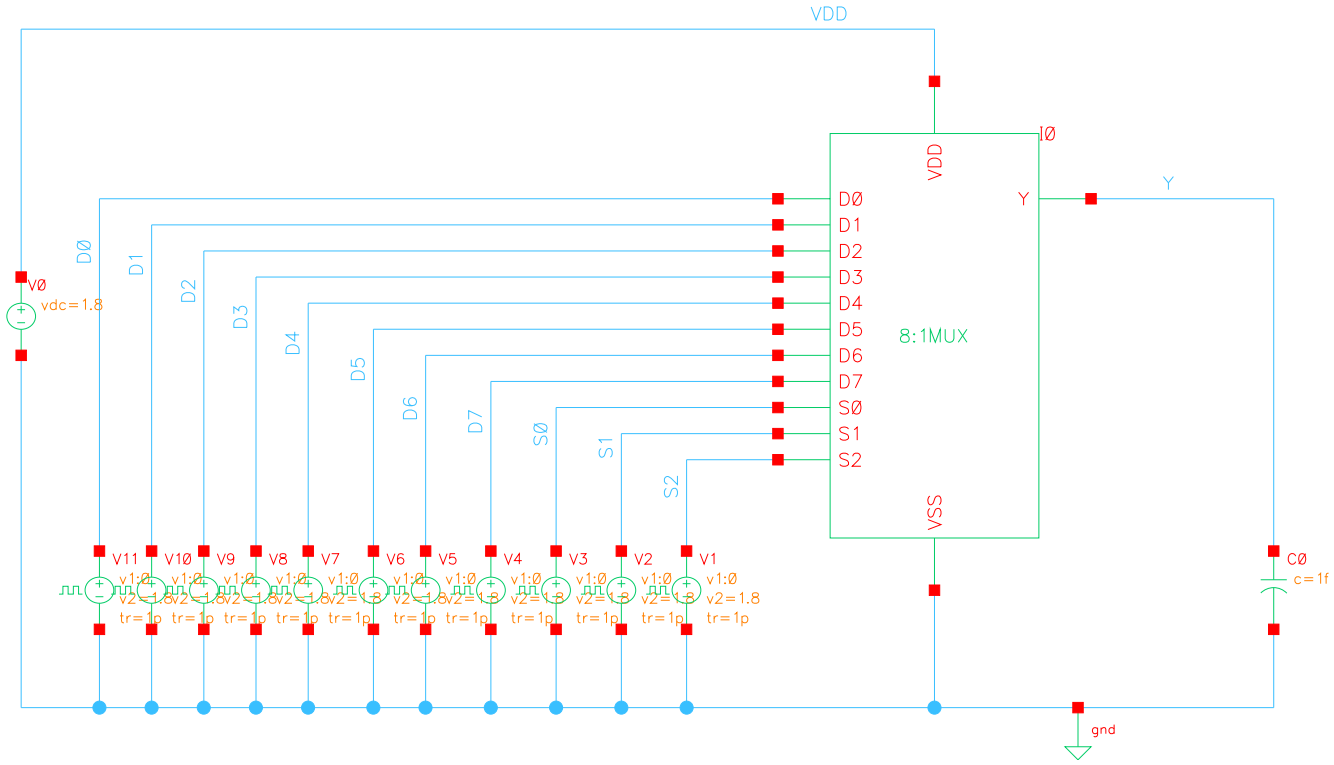
Transient Response **Fri Dec 7 18:33:58 2018**



8:1 MUX

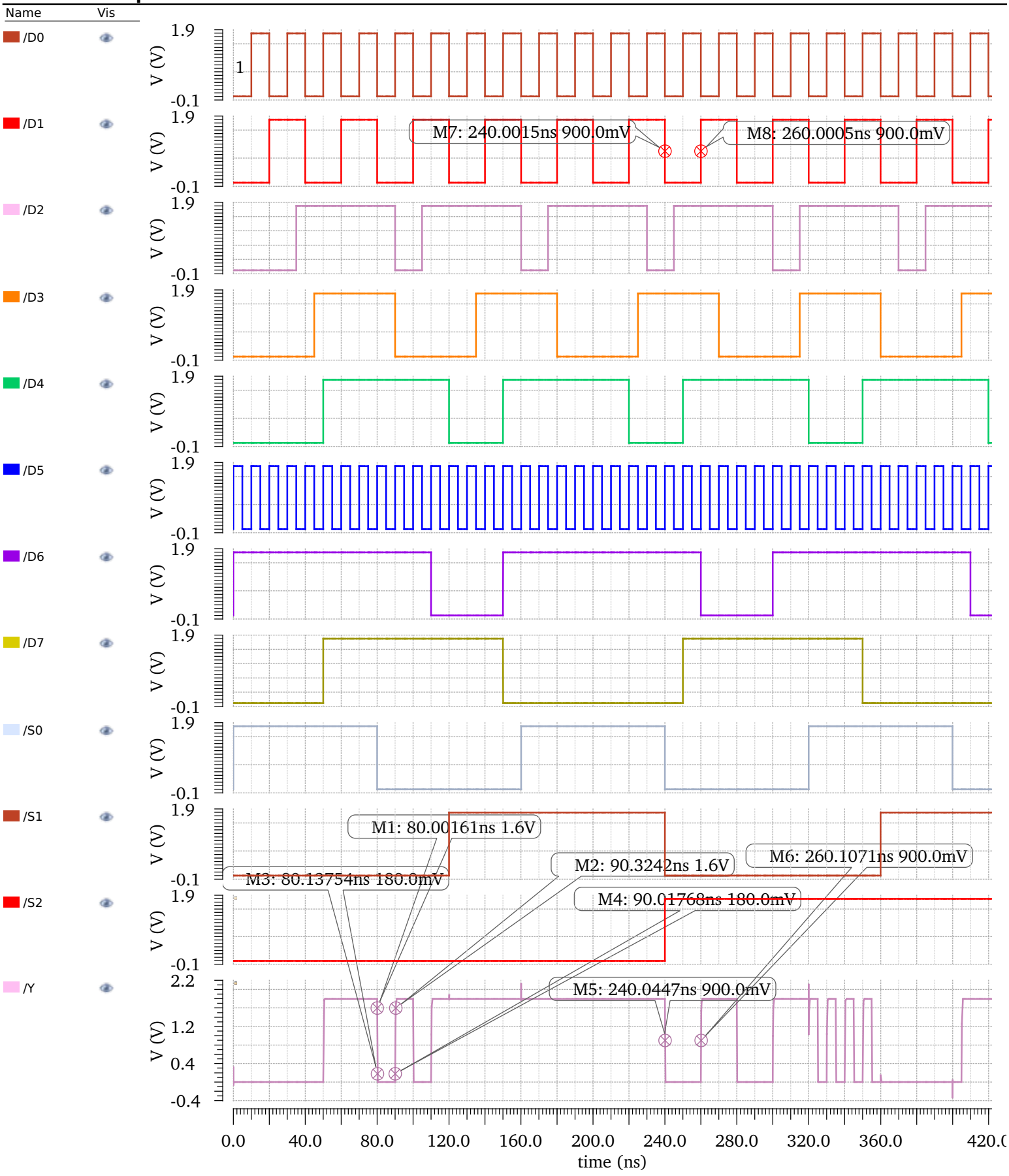

SØ
S1
S2
VSS
VDD
D7
D6
D5
D4
D3
D2
D1
D0
2:1MUX_2
S
B
A
Y
VSS
VDD
Y


[@instanceName]
VDD
D0
D1
D2
D3
D4
D5
D6
D7
S0
S1
S2
Y
8:1MUX
VSS


VDD
VDD
IØ
Y
Y
DØ
D1
D2
D3
D4
D5
D6
D7
SØ
S1
S2
8:1MUX
VSS
VØ
vdc=1.8
V11
V10
V9
V8
V7
V6
V5
V4
V3
V2
V1
v1:0
v2=1.8
tr=1p
CØ
c=1f
gnd

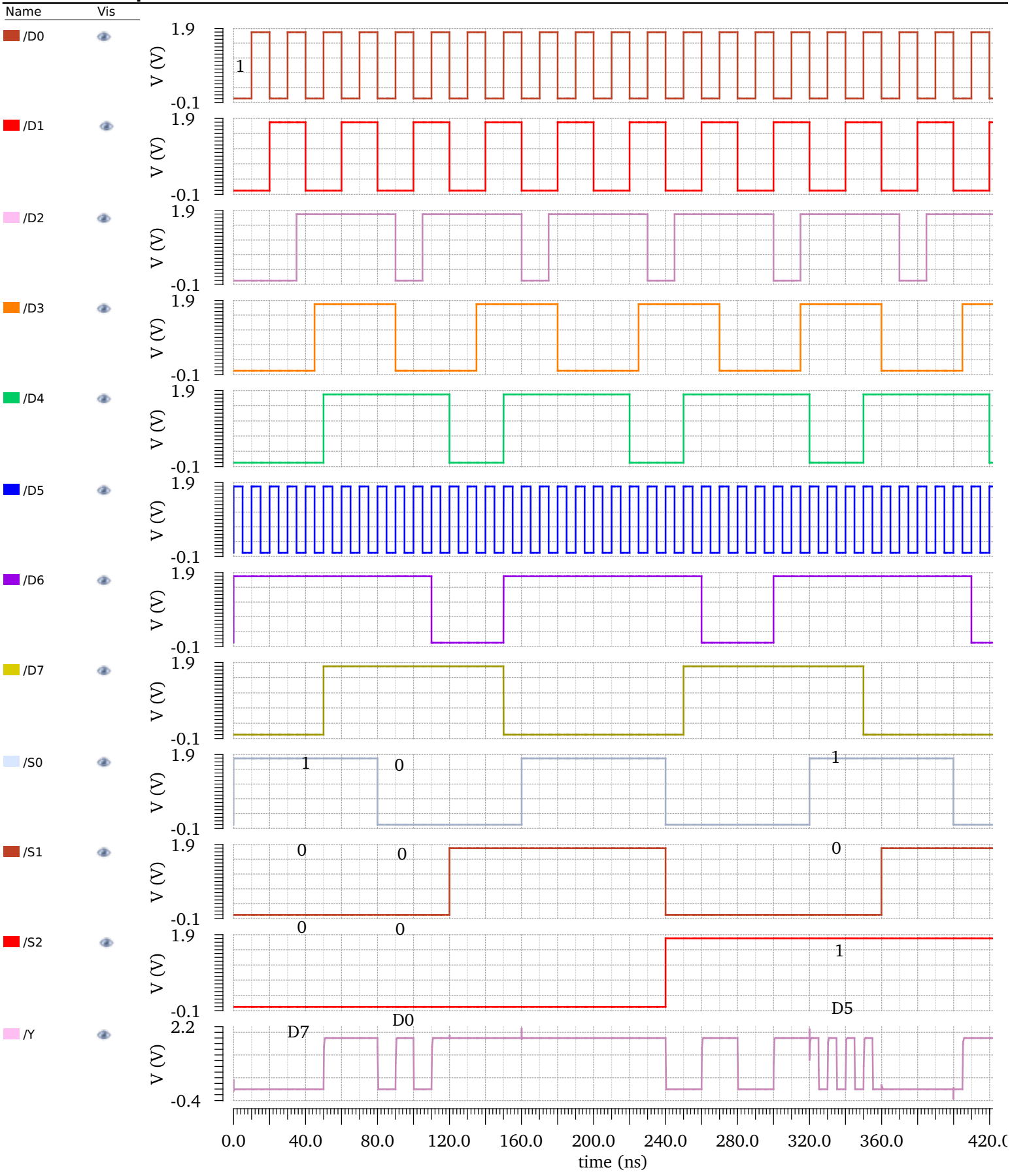
Transient Response

Fri Dec 7 21:07:43 2018

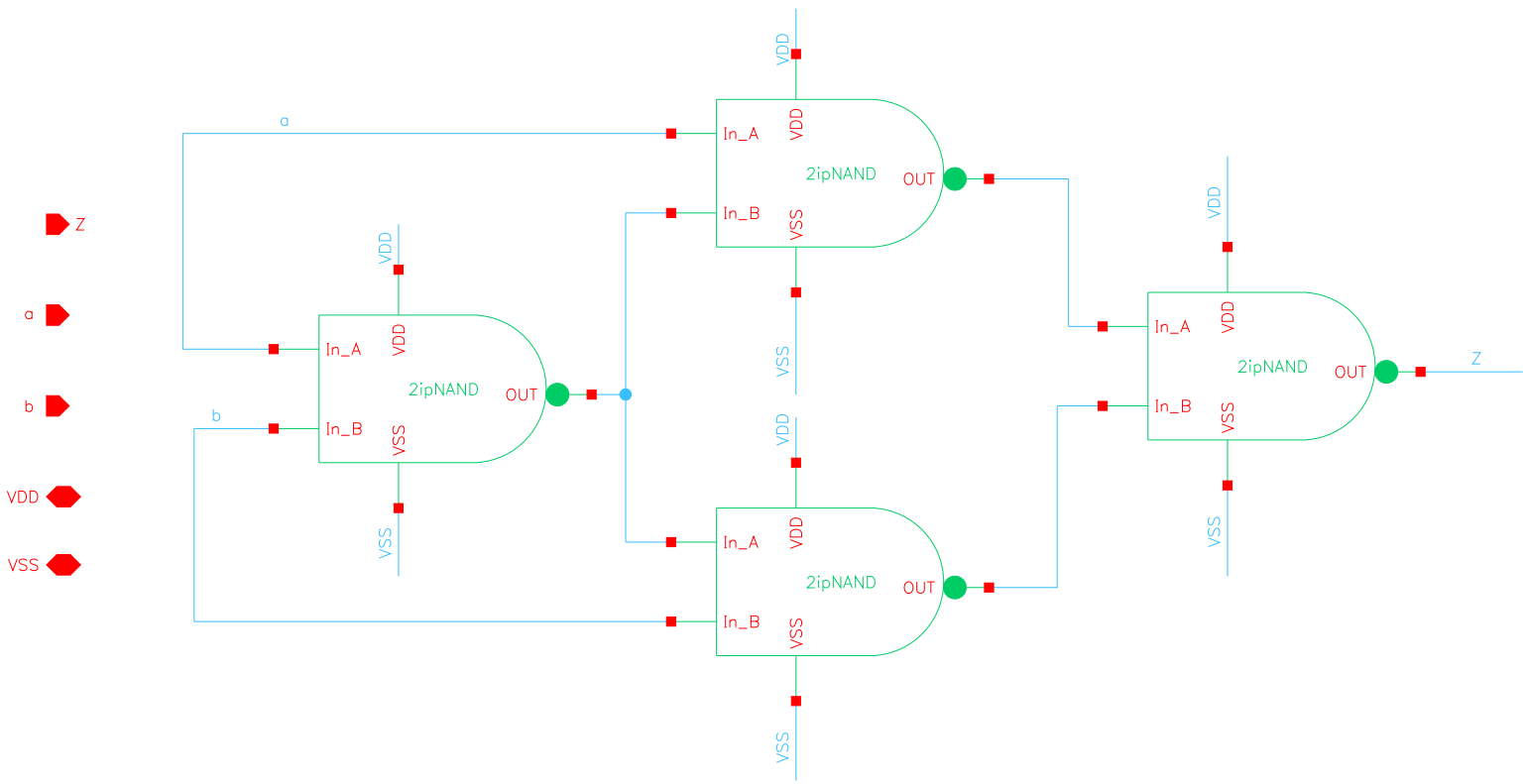


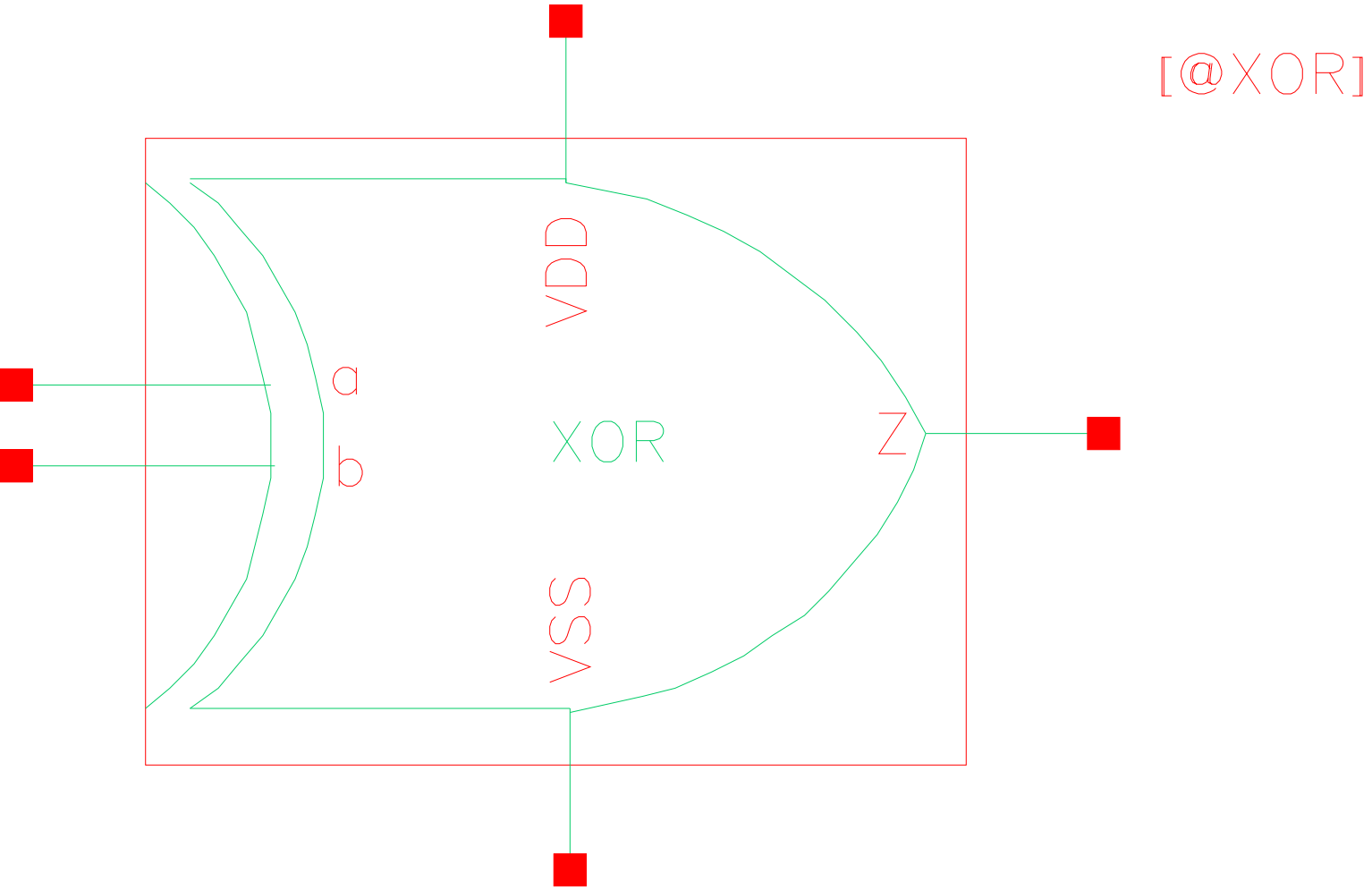
Transient Response

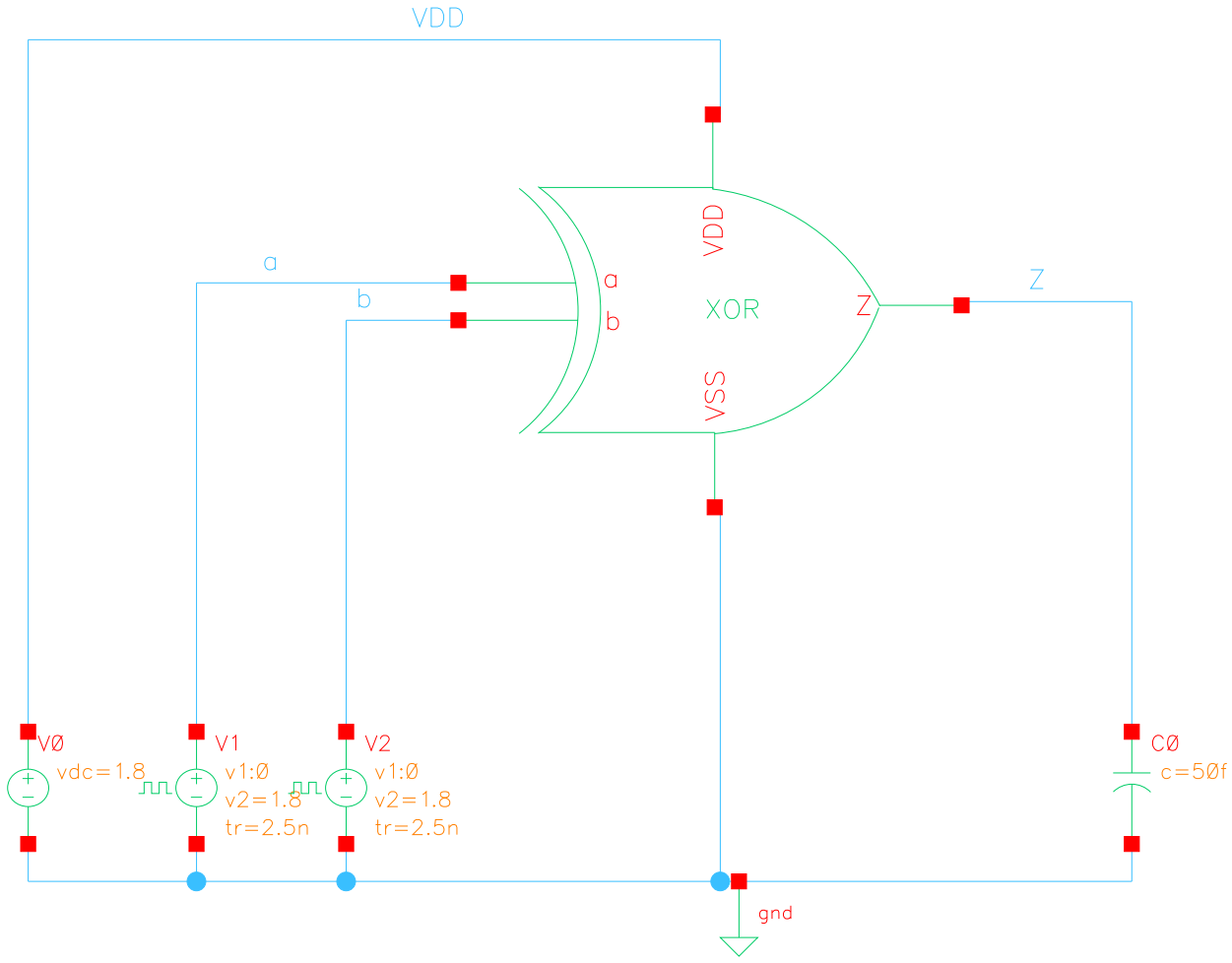
Fri Dec 7 21:07:43 2018



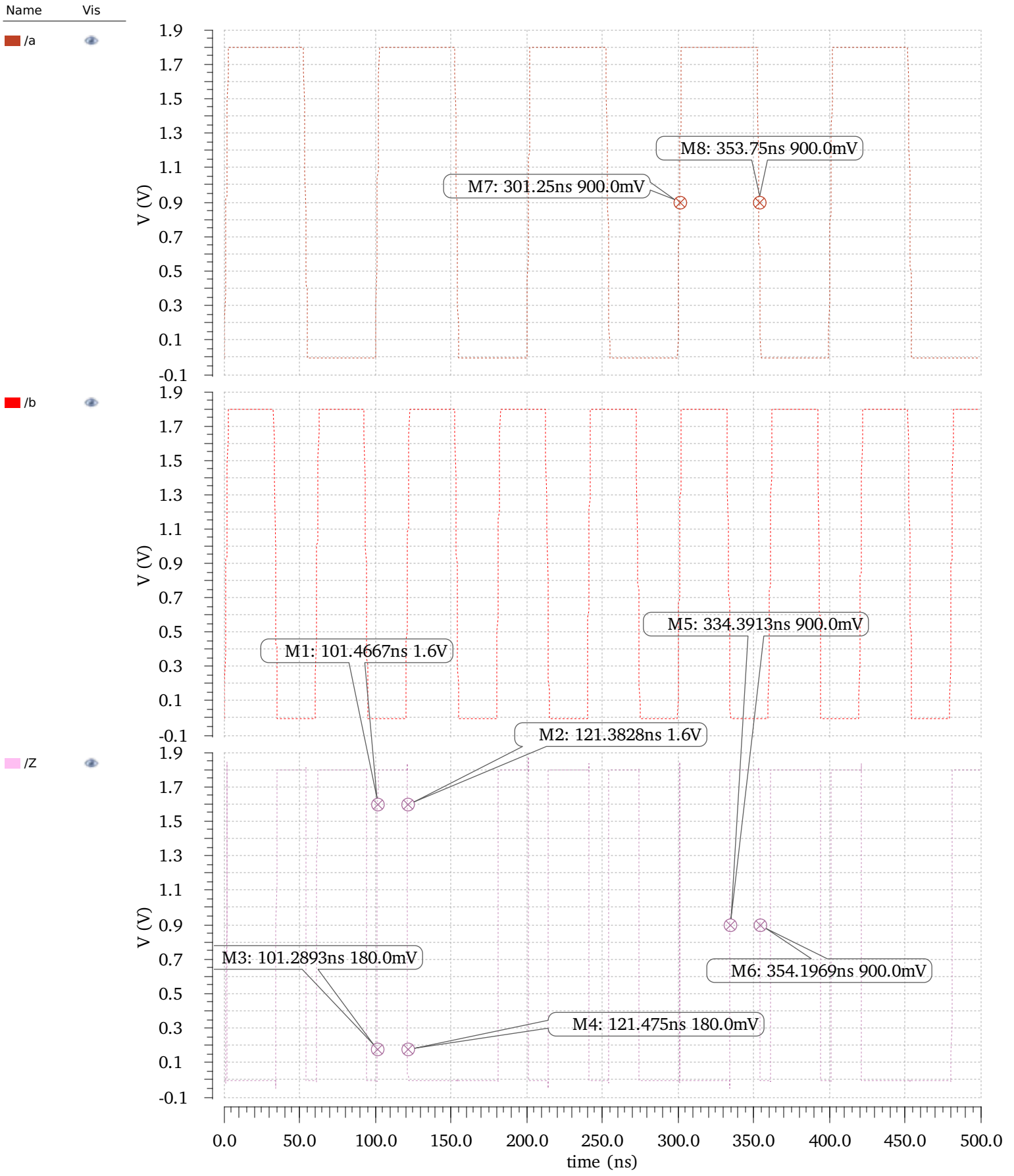
XOR


Z
a
b
VDD
VSS
a
b
VDD
In_A
VDD
2ipNAND
OUT
In_B
VSS
VSS
VDD
In_A
VDD
2ipNAND
OUT
In_B
VSS
VSS
VDD
In_A
VDD
2ipNAND
OUT
In_B
VSS
VSS
VDD
In_A
VDD
2ipNAND
OUT
In_B
VSS
VSS
Z

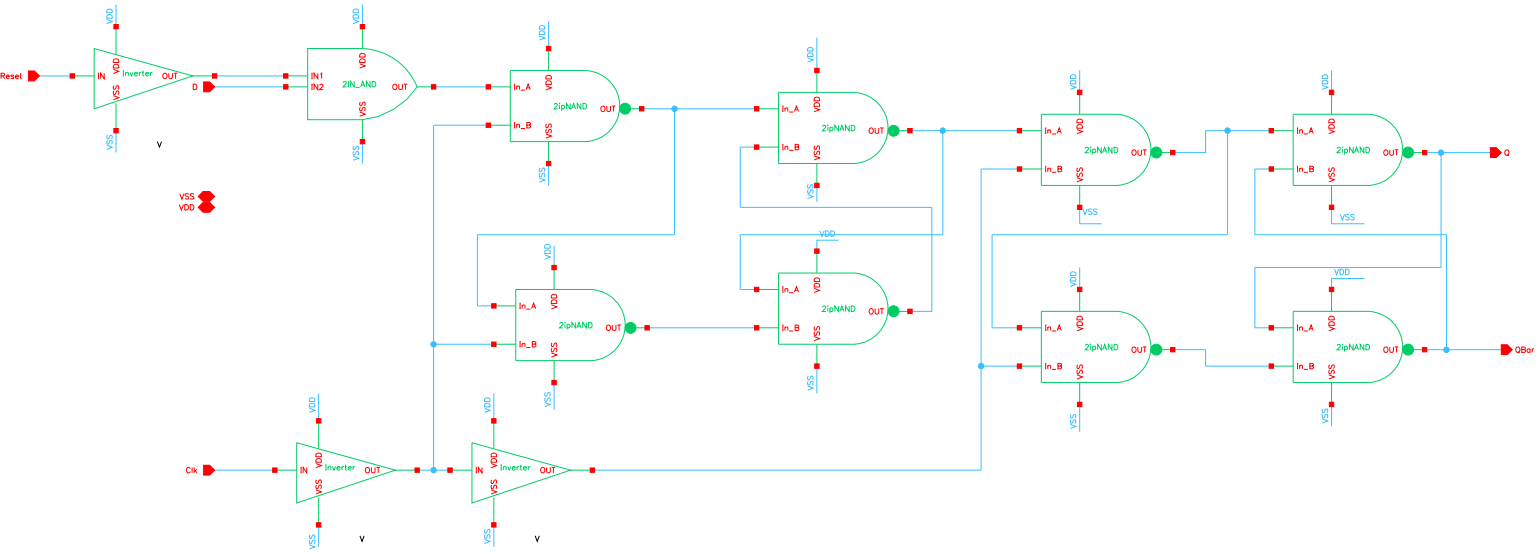

[@XOR]
VDD
a
b
XOR
Z
VSS

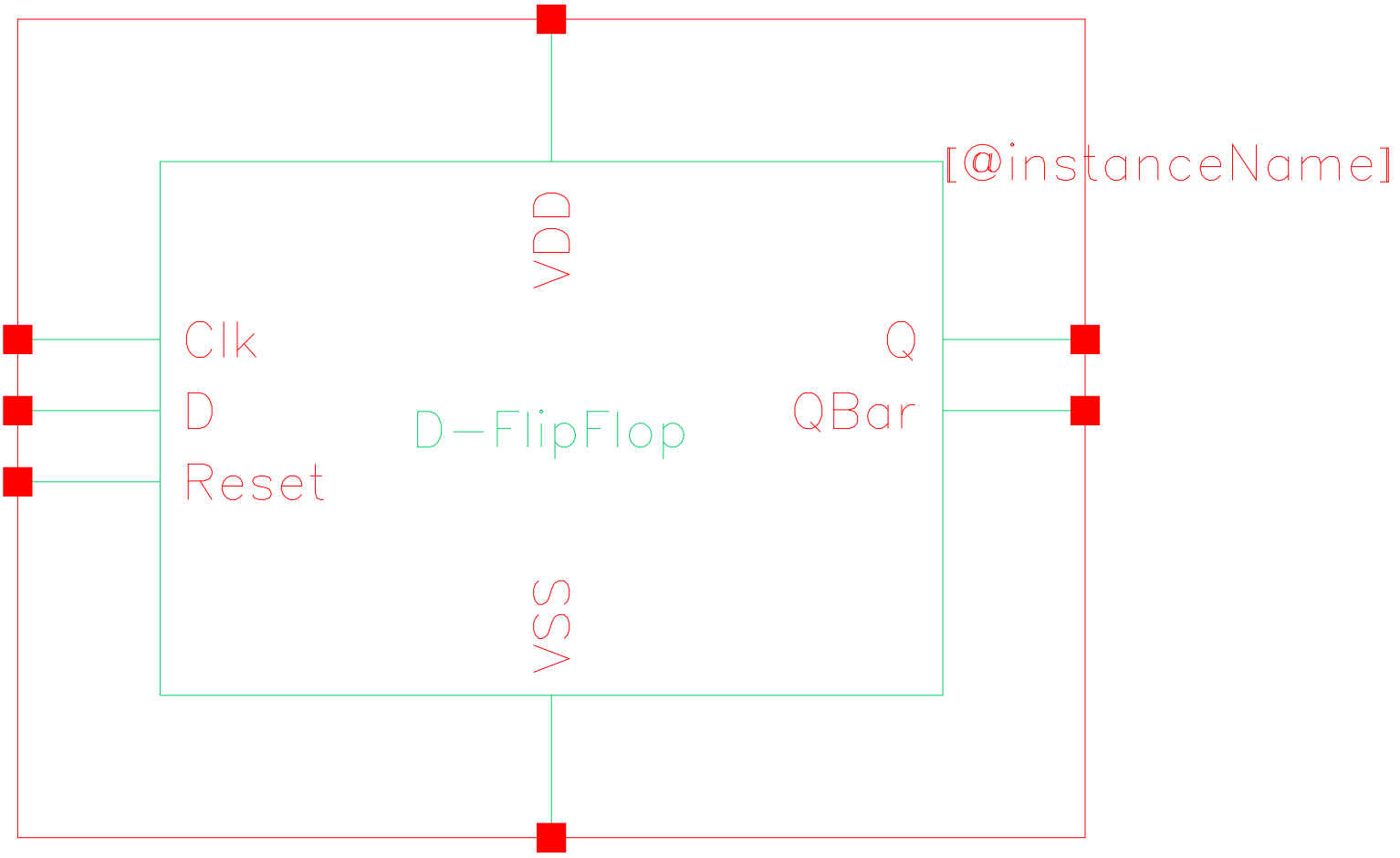

VDD
a
b
a
b
XOR
VDD
VSS
Z
Z
V0
vdc=1.8
V1
v1:0
v2=1.8
tr=2.5n
V2
v1:0
v2=1.8
tr=2.5n
C0
c=50f
gnd

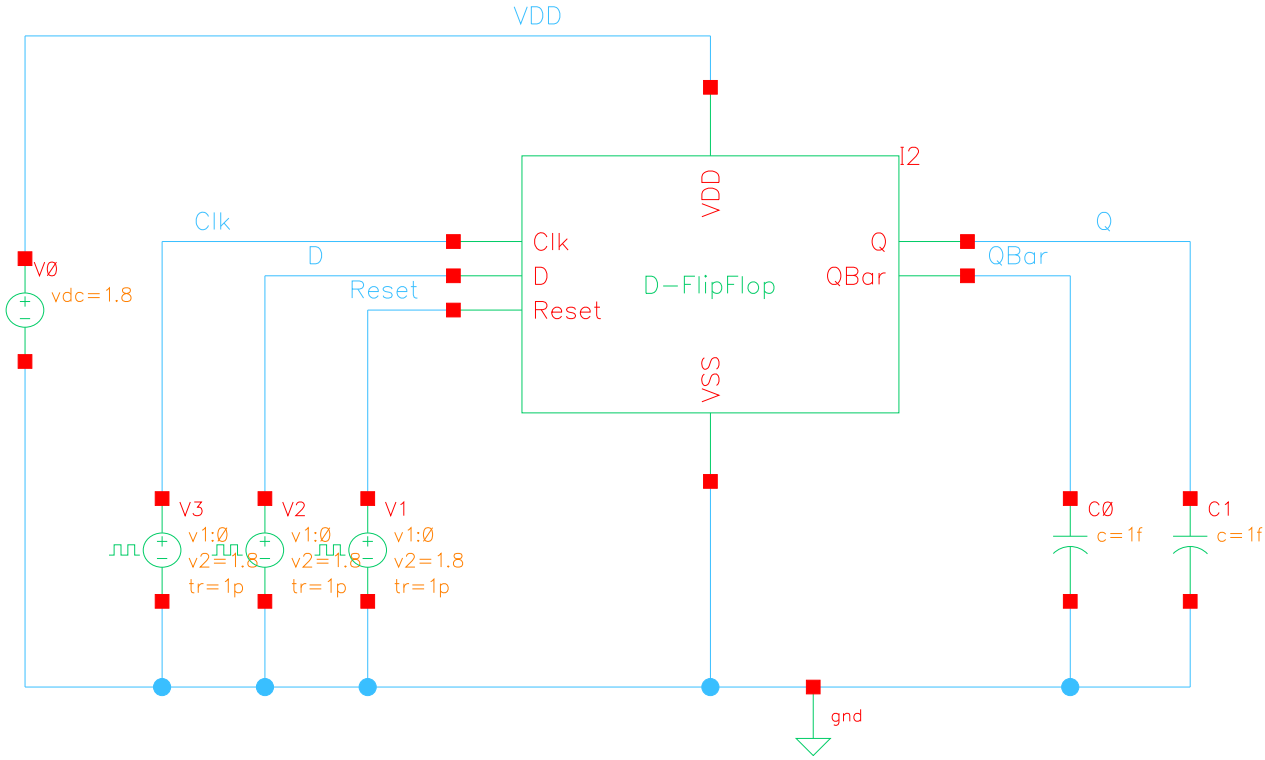
Transient Response **Fri Dec 7 23:24:51 2018**



D Flip Flop

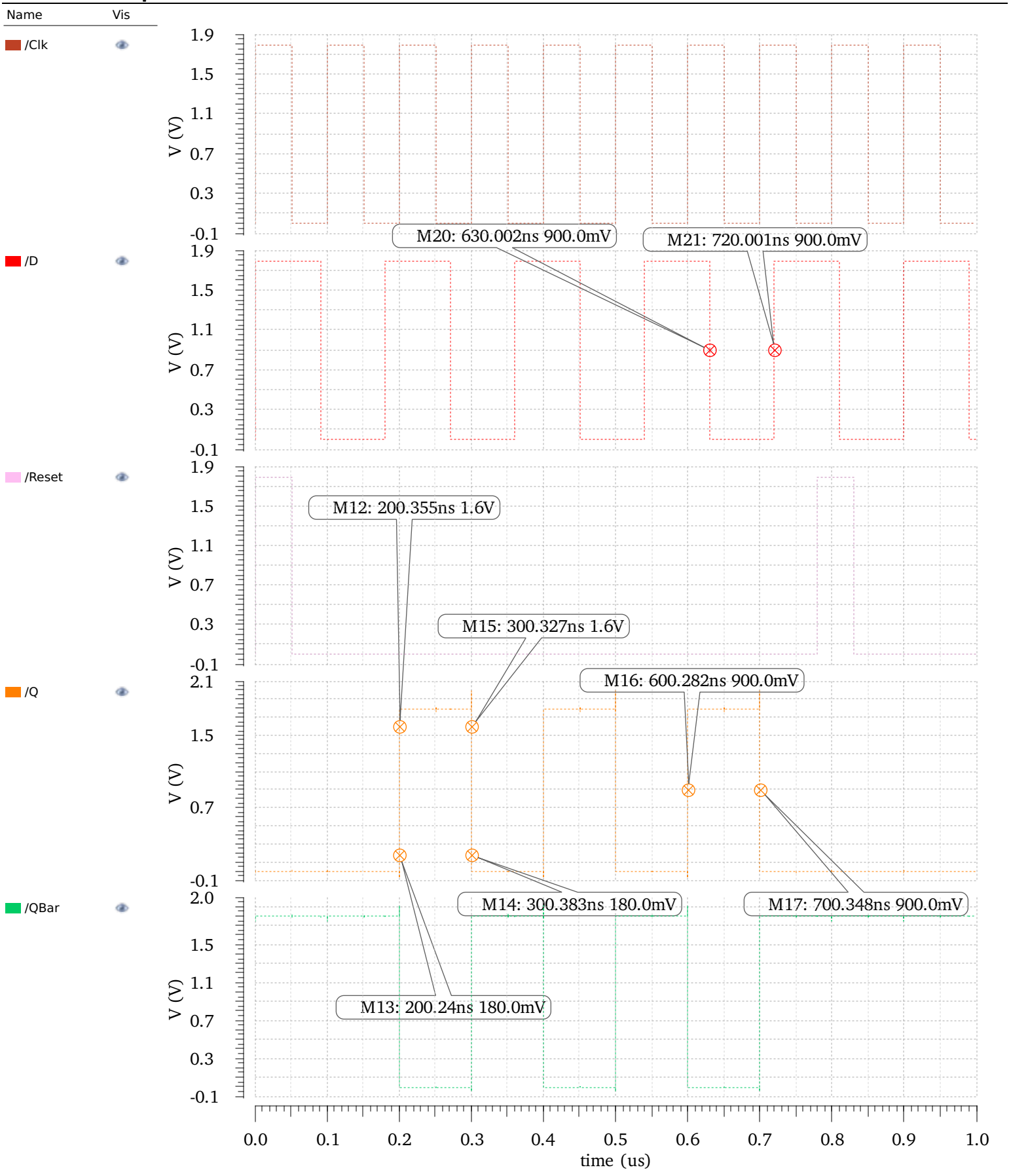

Reset
Clk
D
Q
QBar
Inverter
2IN_AND
2ipNAND
IN
IN1
IN2
OUT
In_A
In_B
VDD
VSS
V


[@instanceName]
VDD
Clk
D
Reset
D_FlipFlop
Q
QBar
VSS

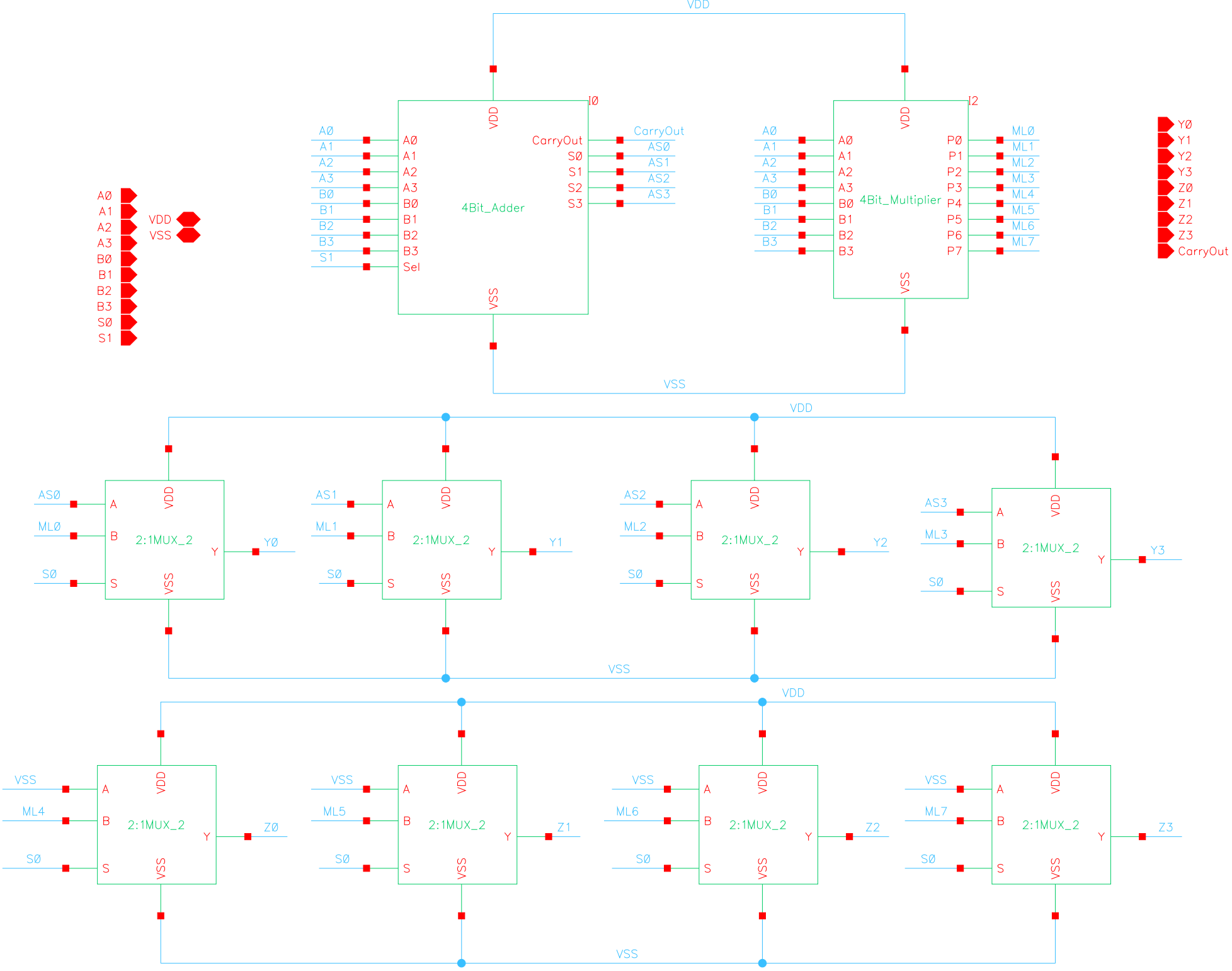

VDD
I2
VDD
Clk
Clk
D
Reset
D
Reset
D−FlipFlop
Q
QBar
VSS
Q
QBar
VØ
vdc=1.8
V3
v1:Ø
v2=1.8
tr=1p
V2
v1:Ø
v2=1.8
tr=1p
V1
v1:Ø
v2=1.8
tr=1p
CØ
c=1f
C1
c=1f
gnd

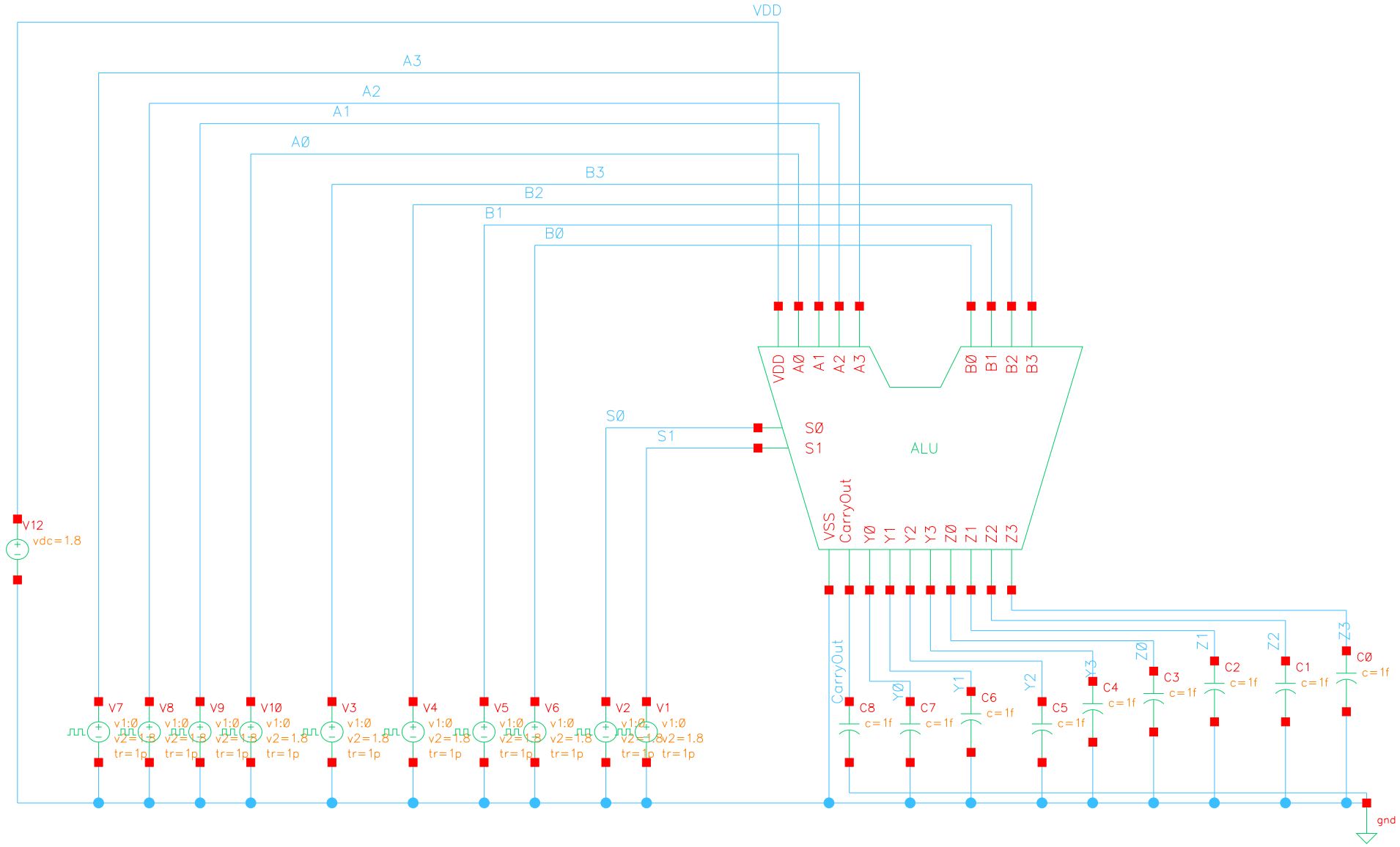
Transient Response

Fri Dec 7 23:09:24 2018



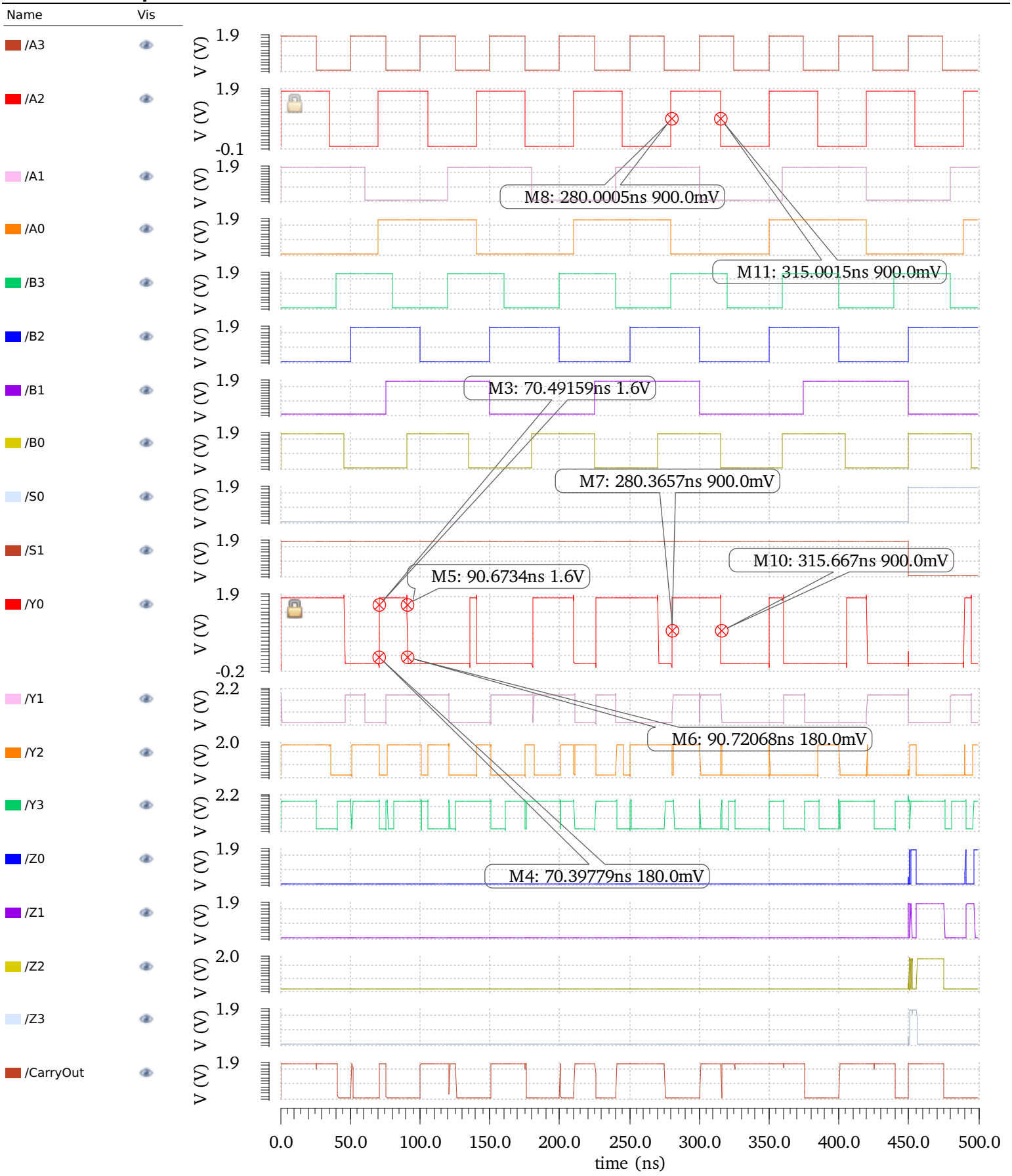
ALU


A0
A1
A2
A3
B0
B1
B2
B3
S0
S1
VDD
VSS
I0
4Bit_Adder
Sel
CarryOut
AS0
AS1
AS2
AS3
I2
4Bit_Multiplier
P0
P1
P2
P3
P4
P5
P6
P7
ML0
ML1
ML2
ML3
ML4
ML5
ML6
ML7
Y0
Y1
Y2
Y3
Z0
Z1
Z2
Z3
2:1MUX_2
A
B
S
Y


VDD
A3
A2
A1
A0
B3
B2
B1
B0
SØ
S1
ALU
VDD
A0
A1
A2
A3
B0
B1
B2
B3
VSS
CarryOut
Y0
Y1
Y2
Y3
Z0
Z1
Z2
Z3
V12
vdc=1.8
V7
V8
V9
V10
V3
V4
V5
V6
V2
V1
v1:0
v2=1.8
tr=1p
C8
C7
C6
C5
C4
C3
C2
C1
C0
c=1f
gnd

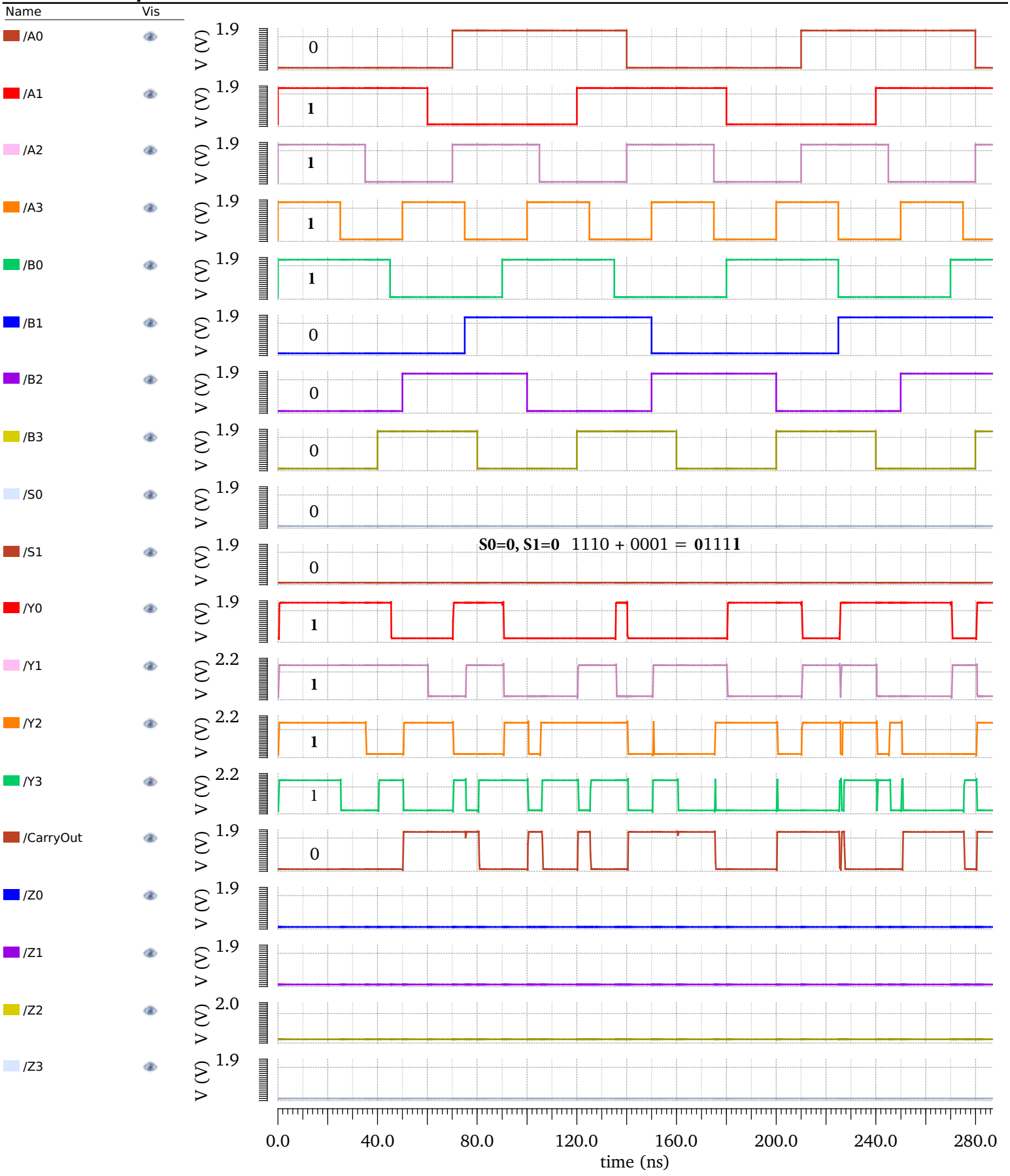
Transient Response

Fri Dec 7 22:44:33 2018



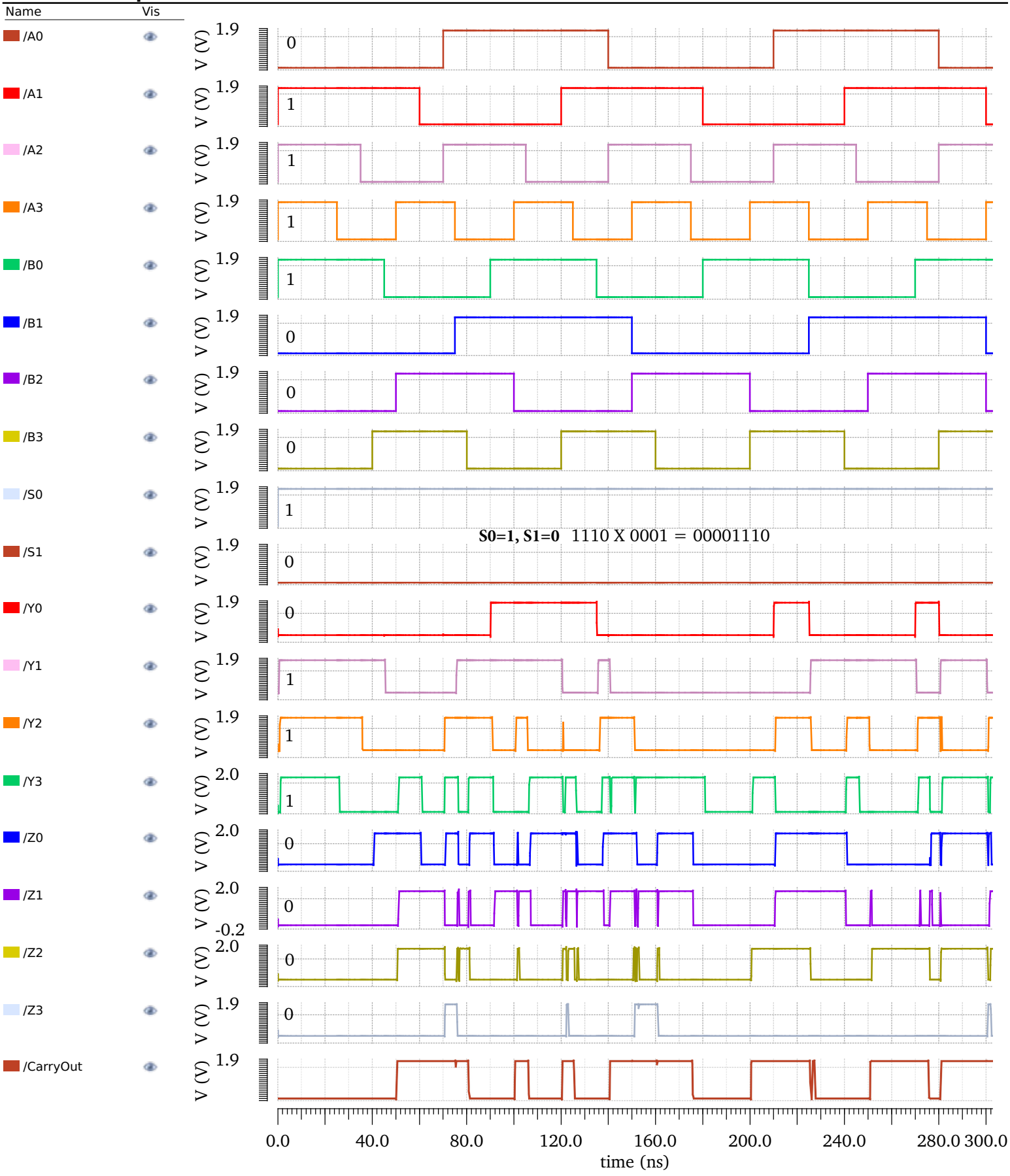
Transient Response

Thu Dec 6 22:26:59 2018



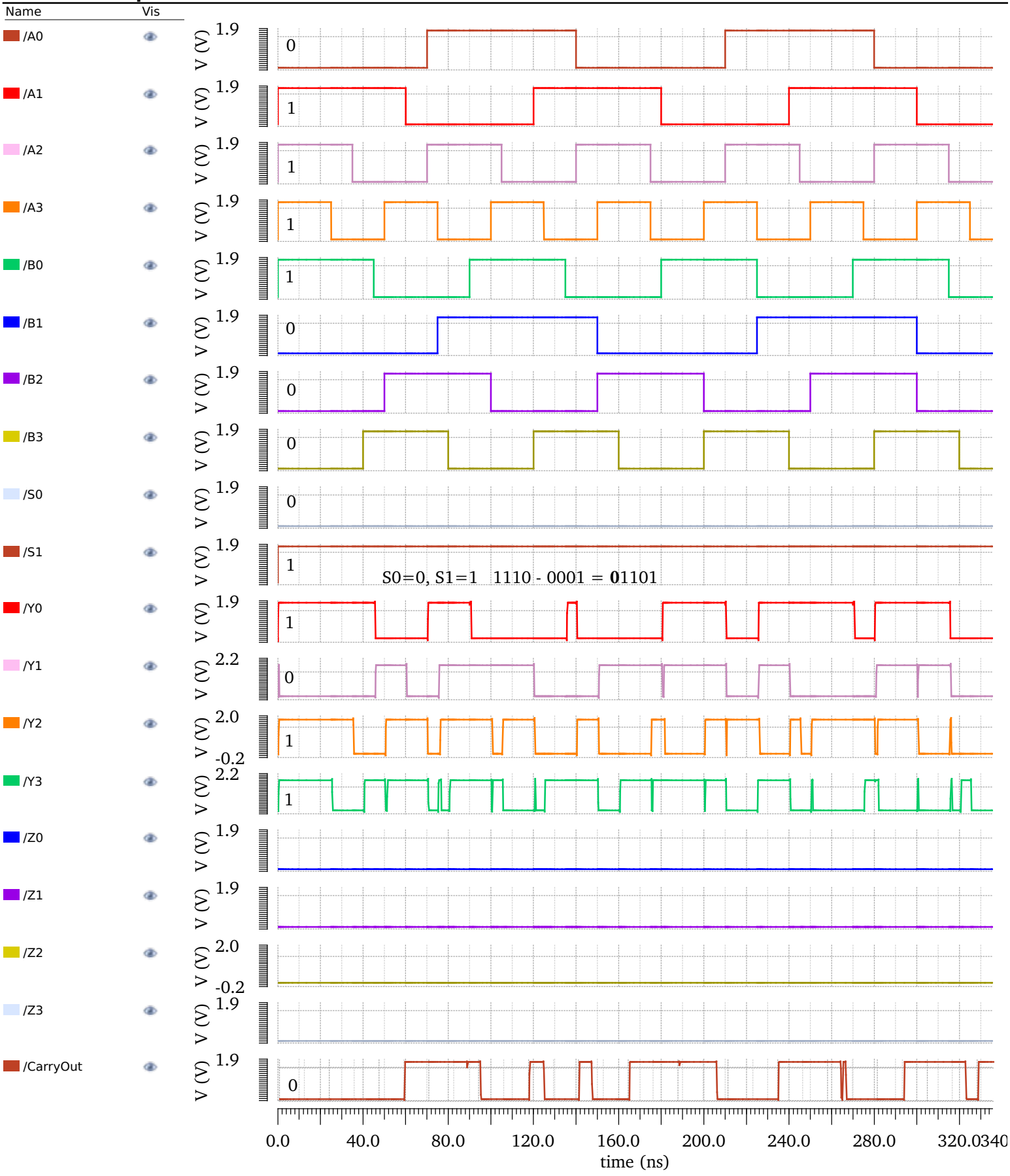
Transient Response

Thu Dec 6 23:30:15 2018



Transient Response

Thu Dec 6 23:59:26 2018



Calculation

Rise Time and Fall Time Calculation

Rise Time= (at 90% Output) - (at 10% Output)

Fall Time = (at (10% Output) - (at 90% Output)

Propagation Delay

Propagation Delay(rising $t_{pdr)}$= 50% of Output time - 50% of Input time
Propagation Delay(falling t_{pdf})= 50% of Output time - 50% of Input time

Average Propagation Delay = (t_{pdr}+t_{pdf})/2

Gate	tr	tf	tpdr	tpdf	Average(Tpdr+tpdf)/2
Inverter	2.17ns	1.67ns	1.02ns	0.9ns	0.96ns
NAND	2.20ns	0.99ns	1.05ns	0.519ns	0.788ns
AND	0.7ns	0.6ns	0.89ns	1.025ns	0.95ns
NOR	3.26ns	0.57ns	1.56ns	0.31ns	0.936ns
OR	0.457ns	0.17ns	0.36ns	0.06ns	0.21s
XOR	2.17ns	1.67ns	0.9ns	1.02ns	0.96ns
TM Gate	0.32ns	0.2ns	0.12ns	0.079ns	0.095ns
1 Bit Half Adder	1.24ns	1.05ns	0.15ns	0.24ns	0.19ns
1 Bit Full Adder	0.18ns	0.09ns	0.36ns	0.34ns	0.35ns
4 Bit Fuller Adder	0.1ns	1.05ns	1.42ns	1.00ns	2.71ns
Multiplier	0.17ns	0.36ns	0.36ns	0.93ns	0.645ns
D Flip-Flop	1.29ns	1.02ns	2.65ns	1.26ns	1.95
2:1 MUX	0.59ns	0.43ns	1.02ns	0.59ns	0.805ns
8:1 MUX	0.12ns	0.25ns	0.04ns	0.107ns	0.03ns
ALU	0.1ns	0.54ns	0.3ns	0.667ns	0.48ns

CONCLUSION:

Thus the layout of the ALU is designed using the basic gates and the Post Simulation results are obtained.