1. Introduction

The goal of this project was to design and simulate a five-transistor operational transconductance amplifier (5T-OTA) using 45nm CMOS technology in Cadence Virtuoso. The amplifier was expected to meet specific performance criteria related to gain, bandwidth, power consumption, and output swing.

2. Procedure (Brief Overview) & Results:

- Created 5T-OTA schematic in Cadence using gpdk45 NMOS and PMOS devices
- Configured differential inputs with 180° phase difference
- Set up a 10 µA tail current using a current mirror
- Sized transistors based on gain, swing, and bandwidth requirements
- Connected a 100 fF load capacitor in the testbench
- Verified all transistor DC operating points
- Ran AC analysis to measure voltage gain, 3-dB bandwidth, and GBW
- Ran transient analysis with a 10 mV, 100 MHz sine input to observe amplifier response
- Performed large-signal transient simulation to measure peak-to-peak output swing
- Recorded simulation plots and extracted key performance metrics

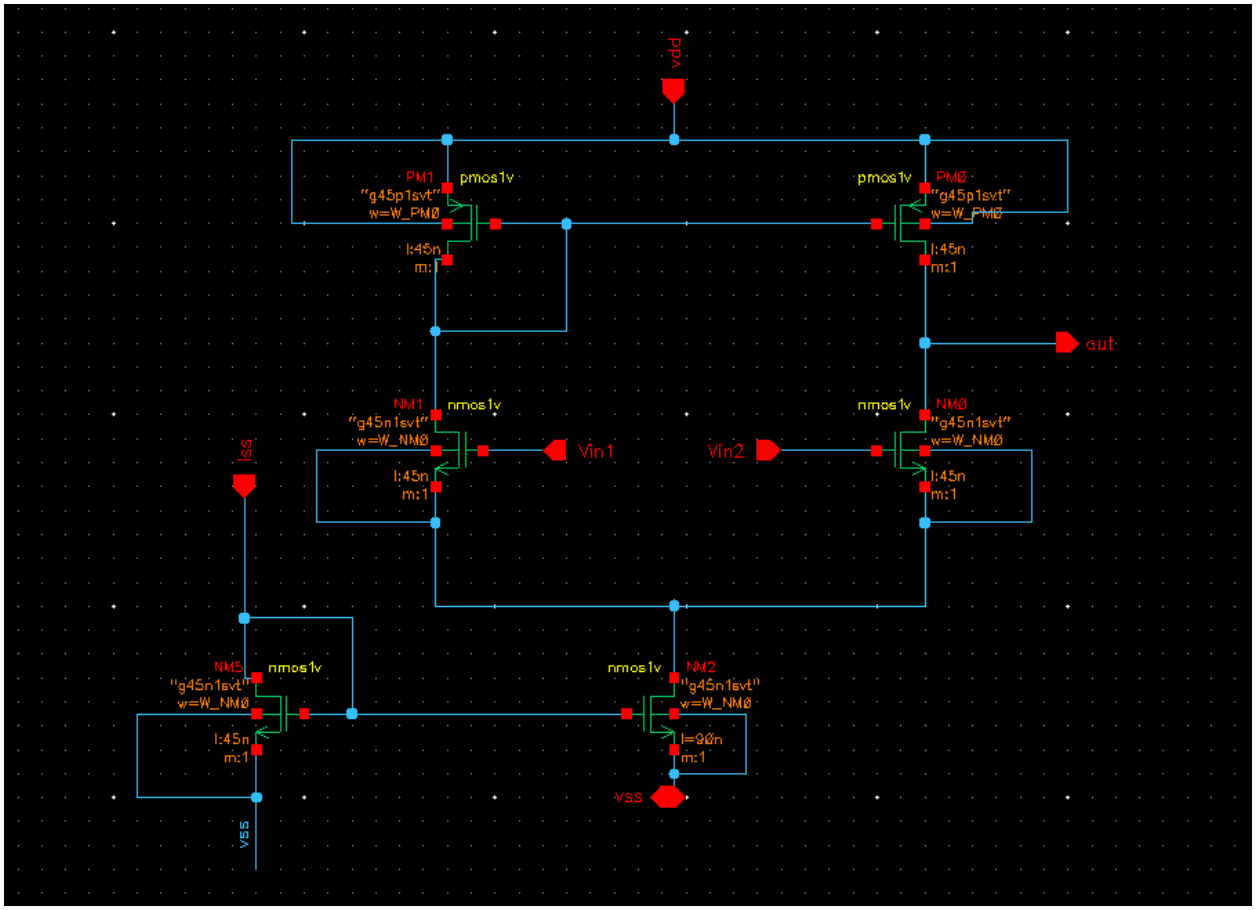

Figure: Circuit schematic for the 5 OTA

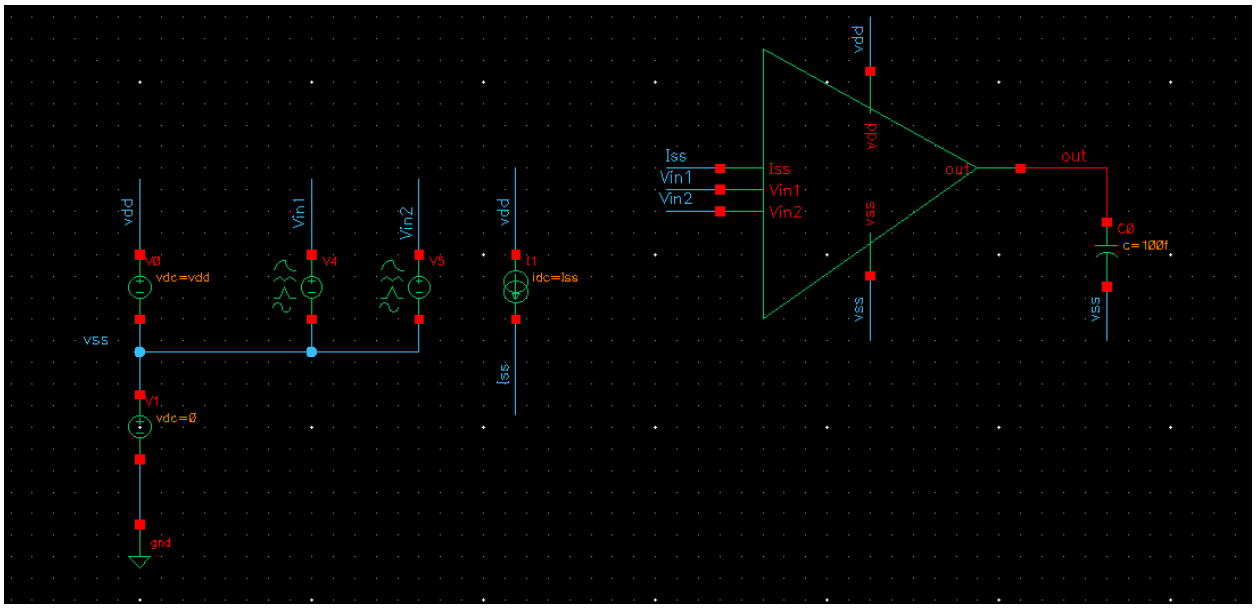

Figure: Circuit testbench for the 5 OTA

NMOS	Num. of fingers	Multiplicity	W (all fingers)	L	I_d	g_m	V_{gs}	V_{ds}
NM0, NM1	16	1	1.0 um	45nm	5 uA	50	0.9	1
NM2 (Current source)	40	1	1.0 um	90nm	10 uA	100	0.9	1.1
NM3 (Current mirror)	2	1	1.0 um	90nm	5 uA	50 or 47.1	0.9	1

PMOS	Num. of fingers	Multiplicity	W (all fingers)	L	I_d	g_m	V_{gs}	V_{ds}
PM0, PM1	16	1	0.8 um	45nm	5 uA	28.3	-0.98	1

Figure: Q-point values for the transistors

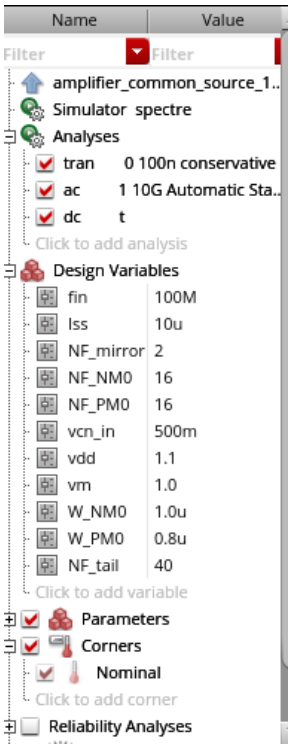

Figure: Values from Cadence

Specification	Value
Power Supply Voltage	1.1 V
Voltage Gain	> 15 dB
Peak to peak output swing	> 1 V
3-dB gain bandwidth	> 500 MHz
Power Consumption	< 2 mW
Gain-bandwidth product	> 2.5 GHz
Load	100 fF capacitor

Figure: Constraints for the 5-OTA

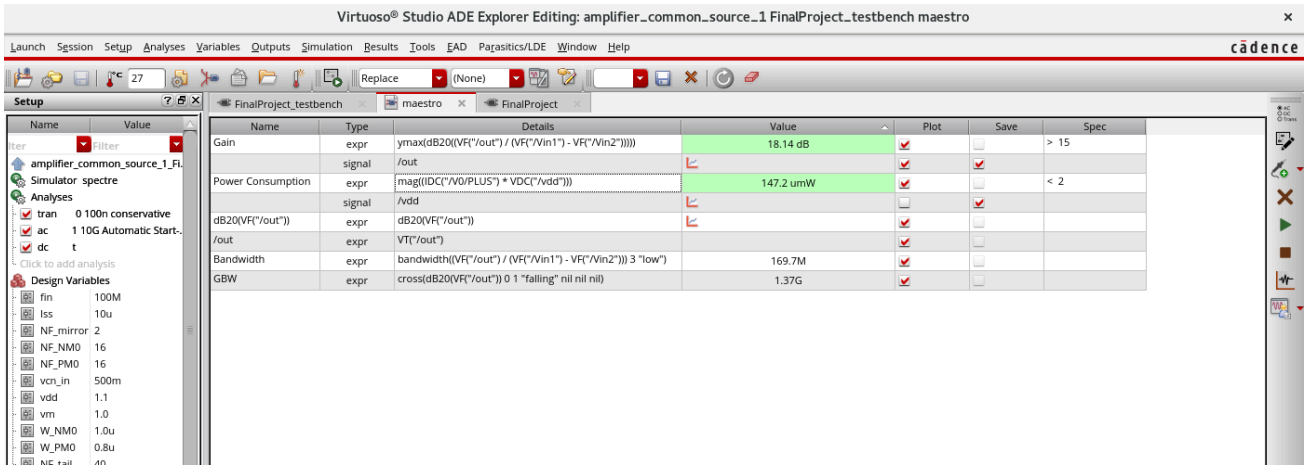

Figure: Simulation results for the constraints

Low frequency gain = 18.144 dB > 15dB (dB value at lower frequencies)
3-dB gain bandwidth = 558.4 MHz > 500 MHz (Low frequency gain dB value - 3)
Gain bandwidth product = 2.58 GHz > 2.5 GHz (Measured when dB crosses 0)
Output swing = 1.100036V > 1V
Power consumption = 147.2 umW < 2 mW
Load = 100 fF

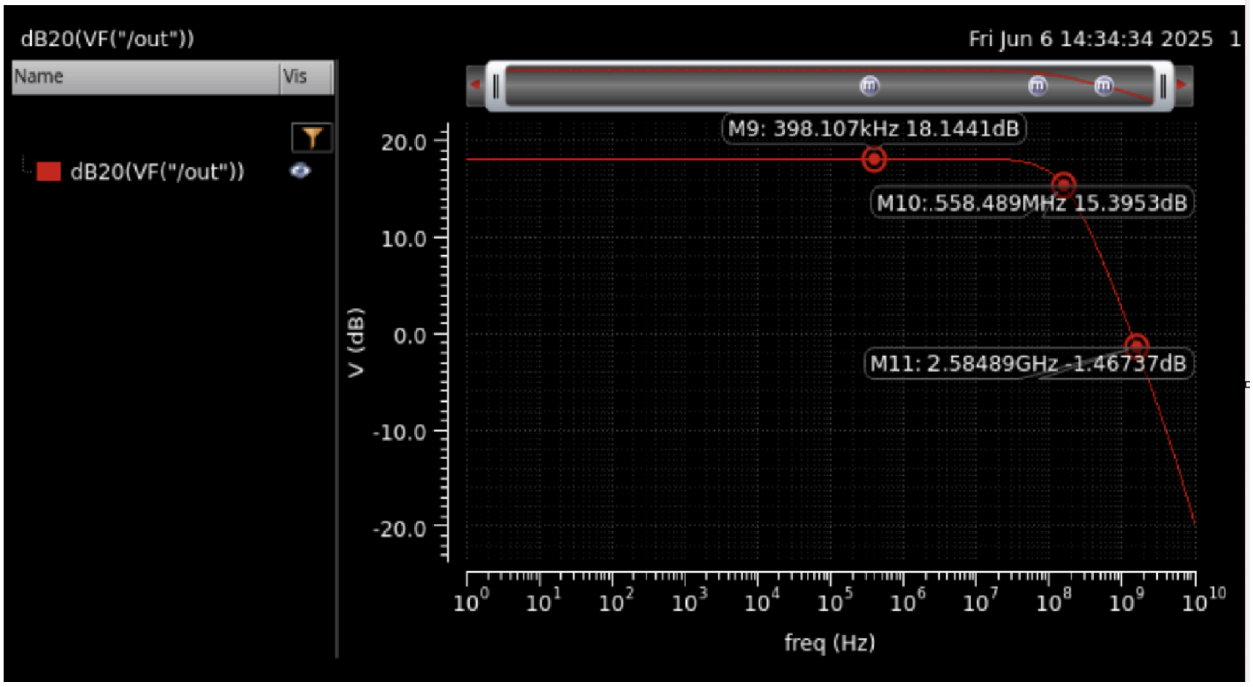

Figure: low-frequency gain, 3-dB gain bandwidth, and gain-bandwidth product

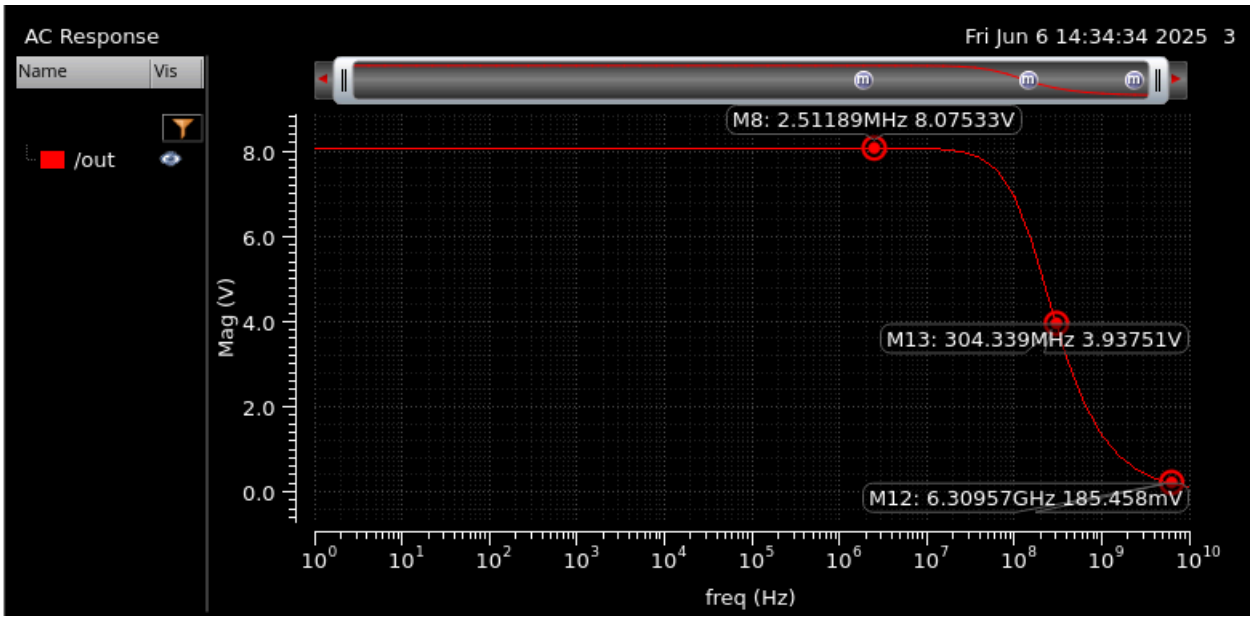

Figure: AC analysis

Transient response and peak to peak Output swing > 1V
Max and Min values marked:

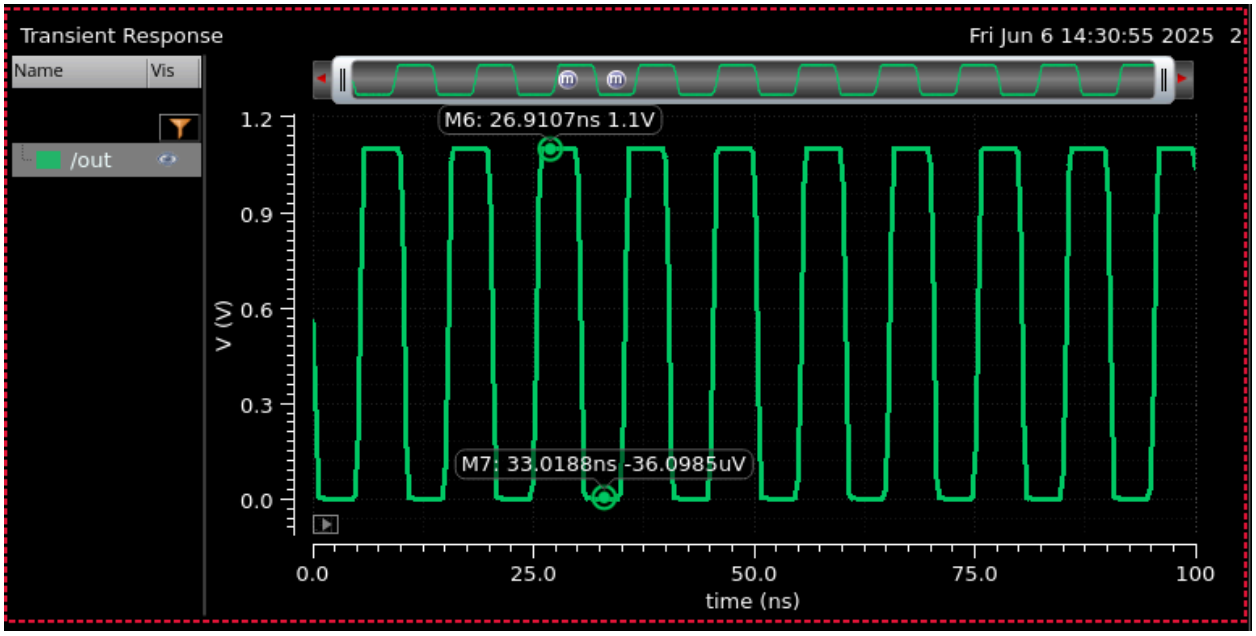

Figure: Output swing for vm = 1.0 V

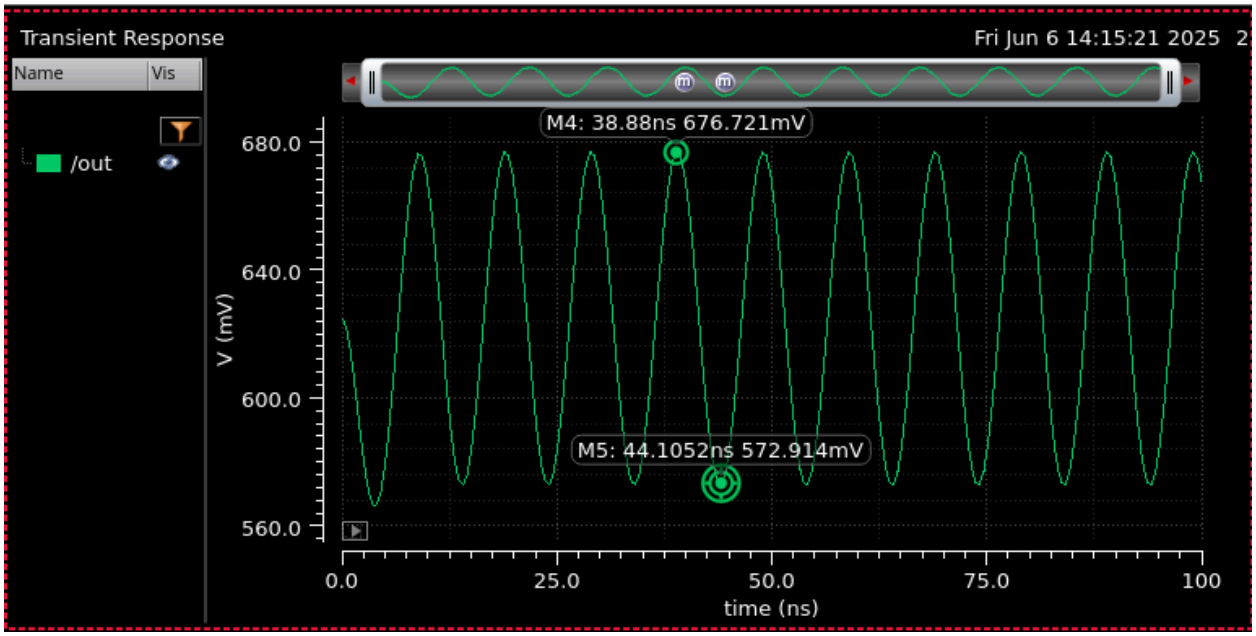

Figure: Output swing for vm = 10 mV

Output swing = 1.1 V - (-36 uV) = 1.100036V (from vm = 1.0 V)

Number of Hours: 10 Hours

3. Findings

The five-transistor OTA was successfully designed and simulated to meet the specified performance criteria. Key observations are summarized below:

- **Voltage Gain**: The amplifier achieved a voltage gain exceeding 15 dB, which confirms sufficient transconductance from the differential pair and output resistance from the current mirrors.

- **3-dB Bandwidth & GBW**: AC analysis showed a 3-dB bandwidth greater than 500 MHz and a gain-bandwidth product above 2.5 GHz, satisfying the high-frequency performance requirements for analog applications.

- **Output Swing**: The transient large-signal simulation demonstrated an output swing greater than 1 V peak-to-peak, indicating the amplifier's ability to handle wide signal ranges. Proper biasing of the PMOS transistors helped avoid clipping at both supply rails.

- **Power Consumption**: With a total bias current of 10 µA and a 1.1 V supply, the amplifier's power consumption remained under 2 mW, complying with the low-power constraint.

- **Matching & Symmetry**: The use of identical sizing and layout symmetry ensured stable performance.

- **DC Operating Point**: All transistors operated in the saturation region, with expected values.

Overall, the design met or exceeded all specified requirements for gain, bandwidth, swing, and power, validating the effectiveness of the sizing and biasing strategy used.

4. References

- EE 332 Final Project Handout, Spring 2025