Mihir Sharma
EE 332
Lab 4:Inverter Layout, Schematic, Verification
05/21/2025

1. Introduction

The objective of this lab was to design, lay out, and verify a CMOS inverter using Cadence Virtuoso and the FreePDK45 process. This lab introduced layout design concepts and verification tools, including Design Rule Check (DRC) and Layout Versus Schematic (LVS)

2. Procedure (Brief Overview)

The inverter circuit was built and verified using Virtuoso and Calibre. The process involved:

- Schematic design using PMOS and NMOS transistors from the FreePDK45 library.
- DC and transient simulation in ADE using Spectre, verifying inverter switching behavior.
- Layout construction with correct layer usage (active, poly, metal, etc.) and design rule compliance.
- DRC to ensure layout adheres to fabrication constraints.
- LVS to verify the layout matches the schematic.

Best practices used include:

- Following FreePDK45 design rules (e.g., minimum poly extension).
- Proper transistor sizing (PMOS: 300nm, NMOS: 150nm) and orientation.
- Use of poly contacts and metal routing to connect gates and drains.
- Addition of n-well and Vth implants for proper transistor threshold type.

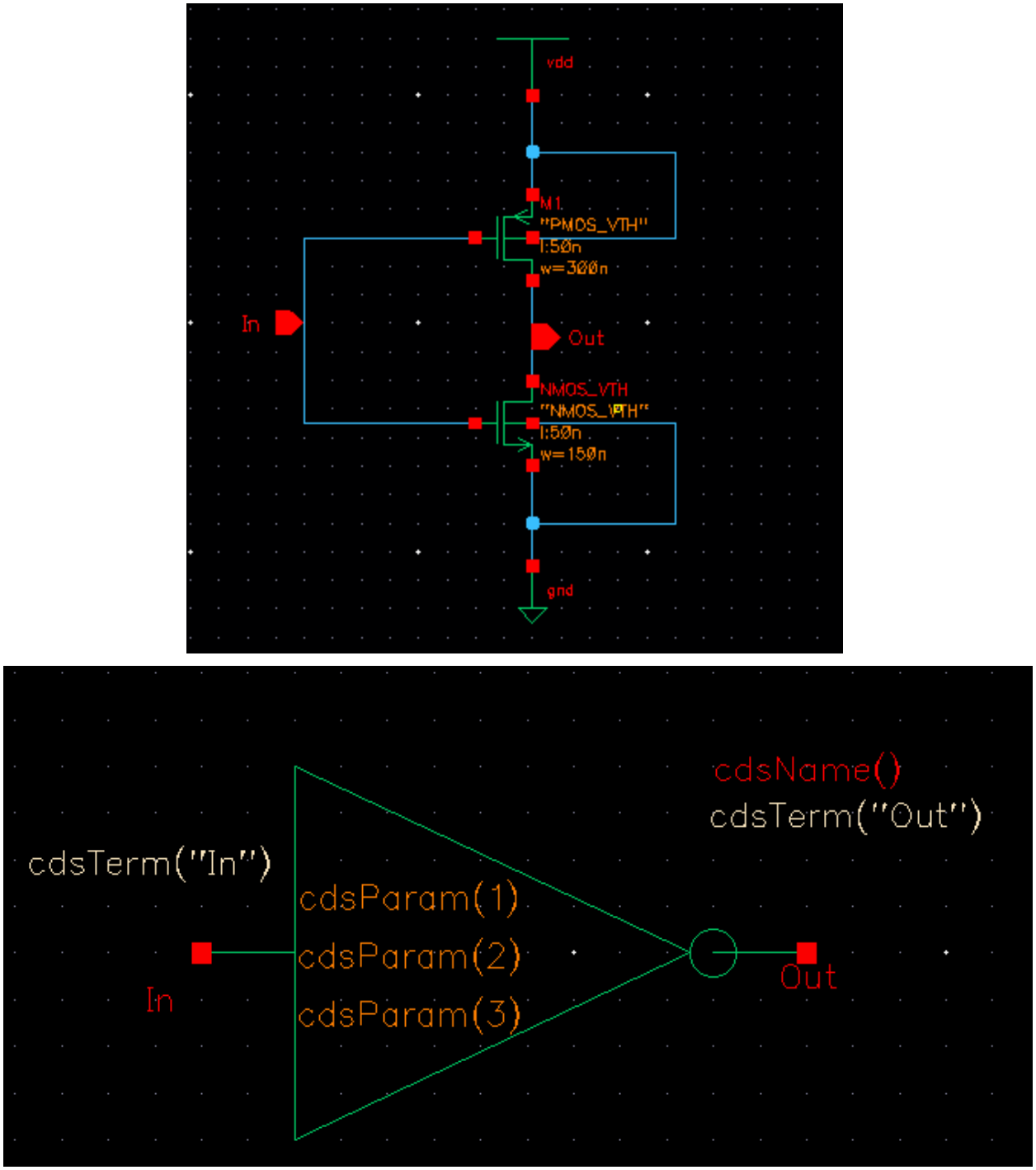
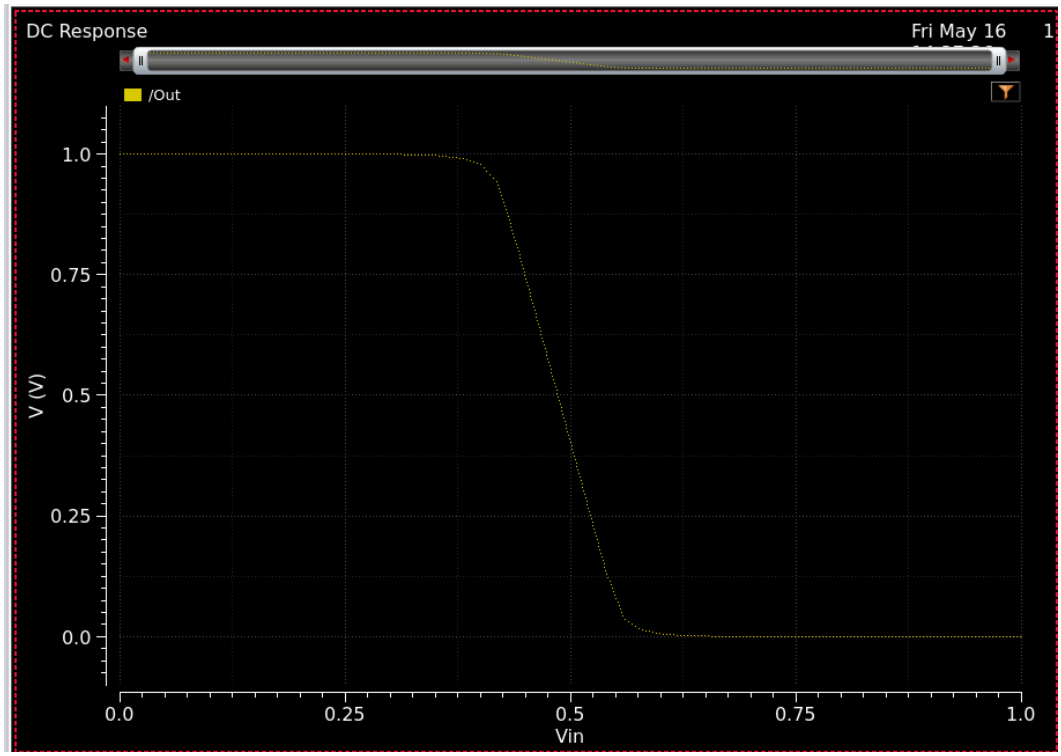


Figure: Schematic view of CMOS inverter



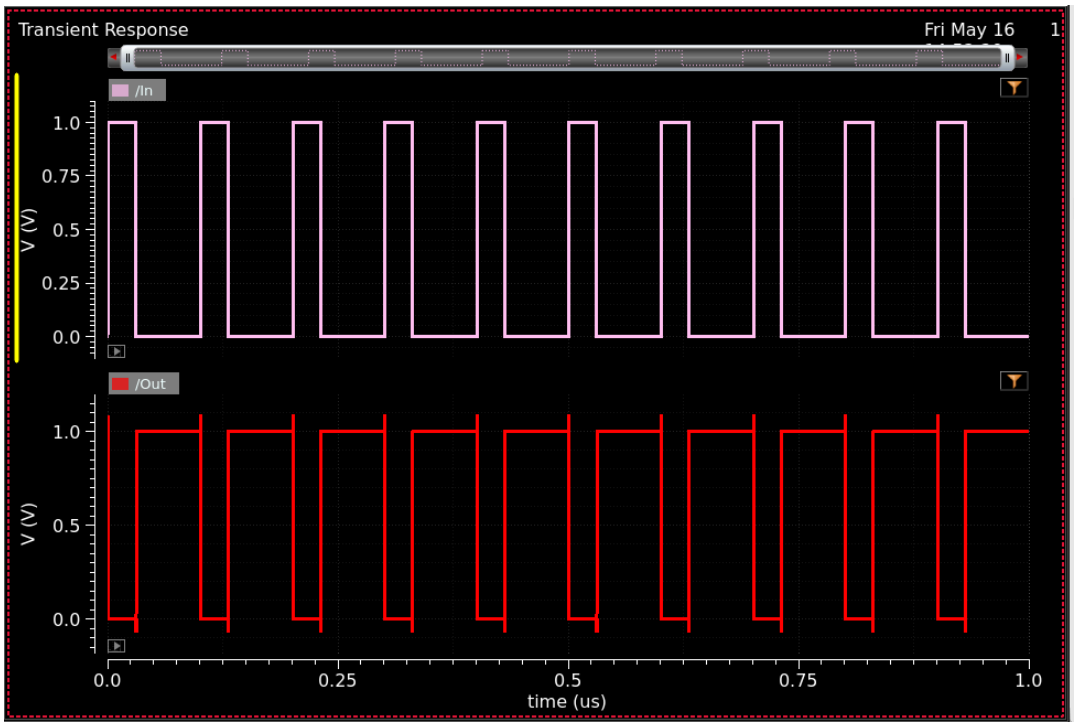


Figure: DC and Transient Simulation Results

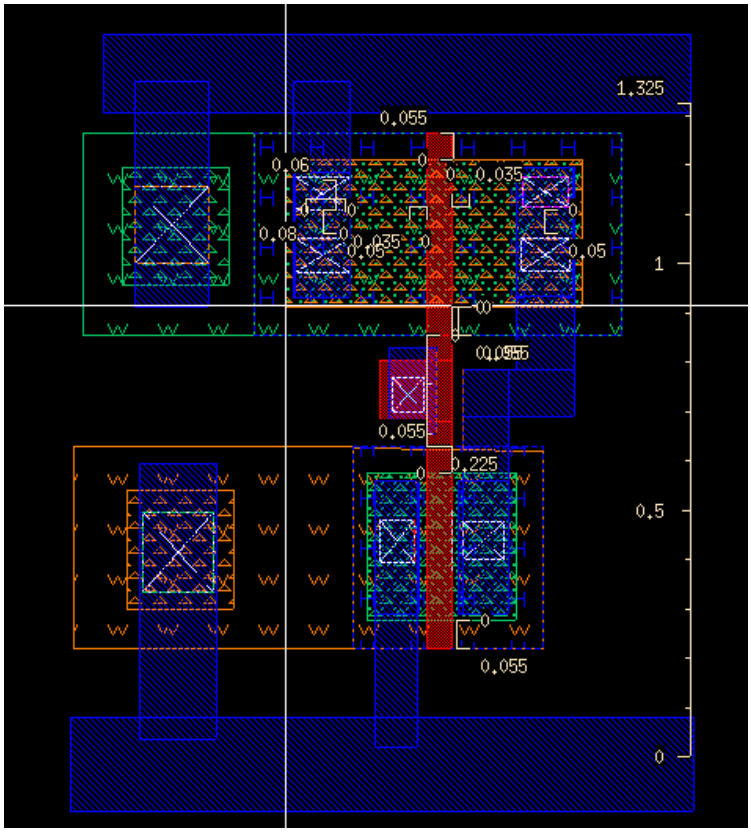


Figure: Final Layout of Inverter

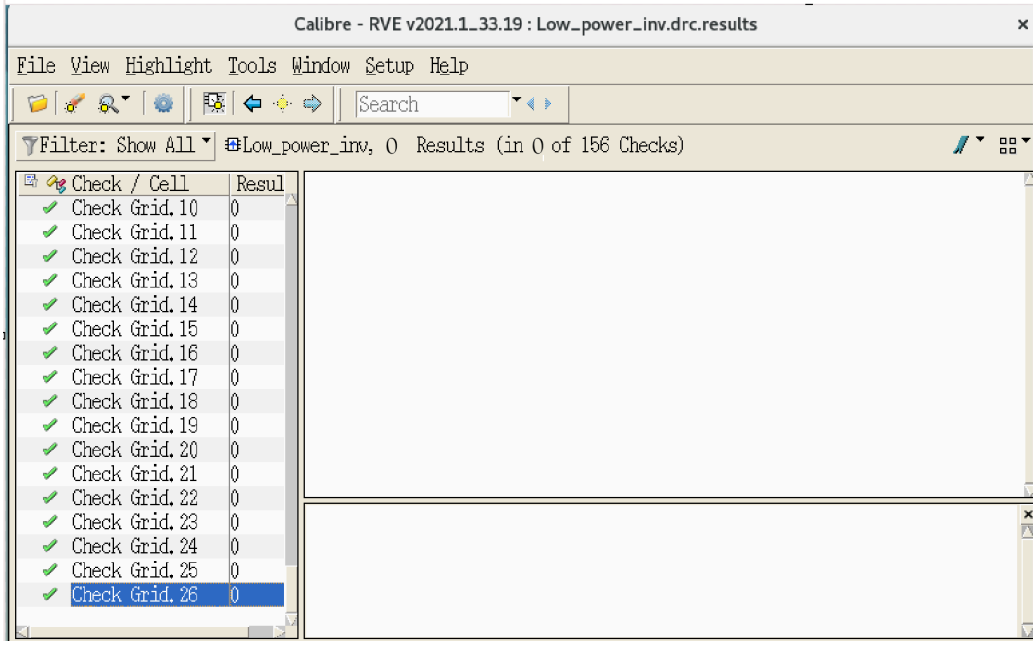


Figure: DRC Results

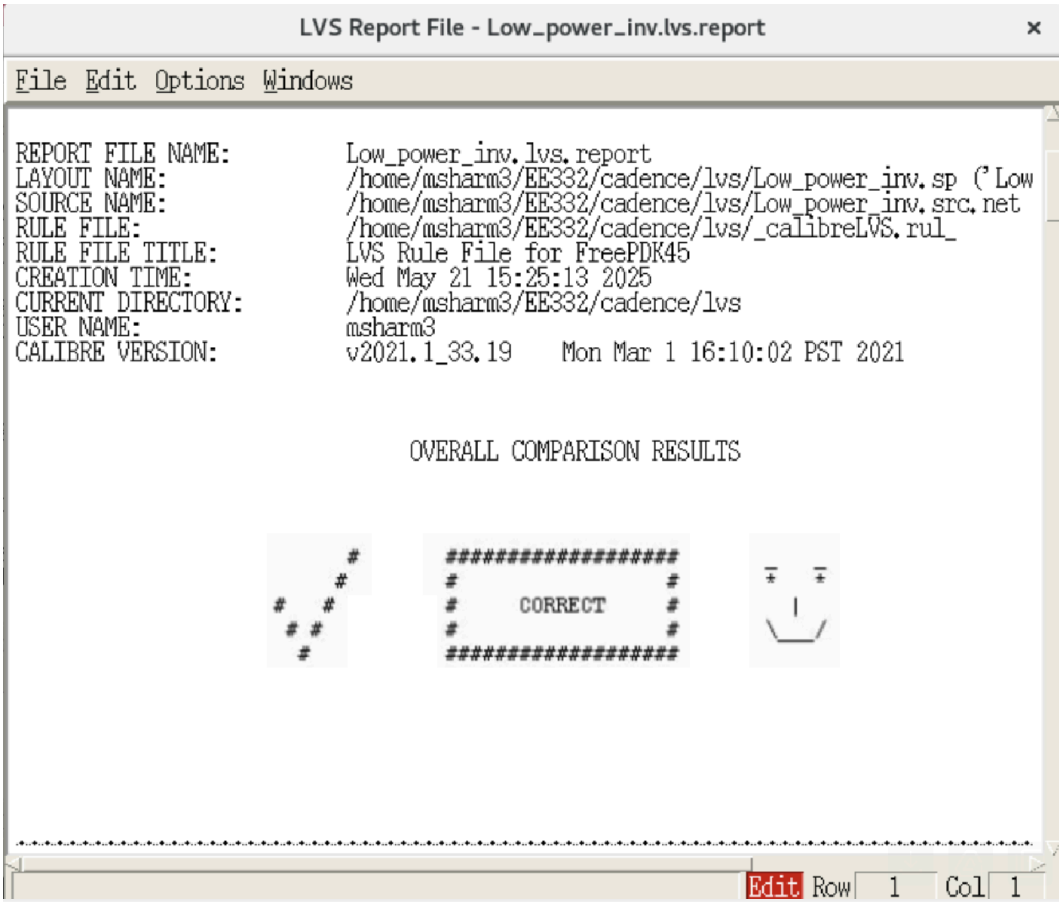


Figure: LVS Results

3. Results and Findings:

The inverter design passed all checks and matched its schematic.

DRC Findings

- Layout passed without any design rule violations after adjusting poly extensions and metal overlaps.
- Design adhered to minimum feature sizes and spacing guidelines per FreePDK45.

LVS Findings

- Schematic-to-layout matching was confirmed using Calibre LVS.

- Adding metal1 labels (In, Out, VDD, GND) were important for proper LVS matching.

Simulation Results

- The DC sweep confirmed proper VTC (voltage transfer characteristics) for the inverter.
- Transient simulation with a pulse input showed clean switching behavior.
- Propagation delays were within expected range.

4. References

- EE 332 Lab 4 Reference Sheet, Spring 2025.
- Cadence Tutorial: ENGN1600, Brown University.