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EE 332
Lab 3: Layout of a Common Source Amplifier
05/11/2025

1. Introduction

The objective of this lab was to design and layout a common-source amplifier using Cadence Virtuoso. This task builds on our schematic design from Lab 2 and introduces key layout practices to mitigate device mismatch in analog circuits.

2. Procedure (Brief Overview)

Using the results and values from Lab 2, the amplifier was laid out in Virtuoso. Several best practices were followed to reduce mismatch:

- **Identical device orientation** for symmetry.
- **Common-centroid layout** techniques for critical transistor pairs.
- **Dummy structures** were included at the edges to ensure uniform etching.
- **Multiple device sizing** to match current mirrors and differential pairs.

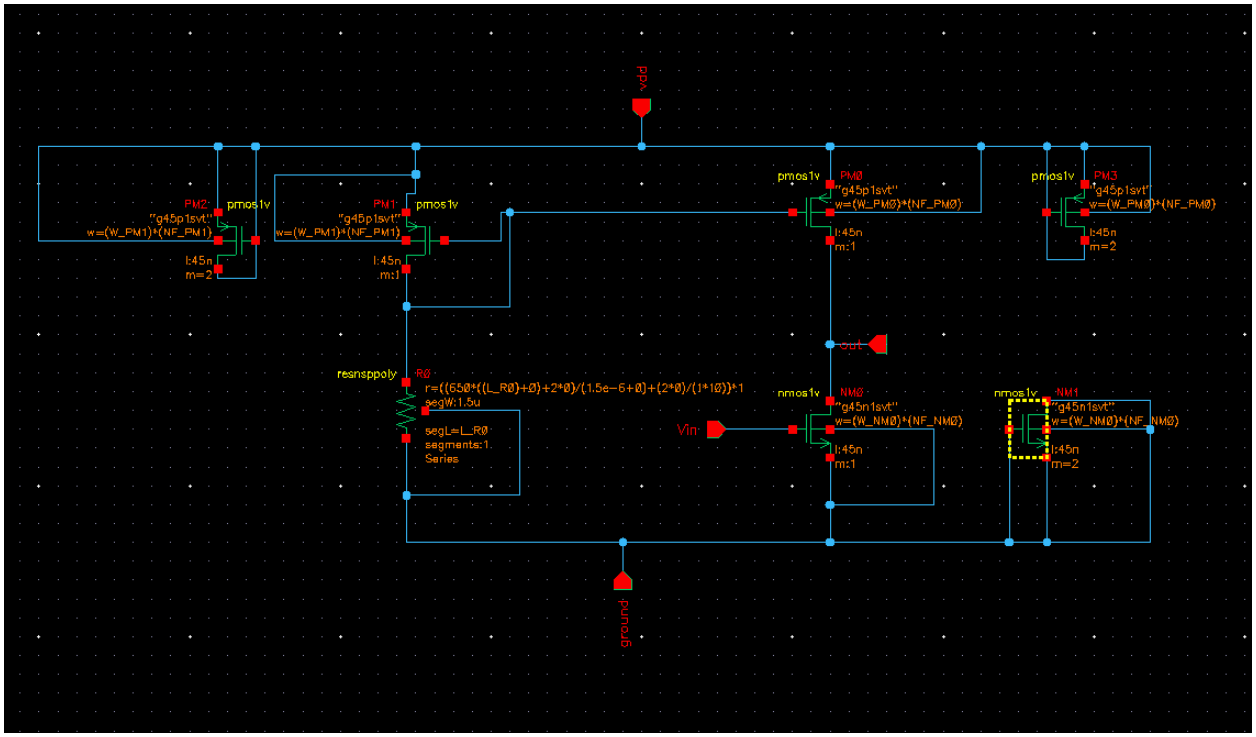
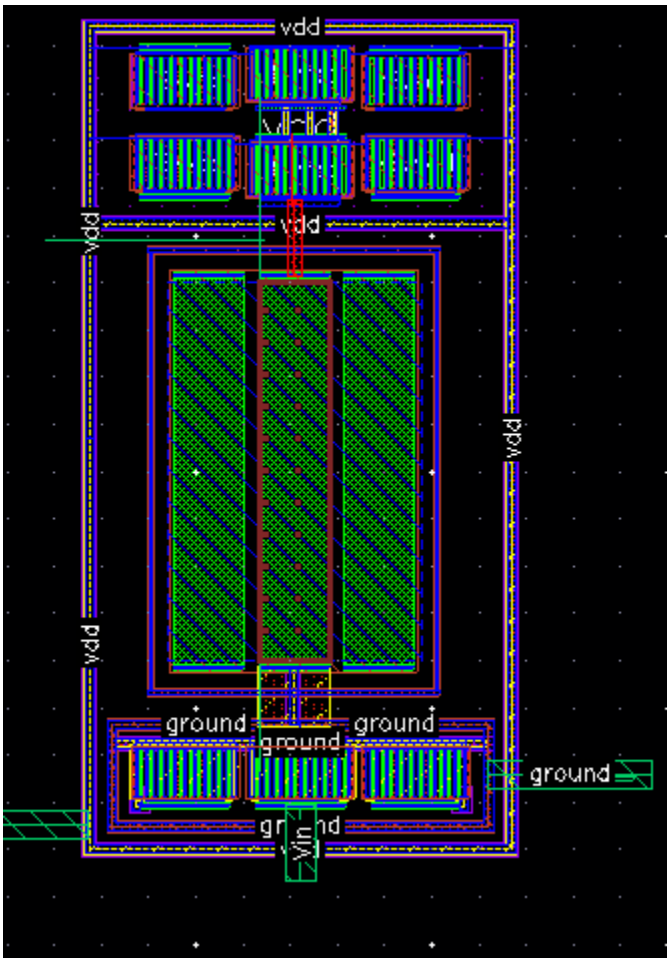
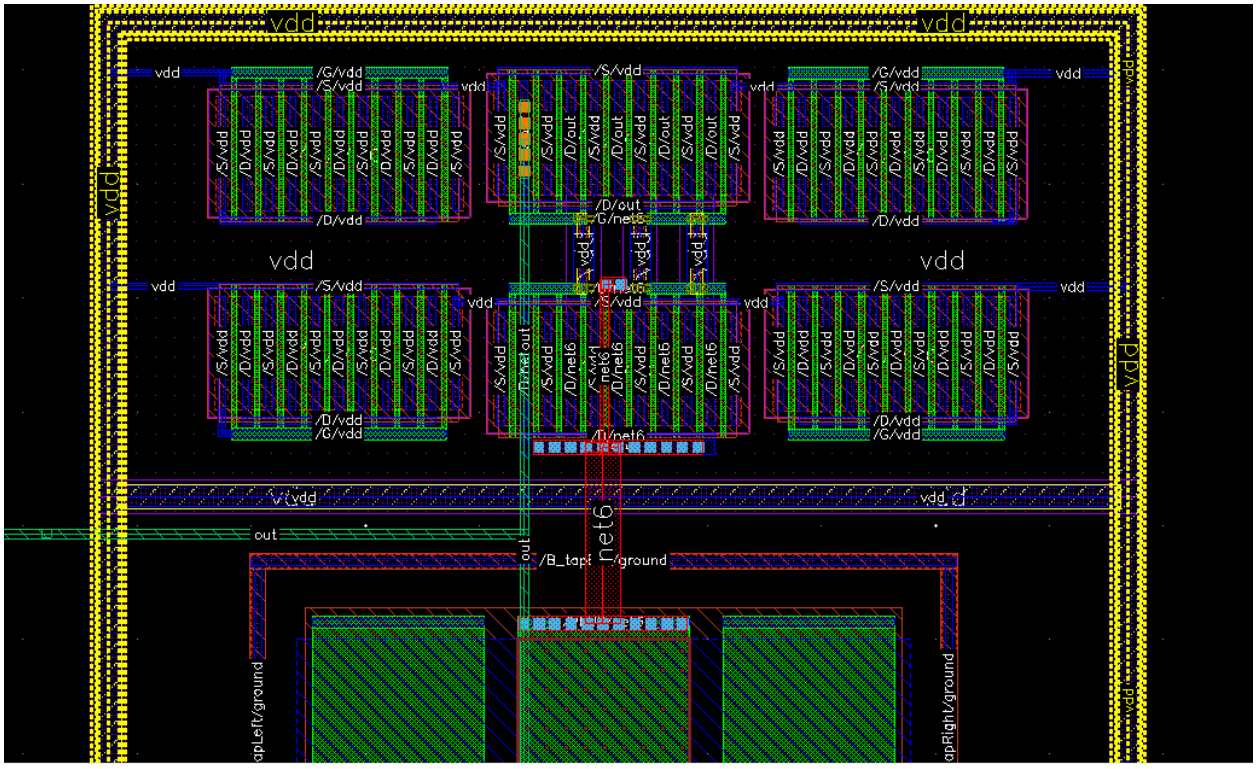
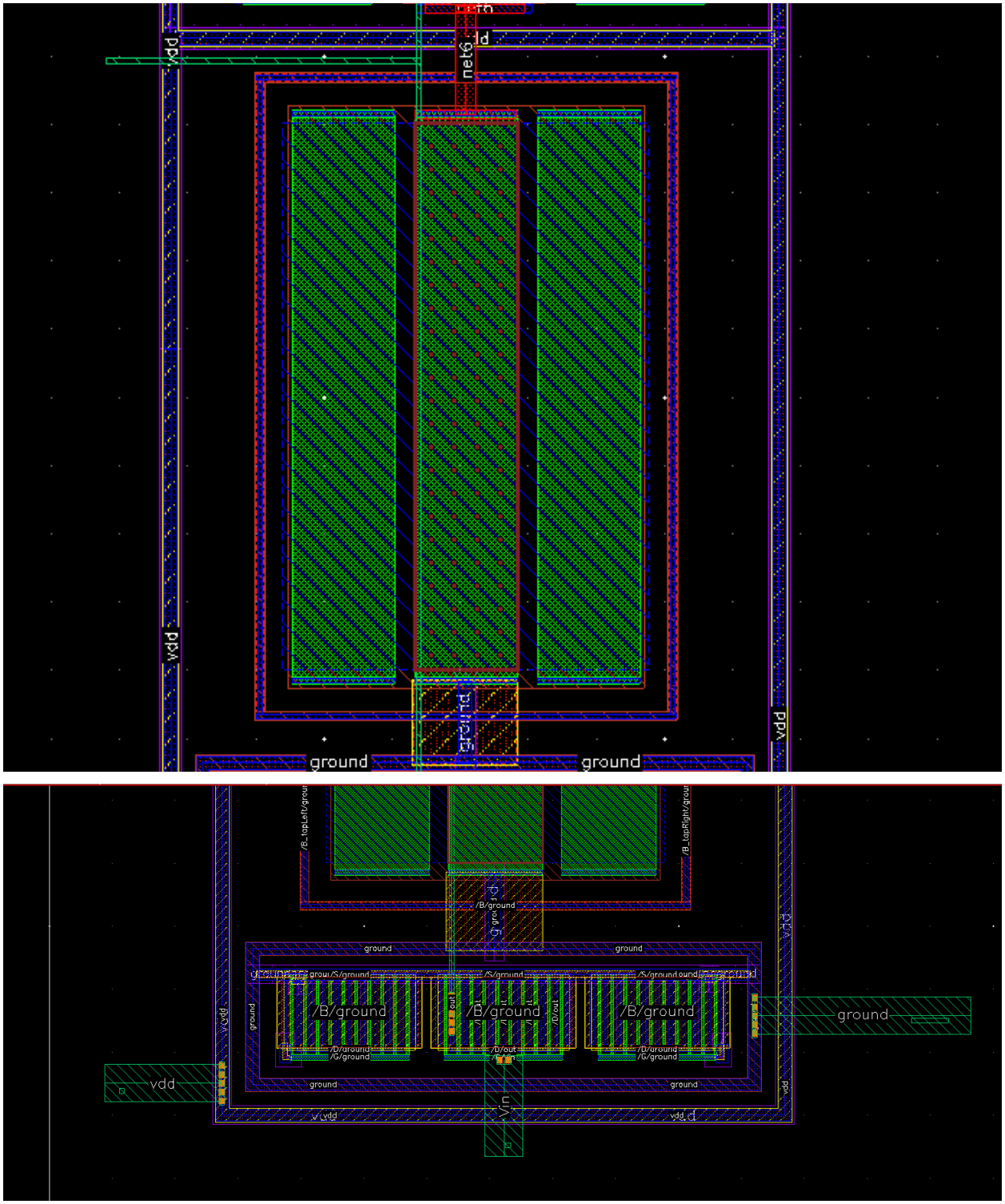


Figure: Circuit layout for the common source amplifier




vdd
/G/vdd
/S/vdd
/D/vdd
/D/out
/G/net5
/S/net6
/D/net6
/G/net6
out
/B_tap
/ground
tapLeft/ground
tapRight/ground
net6



Figures: Layout for amplifier

3. Results and Findings

The amplifier was laid out with symmetry and matching considerations. The Common-centroid layout and dummy structures notably helped improve matching and avoid edge-related etching issues.

The layout includes several design techniques known to reduce mismatch-related performance degradation:

- Identical orientation of transistors ensures uniform current flow and consistent threshold behavior.
- Common-centroid layout was used for matched pairs to symmetrically distribute process gradients.
- Dummy devices were added at the edges of active devices to maintain uniform etching and diffusion.
- Symmetrical routing of VDD, GND, and signal lines to minimize systematic mismatch from interconnect parasitics.
- Minimized Device Spacing: Keeping matched transistors close together reduces gradient mismatches due to temperature or process variations.
- Ensuring both devices have identical source/drain contact structures
- Encapsulating devices in shared guard rings and well ties ensures both devices experience the same substrate noise and bulk biasing.
- Every transistor used in matching groups has equal W/L, contact shape, and routing load.

These strategies help ensure better analog performance, particularly in gain and bias stability.

4. References

- Lab 3 Reference Sheet, EE 332 Canvas, Spring 2025.