EE618 Project

Prashant Kurrey 17d070057
Mihir Kavishwar 17d070004

December 5, 2020

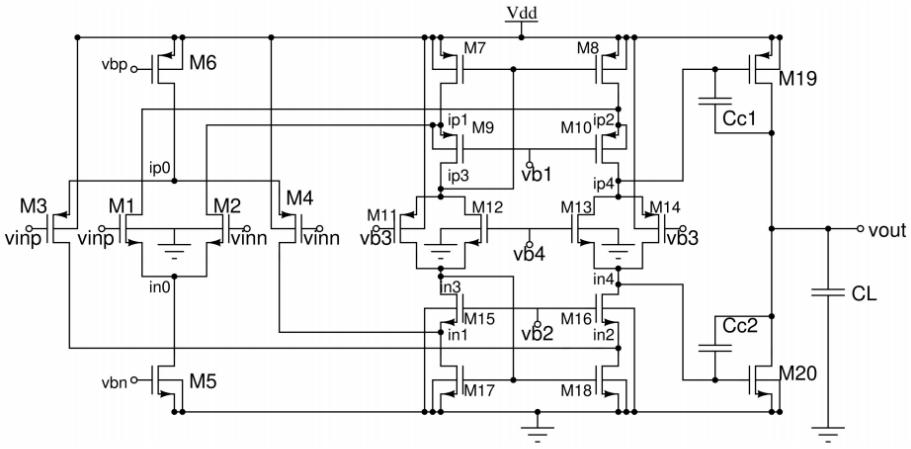


Figure 1: Two stage rail-to-rail folded cascode Op-amp with Class AB output stage

Target Specifications:

- Single ended output
- Open loop small signal low-frequency voltage gain $>$ 100 dB
- Unity gain bandwidth $>$ 10 MHz
- Input CM voltage range: 100 mV to 1.7 V
- Output voltage range: 100 mV to 1.7 V
- Phase margin $> 60^{o}$ (Load capacitance = 5 pF)
- Slew rate $>$ 2 V/µs (Load capacitance = 5 pF)

1 Op-Amp Design Flow

1.1

The PTM 180nm CMOS technology parameters are as follows:

- For $L = 1\mu\ m$,
  $\lambda_p = 0.1V^{-1}$ and $\lambda_n = 0.05V^{-1}$
- For $t_{ox} = 4nm$,
  $C_{ox} = 8.78\ fF/\mu m^2$, $\mu_n C_{ox} = 300\ \mu A/V^2$, $\mu_p C_{ox} = 68\ \mu A/V^2$
- $|V_{tp}| \approx 0.4\ V$ and $V_{tn} \approx 0.4\ V$

1.1.1 Bias Current

We know that for the given OpAmp architecture,

$$slew\ rate \approx \frac{I_{bias}}{C_c}$$

For slew rate $> 2\ V/\mu s$, we need

$$\frac{I_{bias}}{C_c} > 2\ V/\mu s$$

For $C_c = 4\ pF$,

$$I_{bias} > 2 \times 4 \times 10^{-12+6} = 8\ \mu A$$

A higher bias current results in reduced output resistance for transistors (since $r_o = \frac{1}{\lambda I_{ds}}$) as well as higher power consumption. Therefore if possible, it's always better to have low bias current. The drawback of using very small bias current is that to get the same trans-conductance we need larger aspect ratio (since $g_m = \frac{2I_{ds}}{V_{gst}}$).

For first iteration we are assuming

$$I_{bias} = 50\ \mu A$$

Therefore for nominal voltage of 0.9 V,

$$I_{d_1} = I_{d_2} = I_{d_3} = I_{d_4} = 25\ \mu A$$

$I_{d_{17}} = I_{d_{18}} = I_{d_7} = I_{d_8} \geq I_{bias}$
In our design we are assuming them to be equal.

Also the slew rate puts a constraint on I_{d20}:

$$I_{d20} = I_{bias}(1 + \frac{C_L}{C_c}$$

For $C_L = 5\ pF$ and $C_c = 4\ pF$,

$$I_{d20} \geq 112\mu A$$

We assumed $I_{d20} = 120\mu A$

1.1.2 Overdrive Voltage

When $V_{cm} = V_{in,min} = 0.1\ V$,
M_3, M_4, M_{17}, M_{18} have to be in saturation, therefore,

$$|0.1 + 0.4| \geq V_{ds,17,18} \geq V_{gst,17,18}$$

and $V_{in,max} = 1.7\ V$ M1 and M2 as well as M7 and M8 have to be in saturation.

$$|1.8 - 1.7 + 0.4| \geq V_{ds,7,8} \geq V_{gst,7,8}$$

$$\implies V_{gst,7,8,17,18} \leq 0.5\ V$$

We are assuming $V_{gst,1,2,3,4} = 0.1\ V$ and $V_{gst,7,8} = 0.3\ V$ and $V_{gst,17,18,5,6} = 0.2\ V$ We are also assuming $V_{gst,9,10,11,14,19} = 0.3\ V$ and $V_{gst,12,13,15,16,20} = 0.2\ V$

1.1.3 Trans-conductance

We know, $g_m = \frac{2I_{ds}}{V_{gst}}$. For the above assumed bias currents and overdrive voltages we have,

$$\begin{aligned} g_{m_1} = g_{m_2} = g_{m_3} = g_{m_4} &= 0.5\ mS \\ g_{m_7} = g_{m_8} &= 0.34\ mS \\ g_{m_9} = g_{m_{10}} &= 0.17\ mS \\ g_{m_{11}} = g_{m_{14}} &= 0.085\ mS \\ g_{m_{12}} = g_{m_{13}} &= 0.125\ mS \\ g_{m_{15}} = g_{m_{16}} &= 0.25\ mS \\ g_{m_{17}} = g_{m_{18}} &= 0.5\ mS \\ g_{m_{19}} = 0.8\ mS g_{m_{19}} = g_{m_{20}} &= 1.2\ mS \end{aligned}$$

1.1.4 Gain Calculation

Stage 1 small signal AC gain,

$$A_{v_1} \approx -g_{m_{1,2}} \times (g_{m_{10}} r_{o_{10}} (r_{o_2} || r_{o_7}) || (g_{m_{16}} r_{o_{16}} r_{o_{18}}))$$

Stage 2 small signal Ac gain,

$$A_{v_2} \approx -(g_{m_{19}} + g_{m_{20}})(r_{o_19} || r_{o_20})$$

OpAmp gain,

$$A_{v_0} \approx A_{v_1} A_{v_2}$$

Assuming the length of the transistor is 1 μm

$$
\begin{aligned}
r_{o_1} = r_{o_2} &= 800\ k\Omega \\
r_{o_3} = r_{o_4} &= 400\ k\Omega \\
r_{o_7} = r_{o_8} &= 200\ k\Omega \\
r_{o_9} = r_{o_10} &= 400\ k\Omega \\
r_{o_11} = r_{o_14} &= 800\ k\Omega \\
r_{o_12} = r_{o_13} &= 1600\ k\Omega \\
r_{o_15} = r_{o_16} &= 800\ k\Omega \\
r_{o_17} = r_{o_18} &= 400\ k\Omega \\
r_{o_19} &= 167\ k\Omega \\
r_{o_20} &= 84\ k\Omega
\end{aligned}
$$

Substituting these values in the gain equation we get

$$
\begin{aligned}
A_{v_1} &\approx 4440 \\
A_{v_2} &\approx 110 \\
\implies A_{v_0} &\approx 4.88 \times 10^5 \approx 113dB
\end{aligned}
$$

1.1.5 $\frac{W}{L}$ calculation

$$
\begin{aligned}
\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 &\approx 16 \\
\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 &\approx 74 \\
\left(\frac{W}{L}\right)_7 = \left(\frac{W}{L}\right)_8 &\approx 16 \\
\left(\frac{W}{L}\right)_9 = \left(\frac{W}{L}\right)_{10} &\approx 8 \\
\left(\frac{W}{L}\right)_{11} = \left(\frac{W}{L}\right)_{14} &\approx 4 \\
\left(\frac{W}{L}\right)_{12} = \left(\frac{W}{L}\right)_{13} &\approx 2 \\
\left(\frac{W}{L}\right)_{15} = \left(\frac{W}{L}\right)_{16} &\approx 4 \\
\left(\frac{W}{L}\right)_{17} = \left(\frac{W}{L}\right)_{18} &\approx 8
\end{aligned}
$$

$$\left(\frac{W}{L}\right)_{19} \approx 40$$

$$\left(\frac{W}{L}\right)_{20} \approx 20$$

$$\left(\frac{W}{L}\right)_{5} \approx 8$$

$$\left(\frac{W}{L}\right)_{6} \approx 36$$

1.1.6 Bias Voltage

$$V_{b2} \geq V_{gst15} + V_{th15} + \delta V_{th15} + V_{gst17} = 0.2 + 0.4 + 0.2 + 0.2 = 1\ V$$

$$V_{b1} \leq VDD - V_{gst9} - V_{th9} - V_{gst7} = 1.8 - 0.3 - 0.4 - 0.3 = 0.8\ V$$

$$V_{b4} \geq V_{gst12} + V_{th12} + \delta V_{th12} + V_{gs17} = 0.2 + 0.4 + 0.2 + 0.6 = 1.4\ V$$

$$V_{b3} \leq VDD - V_{gst11} - V_{th11} - \delta V_{th11} - V_{gs7} = 1.8 - 0.3 - 0.4 - 0.1 - 0.7 = 0.3\ V$$

1.1.7 Unity Gain Bandwidth and Phase Margin

$$f_u = \frac{g_{m,1,2}}{2\pi C_c}$$

For the C_c value of 4pF and $g_{m,1,2}$ of 0.5mS

$$f_u \approx 19.8MHz \geq 10MHz$$

For the phase margin calculation

$$f_{p2} \approx \frac{g_{m,19,20}}{2\pi C_L} = 38.19MHz$$

$$f_{z1} \approx \frac{g_{m,19,20}}{2\pi C_c} = 47.74MHz$$

$$f_{p1} \approx \frac{1}{g_{m,19,20} R_1 R_2 C_c} = 516Hz$$

$$PM = 180 - \arctan(\frac{f_u}{f_{p1}}) - \arctan(\frac{f_u}{f_{p2}}) - \arctan(\frac{f_u}{f_{z1}})$$

$$PM = 180 - 90 - 27.4 - 22.5 = 35\,\text{deg}$$

1.2

As from the previous section using the W/L value, for the first time we may not get the gain greater than the 100dB because some of the mosfet mag go in linear region or weak inversion region because there is body bias effect due to that we will have less gain. So to put all the transistor in strong inversion region the bias voltage should be adjusted or the W/L ration. Also from the above frequency calculation we know that there will be zero at the RHP which will degrade the phase margin. So to get the phase margin we need to add resistor Rz in series with the Cc such that the RHP pole shift to LHP. To overlap with 1st non dominant pole value of resistance Rz can be obtained using the below equation.

$$R_z = \frac{C_L + C_c}{g_{m,19,20} C_c}$$

Using the value from the above section value of Rz is coming as 1875ω.So we have used $2K\omega$ for the vlaue of Rz which will give LHP fz as

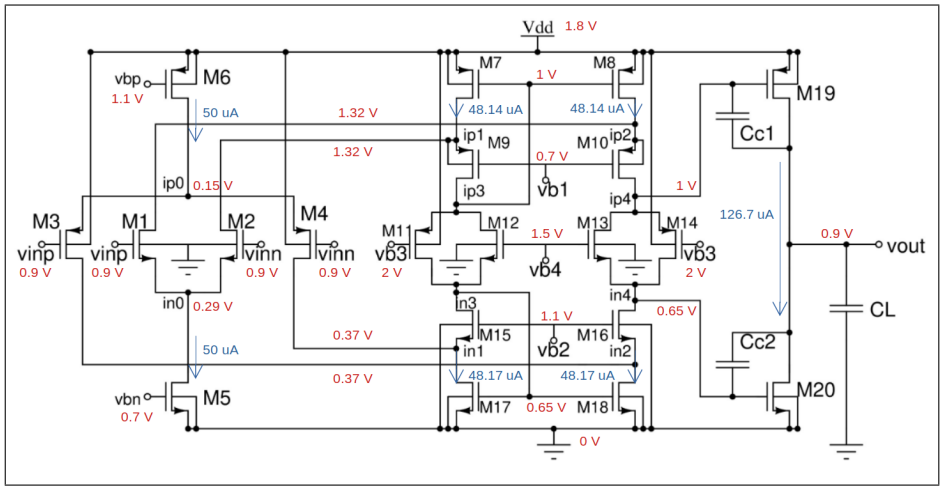
$$f_z = \frac{1}{2\pi(R_z - (g_{m,19,20})^{-}1)C_c} = 34MHz$$

This will give Phase margin as:

$$PM = 180 - \arctan(\frac{f_u}{f_{p1}}) - \arctan(\frac{f_u}{f_{p2}}) + \arctan(\frac{f_u}{f_{z1}})$$

$$PM = 180 - 90 - 27.4 + 30.2 = 92.8\,\text{deg} \geq 60\,\text{deg}$$

1.3



1.4

Transistor	Width (μm)	Length (μm)	Aspect Ratio ($\frac{W}{L}$)
M_1	16	1	16
M_2	16	1	16
M_3	74	1	74
M_4	74	1	74
M_5	4	0.5	8
M_6	18	0.5	36
M_7	16	1	16
M_8	16	1	16
M_9	32	1	32
M_{10}	32	1	32
M_{11}	4	0.5	8
M_{12}	2	0.5	4
M_{13}	2	0.5	4
M_{14}	4	0.5	8
M_{15}	4	0.5	8
M_{16}	4	0.5	8
M_{17}	8	1	8
M_{18}	8	1	8
M_{19}	40	1	40
M_{20}	20	1	20

Table 1: Transistor Sizes

2 Reference Generator Circuit Design

2.1 Schematic

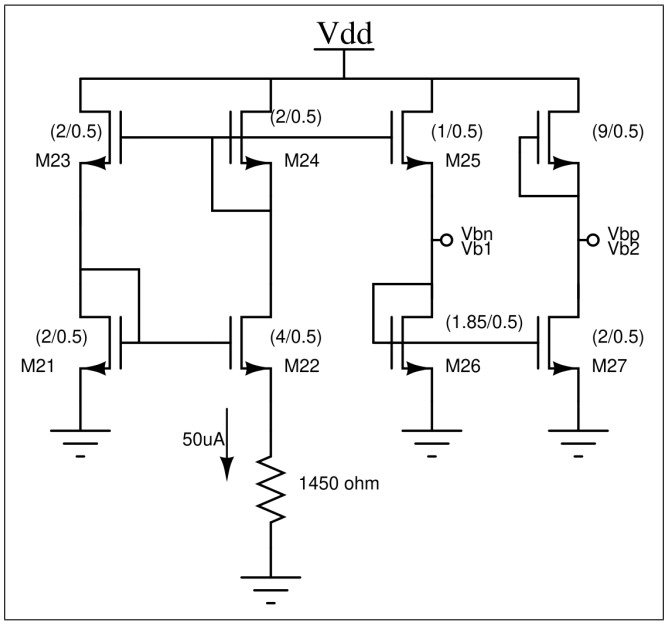


Figure 1: Current reference generator and biasing voltage

2.2 Design Procedure

From the above figure we can see that Vg of M21 and M22 is same and the current in both the branch will be same because of the PMOS current mirror:

$$V_{gs21} = V_{gs22} + Iref * R$$

$$Iref * R = \sqrt{\frac{2 * Iref}{\mu C_{ox}(W/L)_{21}}} - \sqrt{\frac{2 * Iref}{\mu C_{ox} K (W/L)_{21}}}$$

$$Iref = \frac{2}{\mu C_{ox}(W/L)_{21} R^2}(1 - \frac{1}{\sqrt{K}})^2$$

Taking the value $(W/L)_{21} = 2/0.5 and K = 2$ and $R_s = 1450Ohm$ Iref will be 40uA but in the simulation Iref is 50uA and this is because we have neglected channel length modulation. To generate the Vbn we mirror the current through PMOS and pass it through the diode connected NMOS to generate the Vbn and Vb1. Similarly the we mirror the current through NMOS and pass it through the diode connected PMOS to generate the Vbp and Vb2. Vb3 and Vb4 is generated using Resistor divider.

2.3 Transistor Sizes

Transistor	Width (μm)	Length (μm)	Aspect Ratio ($\frac{W}{L}$)
M_{21}	2	0.5	4
M_{22}	4	0.5	8
M_{23}	2	0.5	4
M_{24}	2	0.5	4
M_{25}	1	0.5	2
M_{26}	1.85	0.5	3.7
M_{27}	2	0.5	4

Table 2: Transistor Sizes

3 DC Simulations

3.1 Schematic

Below is the schematic used to run the dc simulation at common input voltage.

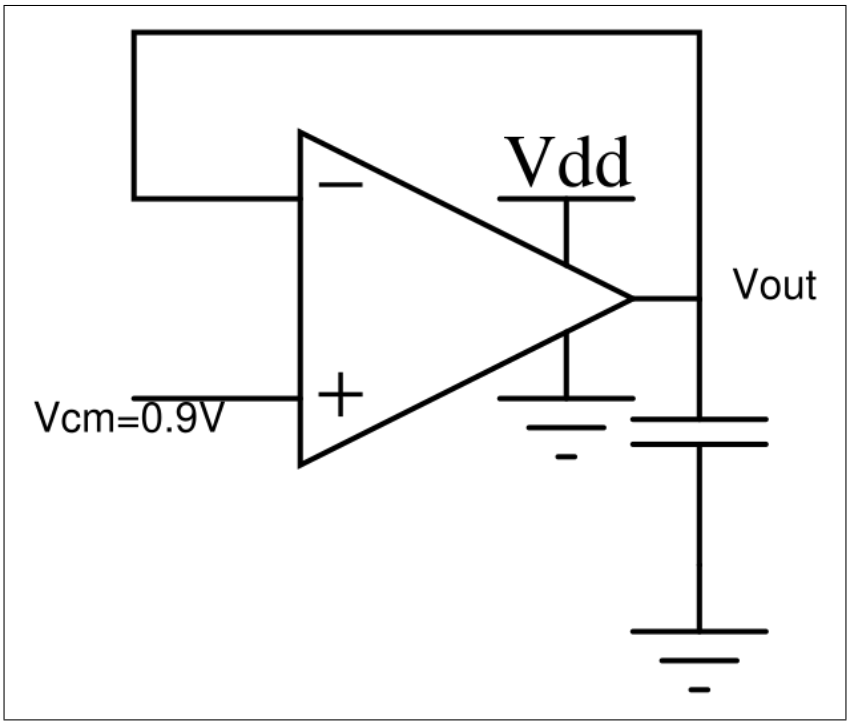


Figure 2: Unity gain schematic

3.2 DC operating Point

We ran the DC simulation by connecting the OpAmp as shown in above figure.

Transistor	I_d (μA)	V_{gs} (V)	V_{th} (V)	V_{ds} (V)	g_m (mS)
M_1	25	0.61	0.53	1.03	0.36
M_2	25	0.61	0.53	1.03	0.36
M_3	25.02	0.63	0.52	1.16	0.41
M_4	25.02	0.63	0.52	1.16	0.41
M_5	50	0.7	0.5	0.29	0.39
M_6	50.05	0.7	0.47	0.27	0.42
M_7	48.14	0.8	0.45	0.48	0.25
M_8	48.14	0.8	0.45	0.48	0.25
M_9	23.14	0.62	0.45	0.32	0.27
M_{10}	23.14	0.62	0.45	0.32	0.27
M_{11}	4	0.8	0.67	0.35	0.06
M_{12}	19.14	0.85	0.67	0.35	0.16
M_{13}	19.15	0.85	0.67	0.35	0.16
M_{14}	4	0.8	0.67	0.35	0.06
M_{15}	23.14	0.73	0.6	0.28	0.02
M_{16}	23.14	0.73	0.6	0.28	0.02
M_{17}	48.17	0.65	0.45	0.37	0.39
M_{18}	48.17	0.65	0.45	0.37	0.39
M_{19}	126.7	0.8	0.45	0.9	0.66
M_{20}	126.7	0.8	0.45	0.9	0.66

Table 3: DC Operating Points

3.3 Node Voltage

Below is the table which shows the node voltage and the current values are given in the above section.

Node	Voltage (V)	Node	Voltage (V)
vinp	0.9	vinn	0.9
ip0	1.53	in0	0.29
ip1	1.32	in1	0.37
ip2	1.32	in2	0.37
ip3	1	in3	0.65
ip4	0.65	in4	1
vb1	0.7	vb2	1.1
vb3	2	vb4	1.5
vbp	1.1	vbn	0.7

Table 4: Node Voltages

4 AC Simulations

4.1 Gain plot

Below is the gain and phase plot which shows that the low frequency gain is greater than the 100dB and also the unity gain frequency is greater than 10MHz.

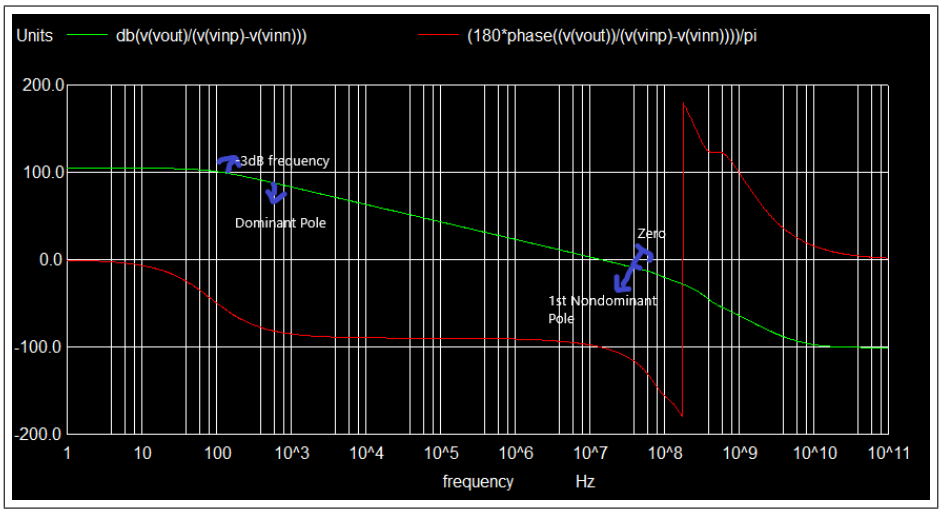


Figure 3: Gain and Phase plot

4.2 Pole and Zero location

Below is the table for which shows the simulated and calculated dominant pole, first non dominant pole and zero. From the section of first question we used the calculated value. Form the table we can observe that the calculated value is approximately same as that of simulated value.

Pole/Zero	Calculated	Simulated
Dominant Pole	516 Hz	535 Hz
First Non dominant pole	38.19 MHz	40.48 MHz
Zero	34 MHz	41.98 MHz

Table 5: Pole and Zero location

4.3 Phase plot and Phase Margin

Below is the gain and phase plot which shows the Phase margin is 80 degree which is greater than 60 degree.

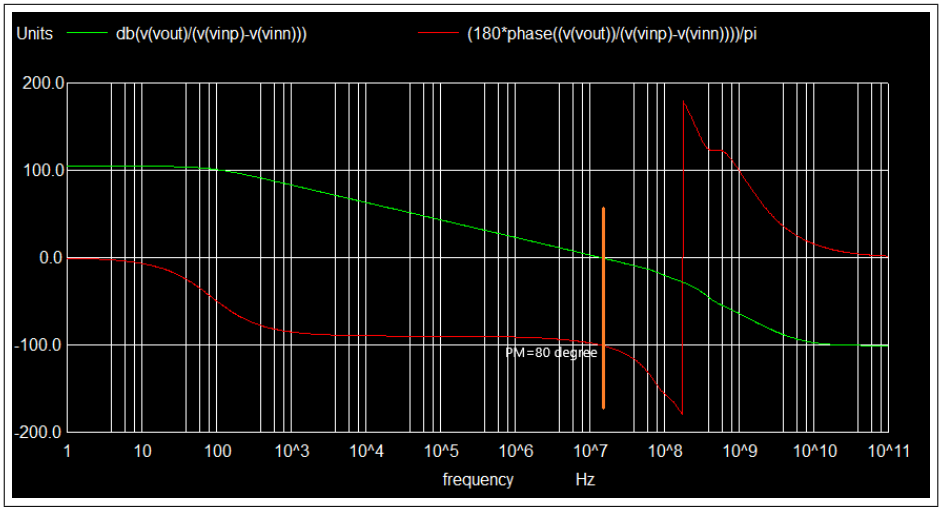


Figure 4: Phase margin

4.4 Roll off

Unity gain frequency, $f_u = 14.7\ MHz$
From the bode plot we can see that roll off at 1 octave above unity gain frequency ($f_u \times 8 = 117.6\ MHz$) = **-45 dB per decade**

5 Slew rate Simulation

5.1 Schematic

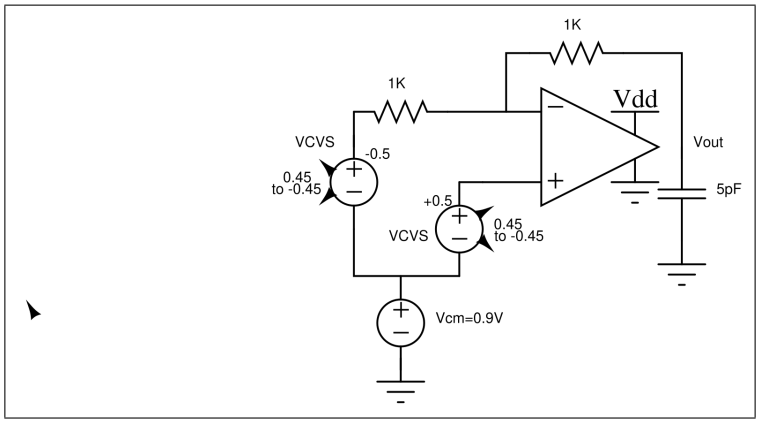


Figure 5: Unity gain for output swing

5.2 Slew Rate

Below is the plot which shows the output and input waveform during the positive slewing and negative slewing.

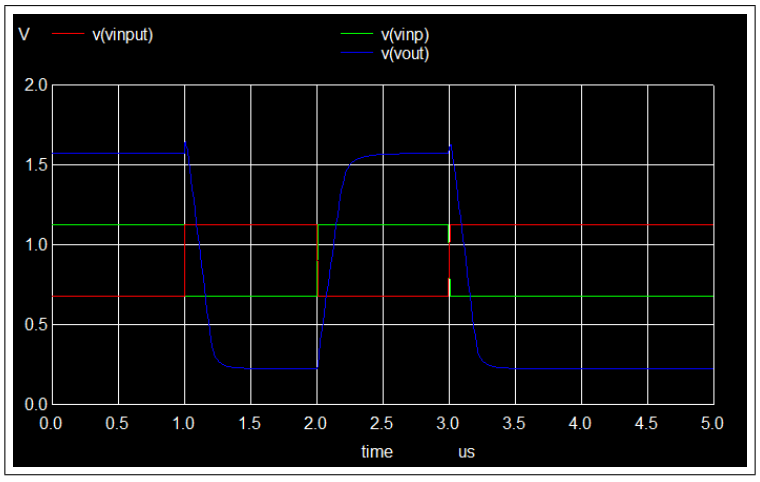


Figure 6: Gain of -1 for slew rate

Below graph is the plot of derivative of the output voltage. from the figure we can observe that the maximum rate is

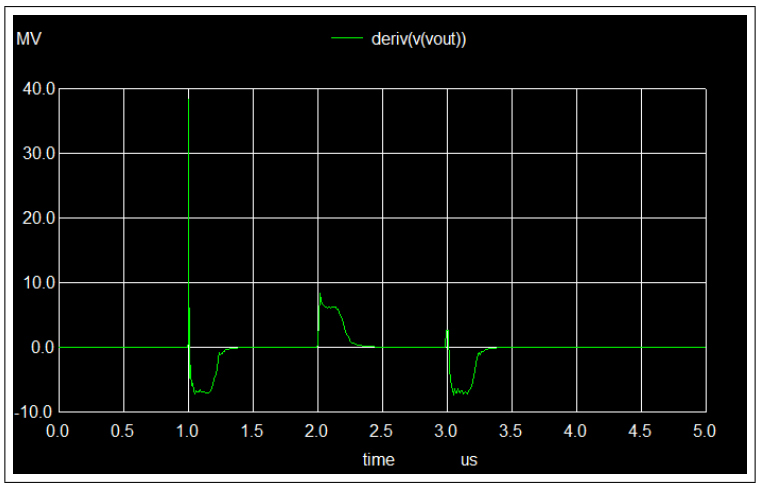


Figure 7: Positive slew rate and negative slew rate

The positive slew rate is 6.3 $V/\mu s$
The negative slew rate is 6.72 $V/\mu s$
The positive and negative slew rate is greater than the 2 $V/\mu s$.

6 Transient Simulation

6.1 Schematic

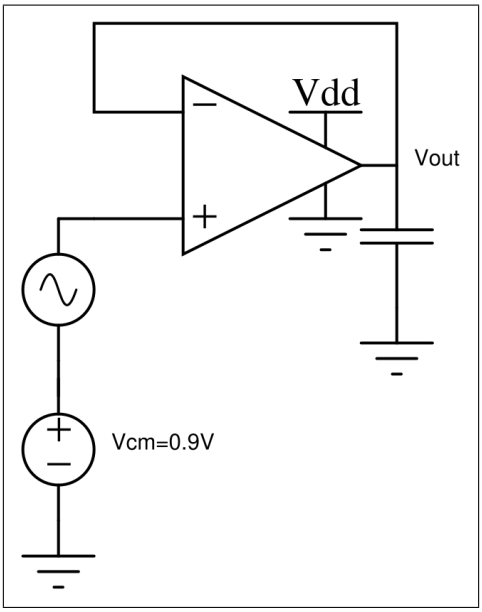


Figure 8: Unity gain for output swing

6.2 Output Swing

Below is the waveform of the output and input voltage connected in unity gain. From the graph we can observe that the for the input voltage swing of 0 to 1.8V, the output voltage swing is 0 to 1.8V which is rail to rail.

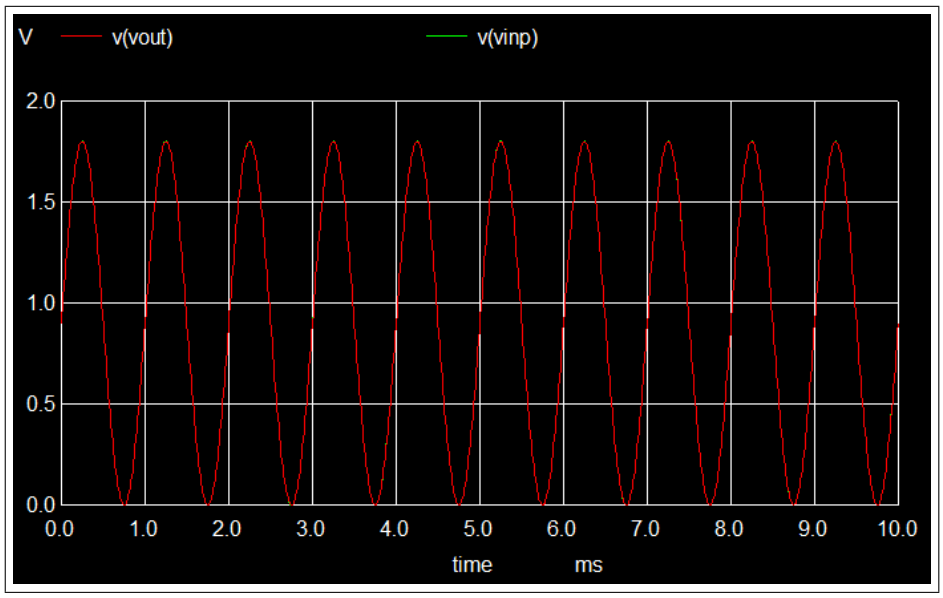


Figure 9: Output voltage swing

7 Common-mode (CM) DC Simulation

7.1 Schematic

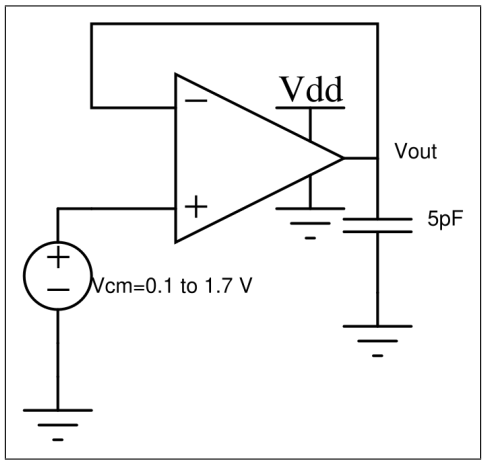


Figure 10: Common mode DC schematic

7.2 Common mode DC simulation

Below is the figure which shows the output CM DC voltage as a function of input CM DC voltage.

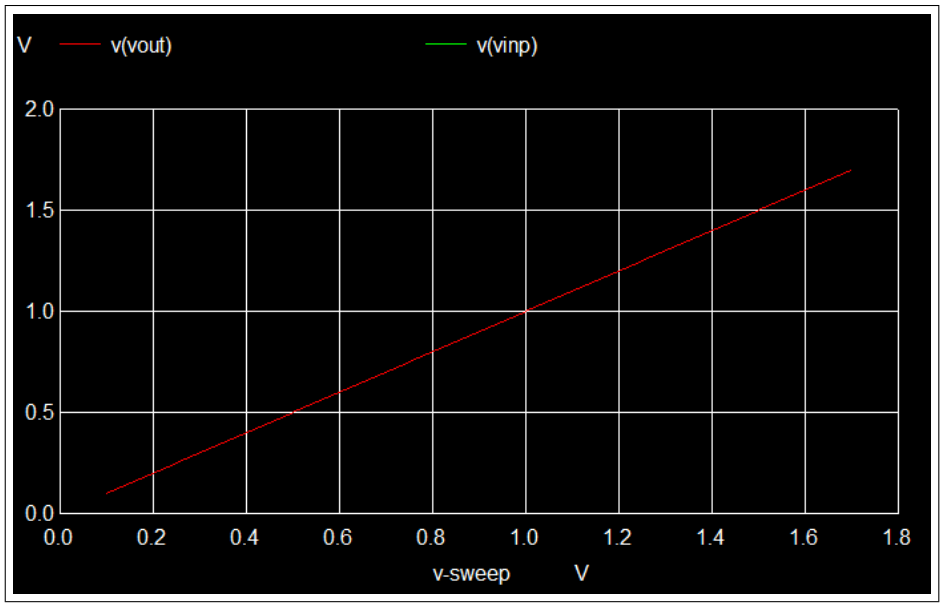


Figure 11: Common mode DC schematic

7.3 Non linearity

Below is the plot for the non linearity of the output voltage when we vary the input common voltage from 0.1 to 1.7V.

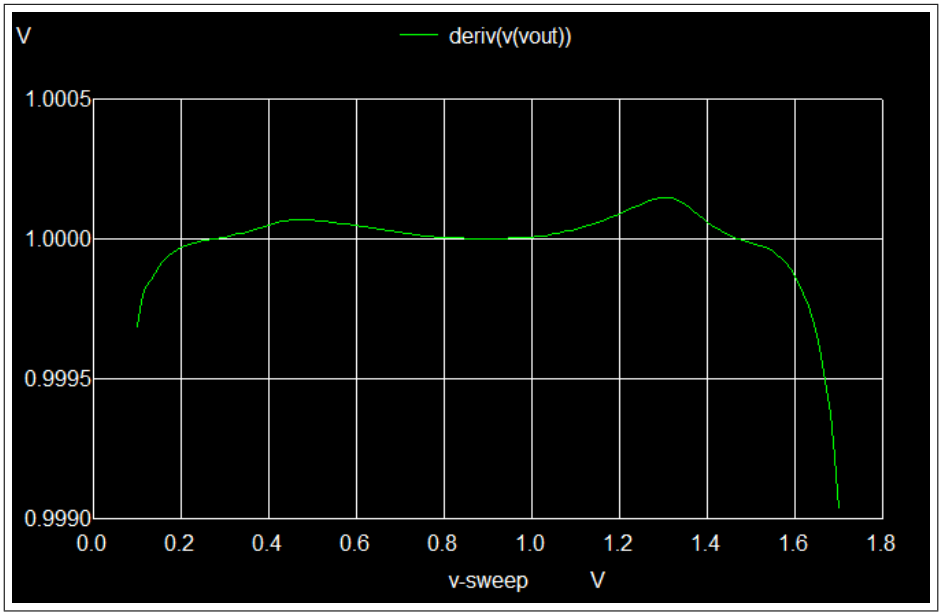


Figure 12: Non linearity of Op-amp

Below is table which shows the non linearity:

Voltage	**slope**
100 mV	0.999691
0.9 V	1
1.6 V	0.999863

Table 6: Non linearity of Op-amp

7.4 Max and Min slope

From the above graph we observer that the Op-amp has non linearity. The maximum and minimum slope is:

$$\textbf{Maximum slope} = \textbf{1.00015}$$

$$\textbf{Minimum slope} = \textbf{0.999039}$$

8 Power Consumption

Average current drawn through the entire circuit during transient operation with input 0.9 V common mode voltage was **0.434834 mA**. Therefore the power consumed is $0.434834 \times 1.8 = \textbf{0.7827 mW}$.

9 Work Contribution

Question Number	Prashant	Mihir
1.1	✓	
1.2	✓	
1.3		✓
1.4		✓
2.1	✓	
2.2	✓	
2.3	✓	
3.1		✓
3.2		✓
3.3		✓
4.1	✓	
4.2	✓	
4.3		✓
4.4		✓
5.1	✓	
5.2	✓	
6.1		✓
6.2		✓
7.1	✓	
7.2		✓
7.3	✓	
7.4		✓