Mihir Kavishwar | **17D070004**
Electrical Engineering | **Dual Degree (B.Tech. + M.Tech.)**
Indian Institute of Technology, Bombay | **Gender: Male**
Specialization: Microelectronics and VLSI | **DOB: 07-10-1999**

Examination	University	Institute	Year	CPI / %
Graduation	IIT Bombay	IIT Bombay	2022	9.19
Intermediate	HSC	Pace Junior Science College	2017	92.15%
Matriculation	ICSE	Lakshdham High School	2015	96.83%

SCHOLASTIC ACHIEVEMENTS

- Pursuing **Minor Degree** in **Systems and Control Engineering** *[2021]*
- Secured **All India Rank 287** in **JEE Advanced** amongst 1,60,000 candidates *[2017]*
- Received **Kishore Vaigyanik Protsahan Yojana** fellowship with an **All India Rank 584** *[2016]*

PROFESSIONAL & RESEARCH EXPERIENCE

System Design of PCI Express 6.0 Receiver *[May '21 - July '21]*

Company: Ceremorphic India Pvt. Ltd. | *Guide : Mr. Ajay Mantha, Director of Engineering*

- Conducted literature review of **non-ADC** based receivers for **multi-Gigabit**, **ultra-low-power** serial links
- Proposed **system architecture** for PCIe6 receiver to compensate **33 dB channel loss** at **16 GHz** in **PAM-4**
- Used **MATLAB SerDes toolbox** to perform **statistical** and **time domain** analysis of equalized output
- Implemented **gradient descent** to get optimal parameters of **multi-stage CTLE** for known channel response

Current Copier based Mixed-Signal Multiplier *[Jan '20 - May '21]*

Research Project | *Advanced Integrated Circuits and Systems Lab, IIT Bombay* | *Guide : Prof. Rajesh Zele*

- Explored a **novel circuit** for Mixed-Signal Multiplication with support for **fractional multiplicand**
- Implemented **4-bit** Multiplier operating at **1 MHz** with $< 7\%$ output error for input current range of **500 nA - 5A**

Analog and Mixed-Signal Circuits for Machine Learning Applications *[Aug '20 - Dec '20]*

Supervised Research Exposition | *Advanced Integrated Circuits and Systems Lab, IIT Bombay* | *Guide : Prof. Rajesh Zele*

- Reviewed literature on **Multiply and Accumulate** circuits operating in current, charge, phase and time domains
- Studied **subthreshold** circuits such as **Bump Anti-Bump** and **Winner-Take-All** used in **RBF Classifiers**
- Implemented a simple **binary classifier** in **Cadence** using **In-Memory Computing** in standard **6T SRAM** array

Verification of FPGA based High Frequency Trading Platform *[May '20 - July '20]*

Company: APT Portfolio Pvt. Ltd. | *Guide : Mr. Vivek Panikkar, Senior Verification Engineer*

- Emulated **MicroBlaze** processor in **QEMU** and proposed an efficient method for verifying **bare-metal** code
- Used **Vivado** and **Xilinx SDK** tools for simulating RTL design and generating **Device Tree** files

Receiver Equalizers in High Speed Serial Links *[May '19 - July '19]*

Company: STMicroelectronics Pvt. Ltd. | *Guide : Mr. Paras Garg, Senior Group Manager*

- Designed **CTLE** and **3-tap adaptive DFE** for **800 Mbps** NRZ wireline receiver in **32 nm LP CMOS** technology
- Implemented a **StrongArm Latch** with **30 mV sensitivity** to function as decision slicer at the receiver

COURSEWORK & TECHNICAL SKILLS

VLSI	Digital, Analog, Mixed Signal, $\Delta\Sigma$ Modulators, High Speed Interconnects, Neuromorphic†
Computer Science	Data Structures and Algorithms, Machine Learning, Microprocessor, Computer Aided Design
Miscellaneous	Probability, Signal Processing, Mobile Robotics, State Estimation, Game Theory, Economics
Software Tools	C++, Python, MATLAB, Verilog, VHDL, Cadence Virtuoso, ModelSim, ROS, SolidWorks

† *to be completed by Nov '21*

KEY COURSE PROJECTS

Digital to Analog Converter Design | *Mixed Signal VLSI Design* *[March '21 - April '21]*

- Designed and characterized an **8-bit Binary Current Steering Digital to Analog Converter** in **gpdk 45nm** for **1.2 V** supply, **1 GSps** sampling frequency and **0.9 V** full scale output voltage swing
- Designed **current source biasing** circuit and **digital input driver** for unit cell at transistor level
- Performed **FFT** and **Monte Carlo** analysis, achieved **50 dB SFDR**, < 0.5 **LSB INL** and < 1 **LSB DNL**

Clock and Data Recovery System Design | *High Speed Interconnects* *[March '21 - April '21]*

- Designed **Half Rate Phase Detector** in **Verilog-A** using **D-latch** and **XOR gate** and characterized it for PRBS input
- Simulated **CDR loop** in Cadence using specifications for **charge pump** and **loop filter** from MATLAB simulations

Hardware Implementation of ML Classifiers | *VLSI Design Lab* *[Jan '21 - April '21]*

- Implemented **RBF Kernel SVM** and **3-layer Neural Net** classifiers in **Verilog** with structural design methodology
- Achieved **80.2%** accuracy for SVM and **67.2%** accuracy for Neural Net on testing over open source diabetes dataset

Operational Amplifier Design | *CMOS Analog VLSI Design* *[Oct '20 - Nov '20]*

- Designed a two stage rail-to-rail **folded cascode OpAmp** with **Class AB** output stage in **PTM 180nm**
- Achieved **100 dB** DC gain, **10 MHz** unity gain bandwidth, **100 mV to 1.7 V** output voltage swing, **60°** phase margin and **2 V**/μs slew rate for 5 pF capacitive load

Attitude Estimation using MEMS Sensors | *Sensors in Instrumentation* *[Oct '20 - Nov '20]*

- Critically analysed different techniques in literature for attitude estimation of rigid bodies using low-cost sensors
- Implemented **Extended Kalman Filter** and **Unscented Kalman Filter** in **MATLAB** to estimate **roll** and **pitch** from a smartphone's raw **accelerometer** and **gyroscope** sensor data

Pipelined RISC Processor | *Microprocessors* *[Oct '19 - Nov '19]*

- Designed and tested on FPGA an 8-register, 16-bit, 6-stage **Pipelined RISC** processor written in VHDL
- Employed **Branch Prediction** and **Hazard Mitigation techniques** to optimize the performance of processor

POSITIONS OF RESPONSIBILITY

Teaching Assistant | *Digital Systems, Instructor: Prof. Siddharth Tallur* *[July '21 - Present]*

- Responsible for designing assignments, conducting tutorial sessions and evaluating answer scripts

Institute Student Mentor | *Student Mentorship Program, IIT Bombay* *[July '20 - May '21]*

- Mentored **14 freshmen** by providing guidance in academic and extracurricular endeavors
- Awarded **Special Recognition** for going above and beyond the call of responsibility

Department Academic Mentor | *Student Mentorship Program, IIT Bombay* *[July '20 - Present]*

- Mentored **6 sophomores** with the focus on helping academically weaker students
- Assisting a **4^{th} year student** clear his backlogs to ensure timely completion of curriculum

Editorial Team Member | *Background Hum, EE Department Newsletter* *[June '21 - Present]*

- Leading an article on **Global Chip Shortage** and a different article on **Research Scholars** for upcoming edition
- Contributing to an article covering **Deep Tech Startups** founded by electrical engineering department faculty

Electrical Subdivision Head | *Robocon India 2019* *[Sept '18 - April '19]*

- Led the electrical subdivision of technical team which achieved **All India Rank 9** in first stage of **Robocon India**
- Interfaced Xbox remote with microcontroller for wheeled robot and worked on control of quadruped robot

EXTRACURRICULAR

- Secured **88th position** among **1490 participants** in **10 km run** organised by Hari Krishna Group *[2019]*
- Won **Bronze medal** in inter-hostel **Table Tennis General Championship** representing Hostel 4 *[2018]*
- Built a pressure sensitive pen for **dynamic handwriting recognition** as a technical summer project *[2018]*
- Won **2nd prize** in **Android Hackathon** organized by Web and Coding Club of IIT Bombay *[2018]*