Mihir Kavishwar — Curriculum Vitae

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Research Interests

Integrated circuits and systems, machine learning, high speed serial links, computer architecture

Education

Princeton University, New Jersey, USA   [2022 - Present]
- **PhD Student** in the Department of Electrical and Computer Engineering

Indian Institute of Technology Bombay, Mumbai, India   [2017 - 2022]
- **Dual Degree** (B.Tech + M.Tech) in Electrical Engineering, **CPI**: 9.35 / 10
- **Specialization**: Microelectronics
- **Minor Degree**: Systems and Control Engineering

Scholastic Achievements

- Awarded **Gordon Wu Fellowship** for pursuing doctoral studies at Princeton University   [2022]
- Received **Undergraduate Research Award** for exceptional work in the Dual Degree Project   [2022]
- Awarded **Excellence in Teaching Assistantship** in Digital Systems course   [2021]
- Secured **All India Rank 287** in JEE Advanced among 1,60,000+ candidates   [2017]

Publications

- **M. Kavishwar**, P. Kurrey and R. Zele, "Analog Acoustic Feature Extraction and Delta-Sigma Modulation based Neural Network Classification for Voice Activity Detection," 2022 IEEE 19th India Council International Conference (INDICON), Kochi, India, 2022, pp. 1-4, doi: 10.1109/INDICON56171.2022.10039873.

- P. Kurrey, **M. Kavishwar** and R. Zele, "Analog/Mixed-Signal Classification for Voice Activity Detection," 2022 29th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Glasgow, United Kingdom, 2022, pp. 1-4, doi: 10.1109/ICECS202256217.2022.9971057.

Research Experience

Dual Degree Project (Master's Thesis) ⚹   [Aug'21 - June'22]
Title: Analog Acoustic Feature Extraction and Mixed-Signal / Digital Classification for Voice Activity Detection
Guide: Prof. Rajesh Zele, Department of Electrical Engineering, IIT Bombay

- Designed a novel **voice activity detector** up to transistor-level schematics in 65nm CMOS technology
- Validated the system architecture to perform **acoustic feature extraction** in the analog domain and **neural network classification** in mixed-signal / digital domains
- Compared ideal **Mel-spectrograms** with those generated by analog acoustic feature extractor
- Implemented a **convolutional neural network** directly within a delta-sigma ADC and achieved $\leq \mathbf{10\%}$ error

Current Copier based Mixed-Signal Multiplier ⚹   [Jan'21 - May'21]
Guide: Prof. Rajesh Zele, Department of Electrical Engineering, IIT Bombay
- Explored a novel sampled current mode mixed-signal multiplier supporting **fractional multiplicand**
- Designed a **4-bit** multiplier operating at **1 MHz** and achieved $\leq \mathbf{7\%}$ error for 500 nA - 5 μA input range
- Employed **dummy switch compensation** technique to minimize **charge injection** and used **complementary switches** to reduce **clock feedthrough** at the common gate node

Analog and Mixed-Signal Circuits for Machine Learning Applications ⬀ [Aug'20 - Dec'20]
Guide: Prof. Rajesh Zele, Department of Electrical Engineering, IIT Bombay
- Reviewed literature on energy-efficient **multiply and accumulate** circuits operating in different electrical domains such as - voltage, current, charge, phase and time
- Analyzed **subthreshold** circuits such as **bump anti-bump** and **winner-take-all** used in **RBF classifiers**
- Studied chip implementations of analog VLSI trainable classifiers based on **floating-gate MOSFET**
- Designed a **binary classifier** based on **in-memory computing** in standard **6T SRAM** array and simulated the design in Cadence AMS

Industry Experience

System Design of PCI Express 6.0 Receiver [May'21 - July'21]
Ceremorphic India Pvt. Ltd. — Guide: Prof. Nijwm Wary, Consultant, Assistant Professor at IIT Bhubaneswar
Company Overview: Ceremorphic is developing Silicon Systems in TSMC 5nm with its patented architecture for embedded, edge and high-performance markets in evolving AI era
- Conducted literature review of analog mixed-signal receivers for **multi-Gigabit**, **ultra-low-power** serial links
- Proposed system architecture for PCIe6 receiver to compensate **33 dB channel loss** at **16 GHz** in **PAM-4**
- Generated an **IBIS-AMI** model using **MATLAB SerDes toolbox** and performed transient simulations
- Implemented **gradient descent** to get optimal parameters of **multi-stage CTLE** given a channel response
- Achieved **3.46 dB channel operating margin** with statistical simulations of proposed system architecture

Verification of FPGA-based High Frequency Trading Accelerator [May'20 - July'20]
A.P.T. Portfolio Pvt. Ltd. — Guide: Mr. Vivek Panikkar, Senior Verification Engineer
Company Overview: A.P.T. Portfolio specializes in quantitative strategies, statistical analysis and algorithms, and has grown rapidly in the last decade to become the largest proprietary trading house in India
- Completed training in **universal verification methodology** with SystemVerilog and cocotb
- Emulated **MicroBlaze** processor in **QEMU** and proposed an efficient method for verifying **bare-metal** code
- Used Vivado and Xilinx SDK tools for simulating RTL design and generating device tree files

Design and Analysis of Receiver Equalizers in High-Speed Serial Links [May'19 - July'19]
STMicroelectronics N.V. — Guide: Mr. Paras Garg, Senior Group Manager, Analog & IO Solutions
Company Overview: STMicroelectronics is a global semiconductor leader delivering intelligent and energy-efficient products and solutions that power the electronics at the heart of everyday life
- Designed **continuous time linear equalizer** and **3-tap adaptive decision feedback equalizer** in 32nm LP CMOS for an low voltage differential signaling receiver operating at **800 Mbps**
- Designed a **StrongArm latch** with **30 mV sensitivity** to function as decision slicer at the receiver
- Successfully reduced inter-symbol interference and achieved **500 mV eye height** post equalization

Key Technical Projects

FeRAM based RPU for DNN Training and Inference ⬀ [Sep'21 - Nov'21]
Course: Neuromorphic Engineering — Instructor: Prof. Udayan Ganguly
- Simulated a Resistive Processing Unit in MATLAB using FeFET as the non-volatile memory element
- Employed **stochastic computing** to train a DNN-based MNIST classifier and achieved 80% training accuracy
- Proposed a circuit to harness inherent stochasticity of ultrascaled FeFETs for efficient multiplication

Current Steering Digital to Analog Converter Design ⬀ [March'21 - April'21]
Course: Mixed-Signal VLSI Design — Instructor: Prof. Rajesh Zele
- Designed and characterized an 8-bit Binary Current Steering DAC in gpdk 45nm for **1.2 V** supply, **1 GSps** sampling frequency and **0.9 V** full scale output voltage swing
- Performed **FFT** and **Monte Carlo** analysis, achieved **50 dB SFDR**, < 0.5 **LSB INL** and < 1 **LSB DNL**

Clock and Data Recovery Circuits ⧉ [March'21 - April'21]
Course: High Speed Interconnects — Instructor: Prof. Shalabh Gupta
- Designed and characterized **half rate phase detector** in **Verilog-A** using **D-latch** and **XOR gate**
- Simulated **CDR loop** in Cadence after deriving **charge pump** and **loop filter** specifications in MATLAB

Digital Implementation of Machine Learning Classifiers ⧉ [Feb'21 - April'21]
Course: VLSI Design Lab — Instructor: Prof. Sachin Patkar
- Implemented **RBF kernel SVM** and **3-layer neural net** classifiers in Verilog for **edge inference**
- Designed modules for floating point multiply-and-accumulate, ReLU, exponential and winner-take-all

Folded Cascode Operational Amplifier Design ⧉ [Oct'20 - Nov'20]
Course: CMOS Analog VLSI Design — Instructor: Prof. Maryam Shojaei Baghini
- Designed a two stage rail-to-rail folded cascode OpAmp with **class AB** output stage in **PTM 180nm**
- Achieved **100 dB** DC gain, **10 MHz** unity gain bandwidth, **100 mV to 1.7 V** output voltage swing, **60º** phase margin and **2 V/μs** slew rate for 5 pF capacitive load

Attitude Estimation using low-cost MEMS Sensors ⧉ [Oct'20 - Nov'20]
Course: Sensors in Instrumentation — Instructor: Prof. Siddharth Tallur
- Collected raw **accelerometer** and **gyroscope** data from smartphone to estimate **roll** and **pitch**
- Critically analysed different techniques in literature for attitude estimation and implemented **extended Kalman filter** and **unscented Kalman filter** in MATLAB to compare their tracking accuracy

NFC based Battery-Less Sensor Interfacing Platform ⧉ [Jan'20 - March'20]
Course: Electronic Design Lab — Instructor: Prof. Siddharth Tallur
- Demonstrated **battery-less LED blinking** with **NXP NTAG I^{2}C Plus** based electronic system
- Used **MSP430** microcontroller and **BQ25504** Power Management Unit for developing a general purpose **energy harvesting** platform for displaying sensor measurements on NFC-enabled smartphone

Pipelined RISC Processor Design ⧉ [Oct'19 - Nov'19]
Course: Microprocessors — Instructor: Prof. Virendra Singh
- Designed and tested on **FPGA** an **8-register**, **16-bit**, **6-stage** pipelined RISC processor written in **VHDL**
- Employed **branch prediction** and **hazard mitigation** techniques to optimize the performance of processor

Robocon India 2019 Competition ⧉ [Sept'18 - April'19]
DD-Robocon is an annual Robotics competition organized by Doordarshan for college students
- Led the electrical subsystem of Team STRIDE and secured **All India Rank 9** in stage 1
- Interfaced **Xbox remote** with Arduino for wheeled robot and worked on control of **quadruped robot**

Real-time Handwriting Recognition Pen ⧉ [May'18 - June'18]
Institute Technical Summer Project
- Designed and **3D-printed** a pressure sensitive pen to instantly convert handwritten strokes into text
- Worked with **OpenCV Python** and implemented color detection algorithms for tracking pen motion

Key Courses & Technical Skills

VLSI Design:	Analog, Digital, Mixed-Signal, Delta-Sigma Data Converters, VLSI CAD
Computer Science:	Data Structures and Algorithms, Machine Learning, Microprocessors
Robotics:	Control Systems, State Estimation, Advanced Topics in Mobile Robotics
Miscellaneous:	Neuromorphic Engineering, Sensors in Instrumentation, Signal Processing
Design Tools:	Cadence Virtuoso, Ngspice, LaSI, Intel Quartus, Xilinx Vivado HLS, EAGLE
Programming:	C++, Python, MATLAB, VHDL, Verilog, Verilog-AMS, SystemVerilog, cocotb

Positions of Responsibility

Graduate Teaching Assistant   [Jan'22 - May'22]
Course: Mixed Signal VLSI Design — Instructor: Prof. Rajesh Zele
- Assisted professor in managing logistics and course plan for a class of 70+ students
- Responsible for ideation, supervision and evaluation of course project on design of DAC with Cadence tools
- Contributed to design and evaluation of examinations throughout the semester

Undergraduate Teaching Assistant   [July'21 - Nov'21]
Course: Digital Systems — Instructor: Prof. Siddharth Tallur
- Assisted professor in managing logistics and course plan for a class of 200+ students
- Designed assignments and examinations, conducted tutorials and evaluated answer scripts

Editorial Board Member, BackgroundHum   [May'21 - May'22]
BackgroundHum is the official student Newsletter of the Department of Electrical Engineering, IIT Bombay
- Lead panelist for an article covering the **global chip shortage** and it's impact in our department
- Interviewed various stakeholders to understand challenges in setting up **commercial semiconductor fab**
- Lead panelist for an article **demystifying the PhD program** of the Department of Electrical Engineering

Institute and Department Academic Mentor   [July'20 - July'21]
Student Mentorship Program enables constructive interaction and mentorship of junior students by their seniors
- Selected via a rigorous procedure comprising statement of purpose, peer reviews and interviews
- Mentored **14 undergradute freshmen** by providing guidance in academic and extracurricular endeavors
- Mentored **6 sophomores** in the EE department with the focus on helping academically weaker students

Extra-Curricular Activities

- Secured 88th position among 1490 participants in 10 km run organised by Hari Krishna Group
- Won Bronze medal in inter-hostel Table Tennis General Championship representing Hostel 4
- Won 2nd prize in Android Hackathon organized by Web and Coding Club of IIT Bombay
- Achieved top grades in Elementary and Intermediate Drawing Examinations conducted by Gov. of Maharashtra