

# MINSOO KIM

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## Summary

I am a PhD student at UC San Diego, looking for a full-time position (starting in 2022) in the digital VLSI physical design and the Electronic Design Automation (EDA) area. I currently research at VLSI CAD Laboratory (ABKGroup) under the supervision of Prof. Andrew B. Kahng. Before joining UCSD, I worked in the Design Technology team at Samsung as a physical design engineer and developed physical design methodologies for advanced technology nodes (Samsung Foundry 7, 8, 10, 14 and 28nm technologies). My research interests lie in technology-aware physical design methodology, design-technology co-optimization (DTCO), open-source EDA and machine learning-based prediction/optimization for physical design.

**(\*\*Work availability: CPT/pre-OPT/post-OPT (F-1) available from 2022)**

## Skills

### Research Skills

- SoC physical design flows from RTL to GDS
- Develop an open-sourced academic physical design flow from RTL to GDS (OpenROAD)
- Technology-aware physical design optimization
- Design and Technology Co-Optimization (DTCO)
- Machine learning in physical design

### Electronic Design Automation (EDA) Tools

- Synthesis: Design Compiler, Genus
- Place and Route: IC compiler (ICC), IC compiler II (ICC2) and Innovus
- Static Timing Analysis: Primetime and Tempus
- Design Verification: Calibre and IC Validator
- Power Integrity Verification: Redhawk and Voltus

### Programming Language Skills

- Verilog HDL, **Tcl**, **C/C++**, **Python**, Perl
- Version control software: Git, Perforce

## Experience

### Graduate Student Researcher / VLSI CAD Laboratory University of California, San Diego

**09/2017 to Present**  
**La Jolla, CA, USA**

- Design-Technology Co-Optimization (DTCO) methodology for power, performance, area and cost (PPAC) evaluations at an early stage of technology development
- Machine Learning (ML)-assisted pathfinding for advanced technology nodes (Collaboration with Qualcomm)
- Technology-aware leakage optimization/placement methodology and power stapling for advanced technologies (Collaboration with Samsung)
- Optimization of top-level clock trees for memory-dominant designs (Collaboration with NXP semiconductors)
- Open-sourcing research project (OpenROAD, Open-source RTL-to-GDS) (<https://theopenroadproject.org>) supported by Defense Advanced Research Projects Agency (DARPA)
- Collaboration with Qualcomm, Samsung, Intel, Arm, NXP and the C-DEN center (<http://cden.ucsd.edu>)
- Experienced with 7, 12, 14, 16, 28, 45, 65 and 130nm technologies from multiple academia/industry PDKs
- Teaching Assistant (TA) for VLSI Integrated Circuits and Systems Design (ECE260B/CSE241A, Lecturer: Prof. Andrew B. Kahng) in Winter 2019

### Interim Engineering Intern / Design Technology Team Qualcomm Technologies, Inc.

**06/2021 to 09/2021**  
**San Diego, CA, USA**

- Enable PROBE2.0 ([link](#)) for routability assessment and IR drop analysis at 4nm technology

**Software Intern / Digital and Signoff Group**  
**Cadence Design Systems**

**06/2020 to 09/2020**  
**Austin, TX, USA**

- Developed a buffering methodology for detailed balancing of clock trees in clock tree synthesis stage (ccopt, Innovus)

**Physical Design Engineer / Design Technology Team**  
**Samsung Electronics**

**02/2013 to 07/2017**  
**Hwaseong-si, South Korea**

- Developed physical design methodology for Samsung 7/8/10/14/28nm technology nodes
- Developed reference flow scripts and routing technology files of Synopsys IC Compiler and IC Compiler II for Samsung 10/14/28nm technology nodes
- Enabled complex design rule support in P&R tools for 10/14/28nm technology nodes
- Technical support for Samsung foundry customers (Qualcomm, NVIDIA, AMD, ST Microelectronics)
- Collaboration with EDA companies (Cadence, Synopsys and Mentor Graphics) for tool development at advanced technology nodes
- Experienced with multiple SoC projects for design verification (STA, DRC, LVS)
- Physical design and tape-out of the world-first Samsung 10nm SoC project

**Graduate Research Assistant / Smart Sensor Architecture Laboratory**  
**KAIST**

**02/2011 to 02/2013**  
**Daejeon, South Korea**

- Thesis: An Efficient Energy Management for Solar-Powered Wireless Visual Sensor Networks
- Research for an energy management scheme for camera systems with solar-powered batteries in wireless visual sensor networks

## Education and Training

**Ph.D.: Electrical and Computer Engineering**  
UC San Diego  
Advised by Prof. Andrew B. Kahng

**Expected in 06/2022**  
La Jolla, CA, USA

**M. S.: Electrical Engineering**  
KAIST  
Advised by Prof. Chong-Min Kyung

**02/2013**  
Daejeon, South Korea

**B. S.: Electrical Engineering**  
Yonsei University

**02/2011**  
Seoul, South Korea

## Publications

(\*\*\*All papers with Prof. Andrew B. Kahng, have authors listed in alphabetical order)

### Journal

- [J1] C.-K. Cheng, A. B. Kahng, H. Kim, Minsoo Kim, D. Lee, D. Park and M. Woo "**PROBE2.0: A Systematic Framework for Routability Assessment from Technology to Design in Advanced Nodes**", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2021, doi:10.1109/TCAD.2021.3093015.

## Conference

- [C9] C. Chidambaram, A. B. Kahng, **Minsoo Kim**, G. Nallapati, S. C. Song and M. Woo, "**A Novel Framework for DTCO: Fast and Automatic Routability Assessment with Machine Learning for Sub-3nm Technology Options**", *Proc. IEEE Symposium on VLSI Technology*, 2021, pp. 1-2.
- [C8] H. Fatemi, A. B. Kahng, **Minsoo Kim** and J. Pineda de Gyvez "**Optimal Bounded-Skew Steiner Trees to Minimize Maximum k-Active Dynamic Power**", *Proc. ACM/IEEE International Workshop on System-Level Interconnect Problems and Pathfinding*, 2020, pp. 1-8.
- [C7] A. Rovinski, T. Ajayi, **Minsoo Kim**, G. Wang and M. Saligane, "**Bridging Academic Open-Source EDA to Real-World Usability**", *Proc. ACM/IEEE International Conference on Computer-Aided Design*, 2020, pp. 1-7.
- [C6] V. A. Chhabria, A. B. Kahng, **Minsoo Kim**, U. Mallappa, S. S. Sapatnekar, B. Xu, "**Template-based PDN Synthesis in Floorplan and Placement Using Classifier and CNN Techniques**", *Proc. ACM/IEEE Asia and South Pacific Design Automation Conference*, 2020, pp. 44-49.
- [C5] T. Ajayi, V. A. Chhabria, M. Fogaça, S. Hashemi, A. Hosny, A. B. Kahng, **Minsoo Kim**, J. Lee, U. Mallappa, M. Neseem, G. Pradipta, S. Reda, M. Saligane, S. S. Sapatnekar, C. Sechen, M. Shalan, W. Swartz, L. Wang, Z. Wang, M. Woo and B. Xu, "**Toward an Open-Source Digital Flow: First Learnings from the OpenROAD Project**", *Proc. ACM/IEEE Design Automation Conference*, 2019, pp. 76:1-76:4.
- [C4] T. Ajayi, D. Blaauw, T.-B. Chan, C.-K. Cheng, V. A. Chhabria, D. K. Choo, M. Coltella, S. Dobre, R. Dreslinski, M. Fogaça, S. Hashemi, A. Hosny, A. B. Kahng, **Minsoo Kim**, J. Li, Z. Liang, U. Mallappa, P. Penzes, G. Pradipta, S. Reda, A. Rovinski, K. Samadi, S. S. Sapatnekar, L. Saul, C. Sechen, V. Srinivas, W. Swartz, D. Sylvester, D. Urquhart, L. Wang, M. Woo and B. Xu, "**OpenROAD: Toward a Self- Driving, Open-Source Digital Layout Implementation Tool Chain**", *Proc. Government Microcircuit Applications and Critical Technology Conference*, 2019, pp. 1105-1110.
- [C3] S. Heo, A. B. Kahng, **Minsoo Kim**, L. Wang and C. Yang "**Detailed Placement for IR Drop Mitigation by Power Staple Insertion in Sub-10nm**", *Proc. ACM/IEEE Design, Automation and Test in Europe*, 2019, pp. 824-829.
- [C2] S. Heo, A. B. Kahng, **Minsoo Kim** and L. Wang, "**Diffusion Break-Aware Leakage Power Optimization and Detailed Placement in Sub-10nm VLSI**", *Proc. ACM/IEEE Asia and South Pacific Design Automation Conference*, 2019, pp. 550-556. (nominated for Best Paper award)
- [C1] **Minsoo Kim**, C.-M. Kyung, K. Yi, "**An Energy Management Scheme for Solar-Powered Wireless Visual Sensor Networks Toward Uninterrupted Operations**", *Proc. IEEE International SoC Design Conference*, 2013, pp. 23-26.