Minsoo Kim

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**Summary**

I am a PhD student at UC San Diego in the digital VLSI physical design and the Electronic Design Automation (EDA) area. I currently research at VLSI CAD Laboratory (ABKGroup) under the supervision of Prof. Andrew B. Kahng. Before joining UCSD, I worked in the Design Technology team at Samsung as a physical design engineer and developed physical design methodologies for advanced technology nodes (Samsung Foundry 7, 8, 10, 14 and 28nm technologies). My research interests lie in technology-aware physical design methodology, design-technology co-optimization (DTCO), open-source EDA and machine learning-based prediction/optimization for physical design.

**Skills**

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| **Research Skills**   * SoC physical design flows from RTL to GDS * Develop an open-sourced academic physical design flow from RTL to GDS (OpenROAD) * Technology-aware physical design optimization * Design and Technology Co-Optimization (DTCO) * Machine learning in physical design   **Programming Language Skills**   * Verilog HDL, **Tcl**, C/**C++**, **Python**, Perl * Version control software: Git, Perforce | **Electronic Design Automation (EDA) Tools**   * Synthesis: Design Compiler, Genus * Place and Route: IC compiler (ICC), IC compiler II (ICC2) and Innovus * Static Timing Analysis: Primetime and Tempus * Design Verification: Calibre and IC Validator * Power Integrity Verification: Redhawk and Voltus |

**Experience**

Graduate Student Researcher / VLSI CAD Laboratory 09/2017 to Present

University of California, San Diego La Jolla, CA, USA

* Developed DTCO methodology for PPAC evaluations at an early stage of technology development
* Developed Machine Learning (ML)-assisted pathfinding for advanced nodes (w/ Qualcomm)
* Developed Technology-aware leakage optimization and power stapling methodology for advanced nodes (w/ Samsung)
* Developed top-level clock tree synthesis (CTS) optimization for memory-dominant system-on-chip (SoC)
* Participated in an open-sourcing research project (OpenROAD) (https://theopenroadproject.org) supported by DARPA
* Experienced with 7, 12, 14, 16, 28, 45, 65 and 130nm technologies from multiple academia/industry PDKs
* Collaboration with Qualcomm, Samsung, Intel, Arm, NXP and the C-DEN center ([http://cden.ucsd.edu](https://theopenroadproject.org))
* Teaching Assistant (TA) for VLSI Integrated Circuits and Systems Design (ECE260B/CSE241A, Lecturer: Prof. Andrew B. Kahng) in Winter 2019

Interim Engineering Intern / Design Technology Team 06/2021 to 09/2021

Qualcomm Technologies, Inc. San Diego, CA, USA

* Enable PROBE2.0 ([link](https://vlsicad.ucsd.edu/Publications/Journals/j137.pdf)) for routability assessment and IR drop analysis at 4nm technology

Software Intern / Digital and Signoff Group 06/2020 to 09/2020

Cadence Design Systems Austin, TX, USA

* Developed a buffering methodology for detailed balancing of clock trees in clock tree synthesis stage (ccopt, Innovus)

Physical Design Engineer / Design Technology Team 02/2013 to 07/2017

Samsung Electronics Hwaseong-si, South Korea

* Developed physical design methodologies for Samsung 7, 8, 10, 14, 28nm technology nodes
* Developed reference flow scripts and technology files of ICC and ICC2 for Samsung 10, 14, 28nm technology nodes
* Enabled new design rules in P&R tools for 10, 14, 28nm technology nodes
* Technical support for Samsung foundry customers (Qualcomm, NVIDIA, AMD, ST Microelectronics)
* Worked with EDA vendors (Cadence, Synopsys and Mentor Graphics) for tool development at advanced technologies
* Experienced with multiple SoC projects for design verification (including STA, DRC, LVS)
* Participated in physical design and tape-out of the world-first Samsung 10nm SoC project

Graduate Research Assistant / Smart Sensor Architecture Laboratory 02/2011 to 02/2013

KAIST Daejeon, South Korea

* Thesis: An Efficient Energy Management for Solar-Powered Wireless Visual Sensor Networks
* Research for an energy management scheme for camera systems with solar-powered batteries in wireless visual sensor networks

**Education and Training**

Ph.D.: Electrical and Computer Engineering **Expected in 06/2022**

UC San Diego La Jolla, CA, USA

Advised by Prof. Andrew B. Kahng

M.S.: Electrical Engineering **02/2013**

KAIST Daejeon, South Korea

Advised by Prof. Chong-Min Kyung

B.S.: Electrical Engineering **02/2011**

Yonsei University Seoul, South Korea

**Publications**

**(\*\*\*All papers with Prof. Andrew B. Kahng, have authors listed in alphabetical order)**

**Journal**

* [J2]A. B. Kahng, **Minsoo Kim**, S. Kim and M. Woo **"An Open-Source Rosetta Stone for Physical Design Research"**, *IEEE Design & Test*, 2021, in preparation.
* [J1]C.-K. Cheng, A. B. Kahng, H. Kim, **Minsoo Kim**, D. Lee, D. Park and M. Woo **"PROBE2.0: A Systematic Framework for Routability Assessment from Technology to Design in Advanced Nodes"**, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2021, doi:10.1109/TCAD.2021.3093015.

**Conference**

* [C10] C.-K. Cheng, A. B. Kahng, I. Kang, **Minsoo Kim**, D. Lee, B. Lin, D. Park and M. Woo, "**CoRe-ECO: Concurrent Refinement of Detailed Place-and-Route for an Efficient ECO Automation**", Proc. IEEE International Conference on Computer Design, 2021, to appear.
* [C9] C. Chidambaram, A. B. Kahng, **Minsoo Kim**, G. Nallapati, S. C. Song and M. Woo, "**A Novel Framework for DTCO: Fast and Automatic Routability Assessment with Machine Learning for Sub-3nm Technology Options**", *Proc. IEEE Symposium on VLSI Technology*, 2021, pp. 1-2.
* [C8]H. Fatemi, A. B. Kahng, **Minsoo Kim** and J. Pineda de Gyvez **"Optimal Bounded-Skew Steiner Trees to Minimize Maximum k-Active Dynamic Power"**, Proc. *ACM/IEEE International Workshop on System-Level Interconnect Problems and Pathfinding*, 2020, pp. 1-8.
* [C7]A. Rovinski, T. Ajayi, **Minsoo Kim**, G. Wang and M. Saligane, **"Bridging Academic Open-Source EDA to Real-World Usability"**, *Proc. ACM/IEEE International Conference on Computer-Aided Design*, 2020, pp. 1-7.
* [C6]V. A. Chhabria, A. B. Kahng, **Minsoo Kim**, U. Mallappa, S. S. Sapatnekar, B. Xu, **"Template-based PDN Synthesis in Floorplan and Placement Using Classifier and CNN Techniques"**, *Proc. ACM/IEEE Asia and South Pacific Design Automation Conference*, 2020, pp. 44-49.
* [C5]T. Ajayi, V. A. Chhabria, M. Fogaça, S. Hashemi, A. Hosny, A. B. Kahng, **Minsoo Kim**, J. Lee, U. Mallappa, M. Neseem, G. Pradipta, S. Reda, M. Saligane, S. S. Sapatnekar, C. Sechen, M. Shalan, W. Swartz, L. Wang, Z. Wang, M. Woo and B. Xu, **"Toward an Open-Source Digital Flow: First Learnings from the OpenROAD Project"**, *Proc. ACM/IEEE Design Automation Conference*, 2019, pp. 76:1-76:4.
* [C4]T. Ajayi, D. Blaauw, T.-B. Chan, C.-K. Cheng, V. A. Chhabria, D. K. Choo, M. Coltella, S. Dobre, R. Dreslinski, M. Fogaça, S. Hashemi, A. Hosny, A. B. Kahng, **Minsoo Kim**, J. Li, Z. Liang, U. Mallappa, P. Penzes, G. Pradipta, S. Reda, A. Rovinski, K. Samadi, S. S. Sapatnekar, L. Saul, C. Sechen, V. Srinivas, W. Swartz, D. Sylvester, D. Urquhart, L. Wang, M. Woo and B. Xu, **"OpenROAD: Toward a Self- Driving, Open-Source Digital Layout Implementation Tool Chain"**, *Proc. Government Microcircuit Applications and Critical Technology Conference*, 2019, pp. 1105-1110.
* [C3]S. Heo, A. B. Kahng, **Minsoo Kim**, L. Wang and C. Yang **"Detailed Placement for IR Drop Mitigation by Power Staple Insertion in Sub-10nm"**, *Proc. ACM/IEEE Design, Automation and Test in Europe*, 2019, pp. 824-829.
* [C2]S. Heo, A. B. Kahng, **Minsoo Kim** and L. Wang, **"Diffusion Break-Aware Leakage Power Optimization and Detailed Placement in Sub-10nm VLSI"**, *Proc. ACM/IEEE Asia and South Pacific Design Automation Conference*, 2019, pp. 550-556. **(Nominated for Best Paper award)**
* [C1] **Minsoo Kim**, C.-M. Kyung, K. Yi, **"An Energy Management Scheme for Solar-Powered Wireless Visual Sensor Networks Toward Uninterrupted Operations"**, *Proc. IEEE International SoC Design Conference*, 2013, pp. 23-26.

**Talk**

* [T5] C. Chidambaram, A. B. Kahng, **Minsoo Kim**, G. Nallapati, S. C. Song and M. Woo, "**A Novel Framework for DTCO: Fast and Automatic Routability Assessment with Machine Learning for Sub-3nm Technology Options**", *IEEE Symposium on VLSI Technology*, June 2021.
* [T4]H. Fatemi, A. B. Kahng, **Minsoo Kim** and J. Pineda de Gyvez **"Optimal Bounded-Skew Steiner Trees to Minimize Maximum k-Active Dynamic Power"**, *ACM/IEEE International Workshop on System-Level Interconnect Problems and Pathfinding*, November 2020.
* [T3] **Minsoo Kim**, “P**ROBE2.0: A Systematic Framework for Routability Assessment from Technology to Design in Sub-7nm Nodes"**, *C-DEN Workshop, October* 2020.
* [T2]S. Heo, A. B. Kahng, **Minsoo Kim**, L. Wang and C. Yang **"Detailed Placement for IR Drop Mitigation by Power Staple Insertion in Sub-10nm"**, *ACM/IEEE Design, Automation and Test in Europe*, March 2019.
* [T1] **Minsoo Kim**, “Mixed-Diffusion Break and Power Stapling Optimizations for Improved PPA in 5nm Technology”, *C-DEN Workshop*, November 2018.

**Poster**

* [P5] C.-T. Ho, A. B. Kahng, C. Kim, **Minsoo Kim** and L. Wang, “**Multi-Bit Combinational Cell Placement for Power Reduction**”, *C-DEN Workshop*, November 2019.
* [P4] A. B. Kahng, **Minsoo Kim** and H. Y. Liu, “**Gate-Cut-Aware Detailed Placement and Leakage Optimization in Advanced Technologies**”, *C-DEN Workshop*, June 2019.
* [P3] S. Heo, A. B. Kahng, **Minsoo Kim**, L. Wang and C. Yang “**Detailed Placement for IR Drop Mitigation by Power Staple Insertion in Sub-10nm VLSI**”, *C-DEN Workshop*, November 2018.
* [P2] S. Heo, A. B. Kahng, **Minsoo Kim** and L. Wang “**Single vs. Double Diffusion Break: Studies of 2nd DB Impacts on Leakage and Density in Sub-10nm VLSI**”, *C-DEN Workshop*, May 2018.
* [P1] A. B. Kahng, **Minsoo Kim** and L. Wang, “**Combined Detailed Placement and Power Reduction for 7nm and Beyond IC Technologies**”, *UCSD Research Expo*, April 2018.