| | | | |
|---|---|---|---|
| **School/Faculty** | Computing/Engineering | **Page:** | 1 of 8 |
| **Programme Name** | Bachelor of Computer Science (Computer Networks & Security) | | |
| **Course code:** | SECR1013 | **Academic Session/Semester:** | 2024/2025-1 |
| **Course name:** | DIGITAL LOGIC | **Pre/co requisite:** | NIL |
| **Credit hours:** | 3 | | |

# COURSE OUTLINE

| | |
|---|---|
| **Course synopsis** | Digital electronics is the foundation of all microprocessor-based systems found in computers, robots, automobiles, and industrial control systems. This course introduces the students to digital electronics and provides a broad overview of many important concepts, components, and tools. Students will get up-to-date coverage of digital fundamentals-from basic concepts to programmable logic devices. Laboratory experiments provide hands-on experience with the simulator software, actual devices and circuits studied in the classroom |
| **Course coordinator** | Dr. Mohd Fo'ad bin Rohani |

| | **Name** | **Section** | **Office** | **E-mail @utm.my** |
|---|---|---|---|---|
| **Course lecturer(s)** Bachelor in Software Engineering | Dr. Zuriahati binti Mohd Yunos | 01 | N28-438-02, Level 4 N28 | zuriahati |
| | Dr. Mohd Fo'ad bin Rohani | 02 | 347-02, Level 3 (N28) | foad |
| | Assoc. Prof. Dr. Norafida binti Ithnin | 03 | 02-22-01, Level 2 (N28A) | afida |
| | Mr. Ahmad Fariz bin Ali | 04 | 207-04, Level 2 (N28) | ahmadfariz |
| Bachelor of Computer Science (major) | Mr. Ahmad Fariz bin Ali | 01, 02 | 207-04, Level 2 (N28) | ahmadfariz |
| | Dr. Farkhana Binti Muchtar | 03, 08 | 438-05, Level 4 N28 | farkhana |
| | Ts. Dr. Nur Haliza binti Abdul Wahab | 04 | 02-11-01, Level 2 (N28a) | nur. haliza |
| | Dr. Zuriahati binti Mohd Yunos | 05 | N28-438-02, Level 4 N28 | zuriahati |
| | Dr. Mohd Fo'ad bin Rohani | 06, 07 | 347-02, Level 3 (N28) | foad |
| Bachelor in Software Engineering (MJIIT) | Ts. Dr. Sahnius Bt Usman | | | sahnius.kl |

**Mapping of the Course Learning Outcomes (CLO) to the Programme Learning Outcomes (PLO), Teaching & Learning (T&L) methods and Assessment methods:**

Prepared by:

| | |
|---|---|
| Name: | Dr. Mohd Fo'ad bin Rohani (Course Owner) |
| Signature: | |
| Date: | 1 Oct 2024 |

Certified by:

| | |
|---|---|
| Name: | Professor Dr Md Asri bin Ngadi (Director of Computer Science) |
| Signature: | |
| Date: | |

# COURSE OUTLINE

| No. | CLO | PLO (Code) | Weight (%) | Taxonomies and generic skills | T&L methods | *Assessment methods |
|---|---|---|---|---|---|---|
| CLO1 | Apply the fundamentals of digital knowledge concept and numbering systems to digital logic circuits. | PLO1(KW) | 12 | C3 | Lecture Tutorial | Q, T |
| CLO2 | Design combinational logic circuits using logic gates and Boolean algebra. | PLO1(KW) | 27 | C4 | Lecture Tutorial | Q, T |
| CLO3 | Design sequential asynchronous and synchronous circuits using fundamentals of latches and flip-flops. | PLO1(KW) | 29 | C4 | Lecture Tutorial | Q, F |
| CLO4 | Use the techniques, skills and digital logic tools in a successful lab exercise. | PLO2 (AP) | 17 | P3 | Lab | L1, L2, L3 |
| CLO5 | Design, implement and report on a digital logic circuit based on practical problems. | PLO2 (AP) PLO4(CS) | 15 | P5 CS1 | Problem-based learning | L4, PR, GR D |
| *T – Test; Q – Quiz; HW – Homework; L – Lab, GR – Group Report; PR – Project; D - Demo, F – Final Exam etc. | | | | | | |

**Details on Innovative T&L practices:**

| No. | Type | Implementation |
|---|---|---|
| 1. | Active learning | Conducted through in-class activities |
| 2. | Project-based learning | Conducted through design project. Students in a group of 2 design projects that require digital logic solutions involving the design and verification using real devices. Compliance to the design specifications need to be given in the form of written reports and demo. |

**Weekly Schedule:**

| **PART 1**: BASIC CONCEPT & NUMBER SYSTEMS | |
|---|---|
| **Week 1**<br>**6 – 10 Oct** | **Class briefing**<br>**Module 1: Digital Logic Overview**<br>Digital and Analogue Quantities, Binary Digits, Logic Levels and Digital Waveforms, Introduction to Logic Operations, Overview of Logic Functions, Fixed-Function IC, Programmable Logic Device (PLD) |
| **Week 2**<br>**13 – 17 Oct** | **Module 2: Number Systems and Codes**<br>Numbering System (Decimal, Binary, Octal and Hexadecimal), Number Conversion between Bases, Binary to Octal and Hexadecimal Conversion, Codes: BCD, GRAY, Parity |
| **Week 3**<br>**20 – 24 Oct** | **Module 2: Number Systems and Codes**<br>ASCII Arithmetic Operations: Integer (Unsigned, Signed Number) Operations: Addition and Subtraction |
| **Week 4**<br>**27 – 31 Oct** | **Module 3: Logic Gates**<br>Inverter (NOT), AND, OR, NAND, NOR, XOR and XNOR Gates<br>Introduction to DEEDS |

# COURSE OUTLINE

| | |
|---|---|
| **31 Oct Deepavali (Thu)** | **Module 4: Boolean Algebra and Logic Simplification**<br>Laws and Rules of Boolean Algebra, DeMorgan's Theorem<br><br>**Quiz 1** |
| **Week 5**<br>**3 – 7 Nov** | **Module 4: Boolean Algebra and Logic Simplification**<br>Logic Representation (Boolean to Logic Circuit, Logic Circuit to Boolean, Boolean to Truth Table, Logic Circuit to Truth Table,<br><br>**Lab 1: Basic Gate** |
| **Week 6**<br>**10 – 14 Nov** | **Module 4: Boolean Algebra and Logic Simplification**<br>Simplification Using Boolean Algebra, Standard Forms of Boolean Expressions (SOP and POS Form),<br><br>**Module 4: Boolean Algebra and Logic Simplification**<br>Karnaugh Map (K-Map), K-Map Minimisation (SOP and POS), Don't Care Conditions |
| **Week 7**<br>**17– 21 Nov** | **Module 4: Boolean Algebra and Logic Simplification**<br>Karnaugh Map (K-Map), K-Map Minimisation (SOP and POS), Don't Care Conditions<br><br>**Module 5: Combinational Logic Circuit**<br>Basic Combinational Logic Circuits (AND-OR, AND-OR-INVERT, XOR, XNOR), |
| **Week 8**<br>**24 Nov – 30 Nov** | **MID SEMESTER BREAK** |
| **Week 9**<br>**1 Dis – 5 Dis** | **Module 5: Combinational Logic Circuit**<br>Universal Property of NAND and NOR, Dual Symbol, Design a Combinational Circuit<br><br>**Quiz 2**<br>**Lab 2: Combinational Logic Circuit (Software Deeds)** |
| **Week 10**<br>**8 – 12 Dis** | **Module 6: Functions of Combinational Logic**<br>Basic and Parallel Binary Adders, Comparators, Decoders, Encoders, Multiplexer (Data Selector), Demultiplexer, Code Converter, Parity Generator/ Checker |
| **Week 11**<br>**15 Dis – 19 Dis** | **Module 7: Latches, Flip-Flops and Timers**<br>Latch (SR, Gated SR and Gated D), Flip-flop (SR, JK, D, T),<br><br>**Mid Term (Chap 1-5)**<br>**Tuesday (17 Dis) – 8pm – 10.30 pm** |

# COURSE OUTLINE

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|---|---|
| **Week 12**<br>**22 – 26 Dis**<br><br>***25 Dec – Christmas (Wed)*** | **Module 8: Counters**<br>Types of Sequential Circuits, Counters, Design and Analysis of Asynchronous Counter, Operation (Up/Down, Truncated), Asynchronous Counter Decoder,<br><br>**Project Assignment (Deeds)**<br>- Design Deeds<br>  o Part 1: Basic Counter (Counter, Comparator)<br>  o Part 2: Advanced Features (MSI Chap 5)<br>- Full Report, Presentation & Demo |
| **Week 13**<br>**29 Dec – 2 Jan** | **Module 8: Counters**<br>Flip-flop Excitation Table, Design and Analysis of Synchronous Counter (Up/Down, Truncated), Counter for Arbitrary Sequences,<br><br>**Lab 3- Sequential Logic Circuit (Counter)** |
| **Week 14**<br>**5 – 9 Jan** | **Module 8: Counters**<br>Cascaded Counter, Analysis of Sequential Circuits (SR, JK, D, T) |
| **Week 15**<br>**12 – 16 Jan** | **Module 9: Shift Register**<br>Basic Shift Register Functions, SISO, SIPO, PISO, PIPO, Bidirectional Shift Register, Shift Register Counter (Ring and Johnson Counter)<br><br>**Quiz 3** |
| **Week 16**<br>**19 – 25 Jan**<br><br>*29- 30 Jan (Chinese New Year)*<br><br>*11 Feb- Thaipusam* | REVISION WEEK<br>**Project 2 – Group Report, Presentation & Demo (TBA)** |
| | **Final Examination** |

**Transferable skills (generic skills learned in course of study which can be useful and utilised in other settings):**

| |
|---|
| Communication skills |

# COURSE OUTLINE

**Student learning time (SLT) details:**

| Distribution of course content | Teaching and Learning Activities | | | | | | TOTAL SLT |
|---|---|---|---|---|---|---|---|
| | Guided Learning (Face to Face) | | | | Guided Learning NF2F | Independent Learning NF2F | |
| **CLO** | **Lecture** | **Tutorial** | **Practical** | **Others** | | | |
| CLO 1 | 5 | 1 | | 2 | 2 | 4 | **14h** |
| CLO 2 | 13 | 2 | | 2 | 4 | 16 | **37h** |
| CLO 3 | 18 | 3 | | 2 | 4 | 22 | **49h** |
| CLO 4 | | | 8 | 2 | | 2 | **12h** |
| CLO 5 | | | 2 | 2 | | 4 | **8h** |
| **Total SLT** | **36** | **6** | **10** | **10** | **10** | **48** | **120h** |

| Formative Assessment | | PLO | Percentage | Total SLT |
|---|---|---|---|---|
| 1 | Lab 1 – 3 (CLO4) | PLO2 (AP) | 17 | As in CLO4 (12h) |
| 2 | Quiz 1 – 3 (CLO1, CLO2, CLO3) | PLO1 (KW) | 18 | **2h** |
| 3 | Project Design (CLO5) | PLO2 (AP) | 5 | As in CLO5 (2h) |
| 4 | Project Report (CLO5) | PLO2 (AP) | 5 | As in CLO5 (5h) |
| | Presentation/Demo (CLO5) | PLO4 (CS) | 5 | As in CLO5 (1h) |
| 5 | Mid-term (CLO1, CLO2, CLO3) | PLO1 (KW) | 20 | **2h** |
| | **Total** | | **70** | |
| Summative Assessment | | | Percentage | Total SLT |
| 1 | Final Exam (CLO3) | PLO1 (KW) | 30 | **3h** |
| | **Total** | | **30** | |
| Grand Total SLT | | | | **120h** |

**Special requirement to deliver the course (e.g: software, nursery, computer lab, simulation room):**

| |
|---|
| Digital Logic Lab and Lab Assistant (TA) |

# COURSE OUTLINE

Software: Deeds Software, WinCUPL software, Wellon software, Universal Programmer Hardware: Burner device, ETS5000, Integrated Circuits (IC), IC Tester, Coloured wire.

**Learning resources:**

**Text book (if applicable)**
Digital Logic (2018), School of Computing, Faculty of Engineering, UTMJB
Digital Logic Lab Manual (2021), School of Computing, Faculty of Engineering, UTMJB

**Main references**
Floyd, T.L., (2014), "Digital Fundamentals", 10th Edition, Prentice Hall, USA.

**Additional references**
Tocci, R.J., Widmer, N.S. and Moss, G.L, (2014), "Digital Systems", 11th Edition, Prentice Hall, USA.
Roth, C., (2014), "Fundamental of Logic Design", 7th Edition, Thomson Brooks, USA.

**Online**
**http://elearning.utm.my**

**Academic honesty and plagiarism:**

Assignments are individual tasks and NOT group activities (UNLESS EXPLICITLY INDICATED AS GROUP ACTIVITIES). Copying of work (texts, lab results etc.) from other students/groups or from other sources is not allowed. Brief quotations are allowed and then only if indicated as such. Existing texts should be reformulated with your own words used to explain what you have read. It is not acceptable to retype existing texts and just acknowledge the source as a reference. Be warned: students who submit copied work will obtain a mark of **zero** for the assignment and exams and disciplinary steps may be taken by the Faculty. It is also unacceptable to do somebody else's work, to lend your work to them or to make your work available to them to copy.

**Other additional information (Course policy, any specific instruction etc.):**

1. Attendance is compulsory and will be taken in every lecture session. Student with less than 80% of total attendance is not allowed to sit for final exam.
2. Students are required to behave and follow the University's dressing regulation and etiquette all the time.
3. Exercises and tutorial will be given in class and some may be taken for assessment. Students who do not do the exercise will lose the coursework marks for the exercise.
4. Assignments must be submitted on the due dates. Some points will be deducted for late submissions. Assignments submitted three days after the due date will not be accepted.
5. Make up exam will not be given, except to students who are sick and submit medical certificate confirmed by UTM panel doctors. Make up exam can only be given within one week of the initial date of exam.

# COURSE OUTLINE

| | | | Technical | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | PLO 1 (KW) | | | PLO2 (AP) | | PLO4 (CS) | |
| | **No.** | **Assessment** | **CLO1** | **CLO2** | **CLO3** | **CLO4** | **CLO5** | **CLO5** | **Total %** |
| | **1** | **LAB 1** | | | | **5** | | | **5** |
| | **2** | **LAB 2** | | | | **6** | | | **6** |
| | **3** | **LAB 3** | | | | **6** | | | **6** |
| | **4** | **QUIZ 1** | **6** | | | | | | **6** |
| | | **QUIZ 2** | | **6** | | | | | **6** |
| | | **QUIZ 3** | | | **6** | | | | **6** |
| | **5** | **PROJECT** | | | | | | | |
| | | **PROJECT PART 1 (Basic Design)** | | | | | **3** | | **5** |
| | | **PROJECT PART 2 (Advanced Features)** | | | | | | **2** | |
| | | **REPORT** | | | | | **5** | | **5** |
| | | **PRESENTATION** | | | | | **3** | | **5** |
| | | **DEMO** | | | | | | **2** | |
| | **6** | **MID TERM** | **6** | **14** | | | | | **20** |
| | **7** | **FINAL EXAM** | | **7** | **23** | | | | **30** |
| | | | | | | | | | |
| | **Total** | | 12 | 27 | 29 | 17 | 10 | 5 | **100** |
| | | | **68** | | | **27** | | **5** | |

# COURSE OUTLINE