NEW YORK INSTITUTE OF TECHNOLOGY

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Laboratory Report

Analysis of Binary and Ternary Capacitor Combinations

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ABSTRACT

This experiment investigated the behaviour of capacitors in **binary series** and **parallel combinations** using a breadboard (Figure 1) and capacitance meter (Figure 2). Initially, three commercial capacitors, labelled 330 μF, 100 μF, and 1000 μF, were individually tested to compare actual values with their labeled values. Each possible binary combination of capacitors was tested both in series and in parallel, and the experimental capacitance was recorded and compared to theoretical predictions. The results demonstrated minimal error percentages ranging from 0.38% to 7.74%, affirming the validity of capacitor combination formulas. Additionally, all eight theoretical configurations of three capacitors were drawn and tested to support extended understanding.

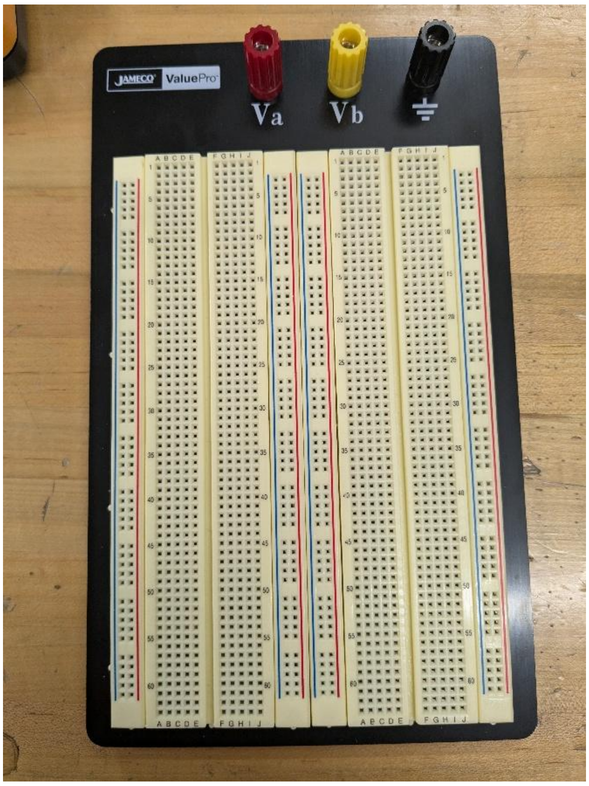


FIGURE 1. *This "breadboard" features a metal base and screw terminals for quick electronic circuits and easy wire connections to a power supply.*

FIGURE 2. *Capacitor Meter. Ensure the meter meter is zeroed before use for precise setup of readings.*

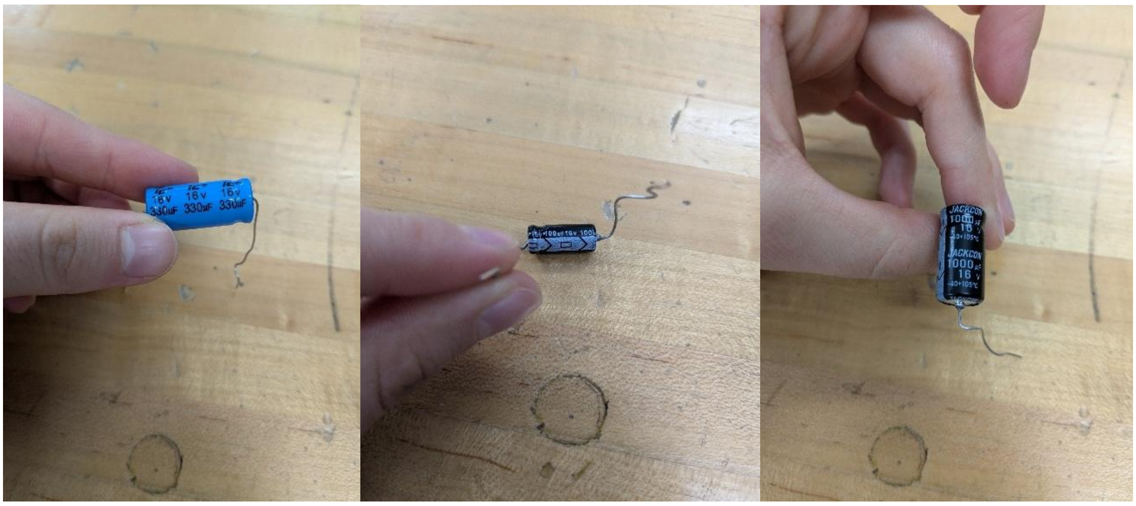


FIGURE 3. *Three commercial capacitors used in the experiment: 330 µF (blue), 100 µF (small black), and 1000 µF (large black), each rated for 16 V.*

OBJECTIVES

- To measure the actual capacitance values of three commercial capacitors and compare them to their labelled values.
- To test all binary series and parallel combinations of those capacitors.
- To compare experimental results with theoretical predictions.
- (Optional) To draw and test all 8 possible three-capacitor combinations using a breadboard.

THEORETICAL BACKGROUND

Capacitors are fundamental components in **electrical circuits**, used for ***storing electrical energy*** *by accumulating electric charge on parallel plates separated by an insulator*. The **capacitance** $\boldsymbol{C}$ is given by:

$$C = \frac{\varepsilon_0 A}{d}$$

where:

- A is the plate area,
- d is the distance between plates,
- ε_0 is the vacuum permittivity.

which shows that capacitance is **directly proportional** to **plate area** and **inversely proportio**nal to the **separation distance**.

Depending on how capacitors are arranged in a circuit, their total capacitance differs. Two standard configurations are **parallel** and **series** connections.

CAPACITORS IN PARALLEL

In a parallel configuration, the **voltage across each capacitor is the same**, and the **total charge is the sum of the individual charges**:

$$Q_{total} = Q_1 + Q_2 + Q_3 + \cdots$$

Since $\boldsymbol{Q = CV}$**,** substituting gives:

$$C_{total}V = C_1V + C_2V + C_3V + \cdots$$

Dividing both sides by V:

$$C_{parallel} = C_1 + C_2 + C_3 + \cdots$$

Thus, the **total capacitance in parallel** increases by the **direct sum** of **each capacitor's value**.

CAPACITORS IN SERIES

In a series configuration, each **capacitor has the same charge**, but the **total voltage** is the **sum of individual voltages**:

$$V_{total} = V_1 + V_2 + V_3 + \cdots$$

Using $\boldsymbol{V = \frac{Q}{C}}$, substitute:

$$\frac{Q}{C_{series}} = \frac{Q}{C_1} + \frac{Q}{C_2} + \frac{Q}{C_3} + \cdots$$

Dividing both sides by Q:

$$\frac{1}{C_{series}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} + \cdots$$

So, the **total capacitance in series** is always **less than the smallest individual capacitor**.

PRELIMINARY EXERCISE – COMMERCIAL CAPACITOR TESTING:

Before conducting the main experiment, we measured the capacitance of three commercial capacitors (Figure 3) using a capacitance meter (Figure 2) and compared the results with their labelled values.

FIGURE 4. *Capacitor C_1: 330 μF (labelled) vs. 319.64 μF (measured)*

FIGURE 5. *Capacitor C_2: 1000 μF (labelled) vs. 1075.5 μF (measured)*

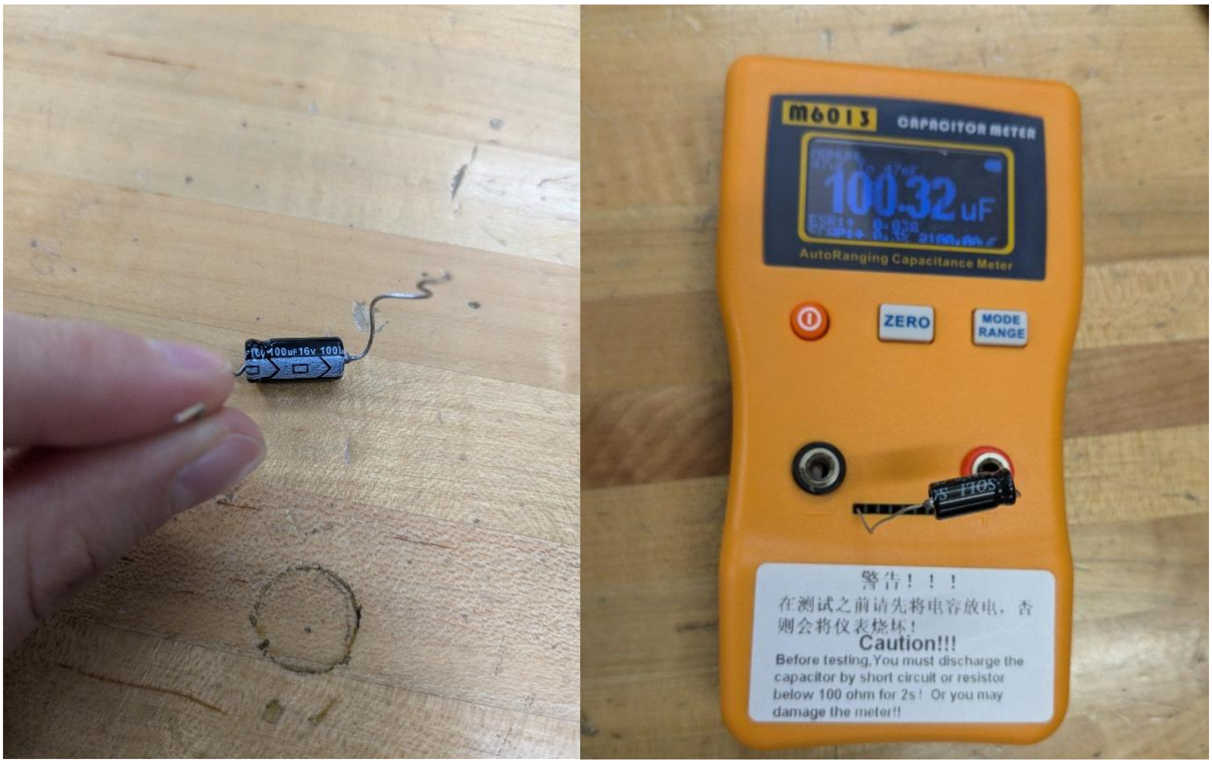


FIGURE 6. *Capacitor C_3: 100 μF (labelled) vs. 100.32 μF (measured)*

This exercise demonstrated that real-world capacitance values often differ from manufacturer specifications due to tolerance and environmental factors.

PROCEDURE

APPARATUS:

1. Breadboard (Figure 1)
2. Three electrolytic capacitors (Figure 3)
3. Capacitance meter (Figure 2)
4. Jumper wires (Figure 7)

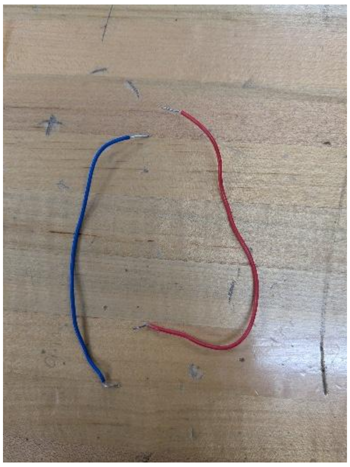
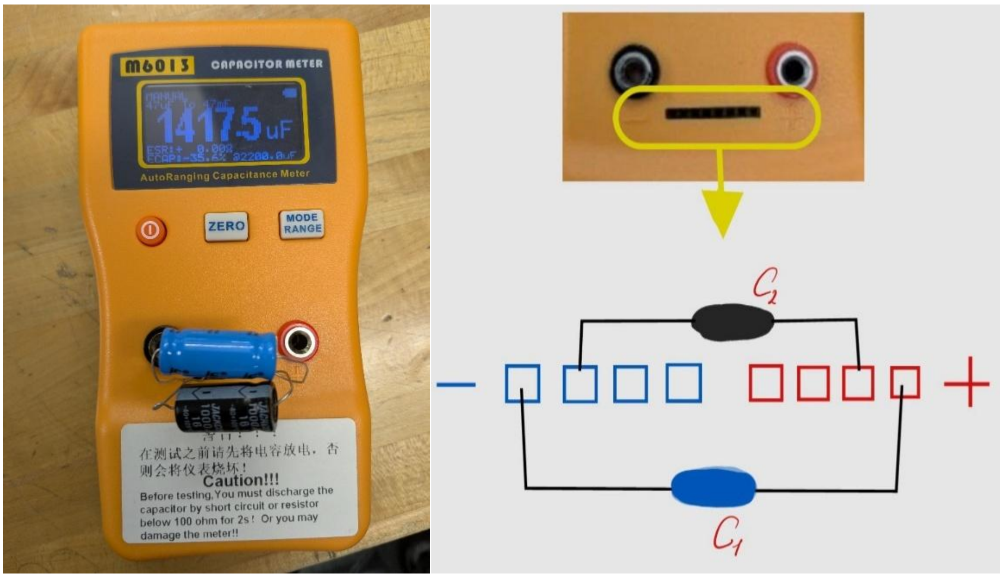


FIGURE 7. *Red and blue jumper wires.*

PARALLEL COMBINATIONS ON A METER

1. Begin by turning on the capacitance meter and pressing the ZERO button to calibrate it before inserting any components.

2. Select two capacitors to test (e.g., C_1 and C_2), and carefully insert both into the meter's testing slots in parallel configuration.
    - All positive (longer) legs of the capacitors go into one side of the clip.
    - All negative (shorter) legs go into the opposite side.
    - This aligns their terminals in parallel, sharing the same voltage.

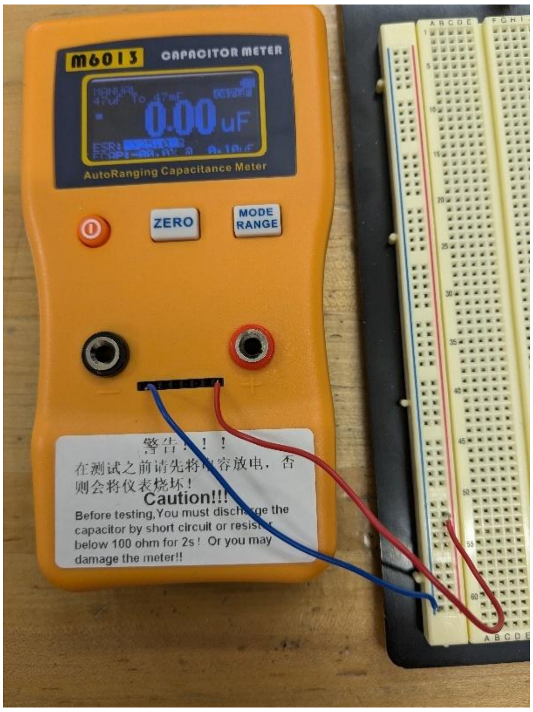


3. After each increment, record the new capacitance reading. Continue this process until reaching a plate separation of 10 mm, collecting at least 10 data points.
4. Make sure the metal legs make firm contact with the test leads.

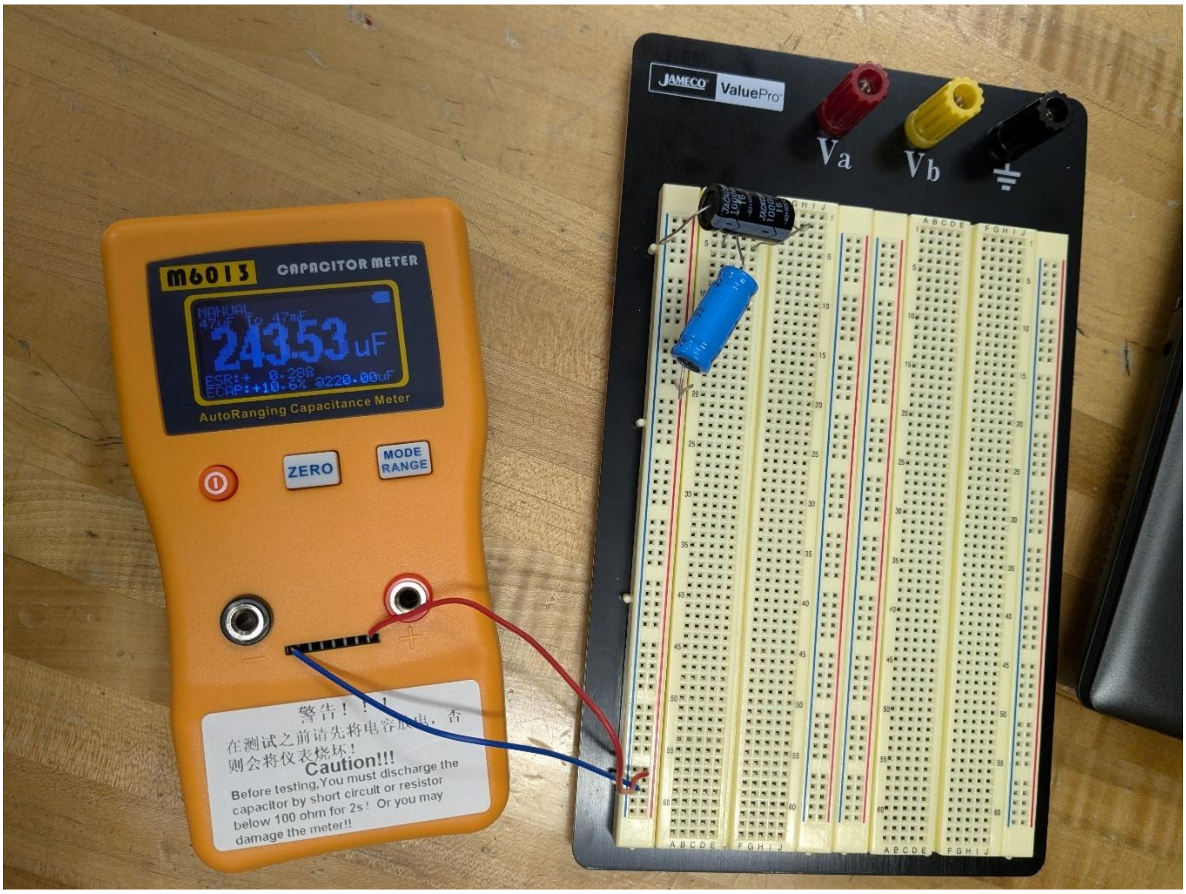
5. Observe the capacitance reading on the meter and record it.
6. Repeat steps for C1 + C3 and C2 + C3.

SERIES COMBINATIONS ON THE BREADBOARD

1. Plug the red wire from the capacitance meter into the positive slot and insert the other end into the red horizontal rail on the breadboard.
2. Plug the blue wire from the meter's negative slot into the blue horizontal rail of the breadboard.



3. For each series test:
    a) Insert the first capacitor (e.g., C1) so that:
        1. One leg goes into the **red power rail**, and
        2. The other leg goes into a **separate vertical row**.
    b) Insert the **second capacitor** (e.g., C2) so that:
        1. One leg shares the same **horizontal row** as the second leg of C1 (connecting them in series),
        2. The remaining leg goes into the **blue power rail.**



3. Make sure connections are tight and the leads aren't shorted.
4. Read the displayed capacitance and record it.
5. Repeat for C1 + C3 and C2 + C3 combinations.

DATA & ANALYSIS

The experimental data collected is summarized in the following tables:

Capacitor	Labelled Value / μF	Measured Value / μF	Error (%)
C1 (Blue)	330	319.67	3.13%
C2 (Big Black)	1000	1075.5	7.55%
C3 (Small Black)	100	100.32	0.32%

TABLE 1. *Comparison of labelled and experimentally measured capacitance values for individual capacitors.*

Combination	Type	Measured C / µF	Labelled C / µF	Error (%)
C1 + C2	Parallel	1417.5	1330	6.58%
C2 + C3	Parallel	1185.1	1100	7.74%
C1 + C3	Parallel	428.37	430	0.38%
C1 + C2	Series	243.53	252.51	3.56%
C2 + C3	Series	92.1	90.91	1.31%
C1 + C3	Series	75.42	76.74	1.73%

TABLE 2. *Comparison of measured and theoretical capacitance values for all binary combinations of capacitors in series and parallel.*

(OPTIONAL) TERNARY COMBINATIONS

As an extension to the binary capacitor analysis, all **eight** possible configurations of the **three capacitors** (C1, C2, and C3) were explored using combinations of series and parallel arrangements. Circuit diagrams were first sketched to visualize each configuration, as depicted in the figure below:

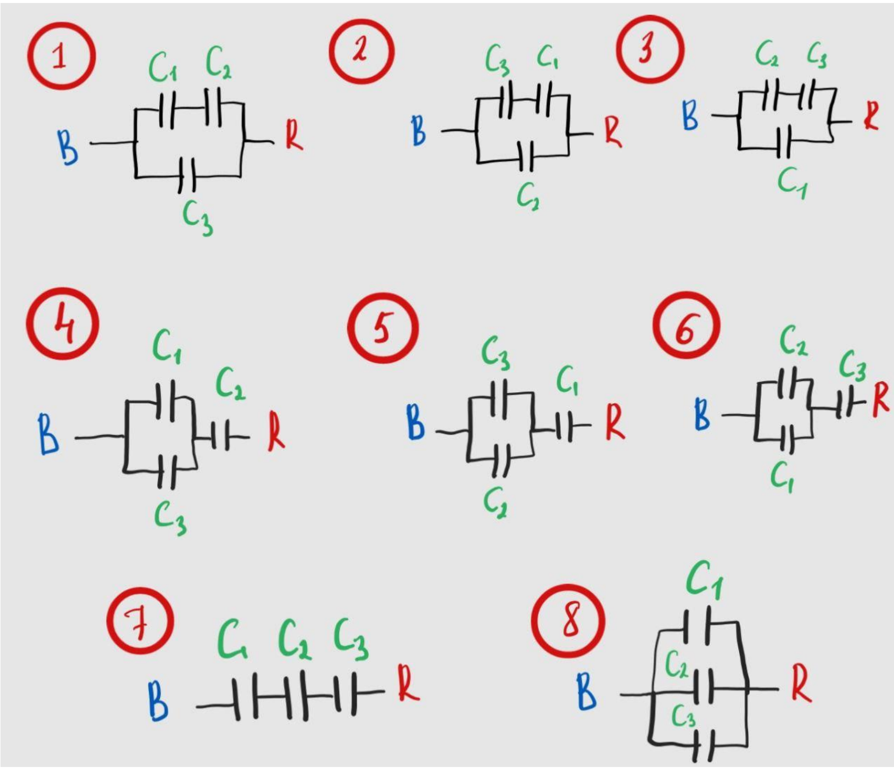
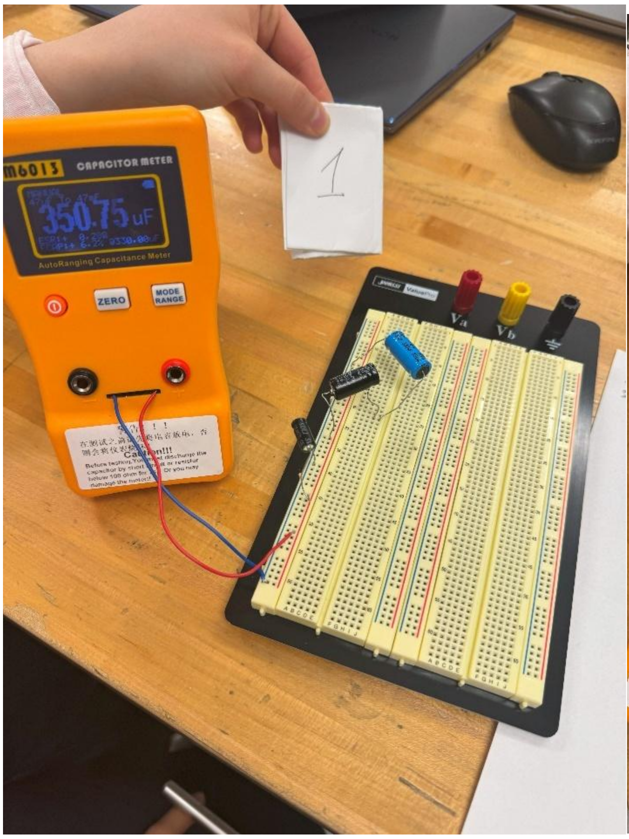
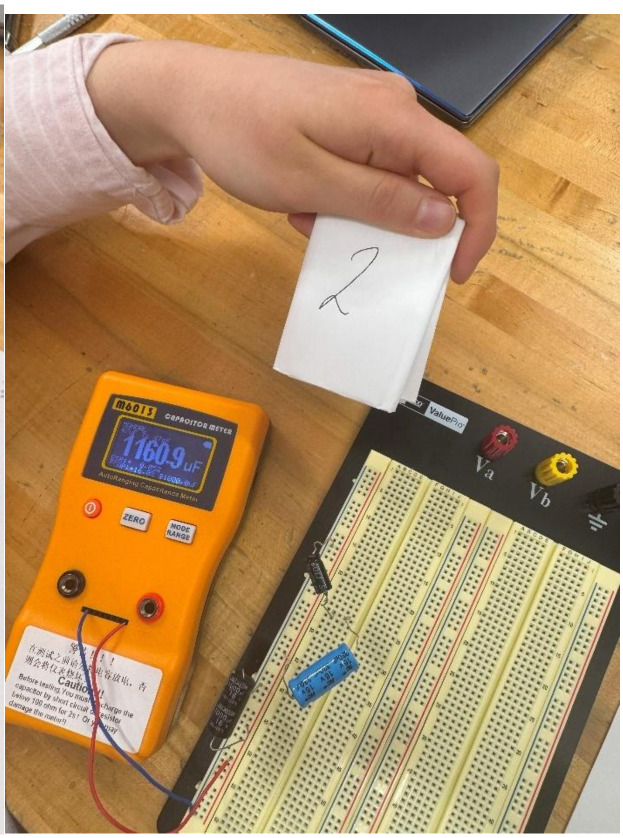
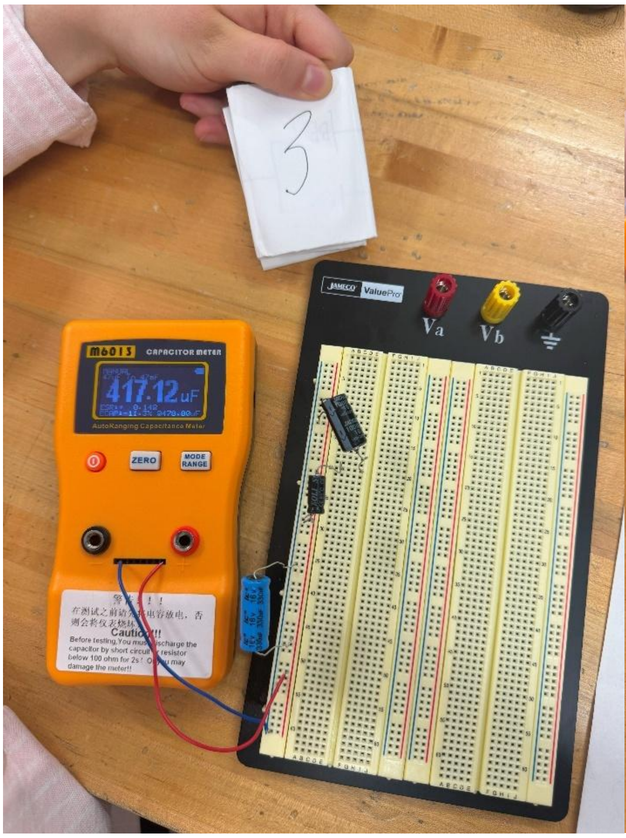


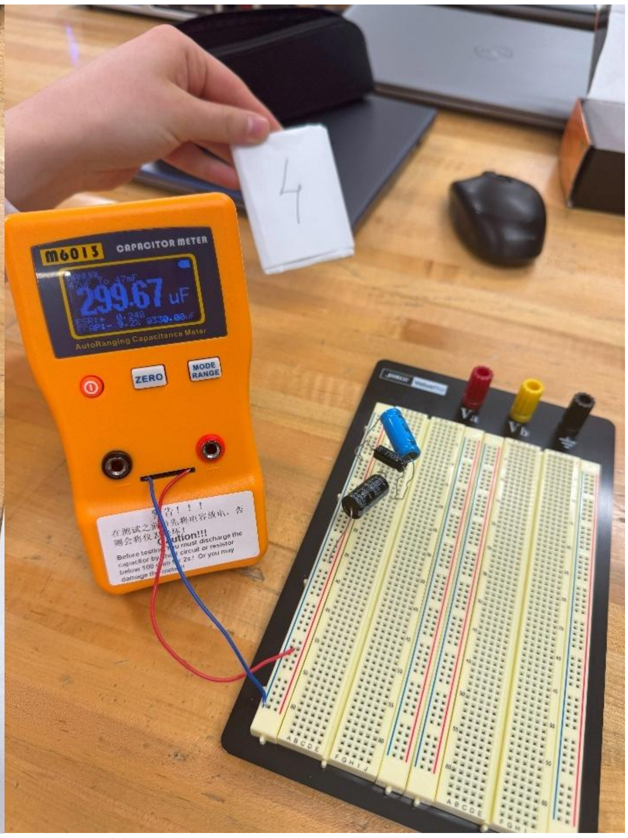
FIGURE 8. *All eight possible ternary capacitor combinations using C_1 (Blue), C_2 (Big Black), and C_3 (Small Black), illustrated through circuit diagrams showing series and parallel arrangements. B and R represent the blue (negative) and red (positive) power tails on the breadboard.*

Photographic documentation of each configuration build on a breadboard is depicted in the pictures below:









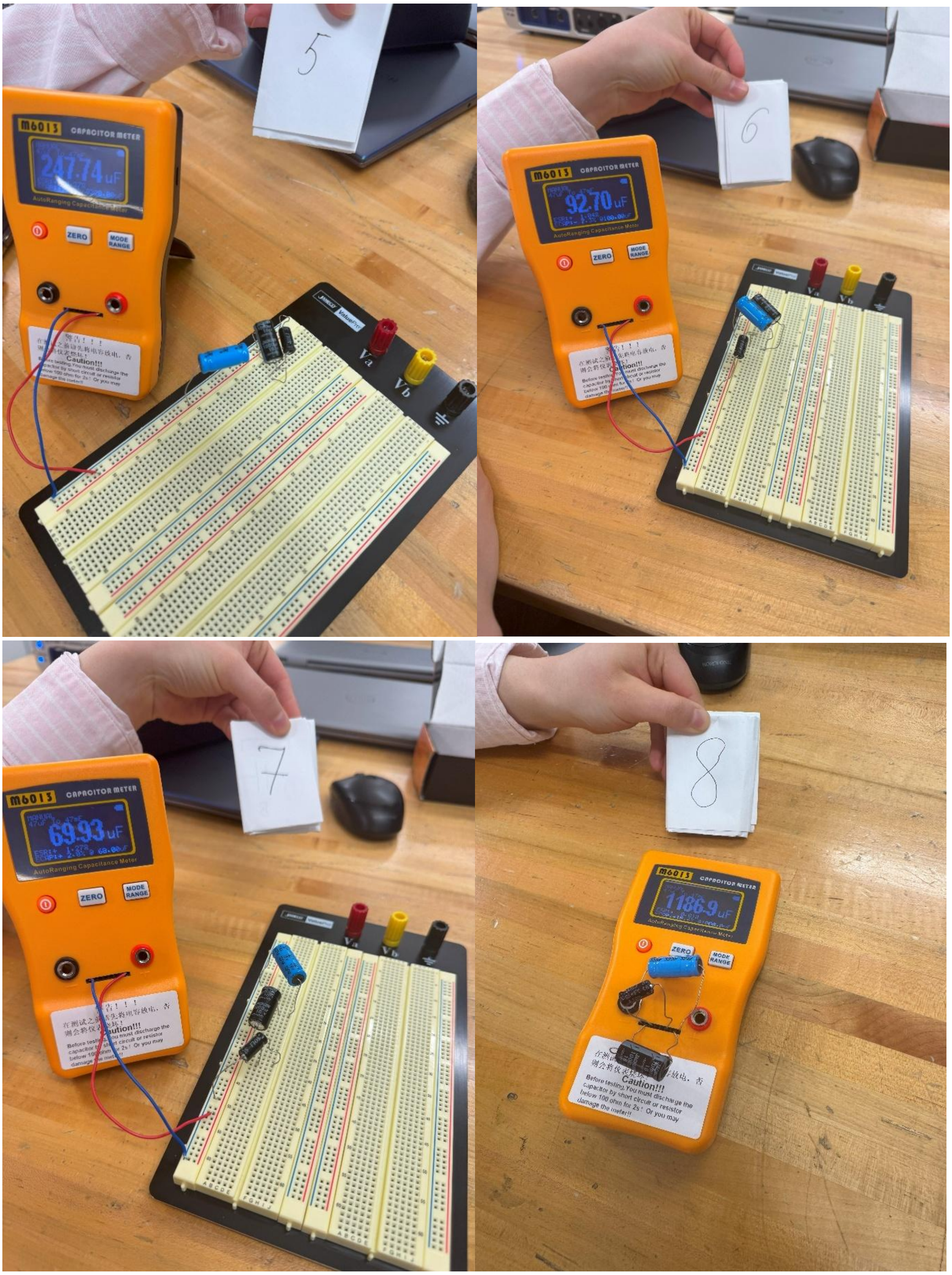


FIGURE 9. *Photographs of all eight ternary capacitor combinations built on a breadboard. Each configuration corresponds to its circuit diagram from Figure 8, as indicated by the hand-labelled number on the paper shown in each photo.*

CONCLUSION

This experiment successfully demonstrated the theoretical and practical principles of capacitors in both series and parallel configurations. By measuring the **actual capacitance values** of three distinct capacitors (C1, C2, and C3), and comparing them with their labelled values, the lab verified fundamental capacitor behaviour. The errors observed across single, binary, and ternary combinations were generally minimal **(0.38%-7.74%),** confirming the **accuracy of standard capacitor formulas**. Additionally, deriving the equations for both configurations enriched our theoretical understanding. This lab not only solidified essential electronics concepts but also developed practical circuit-building and measurement skills.

ACKNOWLEDGMENTS

I would like to acknowledge my lab partner Jonah Villafan and Jabir Rahman for his assistance in data collection. I also appreciate Dr. Ray D. Sameshima's guidance during the lab.

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FIGURES

Figures 1-9. *Photos taken during lab performance*. Photographs by Zhasmin Tuiachieva and Jabir Rahman.

TABLES

Table 1. *Labelled and measured capacitance values for individual capacitors*. By Zhasmin Tuiachieva, Jonah Villafan, and Jabir Rahman.

Table 2. *Measured and theoretical capacitance values for binary capacitor combinations*. By Zhasmin Tuiachieva, Jonah Villafan, and Jabir Rahman.