EXPERIMENT 4: CPU Datapath, Datapath/Control Unit Integration and System Testing

COEN 316-WE-X

Mik Driver

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"I certify that this submission is my original work and meets the Faculty's Expectations of Originality"

- Mik Driver

1 Introduction

Over the four labs of this course, different portions of a CPU were designed and implemented. In this lab the full working CPU will be assembled. The complete 32-bit unit will be designed as well as a 4-bit version that maps to the NEXYS A-7 development board.

2 Theory

The MIPS processor in this lab supports 20 instructions categorized into R-type (register, e.g., add, sub), I-type (immediate, e.g., addi, lw), and J-type (jump, e.g., j, jr). The datapath integrates the ALU, register file, and next-address unit with additional hardware:

- PC register: 32-bit counter tracking the current instruction address.
- Instruction cache: ROM storing machine code.
- Sign Extension unit: Expands 16-bit immediates to 32 bits (mode set by func signal).
- Data cache: RAM for load/store operations.

The control unit decodes the opcode and func fields to generate 10 critical signals (Tables 1–2):

- Single-bit signals: E.g., reg_dst selects rd (R-type) or rt (I-type) as the destination register.
- Two-bit signals: E.g., branch_type=01 triggers a branch-if-equal (beq).

Testing involves loading programs into the instruction cache and simulating execution to verify correct control signal generation (e.g., alu_src=1 for I-type instructions). For FPGA implementation, resource utilization (Slice LUTs, registers) is analyzed to assess scalability, with DONT_TOUCH attributes preserving multiple CPU instances during synthesis.

3 Experiment

In this lab, the Modelsim tool is used to perform the simulation of source code for a 32-bit CPU circuit written in VHDL. The Xilinx Vivado tool is then used to synthesise and implement the code.

To begin, the 32-bit code for the new components was written, which can be found in Tables 1, 2, 3 and 4.

Table 1: pc.vhd

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_signed.all;

entity pc is
        port (
                din : in std_logic_vector(31 downto 0);
                reset : in std_logic;
                clk : in std_logic;
                dout: out std_logic_vector(31 downto 0)
        );
end pc;

architecture arch of pc is

begin

   process( clk, reset )
   begin
      if (reset = '1') then
         dout <= (others => '0');

      elsif (clk'event and clk='1') then
         dout <= din;
      end if ;
   end process ;

end arch ;
```

Table 2: i_cache.vhd

```
library IEEE;
use IEEE.std_logic_1164.all;

entity i_cache is
   port(
      address_input     : in std_logic_vector(4 downto 0);  -- 5-bit address input
      instruction_out : out std_logic_vector(31 downto 0) -- 32-bit instruction output
   );
end i_cache;

architecture arch of i_cache is
begin
   process(address_input)
   begin
```

```
    case address_input is
        when "00000" => instruction_out <= "00100000000000110000000000000000"; -- addi r3, r0, 0
        when "00001" => instruction_out <= "00100000000000010000000000000000"; -- addi r1, r0, 0
        when "00010" => instruction_out <= "00100000000000100000000000000101"; -- addi r2, r0, 5
        when "00011" => instruction_out <= "00000000001000100000100000100000"; -- add r1, r1, r2
        when "00100" => instruction_out <= "00100000100001011111111111111111"; -- addi r2, r2, -1
        when "00101" => instruction_out <= "00010000100001100000000000000001"; -- beq r2, r3 (+1)
        when "00110" => instruction_out <= "00001000000000000000000000000011"; -- jump 3 (LOOP)
        when "00111" => instruction_out <= "10101100000000010000000000000000"; -- sw r1, 0(r0)
        when "01000" => instruction_out <= "10001100000001000000000000000000"; -- lw r4, 0(r0)
        when "01001" => instruction_out <= "00110000100001000000000000001010"; -- andi r4, r4, 0x000A
        when "01010" => instruction_out <= "00110100100001000000000000000001"; -- ori r4, r4, 0x0001
        when "01011" => instruction_out <= "00111000100001000000000000001011"; -- xori r4, r4, 0x000B
        when "01100" => instruction_out <= "00111000100001000000000000000000"; -- xori r4, r4, 0x0000
        when others  => instruction_out <= "00000000000000000000000000000000"; -- default NOP (no operation)
    end case;
  end process;
end arch;
```

Table 3: d_cache.vhd

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity d_cache is
port( din     : in std_logic_vector(31 downto 0);  -- Data input
      reset   : in std_logic;                      -- Reset signal
      clk     : in std_logic;                     -- Clock signal
      write   : in std_logic;                      -- Write enable
      address : in std_logic_vector(4 downto 0);   -- 5-bit address (32 locations)
      d_out   : out std_logic_vector(31 downto 0)  -- Data output
  );
end d_cache;

architecture arch of d_cache is
  -- Define a memory array of 32 registers, each 32 bits wide
  type t_reg_array is array (0 to 31) of std_logic_vector(31 downto 0);
  signal reg_array : t_reg_array;
begin

  -- Write process
  process(clk, reset)
  begin
    if (reset = '1') then
      -- Reset all registers to zero
      for i in 0 to 31 loop
        reg_array(i) <= (others => '0');
      end loop;
    elsif (clk'event and clk='1') then
      if write = '1' then
        reg_array(conv_integer(address)) <= din;
      end if;
    end if;
  end process;

  -- Read process
  process(address, reg_array)
  begin
    d_out <= reg_array(conv_integer(address));
  end process;

end arch;
```

Table 4: sign_extender.vhd

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;

entity sign_extender is
        port (
                sign_extender_in    : in std_logic_vector (15 downto 0); -- 16-bit input
                sign_extender_func  : in std_logic_vector (1 downto 0);  -- Function select
                sign_extender_out   : out std_logic_vector (31 downto 0) -- 32-bit output
        );
end sign_extender;

architecture arch of sign_extender is
begin
   process(sign_extender_in, sign_extender_func)
   begin
      case sign_extender_func is
         -- Load Upper Immediate (Pad LSBs with 0s)
         when "00" =>
            sign_extender_out <= sign_extender_in & X"0000";

         -- Sign Extend (Pad MSBs with sign bit)
         when "01" | "10" =>
            sign_extender_out(15 downto 0)  <= sign_extender_in;
            sign_extender_out(31 downto 16) <= (others => sign_extender_in(15));

         -- Logical Extension (Pad MSBs with 0s)
         when "11" =>
            sign_extender_out <= X"0000" & sign_extender_in;

         -- Default (Should Never Happen)
         when others =>
            sign_extender_out <= (others => '0');
      end case;
   end process;
end arch;
```

Table 5: control_unit.vhd

```
library ieee;
use IEEE.std_logic_1164.all;

entity control_unit is
  port (
    op: in std_logic_vector(5 downto 0);
    fn: in std_logic_vector(5 downto 0);
    reg_write : out std_logic;
    reg_dst : out std_logic;
    reg_in_src : out std_logic;
    alu_src : out std_logic;
    add_sub : out std_logic;
    logic_func : out std_logic_vector(1 downto 0);
    func : out std_logic_vector(1 downto 0); -- specifying the type of sign extension to be performed
    data_write : out std_logic;
    branch_type : out std_logic_vector(1 downto 0);
    pc_sel : out std_logic_vector(1 downto 0)
    );
end control_unit;
```

```
architecture arch of control_unit  is

begin

   -- generate the control signals based on opcode and fn
   process(op, fn)
   begin
      case( op ) is

         -- lui
         when "001111" =>
                  reg_write   <= '1';
                  reg_dst     <= '0';
                  reg_in_src  <= '1';
                  alu_src     <= '1';
                  add_sub     <= '0';    -- don't care
                  data_write  <= '0';
                  logic_func  <= "00";   -- don't care
                  func        <= "00";
                  branch_type <= "00";
                  pc_sel      <= "00";

         when "000000" =>
                  case( fn ) is

                     -- add
                     when "100000" =>
                              reg_write   <= '1';
                              reg_dst     <= '1';
                              reg_in_src  <= '1';
                              alu_src     <= '0';
                              add_sub     <= '0';    -- add
                              data_write  <= '0';
                              logic_func  <= "00";
                              func        <= "10";
                              branch_type <= "00";
                              pc_sel      <= "00";

                     -- sub
                     when "100010" =>
                              reg_write   <= '1';
                              reg_dst     <= '1';
                              reg_in_src  <= '1';
                              alu_src     <= '0';
                              add_sub     <= '1';    -- sub
                              data_write  <= '0';
                              logic_func  <= "00";
                              func        <= "10";
                              branch_type <= "00";
                              pc_sel      <= "00";

                     -- slt
                     when "101010" =>
                              reg_write   <= '1';
                              reg_dst     <= '1';
                              reg_in_src  <= '1';
                              alu_src     <= '0';
                              add_sub     <= '1';
                              data_write  <= '0';
                              logic_func  <= "00";
                              func        <= "01";
                              branch_type <= "00";
                              pc_sel      <= "00";

                     -- and
```

```
when "100100" =>
        reg_write   <= '1';
        reg_dst     <= '1';
        reg_in_src  <= '1';
        alu_src     <= '0';
        add_sub     <= '1';
        data_write  <= '0';
        logic_func  <= "00";
        func        <= "11";
        branch_type <= "00";
        pc_sel      <= "00";

-- or
when "100101" =>
        reg_write   <= '1';
        reg_dst     <= '1';
        reg_in_src  <= '1';
        alu_src     <= '0';
        add_sub     <= '1';
        data_write  <= '0';
        logic_func  <= "01";
        func        <= "11";
        branch_type <= "00";
        pc_sel      <= "00";

-- xor
when "100110" =>
        reg_write   <= '1';
        reg_dst     <= '1';
        reg_in_src  <= '1';
        alu_src     <= '0';
        add_sub     <= '1';
        data_write  <= '0';
        logic_func  <= "10";
        func        <= "11";
        branch_type <= "00";
        pc_sel      <= "00";

-- nor
when "100111" =>
        reg_write   <= '1';
        reg_dst     <= '1';
        reg_in_src  <= '1';
        alu_src     <= '0';
        add_sub     <= '1';
        data_write  <= '0';
        logic_func  <= "11";
        func        <= "11";
        branch_type <= "00";
        pc_sel      <= "00";

-- jr
when "001000" =>
        reg_write   <= '0';
        reg_dst     <= '0';
        reg_in_src  <= '0';
        alu_src     <= '0';
        add_sub     <= '0';
        data_write  <= '0';
        logic_func  <= "00";
        func        <= "00";
        branch_type <= "00";
        pc_sel      <= "10"; -- jump register

when others =>
        reg_write   <= '0';
```

```
                        reg_dst    <= '0';
                        reg_in_src <= '0';
                        alu_src    <= '0';
                        add_sub    <= '0';
                        data_write <= '0';
                        logic_func <= "00";
                        func       <= "00";
                        branch_type <= "00";
                        pc_sel     <= "00";

            end case ;

    -- addi
    when "001000" =>
            reg_write  <= '1';
            reg_dst    <= '0';
            reg_in_src <= '1';
            alu_src    <= '1';
            add_sub    <= '0';
            data_write <= '0';
            logic_func <= "00";
            func       <= "10";
            branch_type <= "00";
            pc_sel     <= "00";

    -- slti
    when "001010" =>
            reg_write  <= '1';
            reg_dst    <= '0';
            reg_in_src <= '1';
            alu_src    <= '1';
            add_sub    <= '1';
            data_write <= '0';
            logic_func <= "00";
            func       <= "01";
            branch_type <= "00";
            pc_sel     <= "00";

    -- andi
    when "001100" =>
            reg_write  <= '1';
            reg_dst    <= '0';
            reg_in_src <= '1';
            alu_src    <= '1';
            add_sub    <= '1';
            data_write <= '0';
            logic_func <= "00";
            func       <= "11";
            branch_type <= "00";
            pc_sel     <= "00";
    -- ori
    when "001101" =>
            reg_write  <= '1';
            reg_dst    <= '0';
            reg_in_src <= '1';
            alu_src    <= '1';
            add_sub    <= '1';
            data_write <= '0';
            logic_func <= "01";
            func       <= "11";
            branch_type <= "00";
            pc_sel     <= "00";
    -- xori
    when "001110" =>
            reg_write  <= '1';
            reg_dst    <= '0';
```

```
                reg_in_src  <=  '1';
                alu_src     <=  '1';
                add_sub     <=  '1';
                data_write  <=  '0';
                logic_func  <=  "10";
                func        <=  "11";
                branch_type <=  "00";
                pc_sel      <=  "00";

        -- lw
        when "100011" =>
                reg_write   <=  '1';
                reg_dst     <=  '0';
                reg_in_src  <=  '0';
                alu_src     <=  '1';
                add_sub     <=  '0';
                data_write  <=  '0';
                logic_func  <=  "10";
                func        <=  "10";
                branch_type <=  "00";
                pc_sel      <=  "00";

        -- sw
        when "101011" =>
                reg_write   <=  '0';
                reg_dst     <=  '0';
                reg_in_src  <=  '0';
                alu_src     <=  '1';
                add_sub     <=  '0';
                data_write  <=  '1';
                logic_func  <=  "00";
                func        <=  "10";
                branch_type <=  "00";
                pc_sel      <=  "00";

        -- j
        when "000010" =>
           reg_write   <=  '0';
           reg_dst     <=  '0';
           reg_in_src  <=  '0';
           alu_src     <=  '0';
           add_sub     <=  '0';
           data_write  <=  '0';
           logic_func  <=  "00";
           func        <=  "00";
           branch_type <=  "00";
           pc_sel      <=  "01";


        -- bltz
        when "000001" =>
           reg_write   <=  '0';
           reg_dst     <=  '0';
           reg_in_src  <=  '0';
           alu_src     <=  '0';
           add_sub     <=  '0';
           data_write  <=  '0';
           logic_func  <=  "00";
           func        <=  "00";
           branch_type <=  "11";
           pc_sel      <=  "00";

        -- beq
        when "000100" =>
           reg_write   <=  '0';
           reg_dst     <=  '0';
```

```
            reg_in_src  <=  '0';
            alu_src     <=  '0';
            add_sub     <=  '0';
            data_write  <=  '0';
            logic_func  <=  "00";
            func        <=  "00";
            branch_type <=  "01";
            pc_sel      <=  "00";

         -- bne
         when "000101" =>
            reg_write   <=  '0';
            reg_dst     <=  '0';
            reg_in_src  <=  '0';
            alu_src     <=  '0';
            add_sub     <=  '0';
            data_write  <=  '0';
            logic_func  <=  "00";
            func        <=  "00";
            branch_type <=  "10";
            pc_sel      <=  "00";

         when others =>

      end case ;
   end process ;

end arch ;
```

Next, a few “brute-force” DO files were written to ensure the various new components were functioning as intended. The Do files can be found in Tables 6, 7 and 8.

Table 6: d_cache.do

```
add wave *

# Test Case 1 - Reset: Clear all registers
# Expected: All registers should be set to 0 due to reset being active.
force din x"ABCDABCD"
force reset 1
force clk 0
force write 1
force address "00000"
run 2

# Test Case 2 - Write to register 0
# Expected: reg(0) should store x"ABCDABCD" after clk rising edge
force clk 0
run 2
force din x"ABCDABCD"
force reset 0
force clk 1
force write 1
force address "00000"
run 2

# Test Case 3 - Read from an unwritten location
```

```
# Expected: d_out should be "00000000" since reg(1) was never written to.
force clk 0
run 2
force din x"ABCDABCD"
force reset 0
force clk 1
force write 0
force address "00001"
run 2

# Test Case 4 - Read from register 0 (which should contain ABCDABCD)
# Expected: d_out should return x"ABCDABCD" since reg(0) was written earlier.
force clk 0
run 2
force clk 1
force write 0
force address "00000"
run 2

# Finish simulation
quit
```

Table 7: i_cache.do

```
add wave *

# Run initial setup
run 1ns

# Test Case 1: Fetch instruction at address "00000"
# instruction_out = "00100000000000110000000000000000" ( addi r3, r0, 0 )
force address_in 00000
run 2ns

# Test Case 2: Fetch instruction at address "00001"
# Instruction_out = "00100000000000010000000000000000" ( addi r1, r0, 0 )
force address_in 00001
run 2ns

# Test Case 3: Fetch instruction at address "00110"
# Instruction_out = "00001000000000000000000000000011" ( jump 3 (LOOP) )
force address_in 00110
run 2ns
```

Table 8: sign_extender.do

```
add wave *

#   Test Case 1 - (load upper immediate)
# sign_extender_out = "10000000000000010000000000000000"
# Pad LSBs with 16 zeros
force sign_extender_in "1000000000000001"
```

```
force sign_extender_func "00"
run 2


#   Test Case 2 - (set less immediate)
# sign_extender_out = "11111111111111111000000000000001"
# Extend MSBs with sign bit (1)
force sign_extender_in "1000000000000001"
force sign_extender_func "01"
run 2


#   Test Case 3 - (arithmetic)
# sign_extender_out = "11111111111111111000000000000001"
# Extend MSBs with sign bit (1)
force sign_extender_in "1000000000000001"
force sign_extender_func "10"
run 2


#    Test Case 4 - (logical)
# sign_extender_out = "00000000000000001000000000000001"
# Pad MSBs with 0s
force sign_extender_in "1000000000000001"
force sign_extender_func "11"
run 2
```

Following the synthesis check of all components and successful waveform simulations, the CPU code was written for the ful CPU implementation. The CPU code used port maps to connect the 32 bit components and wrapped the outputs to fit the board. The code can be found in table 9.

Table 9: CPU.vhd

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_signed.all;

entity cpu is
port(  reset : in std_logic;
        clk : in std_logic;
        rs_out, rt_out : out std_logic_vector(3 downto 0);
        pc_out : out std_logic_vector(3 downto 0); -- pc reg
        overflow, zero : out std_logic);
end cpu;

architecture rtl of cpu is
   ---------- Components ----------
component next_address
port( rt, rs : in std_logic_vector(31 downto 0);
        pc : in std_logic_vector(31 downto 0);
        target_address : in std_logic_vector(25 downto 0);
        branch_type : in std_logic_vector(1 downto 0);
```

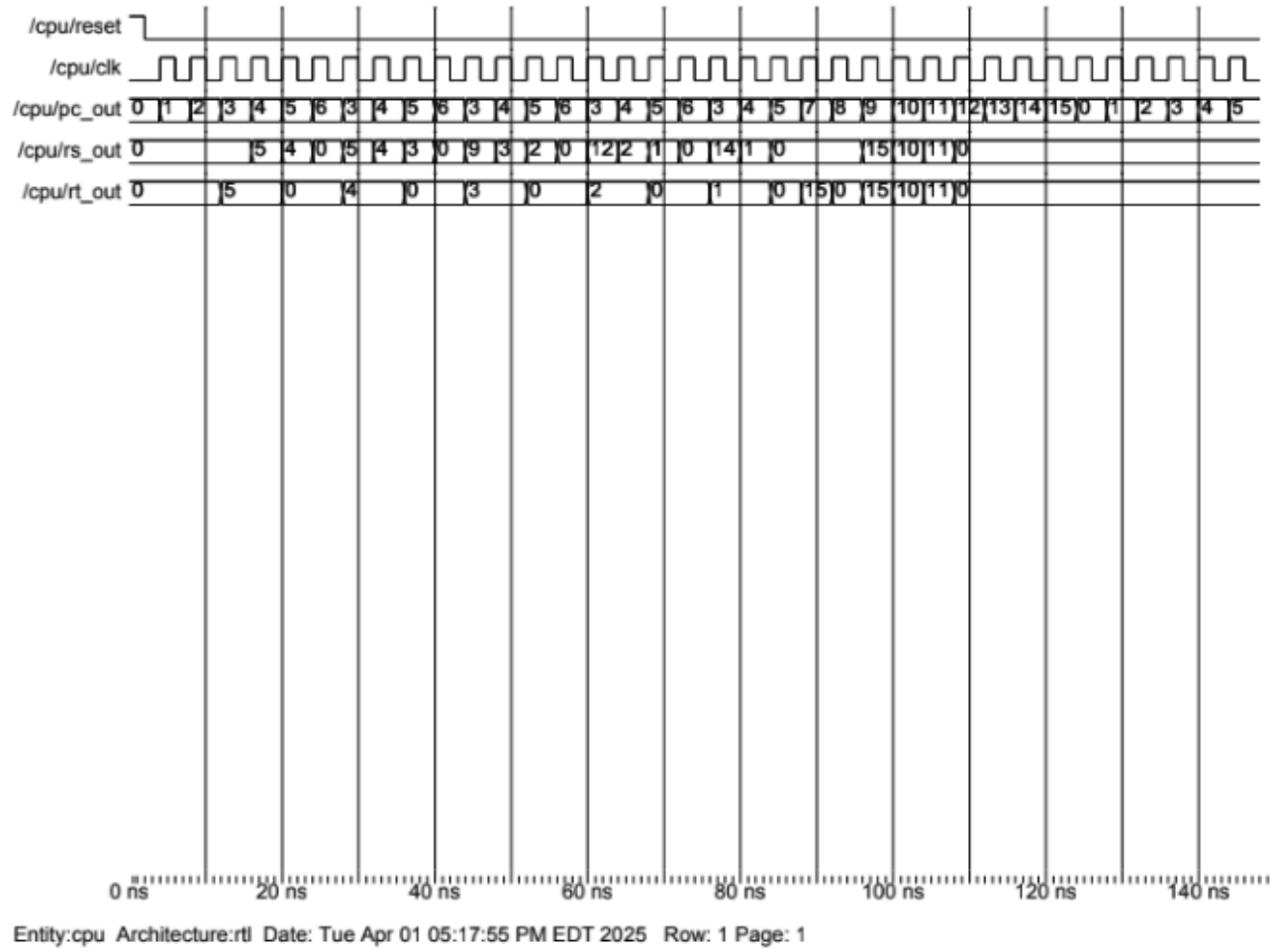
```
        pc_sel : in std_logic_vector(1 downto 0);
        next_pc : out std_logic_vector(31 downto 0));
end component ;

component pc
port ( din : in std_logic_vector(31 downto 0) := (others => '0');
        reset : in std_logic;
        clk : in std_logic;
        dout: out std_logic_vector(31 downto 0) := (others => '0')) ;
end component;

component i_cache
port(  address_input : in std_logic_vector(4 downto 0);
        instruction_out : out std_logic_vector(31 downto 0));
end component ;

component regfile
 port( din : in std_logic_vector(31 downto 0);
        reset : in std_logic;
        clk : in std_logic;
        write : in std_logic;
        read_a : in std_logic_vector(4 downto 0);
        read_b : in std_logic_vector(4 downto 0);
        write_address : in std_logic_vector(4 downto 0);
        out_a : out std_logic_vector(31 downto 0);
        out_b : out std_logic_vector(31 downto 0));
end component ;

component alu
port( x, y : in std_logic_vector(31 downto 0);
        add_sub : in std_logic ; -- 0 = add , 1 = sub
        logic_func : in std_logic_vector(1 downto 0 ) ;
        func : in std_logic_vector(1 downto 0 ) ;
        output : out std_logic_vector(31 downto 0) ;
        overflow : out std_logic ;
        zero : out std_logic);
end component ;

component d_cache
port( din : in std_logic_vector(31 downto 0);
        reset : in std_logic;
        clk : in std_logic;
        write : in std_logic;
        address : in std_logic_vector(4 downto 0);
        d_out : out std_logic_vector(31 downto 0));
end component ;

component sign_extender
port ( sign_extender_in    : in std_logic_vector (15 downto 0); -- (16-bit)
        sign_extender_func  : in std_logic_vector (1 downto 0);  -- func
        sign_extender_out   : out std_logic_vector (31 downto 0)) ;
end component;

component control_unit
port ( op: in std_logic_vector(5 downto 0);
        fn: in std_logic_vector(5 downto 0);
        reg_write : out std_logic;
```

```
        reg_dst : out std_logic;
        reg_in_src : out std_logic;
        alu_src : out std_logic;
        add_sub : out std_logic;
        logic_func : out std_logic_vector(1 downto 0);
        func : out std_logic_vector(1 downto 0);
        data_write : out std_logic;
        branch_type : out std_logic_vector(1 downto 0);
        pc_sel : out std_logic_vector(1 downto 0));
end component;

    ------------ Signals -----------
signal sig_next_pc     : std_logic_vector(31 downto 0);
signal sig_pc_dout        : std_logic_vector(31 downto 0);
signal sig_instruction_out :   std_logic_vector(31 downto 0);
signal sig_din          : std_logic_vector(31 downto 0);
signal sig_reg_address  : std_logic_vector(4 downto 0);
signal sig_out_a        : std_logic_vector(31 downto 0);
signal sig_out_b        : std_logic_vector(31 downto 0);
signal sig_alusrc_out   : std_logic_vector(31 downto 0);
signal sig_alu_output   : std_logic_vector(31 downto 0);
signal sig_d_out        : std_logic_vector(31 downto 0);
signal sig_extender_out    : std_logic_vector(31 downto 0);
signal sig_reg_in_src_out   : std_logic_vector(31 downto 0);

-- Control Signals
signal sig_op: std_logic_vector(5 downto 0);
signal sig_fn: std_logic_vector(5 downto 0);
signal sig_reg_write :  std_logic;
signal sig_reg_dst :  std_logic;
signal sig_reg_in_src :  std_logic;
signal sig_alu_src :  std_logic;
signal sig_add_sub :  std_logic;
signal sig_logic_func :  std_logic_vector(1 downto 0);
signal sig_func :  std_logic_vector(1 downto 0);
signal sig_data_write :  std_logic;
signal sig_branch_type :  std_logic_vector(1 downto 0); signal sig_pc_sel :  std_logic_vector(1 downto 0);

begin
    ---------------- Port Mapping ----------------
    program_counter : pc port map(
        din => sig_next_pc,
        reset => reset,
        clk => clk,
        dout => sig_pc_dout
    );

    instructions : i_cache port map(
        address_input => sig_pc_dout(4 downto 0),
        instruction_out => sig_instruction_out
    );

    registers_f : regfile port map(
        din => sig_reg_in_src_out,
        reset => reset,
        clk => clk,
        write => sig_reg_write,
```

```
    read_a => sig_instruction_out(25 downto 21),
    read_b => sig_instruction_out(20 downto 16),
    write_address => sig_reg_address,
    out_a => sig_out_a,
    out_b => sig_out_b
);

alu_comp : alu port map(
    x => sig_out_a,
    y => sig_alusrc_out,
    add_sub => sig_add_sub,
    logic_func => sig_logic_func,
    func => sig_func,
    output => sig_alu_output,
    overflow => overflow,
    zero => zero
);

datacache : d_cache port map(
    din => sig_out_b,
    reset => reset,
    clk => clk,
    write => sig_data_write,
    address => sig_alu_output(4 downto 0),
    d_out => sig_d_out
);

sign : sign_extender port map(
    sign_extender_in => sig_instruction_out(15 downto 0),
    sign_extender_func => sig_func,
    sign_extender_out => sig_extender_out
);

next_pc : next_address port map(
    rt => sig_out_b,
    rs => sig_out_a,
    pc => sig_pc_dout,
    target_address => sig_instruction_out(25 downto 0),
    branch_type => sig_branch_type,
    pc_sel => sig_pc_sel,
    next_pc => sig_next_pc
);

controller : control_unit port map(
    op => sig_instruction_out(31 downto 26),
    fn => sig_instruction_out(5 downto 0),
    reg_write => sig_reg_write,
    reg_dst => sig_reg_dst,
    reg_in_src => sig_reg_in_src,
    alu_src => sig_alu_src,
    add_sub => sig_add_sub,
    logic_func => sig_logic_func,
    func => sig_func,
    data_write => sig_data_write,
    branch_type => sig_branch_type,
    pc_sel => sig_pc_sel
);
```

```
    ---------- MUXes ----------
    sig_reg_address     <=  sig_instruction_out(20 downto 16) when (sig_reg_dst = '0') else
                            sig_instruction_out(15 downto 11) when (sig_reg_dst = '1');

    sig_alusrc_out      <=  sig_out_b when (sig_alu_src = '0') else
                            sig_extender_out  when (sig_alu_src = '1');

    sig_reg_in_src_out  <=  sig_d_out  when (sig_reg_in_src = '0') else
                            sig_alu_output  when (sig_reg_in_src = '1');

    ---------- Output Connections ----------
    rs_out  <= sig_out_a(3) & sig_out_a(2) & sig_out_a(1) & sig_out_a(0);
    rt_out  <= sig_out_b(3) & sig_out_b(2) & sig_out_b(1) & sig_out_b(0);
    pc_out  <= sig_pc_dout(3) & sig_pc_dout(2) & sig_pc_dout(1) & sig_pc_dout(0);

end rtl;
```

Running the source code and the do file (given) on ModelSim produced the waveform below.

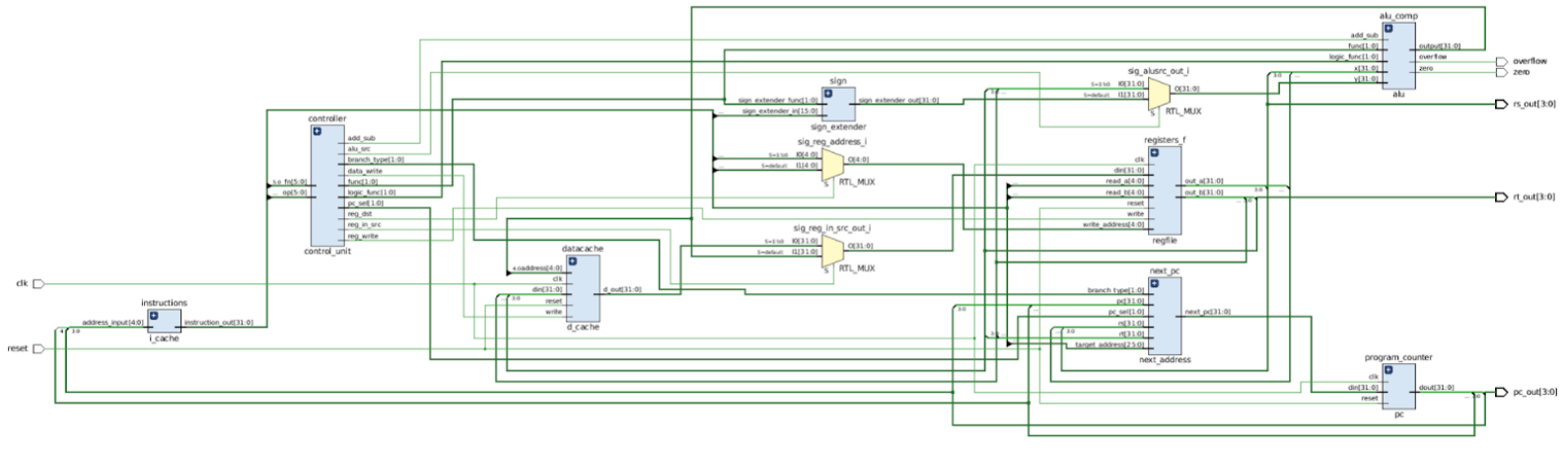


The following section of the lab is dedicated to the Xilinx tool. The constraint xdc file was given and can be found below.

Table 10: lab4.xdc

```
# Ted Obuchowicz
# XDC file for complete CPU

set_property CLOCK_DEDICATED_ROUTE  FALSE [ get_nets clk ] ;

# set the reset to the left most switch
set_property -dict { PACKAGE_PIN V10 IOSTANDARD LVCMOS33 }  [ get_ports { reset }  ] ;

# use the centre pushbutton as the clock
set_property -dict { PACKAGE_PIN N17 IOSTANDARD LVCMOS33 }  [ get_ports { clk }  ] ;

# set pc_out to left hand LEDS
set_property -dict { PACKAGE_PIN V11   IOSTANDARD LVCMOS33 } [ get_ports { pc_out[3] }  ] ;
set_property -dict { PACKAGE_PIN V12 IOSTANDARD LVCMOS33 }   [ get_ports { pc_out[2] }  ] ;
set_property -dict { PACKAGE_PIN V14 IOSTANDARD LVCMOS33 }   [ get_ports { pc_out[1] }  ] ;
set_property -dict { PACKAGE_PIN V15 IOSTANDARD LVCMOS33 }   [ get_ports { pc_out[0] }  ] ;

# set overflow and zero immediately after pc_out
set_property -dict { PACKAGE_PIN T16 IOSTANDARD LVCMOS33 }   [ get_ports { overflow }  ] ;
set_property -dict { PACKAGE_PIN U14 IOSTANDARD LVCMOS33 }   [ get_ports { zero }  ] ;

# set rs_out and rt_out to the right hand LEDS  with a gap between the two rs_out
set_property -dict { PACKAGE_PIN V16 IOSTANDARD LVCMOS33 }   [ get_ports { rs_out[3] }  ] ;
set_property -dict { PACKAGE_PIN U16 IOSTANDARD LVCMOS33 }   [ get_ports { rs_out[2] }  ] ;
set_property -dict { PACKAGE_PIN U17 IOSTANDARD LVCMOS33 }   [ get_ports { rs_out[1] }  ] ;
set_property -dict { PACKAGE_PIN V17 IOSTANDARD LVCMOS33 }   [ get_ports { rs_out[0] }  ] ;

# rt_out
set_property -dict { PACKAGE_PIN N14  IOSTANDARD LVCMOS33 }  [ get_ports { rt_out[3] }  ] ;
set_property -dict { PACKAGE_PIN J13 IOSTANDARD LVCMOS33 }   [ get_ports { rt_out[2] }  ] ;
set_property -dict { PACKAGE_PIN K15 IOSTANDARD LVCMOS33 }   [ get_ports { rt_out[1] }  ] ;
set_property -dict { PACKAGE_PIN H17 IOSTANDARD LVCMOS33 }   [ get_ports { rt_out[0] }  ] ;
```

The Xilinx tool was then used to synthesise and implement the code. The code was uploaded to the FPGA board. The resulting implementation log and synthesis log can be found in Tables 12 and 13, respectively, in the Appendix. The RTL Schematic of the CPU can be found below.



The xilinx tool produced **warings** during synthesis and implementation. Since the port maps used the full 32 bit version of the units but the output only used 4 bits, unused bits that were discarded in the board wrapping produced warnings such as the following:

• [Synth 8-3332] Sequential alement (registers_f/register_array_reg[9]([29]) is unused and will be removed from module cpu.

Since the clock was hardcoded and mapped to a button instead of using the boards clock there was also warnings such as:

• [Power 33-2321 No user defined clocks were found in the design!

Resolution: Please specify clocks using create_clock/create_generated _clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock.

otherwise the vectorless estimation might be inaccurate

• (Timing 38-313) There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.

4 Conclusion

In conclusion, a fully integrated 32-bit MIPS CPU was successfully designed and implemented using VHDL. The datapath and control unit were combined to support 20 instructions across R-type, I-type, and J-type operations, with critical control signals (e.g., reg_dst, branch_type) validated through functional simulation in ModelSim. The design included key components such as the PC register, instruction/data caches, and sign-extension unit, all coordinated by the control unit's opcode decoding logic. The code was board wrapped to 4 bit output to account for the hardware limits of the Nexys Board. The code was simulated in ModelSim then synthesized and downloaded to a Nexys-A7100T FPGA board using the Xilinx Vivado tool. Both tools were used successfully and all the outputs obtained were as desired.

5 Appendix

Table 11: synth_1<runme.log

```
*** Running vivado
    with args -log cpu.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source cpu.tcl


****** Vivado v2018.2 (64-bit)
  **** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
  **** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

source cpu.tcl -notrace
Command: synth_design -top cpu -part xc7a100tcsg324-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: Launching helper process for spawning children vivado processes
INFO: Helper process launched with PID 17177
---------------------------------------------------------------------------------
Starting RTL Elaboration : Time (s): cpu = 00:00:01 ; elapsed = 00:00:02 . Memory (MB): peak = 1401.586 ; gain = 85.805 ; free physical = 10367 ; free
virtual = 22251
---------------------------------------------------------------------------------
INFO: [Synth 8-638] synthesizing module 'cpu' [/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/cpu.vhd:15]
INFO: [Synth 8-3491] module 'pc' declared at '/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/pc.vhd:5' bound
to instance 'program_counter' of component 'pc' [/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/cpu.vhd:162]
INFO: [Synth 8-638] synthesizing module 'pc' [/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/pc.vhd:14]
INFO: [Synth 8-256] done synthesizing module 'pc' (1#1)
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/pc.vhd:14]
INFO: [Synth 8-3491] module 'i_cache' declared at
'/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/i_cache.vhd:4' bound to instance 'instructions' of component
'i_cache' [/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/cpu.vhd:167]
INFO: [Synth 8-638] synthesizing module 'i_cache'
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/i_cache.vhd:11]
INFO: [Synth 8-256] done synthesizing module 'i_cache' (2#1)
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/i_cache.vhd:11]
INFO: [Synth 8-3491] module 'regfile' declared at '/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/regfile.vhd:8'
bound to instance 'registers_f' of component 'regfile'
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/cpu.vhd:170]
INFO: [Synth 8-638] synthesizing module 'regfile'
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/regfile.vhd:21]
WARNING: [Synth 8-614] signal 'write' is read in the process but is not in the sensitivity list
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/regfile.vhd:27]
INFO: [Synth 8-256] done synthesizing module 'regfile' (3#1)
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/regfile.vhd:21]
INFO: [Synth 8-3491] module 'alu' declared at '/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/alu.vhd:5' bound
to instance 'alu_comp' of component 'alu' [/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/cpu.vhd:180]
INFO: [Synth 8-638] synthesizing module 'alu' [/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/alu.vhd:25]
WARNING: [Synth 8-614] signal 'x' is read in the process but is not in the sensitivity list
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/alu.vhd:79]
WARNING: [Synth 8-614] signal 'y' is read in the process but is not in the sensitivity list
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/alu.vhd:79]
INFO: [Synth 8-256] done synthesizing module 'alu' (4#1)
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/alu.vhd:25]
INFO: [Synth 8-3491] module 'd_cache' declared at
'/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/d_cache.vhd:5' bound to instance 'datacache' of component
'd_cache' [/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/cpu.vhd:189]
INFO: [Synth 8-638] synthesizing module 'd_cache'
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/d_cache.vhd:16]
INFO: [Synth 8-256] done synthesizing module 'd_cache' (5#1)
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/d_cache.vhd:16]
INFO: [Synth 8-3491] module 'sign_extender' declared at
'/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/sign_extender.vhd:5' bound to instance 'sign' of component
'sign_extender' [/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/cpu.vhd:196]
INFO: [Synth 8-638] synthesizing module 'sign_extender'
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/sign_extender.vhd:13]
INFO: [Synth 8-226] default block is never used
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/sign_extender.vhd:17]
INFO: [Synth 8-256] done synthesizing module 'sign_extender' (6#1)
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/sign_extender.vhd:13]
INFO: [Synth 8-3491] module 'next_address' declared at
'/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/next_address.vhd:6' bound to instance 'next_pc' of component
'next_address' [/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/cpu.vhd:200]
INFO: [Synth 8-638] synthesizing module 'next_address'
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/next_address.vhd:22]
```

```
INFO: [Synth 8-256] done synthesizing module 'next_address' (7#1)
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/next_address.vhd:22]
INFO: [Synth 8-3491] module 'control_unit' declared at
'/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/control_unit.vhd:4' bound to instance 'controller' of component
'control_unit' [/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/cpu.vhd:208]
INFO: [Synth 8-638] synthesizing module 'control_unit'
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/control_unit.vhd:21]
INFO: [Synth 8-256] done synthesizing module 'control_unit' (8#1)
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/control_unit.vhd:21]
INFO: [Synth 8-256] done synthesizing module 'cpu' (9#1)
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/cpu.vhd:15]
---------------------------------------------------------------------------------
Finished RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1447.227 ; gain = 131.445 ; free physical = 10372 ; free
virtual = 22257
---------------------------------------------------------------------------------

Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
---------------------------------------------------------------------------------
Start Handling Custom Attributes
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1447.227 ; gain = 131.445 ; free physical =
10377 ; free virtual = 22261
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1447.227 ; gain = 131.445 ; free physical =
10377 ; free virtual = 22261
---------------------------------------------------------------------------------
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints
Initializing timing engine
Parsing XDC File [/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/constrs_1/imports/LAB4/lab4.xdc]
Finished Parsing XDC File [/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/constrs_1/imports/LAB4/lab4.xdc]
INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/constrs_1/imports/LAB4/lab4.xdc]. These constraints will be ignored for synthesis but will
be used in implementation. Impacted constraints are listed in the file [.Xil/cpu_propImpl.xdc].
Resolution: To avoid this warning, move constraints listed in [.Xil/cpu_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the
used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 1842.980 ; gain = 0.000 ; free physical = 10097 ;
free virtual = 21982
---------------------------------------------------------------------------------
Finished Constraint Validation : Time (s): cpu = 00:00:10 ; elapsed = 00:00:38 . Memory (MB): peak = 1842.980 ; gain = 527.199 ; free physical = 10180 ;
free virtual = 22065
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Loading Part and Timing Information
---------------------------------------------------------------------------------
Loading part: xc7a100tcsg324-1
---------------------------------------------------------------------------------
Finished Loading Part and Timing Information : Time (s): cpu = 00:00:10 ; elapsed = 00:00:38 . Memory (MB): peak = 1842.980 ; gain = 527.199 ; free
physical = 10180 ; free virtual = 22065
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Applying 'set_property' XDC Constraints
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:10 ; elapsed = 00:00:38 . Memory (MB): peak = 1842.980 ; gain = 527.199 ; free
physical = 10182 ; free virtual = 22066
---------------------------------------------------------------------------------
INFO: [Synth 8-5546] ROM "instruction_out" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[0]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[1]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[2]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[3]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[4]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[5]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[6]" won't be mapped to RAM because it is too sparse
```

```
INFO: [Synth 8-5546] ROM "register_array_reg[7]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[8]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[9]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[10]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[11]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[12]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[13]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[14]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[15]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[16]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[17]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[18]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[19]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[20]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[21]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[22]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[23]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[24]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[25]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[26]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[27]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[28]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[29]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[30]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "register_array_reg[31]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the
operator [/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/alu.vhd:32]
INFO: [Synth 8-5545] ROM "zero" won't be mapped to RAM because address size (32) is larger than maximum supported(25)
INFO: [Synth 8-5546] ROM "reg_array_reg[0]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[1]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[2]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[3]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[4]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[5]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[6]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[7]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[8]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[9]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[10]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[11]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[12]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[13]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[14]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[15]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[16]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[17]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[18]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[19]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[20]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[21]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[22]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[23]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[24]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[25]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[26]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[27]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[28]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[29]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[30]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_array_reg[31]" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_write" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5546] ROM "reg_write" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5587] ROM size for "add_sub" is below threshold of ROM address width. It will be mapped to LUTs
INFO: [Synth 8-5546] ROM "logic_func" won't be mapped to RAM because it is too sparse
INFO: [Synth 8-5587] ROM size for "func" is below threshold of ROM address width. It will be mapped to LUTs
INFO: [Synth 8-5546] ROM "pc_sel" won't be mapped to RAM because it is too sparse
WARNING: [Synth 8-327] inferring latch for variable 'reg_write_reg'
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/control_unit.vhd:32]
WARNING: [Synth 8-327] inferring latch for variable 'reg_dst_reg'
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/control_unit.vhd:33]
WARNING: [Synth 8-327] inferring latch for variable 'reg_in_src_reg'
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/control_unit.vhd:34]
WARNING: [Synth 8-327] inferring latch for variable 'alu_src_reg'
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/control_unit.vhd:35]
WARNING: [Synth 8-327] inferring latch for variable 'add_sub_reg'
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/control_unit.vhd:36]
WARNING: [Synth 8-327] inferring latch for variable 'logic_func_reg'
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/control_unit.vhd:38]
```

```
WARNING: [Synth 8-327] inferring latch for variable 'func_reg'
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/control_unit.vhd:39]
WARNING: [Synth 8-327] inferring latch for variable 'data_write_reg'
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/control_unit.vhd:37]
WARNING: [Synth 8-327] inferring latch for variable 'branch_type_reg'
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/control_unit.vhd:40]
WARNING: [Synth 8-327] inferring latch for variable 'pc_sel_reg'
[/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/sources_1/imports/LAB4/control_unit.vhd:41]
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:10 ; elapsed = 00:00:39 . Memory (MB): peak = 1842.980 ; gain = 527.199 ; free physical =
10176 ; free virtual = 22061
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start RTL Component Statistics
---------------------------------------------------------------------------------
Detailed RTL Component Info :
+---Adders :
                3 Input     32 Bit       Adders := 2
+---XORs :
                2 Input     32 Bit         XORs := 1
+---Registers :
                          32 Bit    Registers := 65
+---Muxes :
                2 Input     32 Bit       Muxes := 4
                4 Input     32 Bit       Muxes := 4
                3 Input     32 Bit       Muxes := 1
                2 Input      5 Bit       Muxes := 1
               14 Input      3 Bit       Muxes := 1
               14 Input      2 Bit       Muxes := 4
                9 Input      2 Bit       Muxes := 3
                5 Input      2 Bit       Muxes := 1
                4 Input      2 Bit       Muxes := 1
                2 Input      1 Bit       Muxes := 66
                9 Input      1 Bit       Muxes := 2
               14 Input      1 Bit       Muxes := 4
                4 Input      1 Bit       Muxes := 1
---------------------------------------------------------------------------------
Finished RTL Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
Hierarchical RTL Component report
Module cpu
Detailed RTL Component Info :
+---Muxes :
                2 Input     32 Bit       Muxes := 2
                2 Input      5 Bit       Muxes := 1
Module pc
Detailed RTL Component Info :
+---Registers :
                          32 Bit    Registers := 1
Module i_cache
Detailed RTL Component Info :
+---Muxes :
                2 Input     32 Bit       Muxes := 1
Module regfile
Detailed RTL Component Info :
+---Registers :
                          32 Bit    Registers := 32
+---Muxes :
                2 Input      1 Bit       Muxes := 32
Module alu
Detailed RTL Component Info :
+---Adders :
                3 Input     32 Bit       Adders := 1
+---XORs :
                2 Input     32 Bit         XORs := 1
+---Muxes :
                4 Input     32 Bit       Muxes := 2
                2 Input     32 Bit       Muxes := 1
                2 Input      1 Bit       Muxes := 2
Module d_cache
```

```
Detailed RTL Component Info :
+---Registers :
                32 Bit    Registers := 32
+---Muxes :
                 2 Input      1 Bit       Muxes := 32
Module sign_extender
Detailed RTL Component Info :
+---Muxes :
                 3 Input     32 Bit       Muxes := 1
Module next_address
Detailed RTL Component Info :
+---Adders :
                 3 Input     32 Bit       Adders := 1
+---Muxes :
                 4 Input     32 Bit       Muxes := 2
Module control_unit
Detailed RTL Component Info :
+---Muxes :
                14 Input      3 Bit       Muxes := 1
                14 Input      2 Bit       Muxes := 4
                 9 Input      2 Bit       Muxes := 3
                 5 Input      2 Bit       Muxes := 1
                 4 Input      2 Bit       Muxes := 1
                 9 Input      1 Bit       Muxes := 2
                14 Input      1 Bit       Muxes := 4
                 4 Input      1 Bit       Muxes := 1
---------------------------------------------------------------------------------
Finished RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Part Resource Summary
---------------------------------------------------------------------------------
Part Resources:
DSPs: 240 (col length:80)
BRAMs: 270 (col length: RAMB18 80 RAMB36 40)
---------------------------------------------------------------------------------
Finished Part Resource Summary
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Cross Boundary and Area Optimization
---------------------------------------------------------------------------------
Warning: Parallel synthesis criteria is not met
INFO: [Synth 8-5545] ROM "zero" won't be mapped to RAM because address size (32) is larger than maximum supported(25)
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][4]' (FDCE) to 'registers_f/register_array_reg[11][4]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][4]' (FDCE) to 'registers_f/register_array_reg[11][4]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][4] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][5]' (FDCE) to 'registers_f/register_array_reg[11][5]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][5]' (FDCE) to 'registers_f/register_array_reg[11][5]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][5] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][6]' (FDCE) to 'registers_f/register_array_reg[11][6]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][6]' (FDCE) to 'registers_f/register_array_reg[11][6]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][6] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][7]' (FDCE) to 'registers_f/register_array_reg[11][7]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][7]' (FDCE) to 'registers_f/register_array_reg[11][7]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][7] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][8]' (FDCE) to 'registers_f/register_array_reg[11][8]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][8]' (FDCE) to 'registers_f/register_array_reg[11][8]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][8] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][9]' (FDCE) to 'registers_f/register_array_reg[11][9]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][9]' (FDCE) to 'registers_f/register_array_reg[11][9]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][9] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][10]' (FDCE) to 'registers_f/register_array_reg[11][10]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][10]' (FDCE) to 'registers_f/register_array_reg[11][10]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][10] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][11]' (FDCE) to 'registers_f/register_array_reg[11][11]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][11]' (FDCE) to 'registers_f/register_array_reg[11][11]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][11] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][12]' (FDCE) to 'registers_f/register_array_reg[11][12]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][12]' (FDCE) to 'registers_f/register_array_reg[11][12]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][12] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][13]' (FDCE) to 'registers_f/register_array_reg[11][13]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][13]' (FDCE) to 'registers_f/register_array_reg[11][13]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][13] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][14]' (FDCE) to 'registers_f/register_array_reg[11][14]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][14]' (FDCE) to 'registers_f/register_array_reg[11][14]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][14] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][15]' (FDCE) to 'registers_f/register_array_reg[11][15]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][15]' (FDCE) to 'registers_f/register_array_reg[11][15]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][15] )
```

```
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][16]' (FDCE) to 'registers_f/register_array_reg[11][16]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][16]' (FDCE) to 'registers_f/register_array_reg[11][16]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][16] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][17]' (FDCE) to 'registers_f/register_array_reg[11][17]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][17]' (FDCE) to 'registers_f/register_array_reg[11][17]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][17] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][18]' (FDCE) to 'registers_f/register_array_reg[11][18]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][18]' (FDCE) to 'registers_f/register_array_reg[11][18]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][18] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][19]' (FDCE) to 'registers_f/register_array_reg[11][19]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][19]' (FDCE) to 'registers_f/register_array_reg[11][19]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][19] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][20]' (FDCE) to 'registers_f/register_array_reg[11][20]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][20]' (FDCE) to 'registers_f/register_array_reg[11][20]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][20] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][21]' (FDCE) to 'registers_f/register_array_reg[11][21]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][21]' (FDCE) to 'registers_f/register_array_reg[11][21]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][21] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][22]' (FDCE) to 'registers_f/register_array_reg[11][22]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][22]' (FDCE) to 'registers_f/register_array_reg[11][22]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][22] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][23]' (FDCE) to 'registers_f/register_array_reg[11][23]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][23]' (FDCE) to 'registers_f/register_array_reg[11][23]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][23] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][24]' (FDCE) to 'registers_f/register_array_reg[11][24]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][24]' (FDCE) to 'registers_f/register_array_reg[11][24]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][24] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][25]' (FDCE) to 'registers_f/register_array_reg[11][25]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][25]' (FDCE) to 'registers_f/register_array_reg[11][25]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][25] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][26]' (FDCE) to 'registers_f/register_array_reg[11][26]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][26]' (FDCE) to 'registers_f/register_array_reg[11][26]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][26] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][27]' (FDCE) to 'registers_f/register_array_reg[11][27]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][27]' (FDCE) to 'registers_f/register_array_reg[11][27]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][27] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][28]' (FDCE) to 'registers_f/register_array_reg[11][28]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][28]' (FDCE) to 'registers_f/register_array_reg[11][28]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][28] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][29]' (FDCE) to 'registers_f/register_array_reg[11][29]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][29]' (FDCE) to 'registers_f/register_array_reg[11][29]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][29] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][30]' (FDCE) to 'registers_f/register_array_reg[11][30]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][30]' (FDCE) to 'registers_f/register_array_reg[11][30]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][30] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][31]' (FDCE) to 'registers_f/register_array_reg[11][31]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][31]' (FDCE) to 'registers_f/register_array_reg[11][31]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][31] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][0]' (FDCE) to 'registers_f/register_array_reg[11][0]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][0]' (FDCE) to 'registers_f/register_array_reg[11][0]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][0] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][1]' (FDCE) to 'registers_f/register_array_reg[11][1]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][1]' (FDCE) to 'registers_f/register_array_reg[11][1]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][1] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][2]' (FDCE) to 'registers_f/register_array_reg[11][2]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][2]' (FDCE) to 'registers_f/register_array_reg[11][2]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][2] )
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[14][3]' (FDCE) to 'registers_f/register_array_reg[11][3]'
INFO: [Synth 8-3886] merging instance 'registers_f/register_array_reg[13][3]' (FDCE) to 'registers_f/register_array_reg[11][3]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\registers_f/register_array_reg[11][3] )
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][31]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][30]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][29]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][28]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][27]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][26]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][25]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][24]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][23]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][22]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][21]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][20]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][19]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][18]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][17]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][16]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][15]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][14]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][13]) is unused and will be removed from module cpu.
```

WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][12]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][11]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][10]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][9]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][8]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][7]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][6]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][5]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][4]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][3]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][2]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][1]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[8][0]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][31]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][30]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][29]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][28]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][27]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][26]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][25]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][24]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][23]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][22]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][21]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][20]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][19]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][18]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][17]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][16]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][15]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][14]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][13]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][12]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][11]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][10]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][9]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][8]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][7]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][6]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][5]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][4]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][3]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][2]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][1]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[9][0]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][31]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][30]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][29]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][28]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][27]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][26]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][25]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][24]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][23]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][22]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][21]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][20]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][19]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][18]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][17]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][16]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][15]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][14]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][13]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][12]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][11]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][10]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][9]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][8]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][7]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][6]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][5]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][4]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][3]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][2]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][1]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[10][0]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[12][31]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[12][30]) is unused and will be removed from module cpu.

```
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[12][29]) is unused and will be removed from module cpu.
WARNING: [Synth 8-3332] Sequential element (registers_f/register_array_reg[12][28]) is unused and will be removed from module cpu.
INFO: [Common 17-14] Message 'Synth 8-3332' appears 100 times and further instances of the messages will be disabled. Use the Tcl command set_msg_config to change the current settings.
---------------------------------------------------------------------------------
Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:19 ; elapsed = 00:00:48 . Memory (MB): peak = 1842.980 ; gain = 527.199 ; free physical = 10138 ; free virtual = 22027
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start Applying XDC Timing Constraints
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:24 ; elapsed = 00:00:59 . Memory (MB): peak = 1842.980 ; gain = 527.199 ; free physical = 10024 ; free virtual = 21912
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Timing Optimization
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Timing Optimization : Time (s): cpu = 00:00:24 ; elapsed = 00:00:59 . Memory (MB): peak = 1842.980 ; gain = 527.199 ; free physical = 10023 ; free virtual = 21911
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start Technology Mapping
---------------------------------------------------------------------------------
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\controller/branch_type_reg[1] )
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\controller/pc_sel_reg[1] )
---------------------------------------------------------------------------------
Finished Technology Mapping : Time (s): cpu = 00:00:25 ; elapsed = 00:01:00 . Memory (MB): peak = 1842.980 ; gain = 527.199 ; free physical = 10021 ; free virtual = 21909
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start IO Insertion
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Flattening Before IO Insertion
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Flattening Before IO Insertion
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Final Netlist Cleanup
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Final Netlist Cleanup
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished IO Insertion : Time (s): cpu = 00:00:25 ; elapsed = 00:01:00 . Memory (MB): peak = 1842.980 ; gain = 527.199 ; free physical = 10021 ; free virtual = 21909
---------------------------------------------------------------------------------

Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
---------------------------------------------------------------------------------
Start Renaming Generated Instances
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
```

```
Finished Renaming Generated Instances : Time (s): cpu = 00:00:25 ; elapsed = 00:01:00 . Memory (MB): peak = 1842.980 ; gain = 527.199 ; free physical = 10021 ; free virtual = 21909
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start Rebuilding User Hierarchy
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:25 ; elapsed = 00:01:00 . Memory (MB): peak = 1842.980 ; gain = 527.199 ; free physical = 10021 ; free virtual = 21909
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Renaming Generated Ports
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Renaming Generated Ports : Time (s): cpu = 00:00:25 ; elapsed = 00:01:00 . Memory (MB): peak = 1842.980 ; gain = 527.199 ; free physical = 10021 ; free virtual = 21909
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Handling Custom Attributes
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:25 ; elapsed = 00:01:00 . Memory (MB): peak = 1842.980 ; gain = 527.199 ; free physical = 10021 ; free virtual = 21909
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Renaming Generated Nets
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Renaming Generated Nets : Time (s): cpu = 00:00:25 ; elapsed = 00:01:00 . Memory (MB): peak = 1842.980 ; gain = 527.199 ; free physical = 10021 ; free virtual = 21909
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-------+------+
|      |Cell   |Count |
+------+-------+------+
|1     |BUFG   |     1|
|2     |CARRY4 |    13|
|3     |LUT1   |     4|
|4     |LUT3   |    50|
|5     |LUT4   |    13|
|6     |LUT5   |   136|
|7     |LUT6   |   471|
|8     |MUXF7  |   174|
|9     |MUXF8  |    62|
|10    |FDCE   |  1285|
|11    |IBUF   |     2|
|12    |OBUF   |    14|
+------+-------+------+

Report Instance Areas:
+------+-----------------+-------------+------+
|      |Instance         |Module       |Cells |
+------+-----------------+-------------+------+
|1     |top              |             |  2225|
|2     |  alu_comp       |alu          |    17|
|3     |  datacache      |d_cache      |  1472|
|4     |  next_pc        |next_address |     2|
|5     |  program_counter |pc          |   255|
|6     |  registers_f    |regfile      |   462|
+------+-----------------+-------------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:25 ; elapsed = 00:01:00 . Memory (MB): peak = 1842.980 ; gain = 527.199 ; free physical = 10021 ; free virtual = 21909
```

```
---------------------------------------------------------------------------------
Synthesis finished with 0 errors, 0 critical warnings and 755 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:19 ; elapsed = 00:00:29 . Memory (MB): peak = 1842.980 ; gain = 131.445 ; free physical =
10077 ; free virtual = 21965
Synthesis Optimization Complete : Time (s): cpu = 00:00:25 ; elapsed = 00:01:00 . Memory (MB): peak = 1842.980 ; gain = 527.199 ; free physical =
10086 ; free virtual = 21974
INFO: [Project 1-571] Translating synthesized netlist
INFO: [Netlist 29-17] Analyzing 251 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis
212 Infos, 113 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:27 ; elapsed = 00:01:02 . Memory (MB): peak = 1844.984 ; gain = 541.852 ; free physical = 10072 ; free virtual =
21960
WARNING: [Constraints 18-5210] No constraint will be written out.
INFO: [Common 17-1381] The checkpoint '/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.runs/synth_1/cpu.dcp' has been generated.
INFO: [runtcl-4] Executing : report_utilization -file cpu_utilization_synth.rpt -pb cpu_utilization_synth.pb
report_utilization: Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.11 . Memory (MB): peak = 1869.004 ; gain = 0.000 ; free physical = 10072 ; free
virtual = 21961
INFO: [Common 17-206] Exiting Vivado at Tue Apr  1 17:09:57 2025...
```

Table 12: impl_1<runme.log

```
*** Running vivado
    with args -log cpu.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source cpu.tcl -notrace


****** Vivado v2018.2 (64-bit)
  **** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
  **** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

source cpu.tcl -notrace
Command: link_design -top cpu -part xc7a100tcsg324-1
Design is defaulting to srcset: sources_1
Design is defaulting to constrset: constrs_1
INFO: [Netlist 29-17] Analyzing 251 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-479] Netlist was created with Vivado 2018.2
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization
Parsing XDC File [/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/constrs_1/imports/LAB4/lab4.xdc]
Finished Parsing XDC File [/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.srcs/constrs_1/imports/LAB4/lab4.xdc]
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

7 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
link_design completed successfully
link_design: Time (s): cpu = 00:00:07 ; elapsed = 00:00:32 . Memory (MB): peak = 1655.379 ; gain = 347.242 ; free physical = 10188 ; free virtual =
22073
Command: opt_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command opt_design

Starting DRC Task
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Project 1-461] DRC finished with 0 Errors
INFO: [Project 1-462] Please refer to the DRC report (report_drc) for more information.

Time (s): cpu = 00:00:00.94 ; elapsed = 00:00:02 . Memory (MB): peak = 1729.406 ; gain = 74.027 ; free physical = 10182 ; free virtual = 22067

Starting Cache Timing Information Task
INFO: [Timing 38-35] Done setting XDC timing constraints.
Ending Cache Timing Information Task | Checksum: 2132bb8d2

Time (s): cpu = 00:00:10 ; elapsed = 00:00:37 . Memory (MB): peak = 2201.902 ; gain = 472.496 ; free physical = 9744 ; free virtual = 21631

Starting Logic Optimization Task

Phase 1 Retarget
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Opt 31-49] Retargeted 0 cell(s).
Phase 1 Retarget | Checksum: 163e04902

Time (s): cpu = 00:00:00.16 ; elapsed = 00:00:00.07 . Memory (MB): peak = 2201.902 ; gain = 0.000 ; free physical = 9767 ; free virtual = 21653
INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Phase 2 Constant propagation | Checksum: 163e04902

Time (s): cpu = 00:00:00.18 ; elapsed = 00:00:00.08 . Memory (MB): peak = 2201.902 ; gain = 0.000 ; free physical = 9767 ; free virtual = 21653
INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep
Phase 3 Sweep | Checksum: a567f2ab

Time (s): cpu = 00:00:00.20 ; elapsed = 00:00:00.10 . Memory (MB): peak = 2201.902 ; gain = 0.000 ; free physical = 9767 ; free virtual = 21653
INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization
Phase 4 BUFG optimization | Checksum: a567f2ab

Time (s): cpu = 00:00:00.22 ; elapsed = 00:00:00.12 . Memory (MB): peak = 2201.902 ; gain = 0.000 ; free physical = 9767 ; free virtual = 21653
INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.

Phase 5 Shift Register Optimization
```

```
Phase 5 Shift Register Optimization | Checksum: 12ab9b440

Time (s): cpu = 00:00:00.24 ; elapsed = 00:00:00.14 . Memory (MB): peak = 2201.902 ; gain = 0.000 ; free physical = 9767 ; free virtual = 21653
INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist
Phase 6 Post Processing Netlist | Checksum: 12ab9b440

Time (s): cpu = 00:00:00.24 ; elapsed = 00:00:00.15 . Memory (MB): peak = 2201.902 ; gain = 0.000 ; free physical = 9767 ; free virtual = 21653
INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Starting Connectivity Check Task

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00 . Memory (MB): peak = 2201.902 ; gain = 0.000 ; free physical = 9767 ; free virtual = 21653
Ending Logic Optimization Task | Checksum: 12ab9b440

Time (s): cpu = 00:00:00.25 ; elapsed = 00:00:00.15 . Memory (MB): peak = 2201.902 ; gain = 0.000 ; free physical = 9767 ; free virtual = 21653

Starting Power Optimization Task
INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
Ending Power Optimization Task | Checksum: 12ab9b440

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2201.906 ; gain = 0.004 ; free physical = 9767 ; free virtual = 21653

Starting Final Cleanup Task
Ending Final Cleanup Task | Checksum: 12ab9b440

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2201.906 ; gain = 0.000 ; free physical = 9767 ; free virtual = 21653
INFO: [Common 17-83] Releasing license: Implementation
23 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
opt_design completed successfully
opt_design: Time (s): cpu = 00:00:11 ; elapsed = 00:00:39 . Memory (MB): peak = 2201.906 ; gain = 546.527 ; free physical = 9767 ; free virtual = 21653
INFO: [Timing 38-480] Writing timing data to binary archive.
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:00.16 ; elapsed = 00:00:00.11 . Memory (MB): peak = 2233.922 ; gain = 0.004 ; free physical = 9762 ; free virtual = 21649
INFO: [Common 17-1381] The checkpoint '/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.runs/impl_1/cpu_opt.dcp' has been generated.
INFO: [runtcl-4] Executing : report_drc -file cpu_drc_opted.rpt -pb cpu_drc_opted.pb -rpx cpu_drc_opted.rpx
Command: report_drc -file cpu_drc_opted.rpt -pb cpu_drc_opted.pb -rpx cpu_drc_opted.rpx
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/data/ip'.
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Coretcl 2-168] The results of DRC are in file /nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.runs/impl_1/cpu_drc_opted.rpt.
report_drc completed successfully
report_drc: Time (s): cpu = 00:00:03 ; elapsed = 00:00:05 . Memory (MB): peak = 2313.961 ; gain = 80.031 ; free physical = 9720 ; free virtual = 21607
Command: place_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.
Running DRC as a precondition to command place_design
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.

Starting Placer Task
INFO: [Place 30-611] Multithreading enabled for place_design using a maximum of 8 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2313.961 ; gain = 0.000 ; free physical = 9716 ; free virtual = 21602
Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 115e48f89

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2313.961 ; gain = 0.000 ; free physical = 9716 ; free virtual = 21602
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2313.961 ; gain = 0.000 ; free physical = 9716 ; free virtual = 21602

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device
INFO: [Timing 38-35] Done setting XDC timing constraints.
WARNING: [Place 30-574] Poor placement for routing between an IO pin and BUFG. This is normally an ERROR but the CLOCK_DEDICATED_ROUTE constraint is set to FALSE allowing your design to continue. The use of this override is highly discouraged as it may lead to very poor timing results. It is recommended that this error condition be corrected in the design.
```

clk_IBUF_inst (IBUF.O) is locked to IOB_X0Y82
clk_IBUF_BUFG_inst (BUFG.I) is provisionally placed by clockplacer on BUFGCTRL_X0Y0
Resolution: Poor placement of an IO pin and a BUFG has resulted in the router using a non-dedicated path between the two. There are several things that could trigger this DRC, each of which can cause unpredictable clock insertion delays that result in poor timing. This DRC could be caused by any of the following: (a) a clock port was placed on a pin that is not a CCIO-pin (b)the BUFG has not been placed in the same half of the device or SLR as the CCIO-pin (c) a single ended clock has been placed on the N-Side of a differential pair CCIO-pin.
Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: 102612141

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.61 . Memory (MB): peak = 2313.961 ; gain = 0.000 ; free physical = 9714 ; free virtual = 21600

Phase 1.3 Build Placer Netlist Model
Phase 1.3 Build Placer Netlist Model | Checksum: 15243675a

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.65 . Memory (MB): peak = 2313.961 ; gain = 0.000 ; free physical = 9714 ; free virtual = 21600

Phase 1.4 Constrain Clocks/Macros
Phase 1.4 Constrain Clocks/Macros | Checksum: 15243675a

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.65 . Memory (MB): peak = 2313.961 ; gain = 0.000 ; free physical = 9714 ; free virtual = 21600
Phase 1 Placer Initialization | Checksum: 15243675a

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.65 . Memory (MB): peak = 2313.961 ; gain = 0.000 ; free physical = 9714 ; free virtual = 21600

Phase 2 Global Placement

Phase 2.1 Floorplanning
Phase 2.1 Floorplanning | Checksum: 15243675a

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.67 . Memory (MB): peak = 2313.961 ; gain = 0.000 ; free physical = 9712 ; free virtual = 21598
WARNING: [Place 46-29] place_design is not in timing mode. Skip physical synthesis in placer
Phase 2 Global Placement | Checksum: 157118450

Time (s): cpu = 00:00:05 ; elapsed = 00:00:01 . Memory (MB): peak = 2368.980 ; gain = 55.020 ; free physical = 9689 ; free virtual = 21576

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros
Phase 3.1 Commit Multi Column Macros | Checksum: 157118450

Time (s): cpu = 00:00:05 ; elapsed = 00:00:01 . Memory (MB): peak = 2368.980 ; gain = 55.020 ; free physical = 9689 ; free virtual = 21576

Phase 3.2 Commit Most Macros & LUTRAMs
Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 197fd3be3

Time (s): cpu = 00:00:05 ; elapsed = 00:00:01 . Memory (MB): peak = 2368.980 ; gain = 55.020 ; free physical = 9689 ; free virtual = 21576

Phase 3.3 Area Swap Optimization
Phase 3.3 Area Swap Optimization | Checksum: 1e7224a71

Time (s): cpu = 00:00:05 ; elapsed = 00:00:01 . Memory (MB): peak = 2368.980 ; gain = 55.020 ; free physical = 9689 ; free virtual = 21576

Phase 3.4 Pipeline Register Optimization
Phase 3.4 Pipeline Register Optimization | Checksum: 1e7224a71

Time (s): cpu = 00:00:05 ; elapsed = 00:00:01 . Memory (MB): peak = 2368.980 ; gain = 55.020 ; free physical = 9689 ; free virtual = 21576

Phase 3.5 Small Shape Detail Placement
Phase 3.5 Small Shape Detail Placement | Checksum: 1e0409d27

Time (s): cpu = 00:00:06 ; elapsed = 00:00:02 . Memory (MB): peak = 2368.980 ; gain = 55.020 ; free physical = 9685 ; free virtual = 21571

Phase 3.6 Re-assign LUT pins
Phase 3.6 Re-assign LUT pins | Checksum: 1e0409d27

Time (s): cpu = 00:00:06 ; elapsed = 00:00:02 . Memory (MB): peak = 2368.980 ; gain = 55.020 ; free physical = 9685 ; free virtual = 21571

Phase 3.7 Pipeline Register Optimization
Phase 3.7 Pipeline Register Optimization | Checksum: 1e0409d27

Time (s): cpu = 00:00:06 ; elapsed = 00:00:02 . Memory (MB): peak = 2368.980 ; gain = 55.020 ; free physical = 9685 ; free virtual = 21571
Phase 3 Detail Placement | Checksum: 1e0409d27

Time (s): cpu = 00:00:06 ; elapsed = 00:00:02 . Memory (MB): peak = 2368.980 ; gain = 55.020 ; free physical = 9685 ; free virtual = 21571

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization
Phase 4.1 Post Commit Optimization | Checksum: 1e0409d27

Time (s): cpu = 00:00:06 ; elapsed = 00:00:02 . Memory (MB): peak = 2368.980 ; gain = 55.020 ; free physical = 9685 ; free virtual = 21571

Phase 4.2 Post Placement Cleanup
Phase 4.2 Post Placement Cleanup | Checksum: 1e0409d27

Time (s): cpu = 00:00:06 ; elapsed = 00:00:02 . Memory (MB): peak = 2368.980 ; gain = 55.020 ; free physical = 9687 ; free virtual = 21573

Phase 4.3 Placer Reporting
Phase 4.3 Placer Reporting | Checksum: 1e0409d27

Time (s): cpu = 00:00:06 ; elapsed = 00:00:02 . Memory (MB): peak = 2368.980 ; gain = 55.020 ; free physical = 9687 ; free virtual = 21573

Phase 4.4 Final Placement Cleanup
Phase 4.4 Final Placement Cleanup | Checksum: 1618aa475

Time (s): cpu = 00:00:06 ; elapsed = 00:00:02 . Memory (MB): peak = 2368.980 ; gain = 55.020 ; free physical = 9687 ; free virtual = 21573
Phase 4 Post Placement Optimization and Clean-Up | Checksum: 1618aa475

Time (s): cpu = 00:00:06 ; elapsed = 00:00:02 . Memory (MB): peak = 2368.980 ; gain = 55.020 ; free physical = 9687 ; free virtual = 21573
Ending Placer Task | Checksum: 89f5f4dc

Time (s): cpu = 00:00:06 ; elapsed = 00:00:02 . Memory (MB): peak = 2368.980 ; gain = 55.020 ; free physical = 9704 ; free virtual = 21591
INFO: [Common 17-83] Releasing license: Implementation
41 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.
place_design completed successfully
INFO: [Timing 38-480] Writing timing data to binary archive.
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:00.32 ; elapsed = 00:00:00.32 . Memory (MB): peak = 2368.980 ; gain = 0.000 ; free physical = 9702 ; free virtual = 21592
INFO: [Common 17-1381] The checkpoint '/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.runs/impl_1/cpu_placed.dcp' has been generated.
INFO: [runtcl-4] Executing : report_io -file cpu_io_placed.rpt
report_io: Time (s): cpu = 00:00:00.08 ; elapsed = 00:00:00.13 . Memory (MB): peak = 2368.980 ; gain = 0.000 ; free physical = 9697 ; free virtual = 21584
INFO: [runtcl-4] Executing : report_utilization -file cpu_utilization_placed.rpt -pb cpu_utilization_placed.pb
report_utilization: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.07 . Memory (MB): peak = 2368.980 ; gain = 0.000 ; free physical = 9704 ; free virtual = 21591
INFO: [runtcl-4] Executing : report_control_sets -verbose -file cpu_control_sets_placed.rpt
report_control_sets: Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2368.980 ; gain = 0.000 ; free physical = 9705 ; free virtual = 21592
Command: route_design
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command route_design
INFO: [DRC 23-27] Running DRC with 8 threads
WARNING: [DRC PLCK-12] Clock Placer Checks: Poor placement for routing between an IO pin and BUFG.
Resolution: Poor placement of an IO pin and a BUFG has resulted in the router using a non-dedicated path between the two. There are several things that could trigger this DRC, each of which can cause unpredictable clock insertion delays that result in poor timing. This DRC could be caused by any of the following: (a) a clock port was placed on a pin that is not a CCIO-pin (b)the BUFG has not been placed in the same half of the device or SLR as the CCIO-pin (c) a single ended clock has been placed on the N-Side of a differential pair CCIO-pin.
 This is normally an ERROR but the CLOCK_DEDICATED_ROUTE constraint is set to FALSE allowing your design to continue. The use of this override is highly discouraged as it may lead to very poor timing results. It is recommended that this error condition be corrected in the design.

	clk_IBUF_inst (IBUF.O) is locked to IOB_X0Y82
	clk_IBUF_BUFG_inst (BUFG.I) is provisionally placed by clockplacer on BUFGCTRL_X0Y0
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors, 1 Warnings
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.

Starting Routing Task
INFO: [Route 35-254] Multithreading enabled for route_design using a maximum of 8 CPUs
Checksum: PlaceDB: 24de75b4 ConstDB: 0 ShapeSum: 65177f28 RouteDB: 0

Phase 1 Build RT Design
Phase 1 Build RT Design | Checksum: de687e44

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2410.980 ; gain = 42.000 ; free physical = 9551 ; free virtual = 21438
Post Restoration Checksum: NetGraph: 278aeb41 NumContArr: b6dd9303 Constraints: 0 Timing: 0

Phase 2 Router Initialization
INFO: [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.

Phase 2.1 Fix Topology Constraints
Phase 2.1 Fix Topology Constraints | Checksum: de687e44

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2417.969 ; gain = 48.988 ; free physical = 9520 ; free virtual = 21407

```
Phase 2.2 Pre Route Cleanup
Phase 2.2 Pre Route Cleanup | Checksum: de687e44

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2417.969 ; gain = 48.988 ; free physical = 9520 ; free virtual = 21407
 Number of Nodes with overlaps = 0
Phase 2 Router Initialization | Checksum: d8323cba

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2428.234 ; gain = 59.254 ; free physical = 9510 ; free virtual = 21397

Phase 3 Initial Routing
Phase 3 Initial Routing | Checksum: e5626c39

Time (s): cpu = 00:00:18 ; elapsed = 00:00:13 . Memory (MB): peak = 2431.234 ; gain = 62.254 ; free physical = 9512 ; free virtual = 21399

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0
 Number of Nodes with overlaps = 202
 Number of Nodes with overlaps = 1
 Number of Nodes with overlaps = 0
Phase 4.1 Global Iteration 0 | Checksum: ee1b560e

Time (s): cpu = 00:00:20 ; elapsed = 00:00:14 . Memory (MB): peak = 2431.234 ; gain = 62.254 ; free physical = 9510 ; free virtual = 21398
Phase 4 Rip-up And Reroute | Checksum: ee1b560e

Time (s): cpu = 00:00:20 ; elapsed = 00:00:14 . Memory (MB): peak = 2431.234 ; gain = 62.254 ; free physical = 9510 ; free virtual = 21398

Phase 5 Delay and Skew Optimization
Phase 5 Delay and Skew Optimization | Checksum: ee1b560e

Time (s): cpu = 00:00:20 ; elapsed = 00:00:14 . Memory (MB): peak = 2431.234 ; gain = 62.254 ; free physical = 9510 ; free virtual = 21398

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter
Phase 6.1 Hold Fix Iter | Checksum: ee1b560e

Time (s): cpu = 00:00:20 ; elapsed = 00:00:14 . Memory (MB): peak = 2431.234 ; gain = 62.254 ; free physical = 9510 ; free virtual = 21398
Phase 6 Post Hold Fix | Checksum: ee1b560e

Time (s): cpu = 00:00:20 ; elapsed = 00:00:14 . Memory (MB): peak = 2431.234 ; gain = 62.254 ; free physical = 9510 ; free virtual = 21398

Phase 7 Route finalize

Router Utilization Summary
  Global Vertical Routing Utilization    = 0.298298 %
  Global Horizontal Routing Utilization  = 0.358554 %
  Routable Net Status*
  *Does not include unroutable nets such as driverless and loadless.
  Run report_route_status for detailed report.
  Number of Failed Nets               = 0
  Number of Unrouted Nets             = 0
  Number of Partially Routed Nets     = 0
  Number of Node Overlaps             = 0

Congestion Report
North Dir 1x1 Area, Max Cong = 41.4414%, No Congested Regions.
South Dir 1x1 Area, Max Cong = 38.7387%, No Congested Regions.
East Dir 1x1 Area, Max Cong = 35.2941%, No Congested Regions.
West Dir 1x1 Area, Max Cong = 35.2941%, No Congested Regions.

---------------------------------
Reporting congestion hotspots
---------------------------------
Direction: North
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: South
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: East
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: West
----------------
```

```
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: ee1b560e

Time (s): cpu = 00:00:20 ; elapsed = 00:00:14 . Memory (MB): peak = 2431.234 ; gain = 62.254 ; free physical = 9510 ; free virtual = 21398

Phase 8 Verifying routed nets

 Verification completed successfully
Phase 8 Verifying routed nets | Checksum: ee1b560e

Time (s): cpu = 00:00:20 ; elapsed = 00:00:14 . Memory (MB): peak = 2431.234 ; gain = 62.254 ; free physical = 9510 ; free virtual = 21397

Phase 9 Depositing Routes
Phase 9 Depositing Routes | Checksum: 95d5ab1f

Time (s): cpu = 00:00:20 ; elapsed = 00:00:14 . Memory (MB): peak = 2431.234 ; gain = 62.254 ; free physical = 9510 ; free virtual = 21397
INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:20 ; elapsed = 00:00:14 . Memory (MB): peak = 2431.234 ; gain = 62.254 ; free physical = 9545 ; free virtual = 21432

Routing Is Done.
INFO: [Common 17-83] Releasing license: Implementation
54 Infos, 3 Warnings, 0 Critical Warnings and 0 Errors encountered.
route_design completed successfully
route_design: Time (s): cpu = 00:00:21 ; elapsed = 00:00:16 . Memory (MB): peak = 2431.238 ; gain = 62.258 ; free physical = 9545 ; free virtual = 21432
INFO: [Timing 38-480] Writing timing data to binary archive.
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:00.61 ; elapsed = 00:00:00.44 . Memory (MB): peak = 2431.238 ; gain = 0.000 ; free physical = 9540 ; free
virtual = 21431
INFO: [Common 17-1381] The checkpoint '/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.runs/impl_1/cpu_routed.dcp' has been generated.
INFO: [runtcl-4] Executing : report_drc -file cpu_drc_routed.rpt -pb cpu_drc_routed.pb -rpx cpu_drc_routed.rpx
Command: report_drc -file cpu_drc_routed.rpt -pb cpu_drc_routed.pb -rpx cpu_drc_routed.rpx
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Coretcl 2-168] The results of DRC are in file /nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.runs/impl_1/cpu_drc_routed.rpt.
report_drc completed successfully
INFO: [runtcl-4] Executing : report_methodology -file cpu_methodology_drc_routed.rpt -pb cpu_methodology_drc_routed.pb -rpx
cpu_methodology_drc_routed.rpx
Command: report_methodology -file cpu_methodology_drc_routed.rpt -pb cpu_methodology_drc_routed.pb -rpx cpu_methodology_drc_routed.rpx
INFO: [Timing 38-35] Done setting XDC timing constraints.
INFO: [Timing 38-35] Done setting XDC timing constraints.
INFO: [DRC 23-133] Running Methodology with 8 threads
INFO: [Coretcl 2-1520] The results of Report Methodology are in file
/nfs/home/m/mi_drive/COEN316/LAB4/project_2/project_2.runs/impl_1/cpu_methodology_drc_routed.rpt.
report_methodology completed successfully
INFO: [runtcl-4] Executing : report_power -file cpu_power_routed.rpt -pb cpu_power_summary_routed.pb -rpx cpu_power_routed.rpx
Command: report_power -file cpu_power_routed.rpt -pb cpu_power_summary_routed.pb -rpx cpu_power_routed.rpx
WARNING: [Power 33-232] No user defined clocks were found in the design!
Resolution: Please specify clocks using create_clock/create_generated_clock for sequential elements. For pure combinatorial circuits, please specify a
virtual clock, otherwise the vectorless estimation might be inaccurate
INFO: [Timing 38-35] Done setting XDC timing constraints.
Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation
66 Infos, 4 Warnings, 0 Critical Warnings and 0 Errors encountered.
report_power completed successfully
INFO: [runtcl-4] Executing : report_route_status -file cpu_route_status.rpt -pb cpu_route_status.pb
INFO: [runtcl-4] Executing : report_timing_summary -max_paths 10 -file cpu_timing_summary_routed.rpt -pb cpu_timing_summary_routed.pb -rpx
cpu_timing_summary_routed.rpx -warn_on_violation
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min_max, Timing Stage: Requireds.
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs
WARNING: [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.
INFO: [runtcl-4] Executing : report_incremental_reuse -file cpu_incremental_reuse_routed.rpt
INFO: [Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.
INFO: [runtcl-4] Executing : report_clock_utilization -file cpu_clock_utilization_routed.rpt
INFO: [runtcl-4] Executing : report_bus_skew -warn_on_violation -file cpu_bus_skew_routed.rpt -pb cpu_bus_skew_routed.pb -rpx
cpu_bus_skew_routed.rpx
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min_max, Timing Stage: Requireds.
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs
INFO: [Common 17-206] Exiting Vivado at Tue Apr  1 17:12:02 2025...

*** Running vivado
    with args -log cpu.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source cpu.tcl -notrace
```

```
****** Vivado v2018.2 (64-bit)
  **** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
  **** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

source cpu.tcl -notrace
Command: open_checkpoint cpu_routed.dcp

Starting open_checkpoint Task

Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.13 . Memory (MB): peak = 1277.113 ; gain = 0.000 ; free physical = 10464 ; free virtual = 22354
INFO: [Netlist 29-17] Analyzing 251 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-479] Netlist was created with Vivado 2018.2
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Timing 38-478] Restoring timing data from binary archive.
INFO: [Timing 38-479] Binary timing data restore complete.
INFO: [Project 1-856] Restoring constraints from binary archive.
INFO: [Project 1-853] Binary constraint restore complete.
Reading XDEF placement.
Reading placer database...
Reading XDEF routing.
Read XDEF File: Time (s): cpu = 00:00:00.15 ; elapsed = 00:00:00.29 . Memory (MB): peak = 2091.062 ; gain = 0.004 ; free physical = 9719 ; free virtual
= 21609
Restored from archive | CPU: 0.290000 secs | Memory: 3.019234 MB |
Finished XDEF File Restore: Time (s): cpu = 00:00:00.15 ; elapsed = 00:00:00.29 . Memory (MB): peak = 2091.062 ; gain = 0.004 ; free physical = 9719 ;
free virtual = 21609
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

INFO: [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646
open_checkpoint: Time (s): cpu = 00:00:17 ; elapsed = 00:01:12 . Memory (MB): peak = 2091.062 ; gain = 813.953 ; free physical = 9718 ; free virtual =
21608
Command: write_bitstream -force cpu.bit
Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'
Running DRC as a precondition to command write_bitstream
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/data/ip'.
INFO: [DRC 23-27] Running DRC with 8 threads
WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG_VOLTAGE Design Properties: Neither the CFGBVS nor CONFIG_VOLTAGE voltage
property is set in the current_design.  Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG_VOLTAGE must be set
to the correct configuration voltage, in order to determine the I/O voltage support for the pins in bank 0.  It is suggested to specify these either using the
'Edit Device Properties' function in the GUI or directly in the XDC file using the following syntax:

 set_property CFGBVS value1 [current_design]
 #where value1 is either VCCO or GND

 set_property CONFIG_VOLTAGE value2 [current_design]
 #where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.
INFO: [Vivado 12-3199] DRC finished with 0 Errors, 1 Warnings
INFO: [Vivado 12-3200] Please refer to the DRC report (report_drc) for more information.
INFO: [Designutils 20-2272] Running write_bitstream with 8 threads.
Loading data files...
Loading site data...
Loading route data...
Processing options...
Creating bitmap...
Creating bitstream...
Writing bitstream ./cpu.bit...
INFO: [Vivado 12-1842] Bitgen Completed Successfully.
INFO: [Common 17-83] Releasing license: Implementation
21 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
write_bitstream completed successfully
write_bitstream: Time (s): cpu = 00:00:09 ; elapsed = 00:00:12 . Memory (MB): peak = 2568.902 ; gain = 477.840 ; free physical = 9650 ; free virtual =
21543
INFO: [Common 17-206] Exiting Vivado at Tue Apr  1 17:13:43 2025...
```