EEE211

PSpice experiment – Part 1
Design of Basic Transistor Amplifiers

QUESTION FORM

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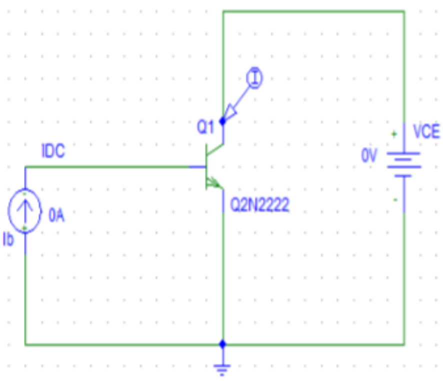
Question	Answer	For use by the marker
1) Enter the Early voltages you have obtained for the transistors: a) Q2N2222 b) Q2N2907 .	This part requires students to obtain the output characteristics of Q2N2222 and Q2N2907. Therefore, below will show their individual circuits, output characteristics and Early voltage. During this section, ‘DC sweep’ needs to choose the voltage source and ‘DC nested sweep’ needs to choose current source. In order to obtain the output characteristics in one simulation, V_{CE} should be set 0 - 20V and increases 0.5V every time while I_B should be set 0 - 40µA and increases 4µA every time. a) The circuit of Q2N2222 is shown in Figure 1.  Figure 1: The circuit of Q2N2222 Subsequently, Figure 2 is the outcome simulation of Figure 1.	

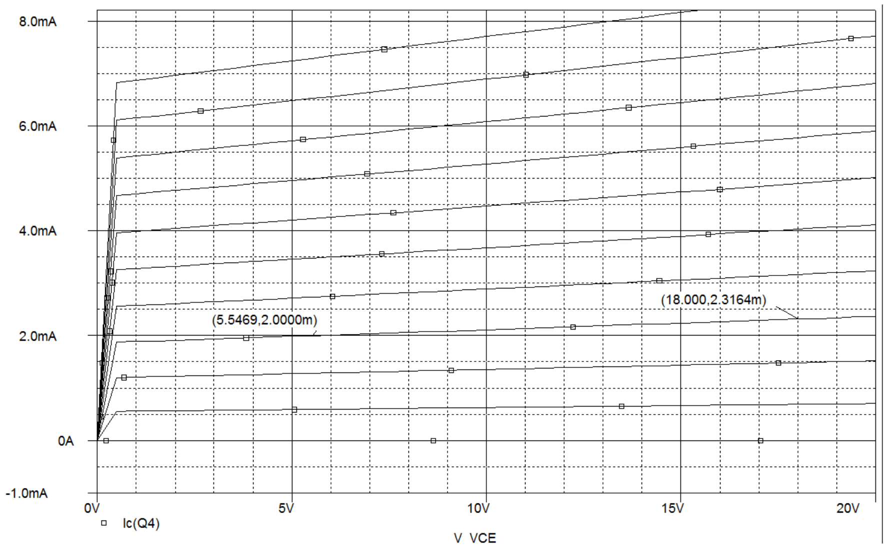


Figure 2: The output characteristics of Q2N2222

Because I_C is 2 mA and I_B is 12 μA, so β is easily to be calculated, which is

$$\beta = \frac{\boldsymbol{I_C}}{\boldsymbol{I_B}} = \frac{\mathbf{2}}{\mathbf{12 \times 10^{-3}}} = \mathbf{167}$$

From Figure 2, point (18,0.0023) and point (5.55,0.002) have been chosen, therefore these points could form a line. In order to obtain the Early voltage, the line will cross x-axis, of which the x value is the Early voltage. **In this case, the Early voltage is 73V.**

The Early Voltage of Q2N2222: 73V

b) The circuit of Q2N2907 is shown in Figure 3.

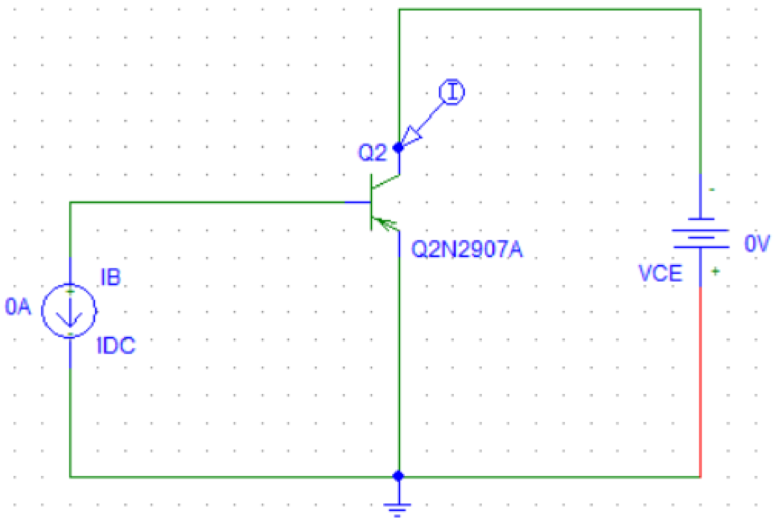


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Figure 3: The circuit of Q2N2907

Subsequently, Figure 4 is the outcome simulation of Figure 3.

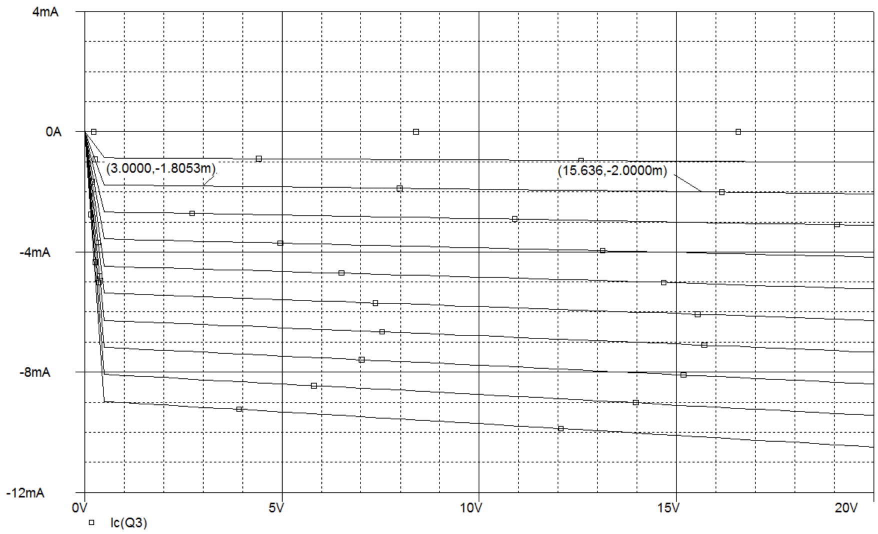

Figure 4: The output characteristics of Q2N2907

From Figure 4, point (3.0, -0.0018) and point (15.64, -0.002) have been chosen, therefore these points could form a line. In order to obtain the Early voltage, the line will cross x-axis, of which the x value is the Early voltage. In this case, the Early voltage is 112V.

The Early Voltage of Q2N2907: 112V.
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<td>2) Derive Eqn. 1 and explain the validity of it.</td>
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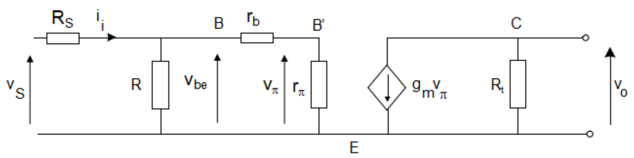
In order to operate AC analysis, the small signal equivalent circuit is desired to obtain. Therefore, Figure 5 is the small signal equivalent circuit of common-emitter amplifier.


Figure 5: The small signal equivalent circuit of common-emitter amplifier.
During this part, the voltage gain $A_V = \frac{v_O}{v_{in}}$ is required and Vin input voltage needs to be measured at the transistor base terminal. Therefore, the equation for A_V could be written as:
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$$A_v = \frac{v_o}{v_S} = \frac{v_o}{v_\pi} \times \frac{v_\pi}{v_{be}} \times \frac{v_{be}}{v_S} = -g_m R_t \times \frac{r_\pi}{r_\pi + r_b} \times \frac{R//(r_b + r_\pi)}{R_S + R//(r_b + r_\pi)}$$

Normally, compared with r_π , r_b could be ignored and $V_{be} = V_\pi$. Subsequently, A_V voltage gain will become:

$$A_v = \frac{v_o}{v_S} = \frac{v_o}{v_{be}} \times \frac{v_{be}}{v_S} = -g_m R_t \times \frac{R//r_\pi}{R_S + R//r_\pi}$$

Additionally, A_V could be also verified as:

$$A_v = -g_m R_t \approx -g_m R_C // R_L$$

where R >> r_π, r_π >> R_S and r_o >> $R_C//R_L$.

It is obvious that R_L does not exist, therefore, A_V could be written as :

$$|A_V| = g_m R_C$$

Considering the condition that:

$$I_C \approx I_S \exp\left(\frac{V_{BE}}{V_T}\right)$$

and

$$g_m \equiv \frac{\Delta I_C}{\Delta V_{BE}} = \frac{I_S}{V_T} \exp\left(\frac{V_{BE}}{V_T}\right) = \frac{I_C}{V_T}$$

Normally, the temperature of the room is 300K, therefore, V_T could be assumed as 0.25 V.

Consequently, A_V could be found which is:

$$A_V = g_m R_c = 40 I_C R_C$$

The next step is to apply KVL at C-E loop:

$$V_{CC} = I_C R_C + V_{CE}$$

Considering the maximum of A_V is desired, $I_C R_C$ should set as the maximum whose value is V_{CC}.

Finally, it could be obtained that

$$A_{Vmax} = 40 V_{CC}$$

3) Give the three values of R_C that you used and the corresponding *measured* and *theoretical* values for the circuit voltage gains.

During this section, it is required to obtain the measured values and theoretical values of voltage gain A_V. The first step is to build the circuit shown in Figure 6.

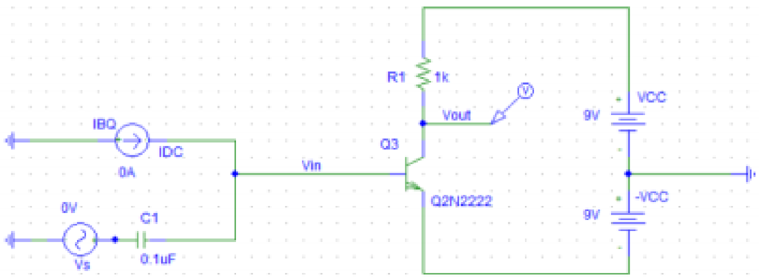

Figure 6: The circuit involved in this section.

There are three groups of measured values and theoretical values. In order to verify the authenticity, R_C will be replaced by 1KΩ, 2KΩ, 3K Ω, correspondingly.

Step 1: Before operating AC analysis, DC analysis is vital to be applied. Regarding to the DC analysis, DC signal should be connected and AC signal should be open.

Step 2: After having simulation, the base current IB should be chosen when collector voltage is at 0 V, which means IB is at the quiescent point which is I_{BQ}.

Step 3: At this stage, I_{BQ} is known, it is subsequently AC signal should be connected and operate the simulation. In the simulation page, $A_V = \frac{V_O}{V_{in}}$ could be obtained by clicking add trace and then inputting the previous A_V formula. Finally, $A_{Vmeasured}$ could be measured.

Step 4: $A_{Vtheoretical}$ will be verified below. In Question 2), it has given that $A_V = g_m R_t$. Actually, $R_t = R_C//r_o$. Therefore, $A_V = g_m R_C//r_o$. r_o would be ignored only when r_o is infinity large. Additionally, $r_o = \frac{V_A + V_{CE}}{I_{CQ}}$. Considering it is the theoretical value, so r_o cannot be ignored. Due to the fact that R_C in each group is distinct, therefore $A_{Vtheoretical}$ will be different as well.

After having described the steps for this section, students need to follow and repeat these 4 steps until outcomes for each group have been recorded.

Below will show figures of simulation for each I_{BQ} and $A_{V measured}$ and the process to find $A_{V theoretical}$.

a) R_C = 1KΩ

As it has been referred previously, Figure 6 is the circuit when R_C = 1KΩ. Figure 7 is the output for finding I_{BQ} when R_C = 1KΩ.

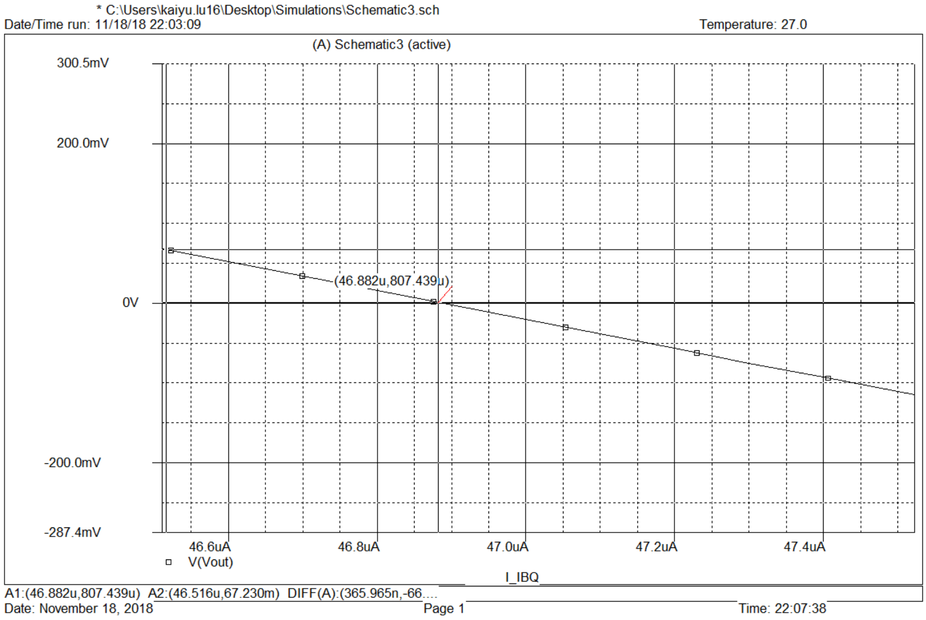

Figure 7: Output for finding I_{BQ} when R_C = 1KΩ.

From Figure 7, it could be observed that I_{BQ} is 46.882uA.

The value of straight line in Figure 8 is the simulation for obtaining A_V.

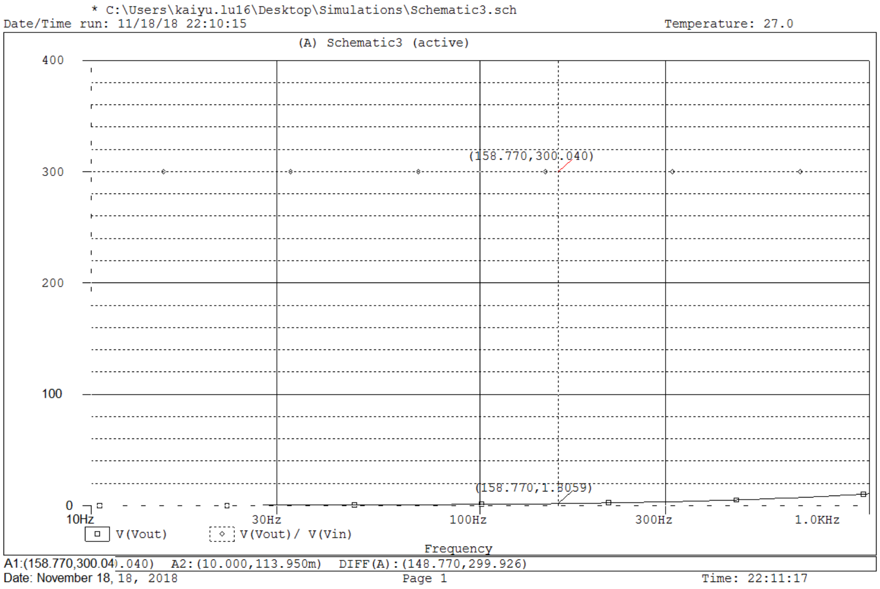

Figure 8: Measured A_V when R_C = 1KΩ.

Therefore, **$A_{Vmeasured}$ is 300.04** from Figure 8.

Figure 9 is AC analysis to obtain I_{CQ} so that $A_{Vtheoretical}$ could be verified.

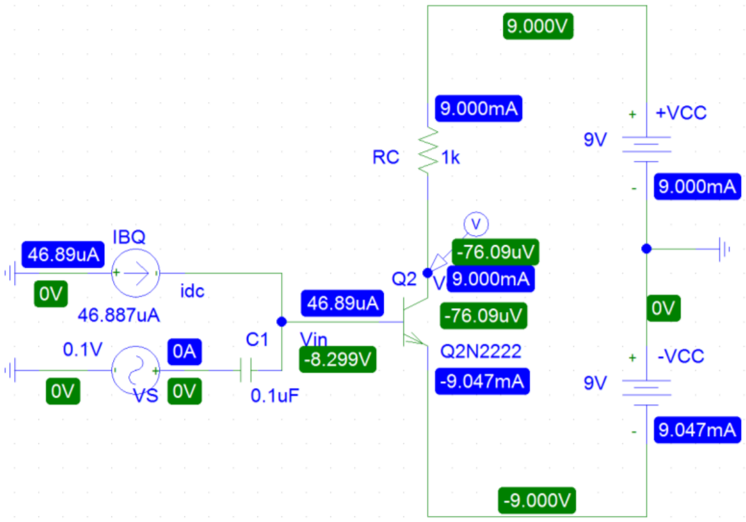

Figure 9: AC analysis when R_C = 1KΩ.

Due to $r_o = \frac{V_A + V_{CE}}{I_{CQ}} = \frac{73+9}{9m}$ = 9.78 KΩ

Therefore,

$$A_{Vtheoretical} = g_m R_C // r_o = 40 I_{CQ} R_C // r_o = 40 \times 9m \times \frac{1k \times 9.78k}{1k + 9.78k} =$$

$$\mathbf{326.60}$$

In conclusion

$A_{V\text{measured}}$ = 300.04 **$A_{V\text{theoretical}}$ = 326.60**

b) R_C = 2KΩ

Figure 10 is the circuit when R_C = 2KΩ.

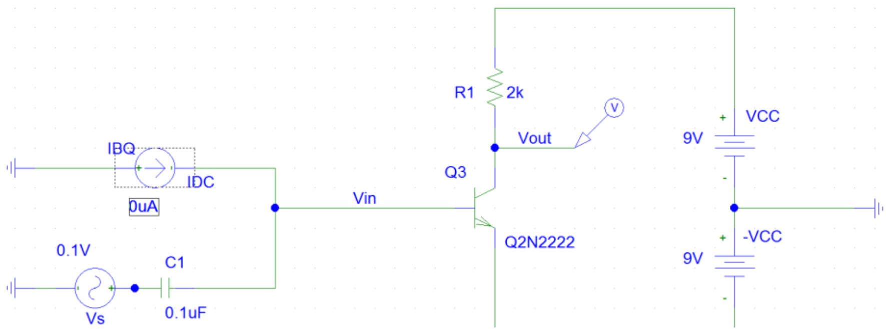

Figure 10: Circuit when R_C = 2KΩ (DC).

Figure 11 is the output for finding I_{BQ} when R_C = 2KΩ.

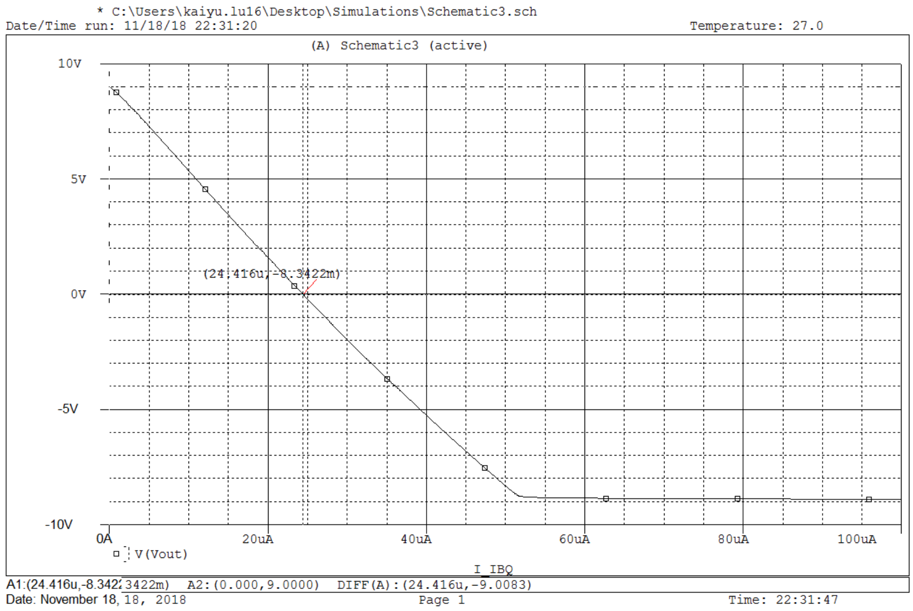

Figure 11: Output for finding I_{BQ} when R_C = 2KΩ.

From Figure 11, it could be observed that I_{BQ} is 24.416uA.

The value of straight line in Figure 12 is the simulation for obtaining A_V.

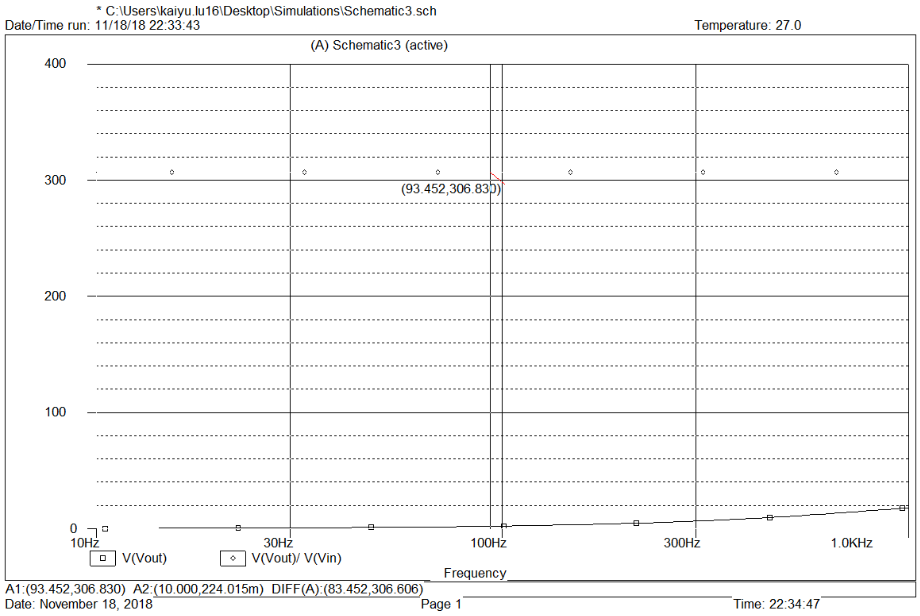

Figure 12: Measured A_V when R_C = 2KΩ.

Therefore, A_V is 306.83 from Figure 12.

Figure 13 is AC analysis to obtain I_{CQ} so that $A_{Vtheoretical}$ could be verified.

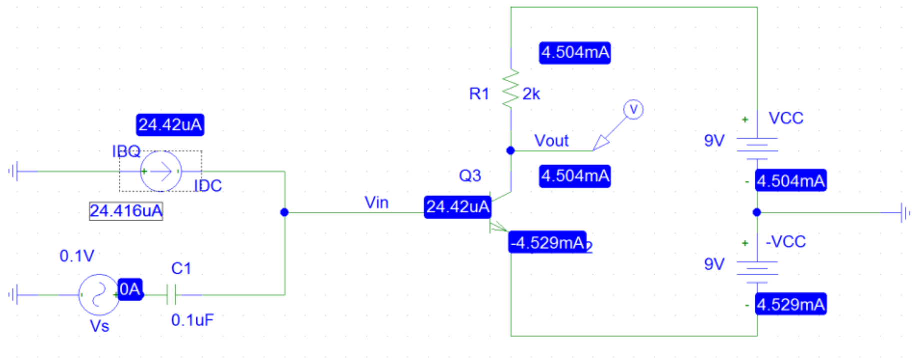

Figure 13: AC analysis when R_C = 2KΩ.

Due to $r_o = \frac{V_A + V_{CE}}{I_{CQ}} = \frac{73+9}{4.5m} =$ 18.22 KΩ

Therefore,

$$A_{Vtheoretical} = g_m R_C // r_o = 40 I_{CQ} R_C // r_o = 40 \text{ x } 4.5\text{m x } \frac{2k \ x \ 18.22k}{2k + 18.22k} =$$

$$324.39$$

In conclusion

$A_{Vmeasured}$ = 306.83 **$A_{Vtheoretical}$ = 324.39**

c) R_C = 3KΩ

Figure 14 is the circuit when R_C = 3KΩ.

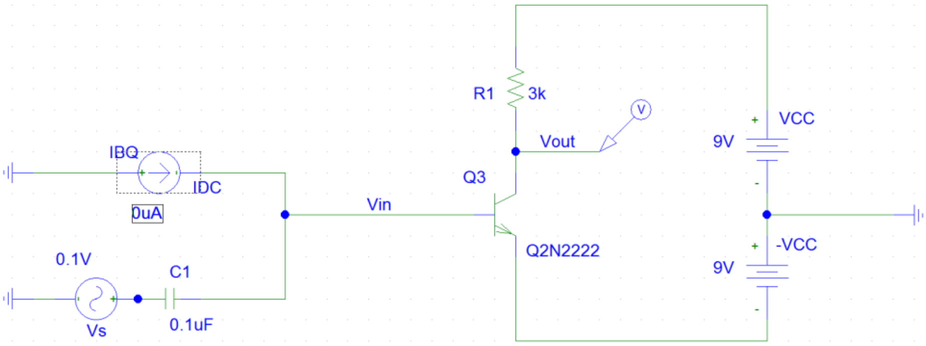

Figure 14: Circuit when R_C = 3KΩ (DC).

Figure 15 is the output for finding I_{BQ} when R_C = 3KΩ.

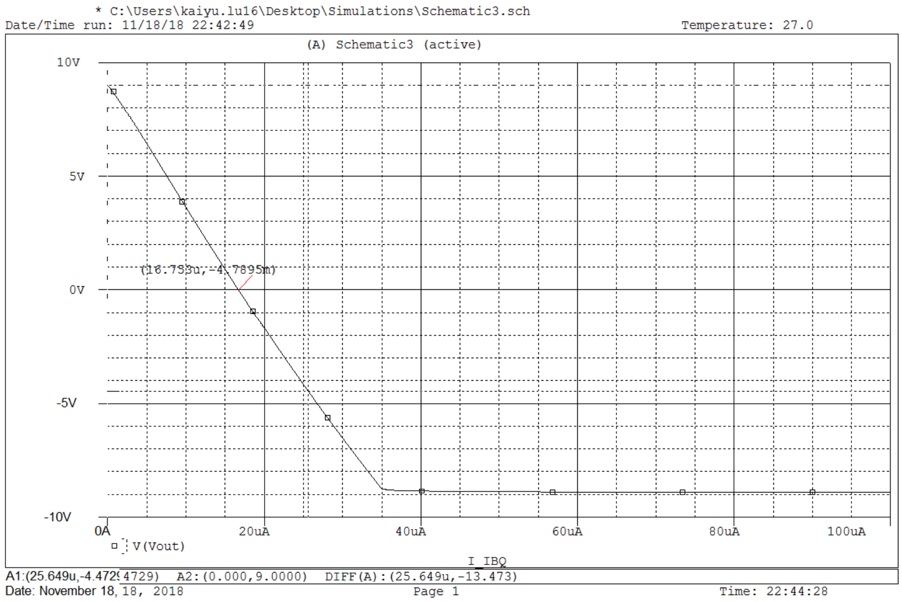

Figure 15: Output for finding I_{BQ} when R_C = 3KΩ.

From Figure 15, it could be observed that I_{BQ} is 16.753uA.

The value of straight line in Figure 16 is the simulation for obtaining A_V.

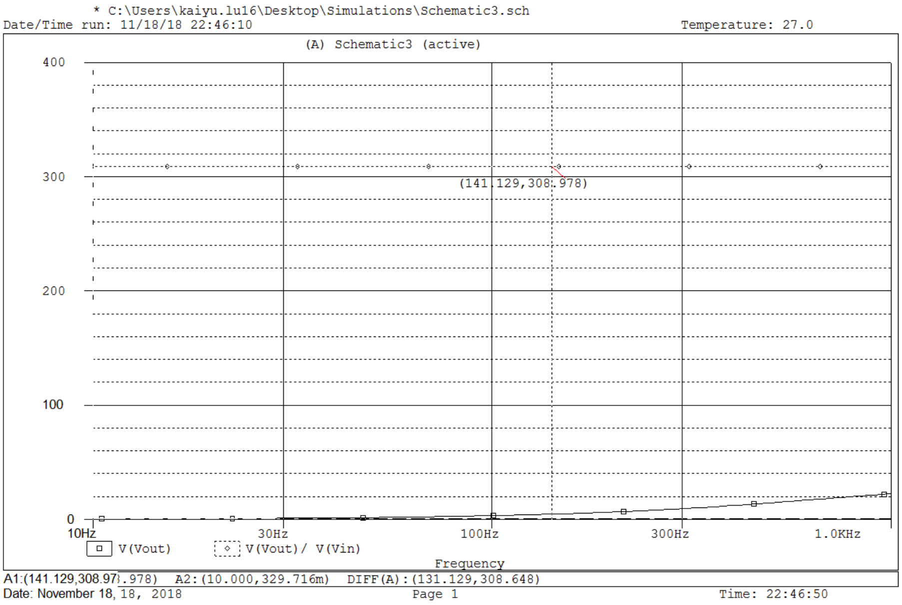

Figure 16: Measured A_V when R_C = 3KΩ.

Therefore, A_V is 308.978 from Figure 16.

Figure 17 is AC analysis to obtain I_{CQ} so that $A_{V\text{theoretical}}$ could be verified.

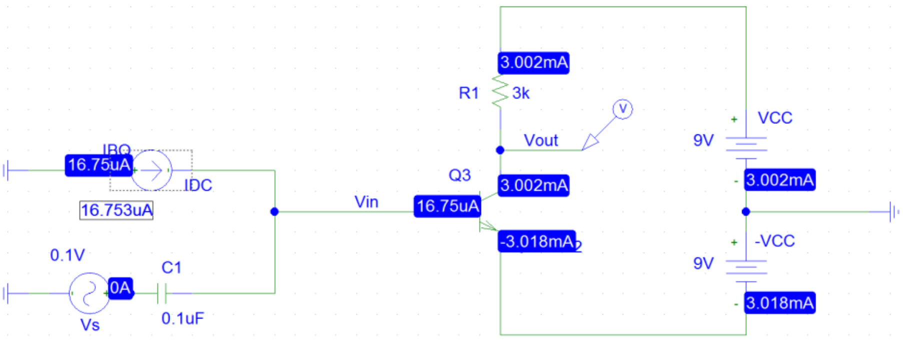

Figure 17: AC analysis when R_C = 1KΩ.

Due to $r_o = \frac{V_A+V_{CE}}{I_{CQ}} = \frac{73+9}{3m} =$ 27.33KΩ

Therefore,

$$A_{V\text{theoretical}} = g_m R_C//r_o = 40 I_{CQ} R_C//r_o = 40 \times 3m \times \frac{3k \times 27.33k}{3k + 27.33k} =$$

324.39

In conclusion

$A_{V\text{measured}}$ = 308.978 **$A_{V\text{theoretical}}$ = 324.39**

4) Consider R_L to – Vcc same of R_C. Repeat for A_I.

In order to obtain A_I, R_L should be connected in output whose value is the same as R_C.

This section is the following part of Question 3, of which the reason is that students will set I_{BQ} which has been simulated corresponding. Subsequently, it is supposed to operate the simulation and obtain $A_{Imeasured}$ by adding trace so that $A_{Imeasured} = \frac{I_o}{I_i}$.

d) **R_C = 1KΩ**

Figure 18 is the circuit when R_L = 1K Ω which is the condition of AC analysis.

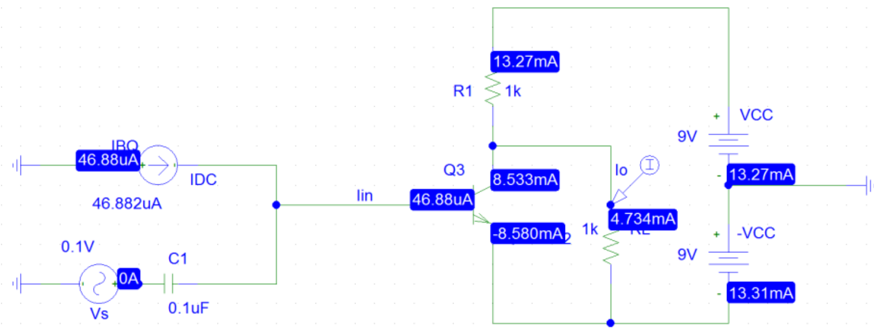

Figure 18: AC analysis when R_L = 1K Ω

After having I_{BQ} and I_{CQ} from Figure 18, Figure 19 is the sequential simulation by adding trace in order to obtain current gain $A_{Imeasured}$.

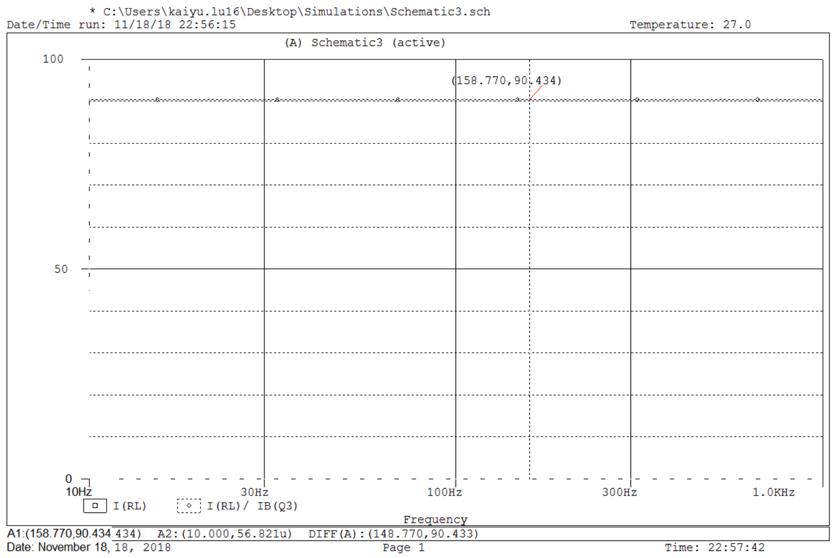

Figure 19: $A_{Imeasured}$ when R_L = 1K Ω

Regarding to $A_{Itheoretical}$, it could be verified below.

Due to

$$r_o = \frac{V_A + V_{CE}}{I_{CQ}} = 9.78\ \mathrm{K}\Omega$$

And we have

$$\beta = \frac{I_{CQ}}{I_{BQ}} = \frac{8553}{46.88} = 182.44$$

Therefore,

$$A_{Itheoretical} = \beta \times \frac{R_C//r_o}{R_C//r_o + R_L} = 86.78$$

In conclusion,

$A_{Imeasured}$ = 90.434 **$A_{Itheoretical}$ = 86.78**

e) R_C = 2KΩ

Figure 20 is the circuit when R_L = 1K Ω which is the condition of AC analysis.

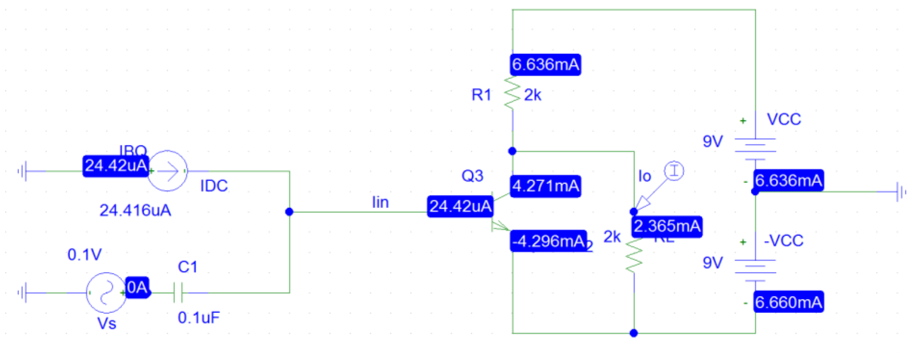

Figure 20: AC analysis when R_L = 2K Ω

After having I_{BQ} and I_{CQ} from Figure 20, Figure 21 is the sequential simulation by adding trace in order to obtain current gain $A_{Imeasured}$.

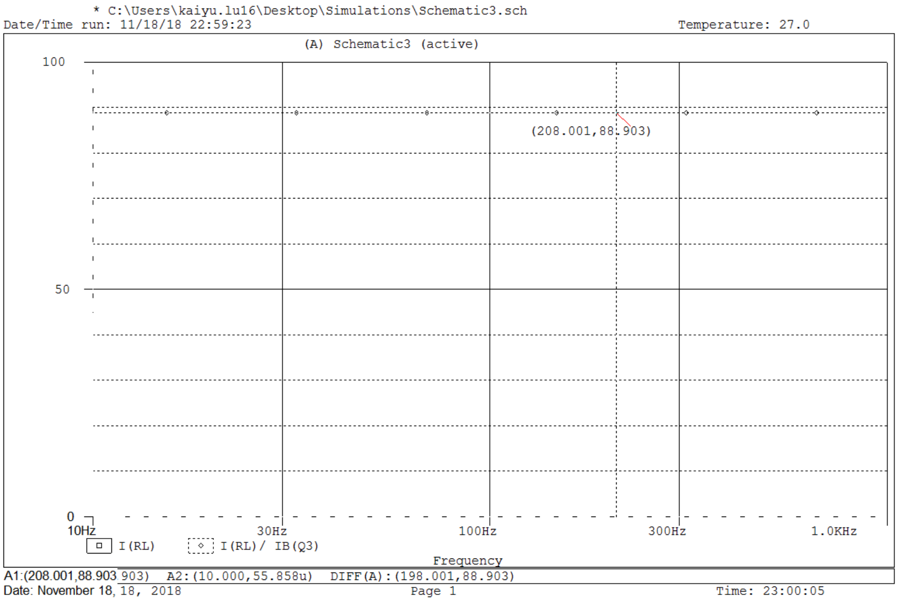

Figure 21: $A_{Imeasured}$ when R_L = 2K Ω

Regarding to $A_{Itheoretical}$, it could be verified below.

Due to

$$r_o = \frac{V_A + V_{CE}}{I_{CQ}} = 18.22\ \text{K}\Omega$$

And we have

$$\beta = \frac{I_{CQ}}{I_{BQ}} = \frac{4271}{24.42} = 175$$

Therefore,

$$A_{Itheoretical} = \beta \times \frac{R_C//r_o}{R_C//r_o + R_L} = 82.91$$

In conclusion,

$A_{Imeasured}$ = 88.903 **$A_{Itheoretical}$ = 82.91**

f) R_C = 3KΩ

Figure 22 is the circuit when R_L = 1K Ω which is the condition of AC analysis.

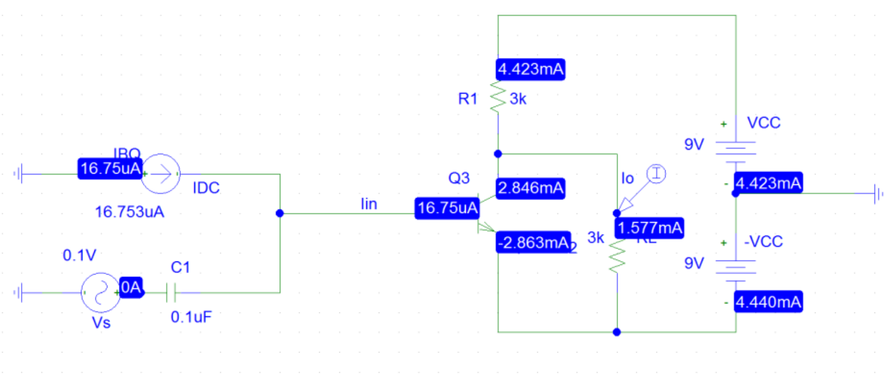

Figure 22: AC analysis when R_L = 3K Ω

After having I_{BQ} and I_{CQ} from Figure 22, Figure 23 is the sequential simulation by adding trace in order to obtain current gain $A_{Imeasured}$.

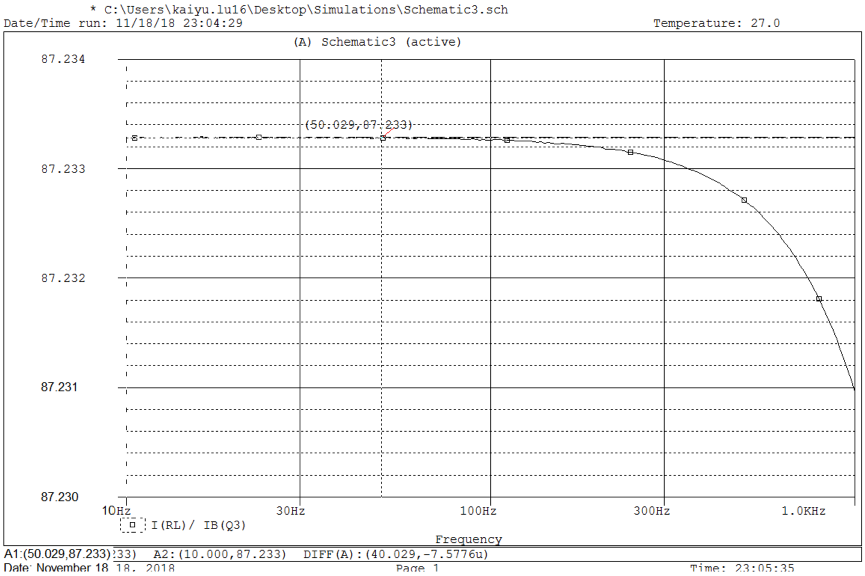

Figure 23: $A_{Imeasured}$ when R_L = 3K Ω

Regarding to $A_{Itheoretical}$, it could be verified below.

Due to

$$r_o = \frac{V_A + V_{CE}}{I_{CQ}} = 27.33\ \text{K}\Omega$$

And we have

$$\beta = \frac{I_{CQ}}{I_{BQ}} = \frac{2846}{16.75} = 169.91$$

Therefore,

$$A_{Itheoretical} = \beta \times \frac{R_C//r_o}{R_C//r_o + R_L} = 80.497$$

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In conclusion,

$A_{Imeasured}$ = 87.233 **$A_{Itheoretical}$ = 80.497**

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5) Give the measured output resistance and voltage limits of the circuit.

How are these values related to the transistor characteristics?

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This section requires to build a current mirror circuit and verify its performance on acting as a constant source. R_{out} and $V_{lower\ limit}$ is the significant parameters to identify the property. Accordingly, Figure 24 is the desired circuit in this section.

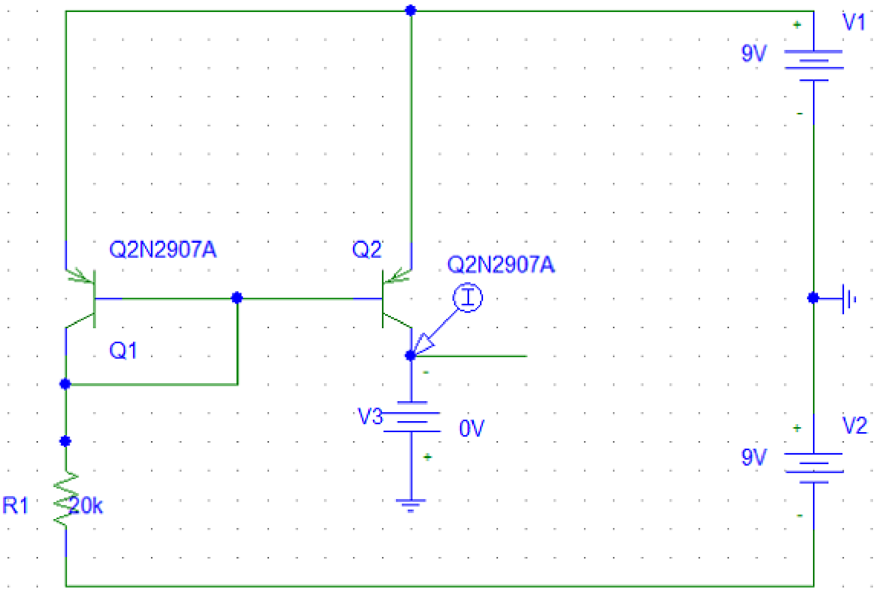

Figure 24: The diagram of the current mirror circuit.

Due to the requirement that total current drawn from the power supply should be less than 5 mA. Therefore, R_1 should be set as 20 KΩ in order to meet the requirement. As for the DC situation, voltage source V_{CC} should be swept from -9V to 9V with 0.1 increments.

Subsequently, Figure 25 is the simulation for the Figure 24.

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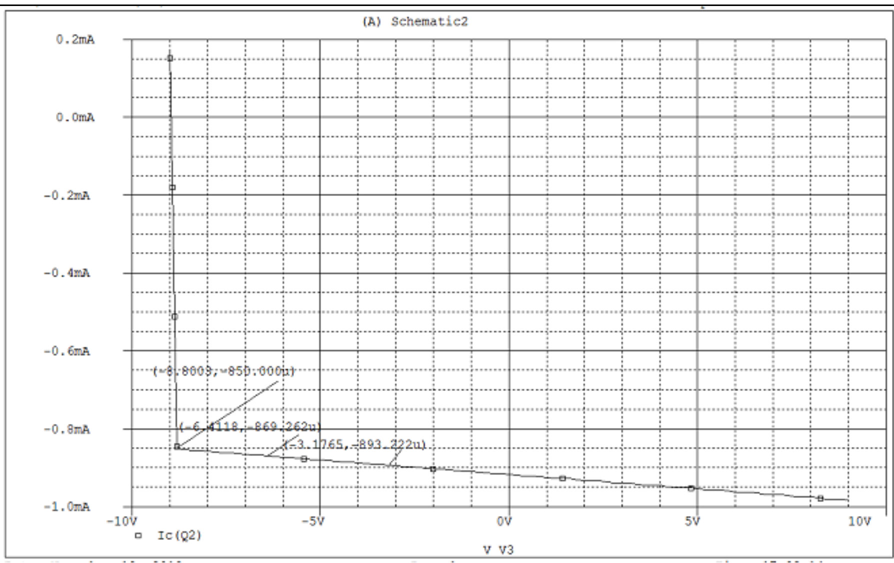


Figure 25: The output simulation for obtaining R_{out}.

Because the slope of the line in Figure 25 is the inverse of R_{out}, it is therefore in order to obtain R_{out}, the slope of the line should be calculated firstly by choosing two points. Then the real R_{out} is the inverse of the slope of the line.

Two chosen points: (6.4118, -869.262u) and (-3.1765, -893.222u).

Therefore,

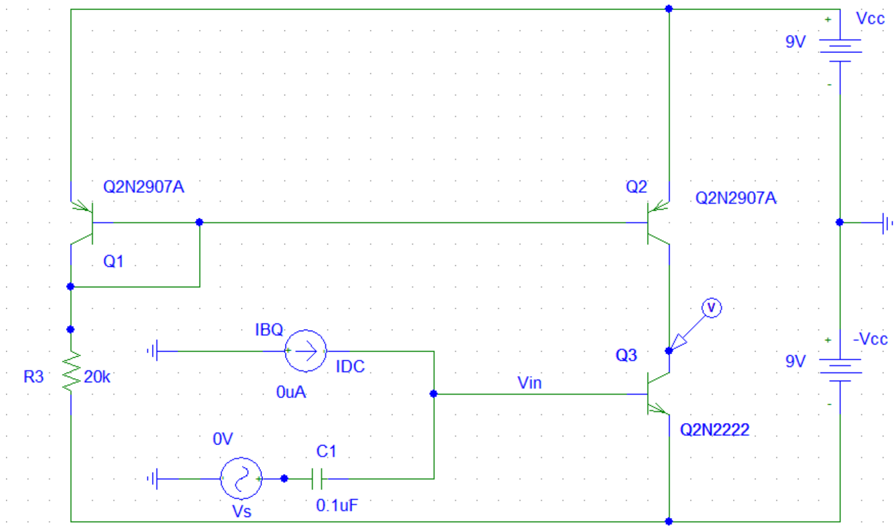
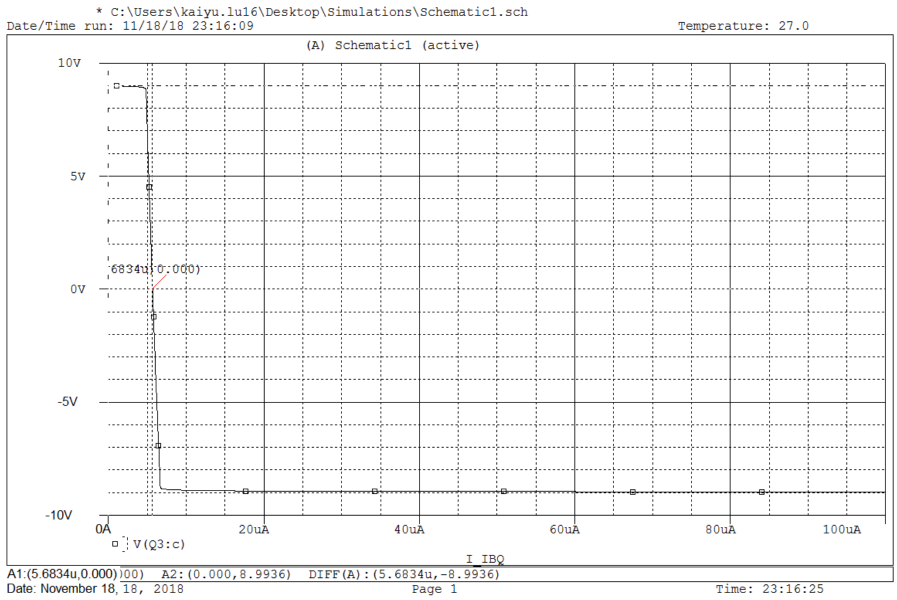
$$\mathbf{R_{out}} = \frac{\mathbf{1}}{\frac{\mathbf{-869.262u+961.239u}}{\mathbf{6.4118+3.1765}}} = \mathbf{135.029\ K\Omega}$$

From Figure 25, it could be observed that when the point is at (8.8, -851u), the slop of the line will increase rapidly.

Therefore, $V_{lower\ limit}$ = 8.8V.

In conclusion

R_{out} = 135.029 KΩ **$V_{lower\ limit}$ = 8.8V**

6) Copy your circuit in which current mirror acting as the collector load of the common emitter stage.	 Figure 26: C-E amplifier circuit with current mirror circuit.	
7) Enter the values you have obtained for the voltage gain, A_V and the current drawn from the voltage supply, I_{CC}.	In terms of this section, it is desired to combine the common-emitter amplifier circuit with the current mirror circuit. More specifically, the R_C in the common-emitter amplifier is replaced by a constant current source. Figure 26 is the described circuit in this section. Additionally, I_{BQ} has been found subsequently by DC analysis. From Figure 27, it could be observed that I_{BQ} is 5.6834uA.  Figure 27: DC analysis for finding I_{BQ}. After that, AC analysis with I_{BQ} should be implemented by adding trace in order to obtain voltage gain A_V. Therefore, Figure 28 is the result.	

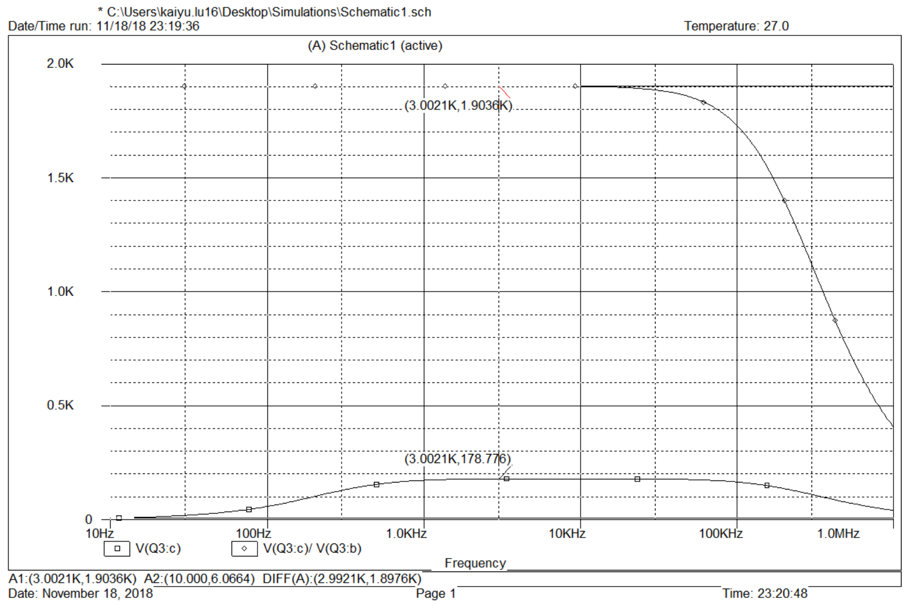


Figure 28: AC analysis for finding voltage gain A_V.

Figure 29 is the detailed circuit of the circuit in Figure 26 which includes the currents and voltages in every branch.

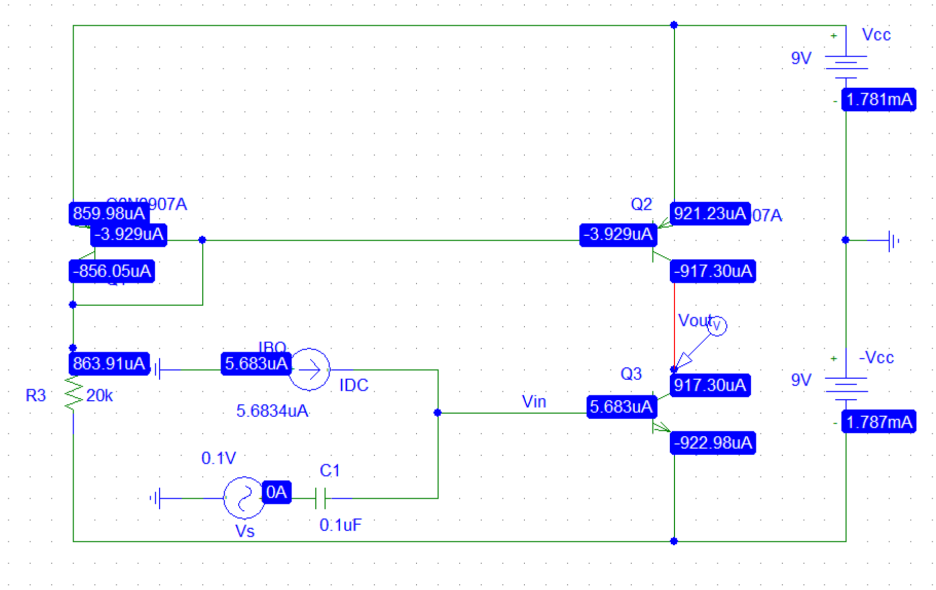


Figure 29: Detailed circuit of the circuit in Figure 26

Consequently, it is convenient to obtain I_{CC}. That is,

$$I_{CC} = 858.98\mu A + 921.23\mu A = 1.78021mA$$

In conclusion:

A_V = 1.9036K **I_{CC} = 1.78021mA**

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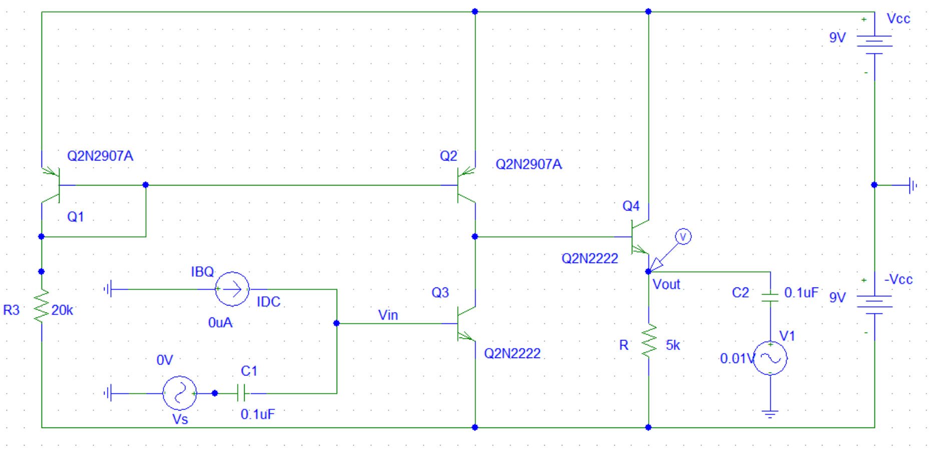

Figure 30: The combination of last two kinds of circuits with the emitter follower circuit

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<td>9) Enter the values for the voltage gain A_V, I_{CC} and the output resistance R_O</td>
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Regarding to this section, it is the combination of last two kinds of circuits with the emitter follower circuit. The first step is still to operate DC analysis, and then Figure 31 show the simulation for finding I_{BQ}.

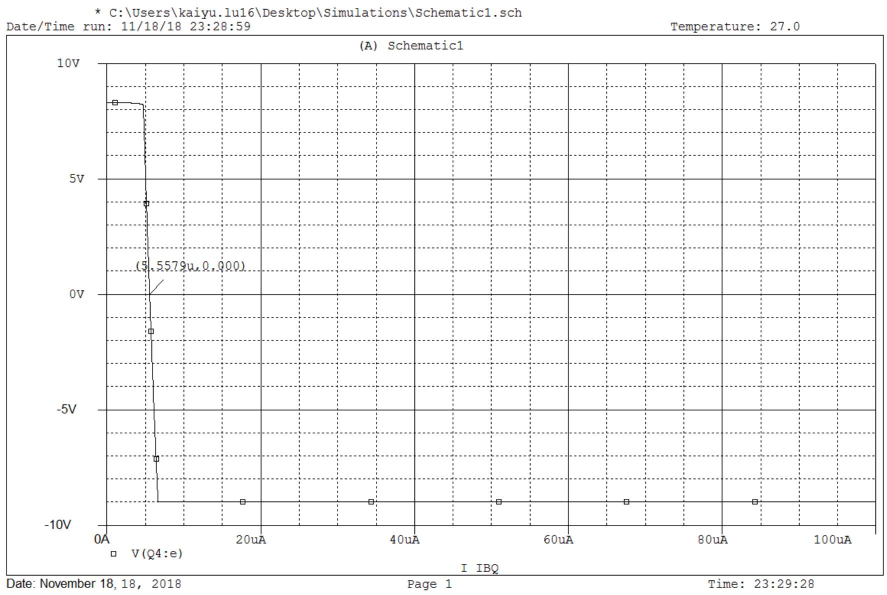

Figure 31: DC analysis for find I_{BQ}.

After having I_{BQ}, the next step is to simulate AC analysis which could obtain A_V, so Figure 32 is the measured A_V whose value is 1.7793K.

</td>
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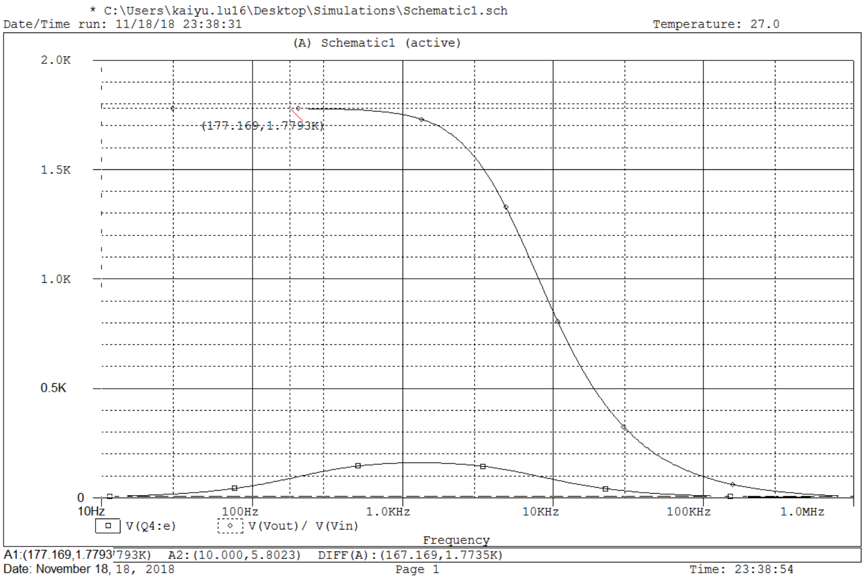

Figure 32: Result for obtaining A_V.

Regarding to I_{CC}, it could be operated in the similar way which is to show the detailed circuit and then add the necessary current belongs to I_{CC}. Therefore, Figure 33 is the detailed circuit.

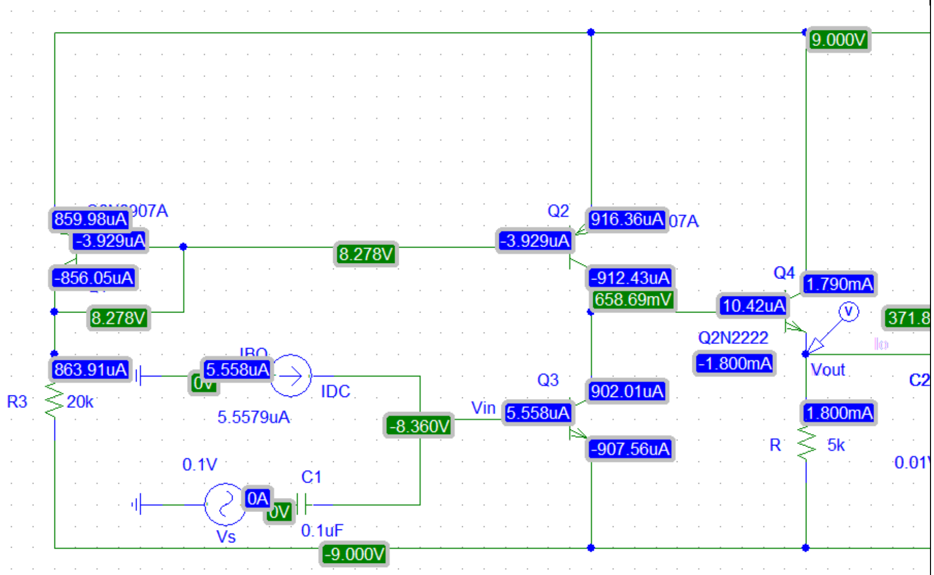

Figure 33: The detailed circuit for Figure 30.

Consequently, it is convenient to obtain I_{CC}. That is,

$$I_{CC} = 859.98\mu A + 916.36\mu A + 1.79mA = 3.56634mA$$

In order to obtain R_{out}, after the simulation, it should be done by adding trace. During choosing the point, it should be chosen at the point where is more flat compared with other points. Finally, R_o is from Figure 34.

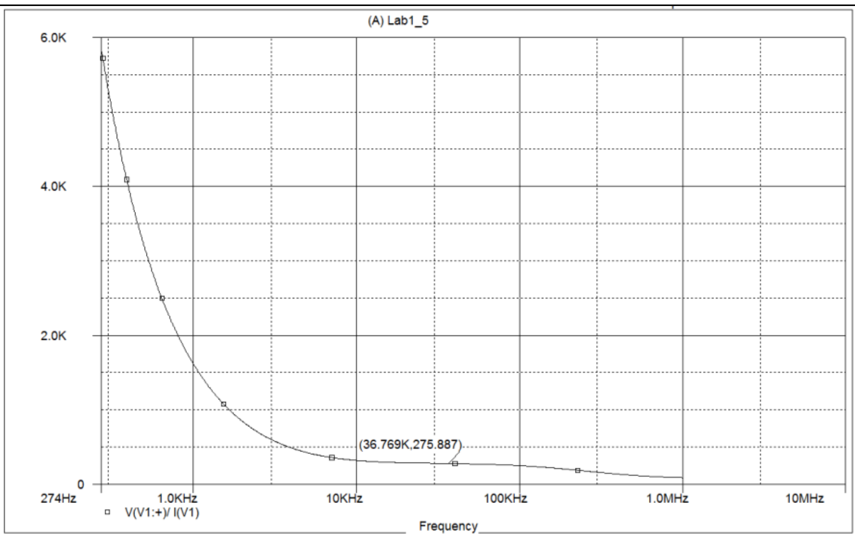

Figure 34: The simulation for finding R_o.

In conclusion,

A_V = 1.7793K **I_{CC} = 3.56634mA** **R_O = 275.9**