EEE211

PSpice experiment – Part 2
Design of an Operational Amplifier

QUESTION FORM

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Questions

1. ***Briefly explain how an 'active load' doubles the gain of the differential input stage (10%)***

   In the differential mode, it has passive load and active load. Figure 1 is the circuit for the PNP long tailed pair with passive load.

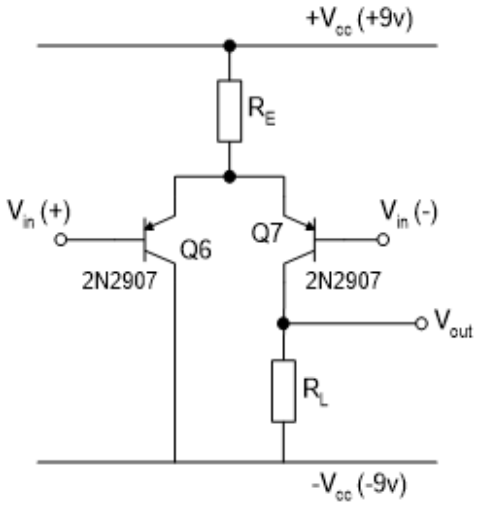

Figure 1: A PNP long tailed pair with passive load.

The fundamental formula for the voltage gain of the circuit is:

$$A_V = \frac{V_{out}}{V_{in}}$$

And, it could be also obtained that $i_c = g_m V_\pi$ and $V_{out} = i_c \times R_L'$, where R_L' is the total effective load 'seen' by the collector of Q7.

Moreover,

$$V_\pi = \frac{V_d}{2} = \frac{V_{in}}{2}$$

Therefore,

$$A_{V1} = \frac{V_{out}}{V_{in}} = \frac{i_c \times R_L{}'}{V_{in}} = \frac{g_m V_\pi R_L{}'}{2V_\pi} = \frac{g_m R_L{}'}{2}$$

Figure 2 is the circuit of the differential amplifier with active load.

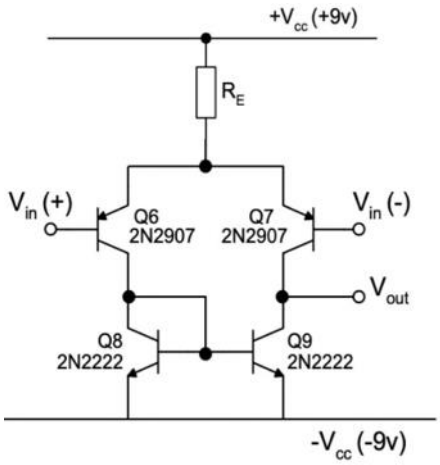

Figure 2: The differential amplifier with active load.

Similarly, the voltage gain of the circuit could be verified following:

$$A_V = \frac{V_{out}}{V_{in}} = \frac{i_{out} \times R_L{}'}{V_{in}}$$

In this circuit, i_{out} could be verified as:

$$i_{out} = i_{C7} - i_{C9}$$

And by the property of the current mirror, it could obtain:

$$i_{C9} = i_{C6}$$

Then $i_{out} = i_{C7} - i_{C6} = g_m v_{in(+)} - g_m v_{in(-)} = g_m V_{in}$ because $V_{in} = v_{in(+)} - v_{in(-)}$.

Therefore,

$$i_{out} = i_{C7} - i_{C6} = g_m(v_{in(+)} - v_{in(-)}) = g_m V_{in}$$

Then, the voltage of output with the load is:

$$V_{out} = i_{out} \times R_L' = g_m V_{in} R_L'.$$

Finally, the voltage gain of the circuit is:

$$A_{V2} = \frac{V_{out}}{V_{in}} = A_V = \frac{g_m V_{in} R_L'}{V_{in}} = g_m R_L'$$

In conclusion, compared with A_{V2} and A_{V1}, 'active load' A_{V2} doubles the gain of the differential input stage A_{V1}.

2. ***Give the circuit diagram of your differential amplifier input circuit and show your calculation of the differential input resistance and voltage gain of the input stage. (15%)***

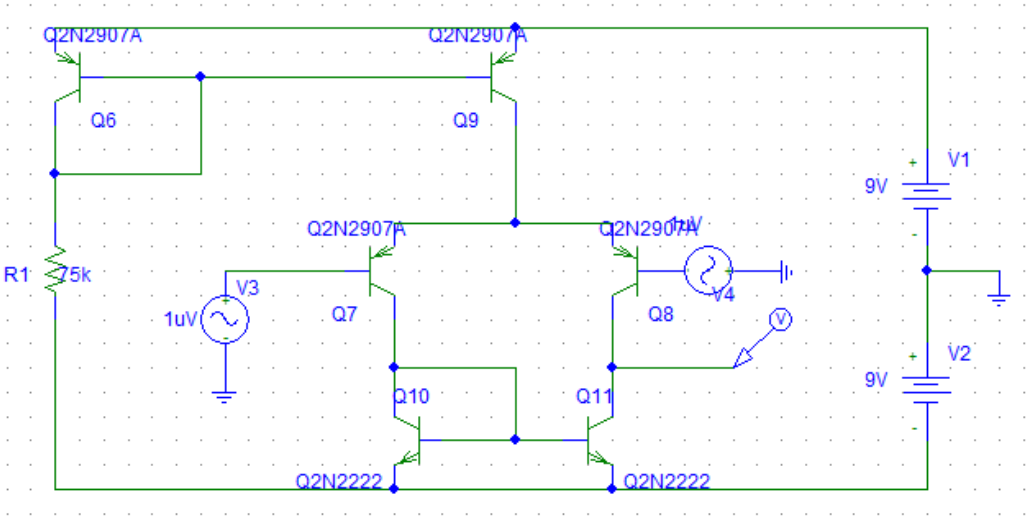

Figure 3: The circuit diagram of the differential amplifier circuit

Regarding to the reference current I_{Ref}, it could be verified as follows:

$$I_{Ref} = \frac{V_{CC} - V_{BE:Q6}(on) - (-V_{CC})}{R_1} = \frac{9 - 0.7 + 9}{75000} = 0.231 \text{ mA}$$

According to the Figure 3, I_{CQ3} and I_{CQ4} are the same due the property of the current mirror. Additionally, $I_{C:Q7}$ and $I_{C:Q8}$ are both the half value of the reference current I_{Ref}. Therefore, $I_{C:Q7}$ and $I_{C:Q8}$ could be calculated by:

$$I_{C:Q7} = I_{C:Q8} = \frac{0.231\ mA}{2} = 0.1155\ mA$$

By the equation $r_\pi = \frac{\beta V_T}{I_{CQ}}$, $r_{\pi:7}$ could be obtained by $I_{C:Q7}$

$$r_{\pi:7} = \frac{\beta V_T}{I_{CQ}} = \frac{\beta}{40 I_{C:Q7}} = \frac{250}{40 I_{CQ}} = 54.4\ k\Omega$$

Subsequently, the input resistance R_{in} could be verified from $r_{\pi:7}$:

$$R_{in} = 2r_{\pi 7} = 108.8\ k\Omega$$

Because the voltage gain is related with R_L', and $R_L' = r_{o8} || r_{o11}$. Therefore, r_{o8} and r_{o11} should be calculated firstly as follows:

$$r_{o8} = \frac{V_A}{I_{C:Q8}} = \frac{113}{0.1155 \times 10^{-3}} = 978.35\ k\Omega$$

$$r_{o11} = \frac{V_A}{I_{CQ:11}} = \frac{73}{0.1155 \times 10^{-3}} = 632.034\ k\Omega$$

Therefore, $R_L' = r_{o8} || r_{o11} = \frac{r_{o8} r_{o11}}{r_{o8} + r_{o11}} = \frac{978.35 * 632.034}{978.35 + 632.034} = 383.98\ k\Omega$

It is eventually the voltage gain A_V could be obtained by:

$$A_V = -g_m \mathrm{R_L}' = -40 \times I_{C:Q7} \times \mathrm{R_L}' = -40 \times 0.1155m \times 383.98k$$

$$= -1773.99$$

In conclusion:
voltage gain $\boldsymbol{A_V = -1773.99}$ and input resistance $\boldsymbol{R_{in} = 108.8\ k\Omega}$

3. ***Give your measurements used to obtain the input resistance and voltage gain of the input stage by simulation of the circuit. (10%)***

In order to obtain the measurement of the input resistance and voltage gain, Figure 4 could be generated.

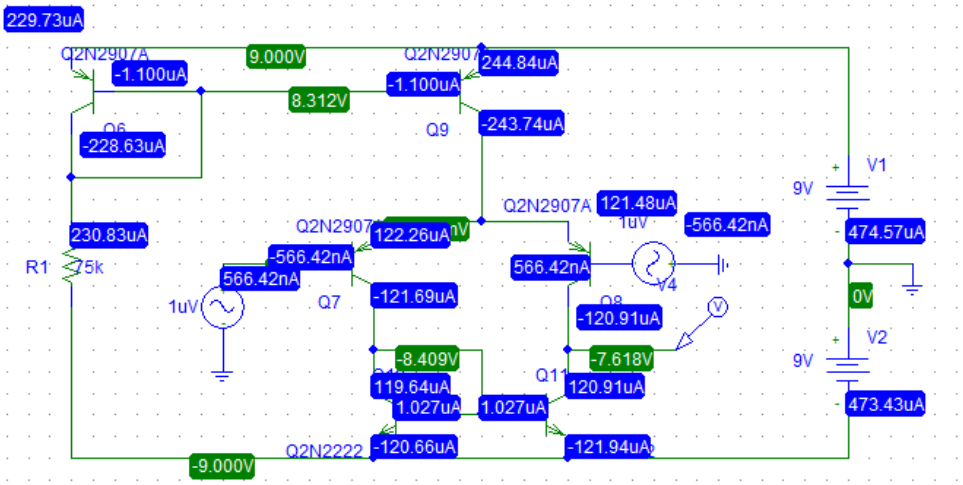

Figure 4: Figure 3 in details

After constructing the circuit, it should be simulated. Regarding to finding the input resistance, adding trace should be then implemented. In adding trace, the formula should is: $\frac{V(V_7{:}b)}{I(Q7)} + \frac{V(V_8{:}b)}{I(Q8)}$.

Then, Figure 5 the result for measuring input resistance after adding trace.

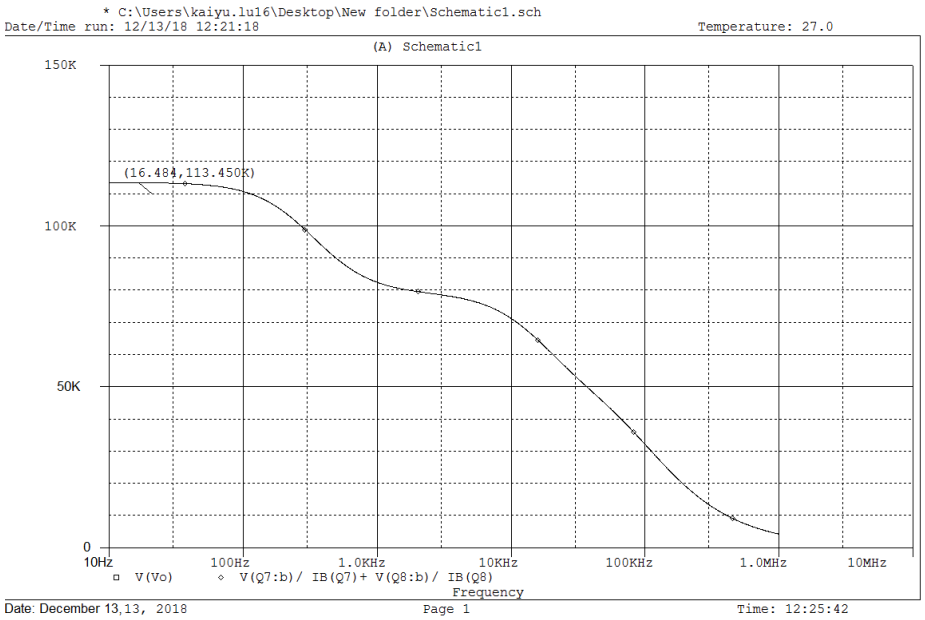

Figure 5: The measured input resistance

From Figure 5, it could be observed that the input resistance $\boldsymbol{R_{in} = 113.45\ k\Omega}$.

The next step is to find the voltage gain. In order to obtain the voltage gain, adding trace should be set again whose formula is: $V(V_o)/V(V3:+)-V(V4:-)$.

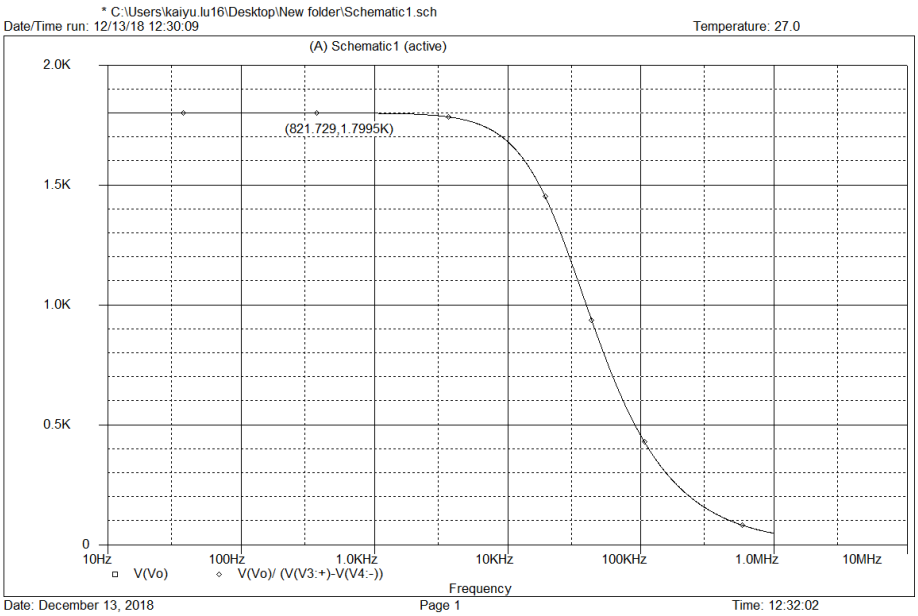

Figure 6: The result of measuring voltage gain

From Figure 6, it could be found that the voltage gain $\boldsymbol{A_V = 1.7995K}$.

In conclusion, the input resistance $\boldsymbol{R_{in} = 113.45\ k\Omega}$ and the voltage gain $\boldsymbol{A_V = 1.7995K}$.

4. ***Show the voltage transfer characteristic obtained by simulation. (10%)***

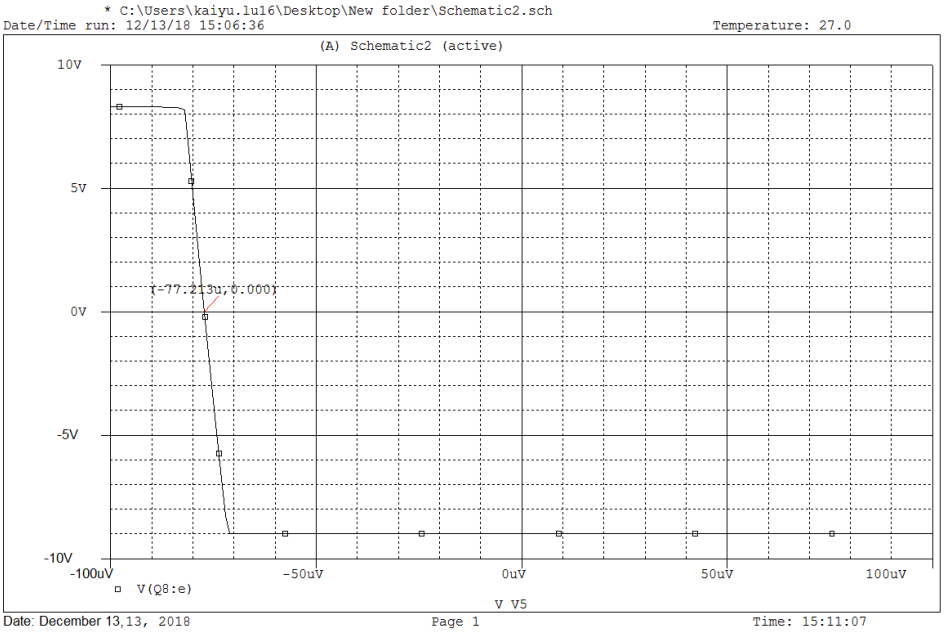

Figure 7: The voltage transfer characteristic obtained by simulation

5. ***Give your calculation of the open-loop differential voltage gain and the output resistance of the whole amplifier. You should make reference to the amplifier properties sheet included in the laboratory script and make reasonable approximations. (20%)***

Figure 8 is the completed circuit after simulating.

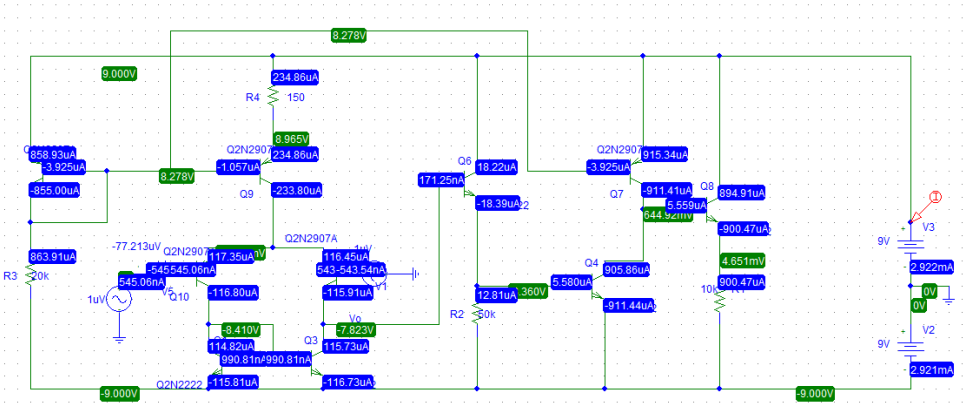

Figure 8: The completed circuit.

In order to obtain the open-loop differential voltage gain and the output, the detailed currents and voltages could be observed and calculated form Figure 8. Overall, there are four stages for the voltage gain. Firstly, the transistors Q9 and Q7 could generate the current mirror. As for the third and the fifth stages are common-collector amplifiers which could be assumed as 1. Regarding to the second and the fourth stages are the differential amplifier and common emitter amplifier, respectively. Therefore, the total voltage gain of this circuit could be verified as:

$$A_v = A_{v2} \times A_{v4}$$

For A_{v2}, it could be also verified as:

$$A_{v2} = -g_{m2}\left(r_{o2}||r_{o3}||R_{iQ6}\right)$$

$$r_{o2} = \frac{V_A}{I_{C2}} = \frac{113}{0.1155\ mA} = 978.355\ k\Omega$$

$$r_{o3} = \frac{V_A}{I_{C2}} = \frac{74}{0.1155\ mA} = 640.693\ k\Omega$$

$$R_{iQ6} = (1+\beta)(R_2||r_{\pi4}) + r_{\pi6}$$

And

$$r_{\pi2} = \frac{\beta}{g_{m2}}$$

$$g_{m2} = 40 \times I_{C2} = 4.64\ mA/V$$

$$r_{\pi6} = \frac{\beta}{g_{m6}} = \frac{167}{0.56} = 298.21\ \ k\Omega$$

$$g_{m4} = 40 \times I_{C4} = 36.4\ mA/V$$

$$r_{\pi4} = \frac{\beta}{g_{m4}} = \frac{167}{36.4} = 4.59\ k\Omega$$

Therefore,

$$R_{iQ6} = (1+\beta)(R_2||r_{\pi4}) + r_{\pi6} = 706.28 + 298.21 = 1005\ k\Omega$$

$$A_{v2} = -g_{m2}\left(r_{o2}||r_{o3}||R_{iQ6}\right) = -4.64 \times 279.5 = -1296.84$$

As for A_{v4}, it is :

$$A_{v4} = -g_{m4}\left(r_{07}||r_{o4}||R_{iQ8}\right)$$

From Figure 10, I_{C4} and I_{C8} could be found:

$$I_{C4} + \frac{I_{C8}}{\beta} = I_{C7}$$

$$I_{C8} = \frac{V_{CC}}{10\ k\Omega} = \frac{9\ V}{10\ k\Omega} = 0.9\ mA$$

And Apply KVL at the transistor Q7:

$$I_{C7} = \frac{V_{CC} - V_{BE}(on) - (-V_{CC})}{R_3} = \frac{9 - 0.7 + 9\ V}{20\ k\Omega} = 0.865\ mA$$

Therefore

$$I_{C4} = 0.865 - \frac{0.9}{167} = 0.860\ mA$$

Them g_{m4} could be calculated from I_{C4}:

$$g_{m4} = 40 \times I_{C4} = 34.4$$

Similarly, r_{07} and r_{04} are:

$$r_{07} = \frac{V_A}{I_{C7}} = \frac{113}{0.865} = 130.6\ k\Omega$$

$$r_{04} = \frac{V_A}{I_{C4}} = \frac{74}{0.86} = 84\ k\Omega$$

For the input resistance of transistor Q8 R_{iQ8},

$$R_{iQ8} = (1 + \beta)R_2 + r_{\pi 8}$$

Then $r_{\pi 8}$ is desired:

$$r_{\pi 8} = \frac{\beta}{40 \times I_{C8}} = \frac{167}{40 \times 0.895m} = 4.66\ k\Omega$$

Therefore,

$$R_{iQ8} = (1 + 167) * (10) + 4.68 = 1684.68\ k\Omega$$

Finally, A_{v4} could be calculated:

$$A_{v4} = -g_{m4}(r_{07}||r_{o4}||R_{iQ8}) = -1706.74$$

As for the output resistance, it could be also verified as:

$$R_{out} = \frac{(r_{o7}||r_{o4}) + r_{\pi 8}}{\beta + 1}||10k = (\frac{55.78}{168}||10)k = 0.322k\Omega$$

In conclusion, the total voltage gain of this circuit could be verified as:

$$\boldsymbol{A_v = A_{v2} \times A_{v4} = 1296.84 * 1706.74 = 2.21 \times 10^6}$$

$$\boldsymbol{R_{out} = \frac{(r_{o7}||r_{o4}) + r_{\pi 8}}{\beta + 1}||10k = 0.322k\Omega}$$

6. Complete the table below.

Specification	Open loop voltage gain	Input resistance (MΩ)	Output resistance (kΩ)	Current from supply (mA)	Input offset voltage Vos
Specified value	**> 5 x10^5**	**> 0.1MΩ**	**< 1kΩ**	**< 5mA**	**--------**
Measured value	**1.62× 10^6**	**107.824 kΩ**	**321.233 Ω**	**2.922mA**	**-77.213uV**
Calculated value	**2.24× 10^6**	**110.87 kΩ**	**0.321 kΩ**	**2. 919mA**	**---------**

In order to calculate the measured of the open-loop voltage gain, the slope of the middle line in Figure 9 is desired.

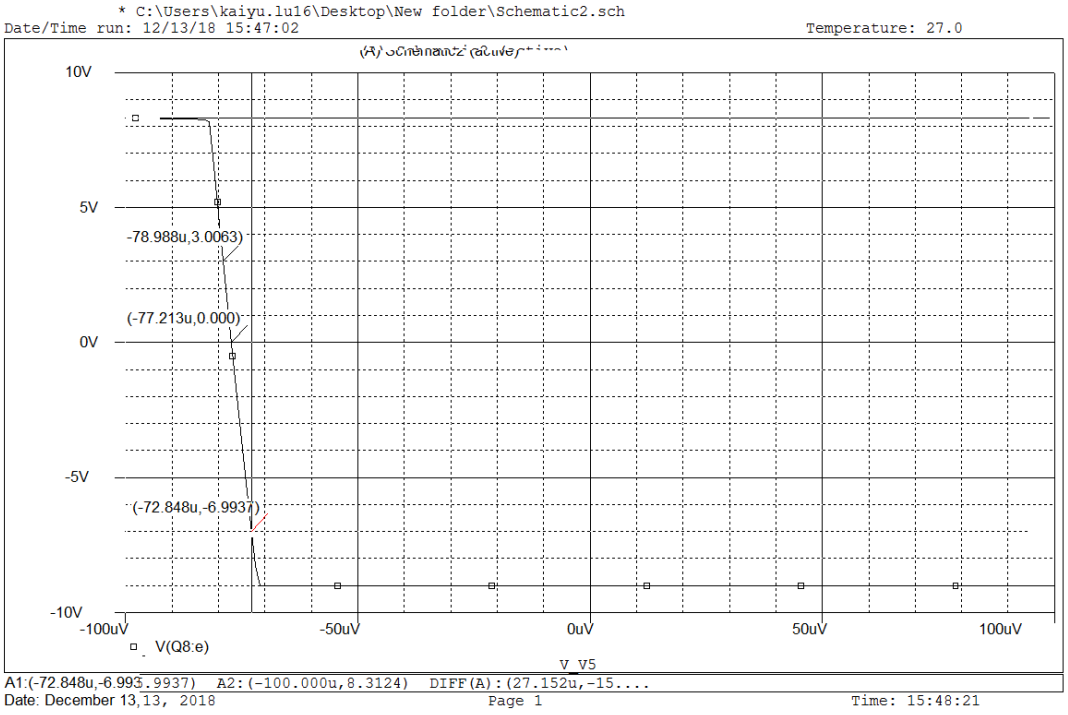

Figure 9: voltage transfer characteristic obtained by simulation (with two more points)

Take two points: (-78.988u, 3.0063) and (-72.848u, -6.9937). Then the slope is -1.62× 10^6. Regarding to the measured input resistance, adding trace should be implemented after simulating and the adding trace formula is: $\frac{V(V4:+)}{IB(Q10)} + \frac{V(V1:-)}{IB(Q2)}$. And Figure 10 the screenshot for the measured input resistance.

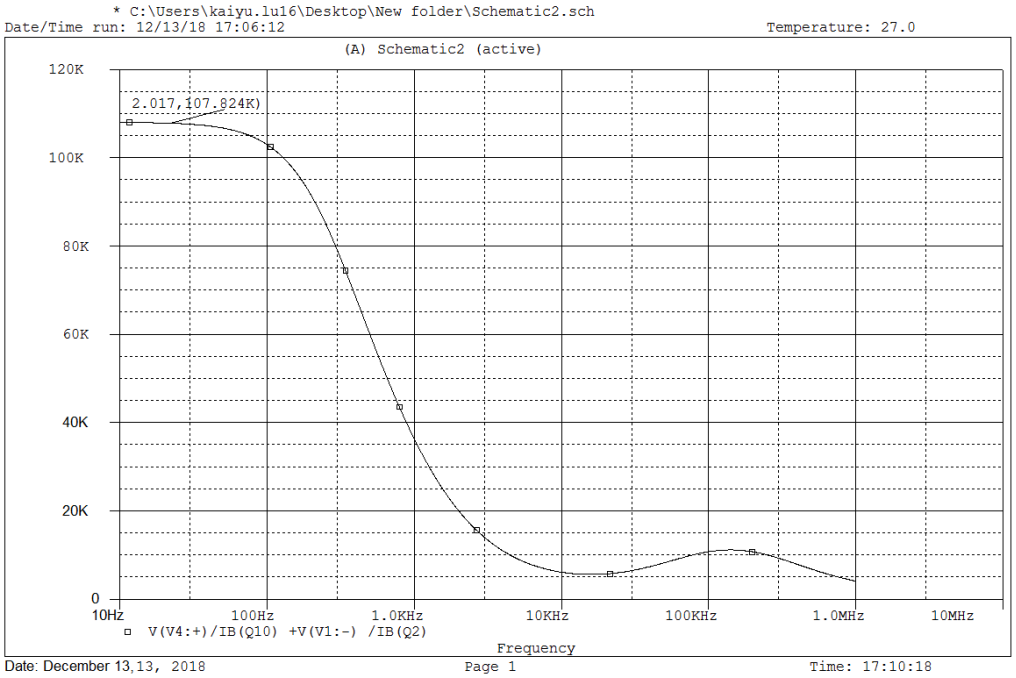

Figure 10: The measured input resistance.

Then Figure 11 is the result of measured output resistance.

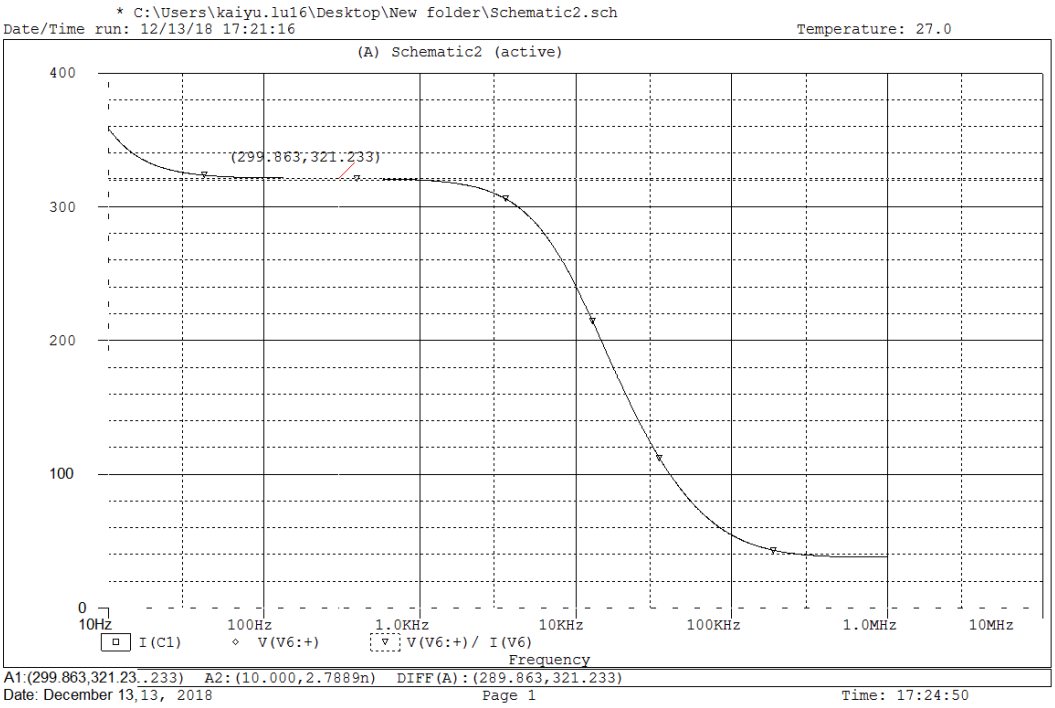

Figure 11: The result of measured output resistance.

For the current from supply is:

$$I_{E:1} + I_{E:9} + I_{C:6} + I_{E:7} + I_{C:8} = 0.855 + 0.234 + 0.018 + 0.911 + 0.901$$
$$= 2.919\,mA$$

For the calculation part, the input resistance is: $\frac{V(V4:+)}{IB(Q10)} + \frac{V(V1:-)}{IB(Q2)}$

$$R_{in} = \frac{V(V4:+)}{IB(Q10)} + \frac{V(V1:-)}{IB(Q2)} = \frac{V(V4:+)}{\frac{I_e(Q10)}{\beta+1}} + \frac{V(V1:-)}{\frac{I_e(Q2)}{\beta+1}}$$

$I_e(Q10)$ and $I_e(Q2)$ could be regarded as the same which is:
0.117 mA.
So,

$$R_{in} = \frac{77.213\mu}{\frac{0.117}{167+1}} + \frac{0\mu}{\frac{0.117}{167+1}} = 110.87\ \text{k}\Omega$$

Compare your measured and calculated values given in the table and account for any significant discrepancies. (10%)

Compared with the measured values and calculated values, they are almost the same. During the calculations, all the parameters are the same as the simulated values. However, the chosen β might be slightly different which might cause the discrepancies. In addition, the voltage gain of the common-collector is theoretically 0.9. However, it is normally assumed as 1 for convenience. Then the temperature is a significant parameter as well. In conclusion, the analysis above are the reasons could cause the discrepancies.

7. ***Give your measured Bode plots***

   (a) log_{10} gain magnitude vs log_{10} frequency, and

   (b) linear phase vs log_{10} frequency

   for the op-amp. What can you deduce about the stability of your amplifier from the Bode plots when it is used in a negative feedback circuit? (15%)

Figure 12: The Bode plot of the log10 gain magnitude vs log10 frequency

Figure 13: The Bode plot of the linear phase vs log10 frequency

The next step was to construct the circuit for negative feedback and it could be shown in Figure 14.

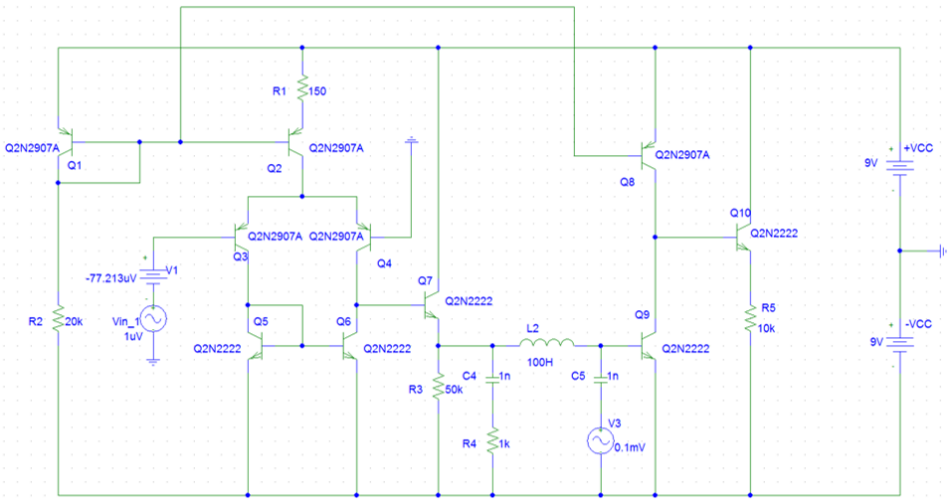

Figure 14: The circuit for negative feedback

Figure 15: The gain in dB.

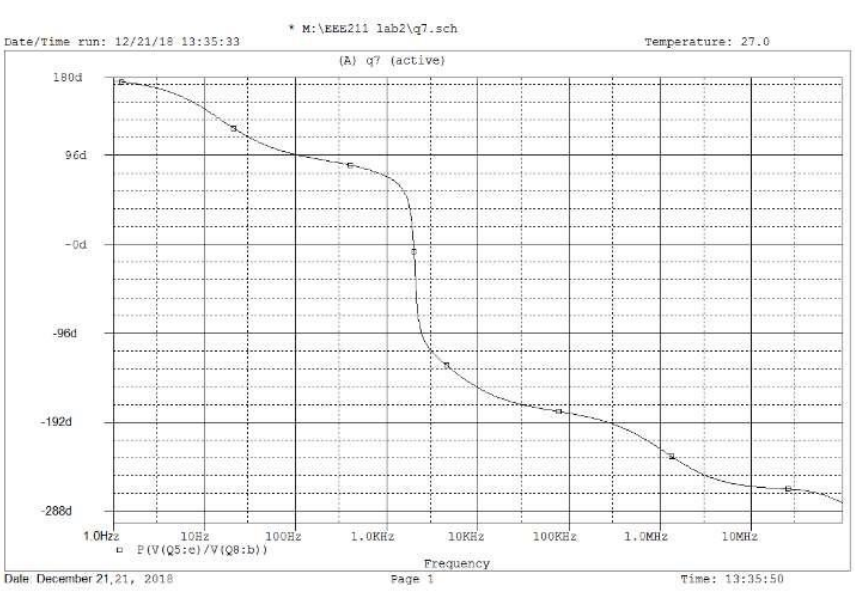

Figure 16: The gain in phase.

8. ***Give your results for the Bode plots obtained with the 'phase compensating capacitor', C_C, added. With reference to these results, comment on how the addition of C_C affects the stability of the op-amp discussed in Question 7. (10%)***

Figure 17 is the simulated result of the modified circuit that a phase compensating capacitor C_C is added.

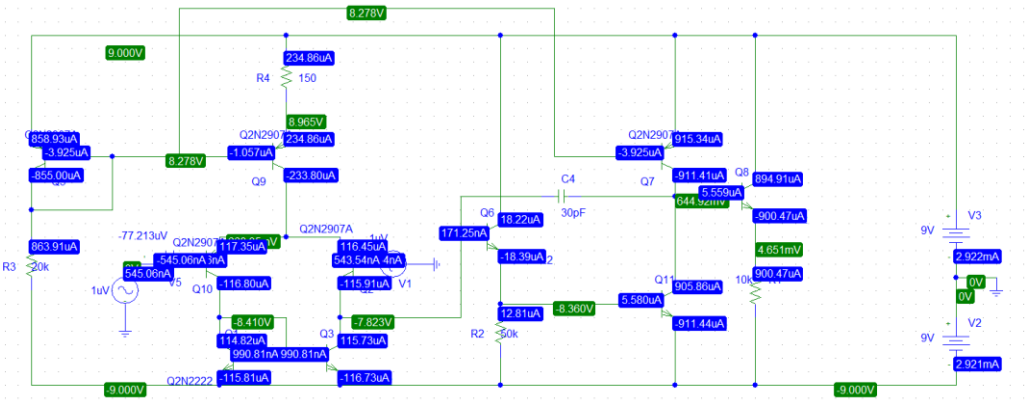

Figure 17: The modified circuit that a phase compensating capacitor C_C added.

Figure 18 is the simulated results after adding trace in order to obtain the Bode plots of gain in dB and of the linear phase.

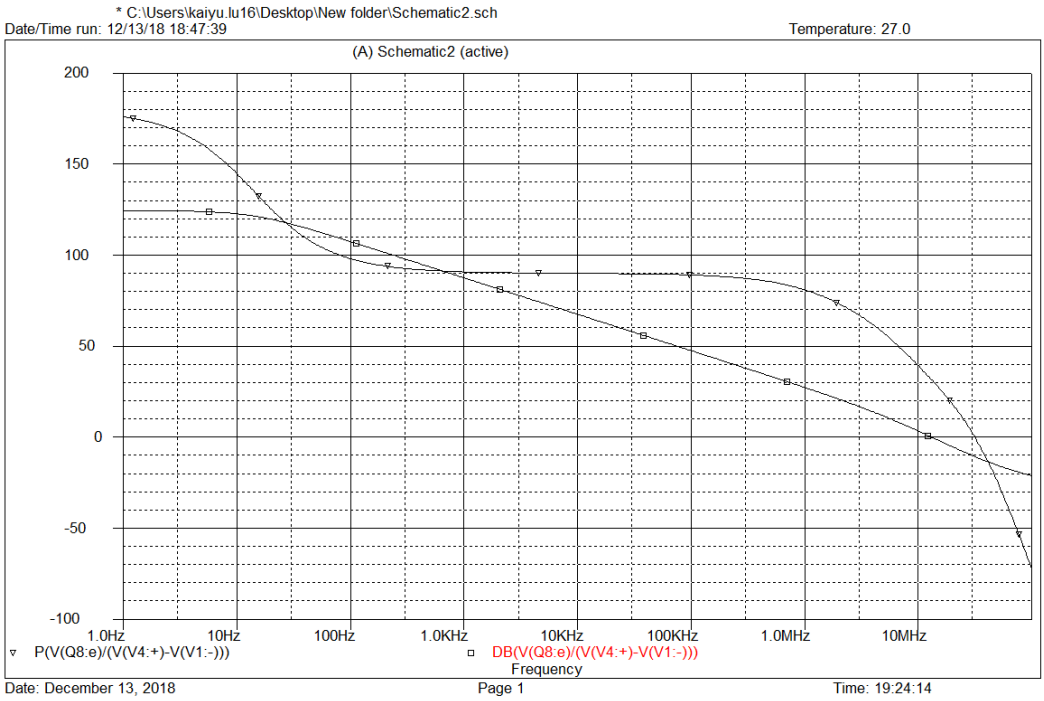

Figure 18: Results for the Bode plots obtained with the 'phase compensating capacitor' added with C_C.

Compared the results of this section and the results of previous section, it could be observed that the stability of the system has been enhanced. After adding the phase compensating capacitor, when the frequency reaches to 100Hz, the magnitude begins changing but the decreasement of phase is less than the previous one. Due to the fact that the phase compensating capacitor could be divided into two capacitors according to the Miller Effect, and the value of the added capacitor is much smaller than the value of the Miller capacitor, which could change the gain.