Xi'an JIAOTONG-LIVERPOOL UNIVERSITY

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COURSEWORK SUBMISSION COVER SHEET

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1. Introduction

MOS is an integrated circuit consisting of metal-oxide-semiconductor. This project required students to design a simple integrated circuit whose circuit is shown in Figure 1 and write a consistent report. During this project, students need to design and observe the MOSIS Layout Design Rules to minimize the layout and masks for each layout. Additionally, the component level of the circuit is indicated in Figure 2.

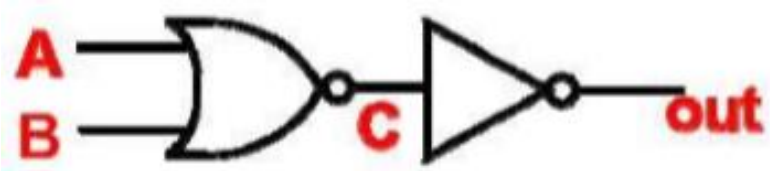


Figure 1: The logic circuit of the OR gate.

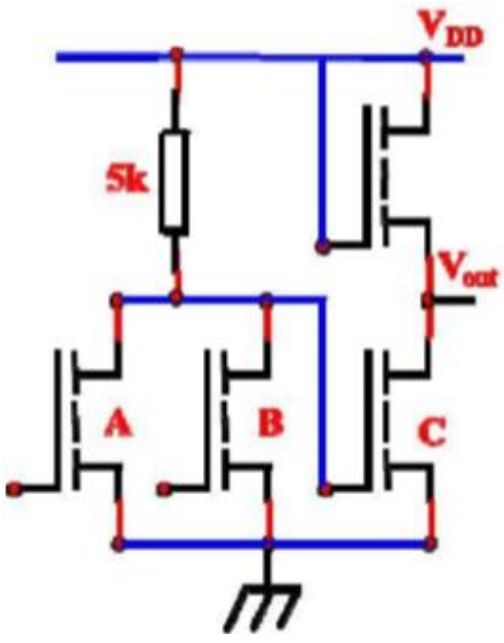


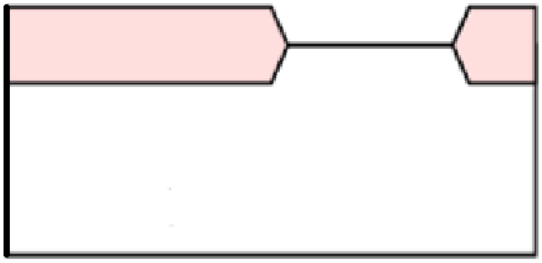
Figure 2: The component level of the OR gate.

2. Fabrication process flow of nMOS ICs and design rules' description.

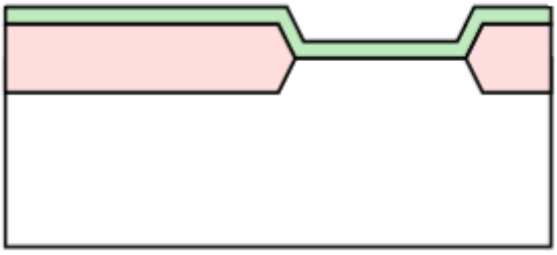
This section will briefly describe the fabrication process flow of nMOS and then provide the design rules.

Below is the process flow:

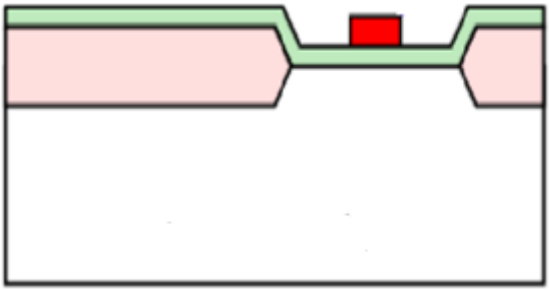
1) Oxidation (Patterning SiO_2 Layer after etching)



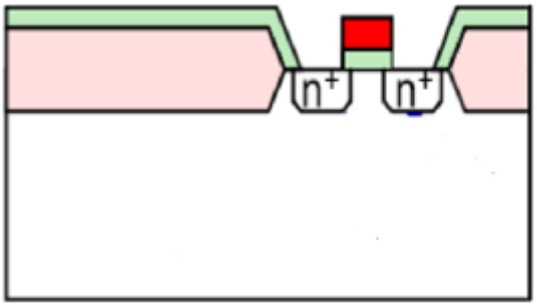
2) SiO_2 Gate Oxide



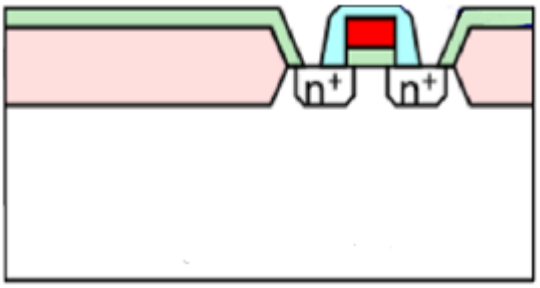
3) Patterning Polysilicon (Polysilicon etching)



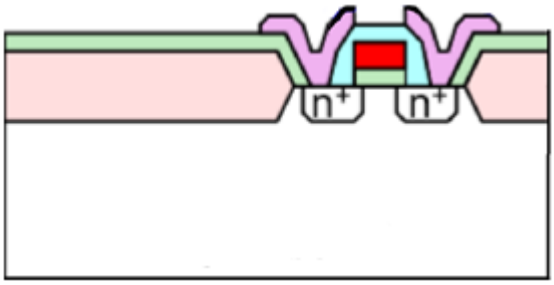
4) Ion implantation after oxide etching (Doping)



5) Oxidation (SiO_2 Insulated Oxide)



6) Patterning metal (Al) layer



According to the above process flow, the first step is to oxidize the original Si to form a thin SiO_2 above the Si. Then, in order to form the pattern on the Si, a key step called etching is significant. After etching, the current surface of the component should be oxidized again. The next step is to deposit the polysilicon and then etching again. After deposing and etching the polysilicon, the next step is to implant ion. Subsequently, the figure of the current component could be referred in 4). The next step is to oxidize and etch the surface and the operated component could be seen in 5). Finally, metal such as Al should be deposited on the surface and then it will be etched again in order to obtain the aimed shape.

The design rules of MOSIS Layout Design are shown below:

MOSIS Layout Design Rules

Active Area Rules		
R1	Minimum Active area Width	3λ
R2	Minimum Active area Spacing	3λ
Poly-Silicon Rules		
R3	Minimum Poly Width	2λ
R4	Minimum Poly Spacing	2λ
R5	Minimum Gate extension of Poly over Active	2λ
R6	Minimum Poly-Active Edge Spacing (Poly Outside of Active area)	λ
R7	Minimum Poly-Active Edge Spacing (Poly Inside of Active area)	3λ
Metal Rules		
R8	Minimum Metal Width	3λ
R9	Minimum Metal Spacing	3λ
Contact Rules		
R10	Poly Contact size	2λ
R11	Minimum Poly Contact Spacing	2λ
R12	Minimum Poly Contact to Poly Edge Spacing	λ
R13	Minimum Poly Contact to Metal Edge Spacing	λ
R14	Minimum Poly Contact to Active Edge Spacing	3λ
R15	Active Contact size	2λ
R16	Minimum Active Contact Spacing (On the same Active region)	2λ
R17	Minimum Active Contact to Active Edge Spacing	λ
R18	Minimum Active Contact to Metal Edge Spacing	λ
R19	Minimum Active Contact to Poly Edge Spacing	2λ
R20	Minimum Active Contact Spacing (On different Active regions)	6λ
Supply Rail Metal		
R21	V_{DD}	>3λ
R22	Ground	>3λ
Resistor Rules		
R23	Minimum resistor width	2λ

Table 1: MOSIS Layout Design Rules [1]

3. Design of the logic circuit.

Table 2 is the truth table of the OR gate.

A	B	C	Out
0	0	1	0
1	0	0	1
0	1	0	1
1	1	0	1

Table 2: The truth table of the OR gate.

During the design of the nMOS, the significant step is to calculate the aspect ratio of W/L. It is therefore the rest of this section is to explain how to calculate W/L.

According to Figure 2, there are two termed driver MOSFETs, which are transistors A and B. Before calculating the W/L of A and B, the process parameters have been given in Table 3.

Normalized Device Constant β_0	$1.8x10^{-4}$ A/V^2
Threshold Voltage V_T	0.3 V
Supply Voltage V_{DD}	5 V
High Input Voltages (A and B) V_{IN}	V_{DD}
Low Input Voltages (A and B) V_{IN}	0 V
MOSFET Load Resistance R_L	5 kΩ
Sheet Resistance R_S	100 Ω/□

Table 3: Process Parameters [1]

Below is the calculation of W/L for A and B.

Due to A and B are parallel, thus it could be assumed that $V_A = V_B = V_{DD}$ and $R_{D//D} = \frac{R_D * R_D}{R_D + R_D} = 0.5R_D$. Then, let $V_B = 0.1V << V_T$.

Potential divider:

$$\frac{R_{D//D}}{R_{D//D}+R_L} = \frac{0.5R_D}{R_D+R_L} = \frac{V_{Out}}{V_{DD}} = \frac{0.1}{5} = 0.02$$

Therefore, $R_D \approx 200\Omega$.

Due to $I_D = \frac{\beta[(V_G-V_T)V_D-V_D^2]}{2} \approx \beta[(V_G - V_T)$,

and $R_D = \frac{V_{Out}}{I_D} = \frac{1}{\beta[(V_G-V_T)} = \frac{1}{\beta(5-0.3)} = 200\Omega$

and $R_D = \frac{V_{Out}}{I_D} = \frac{1}{\beta_0[(V_G-V_T)} * \frac{L}{W} = \frac{1}{\beta[(V_G-V_T)}$,

so $\beta = \frac{W}{L} * \beta_0 = 10^{-3}$.

Therefore, the aspect ratio for both A and B, $\frac{W}{L}$, are 6.

In terms of the aspect ratio of D, it could be assumed as 6 as well. Consequently, the following step is to calculate the aspect ratio of L.

Assuming $V_{in} = V_{DD}$, and let $V_{Out} = 0.1V$.

$$I_D = \frac{\beta[(V_{in} - V_T)V_{Out} - V_{Out}^2]}{2}$$

$$R_D = \frac{V_{Out}}{I_D} = \frac{1}{6\beta_0[(V_{DD} - V_T)} = 200\Omega$$

Therefore, $R_L \approx 10k\Omega$.

Due to $I_D = \frac{\beta_L(V_{DD}-V_T)^2}{2}$,

$\beta_L = \frac{W}{L} * \beta_0 = 4.4 * 10^{-5}$.

Therefore, the aspect ratio of load L, $\frac{W}{L}$, is 0.25.

In conclusion, the aspect ratio of A, B and the transistor connected to V_{Out} are all 6. Additionally, the aspect ratio of L is 0.25.

4. Results and discussion

After obtaining the value of all the aspect ratios, the final step is to design the layout. There are certain tricks to overly minimize the chip area. The first trick is to use metal to let A and B share a same drain which is connected to the resistor. In addition, although the length and width for each transistor is fixed (proportional), it is determined to make the size to the most minimized. Normally, $\mathrm{V_{Out}}$ is large smaller than $\mathrm{V_T}$, of which value is about 0.1V. Similarly, if $\mathrm{V_{Out}}$ becomes 0.01V, it could be also accepted. However, previously it has just concerned about the situation that A = B, which is << V_T. Below will discuss the worst case and other cases.

Assuming A =1 and B =0 or A = 0, B = 1.

$$\text{So } \mathrm{V_{Out}} = \mathrm{V_{DD}} * \frac{\mathrm{R_D}}{\mathrm{R_D}+5\mathrm{K}} = 0.2\mathrm{V}$$

Another case is when A = 1 and B = 1.

$$\text{So } \mathrm{V_{Out}} = \mathrm{V_{DD}} * \frac{\mathrm{R_D}}{\mathrm{R_D}+5\mathrm{K}} = 0.01\mathrm{V}$$

As for the influence of $\mathrm{V_{Out}}$ on the size of the drivers, $\mathrm{R_D}$ is determined by $\mathrm{V_{Out}}$, and, $\mathrm{V_{Out}}$ is related to β which divided by β_0 is $\frac{\mathrm{W}}{\mathrm{L}}$. Therefore, if V_{Out} increases, $\frac{\mathrm{W}}{\mathrm{L}}$ will increase as well, which means the width would be longer and the shape of the driver would flat.

5. Conclusion

From this project, students have understood the manufacturing processes of nMOSFETs and design process of ICs. In addition, students have known how to design the layout and masks for each layout according the MOSIS Layout Design Rules. Moreover, a more significant procedure is to calculate the aspect ratio of each transistor, so that the rest design could be conducted. In conclusion, this project commendably makes students know how the digital logic circuit combines with semiconductor, such as the internal architecture of each logic component and its working principles and

manufacturing processes.

6. References

[1] *EEE112 Integrated Electronics and Design nMOS IC Design Project*, XJTLU, Suzhou, Jiangsu, 2018.