EEE 104 Digital Electronics

Assessment 4
Laboratory Report

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Catalogue:

1. Section 1: Tests of Basic Logic Gates

1.1 Introduction of NOT gates

NOT gate is also called inverter which is the basic unit of the logic circuit, and its distinctive shape symbol is shown in Figure 1. NOT gate consists of an input and an output. When the input terminal is HIGH (Logic 1), the output terminal is LOW (Logic 0). When the input terminal is LOW (Logic 0), the output terminal is HIGH (Logic 1). The first part of this section required students to use 74LS04 to test the characteristic of NOT gate.

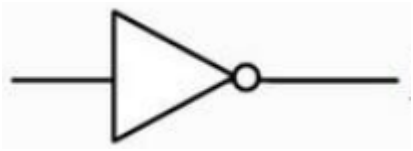


Figure 1: Distinctive shape symbol of NOT gate.

1.1.1 Boolean expression and truth table

Boolean expression of NOT gate: $X = \bar{A}$

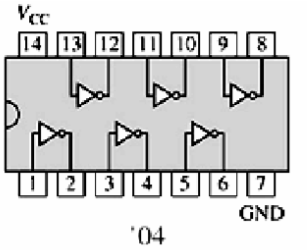
Below is the truth table of NOT gate.

Input	Output
1 (HIGH)	0 (LOW)
0 (LOW)	1 (HIGH)

Table 1: The truth table of NOT gate.

1.1.2 Experimental procedure

The first step was to fix the component 74LS04 on the breadboard whose chip diagram is shown in Figure 2.



7404(NOT)

Figure 2: Chip diagram of NOT gate

Then, a DC voltage supply was set to +5V which should be connected to V_{CC}. Meanwhile, PIN 7 should be connected to GND. Although one 74LS04 has 6 NOT gates, here it was just needed to use one of them. The next step was to connect the input terminal to +5V and connect the output terminal to the GND. Then, students used a multimeter to test the voltage on the output terminal and record the data on it. Similarly, the next step was to connect the input terminal to GND and connect the output terminal to +5V. Then, students used a multimeter to test the voltage on the output terminal and record the data on it.

1.1.3 Observation, explanation and conclusion

After the experiment, the recorded data should be arranged, and they are indicated in Table 2.

Input	Output
+5 V	174.5mV
0V	4.48V

Table 2: The results of recorded data.

Compared Table 2 with Table 1, it could be concluded that this experiment was successful. During this experiment, +5V represents 1 (HIGH) and 0V represents 0 (LOW). Due to the experimental error,

the voltage of output is 174.5 mV could be regarded as 0V and the voltage of input is 4.48V could be regarded as 5V when the input terminal is HIGH. Form this experiment, it could be summarized two rules of NOT gate:

1) If the input is HIGH, the output will be LOW.
2) If the input is LOW, the output will be HIGH.

1.2 Introduction of the 2-input AND gates

AND gate is also one of the basic units of the logic circuit, and its distinctive shape symbol is shown in Figure 3. AND gate consists of two inputs and an output. During this report, A and B will represent the inputs of the AND gate and X will represent the output. The second part of this section required students to use 74LS08 to test the characteristic of AND gate.

Figure 3: Distinctive shape symbol of AND gate.

1.2.1 Boolean expression and truth table

Boolean expression of AND gate: $X = AB$.

Below is the truth table of AND gate.

A	B	X =AB
1 (HIGH)	1 (HIGH)	1 (HIGH)
1 (HIGH)	0 (LOW)	0 (LOW)
0 (LOW)	1 (HIGH)	0 (LOW)
0 (LOW)	0 (LOW)	0 (LOW)

Table 3: The truth table of AND gate.

1.2.2 Experimental procedure

The first step was to fix the component 74LS08 on the breadboard whose chip diagram is shown in Figure 4.

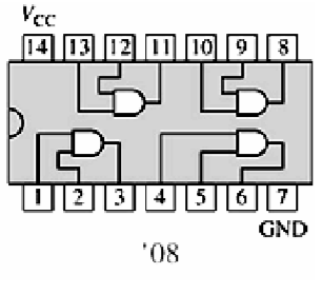


Figure 4: Chip diagram of AND gate

Then, a DC voltage supply was set to +5V which should be connected to V_{CC}. Meanwhile, PIN 7 should be connected to GND. Although one 74LS08 has 4 AND gates, here it was just needed to use one of them. In order to obtain the analog result, this experiment was divided into 4 different stages. The first stage was to connect both A and B to the +5V. The second stage was to connect A to +5V and B to GND. The third stage was to connect B to +5V and A to GND. The fourth stage was to connect both A and B to GND. At the end of each stage, a multimeter was used to measure the voltage of output terminal.

1.2.3 Observation, explanation and conclusion

After the experiment, the recorded data should be arranged, and they are indicated in Table 4.

A	B	X =AB
+5V	+5V	4.39V
+5V	0V	124.4mV
0V	+5V	143.6mV
0V	0V	144.2mV

Table 4: The results of recorded data.

Compared Table 4 with Table 3, it could be concluded that this experiment is successful. Due to the experimental error, the outputs of the second, the third and the fourth stage could be assumed as 0V and the output of the first stage could be assumed as +5V.

Form this experiment, it could be summarized two rules of AND gate:

1) If all inputs are HIGH, the output will be HIGH.
2) If any input is LOW, the output will be LOW.

1.3 Introduction of the 2-input NOR gates

NOR gate is also one of the basic units of the logic circuit, and its distinctive shape symbol is shown in Figure 5. NOR gate consists of two inputs and an output. During this report, A and B will represent the inputs of the NOR gate and X will represent the output. The third part of this section required students to use 74LS02 to test the characteristic of NOR gate.

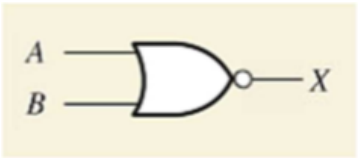


Figure 5: Distinctive shape symbol of NOR gate.

1.3.1 Boolean expression and truth table

Boolean expression of NOR gate: $\mathrm{X} = \overline{\mathrm{A} + \mathrm{B}}$.

Below is the truth table of NOR gate.

A	B	$\mathrm{X} = \overline{\mathrm{A} + \mathrm{B}}$
1 (HIGH)	1 (HIGH)	0 (LOW)
1 (HIGH)	0 (LOW)	0 (LOW)
0 (LOW)	1 (HIGH)	0 (LOW)
0 (LOW)	0 (LOW)	1 (HIGH)

Table 5: The truth table of NOR gate.

1.3.2 Experimental procedure

The first step was to fix the component 74LS02 on the breadboard whose chip diagram is shown in Figure 6.

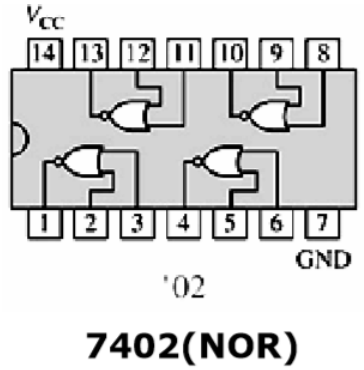


Figure 6: Chip diagram of NOR gate

Then, a DC voltage supply is set to +5V which should be connected to V_{CC}. Meanwhile, PIN 7 should be connected to GND. Although one 74LS08 has 4 AND gates, here it was just needed to use one of them. In order to obtain the analog result, this experiment was divided into 4 different stages. The first stage was to connect both A and B to the +5V. The second stage was to connect A to +5V and B to GND. The third stage was to connect B to +5V and A to GND. The fourth stage was to connect both A and B to GND. At the end of each stage, a multimeter was used to measure the voltage of output terminal.

1.3.3 Observation, explanation and conclusion

After the experiment, the recorded data should be arranged, and they are indicated in Table 6.

A	B	$X = \overline{A + B}$
+5V	+5V	148.6mV
+5V	0V	184.5mV
0V	+5V	161.4mV
0V	0V	4.44V

Table 6: The results of recorded data.

Compared Table 6 with Table 5, it could be concluded that this experiment is successful. Due to the experimental error, the outputs of the first, the second and the third stage could be assumed as 0V and the output of the fourth stage could be assumed as +5V. Form this experiment, it could be summarized two rules of AND gate:

1) If all inputs are LOW, the output will be HIGH.
2) If any input is HIGH, the output will be LOW.

2. Section 2: DE Morgan's Theorem

2.1 Introduction of DE Morgan's Theorem

This section intends to prove DE Morgan's Theorem which is indicated in Figure 7 by using NAND gate and Negative-AND gate. Form Section 1, it has been verified the characteristics of NOR gate, AND gate and NOT gate. In terms of Negative-AND gate, it consists of two inputs of each side has one NOT gate and one output. As for the NAND gate, it consists of two inputs and one output which is connected to a NOT gate.

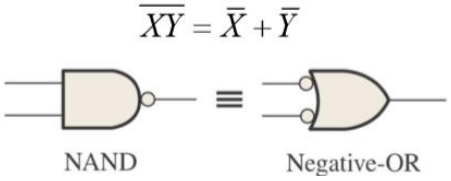


Figure 7: DE Morgan's Theorem

2.2 Boolean expression and truth table

Boolean expression of DE Morgan's Theorem: $\overline{XY} = \overline{X} + \overline{Y}$.

Below is the truth table of DE Morgan's Theorem.

Input		Output	
X	Y	$\overline{XY}$	$\overline{X} + \overline{Y}$
0 (LOW)	0 (LOW)	1 (HIGH)	1 (HIGH)
0 (LOW)	1 (HIGH)	1 (HIGH)	1 (HIGH)
1 (HIGH)	0 (LOW)	1 (HIGH)	1 (HIGH)
1 (HIGH)	1 (HIGH)	0 (LOW)	0 (LOW)

Table 7: The truth table of DE Morgan's Theorem

2.3 Experimental procedure

This section was divided into 2 parts. The first was to obtain the result of NAND gate. The second part was to obtain the result of Negative-AND gate. In addition, each part had four stages which are detailed below.

The first stage was to connect both A and B to the +5V. The second stage was to connect A to +5V and B to GND. The third stage was to connect B to +5V and A to GND. The fourth stage was to connect both A and B to GND. At the end of each stage, a multimeter was used to measure the voltage of output terminal.

2.4 Observation explanation and conclusion

After the experiment, the recorded data should be arranged, and they are indicated in Table 8.

Input		Output	
X	Y	$\overline{XY}$	$\overline{X} + \overline{Y}$
+5V	+5V	169.7mV	151.4mV
+5V	0V	4.47V	4.45V
0V	+5V	4.52V	4.62V
0V	0V	4.49V	4.51V

Table 8: The results of recorded data

From Table 8, it could be observed that $\overline{XY}$ is equal to $\overline{X} + \overline{Y}$, which is the same result in Table 7. Due to the existence of experimental error, if the result is very closed to 0V, it could be assumed as 0V; if the result is very closed to 5V, it could be assumed as 5V. Therefore, it could be concluded that this experiment is successful. From this section, DE Morgan's Theorem was accurately and properly proved, of which Boolean expression is: $\overline{XY} = \overline{X} + \overline{Y}$.

3. Section 3: Combinational Logic Circuits

3.1 Introduction of Combinational Logic Circuits

This section will apply combinational logic circuits to an instance. The instance is described below.

"Consider the logic statement: 'If Mary obtains permission from her mother or her father and if Joe or Tom pick her up, she may go to the cinema'. This statement may be expressed as a Boolean equation using the following Boolean variables:

F = Mary will go to the cinema (true/false)
A = Her mother will give her permission (true/false)
B = Her father will give her permission (true/false)
C = Joe will pick her up (true/false)
D = Tom will pick her up (true/false)

Then F = (A+B)·(C+D) is the Boolean equation that describes this statement. Implement the circuit for this logic equation and complete the Truth Table." [1].

In order to simulate this instance, two OR gates and one AND gate would be used during this experience. One OR gate was used for (A+B), and the other OR gate was used for (C+D). The AND gate was used for F = (A+B)·(C+D).

3.2 Boolean expression and truth table

Boolean expression of this combinational logic circuit: F = (A+B)·(C+D).

Below is the truth table of this combinational logic circuit.

A	B	C	D	F=(A+B)·(C+D).
0	0	0	0	0
0	0	1	0	0
0	0	0	1	0
0	0	1	1	0
1	0	0	0	0
1	0	1	0	1
1	0	0	1	1
1	0	1	1	1
0	1	0	0	0
0	1	1	0	1
0	1	0	1	1
0	1	1	1	1
1	1	0	0	0
1	1	1	0	1
1	1	0	1	1
1	1	1	1	1

Table 9: The truth table of the combinational logic circuit.

3.3 Experimental procedure

In order to obtain F, students should construct the circuit shown below.

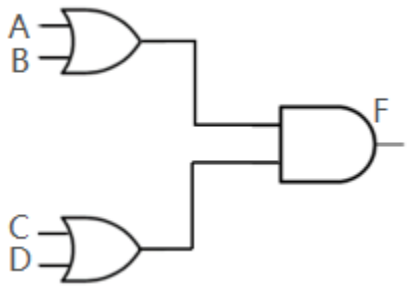


Figure 8: The circuit of F.

After having constructed the circuit, students should check if V_{CC} had

been connected to +5V and if PIN 7 had been connected to GND. The rest steps were to obtain 16 groups as shown in Table 9. However, the terminals should be connected to +5V if the value is 1 in Table 9. Similarly, the terminal should be connected to GND if the value is 0 in Table 9. At the end of each steps, a multimeter was used to measure the voltage of output terminal which is F.

3.4 Observation explanation and conclusion

After the experiment, the recorded data should be arranged, and they are indicated in Table 10.

A	B	C	D	F=(A+B)·(C+D).
0	0	0	0	0.127V
0	0	+5V	0	0.118V
0	0	0	+5V	0.128V
0	0	+5V	+5V	0.131V
+5V	0	0	0	0.209V
+5V	0	+5V	0	4.550V
+5V	0	0	+5V	4.577V
+5V	0	+5V	+5V	4.535V
0	+5V	0	0	0.126V
0	+5V	+5V	0	4.663V
0	+5V	0	+5V	4.378V
0	+5V	+5V	+5V	4.466V
+5V	+5V	0	0	0.121V
+5V	+5V	+5V	0	4.534V
+5V	+5V	0	+5V	4.562V
+5V	+5V	+5V	+5V	4.453V

Table 10: The results of recorded data

Compared Table 10 with Table 9, it could be observed that they are

corresponding. It is therefore this experiment is a success. From this section, it could be concluded that the combinational logic circuit observed the rules:

a) The numbers in the brackets are prior to calculate.
b) If there is no bracket between two numbers, these two number are prior to calculate.

4. Section 4: Implementation of a Half Adder

4.1 Introduction of the Half Adder.

The Half Adder can add two input bits and produces a sum and an output carry. For example, the formulas are the basic rules of binary addition.

$$0 + 0 = 0$$

$$0 + 1 = 1$$

$$1 + 0 = 1$$

$$1 + 1 = 10$$

According to Figure 9, it is the circuit of a Half Adder, A and B represent inputs and $\sum$ and C_{out} are outputs.

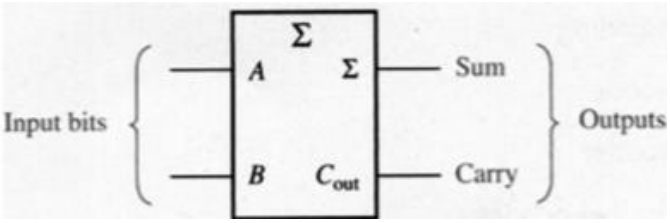


Figure 9: The circuit of the Half Adder

In Figure 9, $\sum$ is the sum of $\overline{A}B + A\overline{B}$ and C_{out} is equal to AB. Therefore, the Half Adder could be also represented by the circuit in Figure 10.

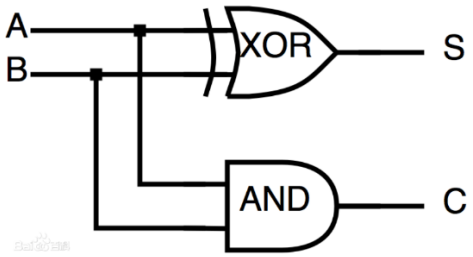


Figure 10: The Half Adder

4.2 Boolean expression and truth table

Boolean expression of the Half Adder: $\sum = \overline{A}B + A\overline{B}$

$C_{out} = AB$

Below is the truth table of the Half Adder.

A	B	$C_{out} = AB$	$\sum = \overline{A}B + A\overline{B}$
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Table 11: The truth table of the Half Adder

4.3 Experimental procedure

During this experiment, one 74LS86 and one 74LS08 would be used. Firstly, students should construct the circuit shown in Figure 10. Additionally, for all components, PIN 14 should be connected to +5V and PIN 7 should be connected to GND. In order to obtain the analog result, this experiment was divided into 4 different stages. The first stage was to connect both A and B to the +5V. The second stage was to connect A to +5V and B to GND. The third stage was to connect B to +5V and A to GND. The fourth stage was to connect both A and B to GND. At the end of each stage, a multimeter was used to measure the voltage of output terminals, which were terminal $\sum$ and

terminal C_{out}.

4.4 Observation explanation and conclusion

After the experiment, the recorded data should be arranged, and they are indicated in Table 12.

A	B	C_{out} = AB	$\sum = \overline{A}B + A\overline{B}$
0	0	147.4mV	147.9mV
0	+5V	145.8mV	4.39V
+5V	0	148.6mV	4.43V
+5V	+5V	4.69V	119.5mV

Table 12: The results of recorded data

Compared Table 12 with Table 1, it could be observed that they are corresponding. It is therefore this experiment is a success. From this section, it could be concluded that the combinational logic circuit observed the rules:

a) For XOR operation: If the inputs are different, their sum is 1, otherwise their sum is 0.
b) For AND operation: When both the inputs are 1, the output carry is 1.

However, one of the limitations of the Half Adder is lacking an input carry. In reality, it is challenging for Half-Add to add two ten digits. Consequently, another adder called Full-Adder which is shown in Figure 11 is suitable for all addition operations because it has the input carry.

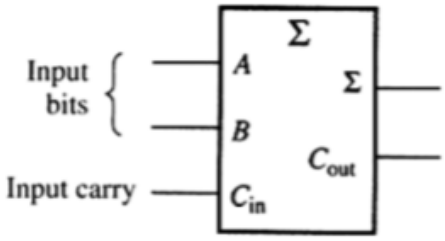


Figure 11: The Full-Adder

5. Section 5: The S-R Latch

5.1 Introduction of the S-R Latch

The S-R Latch is a bistable logic chip. It can realize the function of storing a bit. There are two inputs and two outputs in a S-R Latch. A S-R Latch consists of two NOR gates, each of their output terminal is connect to the different input terminal.

5.2 Boolean expression and truth table

Below is the truth table of the S-R latch with active-HIGH inputs.

Q_n	$\overline{Q_n}$	R	S	Q_{n+1}	$\overline{Q_{n+1}}$
0	1	0	0	0	1
1	0	0	0	1	0
0	1	0	1	1	0
1	0	0	1	1	0
0	1	1	0	0	1
1	0	1	0	0	1
0	1	1	1	X	X
1	0	1	1	X	X

Table 13: The truth table of the S-R latch with active-HIGH inputs

5.3 Experimental procedure

The first step was to construct the circuit shown in Figure 12.

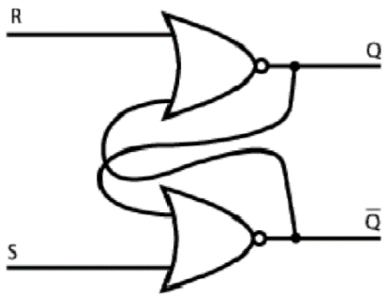


Figure 12: The circuit of the S-R Latch

After having constructed the circuit, students should check that V_{CC} had been connected to +5V and PIN 7 had been connected to GND. In addition, both the output terminals should be connected to an LED and a 330Ω resistor. Here, the function of the resistor is to protect the circuit. However, the terminals should be connected to +5V if the value is 1 in Table 12. Similarly, the terminal should be connected to GND if the value is 0 in Table 12. If the LED on the terminal $\mathrm{Q_n}$ was on, the value in the table would be 1 correspondingly, so was the situation for $\overline{\mathrm{Q_n}}$. $\mathrm{Q_{n+1}}$ and $\overline{\mathrm{Q_{n+1}}}$ are the values after students changed the state of S and R. Due to the value of $\mathrm{Q_{n+1}}$ is influenced be the state of S, R and $\mathrm{Q_n}$, this experiment would need to make $\mathrm{Q_n}$ across equals to 0 and 1. Therefore, students should vary the inputs R and S between 0V and +5V. However, different from previous sections, there was no need to use the multimeter to measure the voltage on the output terminal.

5.4 Observation explanation and conclusion

After marking the results, it was discovered that the result was the same as Table 13. Therefore, this experiment was successful. During this experiment, it was convenient to record the data by observing the state of the LED and recorded the values. The type of this latch the S-R latch with active-HIGH inputs. According to the result shown in Table

13, it could be summarized the following work principle.

a) When S = R = 0, then $\mathrm{Q_n}$ and $\overline{\mathrm{Q_n}}$ will not change.

b) When S = 0 and R = 1, then $\mathrm{Q_n}$ will become 0 and $\overline{\mathrm{Q_n}}$ will become 1. If $\mathrm{Q_n}$ = 0 and $\overline{\mathrm{Q_n}}$ = 1 originally, they will not change.

c) When S = 1 and R = 0, then $\mathrm{Q_n}$ will become 1 and $\overline{\mathrm{Q_n}}$ will become 0. If $\mathrm{Q_n}$ = 1 and $\overline{\mathrm{Q_n}}$ = 0 originally, they will not change.

d) However, S and R could not be 1 at the same time, because the delay time of two NOR gates cannot be determined. Therefore, $\mathrm{Q_n}$ and $\overline{\mathrm{Q_n}}$ are difficult to be determined.

6. Section 6: The Edge-Triggered D Flip-Flop

6.1 Introduction of the Edge-Triggered D Flip-Flop

The Flip-Flop is a component which has two stable state information storage device and has the functions of memorizing. The Edge-Triggered D Flip-Flop is one of the types of the Flip-Flop. The Edge-Triggered D Flip-Flop changes in front of the CLK pulse (0 to 1). In addition, the second state of the trigger depends on the state D terminal before the rising edge of the CLK pulse. The Edge-Triggered D Flip-Flop is multipurpose in numerous components, such as shift resisters, waveform generator and frequency division. Therefore, this section intends to test the characteristic of the Edge-Triggered D Flip-Flop.

6.2 Boolean expression and truth table

Below is the truth table of the Edge-Triggered D Flip-Flop.

Q_n	$\overline{Q_n}$	D	Q_{n+1}	$\overline{Q_{n+1}}$
0	1	0	0	1

1	0	0	0	1
0	1	1	1	0
1	0	1	1	0

Table 14: The truth table of the Edge-Triggered D Flip-Flop

6.3 Experimental procedure

The first step was to construct the circuit as shown in Figure 13.

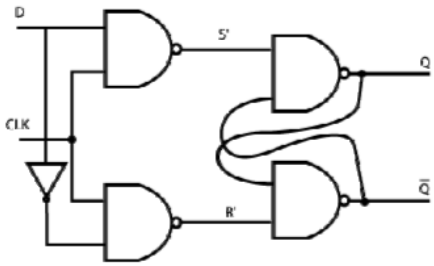


Figure 13: The circuit of the Edge-Triggered D Flip-Flop

After having constructed the circuit, students should check that V_{CC} had been connected to +5V and PIN 7 had been connected to GND. In addition, both the output terminals should be connected to an LED and a 330Ω resistor. Here, the function of the resistor is to protect the circuit. However, the terminals should be connected to +5V if the value is 1 in Table 14. As for the CLK, it should be used another to connect. If CLK needed to be 1, it should be connected to +5V. Therefore, students should operate it by hands. If the LED on the terminal $\mathrm{Q_n}$ was on, the value in the table would be 1 correspondingly, so was the situation for $\overline{\mathrm{Q_n}}$. $\mathrm{Q_{n+1}}$ and $\overline{\mathrm{Q_{n+1}}}$ are the values after students changed the state of D. Due to the value of $\mathrm{Q_{n+1}}$ is influenced be the state of D and $\mathrm{Q_n}$, this experiment would need to make $\mathrm{Q_n}$ across equals to 0 and 1. Therefore, students should vary the inputs R and S between 0V and +5V.

6.4 Observation explanation and conclusion

After marking the results, it was discovered that the result was the same as Table 14. Therefore, this experiment was successful.

From this experiment, it could be summarized that the value of Q_{n+1} is equal to the value of D.

There are two NAND gates individually before S and R. It is therefore if CLK = 0, no matter what the value of D, S will be 1, so is the condition for R. Below is the condition that CLK is 1. If D = 0, S will be 1 and R will be 0, thus Q_{n+1} will be 0. If D = 1, S will be 0 and R will be 1, thus Q_{n+1} will be 1. Consequently, it could be discovered that the value of Q_{n+1} is equal to D.

7. Section 7: The Asynchronous Counter

7.1 Introduction of the Asynchronous Counter

Every Asynchronous Counter has one Edge-Triggered D Flip-Flop. This section intends to use three Edge-Triggered D Flip-Flops to construct a 3-Bit Asynchronous Binary Counter. The circuit shown in Figure 14 would be used during this experiment. This circuit could store one bit for every CLK cycle, consequently, it could count from 0 to 7.

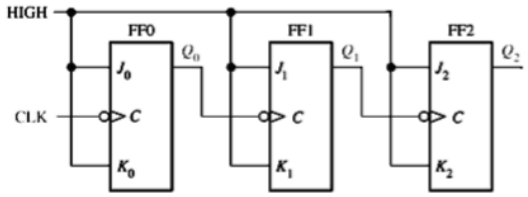


Figure 14: The circuit of 3-Bit Asynchronous Binary Counter

7.2 Boolean expression and truth table

Below is the truth table of the 3-Bit Asynchronous Binary Counter.

	Q_0	Q_1	Q_2

1	0	0	0
2	1	0	0
3	0	1	0
4	1	1	0
5	0	0	1
6	1	0	1
7	0	1	1
8	1	1	1
9	0	0	0
10	1	0	0
etc…	…	…	…

Table 15: The truth table of the 3-Bit Asynchronous Binary Counter

7.3 Experimental procedure

The first step was to construct the circuit shown in Figure 14. Before connecting HIGH to +5V, students should use function generator to apply the CLK pulses (1~2Hz). At the terminals Q_0, Q_1 and Q_2 should be connected with an LED and a 330Ω resistor. The next step was to turn the switch and record the results. If the LED on the terminal were on, the corresponding terminal should be marked in 1. If the LED on the terminal were off, the corresponding terminal should be marked in 0.

7.4 Observation explanation and conclusion

After marking the results, it was discovered that the result was the same as Table 15. Therefore, this experiment was successful.

From Table 15, it could be discovered that three Edge-Triggered D Flip-Flops could realize a 3-Bit Asynchronous Binary Counter. In other words,

it could count from 0 to 7 in decimal (000 to 111 in binary). Q_0 is LSB and Q_2 is MSB.

Due to the influences of CLK cycle and delay, this experience presents the phenomenon that three LEDs will be on regularly, of which the description could be seen in Table 15. In addition, there are 2^N states that this kind of counter have for N flip-flops.

8. Section 8: The Shift Register

8.1 Introduction of the Shift Register

Every Shift Resister consists of a series of cascaded flip-flops which have functions to more and store data. Figure 15 could show the types of shifting.

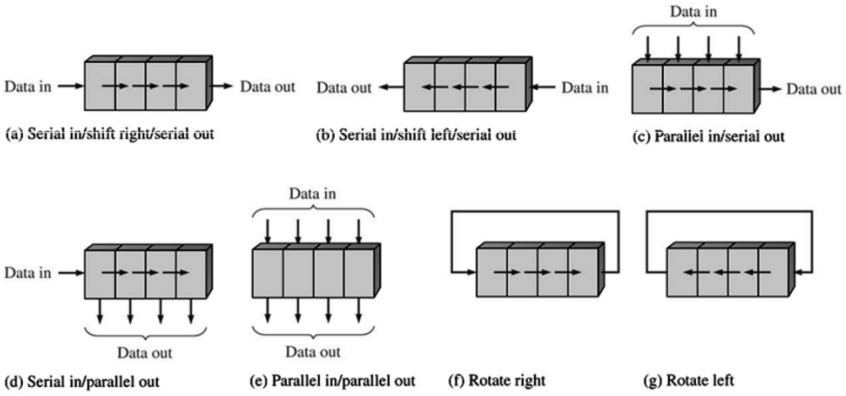


Figure 15: Types of shifting

During this experiment, one of the types of counters was used which is called the Johnson counter, of which the circuit is shown in Figure 16. This section intends to test the characteristic of the Shift Register by using Johnson counter.

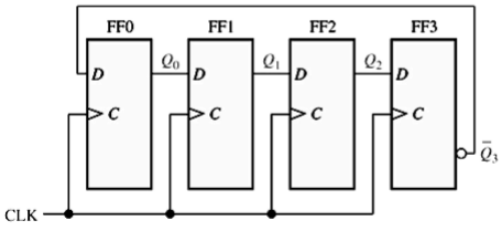


Figure 16: The circuit of the Johnson Counter

8.2 Boolean expression and truth table

Below is the truth table of the Johnson counter.

CLK	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

Table 16: The truth table of the Johnson counter

8.3 Experimental procedure

The first step was to construct the circuit shown in Figure 16. Before connecting HIGH to +5V, students should use function generator to apply the CLK pulses (1~2Hz). At the terminals Q_0, Q_1, Q_2 and Q_3 should be connected with an LED and a 330Ω resistor. The next step was to turn the switch and record the results. If the LED on the terminal were on, the corresponding terminal should be marked in 1. If the LED on the terminal were off, the corresponding terminal should be marked

in 0. Every change during the test, it means the stage of CLK changes orderly.

8.4 Observation explanation and conclusion

After marking the results, it was discovered that the result was the same as Table 16. Therefore, this experiment was successful.

From Table 16, it could be observed that 1 would gradually occupy each output terminal. After all the output terminals are occupied by 1, the next rising CLKs would change the output terminals to 0 from left to right, of which the description could be referred in Table 16. From this experiment, it has tested the characteristic of the Shift Resister. Table 16 indicates that the Shift Resister could store and move the data by using 0 and 1.

9. Conclusion

In this part, it will not list all the results for every section because they have been explained and concluded previously but it will comment other aspects. From this experiment, students have leant how to use equipment to test the knowledge on the lectures. 74LS00, 74LS02, 74LS04, 74LS08, 74LS32, 74LS86, 7474 and 74112 were all used during this experiment. Additionally, there are many identical gates in each chip, which is without the imagination of students. There were many mistakes that students make during the experiment, such as poor connecting and misunderstanding the meaning of the requirements. Fortunately, our group successfully finished every section.

During this experiment, one significant item is the teamwork. Group members took turns to construct the circuit and others check the accuracy of it. In addition, if we could not figure out the right results, we would ask

TAs. During this experiment, TAs were all quite kind, patient and helpful. Although they were busy helping most students in the lab, they would explain the purposes, procedures and principles of sections in this experiment.

Before the lab, both group members had read through the whole material and leant the knowledge existed in every section, which was the key to finish the lab accurately. In conclusion, although this lab was long, the operations and contents were quite abundant and academic. Therefore, most students gave remarkable comments to this lab.

10. Reference

[1] *EEE104 - Digital Electronics Laboratory Manual*, XJTLU, Suzhou, Jiangsu, 2018.