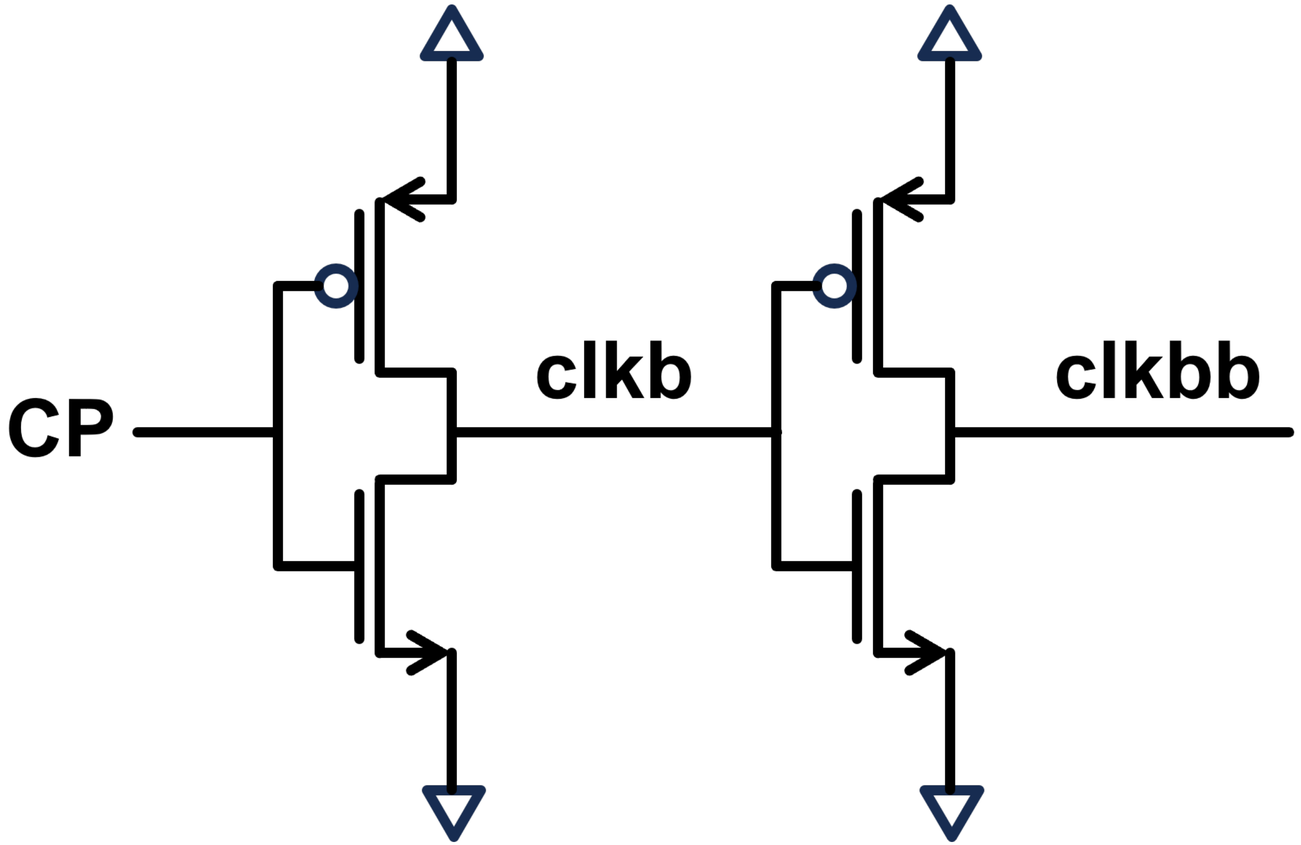
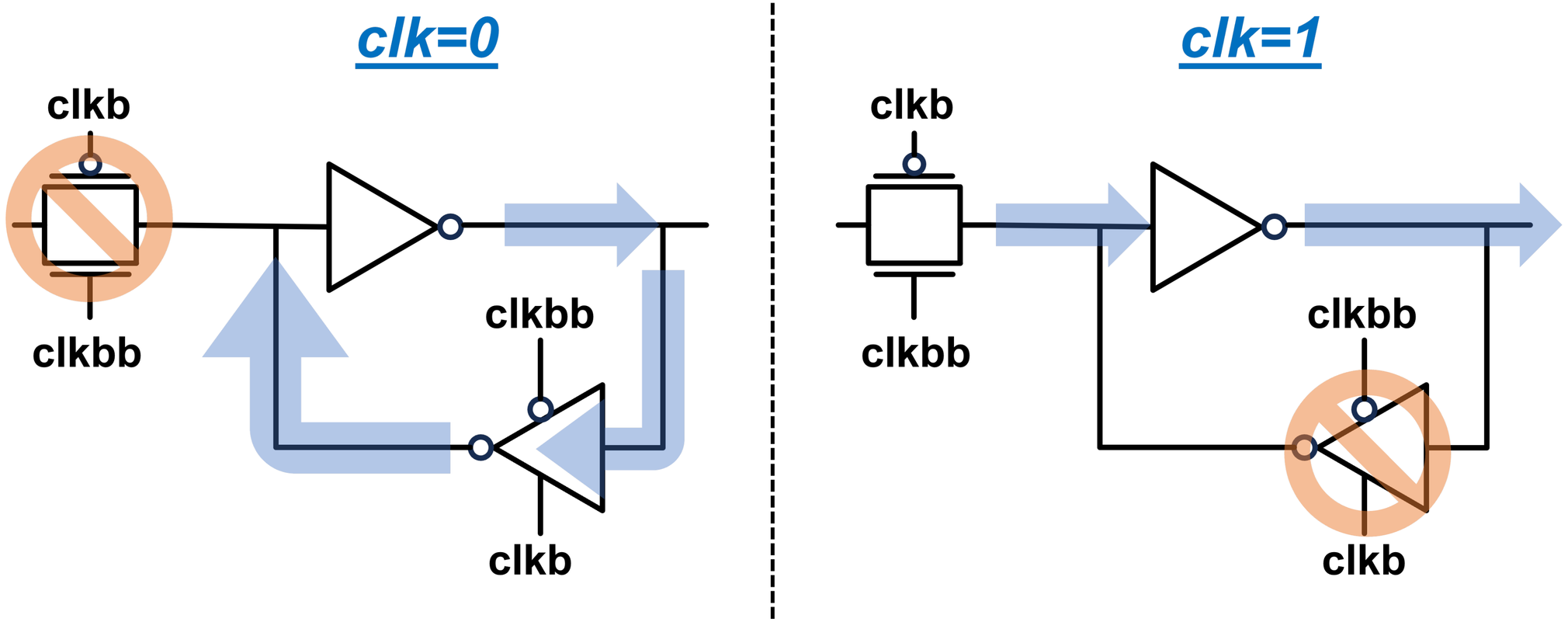
Buffering of Clock Signal



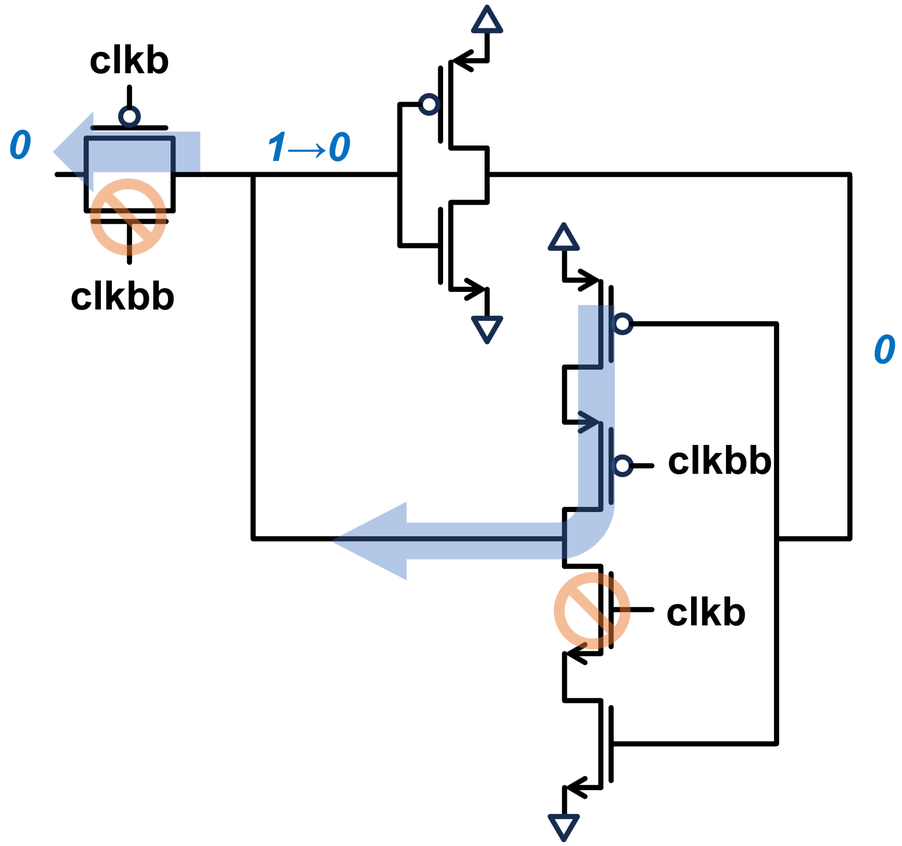
Clock signal always goes through two stage of inverters before they are transmitted to somewhere else in the cell. *clkb* and *clkbb* are always paired and jointly used to control the on/off state of tri-state inverter or transmission gate.

Typical Feedback Loop Structure



This is a typical feedback loop structure, with a tri-state inverter along with a transmission gate. The on/off state of two clock-controlled gates are complementary, making this loop swap between two datapaths. In this example, when the clock is at 0, the loop is in latch mode, pertaining the level stored previously. When the clock is at 1, the signal is passed down from the transmission gate.

Leakage Incurred by Clock Skew



We break down the circuit shown in Page 2 into a transistor-level diagram, and depict when the clock falling signal arrives clkb but not yet to clkbb, i.e., clkb=1 and clkbb=1. When a 0 is to be propagated rightward through the transmission gate, because of the clock skew, the tri-state inverter leaks some current to counteract the efforts by transmission gate. This makes the propagation of a 0 through transmission gate much lower than a 1.