VLSI Homework4

學號：B073040050

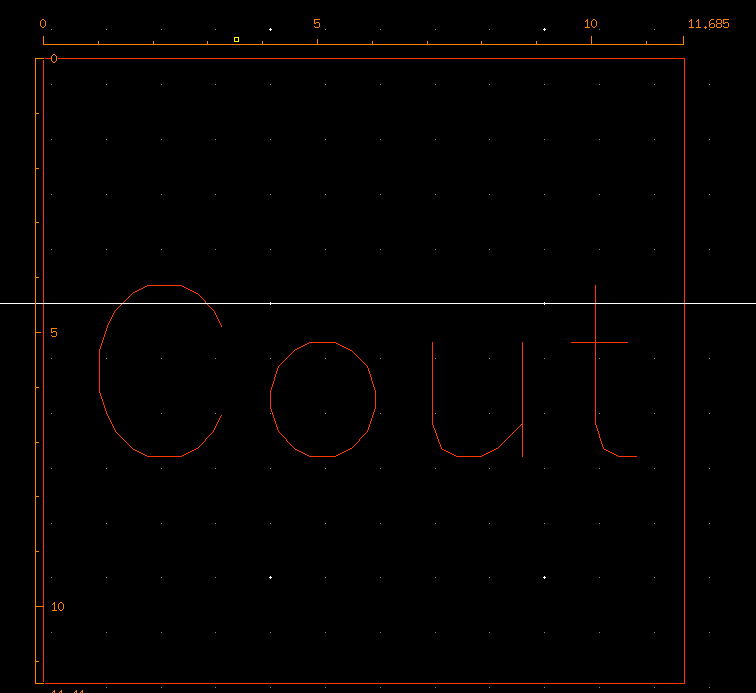
姓名： 翁昌閔

## full\_adder

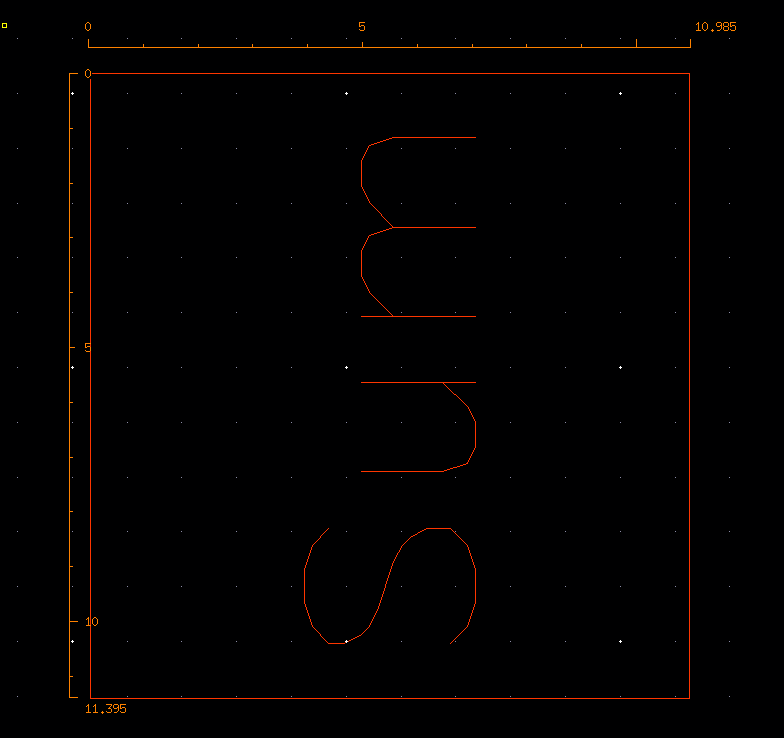
**A.【list the results of propagation delay and compare the worse\_case delay of Pre-simulstion and Post-simulation in Hspice simulation】**

**面積：?? um\*um**

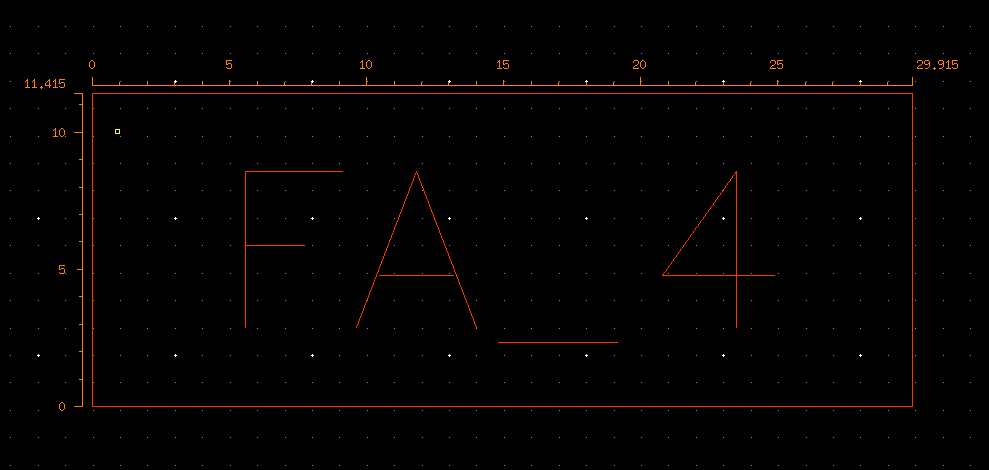
**CMOS\_F1：**



**CMOS\_F2：**



**FA：**

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* **Hspice**

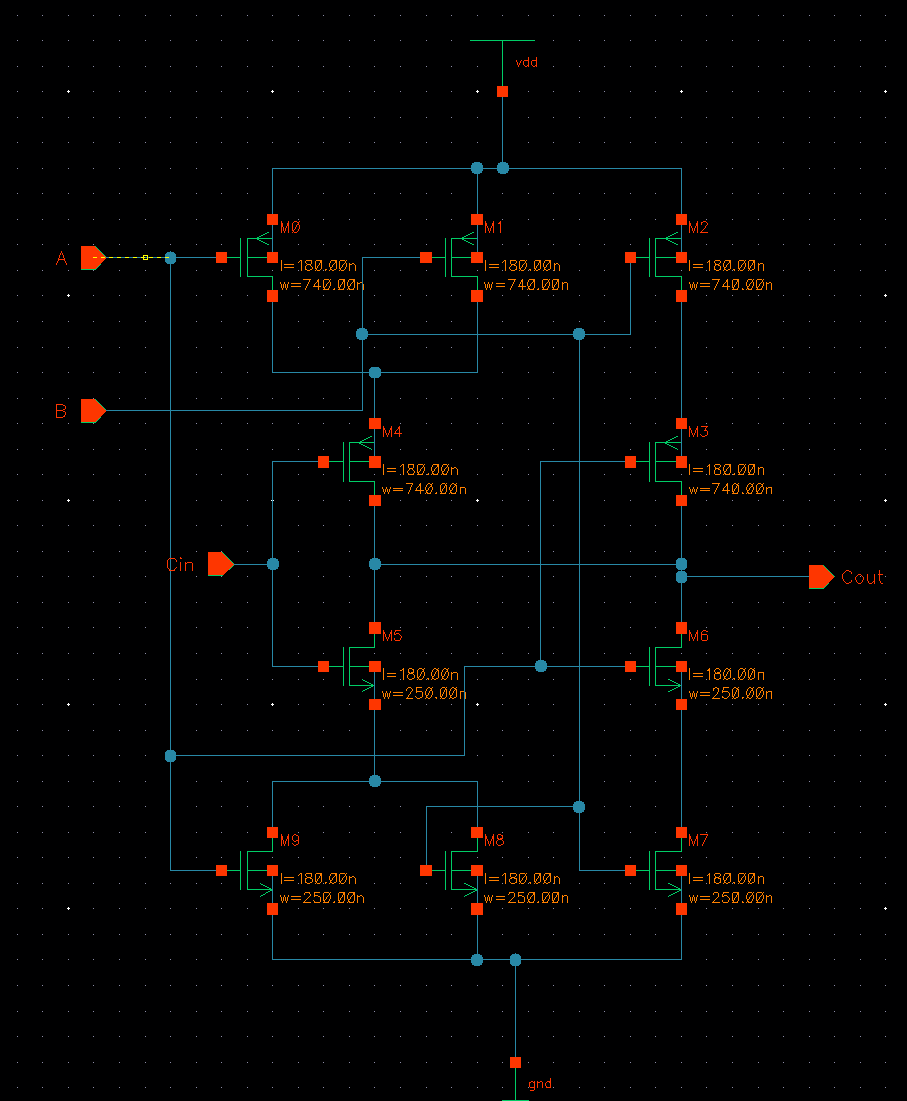
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Cload = 0.01 pF、Temp = 25°C、PC = TT (CMOS\_F1) | | | |  |
|  | | ~Cout | | |
| TpHL | TpLH | Tpd |
| pre\_sim | measure\_A | 152.1526p | 151.8651p | 152.1526p |
| measure\_B | 141.3756p | 151.9946p | 151.9946p |
| measure\_Cin | 136.7484p | 142.7769p | 142.7769p |
| post\_sim | measure\_A |  |  |  |
| measure\_B |  |  |  |
| measure\_Cin |  |  |  |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | |  |  | | | |  | |  | |
| Cload = 0.01 pF、Temp = 25°C、PC = TT (CMOS\_F2) | | | | |  |
|  | | | | ~Sum | | | | | | | |
| TpHL | | | | TpLH | | Tpd | |
| pre\_sim | measure\_A | | | 149.9987p | | | | 228.9729p | | 228.9729p | |
| measure\_B | | | 142.4266p | | | | 221.9842p | | 221.9842p | |
| measure\_Cin | | | 134.6336p | | | | 213.4748p | | 213.4748p | |
| measure\_~cout | | | 136.3573p | | | | 115.7756p | | 136.3573p | |
| post\_sim | measure\_A | | |  | | | |  | |  | |
| measure\_B | | |  | | | |  | |  | |
| measure\_Cin | | |  | | | |  | |  | |
| measure\_~cout | | |  | | | |  | |  | |

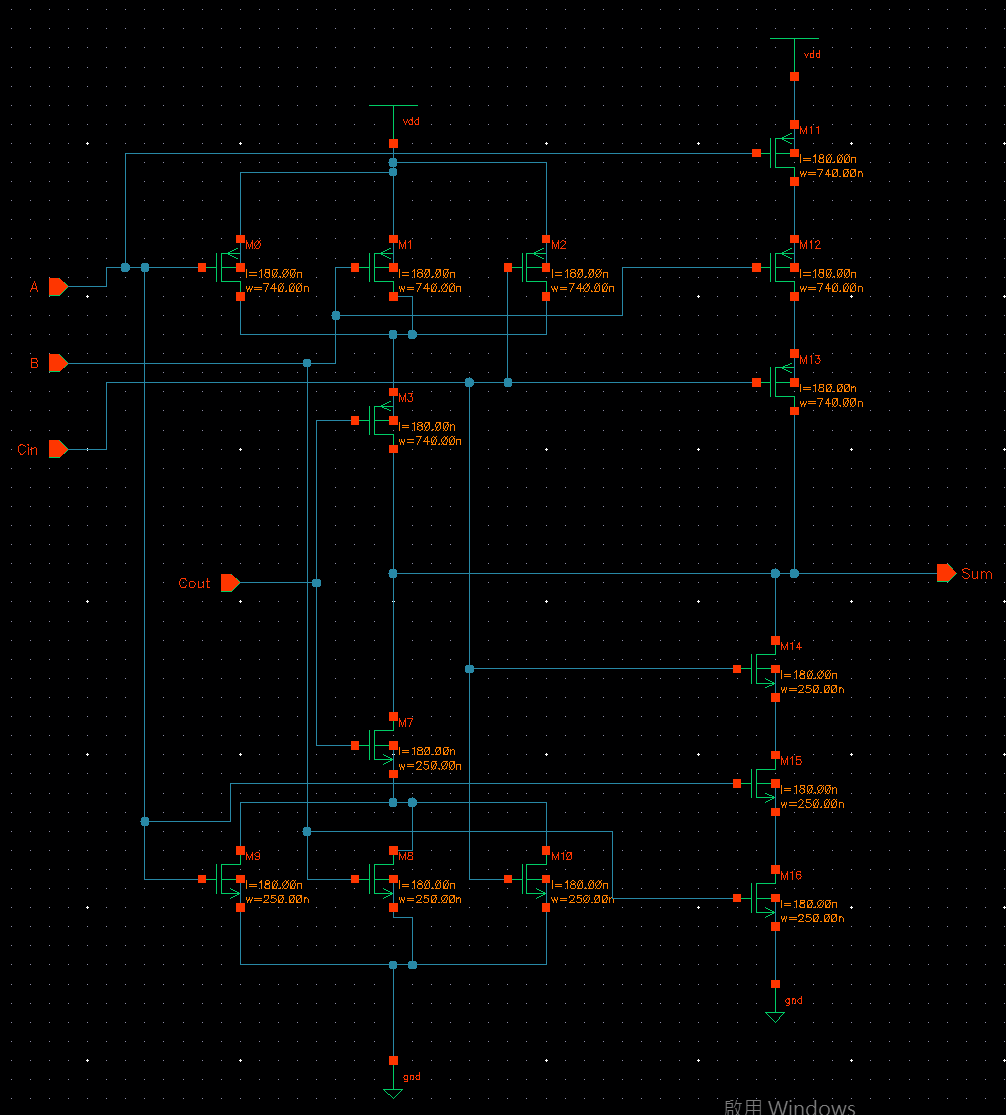
|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Cload = 0.01 pF、Temp = 25°C、PC = TT (Full Adder) | | | |  |  |  |  |  |  |  |  |
|  | | Cout | | | Sum | | | SP(Watts) | DP(Watts) | | |
| TpHL | TpLH | Tpd | TpHL | TpLH | Tpd | max | min | avg |
| pre\_sim | measure\_A | 10.1254n | -9.7046n | 10.1254n | 382.7911p | 362.5626p | 382.7911p | 355.8235p | 497.9698u | 317.3277p | 4.9785u |
| measure\_B | 10.1258n | -9.7169n | 10.1258n | 366.9560p | 367.5445p | 367.5445p | 348.1383p | 486.0770u | 310.2329p | 4.9217u |
| measure\_Cin | 10.1145n | -9.7335n | 10.1145n | 355.9523p | 355.8140p | 355.9523p | 348.1383p | 480.1872u | 308.0052p | 4.8069u |
| post\_sim | measure\_A |  |  |  |  |  |  |  |  |  |  |
| measure\_B |  |  |  |  |  |  |  |  |  |  |
| measure\_Cin |  |  |  |  |  |  |  |  |  |  |

**B.【schematic view】**

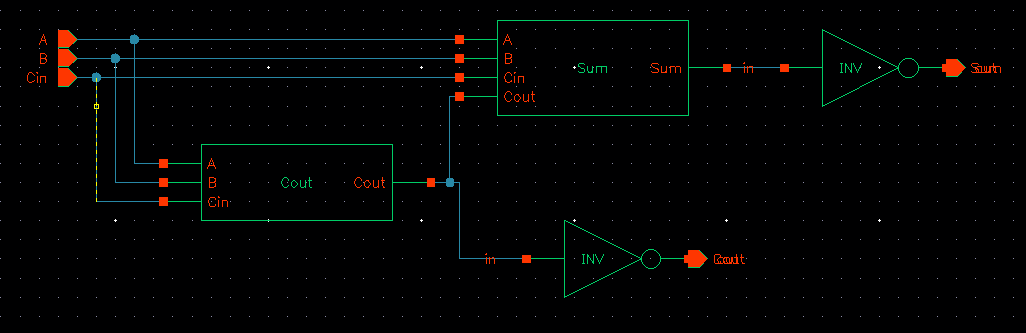
**CMOS\_F1：**

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**CMOS\_F2：**

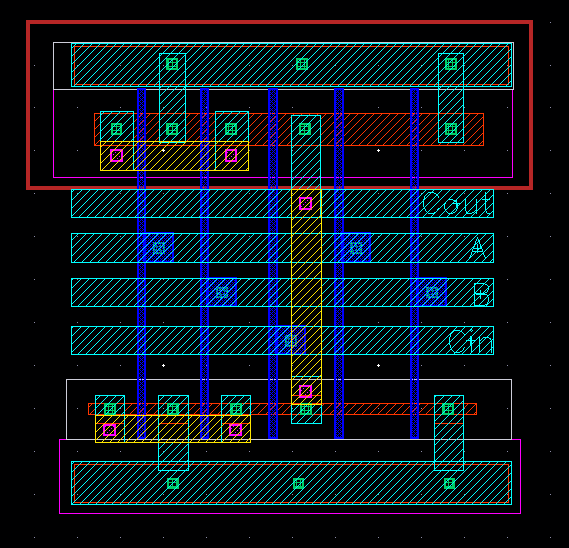
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**FA：**

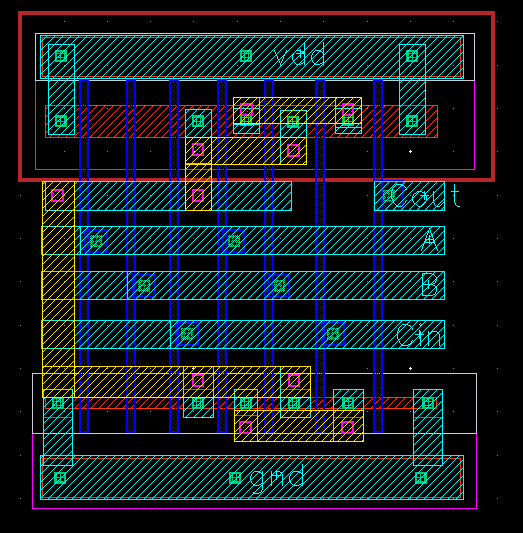


**C.【Layout view】**

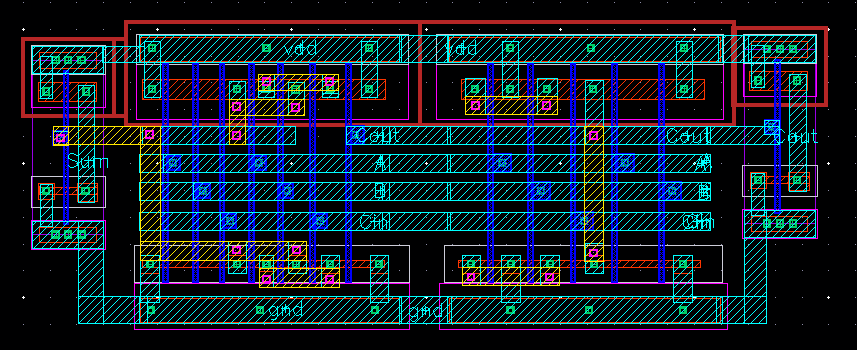
**CMOS\_F1：**

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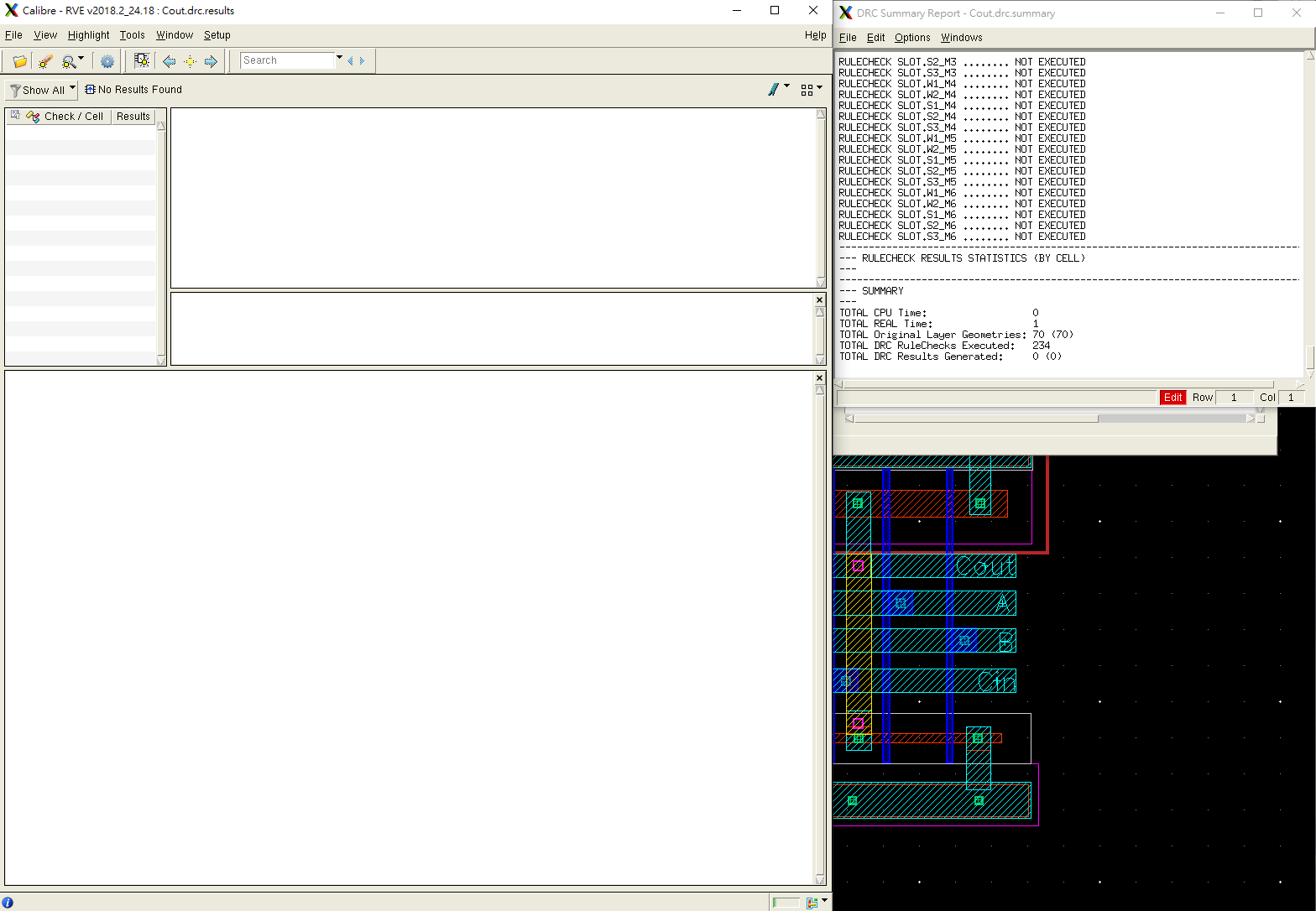
**CMOS\_F2：**

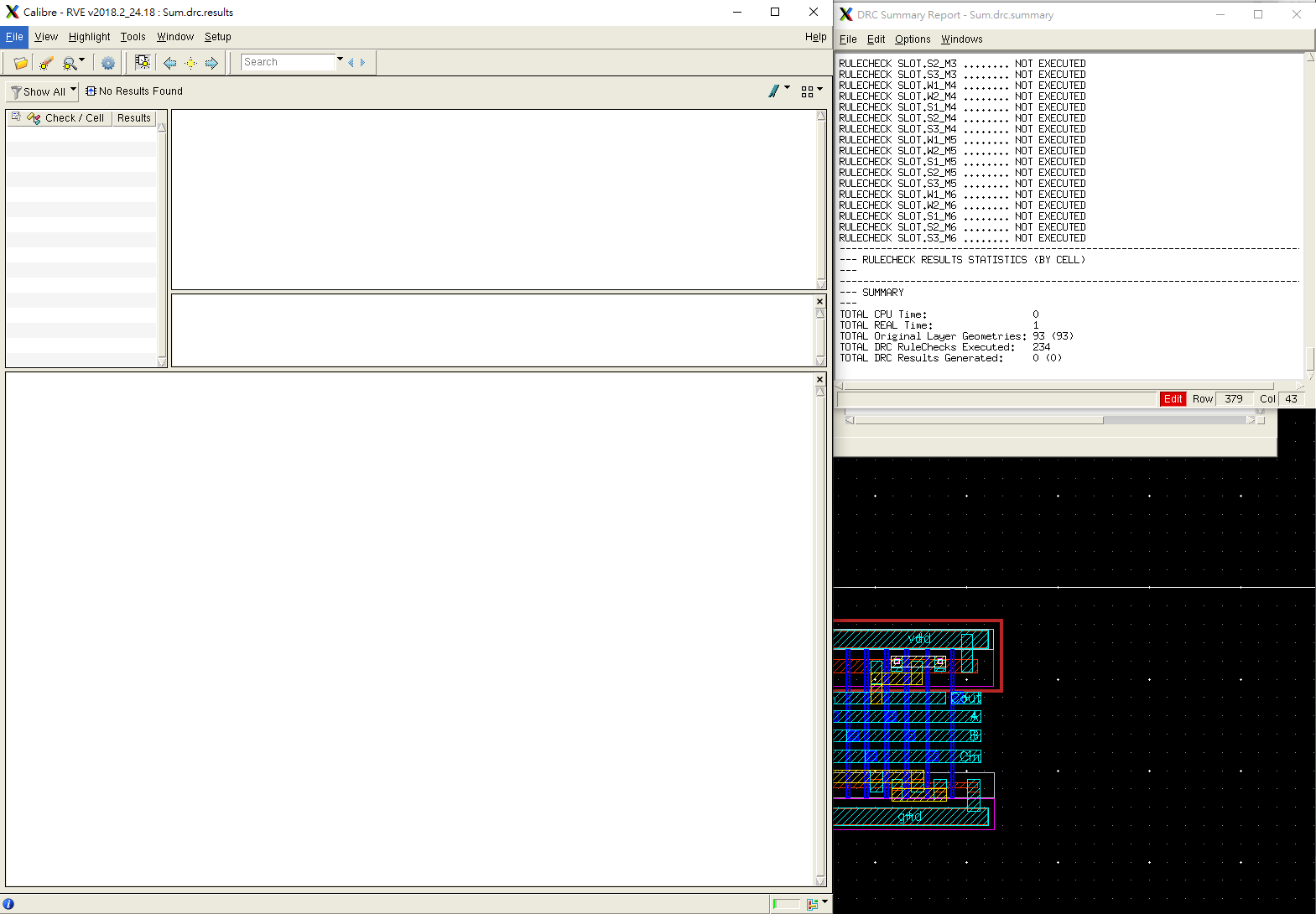
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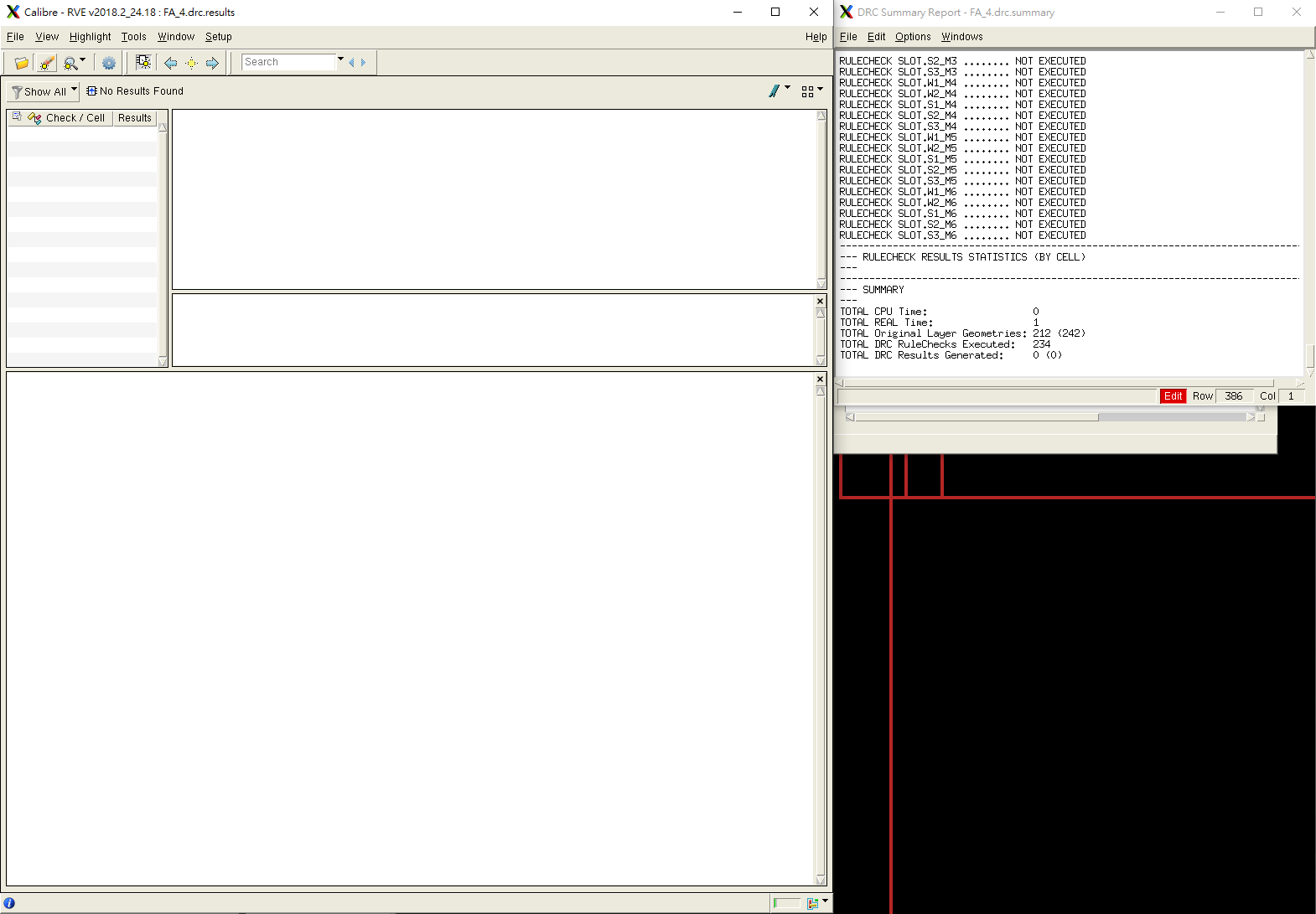
**FA：**

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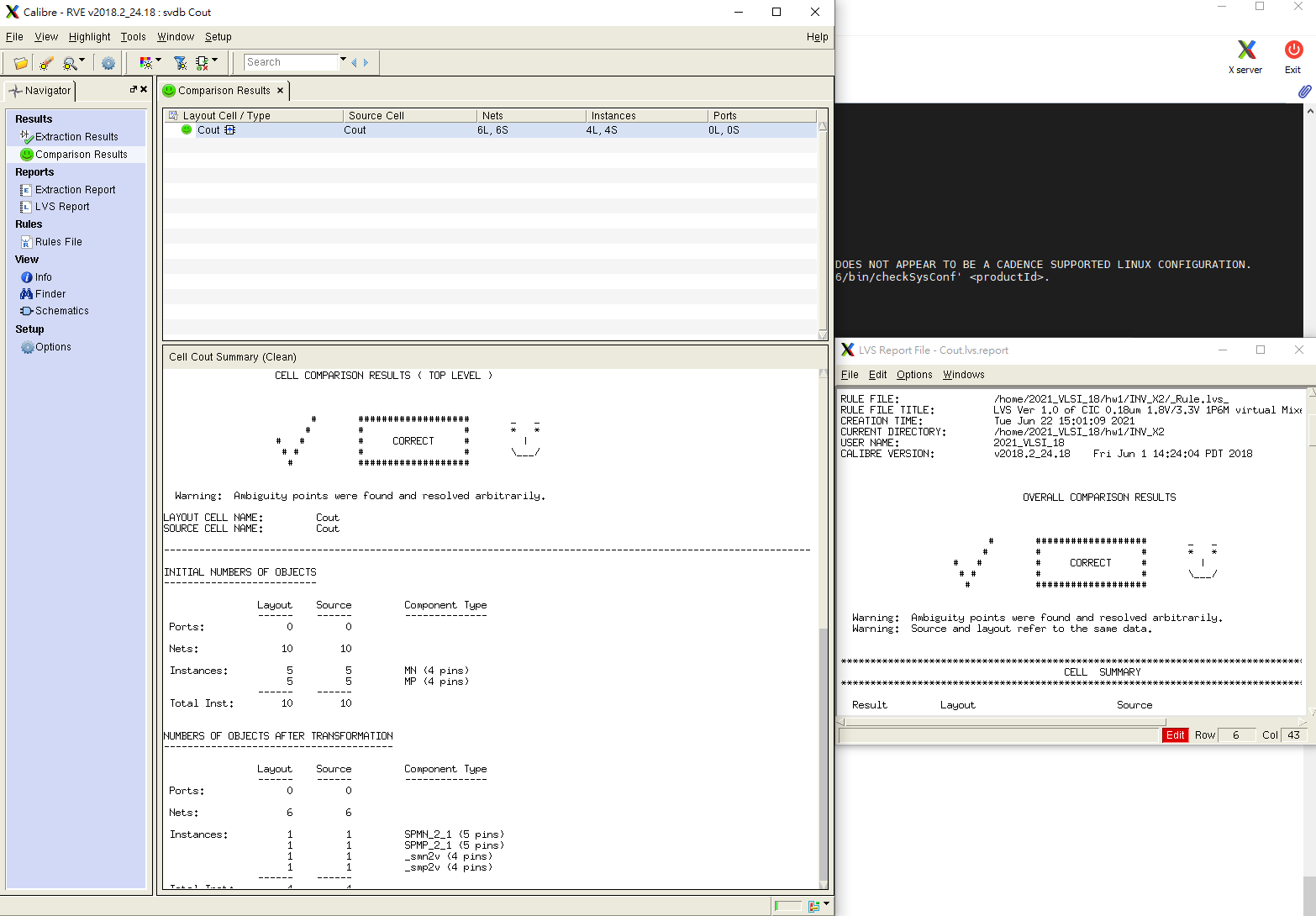
**D.【DRC successful view】\*3**

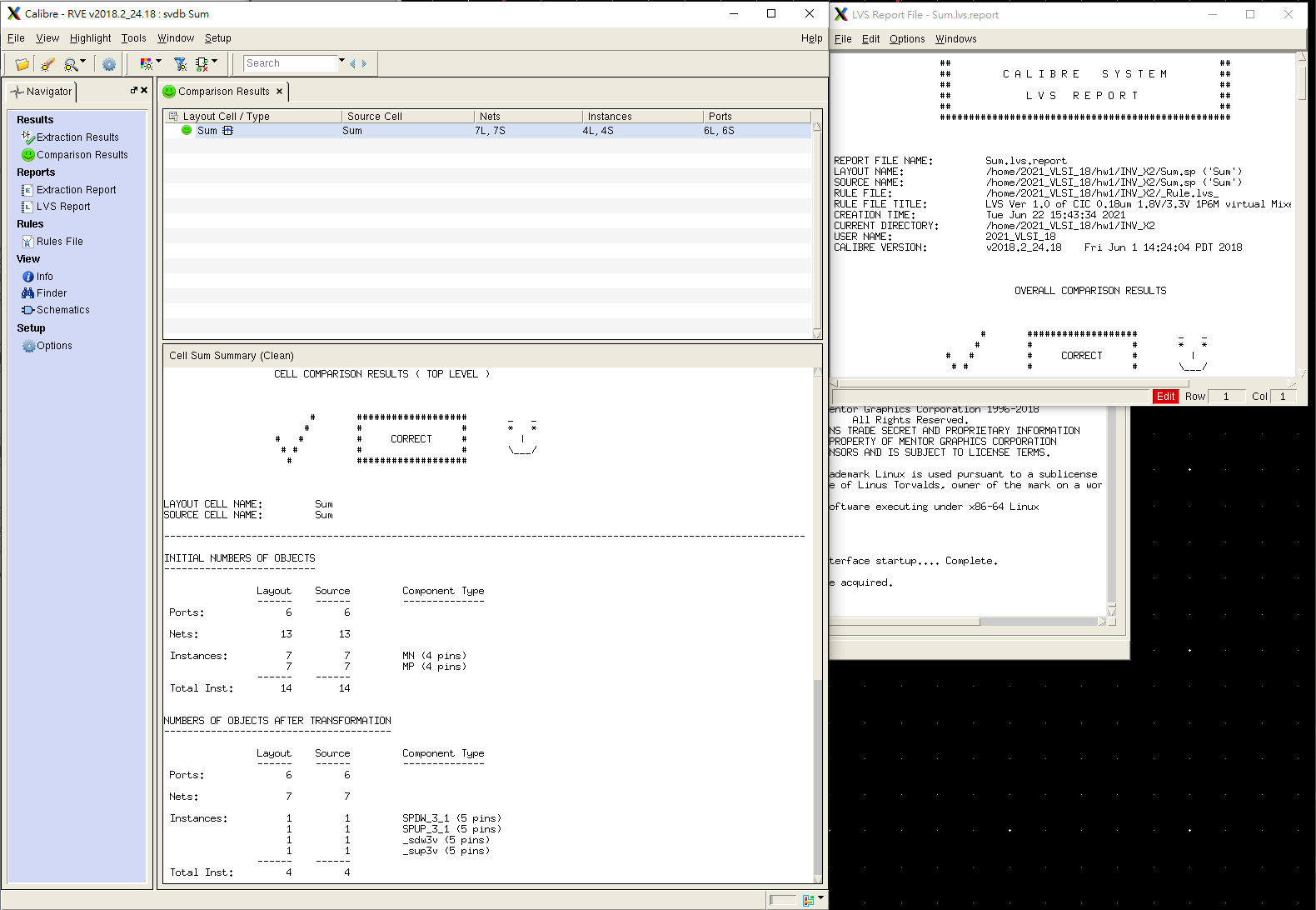
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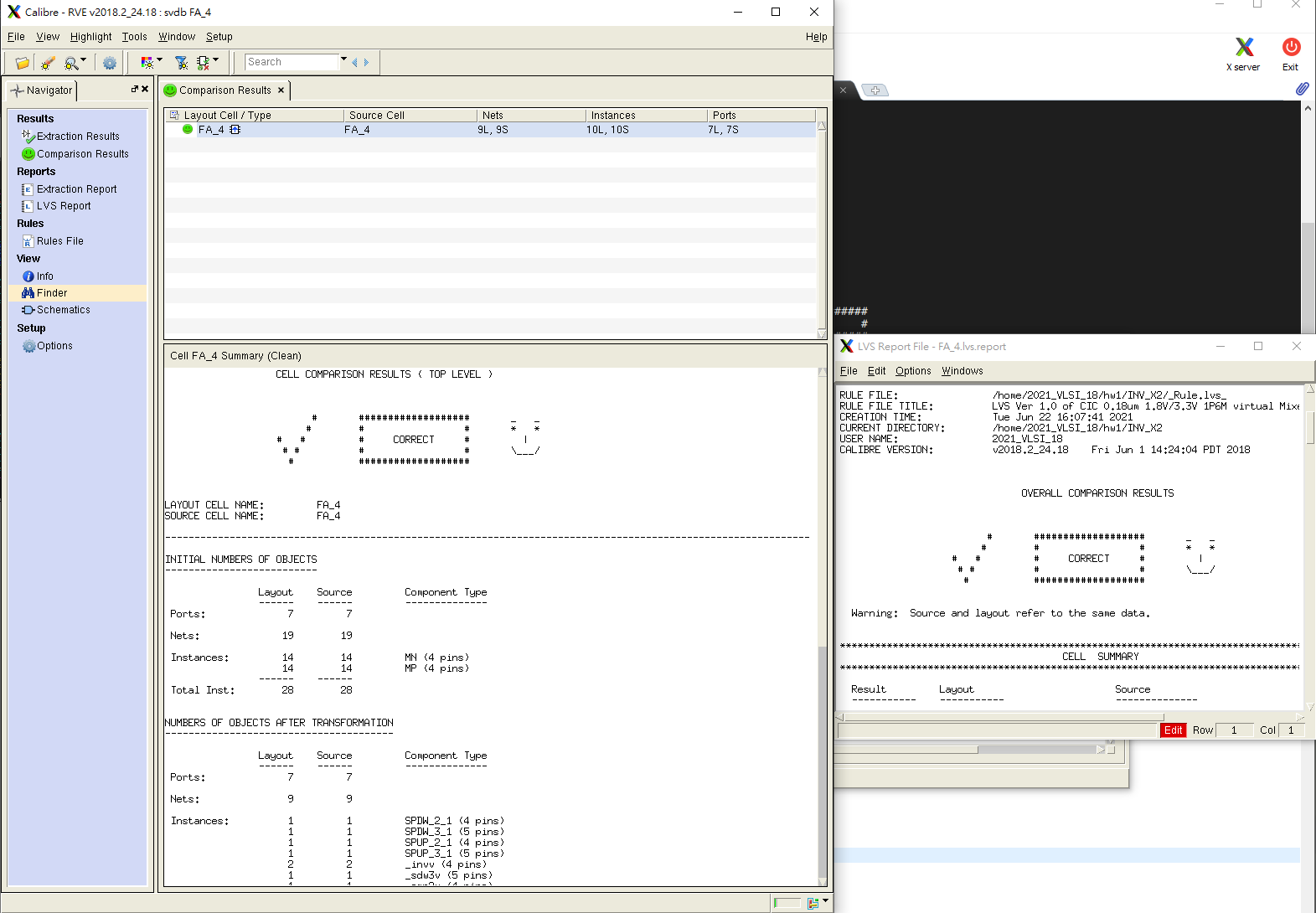
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**E.【LVS successful view】\*3**

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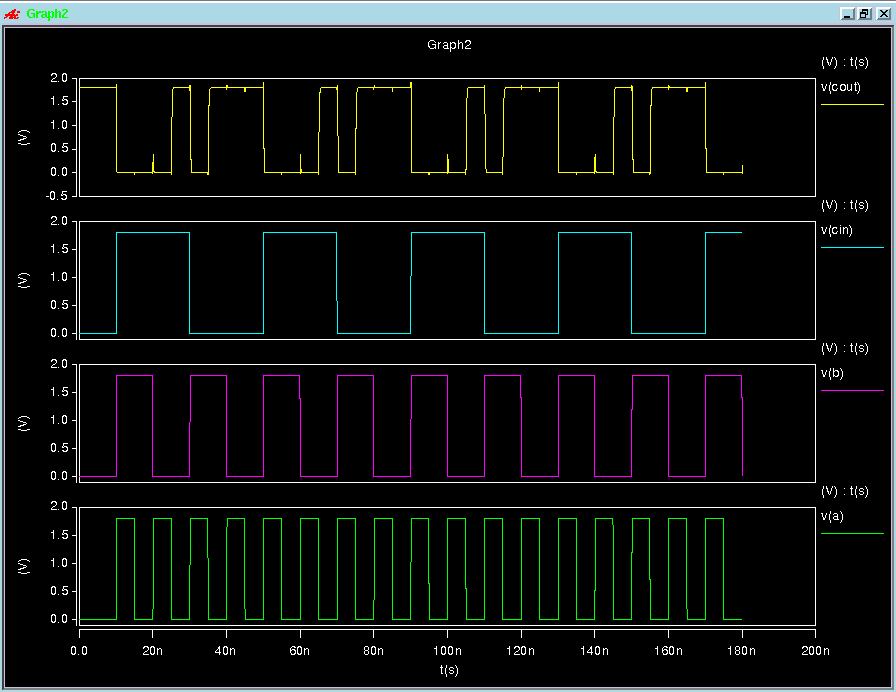
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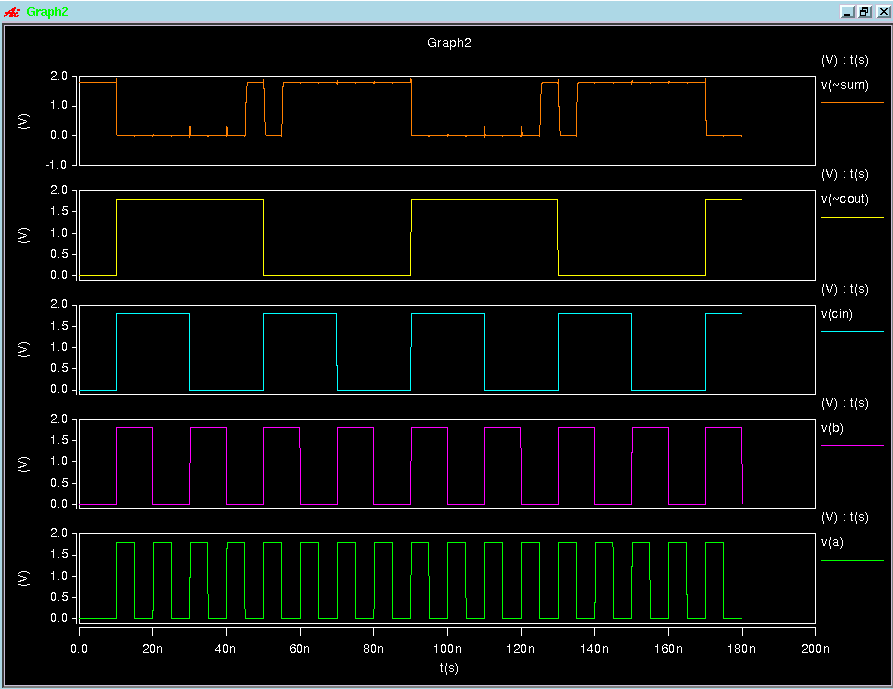
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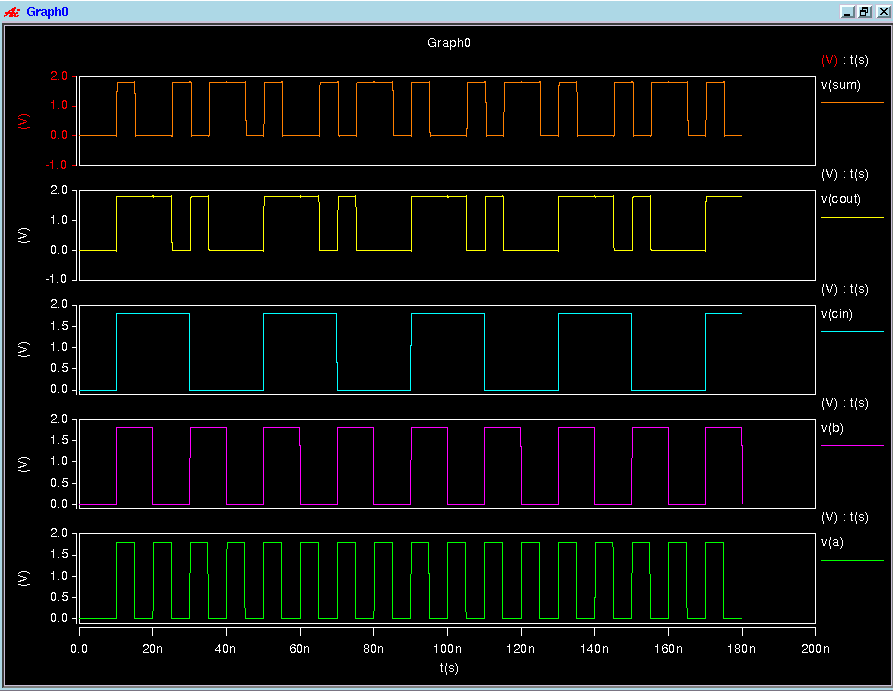
**F.【Pre-layout and Post-layout simulation waveforms】**

**(要包含所有真值表上的值)**

**F-1.(Pre-layout)\*3**

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**F-2.(Post-layout)\*3**

心得: 雖然還是有些東西沒有做完，但是這學期學到了很多VLSI的知識，在實作的過程也覺得挺有趣的。