### ${\tt dont\_enable\_bridge\_and\_let\_it\_configure\_in\_linux\_} {\tt normalmode}$

00:02.0 PCI bridge: Advanced Micro Devices, Inc. [AMD] Family 15h (Models 10h-1fh) Processor Root Port

1	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Ε	F
0*	22	10	12	14	07	04	10	00	00	00	04	06	00	00	01	00
1*	0							Θ	00	04	04	00	31	31	00	00
2*	30	F0	30	F0	F1	FF	01	00	0							0
3*	0			0	50	00	00	00	0			0	FF	01	00	00
4*	0															0
5*	01	58	03	C8	0			Θ	10	Α0	42	01	21	80	00	00
6*	30	29	00	00	02	0D	70	00	40	00	82	В0	00	00	04	00
7*	00	00	48	01	18	00	01	00	0			0	1F	00	70	00
8*	06	80	00	00	06	00	00	00	02	00	00	00	0			0
9*	0															0
Α*	05	В0	81	00	00	00	E0	FE	0							0
В*	0D	В8	00	00	22	10	34	12	80	00	03	A8	0			0
C*	0															0
D*	0															0
E*	50	00	00	00	10	00	00	00	0							0
F*	0															0

 ${\tt dont\_enable\_bridge\_and\_let\_it\_configure\_in\_linux\_} nomodeset = normal$ 

00:02.0 PCI bridge: Advanced Micro Devices, Inc. [AMD] Family 15h (Models 10h-1fh) Processor Root Port

### dont\_enable\_bridge\_and\_let\_it\_configure\_in\_linux\_normalmode (VS 3)

04:00.0 Display controller: Advanced Micro Devices, Inc. [AMD/ATI] Jet PRO [Radeon R5 M230]

2	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Ε	F
0*	02	10	65	66	o <b>3</b>	00	10	00	00	00	80	03	0			Θ
1*	0C	00	00	00	0			0	04	00	30	F0	0			0
2*	01	30	00	00	0											0
3*	00	00	34	Fo	48	00	00	00	0			0	FF	01	00	00
4*	0							0	09	50	08	00	0			0
5*	01	58	03	76	0			0	10	Α0	12	00	A1	8F	00	00
6*	30	29	00	00	82	0C	40	00	40	00	82	10	Θ			0
7*	0															0
8*	0			0	0E	00	00	00	02	00	00	00	0			0
9*	0															0
Α*	05	00	80	00	0											0
B* - F*	0															0

## ${\tt dont\_enable\_bridge\_and\_let\_it\_configure\_in\_linux\_{\bf nomodeset}} \ \ ({\tt VS} \ \ 2)$

04:00.0 Display controller: Advanced Micro Devices, Inc. [AMD/ATI] Jet PRO [Radeon R5 M230]

3	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Е	F
0*	02	10	65	66	ο <b>Ο</b>	00	10	00	00	00	80	03	0			0
1*	0C	00	00	00	0			0	04	00	30	F0	0			0
2*	01	30	00	00	0											0
3*	00	00	00	<b>0</b> 0	48	00	00	00	0			0	FF	01	00	00
4*- F*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*

## core\_enable\_bridge\_--nomodeset (vs 1)

00:02.0 PCI bridge: Advanced Micro Devices, Inc. [AMD] Family 15h (Models 10h-1fh) Processor Root Port

4	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Е	F
0*	22	10	12	14	07	04	10	00	00	00	04	06	10	00	01	00
1*	0							0	00	01	o <b>1</b>	00	11	11	00	00
2*	00	F0	00	F0	01	E0	F <sub>1</sub>	EF	0							0
3*	0			0	50	00	00	00	0			0	00	01	o3	00
4*	0															0
5*	01	58	03	C8	0			0	10	Α0	42	01	21	80	00	00
6*	30	29	00	00	02	0D	70	00	40	00	82	В0	00	00	04	00
7*	00	00	48	01	18	00	01	00	0			0	1F	00	70	00
8*	06	80	00	00	06	00	00	00	02	00	00	00	0			0
9*	0															0
Α*	05	В0	81	00	00	00	E0	FE	0							0
В*	0D	В8	00	00	22	10	34	12	08	00	03	8A	0			0
C*	0															0
D*	0															0
E*	50	00	00	00	10	00	00	00	0							0
F*	0															0

#### dont\_enable\_bridge\_and\_let\_it\_configure\_in\_linux\_nomodeset (VS 4)

00:02.0 PCI bridge: Advanced Micro Devices, Inc. [AMD] Family 15h (Models 10h-1fh) Processor Root Port

1	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Е	F	
0*	22	10	12	14	07	04	10	00	00	00	04	06	<b>0</b> 0	00	01	00	
1*	0							0	00	Θ4	o <b>4</b>	00	31	31	00	00	
2*	30	F0	30	F0	F <sub>1</sub>	FF	01	00	0							0	
3*	0			0	50	00	00	00	0			0	FF	01	ο <b>Θ</b>	00	
4*- F*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	

## core\_enable\_bridge\_-\_nomodeset (vs 3)

01:00.0 Display controller: Advanced Micro Devices, Inc. [AMD/ATI] Jet PRO [Radeon R5 M230]

5	Θ	1	2	3	4	5	6	7	8	9	Α	В	С	D	E	F
0*	02	10	65	66	ο3	00	10	00	00	00	80	03	10	00	00	00
1*	9C	00	00	EΘ	00	00	00	00	04	00	<b>0</b> 0	F0	0			0
2*	01	10	00	00	0											0
3*	00	00	o <b>4</b>	F₀	48	00	00	00	0			0	00	01	00	00
4*	0							0	09	50	08	00	0			0
5*	01	58	03	76	0			Θ	10	Α0	12	00	A1	8F	00	00
6*	30	29	00	00	82	0C	40	00	40	00	82	10	0			0
7*	0															0
8*	0			0	ΘE	00	00	00	02	00	00	00	0			0
9*	0															0
<b>A</b> *	05	00	80	00	0											0
B*- F*	0															0

### dont\_enable\_bridge\_and\_let\_it\_configure\_in\_linux\_nomodeset (VS 5)

01:00.0 Display controller: Advanced Micro Devices, Inc. [AMD/ATI] Jet PRO [Radeon R5 M230]

3	Θ	1	2	3	4	5	6	7	8	9	Α	В	С	D	Ε	F
0*	02	10	65	66	ο <b>Θ</b>	00	10	00	00	00	80	03	00			0
1*	0C	00	00	<b>0</b> 0	0			0	04	00	30	F0	0			0
2*	01	30	00	00	0											0
3*	00	00	ο <b>Ο</b>	<b>0</b> 0	48	00	00	00	0			0	FF	01	00	00
4* - F*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*

## UEFI\_normal\_mode (vs 8)

00:02.0 PCI bridge: Advanced Micro Devices, Inc. [AMD] Family 15h (Models 10h-1fh) Processor Root Port

6	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Е	F
0*	22	10	12	14	07	00	10	00	00	00	04	06	10	00	01	00
1*	0							0	00	01	01	00	31	31	00	20
2*	20	F0	20	F0	01	E0	F1	EF	0							0
3*	0			0	50	00	00	00	0			0	0A	01	00	00
4*	0															0
5*	01	58	03	C8	0			0	10	Α0	42	01	21	80	00	00
6*	10	29	00	00	01	0D	70	00	43	00	81	10	40	00	04	00
7*	00	00	<b>0</b> 8	01	10	00	01	00	0			0	1F	00	00	00
8*	06	00	00	00	06	00	00	00	21	00	00	00	0			0
9*	0															0
Α*	05	В0	80	00	0											0
В*	0D	В8	00	00	22	10	34	12	08	00	03	A8	0			0
C*	0															0
D*	0															0
E*	00			0	FF	FF	FF	FF	0							0
F*	0															0

01:00.0 Display controller: Advanced Micro Devices, Inc. [AMD/ATI] Jet PRO [Radeon R5 M230] (rev ff)

7	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Е	F
0*- F*		FF														

## UEFI\_nomodeset (vs 6)

00:02.0 PCI bridge: Advanced Micro Devices, Inc. [AMD] Family 15h (Models 10h-1fh) Processor Root Port

8	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Е	F
0*	22	10	12	14	07	00	10	00	00	00	04	06	10	00	01	00
1*	0							0	00	01	01	00	31	31	00	20
2*	20	F0	20	F0	01	EΘ	F1	EF	0							0
3*	0			0	50	00	00	00	0			0	0A	01	00	00
4*	0															0
5*	01	58	03	C8	0			0	10	Α0	42	01	21	80	00	00
6*	10	29	00	00	01	0D	70	00	43	00	81	30	40	00	04	00
7*	00	00	48	01	10	00	01	00	0			0	1F	00	00	00
8*	06	00	00	00	06	00	00	00	21	00	00	00	0			0
9*	0															0
Α*	05	В0	80	00	0											0
В*	0D	В8	00	00	22	10	34	12	80	00	03	A8	0			0
C*	0															0
D*	0															0
E*	<b>5</b> <sub>0</sub>	00	00	00	10	00	00	00	0							0
F*	0															0

#### 01:00.0 Display controller: Advanced Micro Devices, Inc. [AMD/ATI] Jet PRO [Radeon R5 M230]

9	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Е	F
0*	02	10	65	66	00	00	10	00	00	00	80	03	10	00	00	00
1*	0C	00	00	E0	0			0	04	00	20	F0	0			0
2*	01	30	00	00	0							0	AA	17	04	38
3*	00	00	00	00	48	00	00	00	0			0	0A	01	00	00
4*	0							0	09	50	08	00	AA	17	04	38
5*	01	58	03	76	0			0	10	Α0	12	00	A1	8F	00	00
6*	10	29	09	00	82	0C	40	00	43	00	81	10	0			0
7*	0															0
8*	0			0	0E	00	00	00	02	00	01	00	0			0
9*	0															0
Α*	05	00	80	00	0											0
B*- F*	0															0

## **UEFI** Windows – Bridge

Α	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	E	F
0*	22	10	12	14	07	00	10	00	00	00	04	06	10	00	01	00
1*	0							0	00	01	01	00	31	31	00	<b>0</b> 0
2*	20	F0	20	F0	01	E0	F1	EF	0							0
3*	00	00	00	00	50	00	00	00	0			0	12	01	00	00
4*	0															0
5*	01	58	03	C8	0			0	10	Α0	42	01	21	80	00	00
6*	10	28	00	00	ο2	0D	70	00	00	00	81	30	40	00	04	00
7*	00	00	<b>4</b> 8	01	<b>0</b> 0	00	01	00	0			0	1F	00	00	00
8*	06	00	00	00	06	00	00	00	02	00	<b>ο1</b>	00	0			0
9*	0															0
Α*	05	В0	80	00	0											0
В*	0D	В8	00	00	22	10	34	12	80	00	03	A8	0			0
C*	0															0
D*	0															0
E*	01	00	00	00	10	00	00	00	0							0
F*	0															0

Туре	PC1	Bus	00	Device	02	Function	00
	Express						
Width	01	Device/	0x14121022	Revision	0×00	Class	0x060400
		<b>VendorID</b>		ID		Code	
Cacheline	0x10	Latency	0×00	<b>Interrupt</b>	INTA	<b>Interrupt</b>	IRQ18
Size		Timer		Pin		Line	_
BAR1	0x00000000	BAR2	0x00000000	Primary	0×00	Secondary	0×01
				Bus#		Bus#	
<b>Subordinate</b>	0×01	<b>IO</b> Range	0x00003000	Memory	0xF0200000		
Bus#			-	Range	-		
			0x00003FFF	•	0xF02FFFF		
<b>Prefetchable</b>	0xE0000000	<b>Expansion</b>	0×00000000	Subsystem	0x12341022		
<b>Memory Range</b>	-	ROM		ĪD			
	0xEFFFFFF						

## **UEFI Windows - R5 M230**

В	Θ	1	2	3	4	5	6	7	8	9	Α	В	С	D	E	F
0*	02	10	65	66	o <b>7</b>	o <b>4</b>	10	00	00	00	80	03	10	00	00	00
1*	9C	00	00	E0	0			0	04	00	2C	F0	0			0
2*	01	3F	00	00	0							0	AA	17	04	38
3*	00	00	ο <b>Θ</b>	<b>0</b> 0	48	00	00	00	0			0	00	01	00	00
4*	Θ							0	09	50	80	00	AA	17	04	38
5*	01	58	03	76	0			0	10	Α0	12	00	A1	8F	00	00
6*	10	29	00	00	82	0C	40	00	00	00	8 <b>1</b>	10	0			0
7*	0															0
8*	0			0	0E	00	00	00	02	00	o <b>1</b>	00	0			0
9*	0															0
A*	05	00	81	00	ΘС	FΘ	EΘ	FE	0			0	52	49	00	00
B* - F*	Θ															0

Туре	PCI	Bus	01	Device	00	Function	00
	Express						
Width	01	Device/	0x66651002	Revision	0×00	Class	0x038000
		VendorID	)	ID		Code	
Cacheline	0x10	Latency	0×00	Interrupt	INTA	<b>Interrupt</b>	None
Size		Timer		Pin		Line	
BAR1	0xE000000C	BAR2	0x00000000	BAR3	0xF02C0004	BAR4	0x00000000
BAR5	0x00003F01	BAR6	0x00000000	<b>ExpansiROM</b>	0x00000000	SubsysID	0x380417AA

# coreinfo\_PCI\_with\_0\_02\_00\_enabled BUS - with bus enabled

				_		•						-				
C	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Ε	F
0*	22	10	12	14	ο7	00	10	00	00	00	04	06	10	00	01	00
1*	0							0	00	o <b>1</b>	01	00	11	11	00	00
2*	00	F₀	00	F₀	01	Εo	F <sub>1</sub>	EF	0							0
3*	00	00	00	00	50	00	00	00	0			0	00	01	o3	00
4*	0															0
5*	01	58	03	C8	00	00	00	00	10	Α0	42	01	21	80	00	00
6*	30	28	00	00	02	0D	70	00	00	00	82	В0	00	00	04	00
7*	00	00	48	01	00	00	01	00	0			0	1F	00	70	00
8*	06	80	00	00	06	00	00	00	02	00	00	00	0			0
9*	0															0
Α*	05	В0	80	00	0											0
В*	0D	В8	00	00	22	10	34	12	08	00	03	A8	0			0
C*	0															0
D*	0															0
E*	50	00	00	00	10	00	00	00	0							0
F*	0															0
				DII	C	=	4 la a	4	ba	- 1	. a b 1	- d				
_		_		BU			tho		bus				•	_	_	_
D	0	1	2	3	4	5	6	7	8	9	A	В	C	D	E	F
0*	22	10	12	14	Θ <b>Ο</b>	00	10	00	00	00	04	06	<b>0</b> 0	00	01	00
1*	0											0	01	01	00	00
2*	0			0	01	<b>0</b> 0	01	00	0							0
3*	0			0	50	00	00	00	0			0	FF	01	ΘΘ	00
	l															
E	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Е	F
0*	**	**	**	**	*0	**	**	**	* *	**	**	**	0*	**	* *	**
1*	**	* *	**	**	* *	**	**	**	* *	*0	*0	**	0*	0*	* *	**
2*	**	0*	* *	0*	* *	0*	0*	EF	* *	* *	* *	* *	* *	**	* *	* *
3*	**	**	**	**	* *	**	**	**	* *	**	**	**	00	**	*0	**
4*-	**	**	**	**	**	**	**	**	**	**	**	**	**	**	**	**

#### BUS - PCI CONFIG SPACE DECODING

04: 07 -> 00 0C: 10 -> 00 19: 01 -> 00 1A: 01 -> 00 1C: 11 -> 01 1D: 11 -> 01 PCI COMMAND PCI CACHE LIN PCI SECONDARY PCI SUBORDINA PCI IO BASE PCI IO LIMIT E\_SIZE \_BUS TE\_BUS 21: F0 -> 00 23: F0 -> 00 25: E0 -> 00 26: F1 -> 01 27: EF -> 00 20 = PCI22 = PCI $24 = PCI_{-}$ 26 = PCIMEMORY\_BASE MEMORY\_LIMIT PREF\_MEMORY\_ PREF\_MEMORY BASE \_LIMIT 3C: FF -> 00 3E: 03 -> 00  $3C = PCI_{-}$  $3E = PCI_{-}$ INTERRUPT\_ BRIDGE CONTROL LINE OE: 01 --> Header Type is O1h (PCI-to-PCI bridge) 04: 07 --> Command = 0000 0111 -> 0000 0000 bit 2) Bus Master - If set to 1 the device can behave as a bus master; otherwise, the device can not generate PCI accesses. bit 1) Memory Space - If set to 1 the device can respond to Memory Space accesses; otherwise, the device's response is disabled. bit 0) I/O Space - If set to 1 the device can respond to I/O Space accesses; otherwise, the device's response is disabled. OC: 10 --> Cache Line Size = 0001 0000 -> 0000 0000 Cache Line Size: Specifies the system cache line size in 32-bit units. A device can limit the number of cacheline sizes it can support, if a unsupported value is written to this field, the device will behave as if a value of 0 was written. /\* Set the cache line size, so far 64 bytes is good for everyone. \*/ pci\_write\_config8(dev, PCI\_CACHE\_LINE\_SIZE, 64 >> 2); // 64 = 0x40 ; 0x40 << 2 = 0x100</pre> 19: 01 --> Secondary Bus Number = 0000 0001 ??? 1A: 01 --> Subordinate Bus Number = 0000 0001 ??? 1C: 11 --> I/O Base 1D: 11 --> I/O Limit 21: F000 --> Memory Base 23: F000 --> Memory Limit 25: E0F1 --> Prefetchable Memory Base 27: 00EF --> Prefetchable Memory Limit 3C: FF --> Interrupt Line

3E: 03 --> Bridge Control = 0000 0011

# coreinfo\_PCI\_with\_0\_02\_00\_enabled R5 M230 WITH BUS ENABLED (BEHIND BUS) (vs B)

									•				•	•	•	
F	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Е	F
0*	02	10	65	66	ο3	ΘΘ	10	00	00	00	80	03	10	00	00	00
1*	0C	00	00	E0	0			0	04	00	00	F0	0			0
2*	01	10	00	00	0											0
3*	00	00	o <b>4</b>	Fο	48	00	00	00	Θ			0	00	01	00	00
4*	0							0	09	50	80	00	0			0
5*	01	58	03	76	0			Θ	10	Α0	12	00	A1	8F	00	00
6*	30	28	00	00	82	0C	40	00	00	00	8 <b>2</b>	10	0			0
7*	0															0
8*	0			0	0E	00	00	00	02	00	ΘΘ	00	0			0
9*	0															0
Α*	05	00	80	00	0											0
B*- F*	0															0
				ι	JEF]	i <b>W</b> 1	indo	DWS	- 1	R5	M23(	Э				
В	0	1	2	<b>(</b>	JEF]	<b>C W</b> j	i <b>nd</b>	<b>DWS</b>	<b>- I</b>	<b>R5</b> I	M23(	<b>9</b> B	С	D	E	F
<i>B</i> ⊙*	0	1 10	2 65										C 10	D 00	E 00	F 00
				3	4	5	6	7	8	9	Α	В				
0*	02	10	65	3 66	<sup>4</sup> <sub>0</sub> 7	5 0 <b>4</b>	6 10	7	8	9	A 80	B 03	10 <sub>0</sub>		00	00
0* 1*	02 0C	10 00	65 00	3 66 E0	9 97 0	5 0 <b>4</b>	6 10	7	8	9	A 80	B 03 F0	10 <sub>0</sub>	00	00	<b>00</b>
0* 1* 2*	02 0C 01	10 00 3F	65 00 00	3 66 E0 00	4 ⊙7 ⊙	5 0 <b>4</b>	6 10 .	7 00 0	8 00 04	9	80 2C	B 03 F0 0	10 0 AA 00	00 17 01	00	90 9 38 90
0* 1* 2* 3*	02 0C 01	10 00 3F	65 00 00	3 66 E0 00	4 ⊙7 ⊙	5 0 <b>4</b>	6 10 .	7 00 0	8 00 04	9 00 00 .	80 2C	B 03 F0 0	10 0 AA 00	00 17 01	00 <b>04</b> 00	90 9 38 90
0* 1* 2* 3*	02 0C 01 00	10 00 3F 00	65 00 00 0 <b>0</b>	3 66 E0 00 <b>O</b> 0	9 0 7 0 0 48 .	5 0 <b>4</b>	6 10 .	7 00 00	8 00 04 0	9 00 00 50	80 2C	B 03 F0 0	10 0 AA 00 AA	00 17 01 17	00 04 00 04	90 9 38 90 38
0* 1* 2* 3* 4*	02 0C 01 00 0	10 00 3F 00	65 00 00 0 <b>0</b>	3 66 E0 00 • 00	4 07 0 48 .	5 04 00	6 10	7 00 00 0	8 00 04 0 09 10	9 00 00 50 A0	80 2C	B 03 F0 0 00 00	10 0 AA 00 AA A1	00 17 01 17	00 04 00 04	00 0 38 00 38 00
0* 1* 2* 3* 4* 5* 6*	02 0C 01 00 0 01 10	10 00 3F 00	65 00 00 0 <b>0</b>	3 66 E0 00 • 00	4 07 0 48 .	5 04 00	6 10	7 00 00 0	8 00 04 0 09 10	9 00 00 50 A0	80 2C	B 03 F0 0 00 00	10 0 AA 00 AA A1	00 17 01 17	00 04 00 04	00 0 38 00 38 00
0* 1* 2* 3* 4* 5* 6* 7*	02 0C 01 00 0 01 10	10 00 3F 00	65 00 00 0 <b>0</b>	3 66 E0 00 • 76 00	4 07 0 48 . 0 82	5 04 00 0c .	6 10 00 40	7 00 00 00	8 00 04 0 09 10 00	9 00 00 50 A0 00	A 80 2C	B 03 F0 0 0 00 10 .	10  O  AA  00  AA  A1  O	00 17 01 17	00 04 00 04	90 38 90 38 90 0
0* 1* 2* 3* 4* 5* 6* 7* 8*	02 0C 01 00 0 01 10 0	10 00 3F 00	65 00 00 0 <b>0</b>	3 66 E0 00 • 76 00	4 07 0 48 . 0 82	5 04 00 0C 00	6 10 00 40	7 00 00 00	8 00 04 0 09 10 00	9 00 00 50 A0 00	A 80 2C	B 03 F0 0 0 00 10 .	10  O  AA  OO  A1  O  . O	00 17 01 17	00 04 00 04	90 38 90 38 90 9

## **UEFI Windows HD8650G** (RW Everything, vs ...normal)

G	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Ε	F
0*	02	10	0B	99	07	04	10	00	00	00	00	03	10	00	80	00
1*	08	00	00	D0	01	40	00	00	00	00	30	F0	0			0
2*	0											0	AA	17	04	38
3*	0			0	50	00	00	00	Θ			0	ΘΘ	01	00	00
4*	0											0	AA	17	04	38
5*	01	58	03	06	0			Θ	10	Α0	92	00	Α0	8F	00	00
6*	10	80	00	00	0											0
7*- 9*	0															0
A*	05	00	81	00	ΘС	Fo	E0	FE	00	00	00	00	62	49	00	00
B*- F*	Θ															0

Туре	PCI	Bus	00	Device	01	Function	00
	Express						
Width	01	Device/	0x990B1002	Revision	0×00	Class	0x030000
		VendorID		ID		Code	
Cacheline	0x10	Latency	0×00	Interrupt	INTA	<b>Interrupt</b>	None
Size		Timer		Pin		Line	
BAR1	0xD0000008	BAR2	0x00004001	BAR3	0xF0300000	BAR4	0x00000000
BAR5	0×00000000	BAR6	0x00000000	<b>ExpansiROM</b>	0x00000000	SubsysID	0x380417AA

## UEFI HD8650G - normal (vs Windows)

Н	Θ	1	2	3	4	5	6	7	8	9	Α	В	С	D	E	F
0*	02	10	0B	99	07	04	10	00	00	00	00	03	10	00	80	00
1*	08	00	00	D0	01	40	00	00	00	00	30	F0	0			0
2*	0											0	AA	17	04	38
3*	0			0	50	00	00	00	Θ			0	οB	01	00	00
4*	0											0	AA	17	04	38
5*	01	58	03	06	0			Θ	10	Α0	92	00	Α0	8F	00	00
6*	10	Θ9	00	00	0											0
7*- 9*	0															0
Α*	05	00	81	00	<sub>0</sub> 4	20	E0	FE	0			0	28	40	00	00
B* - F*	Θ															0

00:01.0 VGA compatible controller: Advanced Micro Devices, Inc. [AMD/ATI] Richland [Radeon HD 8650G]

## UEFI HD8650G - normal (vs J, ...nomodeset)

I	Θ	1	2	3	4	5	6	7	8	9	Α	В	С	D	Ε	F
0*	02	10	0B	99	07	o <b>4</b>	10	00	00	00	00	03	10	00	80	00
1*	08	00	00	D0	01	40	00	00	00	00	30	F0	0			0
2*	0											0	AA	17	04	38
3*	0			0	50	00	00	00	0			0	0B	01	00	00
4*	0											0	AA	17	04	38
5*	01	58	03	06	•			0	10	Α0	92	00	A0	8F	00	00
6*	10	09	ΘΘ	00	0											0
7*- 9*	0															0
Α*	05	00	в <b>1</b>	00	ο4	20	EΘ	FE	0			0	28	40	00	00
B* - F*	0															0

## UEFI HD8650G - nomodeset (vs I, ...normal)

J	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	E	F
0*	02	10	0B	99	07	ΘΘ	10	00	00	00	00	03	10	00	80	00
1*	08	00	00	D0	01	40	00	00	00	00	30	F0	0			0
2*	0											0	AA	17	04	38
3*	0			0	50	00	00	00	0			0	0B	01	00	00
4*	0											0	AA	17	04	38
5*	01	58	03	06	0			0	10	Α0	92	00	Α0	8F	00	00
6*	10	09	ΘА	00	0											0
7*- 9*	0															0
Α*	05	00	8 <b>0</b>	00	0											0
B* - F*	0															0