00:02.0 PCI bridge: Advanced Micro Devices, Inc.
[AMD] Family 15h (Models 10h-1fh) Processor Root Port

1	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0*	22	10	12	14	07	04	10	00	00	00	04	06	00	00	01	00
1*	0	.	.	.	.	.	.	0	00	04	04	00	31	31	00	00
2*	30	F0	30	F0	F1	FF	01	00	0	.	.	.	.	.	.	0
3*	0	.	.	0	50	00	00	00	0	.	.	0	FF	01	00	00
4*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
5*	01	58	03	C8	0	.	.	0	10	A0	42	01	21	80	00	00
6*	30	29	00	00	02	0D	70	00	40	00	82	B0	00	00	04	00
7*	00	00	48	01	18	00	01	00	0	.	.	0	1F	00	70	00
8*	06	80	00	00	06	00	00	00	02	00	00	00	0	.	.	0
9*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
A*	05	B0	81	00	00	00	E0	FE	0	.	.	.	.	.	.	0
B*	0D	B8	00	00	22	10	34	12	08	00	03	A8	0	.	.	0
C*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
D*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
E*	50	00	00	00	10	00	00	00	0	.	.	.	.	.	.	0
F*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0

00:02.0 PCI bridge: Advanced Micro Devices, Inc.
[AMD] Family 15h (Models 10h-1fh) Processor Root Port

dont_enable_bridge_and_let_it_configure_in_linux_normalmode *(vs 3)*

04:00.0 Display controller: Advanced Micro Devices, Inc. [AMD/ATI] Jet PRO [Radeon R5 M230]

2	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0*	02	10	65	66	03	00	10	00	00	00	80	03	0	.	.	0
1*	0C	00	00	00	0	.	.	0	04	00	30	F0	0	.	.	0
2*	01	30	00	00	0	.	.	.	.	.	.	.	.	.	.	0
3*	00	00	34	F0	48	00	00	00	0	.	.	0	FF	01	00	00
4*	0	.	.	.	.	.	.	0	09	50	08	00	0	.	.	0
5*	01	58	03	76	0	.	.	0	10	A0	12	00	A1	8F	00	00
6*	30	29	00	00	82	0C	40	00	40	00	82	10	0	.	.	0
7*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
8*	0	.	.	0	0E	00	00	00	02	00	00	00	0	.	.	0
9*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
A*	05	00	80	00	0	.	.	.	.	.	.	.	.	.	.	0
B*-F*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0

dont_enable_bridge_and_let_it_configure_in_linux_nomodeset *(vs 2)*

04:00.0 Display controller: Advanced Micro Devices, Inc. [AMD/ATI] Jet PRO [Radeon R5 M230]

3	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0*	02	10	65	66	00	00	10	00	00	00	80	03	0	.	.	0
1*	0C	00	00	00	0	.	.	0	04	00	30	F0	0	.	.	0
2*	01	30	00	00	0	.	.	.	.	.	.	.	.	.	.	0
3*	00	00	00	00	48	00	00	00	0	.	.	0	FF	01	00	00
4*-F*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*

core_enable_bridge_-_nomodeset *(vs 1)*

00:02.0 PCI bridge: Advanced Micro Devices, Inc.
[AMD] Family 15h (Models 10h-1fh) Processor Root Port

4	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0*	22	10	12	14	07	04	10	00	00	00	04	06	1_0	00	01	00
1*	0	.	.	.	.	.	.	0	00	$_01$	$_01$	00	1_1	1_1	00	00
2*	0_0	F0	0_0	F0	0_1	E0	F_1	EF	0	.	.	.	.	.	.	0
3*	0	.	.	0	50	00	00	00	0	.	.	0	00	01	$_03$	00
4*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
5*	01	58	03	C8	0	.	.	0	10	A0	42	01	21	80	00	00
6*	30	29	00	00	02	0D	70	00	40	00	82	B0	00	00	04	00
7*	00	00	48	01	18	00	01	00	0	.	.	0	1F	00	70	00
8*	06	80	00	00	06	00	00	00	02	00	00	00	0	.	.	0
9*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
A*	05	B0	81	00	00	00	E0	FE	0	.	.	.	.	.	.	0
B*	0D	B8	00	00	22	10	34	12	08	00	03	A8	0	.	.	0
C*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
D*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
E*	50	00	00	00	10	00	00	00	0	.	.	.	.	.	.	0
F*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0

dont_enable_bridge_and_let_it_configure_in_linux_nomodeset *(vs 4)*

00:02.0 PCI bridge: Advanced Micro Devices, Inc.
[AMD] Family 15h (Models 10h-1fh) Processor Root Port

1	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0*	22	10	12	14	07	04	10	00	00	00	04	06	0_0	00	01	00
1*	0	.	.	.	.	.	.	0	00	$_04$	$_04$	00	3_1	3_1	00	00
2*	3_0	F0	3_0	F0	F_1	FF	0_1	00	0	.	.	.	.	.	.	0
3*	0	.	.	0	50	00	00	00	0	.	.	0	FF	01	$_00$	00
4*-F*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*

core_enable_bridge_-_nomodeset *(vs 3)*

01:00.0 Display controller: Advanced Micro Devices, Inc. [AMD/ATI] Jet PRO [Radeon R5 M230]

5	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0*	02	10	65	66	03	00	10	00	00	00	80	03	10	00	00	00
1*	0C	00	00	E0	00	00	00	00	04	00	00	F0	0	.	.	0
2*	01	10	00	00	0	.	.	.	.	.	.	.	.	.	.	0
3*	00	00	04	F0	48	00	00	00	0	.	.	0	00	01	00	00
4*	0	.	.	.	.	.	.	0	09	50	08	00	0	.	.	0
5*	01	58	03	76	0	.	.	0	10	A0	12	00	A1	8F	00	00
6*	30	29	00	00	82	0C	40	00	40	00	82	10	0	.	.	0
7*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
8*	0	.	.	0	0E	00	00	00	02	00	00	00	0	.	.	0
9*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
A*	05	00	80	00	0	.	.	.	.	.	.	.	.	.	.	0
B*-F*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0

dont_enable_bridge_and_let_it_configure_in_linux_nomodeset *(vs 5)*

01:00.0 Display controller: Advanced Micro Devices, Inc. [AMD/ATI] Jet PRO [Radeon R5 M230]

3	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0*	02	10	65	66	00	00	10	00	00	00	80	03	00	.	.	0
1*	0C	00	00	00	0	.	.	0	04	00	30	F0	0	.	.	0
2*	01	30	00	00	0	.	.	.	.	.	.	.	.	.	.	0
3*	00	00	00	00	48	00	00	00	0	.	.	0	FF	01	00	00
4*-F*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*

UEFI_normal_mode *(vs 8)*

00:02.0 PCI bridge: Advanced Micro Devices, Inc.
[AMD] Family 15h (Models 10h-1fh) Processor Root Port

6	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0*	22	10	12	14	07	00	10	00	00	00	04	06	10	00	01	00
1*	0	.	.	.	.	.	.	0	00	01	01	00	31	31	00	20
2*	20	F0	20	F0	01	E0	F1	EF	0	.	.	.	.	.	.	0
3*	0	.	.	0	50	00	00	00	0	.	.	0	0A	01	00	00
4*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
5*	01	58	03	C8	0	.	.	0	10	A0	42	01	21	80	00	00
6*	10	29	00	00	01	0D	70	00	43	00	81	1₀	40	00	04	00
7*	00	00	0₈	01	10	00	01	00	0	.	.	0	1F	00	00	00
8*	06	00	00	00	06	00	00	00	21	00	00	00	0	.	.	0
9*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
A*	05	B0	80	00	0	.	.	.	.	.	.	.	.	.	.	0
B*	0D	B8	00	00	22	10	34	12	08	00	03	A8	0	.	.	0
C*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
D*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
E*	0₀	.	.	0	FF	FF	FF	FF	0	.	.	.	.	.	.	0
F*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0

01:00.0 Display controller: Advanced Micro Devices, Inc. [AMD/ATI]
Jet PRO [Radeon R5 M230] (rev ff)

7	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0*-F*	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF

UEFI_nomodeset *(vs 6)*

00:02.0 PCI bridge: Advanced Micro Devices, Inc.
[AMD] Family 15h (Models 10h-1fh) Processor Root Port

8	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0*	22	10	12	14	07	00	10	00	00	00	04	06	10	00	01	00
1*	0	.	.	.	.	.	.	0	00	01	01	00	31	31	00	20
2*	20	F0	20	F0	01	E0	F1	EF	0	.	.	.	.	.	.	0
3*	0	.	.	0	50	00	00	00	0	.	.	0	0A	01	00	00
4*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
5*	01	58	03	C8	0	.	.	0	10	A0	42	01	21	80	00	00
6*	10	29	00	00	01	0D	70	00	43	00	81	30	40	00	04	00
7*	00	00	48	01	10	00	01	00	0	.	.	0	1F	00	00	00
8*	06	00	00	00	06	00	00	00	21	00	00	00	0	.	.	0
9*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
A*	05	B0	80	00	0	.	.	.	.	.	.	.	.	.	.	0
B*	0D	B8	00	00	22	10	34	12	08	00	03	A8	0	.	.	0
C*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
D*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
E*	50	00	00	00	10	00	00	00	0	.	.	.	.	.	.	0
F*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0

01:00.0 Display controller: Advanced Micro Devices, Inc.
[AMD/ATI] Jet PRO [Radeon R5 M230]

9	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0*	02	10	65	66	00	00	10	00	00	00	80	03	10	00	00	00
1*	0C	00	00	E0	0	.	.	0	04	00	20	F0	0	.	.	0
2*	01	30	00	00	0	.	.	.	.	.	.	0	AA	17	04	38
3*	00	00	00	00	48	00	00	00	0	.	.	0	0A	01	00	00
4*	0	.	.	.	.	.	.	0	09	50	08	00	AA	17	04	38
5*	01	58	03	76	0	.	.	0	10	A0	12	00	A1	8F	00	00
6*	10	29	09	00	82	0C	40	00	43	00	81	10	0	.	.	0
7*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
8*	0	.	.	0	0E	00	00	00	02	00	01	00	0	.	.	0
9*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
A*	05	00	80	00	0	.	.	.	.	.	.	.	.	.	.	0
B*-F*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0

UEFI Windows – Bridge

A	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0*	22	10	12	14	07	00	10	00	00	00	04	06	10	00	01	00
1*	0	.	.	.	.	.	.	0	00	01	01	00	31	31	00	00
2*	20	F0	20	F0	01	E0	F1	EF	0	.	.	.	.	.	.	0
3*	00	00	00	00	50	00	00	00	0	.	.	0	12	01	00	00
4*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
5*	01	58	03	C8	0	.	.	0	10	A0	42	01	21	80	00	00
6*	10	28	00	00	02	0D	70	00	00	00	81	30	40	00	04	00
7*	00	00	48	01	00	00	01	00	0	.	.	0	1F	00	00	00
8*	06	00	00	00	06	00	00	00	02	00	01	00	0	.	.	0
9*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
A*	05	B0	80	00	0	.	.	.	.	.	.	.	.	.	.	0
B*	0D	B8	00	00	22	10	34	12	08	00	03	A8	0	.	.	0
C*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
D*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
E*	01	00	00	00	10	00	00	00	0	.	.	.	.	.	.	0
F*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0

Type	PCI Express	**Bus**	00	**Device**	02	**Function**	00
Width	01	**Device/ VendorID**	0x14121022	**Revision ID**	0x00	**Class Code**	0x060400
Cacheline Size	0x10	**Latency Timer**	0x00	**Interrupt Pin**	INTA	**Interrupt Line**	IRQ18
BAR1	0x00000000	**BAR2**	0x00000000	**Primary Bus#**	0x00	**Secondary Bus#**	0x01
Subordinate Bus#	0x01	**IO Range**	0x00003000 - 0x00003FFF	**Memory Range**	0xF0200000 - 0xF02FFFFF
Prefetchable Memory Range	0xE0000000 - 0xEFFFFFFF	**Expansion ROM**	0x00000000	**Subsystem ID**	0x12341022

UEFI Windows - R5 M230

B	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0*	02	10	65	66	07	04	10	00	00	00	80	03	10	00	00	00
1*	0C	00	00	E0	0	.	.	0	04	00	2C	F0	0	.	.	0
2*	01	3F	00	00	0	.	.	.	.	.	.	0	AA	17	04	38
3*	00	00	00	00	48	00	00	00	0	.	.	0	00	01	00	00
4*	0	.	.	.	.	.	.	0	09	50	08	00	AA	17	04	38
5*	01	58	03	76	0	.	.	0	10	A0	12	00	A1	8F	00	00
6*	10	29	00	00	82	0C	40	00	00	00	81	10	0	.	.	0
7*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
8*	0	.	.	0	0E	00	00	00	02	00	01	00	0	.	.	0
9*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
A*	05	00	81	00	0C	F0	E0	FE	0	.	.	0	52	49	00	00
B*-F*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0

Type	PCI Express	**Bus**	01	**Device**	00	**Function**	00
Width	01	**Device/VendorID**	0x66651002	**Revision ID**	0x00	**Class Code**	0x038000
Cacheline Size	0x10	**Latency Timer**	0x00	**Interrupt Pin**	INTA	**Interrupt Line**	None
BAR1	0xE000000C	**BAR2**	0x00000000	**BAR3**	0xF02C0004	**BAR4**	0x00000000
BAR5	0x00003F01	**BAR6**	0x00000000	**ExpansiROM**	0x00000000	**SubsysID**	0x380417AA

coreinfo_PCI_with_0_02_00_enabled

BUS - with bus enabled

C	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0*	22	10	12	14	07	00	10	00	00	00	04	06	10	00	01	00
1*	0	.	.	.	.	.	.	0	00	01	01	00	11	11	00	00
2*	00	F0	00	F0	01	E0	F1	EF	0	.	.	.	.	.	.	0
3*	00	00	00	00	50	00	00	00	0	.	.	0	00	01	03	00
4*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
5*	01	58	03	C8	00	00	00	00	10	A0	42	01	21	80	00	00
6*	30	28	00	00	02	0D	70	00	00	00	82	B0	00	00	04	00
7*	00	00	48	01	00	00	01	00	0	.	.	0	1F	00	70	00
8*	06	80	00	00	06	00	00	00	02	00	00	00	0	.	.	0
9*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
A*	05	B0	80	00	0	.	.	.	.	.	.	.	.	.	.	0
B*	0D	B8	00	00	22	10	34	12	08	00	03	A8	0	.	.	0
C*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
D*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
E*	50	00	00	00	10	00	00	00	0	.	.	.	.	.	.	0
F*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0

BUS - without bus enabled

D	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0*	22	10	12	14	00	00	10	00	00	00	04	06	00	00	01	00
1*	0	.	.	.	.	.	.	.	.	.	.	0	01	01	00	00
2*	0	.	.	0	01	00	01	00	0	.	.	.	.	.	.	0
3*	0	.	.	0	50	00	00	00	0	.	.	0	FF	01	00	00

E	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0*	**	**	**	**	*0	**	**	**	**	**	**	**	0*	**	**	**
1*	**	**	**	**	**	**	**	**	**	*0	*0	**	0*	0*	**	**
2*	**	0*	**	0*	**	0*	0*	EF	**	**	**	**	**	**	**	**
3*	**	**	**	**	**	**	**	**	**	**	**	**	00	**	*0	**
4*-F*	**	**	**	**	**	**	**	**	**	**	**	**	**	**	**	**

BUS – PCI CONFIG SPACE DECODING

```
04: 07 -> 00 0C: 10 -> 00 19: 01 -> 00 1A: 01 -> 00 1C: 11 -> 01 1D: 11 -> 01
PCI_COMMAND PCI_CACHE_LIN PCI_SECONDARY PCI_SUBORDINA PCI_IO_BASE  PCI_IO_LIMIT
              E_SIZE         _BUS          TE_BUS

21: F0 -> 00 23: F0 -> 00 25: E0 -> 00 26: F1 -> 01 27: EF -> 00

  20 = PCI_     22 = PCI_      24 = PCI_     26 = PCI_
 MEMORY_BASE MEMORY_LIMIT PREF_MEMORY_  PREF_MEMORY
                             _BASE         _LIMIT

3C: FF -> 00 3E: 03 -> 00

  3C = PCI_     3E = PCI_
 INTERRUPT_     BRIDGE_
    _LINE       _CONTROL
```

```
                0E: 01 --> Header Type is 01h (PCI-to-PCI bridge)

                04: 07 --> Command           = 0000 0111 -> 0000 0000

     bit 2) Bus Master - If set to 1 the device can behave as a bus master;
               otherwise, the device can not generate PCI accesses.

     bit 1) Memory Space - If set to 1 the device can respond to Memory Space
               accesses; otherwise, the device's response is disabled.

   bit 0) I/O Space - If set to 1 the device can respond to I/O Space accesses;
               otherwise, the device's response is disabled.

                0C: 10 --> Cache Line Size = 0001 0000 -> 0000 0000
```

 Cache Line Size: Specifies the system cache line size in 32-bit units. A device
 can limit the number of cacheline sizes it can support, if a unsupported value
is written to this field, the device will behave as if a value of 0 was written.

   /* Set the cache line size, so far 64 bytes is good for everyone. */

 pci_write_config8(dev, PCI_CACHE_LINE_SIZE, 64 >> 2); // 64 = 0x40 ; 0x40 << 2 = 0x100

```
              19: 01 --> Secondary Bus Number   = 0000 0001 ???

              1A: 01 --> Subordinate Bus Number = 0000 0001 ???

                       1C: 11 --> I/O Base

                       1D: 11 --> I/O Limit

                     21: F000 --> Memory Base

                     23: F000 --> Memory Limit

                 25: E0F1 --> Prefetchable Memory Base

                 27: 00EF --> Prefetchable Memory Limit

                     3C: FF --> Interrupt Line

                 3E: 03 --> Bridge Control = 0000 0011
```

coreinfo_PCI_with_0_02_00_enabled

R5 M230 WITH BUS ENABLED (BEHIND BUS) *(vs B)*

F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0*	02	10	65	66	03	00	10	00	00	00	80	03	10	00	00	00
1*	0C	00	00	E0	0	.	.	0	04	00	00	F0	0	.	.	0
2*	01	10	00	00	0	.	.	.	.	.	.	.	.	.	.	0
3*	00	00	04	F0	48	00	00	00	0	.	.	0	00	01	00	00
4*	0	.	.	.	.	.	.	0	09	50	08	00	0	.	.	0
5*	01	58	03	76	0	.	.	0	10	A0	12	00	A1	8F	00	00
6*	30	28	00	00	82	0C	40	00	00	00	82	10	0	.	.	0
7*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
8*	0	.	.	0	0E	00	00	00	02	00	00	00	0	.	.	0
9*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
A*	05	00	80	00	0	.	.	.	.	.	.	.	.	.	.	0
B*-F*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0

UEFI Windows - R5 M230

B	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0*	02	10	65	66	07	04	10	00	00	00	80	03	10	00	00	00
1*	0C	00	00	E0	0	.	.	0	04	00	2C	F0	0	.	.	0
2*	01	3F	00	00	0	.	.	.	.	.	.	0	AA	17	04	38
3*	00	00	00	00	48	00	00	00	0	.	.	0	00	01	00	00
4*	0	.	.	.	.	.	.	0	09	50	08	00	AA	17	04	38
5*	01	58	03	76	0	.	.	0	10	A0	12	00	A1	8F	00	00
6*	10	29	00	00	82	0C	40	00	00	00	81	10	0	.	.	0
7*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
8*	0	.	.	0	0E	00	00	00	02	00	01	00	0	.	.	0
9*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
A*	05	00	81	00	0C	F0	E0	FE	0	.	.	0	52	49	00	00
B*-F*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0

UEFI Windows HD8650G *(RW Everything, vs ...normal)*

G	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0*	02	10	0B	99	07	04	10	00	00	00	00	03	10	00	80	00
1*	08	00	00	D0	01	40	00	00	00	00	30	F0	0	.	.	0
2*	0	.	.	.	.	.	.	.	.	.	.	0	AA	17	04	38
3*	0	.	.	0	50	00	00	00	0	.	.	0	0	01	00	00
4*	0	.	.	.	.	.	.	.	.	.	.	0	AA	17	04	38
5*	01	58	03	06	0	.	.	0	10	A0	92	00	A0	8F	00	00
6*	10	08	00	00	0	.	.	.	.	.	.	.	.	.	.	0
7*-9*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
A*	05	00	81	00	0C	F0	E0	FE	00	00	00	00	62	49	00	00
B*-F*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0

Type	PCI Express	**Bus**	00	**Device**	01	**Function**	00
Width	01	**Device/ VendorID**	0x990B1002	**Revision ID**	0x00	**Class Code**	0x030000
Cacheline Size	0x10	**Latency Timer**	0x00	**Interrupt Pin**	INTA	**Interrupt Line**	None
BAR1	0xD0000008	**BAR2**	0x00004001	**BAR3**	0xF0300000	**BAR4**	0x00000000
BAR5	0x00000000	**BAR6**	0x00000000	**ExpansiROM**	0x00000000	**SubsysID**	0x380417AA

UEFI HD8650G – normal *(vs Windows)*

H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0*	02	10	0B	99	07	04	10	00	00	00	00	03	10	00	80	00
1*	08	00	00	D0	01	40	00	00	00	00	30	F0	0	.	.	0
2*	0	.	.	.	.	.	.	.	.	.	.	0	AA	17	04	38
3*	0	.	.	0	50	00	00	00	0	.	.	0	$_0B$	01	00	00
4*	0	.	.	.	.	.	.	.	.	.	.	0	AA	17	04	38
5*	01	58	03	06	0	.	.	0	10	A0	92	00	A0	8F	00	00
6*	10	$_09$	00	00	0	.	.	.	.	.	.	.	.	.	.	0
7*-9*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
A*	05	00	81	00	$_04$	2_0	E0	FE	0	.	.	0	28	$_40$	00	00
B*-F*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0

00:01.0 VGA compatible controller: Advanced Micro Devices, Inc. [AMD/ATI] Richland [Radeon HD 8650G]

UEFI HD8650G – normal *(vs J, ...nomodeset)*

I	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0*	02	10	0B	99	07	$_04$	10	00	00	00	00	03	10	00	80	00
1*	08	00	00	D0	01	40	00	00	00	00	30	F0	0	.	.	0
2*	0	.	.	.	.	.	.	.	.	.	.	0	AA	17	04	38
3*	0	.	.	0	50	00	00	00	0	.	.	0	0B	01	00	00
4*	0	.	.	.	.	.	.	.	.	.	.	0	AA	17	04	38
5*	01	58	03	06	0	.	.	0	10	A0	92	00	A0	8F	00	00
6*	10	09	$_00$	00	0	.	.	.	.	.	.	.	.	.	.	0
7*-9*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
A*	05	00	$_81$	00	$_04$	2_0	E_0	FE	0	.	.	0	28	4_0	00	00
B*-F*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0

UEFI HD8650G – nomodeset *(vs I,...normal)*

J	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0*	02	10	0B	99	07	00	10	00	00	00	00	03	10	00	80	00
1*	08	00	00	D0	01	40	00	00	00	00	30	F0	0	.	.	0
2*	0	.	.	.	.	.	.	.	.	.	.	0	AA	17	04	38
3*	0	.	.	0	50	00	00	00	0	.	.	0	0B	01	00	00
4*	0	.	.	.	.	.	.	.	.	.	.	0	AA	17	04	38
5*	01	58	03	06	0	.	.	0	10	A0	92	00	A0	8F	00	00
6*	10	09	0A	00	0	.	.	.	.	.	.	.	.	.	.	0
7*-9*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0
A*	05	00	80	00	0	.	.	.	.	.	.	.	.	.	.	0
B*-F*	0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0