HMC6545LP5E

v00.1012

32 Gbps Dual Channel Advanced Linear Equalizer

Typical Applications

- 40G/100G DQPSK Direct Detection Receivers
- Short and Long Reach CFP2 and QSFP+ Modules
- 100GbE Line Card CEI-28G MR and CEI-25G LR
- 16G and 32G Fiber Channel
- Infiniband 14G FDR and 28G EDR Rates
- Signal Conditioning for Backplane and Line Cards
- Broadband Test and Measurement Equipment

Features

Supports data rates from DC up to 32 Gbps

Protocol and data rate agnostic

Low latency (<170 ps)

No reference clock is required

Integrated AGC with differential sensitivity of lower than 50 mV

Up to 20 dB programmable multi UI input equalization at 25G-28G data rates

Extend chromatic and polarization mode dispersion tolerance

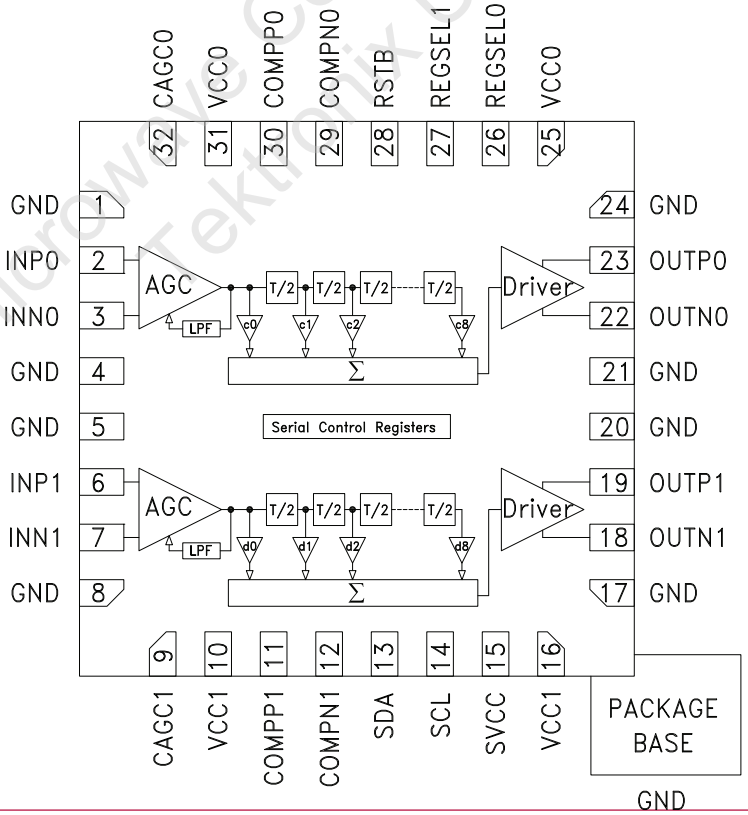
Programmable Differential Output Amplitude Control of up to 600 mV

Single 3.3V supply eliminating external regulators

Wide temperature range from -40°C to 95°C

5x5 mm 32-pin QFN package

Functional Diagram



32 Gbps Dual Channel Advanced Linear Equalizer

General Description

The HMC6545LP5E is a low power, high performance, fully programmable dual channel asynchronous advanced linear equalizer that operates with data rates up to 32 Gbps. The HMC6545LP5E is protocol and data rate agnostic and it can operate on the transmit path to pre-distort transmitted signal in order to invert channel distortion or on the receiver path to equalize the distorted and attenuated received signal. The HMC6545LP5E is effective in dealing with chromatic and polarization mode dispersion and inter-symbol interference (ISI) caused by wide variety of transmission media, backplane and or fiber, and channel lengths.

The HMC6545LPE consists of an automatic gain control (AGC), DC offset correction circuitry, 9-tap 18 ps spaced feed forward equalizer (FFE), summing node, and linear programmable output driver. The input AGC linearly attenuates or amplifies the distorted input signal to generate a constant voltage at the input of FFE. The 9-tap FFE is programmed via two wire interface (TWI) to generate wide range frequency responses that are either pre-cursor or post cursor in nature for compensating signal impairments. After FFE tap coefficients are summed at the summing node, the signal is received by linear output driver. DC offset correction circuitry is controlled either automatically or manually via Forward Error Correction (FEC).

All high speed differential inputs and outputs of the HMC6545LPE are CML and terminated on-chip with 50 Ohms to the positive supply, 3.3V, and may be DC or AC coupled. The inputs and outputs of HMC6545LP5E can be operated either differentially or single ended. The low power, high performance and feature rich HMC6545LP5E is packaged in a 5x5 mm 32 pin QFN package. The device uses a single 3.3V supply eliminating external regulators. The HMC6545LP5E operates over temperature range of -40°C up to +95°C.

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DC Electrical Characteristics

Unless otherwise noted: Typical values at V_{CC} = +3.3V, T_A = +25°C

Parameter	Symbol	Conditions	Min.	Typ.	Max	Units
Power Consumption						
Supply Voltage	V_{CC}		3.00	3.30	3.45	V
Supply Current	I_{CCMAX}	Single channel all tap amplifiers are active		130	150	mA
	I_{CCMIN}	Single channel single tap amplifier is active		93		
Power Down Supply Current				17		
Automatic DC Offset Correction		At maximum AGC gain	-60		60	mV
Manual DC Offset Correction		At maximum AGC gain	-60		60	mV
CML Input Port (INP0-INN0, INP1-INN1)						
Input Termination	R_{IN}	Differential input resistance	80	100	120	ohm
CML Output Port (OUTP0-OUTN0, OUTP1-OUTN1)						
Output Termination	R_{OUT}	Single ended output resistance	45	55	65	ohm
Output High Level	V_{OH}		V_{CC}			V
Output Low Level	V_{OL}				V_{CC} - 0.5	V
CMOS Input (SDA, SCL, RSTB, REGSEL0, REGSEL1)						
Input High Level	V_{IH}		V_{CC} - 1.3			V
Input Low Level	V_{IL}				0.8	V
Input Current	I_{IL}, I_{IH}	V_{IL1} = 0V or V_{IH1} = V_{CC}	-100		100	uA

AC Electrical Characteristics

Unless otherwise noted: Typical values at V_{CC} = +3.3V, T_A = +25°C

Parameter	Conditions	Min.	Typ.	Max	Units
Input Data Rate		DC		32	Gbps
Input Range [1]	Differential input range for linear AGC operation	40		880	mV_{PP}
Differential Input Amplitude		40		1600	mV_{PP}
Differential Output Amplitude	Linear AGC operation [1] [2] [3] [6]		410		mV_{PP}
	Linear AGC operation [2] [4] [6]		600		mV_{PP}
	Saturated AGC operation [4] [5] [6]		960		mV_{PP}
AGC Settling Time	No external cap		0.5		usec
FFE Tap Delay			18		psec
FFE Delay Depth			145		psec
Channel to Channel Isolation	Up to 32 GHz		30		dB
Total Harmonic Distortion	AGC=2, for differential input voltage≤250mV_{PP}			5	%
Output Driver Rise/Fall Times	%20 to %80		16		psec
Additive RMS jitter [2] [3] [7] [8]	1010 pattern			0.4	psec
Differential input return loss	Up to 20 GHz	-9			dB
Differential output return loss	Up to 20 GHz	-8			dB
Number of Taps			9		

[1] THD < 5% [2] All taps are enabled, Tap4 gain=+63, rest of the taps' gain=0,Pre Driver Gain=63. [3] AGC=2 [4] AGC=7
[5] All taps are enabled with maximum gain, Pre Driver Gain=63. [6] Input signal: PRBS 2^{31}-1 @100mV_{PP}
[7] Input signal:28Gbps 1010... pattern [8] Additive RMS jitter is calculated by $J_{RMS,DUT} = \sqrt{[(Jtested)^2 - (Jsource)^2]}$

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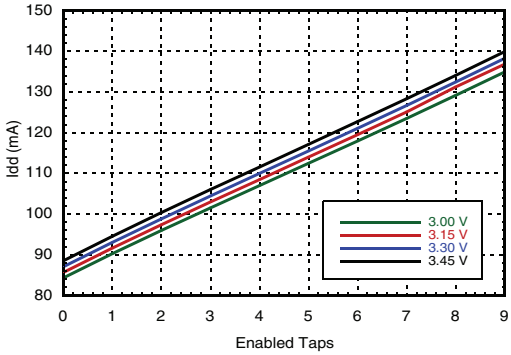
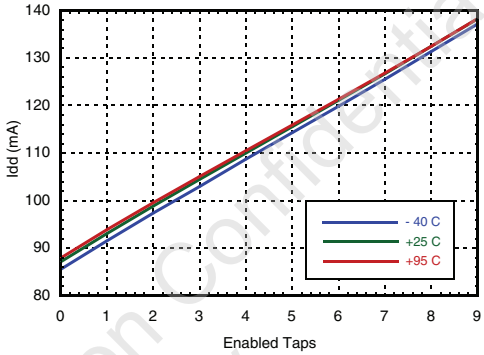
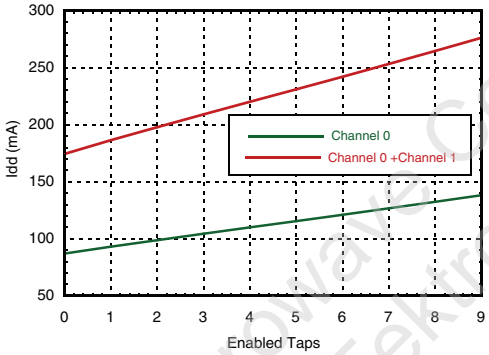
Supply Current vs. Enabled Taps Over Supply Voltage [1]



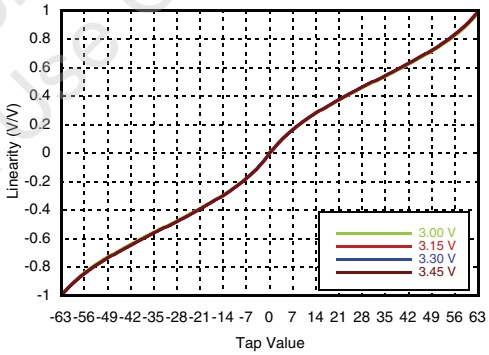
Supply Current vs. Enabled Taps Over Temperature [2]



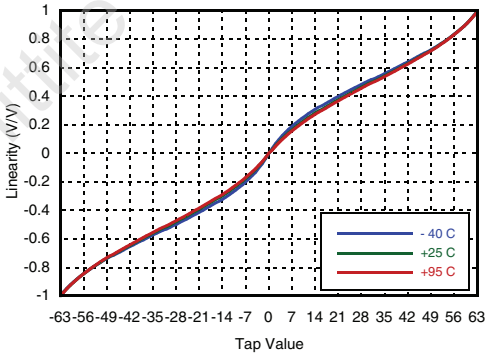
Supply Current vs. Enabled Taps Over Enabled Channels [1] [2] [3]



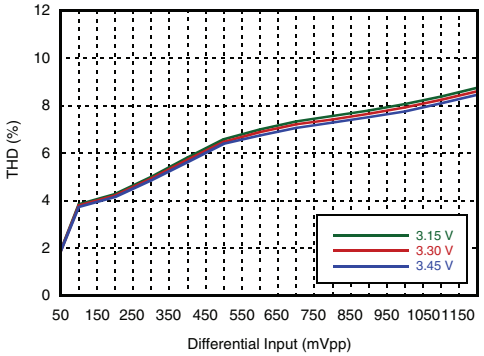
Normalized Linearity vs. Tap Value Over Supply Voltage [1] [3] [4]



Normalized Linearity vs. Tap Value Over Temperature [2] [3] [4]



THD vs. Differential Input Amplitude Over Supply Voltage [1] [5]



[1] T_A = +25C, [2] V_{CC} = 3.3V, [3] AGC = 3, Pre Driver Gain = 63
[4] Tap 4 value is varied, while others are enabled with no gain
[5] AGC = 2, Pre Driver Gain = 63, Tap 4 gain is set to +63, while others are enabled with no gain

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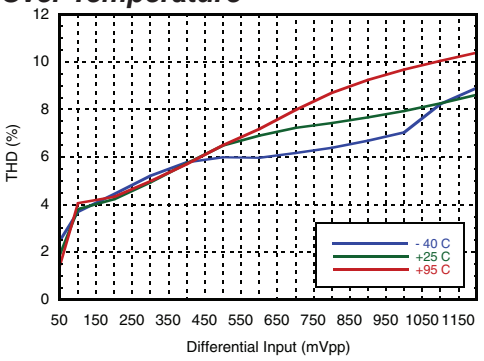
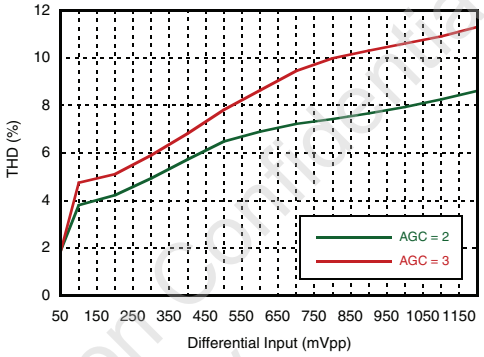
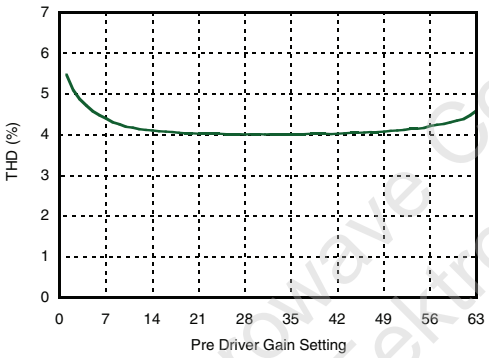
THD vs. Differential Input Amplitude Over Temperature [2] [3] [4] [5]



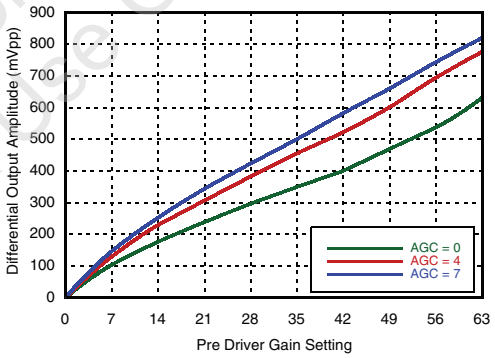
THD vs. Differential Input Amplitude Over AGC Value [1] [2] [4] [5]



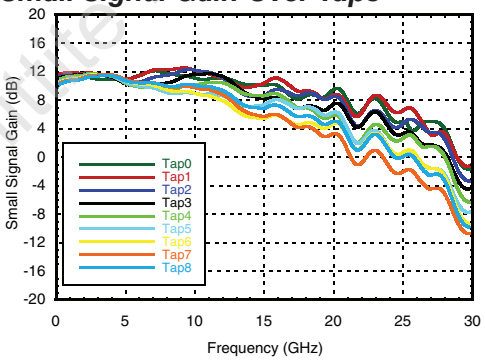
THD vs. Pre Driver Gain [1] [2] [3] [5]



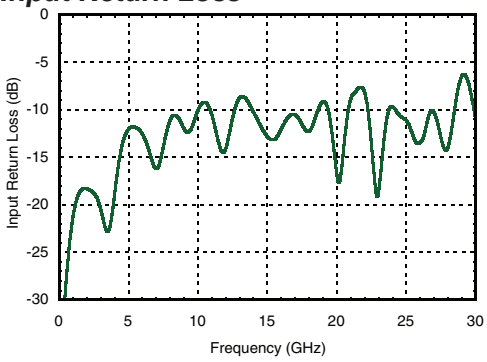
Differential Output Amplitude vs. Pre Driver Gain Over AGC [1] [2] [6] [7]



Small Signal Gain Over Taps [1] [2] [8]



Input Return Loss [1] [2]



[1] T_A = +25C [2] V_{CC} = 3.3V [3] AGC = 2 [4] Pre Driver Gain = 63
[5] Tap 4 gain is set to max gain, while others are enabled with no gain [6] Input signal: Differential PRBS 2^{31}-1, 10Gbps @500 mV_{PP}
[7] AGC=4, Pre Driver Gain=7, Tap0=-3, Tap1=-8, Tap2=-4, Tap3=63, Tap4=63, Tap5=57, Tap6=18, Tap7=-41, Tap8=-35
[8] For each tap's S21 line, relevant tap is set to maximum gain while remaining taps are enabled with no gain

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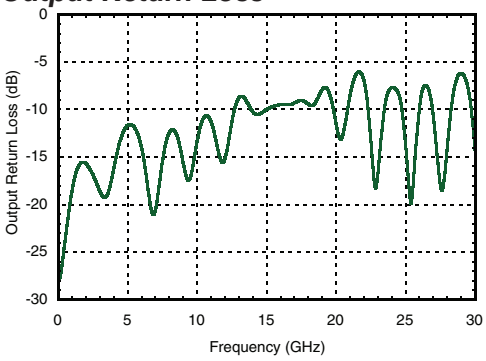
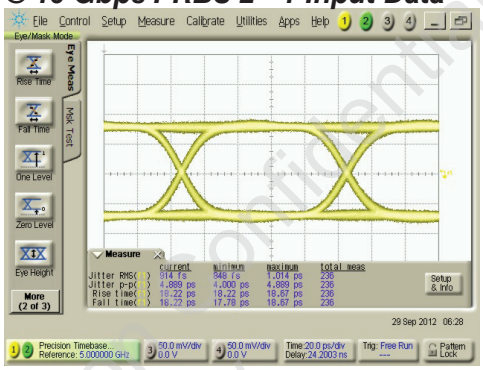
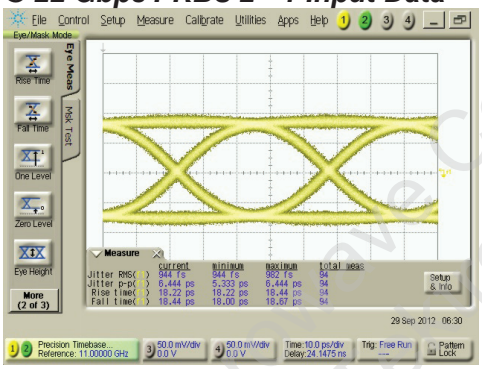
Output Return Loss [1] [2]



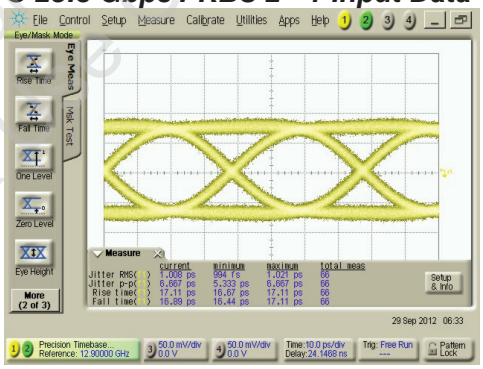
Typical Output Waveform @ 10 Gbps PRBS 2^{31}-1 Input Data [3]



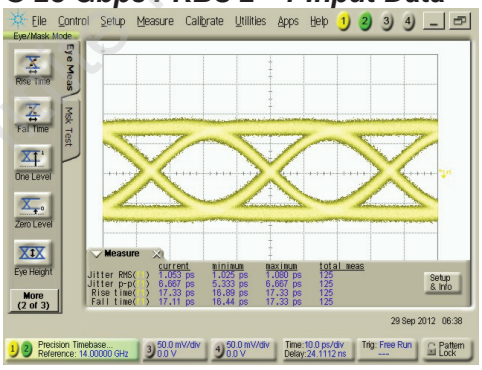
Typical Output Waveform @ 22 Gbps PRBS 2^{31}-1 Input Data [3]



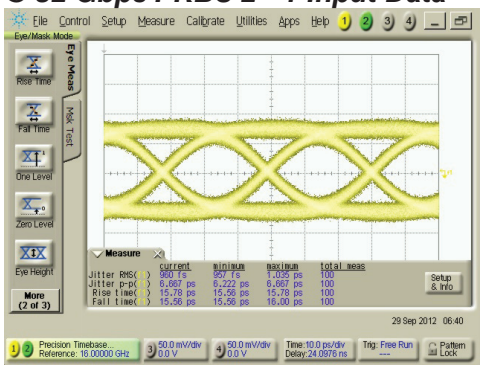
Typical Output Waveform @ 25.8 Gbps PRBS 2^{31}-1 Input Data [3]



Typical Output Waveform @ 28 Gbps PRBS 2^{31}-1 Input Data [3]



Typical Output Waveform @ 32 Gbps PRBS 2^{31}-1 Input Data [3]



[1] TA= +25C [2]VCC = 3.3V

[3] Input signal = 300mVpp differential PRBS 2^{31}-1. Tap0 = -3, Tap1 = 63, Tap2 = -10, Tap3 = -4, Tap4 = -1, Tap5 = -1, Tap6 = -1, Tap7 = -1, Tap8 = -2 Pre Driver Gain = 63, AGC = 4

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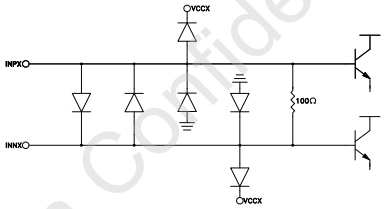
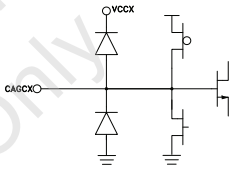
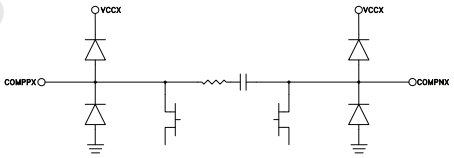
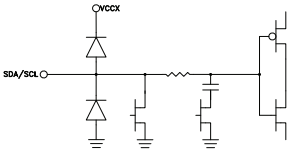
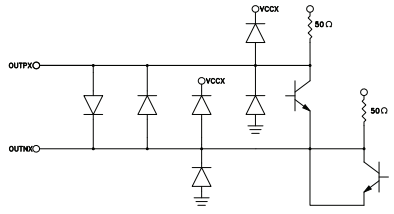
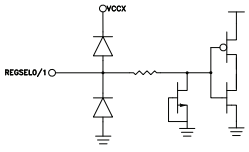
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1,4,5,8,17,20,21,24	GND	This pin and the package base must be connected to RF and DC ground.	
2,3,6,7	INP0,INN0, INP1,INN1	Differential CML Input.	
9,32	CAGC1, CAGC0	External capacitor for AGC bandwidth	
10,16,25,31	VCC1,VCC1, VCC0,VCC0	Power supply for channel 0 and channel 1	
11,12,29,30	COMPP1, COMPN1, COMPN0, COMPP0	External capacitor DC offset cancel.	
13,14	SDA, SCL	Two wire digital data and clock	
15	SVCC	Power supply for digital and bias	
18,19,22,23	OUTN1, OUTP1, OUTN0, OUTP0	Differential CML data output.	
26,27	REGSEL0, REGSEL1	Default coefficient selection for channel & TWI device address.	
28	RSTB	Reset for TWI	

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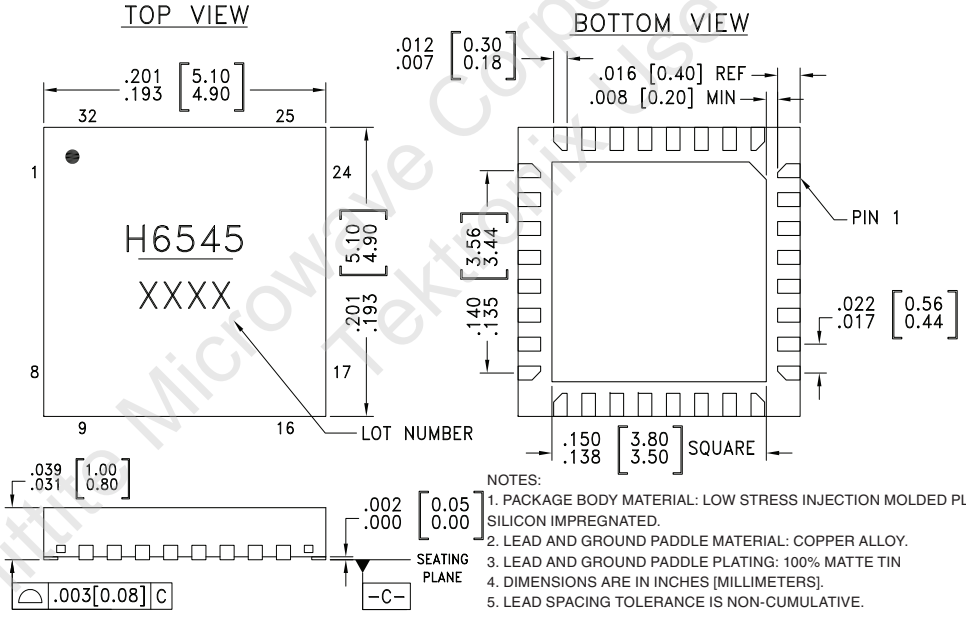
Absolute Maximum Ratings

Vcc to GND	-0.6V to +3.6V
All pins to GND	-0.3V to Vcc + 0.3V
Operating Ambient Temperature Range	-40°C to +95°C
Differential Peak to Peak Input Voltage Swing	1.4 Vpp
Maximum Input Voltage at CML Inputs	Vcc + 0.6V
Maximum Input Voltage at Digital Inputs (SDA, SCL, REGSEL1, REGSEL0, RSTB)	Vcc + 0.6V
Maximum Junction Temperature	125 °C
Continuous Power Dissipation (T=85C) (derate 46.59 mW/C above 85C)	1.86W
Thermal Resistance (junction to ground pedal)	21.46°C/W
ESD Sensitivity (HBM)	Class 1C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:
1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. CHARACTERS TO BE HELVETICA MEDIUM, .025 HIGH, WHITE INK, OR LASER MARK LOCATED APPROX. AS SHOWN.
7. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.05mm MAX.
8. PACKAGE WARP SHALL NOT EXCEED 0.05mm
9. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
10. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking[1]
HMC6545LP5E	RoHS-compliant Low Stress injection Molded Plastic	100% matte Sn	MSL1 [2]	H6545 XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260°C

Detailed Description

The HMC6545LP5E advanced linear equalizer has two symmetrical channels each containing an input AGC, a 9-tap delay chain with each delay tap connected to a variable tap-amplifier, a summation node combining the outputs of the tap-amplifiers, and an output driver.

a.Input Receiver

i. AGC

The HMC6545LP5E has an integrated AGC that linearly amplifies/attenuates the input signal generating a fixed voltage swing level for further processing in the FFE delay line. An input AGC is required both to supply a well-defined voltage swing level to the FFE delay line and also for controlling the internal and external (output) voltage swings since the signal path is linear. The AGC has a sensitivity level of 40 mV_{PP} differential and an overload level of 600mV_{PP} differential, where it can process the input signal linearly.

The AGC loop bandwidth and settling time can be changed using an external capacitor connected to the nodes CAGC0-GND and CAGC1-GND. There is an internal 2.5pF capacitor at this node setting the default AGC settling time to 0.5usec. The evaluation board includes 1nF capacitors for both channels.

ii. Internal and External Offset Correction Circuitry

The input receiver has two modes of offset correction that can be configured changing the offset settings register via TWI (all registers below are identical to each other):

REGISTER	DESCRIPTION
Reg 0x0A	Channel 0 Offset Settings A Register
Reg 0x2A	Channel 0 Offset Settings B Register
Reg 0x4A	Channel 1 Offset Settings A Register
Reg 0x6A	Channel 1 Offset Settings B Register

1. Automatic offset correction
2. Manual offset correction

By default, the input receiver is configured in the automatic offset correction mode which can correct up to +/-60mV input referred DC offset at the worst case AGC gain (maximum AGC gain with minimum input signal level). The input referred automatic offset correction range changes depending on the AGC gain and increases up to +/-180mV for minimum AGC gain with maximum signal level at the input of the receiver.

Automatic offset correction loop bandwidth is externally set by a series RC network (for each channel, R1-C1 and R2-C2) and it is recommended to keep the component values as suggested in the evaluation board schematic.

Automatic offset correction loop can be disabled by setting the register Reg0x4A[6] bit to 0, which enables the manual offset correction. Manual offset correction amount can be adjusted by configuring the Reg0x4A[5:0] bits, where Reg0x4A[5] bit defines the sign and the Reg0x4A[4:0] bits define the magnitude. Similar to automatic offset correction mode, manual offset correction dynamic range changes with the AGC gain with the total correction being +/-60mV for maximum AGC gain. This corresponds to about 2mV/step (5 bit control) adjustment resolution for maximum AGC gain. For minimum AGC gain, the correction dynamic range increases to +/-180mV, and the minimum step for adjustment increases to 6mV/step

Reg 0x4A	Channel 1 Offset Settings A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[4:0]	R/W	Manual Offset Gain	0x00	Channel 1 Manual Offset Gain
[5]	R/W	Manual Offset Sign	0	Channel 1 Manual Offset Sign
[6]	R/W	Automatic Offset Enable	1	Channel 1 Automatic Offset Enable
[7]	R/W	Factory Set	0	Not used

b. FFE Delay Line

The FFE delay line receives an input signal from the AGC (with a controlled magnitude) and this signal propagates along a delay line composed of 8 delay elements where each delay element has 18 ps nominal propogation. The delayed signals are then multiplied by programmable coefficients by the tap amplifiers and summed together. One of the taps near the center can be selected as the main tap, while the taps that follow are called post-cursor and taps that precede are called pre-cursor taps.

By combining different tap values, a wide variety of filter transfer functions can be created that can, for example, compensate for the gain or phase distortion of a lossy channel or the chromatic dispersion of an optical channel.

Tap amplifier gains are controlled using the TWI with 5 bits of magnitude resolution with positive or negative polarity. To disable a coefficient, it is recommended to set the gain of the particular tap amplifier to 0 (positive gain sign, and 0 gain setting). In addition, the tap amplifier can be powered down to save power but this may have an impact on delay and gain of remaining taps at the delay chain. An example tap amplifier setting register is shown below.

Channel 0 Tap 0 Settings A Register				
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 0 Gain	0	Channel 0 Tap 0 Gain
[6]	R/W	Tap 0 Gain Sign	1	Channel 0 Tap 0 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 0 Enable	1	Channel 0 Tap 0 Enable

Each channel has two sets of tap coefficient register arrays (Channel0-A, Channel0-B, Channel1-A, Channel1-B) that can be configured through the TWI. Registers Reg0x00 to Reg0x08 are used to set the tap coefficients of Channel 0-A register array; registers Reg0x20 to Reg0x28 are used to set the tap coefficients of Channel 0-B register array; registers Reg0x40 to Reg0x48 are used to set the tap coefficients of Channel 1-A register array; and registers Reg0x60 to Reg0x68 are used to set the tap coefficients of Channel 1-B register array. REGSEL0 and REGSEL1 pins of the part are used to set the default register array(A or B) determining the tap coefficients of a particular channel. For example, applying REGSEL0 (REGSEL1)=0 activates the Channel0-A (Channel1-A) register array for setting the channel coefficients and applying REGSEL0 (REGSEL1)=1 activates the Channel0-B (Channel1-B) register array for setting the channel coefficients.

c. Output Driver

After the tap amplifier outputs are summed, the combined signal is received by a linear output driver. The output driver consists of two stages, with the first stage being a pre-driver stage providing controllable signal amplification (6 bits resolution) using the registers Reg0x09 (Channel0-A), Reg0x29 (Channel0-B), Reg0x49 (Channel1-A), and Reg0x69 (Channel1-B). Similar to the tap coefficient registers, each pre-driver has two registers that can be selected by the pins REGSEL0 and REGSEL1 asynchronously. The register values should be configured through the TWI prior to the described selection.

Related register table is provided below.

Reg 0x09	Channel 0 Pre Driver Settings A Register					
BIT	TYPE	NAME	DEFLT	MIN.	MAX.	DESCRIPTION
[5:0]	R/W	Pre Driver Gain	0x3F	000000	111111	Channel 0 Pre Driver Gain
[7:6]	R/W	Factory Set	0b00			Not Used
Reg 0x29	Channel 0 Pre Driver Settings B Register					
BIT	TYPE	NAME	DEFLT	MIN	MAX	DESCRIPTION
[5:0]	R/W	Pre Driver Gain	0x30	000000	111111	Channel 0 Pre Driver Gain
[7:6]	R/W	Factory Set	0b00			Not Used
Reg 0x49	Channel 1 Pre Driver Settings A Register					
BIT	TYPE	NAME	DEFLT	MIN	MAX	DESCRIPTION
[5:0]	R/W	Pre Driver Gain	0x3F	000000	111111	Channel 1 Pre Driver Gain
[7:6]	R/W	Factory Set	0b00			Not Used
Reg 0x69	Channel 1 Pre Driver Settings B Register					
BIT	TYPE	NAME	DEFLT	MIN	MAX	DESCRIPTION
[5:0]	R/W	Pre Driver Gain	0x30	000000	111111	Channel 1 Pre Driver Gain
[7:6]	R/W	Factory Set	0b00			Not Used

The final stage of the output driver is a 50 Ohm CML driver stage that provides the specified linearity (according to the THD specification) up to 600 mV_{PP} differential output swing. The linearity degrades at higher output swings.

d. Two-Wire Serial Port

To access all its internal registers, the HMC6545LP5E uses a two-wire interface, which consists of a Serial Data Line (SDA) and a Serial Clock Line (SCL). Both SDA and SCL are implemented with open-drain I/O pins and are connected to a positive supply voltage via pull-up resistors.

Typically, a microcontroller, a microprocessor or a digital signal processor acts as a master, controls the bus and has the responsibility to generate the clock signal and device addresses.

The HMC6545LP5E functions as a slave device. The device address on the HMC6545LP5E is 0x38 default and set by connecting REGSEL0, REGSEL1 pins to either Vcc (logic 1) or GND (logic 0) and writing 1 to Reg80[6]. If Reg0x80[6]= 0(default), then REGSEL0 and REGSEL1 pins are used to select register A or register B. If Reg0x80[6]=1, REGSEL0 and REGSEL1 pins also determine the TWI device address according to table below.

REGSEL1	REGSEL0	TWI Device Address if Reg0x80[6]=1
0	0	0x38 (Default)
0	1	0x39
1	0	0x3A
1	1	0x3B

Protocol

The following are some definitions and conditions occurring in a two-wire data transfer.

START condition: is always generated by the master and is defined as a High to Low transition on the SDA line while SCL is High. The bus becomes busy after a START condition.

STOP condition: is always generated by the master and is defined as a Low to High transition on the SDA line while SCL is High. The bus becomes free after the STOP condition occurs.

Byte format: every byte transmitted on SDA must be 8 bits long and is transferred with the Most Significant Bit (MSB) first. Each byte must be followed by and Acknowledge bit.

Data Valid condition: for data to be considered valid, the SDA line must be stable during the entire high period of its respective clock pulse.

Acknowledge: for each byte sent or received on the bus the master generates an extra clock cycle that is used for acknowledgement, for a total of 9 bits. The transmitter releases the SDA line, which is pulled High by the external resistor, and the receiver must pull down the SDA line and drive it Low while SCL is High in this entire clock cycle to indicate acknowledgment. SDA is left High during this clock cycle to indicate a Not-acknowledge situation, usually because the device addressed is unable to receive or transmit the data requested.

Figure 1 shows a representation of a complete communication cycle on the two wire interface.

The master generates a Start condition to indicate the beginning of a new data transfer.

The master then starts generating clock pulses on SCL and transmits the first byte on SDA. This first byte always consists of a 7-bit slave address followed by 1 bit that indicates the Read/Write direction (R/W). The device on the bus with a matching address generates an acknowledge.

The master continues generating more clock pulses on SCL and, depending on the value of the R/W bit, it sends (Write operation, R/W bit set to 0) or receives (Read operation, R/W bit set to 1) data on SDA. In each case the receiver must acknowledge the data sent by the transmitter. This sequence of 8-bit data followed by a 1-bit acknowledge may be repeated multiple times.

When all data communication is over for the current transfer cycle the master indicates the end of data transfer by generating a Stop condition.

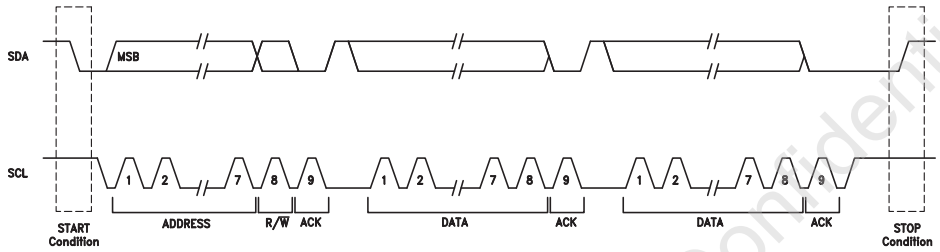


Figure 1. Complete data transfer.

Data Transfer Formats

Write Cycle (master transmitter sends data to slave receiver. See Figure 2: the transfer direction is from Master to Slave and does not change. The master generates a Start condition followed by a 7-bit slave address followed by the R/W bit set to 0. The slave with a matching address replies with an acknowledge. The master then transmits the first byte to the slave device, this first byte is an address of the internal registers of the slave. The slave device replies with an acknowledge bit. For a subsequent Read cycle the master generates a stop bit, otherwise the master then transmits the next byte, which is now a data byte to be stored in the internal slave register previously addressed. This is followed by an acknowledge bit from the slave. This process can continue for multiple bytes and the slave device increments its internal register address count as it receives subsequent bytes from the master. When all data transfer is over, the master generates a Stop condition to end the cycle.

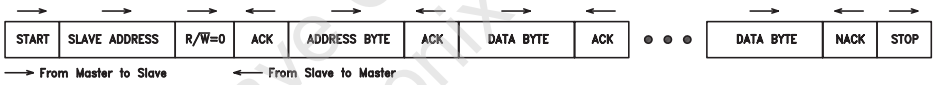


Figure 2. Master transmitter writes to slave recei

Read Cycle (master reads from slave immediately after first byte. See Figure 3: the direction of data transfer changes between master and slave. In this case the R/W bit is set to 1 to indicate that the master will read data from the slave device. The address of the internal register from which the data is to come has been previously set in a precedent Write cycle, otherwise the slave device defaults to address 0. This time the slave device transmits all the data bytes and the master replies with an acknowledge bit, except for the last byte read, in which case the master replies with a No-acknowledge bit to indicate to the slave that it must stop transmitting data. The master then generates a Stop condition and the cycle ends.

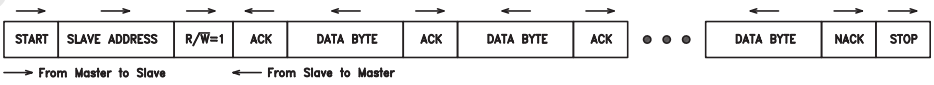


Figure 3. Master reads from slave.

For price, delivery and to place orders: Hittite Microwave Corporation, 2 Elizabeth Drive, Chelmsford, MA 01824
Phone: 978-250-3343 Fax: 978-250-3373 Order On-line at www.hittite.com
Application Support: Phone: 978-250-3343 or fo@hittite.com

Register Map - Summary of Register List and Register Descriptions

Global Register

Global register's bit order is different for read and write operations.

Reg 0x80	Global Register, Write Operation			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[0]	W	Global Reset	1	Global Soft Reset. Write 0 generates soft reset. Resets all the registers to default states. Writing 1 resumes normal chip operation.
[1]	W	Channel 0 Reset	1	Channel 0 Soft Reset. Write 0 generates soft reset. Resets all the registers in Channel 1 to default states. Writing 1 resumes normal chip operation.
[2]	W	Channel 1 Reset	1	Channel 1 Soft Reset. Write 0 generates soft reset. Resets all the registers in Channel 1 to default states. Writing 1 resumes normal chip operation.
[3]	W	Factory Set	1	Not used
[4]	W	Channel 0 Enable	1	Channel 0 Enable. Write 1 enables Channel0.
[5]	W	Channel 1 Enable	1	Channel 1 Enable. Write 1 enables Channel1.
[6]	W	TWI Device Address Read	0	TWI Device Address Set. Write 1 generates TWI Device Addrress Read Command
[7]	W	Factory Set	0	Not used

Reg 0x80	Global Register, Read Operation			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[0]	R	Factory Set	0	Not used
[1]	R	Channel 1 Reset	1	Channel 1 Reset
[2]	R	Factory Set		Not used
[3]	R	Channel 0 Enable		Channel0 Enable
[4]	R	Channel 1 Enable		Channel1 Enable
[5]	R	Factory Set		Not used
[6]	R	TWI Device Address[0]		Least significant bit of device address
[7]	R	TWI Device Address[1]		Bit 1 of device address

Channel 0 A Register Set

Reg 0x00	Channel 0 Tap 0 Settings A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 0 Gain	0x00	Channel 0 Tap 0 Gain
[6]	R/W	Tap 0 Gain Sign	1	Channel 0 Tap 0 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 0 Enable	1	Channel 0 Tap 0 Enable
Reg 0x01	Channel 0 Tap 1 Settings A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 1 Gain	0x04	Channel 0 Tap 1 Gain
[6]	R/W	Tap 1 Gain Sign	0	Channel 0 Tap 1 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 1 Enable	1	Channel 0 Tap 1 Enable
Reg 0x02	Channel 0 Tap 2 Settings A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 2 Gain	0x3F	Channel 0 Tap 2 Gain
[6]	R/W	Tap 2 Gain Sign	1	Channel 0 Tap 2 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 2 Enable	1	Channel 0 Tap 2 Enable
Reg 0x03	Channel 0 Tap 3 Settings A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 3 Gain	0x28	Channel 0 Tap 3 Gain
[6]	R/W	Tap 3 Gain Sign	0	Channel 0 Tap 3 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 3 Enable	1	Channel 0 Tap 3 Enable
Reg 0x04	Channel 0 Tap 4 Settings A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 4 Gain	0x04	Channel 0 Tap 4 Gain
[6]	R/W	Tap 4 Gain Sign	0	Channel 0 Tap 4 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 4 Enable	1	Channel 0 Tap 4 Enable
Reg 0x05	Channel 0 Tap 5 Settings A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 5 Gain	0x00	Channel 0 Tap 5 Gain
[6]	R/W	Tap 5 Gain Sign	1	Channel 0 Tap 5 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 5 Enable	1	Channel 0 Tap 5 Enable
Reg 0x06	Channel 0 Tap 6 Settings A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 6 Gain	0x00	Channel 0 Tap 6 Gain
[6]	R/W	Tap 6 Gain Sign	1	Channel 0 Tap 6 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 6 Enable	1	Channel 0 Tap 6 Enable
Reg 0x07	Channel 0 Tap 7 Settings A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 7 Gain	0x00	Channel 0 Tap 7 Gain
[6]	R/W	Tap 7 Gain Sign	1	Channel 0 Tap 7 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 7 Enable	1	Channel 0 Tap 7 Enable

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Reg 0x08	Channel 0 Tap 8 Settings A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 8 Gain	0x00	Channel 0 Tap 8 Gain
[6]	R/W	Tap 8 Gain Sign	0	Channel 0 Tap 8 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 8 Enable	1	Channel 0 Tap 8 Enable
Reg 0x09	Channel 0 Pre Driver Settings A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Pre Driver Gain	0x3F	Channel 0 Pre Driver Gain
[7:6]	R/W	Factory Set	0b00	Not Used
Reg 0x0A	Channel 0 Offset Settings A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[4:0]	R/W	Manual Offset Gain	0x00	Channel 0 Manual Offset Gain
[5]	R/W	Manual Offset Sign	0	Channel 0 Manual Offset Sign
[6]	R/W	Automatic Offset Enable	1	Channel 0 Automatic Offset Enable.
[7]	R/W	Factory Set	0	Not Used
Reg 0x0B	Channel 0 Internal AGC Amplitude A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[2:0]	R/W	Internal AGC Amplitude	0b100	Internal AGC Amplitude
[7:3]	R/W	Factory Set	0x00	Not Used

Channel 0 B Register Set

Reg 0x20	Channel 0 Tap 0 Settings B Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 0 Gain	0x00	Channel 0 Tap 0 Gain
[6]	R/W	Tap 0 Gain Sign	1	Channel 0 Tap 0 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 0 Enable	1	Channel 0 Tap 0 Enable
Reg 0x21	Channel 0 Tap 1 Settings B Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 1 Gain	0x04	Channel 0 Tap 1 Gain
[6]	R/W	Tap 1 Gain Sign	0	Channel 0 Tap 1 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 1 Enable	1	Channel 0 Tap 1 Enable
Reg 0x22	Channel 0 Tap 2 Settings B Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 2 Gain	0x00	Channel 0 Tap 2 Gain
[6]	R/W	Tap 2 Gain Sign	1	Channel 0 Tap 2 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 2 Enable	1	Channel 0 Tap 2 Enable
Reg 0x23	Channel 0 Tap 3 Settings B Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 3 Gain	0x00	Channel 0 Tap 3 Gain
[6]	R/W	Tap 3 Gain Sign	1	Channel 0 Tap 3 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 3 Enable	1	Channel 0 Tap 3 Enable
Reg 0x24	Channel 0 Tap 4 Settings B Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 4 Gain	0x3F	Channel 0 Tap 4 Gain
[6]	R/W	Tap 4 Gain Sign	1	Channel 0 Tap 4 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 4 Enable	1	Channel 0 Tap 4 Enable
Reg 0x25	Channel 0 Tap 5 Settings B Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 5 Gain	0x00	Channel 0 Tap 5 Gain
[6]	R/W	Tap 5 Gain Sign	1	Channel 0 Tap 5 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 5 Enable	1	Channel 0 Tap 5 Enable
Reg 0x26	Channel 0 Tap 6 Settings B Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 6 Gain	0x00	Channel 0 Tap 6 Gain
[6]	R/W	Tap 6 Gain Sign	1	Channel 0 Tap 6 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 6 Enable	1	Channel 0 Tap 6 Enable
Reg 0x27	Channel 0 Tap 7 Settings B Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 7 Gain	0x00	Channel 0 Tap 7 Gain
[6]	R/W	Tap 7 Gain Sign	1	Channel 0 Tap 7 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 7 Enable	1	Channel 0 Tap 7 Enable

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Reg 0x28	Channel 0 Tap 8 Settings B Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 8 Gain	0x00	Channel 0 Tap 8 Gain
[6]	R/W	Tap 8 Gain Sign	1	Channel 0 Tap 8 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 8 Enable	1	Channel 0 Tap 8 Enable
Reg 0x29	Channel 0 Pre Driver Settings B Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Pre Driver Gain	0x30	Channel 0 Pre Driver Gain
[7:6]	R/W	Factory Set	0b00	Not Used
Reg 0x2A	Channel 0 Offset Settings B Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[4:0]	R/W	Manual Offset Gain	0x00	Channel 0 Manual Offset Gain
[5]	R/W	Manual Offset Sign	0	Channel 0 Manual Offset Sign
[6]	R/W	Automatic Offset Enable	1	Channel 0 Automatic Offset Enable
[7]	R/W	Factory Set	0	Not Used
Reg 0x2B	Channel 0 Internal AGC Amplitude B Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[2:0]	R/W	Internal AGC Amplitude	0b100	Internal AGC Amplitude
[7:3]	R/W	Factory Set	0x00	Not Used

Channel 1 A Register Set

Reg 0x40	Channel 1 Tap 0 Settings A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 0 Gain	0x00	Channel 1 Tap 0 Gain
[6]	R/W	Tap 0 Gain Sign	1	Channel 1 Tap 0 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 0 Enable	1	Channel 1 Tap 0 Enable
Reg 0x41	Channel 1 Tap 1 Settings A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 1 Gain	0x04	Channel 1 Tap 1 Gain
[6]	R/W	Tap 1 Gain Sign	0	Channel 1 Tap 1 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 1 Enable	1	Channel 1 Tap 1 Enable
Reg 0x42	Channel 1 Tap 2 Settings A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 2 Gain	0x3F	Channel 1 Tap 2 Gain
[6]	R/W	Tap 2 Gain Sign	1	Channel 1 Tap 2 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 2 Enable	1	Channel 1 Tap 2 Enable
Reg 0x43	Channel 1 Tap 3 Settings A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 3 Gain	0x28	Channel 1 Tap 3 Gain
[6]	R/W	Tap 3 Gain Sign	0	Channel 1 Tap 3 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 3 Enable	1	Channel 1 Tap 3 Enable
Reg 0x44	Channel 1 Tap 4 Settings A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 4 Gain	0x04	Channel 1 Tap 4 Gain
[6]	R/W	Tap 4 Gain Sign	0	Channel 1 Tap 4 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 4 Enable	1	Channel 1 Tap 4 Enable
Reg 0x45	Channel 1 Tap 5 Settings A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 5 Gain	0x00	Channel 1 Tap 5 Gain
[6]	R/W	Tap 5 Gain Sign	1	Channel 1 Tap 5 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 5 Enable	1	Channel 1 Tap 5 Enable
Reg 0x46	Channel 1 Tap 6 Settings A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 6 Gain	0x00	Channel 1 Tap 6 Gain
[6]	R/W	Tap 6 Gain Sign	1	Channel 1 Tap 6 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 5 Enable	1	Channel 1 Tap 6 Enable
Reg 0x47	Channel 1 Tap 7 Settings A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 7 Gain	0x00	Channel 1 Tap 7 Gain
[6]	R/W	Tap 7 Gain Sign	1	Channel 1 Tap 7 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 7 Enable	1	Channel 1 Tap 7 Enable

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Reg 0x48	Channel 1 Tap 8 Settings A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 8 Gain	0x00	Channel 1 Tap 8 Gain
[6]	R/W	Tap 8 Gain Sign	0	Channel 1 Tap 8 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 8 Enable	1	Channel 1 Tap 8 Enable
Reg 0x49	Channel 1 Pre Driver Settings A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Pre Driver Gain	0x3F	Channel 1 Pre Driver Gain
[7:6]	R/W	Factory Set	0b00	Not Used
Reg 0x4A	Channel 1 Offset Settings A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[4:0]	R/W	Manual Offset Gain	0x00	Channel 1 Manual Offset Gain
[5]	R/W	Manual Offset Sign	0	Channel 1 Manual Offset Sign
[6]	R/W	Automatic Offset Enable	1	Channel 1 Automatic Offset Enable.
[7]	R/W	Factory Set	0	Not Used
Reg 0x4B	Channel 1 Internal AGC Amplitude A Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[2:0]	R/W	Internal AGC Amplitude	0b100	Internal AGC Amplitude
[7:3]	R/W	Factory Set	0x00	Not Used

Channel 1 B Register Set

Reg 0x60	Channel 1 Tap 0 Settings B Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 0 Gain	0x00	Channel 1 Tap 0 Gain
[6]	R/W	Tap 0 Gain Sign	1	Channel 1 Tap 0 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 0 Enable	1	Channel 1 Tap 0 Enable
Reg 0x61	Channel 1 Tap 1 Settings B Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 1 Gain	0x00	Channel 1 Tap 1 Gain
[6]	R/W	Tap 1 Gain Sign	1	Channel 1 Tap 1 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 1 Enable	1	Channel 1 Tap 1 Enable
Reg 0x62	Channel 1 Tap 2 Settings B Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 2 Gain	0x00	Channel 1 Tap 2 Gain
[6]	R/W	Tap 2 Gain Sign	1	Channel 1 Tap 2 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 2 Enable	1	Channel 1 Tap 2 Enable
Reg 0x63	Channel 1 Tap 3 Settings B Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 3 Gain	0x00	Channel 1 Tap 3 Gain
[6]	R/W	Tap 3 Gain Sign	1	Channel 1 Tap 3 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 3 Enable	1	Channel 1 Tap 3 Enable
Reg 0x64	Channel 1 Tap 4 Settings B Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 4 Gain	0x3F	Channel 1 Tap 4 Gain
[6]	R/W	Tap 4 Gain Sign	1	Channel 1 Tap 4 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 4 Enable	1	Channel 1 Tap 4 Enable
Reg 0x65	Channel 1 Tap 5 Settings B Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 5 Gain	0x00	Channel 1 Tap 5 Gain
[6]	R/W	Tap 5 Gain Sign	1	Channel 1 Tap 5 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 5 Enable	1	Channel 1 Tap 5 Enable
Reg 0x66	Channel 1 Tap 6 Settings B Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 6 Gain	0x00	Channel 1 Tap 6 Gain
[6]	R/W	Tap 6 Gain Sign	1	Channel 1 Tap 6 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 6 Enable	1	Channel 1 Tap 6 Enable
Reg 0x67	Channel 1 Tap 7 Settings B Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 7 Gain	0x00	Channel 1 Tap 7 Gain
[6]	R/W	Tap 7 Gain Sign	1	Channel 1 Tap 7 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 7 Enable	1	Channel 1 Tap 7 Enable

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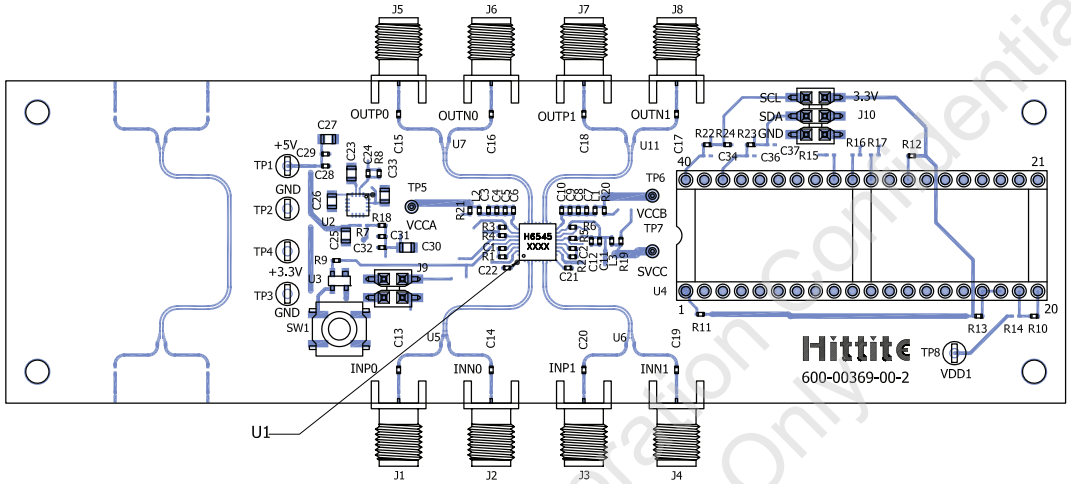
Reg 0x68	Channel 1 Tap 8 Settings B Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Tap 8 Gain	0x00	Channel 1 Tap 8 Gain
[6]	R/W	Tap 8 Gain Sign	1	Channel 1 Tap 8 Gain Sign. 1 means positive, 0 means negative.
[7]	R/W	Tap 8 Enable	1	Channel 1 Tap 8 Enable
Reg 0x69	Channel 1 Pre Driver Settings B Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[5:0]	R/W	Pre Driver Gain	0x30	Channel 1 Pre Driver Gain
[7:6]	R/W	Factory Set	0b00	Not Used
Reg 6Ah	Channel 1 Offset Settings B Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[4:0]	R/W	Manual Offset Gain	0x00	Channel 1 Manual Offset Gain
[5]	R/W	Manual Offset Sign	0	Channel 1 Manual Offset Sign
[6]	R/W	Automatic Offset Enable	1	Channel 1 Automatic Offset Enable.
[7]	R/W	Factory Set	0	Not Used
Reg 6Bh	Channel 1 Internal AGC Amplitude B Register			
BIT	TYPE	NAME	DEFLT	DESCRIPTION
[2:0]	R/W	Internal AGC Amplitude	0b100	Internal AGC Amplitude
[7:3]	R/W	Factory Set	0x00	Not Used

32 Gbps Dual Channel Advanced Linear Equalizer

Evaluation PCB



Evaluation Order Information

Item	Contents	Part Number
Evaluation Kit - 1	HMC6545LP5E Evaluation PCB, 6' USB 2.0 A Male/B Male Cable, User Software CD-ROM (Contains User Software, Evaluation PCB Schematic and User Manual)	EKIT01-HMC6545LP5