

TPS22917x 1 V–5.5-V, 2-A, 80-mΩ Ultra-Low Leakage Load Switch

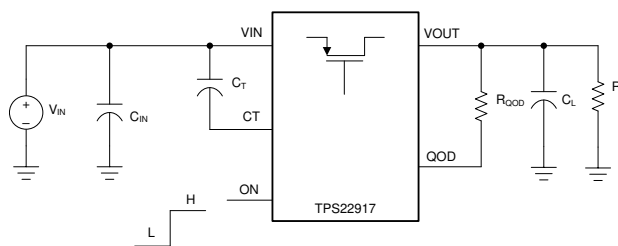
1 Features

3 Description

2 Applications

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)



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Simplified Schematic

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4 Revision History

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Changes from Revision * (September 2017) to Revision A (February 2018)	Page
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5 Device Comparison Table

Device	ON Pin Logic

6 Pin Configuration and Functions

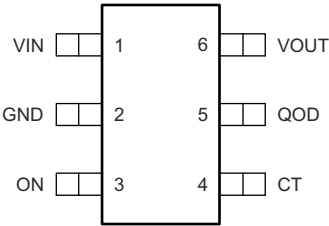


Figure 6-1. DBV Package 6-Pin SOT-23 Top View

Table 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
			Fall Time (t_{FALL}) and Quick Output Discharge (QOD)

7 Specifications

7.1 Absolute Maximum Ratings

	MIN	MAX	UNIT

Absolute Maximum Ratings

Recommended Operating Conditions

7.2 ESD Ratings

	VALUE	UNIT

7.3 Recommended Operating Conditions

	MIN	MAX	UNIT

7.4 Thermal Information

Thermal Parameters	TPS22917	UNIT
	DBV (SOT-23)	
	6 PINS	

7.5 Electrical Characteristics

PARAMETER		TEST CONDITIONS		T _J	MIN	TYP	MAX	UNIT				
INPUT SUPPLY(V _{IN})												
ON-RESISTANCE(R _{ON})												
			ENABLE PIN(ON)									
REVERSE CURRENT BLOCKING(R _{CB})												
QUICK OUTPUT DISCHARGE(Q _{OD})												

7.7 Typical Characteristics

7.7.1 Typical Electrical Characteristics

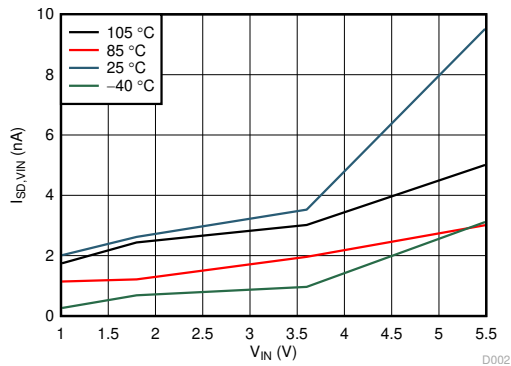
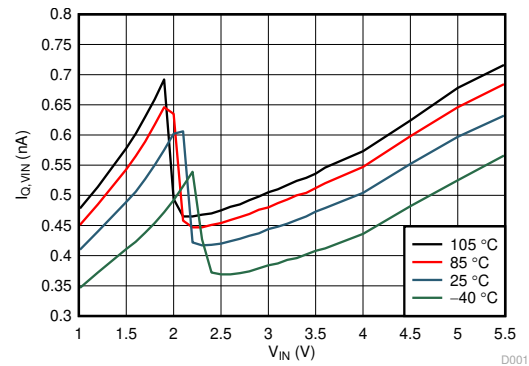
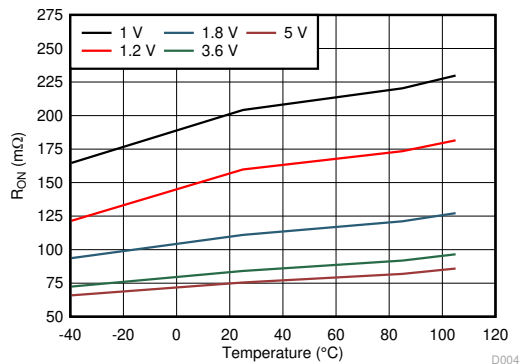
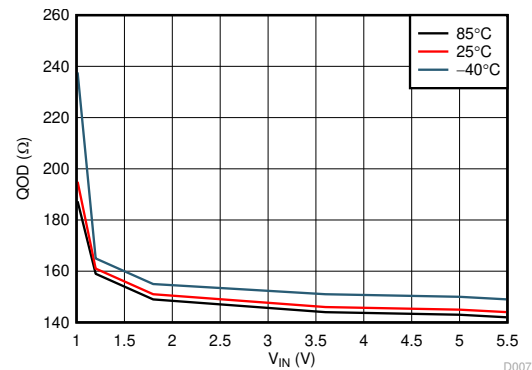
Figure 7-1. Shutdown Current (I_{SD})Figure 7-2. Quiescent Current (I_Q)Figure 7-3. ON-Resistance (R_{ON})

Figure 7-4. Quick Output Discharge (QOD)

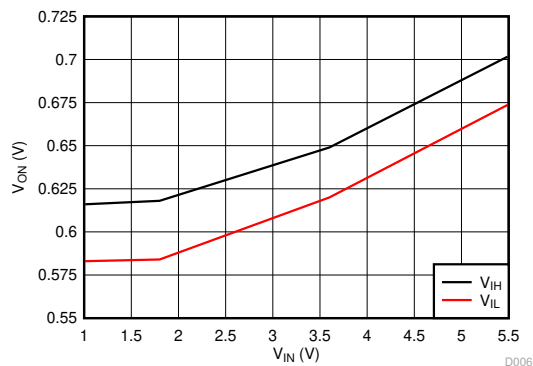
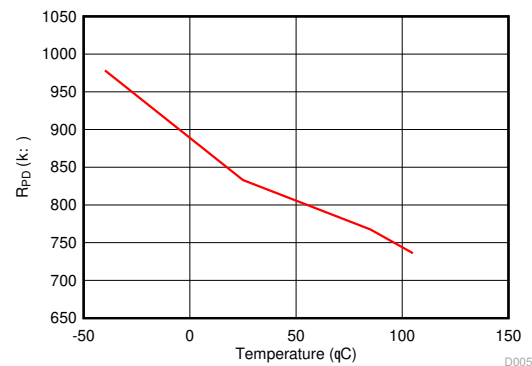


Figure 7-5. ON Pin Threshold

Figure 7-6. ON Pin Smart Pulldown (R_{PD})

7.7.2 Typical Switching Characteristics

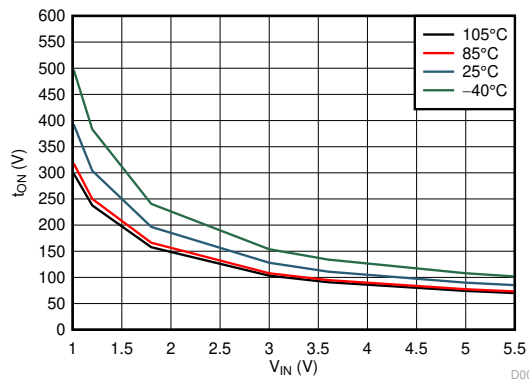


Figure 7-7. Turn-On Time (CT = Open)

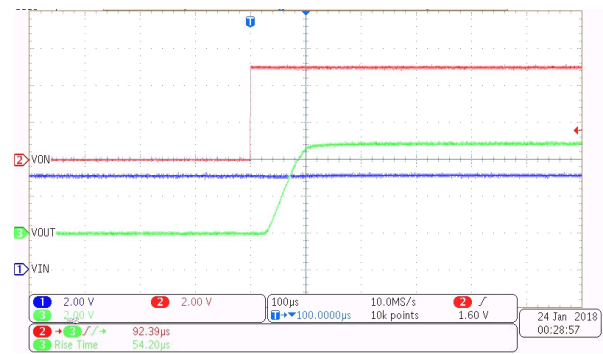


Figure 7-8. Turn-On at 5 V (CT = Open)

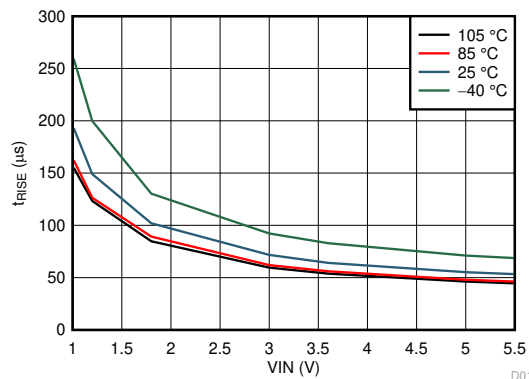


Figure 7-9. Rise Time (CT = Open)

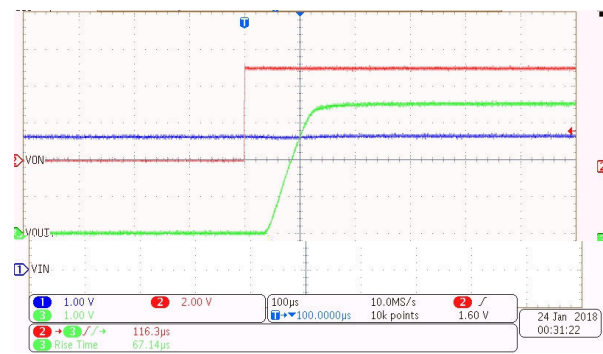


Figure 7-10. Turn-On at 3.6 V (CT = Open)

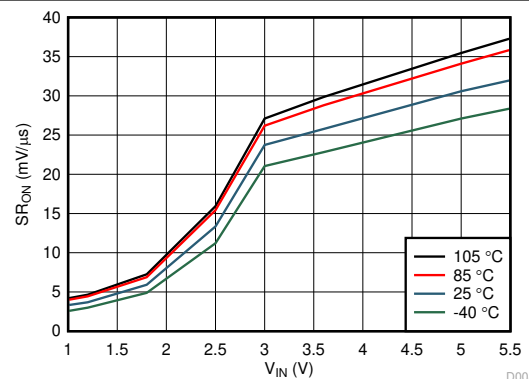


Figure 7-11. Slew Rate (CT = Open)

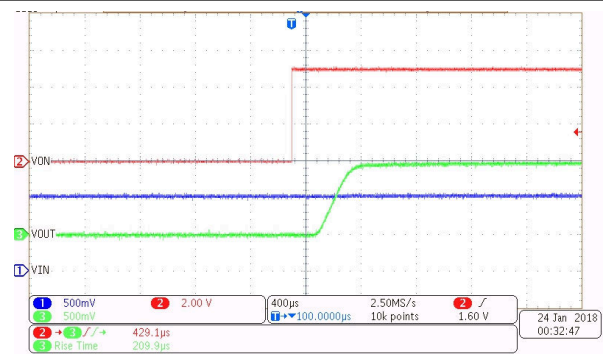
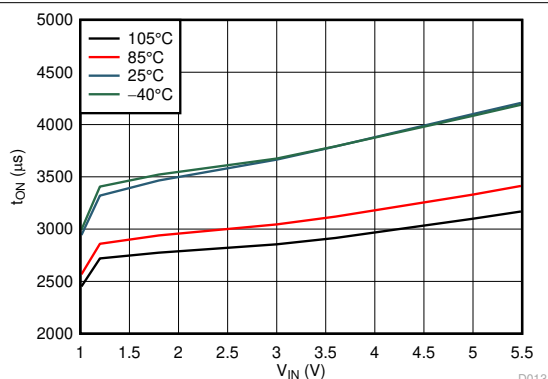
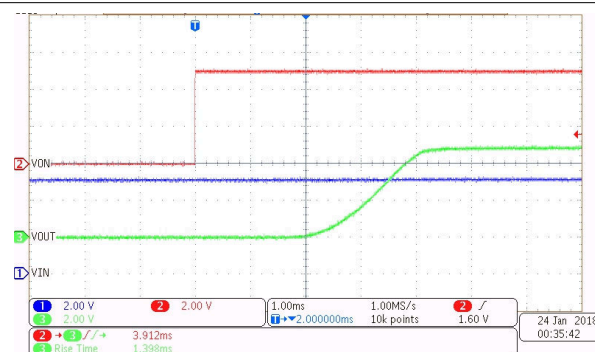
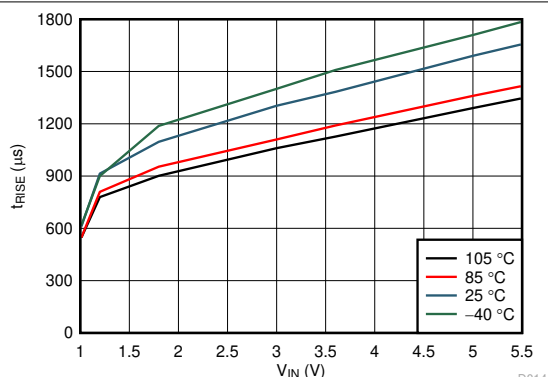
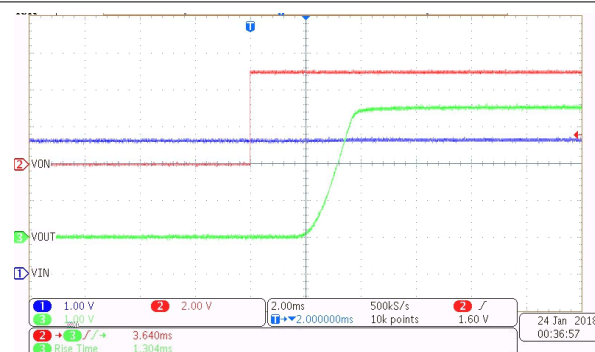
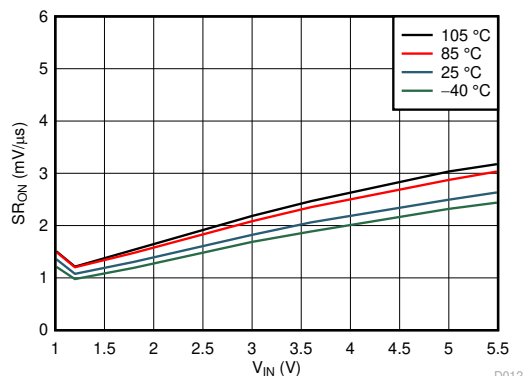
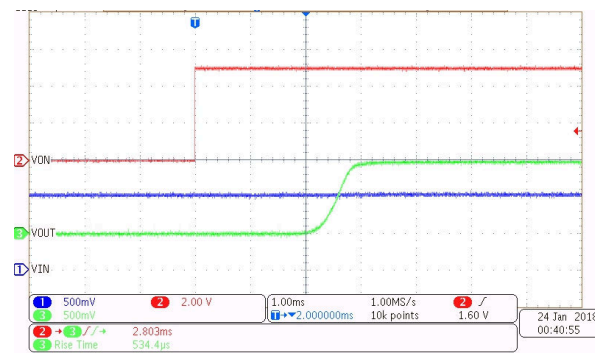


Figure 7-12. Turn On at 1 V (CT = Open)

7.7.2 Typical Switching Characteristics (continued)

Figure 7-13. Turn On Time ($C_T = 1000$ pF)Figure 7-14. Turn-On at 5 V ($C_T = 1000$ pF)Figure 7-15. Rise Time ($C_T = 1000$ pF)Figure 7-16. Turn-On at 3.6 V ($C_T = 1000$ pF)Figure 7-17. Slow Slew Rate ($C_T = 1000$ pF)Figure 7-18. Turn-On at 1 V ($C_T = 1000$ pF)

7.7.2 Typical Switching Characteristics (continued)

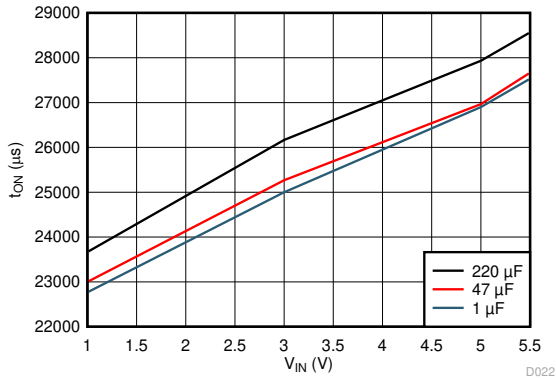


Figure 7-19. Turn-On vs Load Capacitance (CT = 10000 pF)

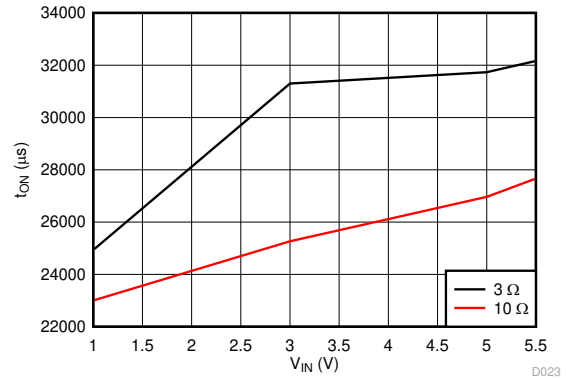


Figure 7-20. Turn-On vs Load Resistance (CT = 10000 pF)

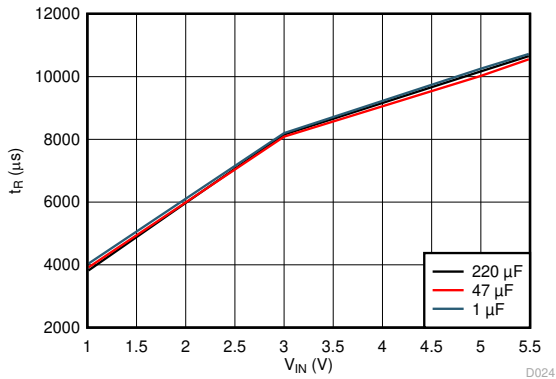


Figure 7-21. Rise Time vs Load Capacitance (CT = 10000 pF)

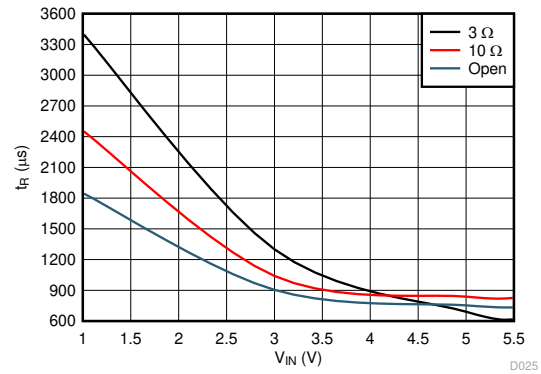


Figure 7-22. Rise Time vs Load Resistance (CT = 10000 pF)

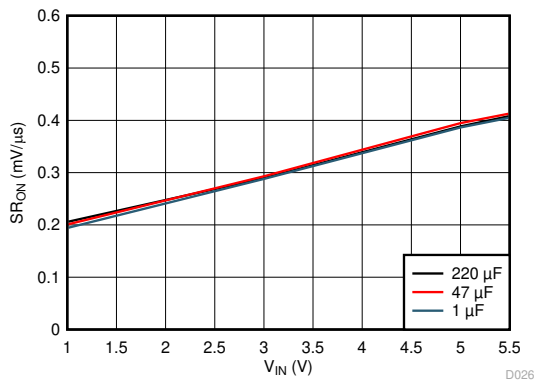


Figure 7-23. Slew Rate vs Load Capacitance (CT = 10000 pF)

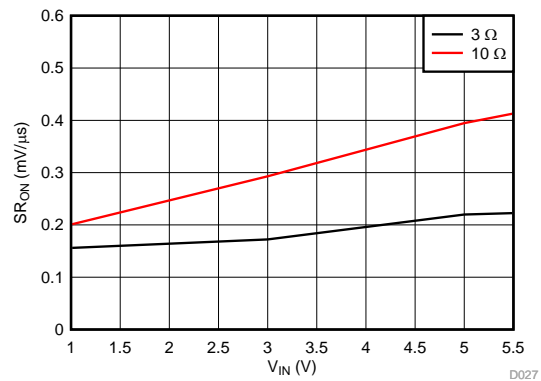
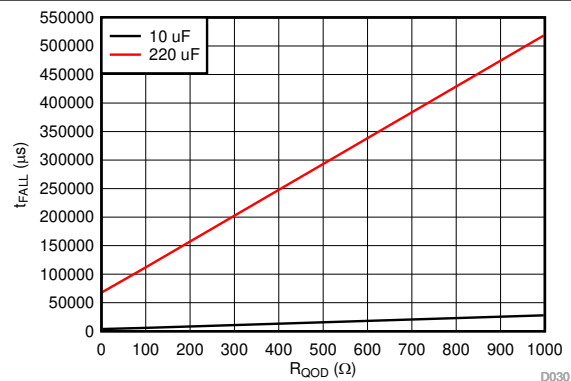
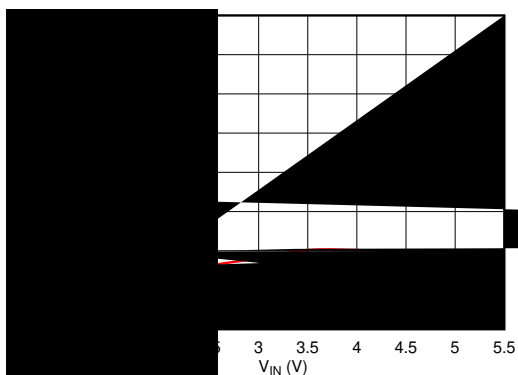
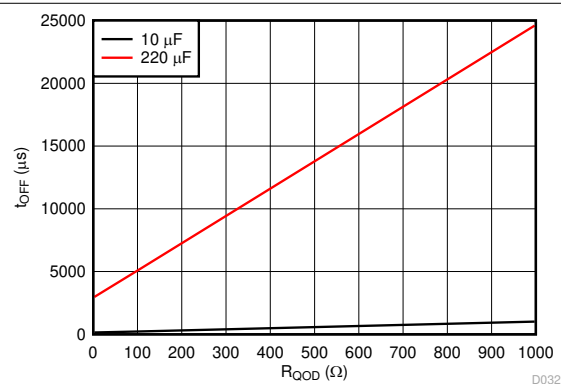
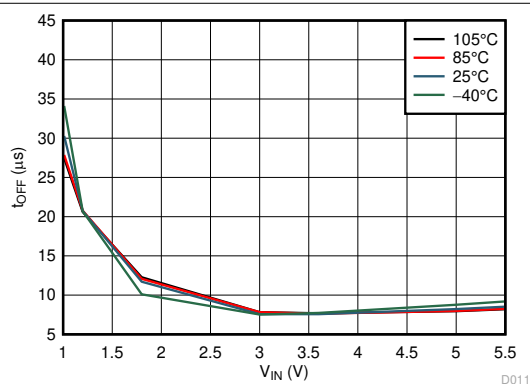
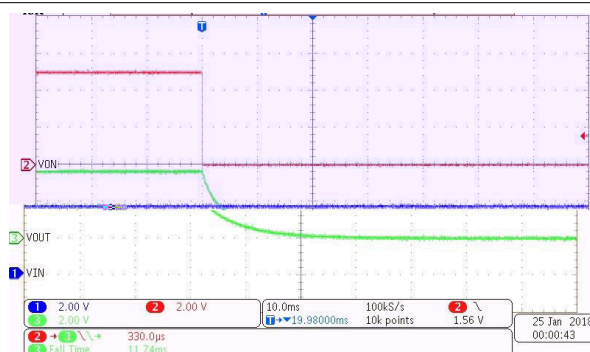
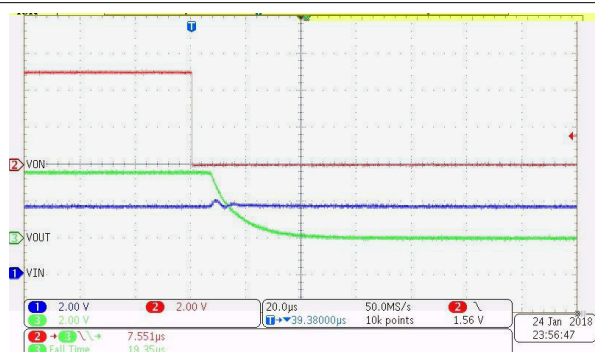


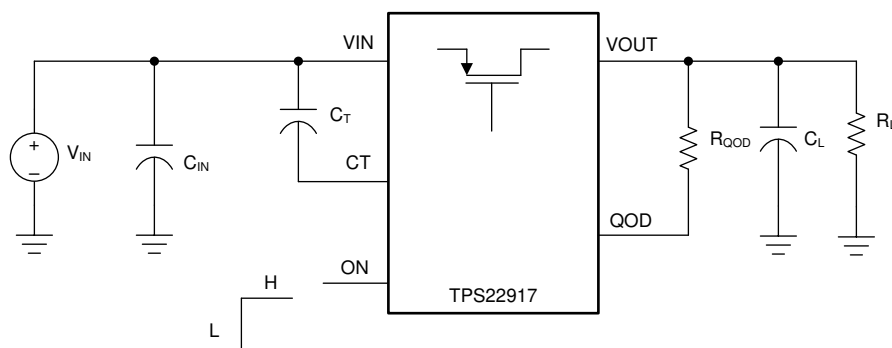
Figure 7-24. Slew Rate vs Load Resistance (CT = 10000 pF)

7.7.2 Typical Switching Characteristics (continued)



8 Parameter Measurement Information

8.1 Test Circuit and Timing Waveforms Diagrams



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Figure 8-1. Test Circuit

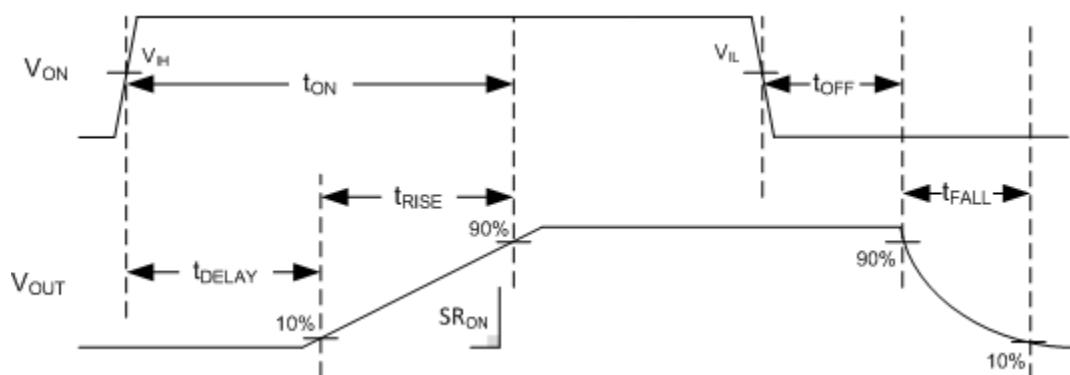
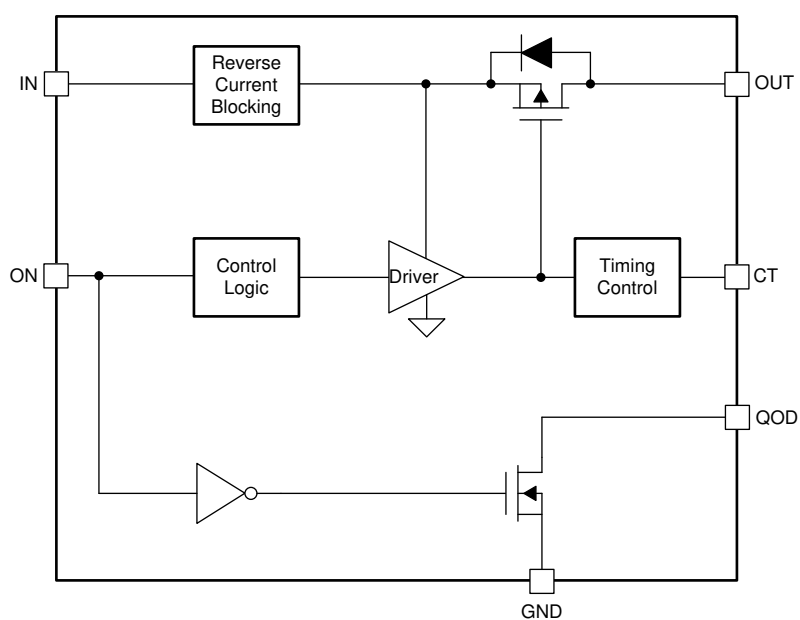


Figure 8-2. Timing Waveforms

9 Detailed Description

9.1 Overview

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 On and Off Control

Table 9-1. Smart-ON Pulldown

VON	Pulldown

9.3.2 Turn-On Time (t_{ON}) and Adjustable Slew Rate (CT)

Switching Characteristics

9.3.3 Fall Time (t_{FALL}) and Quick Output Discharge (QOD)

9.3.3.1 QOD When System Power is Removed

[Sequencing](#)

[Setting Fall Time for Shutdown Power](#)

9.4 Full-Time Reverse Current Blocking

9.5 Device Functional Modes

Table 9-2. VOUT Connection

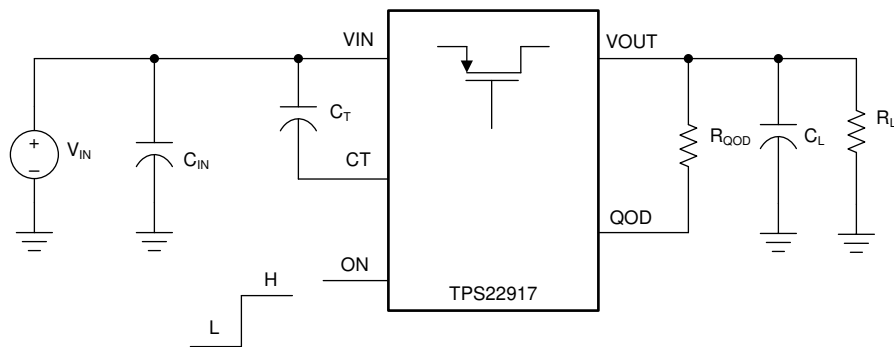
ON	QOD CONFIGURATION	TPS22917 VOUT	TPS22917L VOUT

10 Application and Implementation

Note

10.1 Application Information

10.2 Typical Application



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Figure 10-1. Typical Application Schematic

10.2.1 Design Requirements

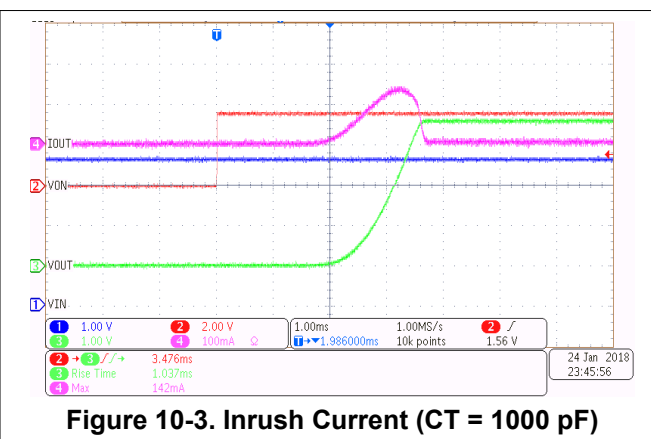
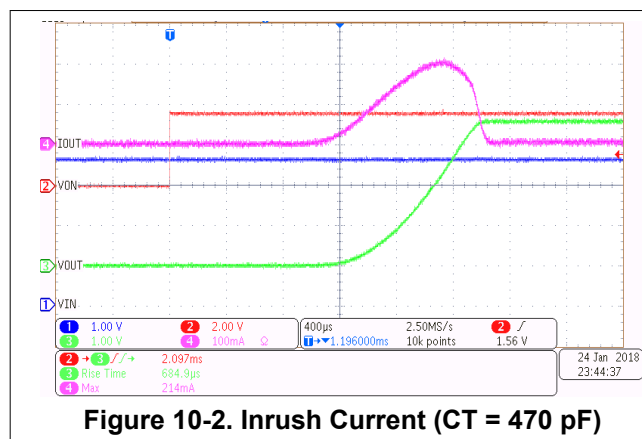
Table 10-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE

10.2.2 Detailed Design Procedure

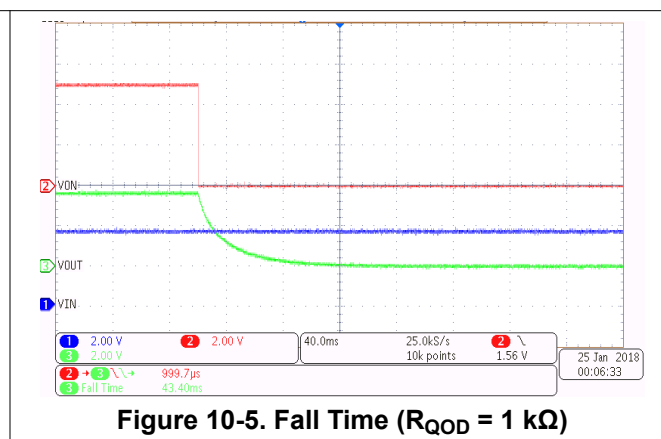
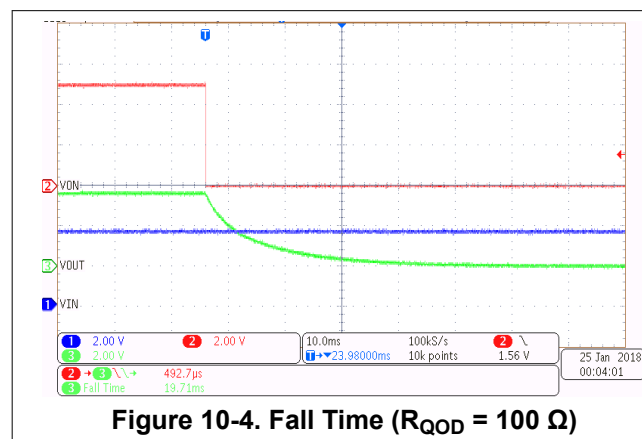
10.2.2.1 Limiting Inrush Current

10.2.2.2 Application Curves



10.2.2.3 Setting Fall Time for Shutdown Power Sequencing

10.2.2.4 Application Curves



11 Power Supply Recommendations

12 Layout

12.1 Layout Guidelines

12.2 Layout Example

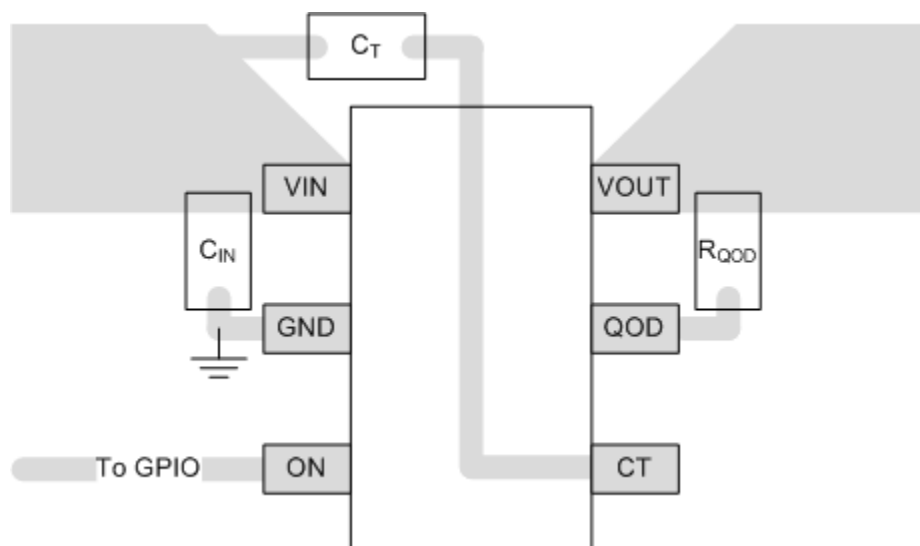


Figure 12-1. Recommended Board Layout

12.3 Thermal Considerations

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Thermal Information

13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

Subscribe to updates

13.2 Support Resources

13.3 Trademarks

13.4 Electrostatic Discharge Caution



13.5 Glossary

14 Mechanical, Packaging, and Orderable Information

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22917DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1IAF	Samples
TPS22917DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	1IAF	Samples
TPS22917LDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-45 to 125	2K7F	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

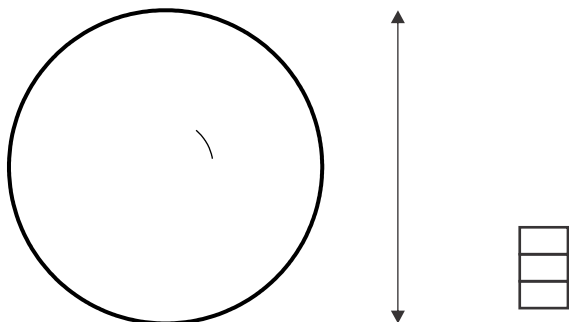
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

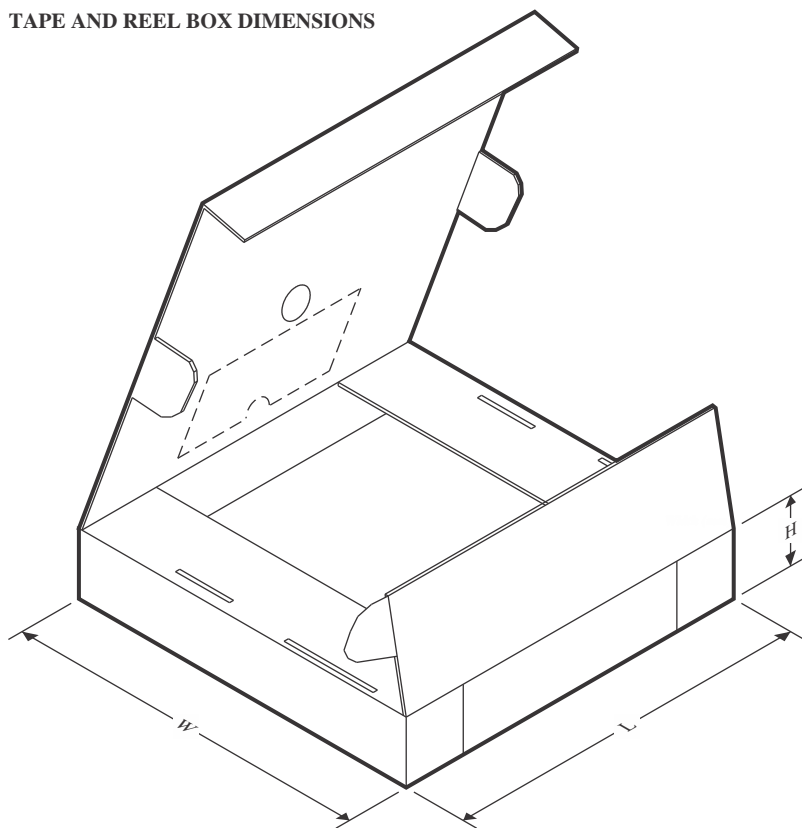
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TAPE AND REEL INFORMATION



TAPE AND REEL BOX DIMENSIONS

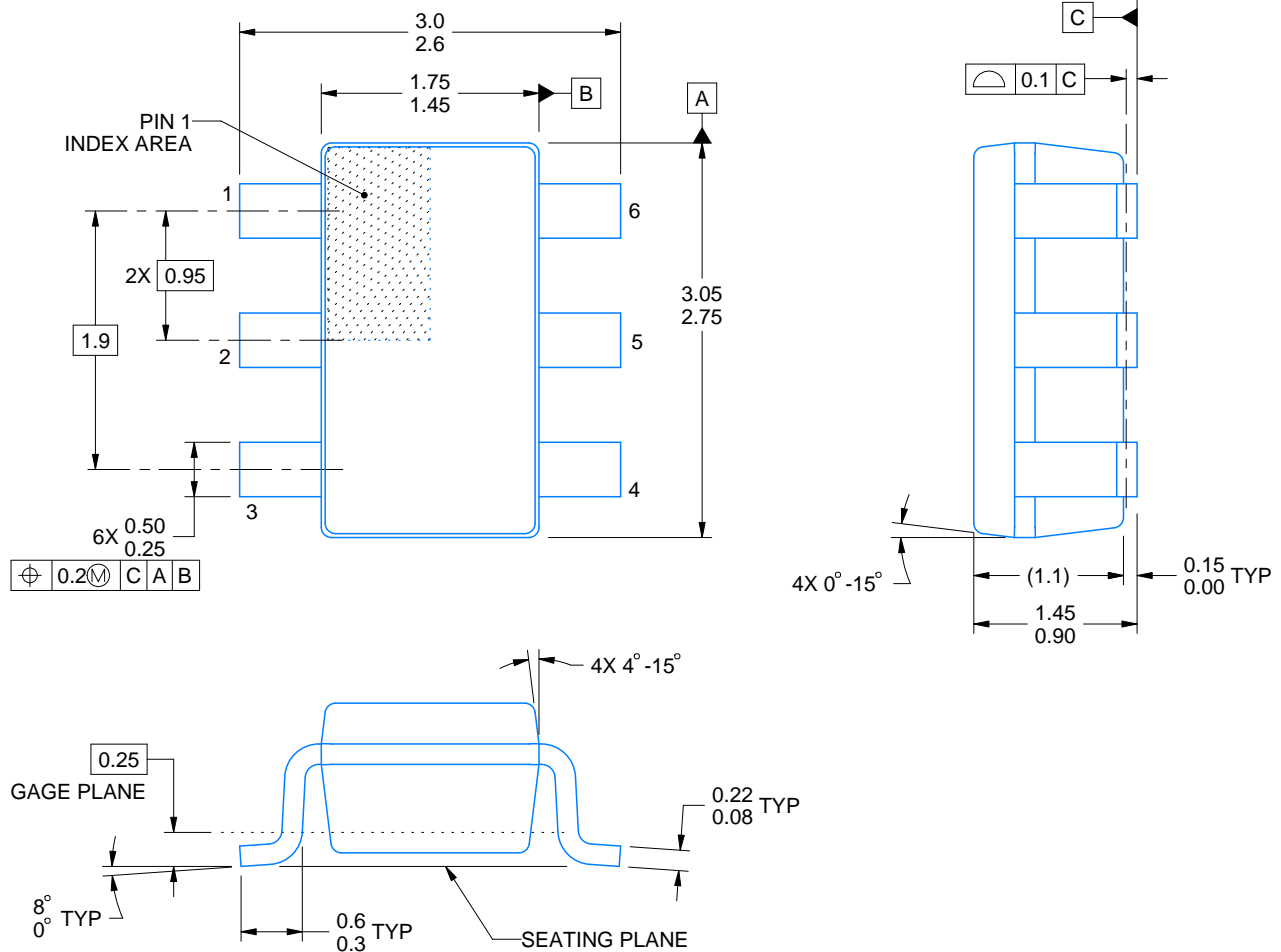


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22917DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS22917DBVT	SOT-23	DBV	6	250	210.0	185.0	35.0
TPS22917LDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS22917LDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0

DBV0006A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



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NOTES:

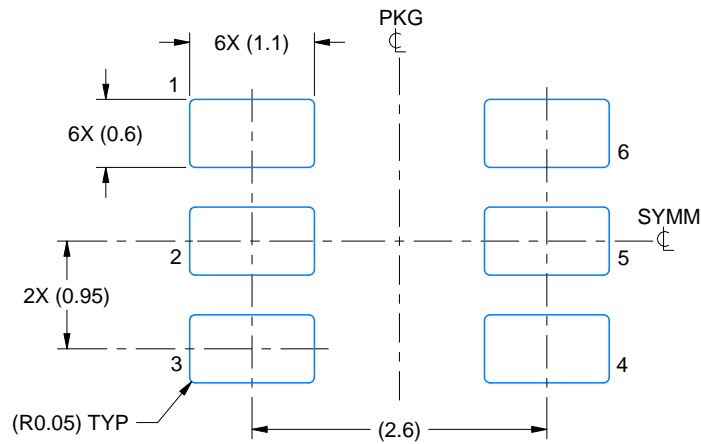
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

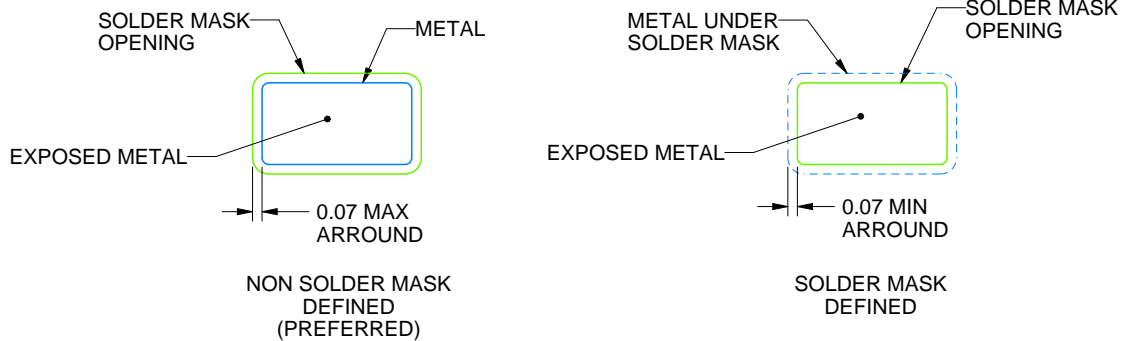
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

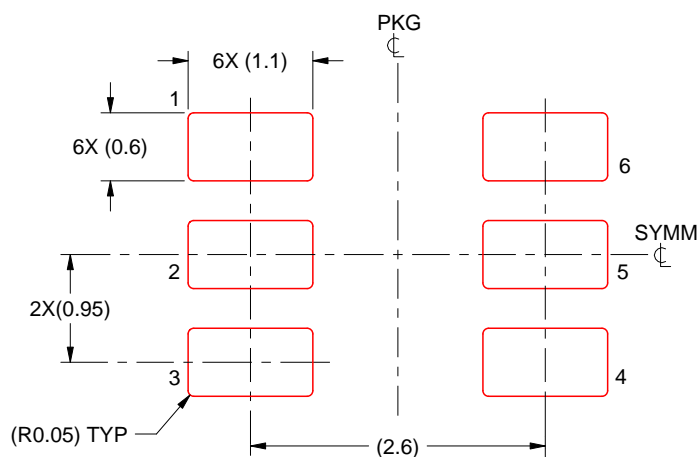
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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