DiiA Specification

DALI Part 252 – Energy Reporting

(Device Type 51)

Version 1.1

October 2019

For any further explanation of the contents of this document, or in case of any perceived inconsistency or ambiguity of interpretation, please contact the DiiA:

E-mail: TM@digitalilluminationinterface.org

Website: www.dali2.org

Document History

Publication Date	Status	Comments
August 2018		First publication.
October 2019	V1.1	Range of validity, TMASK and MASK clarified in memory bank locations. Clarifications and formatting updates, including: MASK for energy and power measurements, and ScaleFactor.

Table of contents

DALI Part 252 – Energy Reporting

1 Scope

This standard specifies the information related to energy reporting accessible through memory banks in control gear. This standard builds on the Digital Addressable Lighting Interface as specified in the IEC62386 series of standards, by adding specific requirements to address data exchange.

2 References

2.1 Normative references

The following normative documents are adopted, in whole or in part as indicated, in this Standards Publication. The latest edition of the publication applies (including amendments).

IEC 62386-102:2014, Digital addressable lighting interface – Part 102: General requirements – control gear

IEC 62386-102:2014/AMD1:2018, Digital addressable lighting interface – Part 102: General requirements – control gear

2.2 Informative references

This standard is intended to be used in conjunction with the following publications. The latest edition of the publication applies (including amendments).

None

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 62386-102:2014 and IEC 62386-102:2014/AMD1:2018, Clause 3 and the following apply.

3.1 Active Power

under periodic conditions, mean value, taken over one period, of the instantaneous power, measured in watt. (http://www.electropedia.org/)

3.2 Active Energy

the integral of the instantaneous power over a time interval, measured in units of watt hour. (http://www.electropedia.org/)

3.3 Apparent Power

the product of the rms voltage between the terminals of a two-terminal element or two-terminal circuit and the rms electric current in the element or circuit. (http://www.electropedia.org/)

3.4 Apparent Energy

the integral of Apparent Power over a time interval, measured in units of VA hour. (http://www.electropedia.org/)

3.5 Load side Power

the input power minus the sum of power used for the DALI bus power supply (if present) and the power used for the AUX power supply (if present).

Note: the losses for both power supplies (if present) may be neglected in the measurement

3.6 Load side Energy

the integral of Load side Power over a time interval, measured in units of watt hour.

3.7 NVM-RO

Non-Volatile Memory Read-Only (cannot be changed through DALI)

3.8 NVM-RW

Non-Volatile Memory Read-Write

3.9 ROM

Read Only Memory (cannot be changed by the control gear)

3.10 RAM-RO

Random Access Memory Read-Only (cannot be changed through DALI)

3.11 RAM-RW

Random Access Memory Read-Write

4 General

4.1 General

The requirements of IEC 62386-102:2014 and IEC 62386-102:2014/AMD1:2018, Clause 4 apply, with the restrictions, changes and additions identified below.

4.2 Version number

In 4.2 of IEC 62386-102:2014 and IEC 62386-102:2014/AMD1:2018, “102” shall be replaced by “252”, “version number” shall be replaced by “extended version number” and “*versionNumber*” shall be replaced by “*extendedVersionNumber*”.

5 Electrical specification

The requirements of IEC 62386-102:2014 and IEC 62386-102:2014/AMD1:2018, Clause 5 apply.

6 Interface power supply

The requirements of IEC 62386-102:2014 and IEC 62386-102:2014/AMD1:2018, Clause 6 apply.

7 Transmission protocol structure

The requirements of IEC 62386-102:2014 and IEC 62386-102:2014/AMD1:2018, Clause 7 apply.

8 Timing

The requirements of IEC 62386-102:2014 and IEC 62386-102:2014/AMD1:2018, Clause 8 apply.

9 Method of operation

9.1 General

The requirements of IEC 62386-102:2014 and IEC 62386-102:2014/AMD1:2018, Clause 9 apply with the following additions.

9.2 Memory banks

The requirements of Clause 9.10 of IEC62386-102:2014 and IEC 62386-102:2014/AMD1:2018 apply with the following additions and changes.

This standard adds Read-Only and Read-Write attributes to locations in a memory bank as per the following table.

Table 1 – Memory bank Read-Only and Read-Write attributes

Memory Type	**Accessibility via DALI bus** **RO: Read-Only** **RW: Read-Write**	**V: volatile (reset at power down)** **NV: non-volatile**	**May be changed autonomously by the control gear during run time**	**Description**
ROM	RO	NV	No	ROM as defined in IEC62386-102:2014. For all fixed value that will not change during run time of control gear. Note: ROM is RO by its nature. A ROM value may change if control gear is programmed during production.
RAM-RO	RO	V	Yes	For all measured values and flags that will be reset at power down.
RAM-RW	RW	V	Yes	For all input values that will be reset at power down.
NVM-RO	RO	NV	Yes	NVM as defined in IEC62386-102:2014 but with additional specification RO

				For all counter values. No reset at power down.
NVM-RW	RW	NV	Yes	NVM as defined in IEC62386-102:2014 For all input values that are non-volatile.

9.2.1 Memory bank reading

Requirements of Clause 9.11.4 “Memory bank reading” in IEC62386-102:2014 and IEC 62386-102:2014/AMD1:2018 apply with the following additions and changes.

A selected memory bank location can be read by means of command “READ MEMORY LOCATION (DTR1, DTR0)”. The answer shall be the value of the byte at the addressed memory bank location.

If the selected memory bank is not implemented, the command shall be ignored. If the memory bank exists, and selected memory bank location is not implemented, the answer shall be MASK.

Table 2 – MASK values for various data types

Data type:	MASK value
1 Byte (unsigned char)	0xFF
2 Bytes (unsigned int):	0xFFFF
3 Bytes (unsigned int24):	0xFFFFFF
4 Bytes (unsigned long):	0xFFFFFFFF
6 Bytes (unsigned int48)	0xFFFFFFFFFFFF
1 Bytes (signed char):	0x7F
2 Bytes (signed int):	0x7FFF
4 Bytes (signed long):	0x7FFFFFFF

9.2.2 Latching of a multi-byte value for reading

To ensure consistent data when reading a multi-byte value from a memory bank, it is required that a mechanism be implemented that latches all bytes of the multi-byte value when the first byte of the multi-byte value is read and holds them latched until the first byte of any multi-byte or single byte value is read.

9.2.3 Latching of a full memory bank for reading

This standard specifies an additional method that enables latching of a full memory bank. The lock byte is used to control the memory bank latch as follows:

If the lock byte contains a value other than 0xAA, writing the following values to the lock byte shall cause the stated result:

- 0xAA: All locations in the memory bank shall be latched and shall not change until the lock byte is written, or a power cycle occurs.
- Other values: The memory bank latch is not affected.

If the lock byte contains the value 0xAA, writing the following values to the lock byte shall cause the stated result:

- 0xAA: All locations in the memory bank shall be re-latched (updated) and shall not change again until the lock byte is written, or a power cycle occurs.
- Other values: The memory bank latch shall be removed. Memory reads shall result in the latest values being returned.

An attempt to write to any location other than the lock byte of a latched memory bank shall result in the same behaviour as if the memory location is not implemented.

Latching of a full memory bank shall not affect reading or writing of other memory banks.

NOTE: If controller A latches a full memory bank 202, controller B needs to be aware that memory bank 202 is latched. When controller B reads from memory bank 202, B will get the latched data. Controller B can find out as B received the command to write the lock byte with 202 or B could read the lock byte to be on the safe side.

9.2.4 Memory bank values that are temporarily not available

In special situations certain memory bank value may not be available temporarily. Read access results in a reserved TMASK value defined for various data types in the table below. Except in fault conditions, the control gear shall provide a valid value within 30 seconds. If TMASK is returned repeatedly over a period of time, the controller may deduce there is a fault in the control gear.

Table 3 – TMASK values for various data types

Data type:	TMASK value
1 Byte (unsigned char)	0xFE
2 Bytes (unsigned int):	0xFFFE
3 Bytes (unsigned int24):	0xFFFFFE
4 Bytes (unsigned long):	0xFFFFFFFE
6 Bytes (unsigned int48)	0xFFFFFFFFFFFE
1 Bytes (signed char):	0x7E
2 Bytes (signed int):	0x7FFE
4 Bytes (signed long):	0x7FFFFFFE

NOTE Example: after an external supply power cycle, a memory bank value may not be available temporarily due to the settling time of digital filters. In this case TMASK should be indicated.

9.2.5 Accuracy of measurements

The accuracy of measurements for the values in the memory banks is determined by the manufacturer and is not specified in this standard.

9.2.6 Rounding of measurement values

Rounding of measurement values shall be performed as follows: Rounding to the nearest integer and a value of 0.5 is rounded up.

9.2.7 Refresh rate of memory bank values

The minimum refresh rate of all memory bank values shall be 1 refresh cycle in 30 s. The minimum refresh rate shall be valid if the driver is powered regardless of the status of lampOn.

9.2.8 No overflow of counters

Counters shall not overflow. Their maximum value shall be MASK -2.

9.2.9 Memory bank 202, active energy and power (Mandatory)

Address	Description	Default value (factory)	RESET value[a]	Memory type
0x00	Address of last addressable memory location	0x0F	No change	ROM
0x01	Indicator byte	Manufacturer specific	Manufacturer specific	Manufacturer specific
0x02	Lock byte Lockable bytes in the memory bank shall be read-only while the lock byte has a value different from 0x55.	0xFF	0xFF[b]	RAM-RW
0x03	Version of the memory bank	0x01	No change	ROM
0x04	ScaleFactorForActiveEnergy, scale factor for measured Active Energy values in this memory bank, expressed as power of 10 (scale factor = $10^{ScaleFactorForActiveEnergy} * 1$ Wh); example: -3 denotes milli, +3 denotes kilo Range of validity: [0, 6],[0xFA,0xFF]	Control gear dependent[c]	No change	ROM
0x05	ActiveEnergy (MSB)	0x00	No change	NVM-RO
0x06	ActiveEnergy	0x00	No change	NVM-RO
0x07	ActiveEnergy	0x00	No change	NVM-RO
0x08	ActiveEnergy	0x00	No change	NVM-RO
0x09	ActiveEnergy	0x00	No change	NVM-RO
0x0A	ActiveEnergy (LSB); scale factor is defined by ScaleFactorForActiveEnergy (0x04) Range of validity: [0, 0xFF FF FF FF FF FD] ,TMASK	0x00	No change	NVM-RO
0x0B	ScaleFactorForActivePower, scale factor for measured Active Power values in this memory bank, expressed as power of 10 (scale factor = $10^{ScaleFactorForActovePower} * 1$ W); example: -3 denotes milli, +3 denotes kilo Range of validity: [0, 6],[0xFA,0xFF]	Control gear dependent[c]	No change	ROM
0x0C	ActivePower (MSB)	[d]	No change	RAM-RO
0x0D	ActivePower	[d]	No change	RAM-RO
0x0E	ActivePower	[d]	No change	RAM-RO
0x0F	ActivePower (LSB); scale factor is defined by ScaleFactorForActivePower (0x0B) Range of validity: [0, 0xFF FF FF FD], TMASK	[d]	No change	RAM-RO

[a] Reset value after “RESET MEMORY BANK”.

[b] Also used as power on value.

[c] The value shall be represented as two’s complement in the range of [-6..+6] such that -3 is represented by a stored value of 0xFD.

[d] The value should reflect the actual situation as soon as possible.

9.2.10 Memory bank 203, apparent energy and power (Optional)

Address	Description	Default value (factory)	RESET value[a]	Memory type
0x00	Address of last addressable memory location	0x0F	No change	ROM
0x01	Indicator byte	Manufacturer specific	Manufacturer specific	Manufacturer specific
0x02	Lock byte Lockable bytes in the memory bank shall be read-only while the lock byte has a value different from 0x55.	0xFF	0xFF[b]	RAM-RW
0x03	Version of the memory bank	0x01	No change	ROM
0x04	ScaleFactorForApparentEnergy, scale factor for measured Apparent Energy values in this memory bank, expressed as power of 10 (scale factor = $10^{ScaleFactorForApparentEnergy} * 1$ VAh); example: -3 denotes milli, +3 denotes kilo Range of validity: [0, 6],[0xFA,0xFF]	Control gear dependent[c]	No change	ROM
0x05	ApparentEnergy (MSB)	0x00	No change	NVM-RO
0x06	ApparentEnergy	0x00	No change	NVM-RO
0x07	ApparentEnergy	0x00	No change	NVM-RO
0x08	ApparentEnergy	0x00	No change	NVM-RO
0x09	ApparentEnergy	0x00	No change	NVM-RO
0x0A	ApparentEnergy (LSB); scale factor is defined by ScaleFactorForApparentEnergy (0x04) Range of validity: [0, 0xFF FF FF FF FF FD], TMASK	0x00	No change	NVM-RO
0x0B	ScaleFactorForApparentPower, scale factor for measured Apparent Power values in this memory bank, expressed as power of 10 (scale factor = $10^{ScaleFactortForApparentPower} * 1$ VA); example: -3 denotes milli, +3 denotes kilo Range of validity: [0, 6],[0xFA,0xFF]	Control gear dependent[c]	No change	ROM
0x0C	ApparentPower (MSB)	[d]	No change	RAM-RO
0x0D	ApparentPower	[d]	No change	RAM-RO
0x0E	ApparentPower	[d]	No change	RAM-RO
0x0F	ApparentPower (LSB); scale factor is defined by ScaleFactorForApparentPower (0x0B) Range of validity: [0, 0xFF FF FF FD], TMASK	[d]	No change	RAM-RO

[a] Reset value after “RESET MEMORY BANK”.

[b] Also used as power on value.

[c] The value shall be represented as two’s complement in the range of [-6..+6] such that -3 is represented by a stored value of 0xFD.

[d] The value should reflect the actual situation as soon as possible.

9.2.11 Memory bank 204, load side energy and power (Optional)

Address	Description	Default value (factory)	RESET value[a]	Memory type
0x00	Address of last addressable memory location	0x0F	No change	ROM
0x01	Indicator byte	Manufacturer specific	Manufacturer specific	Manufacturer specific
0x02	Lock byte Lockable bytes in the memory bank shall be read-only while the lock byte has a value different from 0x55.	0xFF	0xFF[b]	RAM-RW
0x03	Version of the memory bank	0x01	No change	ROM
0x04	ScaleFactorForLoadsideEnergy, scale factor for measured Active Energy Loadside values in this memory bank, expressed as power of 10 (scale factor = $10^{ScaleFactorForLoadsideEnergy} * 1$ Wh); example: -3 denotes milli and +3 denotes kilo Range of validity: [0, 6],[0xFA,0xFF]	Control gear dependent[c]	No change	ROM
0x05	ActiveEnergyLoadside (MSB)	0x00	No change	NVM-RO
0x06	ActiveEnergyLoadside	0x00	No change	NVM-RO
0x07	ActiveEnergyLoadside	0x00	No change	NVM-RO
0x08	ActiveEnergyLoadside	0x00	No change	NVM-RO
0x09	ActiveEnergyLoadside	0x00	No change	NVM-RO
0x0A	ActiveEnergyLoadside (LSB); scale factor is defined by ScaleFactorForLoadsideEnergy (0x04) Range of validity: [0, 0xFF FF FF FF FF FD], TMASK	0x00	No change	NVM-RO
0x0B	ScaleFactorForLoadsidePower, scale factor for measured Active Power Loadside values in this memory bank, expressed as power of 10 (scale factor = $10^{ScaleFactorForLoadsidePower} * 1$ W); example: -3 denotes milli and +3 denotes kilo Range of validity: [0, 6],[0xFA,0xFF]	Control gear dependent[c]	No change	ROM
0x0C	ActivePowerLoadside (MSB)	[d]	No change	RAM-RO
0x0D	ActivePowerLoadside	[d]	No change	RAM-RO
0x0E	ActivePowerLoadside	[d]	No change	RAM-RO
0x0F	ActivePowerLoadside (LSB); scale factor is defined by ScaleFactorForLoadsidePower (0x0B) Range of validity: [0, 0xFF FF FF FD], TMASK	[d]	No change	RAM-RO

[a] Reset value after "RESET MEMORY BANK".

[b] Also used as power on value.

[c] The value shall be represented as two's complement in the range of [-6..+6] such that -3 is represented by a stored value of 0xFD.

[d] The value should reflect the actual situation as soon as possible.

10 Declaration of variables

The requirements of IEC 62386-102:2014 and IEC 62386-102:2014/AMD1:2018, Clause 10 apply, with the following additional variables for this device type, as indicated in following Table.

Table 3 – Declaration of variables

VARIABLE	DEFAULT VALUE (factory)	RESET VALUE	POWER ON VALUE	RANGE OF VALIDITY	MEMORY TYPE
"extendedversionNumber"	2.0	no change	no change	00001000b	ROM

VARIABLE	DEFAULT VALUE (factory)	RESET VALUE	POWER ON VALUE	RANGE OF VALIDITY	MEMORY TYPE
"deviceType"	51	no change	no change	51	ROM

11 Definition of commands

11.1 General

The requirements of IEC 62386-102:2014 and IEC 62386-102:2014/AMD1:2018, Clause 11, apply with the following additions.

11.2 Overview sheets

Following Table gives an overview of the application extended commands for this device type. Unused opcodes of application extended commands shall be reserved for future needs.

Table 4 – Standard commands

Command name	Address byte		Opcode byte	Ed. 1 cmd number	DTR0	DTR1	DTR2	Answer	Send twice	References	Command reference
	See Error! Reference source not found.	Selector bit									
QUERY EXTENDED VERSION NUMBER	*Device*	*1*	*0xFF*	-				✓			11.3.2
ENABLE DEVICE TYPE	*0xC1*		*0x33*								11.4.2

11.3 Application extended commands

11.3.1 General

Application extended commands as defined in this document shall be preceded by “ENABLE DEVICE TYPE (data)” where data equals *“deviceType”*. For device types other than *“deviceType”* these commands may be used in a different way.

11.3.2 QUERY EXTENDED VERSION NUMBER

The answer shall be “*extendedVersionNumber”*.

11.4 Special commands

11.4.1 General

The requirements of IEC 62386-102:2014 and IEC 62386-102:2014/AMD1:2018, Clause 11.7 apply with the following additions.

11.4.2 ENABLE DEVICE TYPE (data)

To enable the command set as defined in this document, *“data”* shall be *“deviceType”*.