Introduction

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The Universal Asynchronous Receiver Transmitter (UART) module with built-in protocol support is a serial communications peripheral that allows users to interface other UART compatible devices. The UART module is designed for full-duplex communication, and supports the following protocols:

- LIN Master and Slave modes
- DMX mode
- DALI Control Gear and Control Device modes

This technical brief highlights the use of this UART module in Basic mode stand-alone, without the use of the other UART protocol support.

Источник <https://onlinedocs.microchip.com/oxy/GUID-167CA20A-2C0F-4CBC-A693-9FD032B9B193-en-US-1/GUID-1D035BDE-0DA9-4CF4-BD8B-CA1CC09120BF.html>

1.1 Transmit and Receive Buffers

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The UART module contains dedicated transmit and receive buffers. The Transmit Enable Control (**TXEN**) bit enables/disables the transmitter, while the Receive Enable Control (**RXEN**) bit enables/disables the receiver.

The **transmitter** consists of the **Transmit Shift Register (TSR)** and one **buffer register**, **UxTXB**. **Writes to UxTXB are transferred to the TSR when the TSR is empty**. Bytes written to UxTXB while the TSR is full will be held in UxTXB until the TSR has completed shifting out its data. The **Transmit Shift Register Empty Interrupt Flag (TXMTIF)** bit can be used to determine if the TSR is empty, while the **Transmit Buffer Empty Status (TXBE)** bit and the **UART Transmit Interrupt Flag (UxTXIF)** bit indicate if the UxTXB is empty. **Additionally, the Transmit Buffer Full Status (TXBF) bit can be used to indicate if the transmit buffer is full. If a new byte was written to UxTXB while the TXBF bit is set (TXBF = 1), the Transmit Write Error Status (TXWRE) bit becomes set and must be cleared in software to continue transmission**. The TXBE bit can also be set by software to clear both the transmit buffer and the transmit shift register.

The receiver consists of the **Receive Shift Register (RSR)** and a **two-level First-In First-Out (FIFO) buffer area.** The buffer at the top of the FIFO, UxRXB, holds the first received byte (earliest byte to enter the FIFO). When a byte is received, it is loaded into the RSR, and if the receive FIFO is empty, the byte is transferred to UxRXB. If a second byte is received while the first byte remains in UxRXB, the second byte is transferred to the bottom of the FIFO. If a third byte is received, it is stored in the RSR until UxRXB is read. If any further bytes are received while the FIFO and RSR are full, the Receive FIFO Overflow Interrupt Flag (RXFOIF) bit becomes set, indicating a receive overflow condition.

In the event of an overflow, the **Run During Overflow Control (RUNOVF) bit** can be used to determine whether the RSR continues to receive data (after the overflow condition is cleared) or stop receiving data (legacy mode). An overflow condition can be cleared by reading UxRXB and clearing the RXFOIF bit, setting the RXBE bit, which flushes the entire FIFO, or by clearing the ON bit, which clears both the transmit and receive buffers and shift registers. When RUNOVF is set, the module will continue to synchronize the RSR with the incoming Start bits after the overflow condition has been cleared. It is important to note that although the FIFO will continue to operate in an overflow condition, the data will not be valid until the overflow condition has been cleared.

Transmit and receive polarity is user selectable. Both transmit and receive lines default to a logic ‘high’ Idle state. The Transmit Polarity Control (TXPOL) bit controls the transmit line polarity, while the Receive Polarity Control (RXPOL) bit controls the receive line polarity.

1.2 Character Length

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Character length is controlled by the **MODE bits of UART Control Register 0 (UxCON0):**

- In Asynchronous 7-bit UART mode, only the seven Least Significant bits (LSbs) of the transmit/receive byte are used, while the Most Significant bit (MSb) is ignored.
- In Asynchronous 8-bit UART mode, all eight bits of the transmitted or received byte are used.
- In Asynchronous 8-bit UART mode with 9th bit odd/even Parity modes, each byte transmitted or received consists of nine bits.

In Parity modes, the first eight bits of each byte are the data bits, and the ninth bit is the parity bit. Parity bits are used in error detection. Even Parity means that the expected number of '1' bits in a character is an even number, while Odd Parity means that the expected number of '1' bits in a character is an odd number. When in Even Parity mode, the parity bit will be set if the number of '1' bits in the 8-bit transmit data is an odd number; when the number of '1' bits are even, the parity bit is cleared. In Odd Parity mode, when the number of '1' bits in the 8-bit transmit data is odd, the parity bit is cleared; when the number of bits are even, the parity bit is set. Table 1-1 gives examples of how the parity bit value is determined.

Table 1-1. Even/Odd Parity Examples

Byte Value	Even Parity Bit Value	Odd Parity Bit Value
1010 1010	0	1
1010 1000	1	0

In Asynchronous 9-bit UART Address mode, each byte transmitted or received consists of nine bits, and the 9th bit determines whether the byte is an address or data. When the 9th bit is set, the other eight bytes are used as an address; when the 9th bit is clear, the other eight bytes are used as data (see Address Mode for more details).

1.3 Address Mode

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The Asynchronous 9-bit UART Address mode allows the UART to communicate with multiple receivers sharing the same transmission line.

When transmitting in Address mode, the address of the receiver of interest is loaded into the UART Parameter 1 Low (UxP1L) re gister. When the address is loaded into UxP1L, hardware sets the 9th bit, indicating to the receiver that the byte is an address. Data bytes are written to the UxTXB register, similarly to normal UART operation. It is important to note that writes to UxP1L take precedence over writes to UxTXB. If both registers are written while the TSR is busy, the next byte loaded into TSR will come from UxP1L.

When receiving in Address mode, no received data will be transferred into the FIFO until a valid address is received. When a character with the 9th bit set is received, the eight LSb's are compared to the UART Parameter 2 Low (UxP2L) register. In receive Address mode, UxP2L holds the receiver address, while the UART Parameter 3 Low (UxP3L) register holds the address mask. If an address match occurs, the eight LSb's are transferred into the FIFO, while the 9th bit is transferred into the Parity Error Interrupt Flag (PERIF) bit. In this case, w hen PERIF is set, the UART Receive Interrupt Flag (UxRXIF) is suppressed, and if the Direct Memory Access (DMA) module is using the UxRXIF as a trigger, DMA transfers will be suspended. This prevents the DMA from writing add ress information into memory.

1.4 Flow Control

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Flow control allows the UART to suspend transactions in order to prevent input buffers from overflowing . **The UART supports both hardware and software flow control methods.** The **flow control** method is determined by the **Handshake Flow Control (FLO) bits** of the UxCON2 register.

1.4.1 Hardware Flow Control

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For hardware flow control, the UART module utilizes a **RTS/CTS flow control scheme commonly found in RS-232 (Recommended Standard 232) networks**. The RS-232 standard **defines the signals connecting Data Terminal Equipment (DTE) to Data Communication Equipment (DCE). In addition to the standard transmit (TX) and receive (RX) lines, RTS flow control** uses the **Request-to-Send (RTS) and Clear-to-Send (CTS)** lines. **The UART module also provides a third line, the Transmit Drive Enable (TXDE) line, to control an RS-485 transceiver.**

The UART module is configured as a DTE device; therefore, UART hardware configures the RTS signal as an output, while the CTS signal is an input. In a DCE system, the opposite is true; the RTS signal is an input, while the CTS signal is an output. It is important to note that connections between DTE and DTE devices (Figure 1-2) are different than connections between DTE and DCE devices (Figure 1-3).

The active-low RTS and CTS signals work together to control transmission flow. Hardware flow is typically controlled by the DTE device, which could be considered a 'master' device. In the case of a DTE-to-DTE configuration, either device can act as a master. When one DTE device wishes to transmit data, the DTE device pulls the RTS line low, which signals the slave device, through its CTS input, to begin to monitor its RX input. When the slave device is ready to accept the data, it pulls its RTS line low, informing the master, through its CTS line, to begin sending data. Once the transaction has completed, the master device pulls the RTS line high.

In a DTE-to-DCE configuration, the DTE is considered the master and the DCE is considered a slave. In this configuration, when the DTE device wishes to transmit data, the DTE device pulls the RTS line low, which signals the DCE device, through its RTS line, to begin to monitor its RX line. When the DCE device is ready to accept the data, it pulls its CTS line low, informing the DTE device, through its CTS connection, to begin sending data.

Figure 1-2. UART Connections Between Two DTE Devices

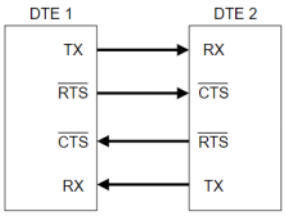
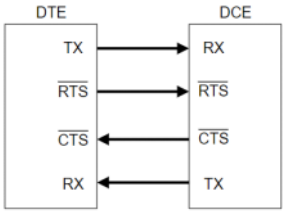


Figure 1-3. UART Connections Between a DTE Device and DCE Device



1.4.2 Software Flow Control

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Software flow control uses the XON/XOFF (Transmit ON/Transmit OFF) method. **This method has an advantage over hardware flow control methods since it does not require additional hardware lines, which significantly reduces wiring complexity.**

In the XON/XOFF method, special characters are sent by the receiver to the transmitter that are used to suspend and resume transactions. These characters are not specifically defined by any standard, such as ASCII. However, the ASCII standard provides generic 'device control' characters, DC1 – DC4. **The UART module specifically uses the ASCII control characters DC1 (0x11) and DC3 (0x13) as the XON and XOFF control characters, respectively. When one terminal is unable to accept data, it sends the XOFF character to the other terminal, which in turn suspends transmission. When the other terminal is ready to accept data again, it simply sends the XON character back to the first terminal, which resumes transmission.** **The Software Flow Control Transmit Enable Status (XON) bit of the UxFIFO STATUS register can be used to determine if the transmitter is enabled/disabled.**

1.5 Stop Bits

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The UART module offers a user-selectable number of Stop bits. The **Stop bit selections** are as follows:

- **1 Stop bit:** UART transmits one Stop bit; **the receiver verifies the first Stop bit received**
- **1.5 Stop bits:** UART transmits 1.5 Stop bits; **the receiver verifies the first Stop bit only**
- **2 Stop bits:** UART transmits two Stop bits; **the receiver verifies the first Stop bit only**
- **2 Stop bits:** UART transmits two Stop bits; **the receiver verifies both**

During normal operation, the transmitter returns to the Idle state for the number of Stop bit periods between each consecutively transmitted word. In all Stop bit configurations, the RX input is checked for an Idle condition during the middle of the first Stop bit period. In the case of the two Stop bit configuration where the receiver verifies both Stop bits, hardware checks the middle of both the first and second Stop bits for an Idle condition. **If any Stop bit verification indicates a non-Idle condition, the Framing Error Interrupt Flag (FERIF) bit of the UART Error Interrupt Flag (UxERRIR) register becomes set, indicating a frame error for that particular byte.**

1.6 Checksums

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Checksum calculations are used to verify that the data contained in a packet was transmitted/received correctly. When the Checksum Mode Select (C0EN) bit of UxCON2 is set, transmit and receive checksum adders accumulate the value of each byte transmitted or received.

In Transmit mode, the checksum adders accumulate the value of each byte transmitted. Once all bytes have been transmitted, th e sum of the byte values are loaded into the UART Transmit Checksum Result (UxTXCHK) register, which is then sent as the final byte of the transmission.

In Receive mode, the checksum adders accumulate the value of each byte received. Once all bytes have been received, including the checksum byte, the sum of the received byte values are loaded into the UART Receive Checksum Result (UxRXCHK) register.

It is important to note that although UART hardware calculates the checksums and loads the results into the appropriate check sum registers, software must clear UxTXCHK and UxRXCHK before beginning UART transactions, and also performs the checksum comparisons at the end of each transaction.

1.7 Baud Rate Generation

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The **UART Baud Rate Generator (BRG) is a 16-bit time**r used to **generate the clocking mechanism required for communication**. The timer consists of the UART Baud Rate Generator High and Low register pair (UxBRGH:UxBRGL). **The Baud Rate Generator Speed Select (BRGS) bit of UxCON0 determines the number of baud clocks used per bit.**

When BRGS is clear (BRGS = 0), the BRG is configured in the normal baud rate range. In the normal baud rate range, the BRG generates 16 clock periods per data bit. Equation 1-1 shows the formula used to calculate the baud rate when BRGS is clear. The result of this formula should be loaded into the UxBRGH:UxBRGL register pair.

Equation 1-1. Baud Rate Formula (BRGS = 0)

$$Desired\,baud\,rate = \frac{Fosc}{16 * (UxBRGH:UxBRGL + 1)}$$

When BRGS is set, the module is configured in the high baud rate range. In high baud rate range, the BRG generates four clock periods per data bit. This range is intended for use when the normal baud range cannot produce the desired baud rate. Equation 1-2 shows the formula used to calculate the baud rate when BRGS is set.

Equation 1-2. Baud Rate Formula (BRGS = 1)

$$Desired\,baud\,rate = \frac{Fosc}{4 * (UxBRGH:UxBRGL + 1)}$$

Writing to the UxBRGH:UxBRGL register pair will immediately change the baud rate. If the register pair is written while the module is actively transmitting or receiving data, a receive error may occur. It is recommended that writes to the register pair occur when the Receive Pin Idle Status (RXIDL) bit of UxFIFO is set (RXIDL = 1), indicating an Idle condition. Additionally, if the system clock (FOSC) is changed during active communication, a receive error may occur.

It is important to note that the BRG relies on the system clock (FOSC) to generate the baud rate. If the system clock deviates from its frequency (due to noise, temperature, oscillator drift, etc.), the baud rate will also change, resulting in framing or overrun errors. The Auto-Baud Detection feature can be used to ensure that the bit rate is acceptable for error-free communication.

1.8 Auto-Baud Detection

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The UART module offers an automatic baud rate detection system when operating in 8-bit modes only. **The Auto-Baud Detection system prevents data loss or corruption by measuring the incoming signal on the RX pin and updating the UxBRGH:UxBRGL register pair to match the incoming rate.** The Auto-baud Detection Enable (ABDEN) bit of UxCON0 controls the automatic baud rate detection system.

It is important to note that the BRG is used to measure the period of the received character 'U', or 0x55. This character is unique in the sense that it contains five alternating rising and falling edges. The auto-baud calibration sequence begins on the first falling edge of the character after the ABDEN bit is set. While the calibration sequence is active, the UART state machine is held in an Idle state, and the UxBRGH:UxBRGL register pair is clocked at 1/8th the base baud rate. The sequence ends on the 5th falling edge of the incoming character. At that point, the measured time value is loaded into the UxBRGH:UxBRGL register pair, the ABDEN bit is cleared, and the Auto-Baud Detect Interrupt Flag (ABDIF) is set.

1.8.1 Auto-Baud Overflow

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If the baud rate counter overflows before the 5th falling edge is detected, the Auto-Baud Detect Overflow Interrupt Flag (ABDOVF) bit of UxERRIR is set, indicating an overflow condition. An overflow occurs when the 16-bit counter exceeds its maximum size. In this case, the state machine continues to wait for the 5th falling edge to occur on the RX pin. Once the 5th falling edge is detected, hardware sets the Auto-Baud Detect Interrupt Flag (ABDIF) bit of the UART General Interrupt Register (UxUIR) and clears the ABDOVF bit of UxERRIR, while the previous BRG values are retained. To terminate the auto-baud process once an overflow is detected, but before the 5th falling edge is detected, software must first clear the ABDEN bit and then clear the ABDOVF bit.

1.8.2 Wake-up on Break

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The UART module is inactive in Sleep mode since the clock sources are disabled. This means that the UART cannot transmit or r eceive data while the device is in Sleep mode. The UART module offers an automatic wake-up feature that will wake the device when activity on the RX pin is detected.

The auto-wake-up feature is enabled by setting the Wake -Up Enable (WUE) bit of UxCON1. When WUE is set, the UART remains in an Idle state while waiting for a transition from the Idl e state to the active state on the RX pin. To prevent data loss, the RXIDL bit should be read to ensure that the receiver is idle before setting WUE and issuing a Sleep command.

If the WUE bit is set, but before the Sleep command is issued, and a transition from the Idle -to-Active state is detected, module hardware sets the WUIF at the beginning of the next instruction cycle, but does not enter Sleep. Once the transition from the Active -to-Idle state occurs, hardware clears the WUE bit.

When the wake-up event occurs, the Wake-Up Interrupt Flag (WUPIF) bit of the UxUIR register and the UART Interrupt Flag (UIF) of the Peripheral Interrupt (PIRx) regi ster are set. At this point, the receiver will begin to monitor for a transition from the Active state back to the Idle state. When the Active state is detected, module hardware cle ars the WUE bit. It is important to note that the UIF is read -only; software must clear WUPIF to clear UIF.

1.8.2.1 Special Considerations

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It is important to note that special considerations must be taken to prevent fragmented or lost data when using the auto-wake-up feature.

When using the auto-wake-up feature, a Break character must be received as the first character to wake the device. A Break character consists of all zeros and must persist for a minimum of 11 bit times before the next character is received. UART hardware uses a dedicated counter to detect when the RX input remains in the Space (0) state, and once the 11 bit period time has expired, the Break condition is detected. The Break Reception Interrupt Flag (RXBKIF) bit of the UxERRIR register can be used by software to detect that a Break condition has completed. The Receive Break Interrupt Mode Select (RXBIMD) bit of the UxCON1 register controls when the RXBKIF becomes set after a Break is detected. When RXBIMD is set, the RXBKIF is set immediately after a Break has been detected. When RXBIMD is clear, RXBKIF is set when the transition from the Active-to-Idle state on the RX input is detected following the Break character.

If WUE is set and a non-zero character is received to wake the device, the time between the Start bit and the first rising edge of the character will be interpreted as the wake-up event. Since the minimum 11 zero-bit times condition was not met, the remaining bits of the received character will be interpreted as a fragmented character, and all subsequent characters will result in farming or overrun errors.

A Break character can be sent by either using a fixed-length Break period or a software-timed Break period.

A fixed-length Break period consists of a Start bit, 12 zero-bits, and a Stop bit. To send a fixed-length Break, software must set the Send Break Control (SENDB) bit of the UxCON1 register. Once SENDB is set, a write to UxTXB will initiate the Break sequence. The receiver will receive the Break character first, followed by the character written into UxTXB.

A software-timed Break period does not contain any specific number of bit times. Instead, a Timer resource can be used to generate the Break condition. The software-timed Break is generated by setting and clearing the Send Break Software Override (BRKOVR) bit of the UxCON1 register. When BRKOVR is set, the TX output is forced into a non-Idle state; when clear, the TSR controls the TX output. In this case, the BRKOVR bit could be set when the Timer resource begins to count and cleared once the Timer has expired. This method allows the user to create a custom Break period.

Additionally, since the system clock is disabled during Sleep, the oscillator start-up time must be considered. In this case, additional time is needed for the oscillator to stabilize. To ensure that the Break period is long enough to meet the minimum eleven zero-bit periods and allow the oscillator to stabilize, the software-timed Break method may be used.

1.9 RX/TX

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The Timer2/4/6 modules contain a Hardware Limit Timer (HLT) function that can be used to monitor activity on the RX and TX lines. The Timer2/4/6 module uses the Timer External Reset Signal Selection Register (TxRST) to reset the Timer when a user-selectable Reset event occurs. In this case, a value representing the desired time-out delay is loaded into the Timer Count Register (TxTMR). When a transition from an Idle state to an Active state on the TX output or RX input line will reset the Timer, indicating that the desired line (RX/TX) is active. If no transitions occur before the Timer expires, the HLT interrupt will occur, signaling a time-out event.