Boost converter

8k6 78mW resistor from B+ to each anode (IN-12B)

VIN
FB2 60R@100MHz
VCC
L1 330u
Vf < 0.92V
D1 ES1D
FB1 60R@100MHz
170V
B+

C7 10u 16V
C9 100n
C8 C11 C13 C14 C16 C19 C22 C24 C25
C6 10u 50V 100uF
GND
C10 560p 250V
C2 1u 250V
C5 GND 2uF
C4 100n 250V
C1 100n 250V
GND

C3 100p 250V
R2 523k, 1%
FB

TP_GATE GND
R18 10R
Q2 BSC900N20NS3 G
TP_FB
R3 7.68k, 1%
GND

GATE_SIG

ISENSE

TP_ISENSE
R17 0R1, 1W
GND

Gate driver

VCC
R19 24R
R6 4k7
D2 BAT54WS-TP
GND
TP_COMP
VCC

VIN
R8 100k
C18 C21 10u 50V 20uF
R11 220k
GND
3.8V
R13 0
C17 100n
GND
Increase resistor if VCC>12V

ENABLE
R16 1k
Q1 BSS131H6327XTSA1
GND
C20 220p
R9 0
R7 0
VCC UVLO thresholds 7.2V - 6.9V

OUT has 0% duty if COMP is at GND

FB
U1 UCC3800
$V_{out}=VCC=12V$
GATE_SIG

VREF
5V +-1.5%
$I_{ref, max}=5mA$
VREF
COMP
FB
VCC
OUT
$I_{out, avg}=Q_g*f=11.6nC*110.33kHz=1.28mA$
$I_{VCC,max}=25mA$

C23 100n
GND
R15 0
R14 41.2k
$U_{p-p}=2.45V$ (0.2V - 2.65V)
REF
RC
GND
CS
VREF
R5 4.12k 1%
R10 1k 1%
ISENSE

C15 330p
GND
$f=1.5/RC=$
$=1.5/(41.2k*330p)=$
$=110.33kHz$
1V @ Imax
1.55V @ Imax,OC
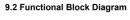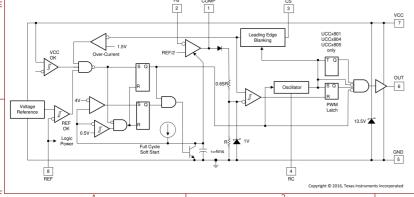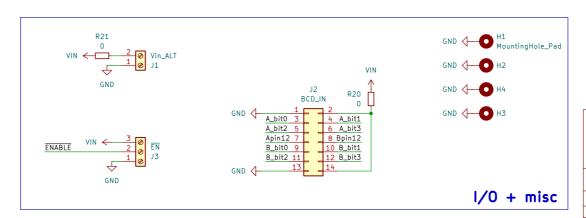OverCurrent triggers soft-start cycle
C12 1n
GND
R12 390k 1%

The maximum duty cycle limit is set by the ratio of the external oscillator charging resistor RT and the internal oscillator discharge transistor on-resistance

Device Comparison Table

PART NUMBER	MAXIMUM DUTY CYCLE	REFERENCE VOLTAGE	TURNON THRESHOLD	TURNOFF THRESHOLD
UCC2800	100%	5 V	7.2 V	6.9 V
UCC2801	50%	5 V	9.4 V	7.4 V
UCC2802	100%	5 V	12.5 V	8.3 V
UCC2803	100%	4 V	4.1 V	3.6 V
UCC2804	50%	5 V	12.5 V	8.3 V
UCC2805	50%	4 V	4.1 V	3.6 V

9.2 Functional Block Diagram

VCC OK
Over-Current 1.5V
REF/2
Leading Edge Blanking
UCCx801 UCCx804 UCCx805 only
VCC 7
FB 2
COMP 1
CS 3
0.65RC
Oscillator
OUT 6
Voltage Reference
4V
REF OK
Logic Power
0.5V
R S Q
Full Cycle Soft Start
PWM Latch
13.5V
t=4ms
1V
GND 5
REF 8
RC 4

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Demux — Open-collector outputs

2 tubes of 11 cathodes

DemultiplexerArray
A_bit0 LSB
A_bit1
A_bit2
A_bit3 MSB
Apin12
OutTransistorArray
CD4028B
SN75468
J5 TubeA
B+
8.66k R1

B_bit0
B_bit1
B_bit2
B_bit3
Bpin12
J4 TubeB
B+
8.66k R4

I/O + misc

R21 0
VIN
Vin_ALT
J1
GND
GND H1 MountingHole_Pad
GND H2
GND H4
GND H3

J2 BCD_IN
R20 0
VIN
GND A_bit0 — A_bit1
A_bit2 — A_bit3
Apin12 — Bpin12
B_bit0 — B_bit1
B_bit2 — B_bit3
GND

ENABLE VIN
EN J3

U5 4028 — C27 100n — VIN — GND

Pin	Signal
16	VDD
10	A — B_bit0
13	B — B_bit1
12	C — B_bit2
11	D — B_bit3
8	VSS / GND
3	S0 — Bpin11
14	S1 — Bpin10
2	S2 — Bpin09
15	S3 — Bpin08
1	S4 — Bpin07
6	S5 — Bpin06
7	S6 — Bpin05
4	S7 — Bpin04
9	S8 — Bpin03
5	S9 — Bpin02

U6 4028 — C26 100n — VIN — GND

Pin	Signal
16	VDD
10	A — A_bit0
13	B — A_bit1
12	C — A_bit2
11	D — A_bit3
8	VSS / GND
3	S0 — Apin11
14	S1 — Apin10
2	S2 — Apin09
15	S3 — Apin08
1	S4 — Apin07
6	S5 — Apin06
7	S6 — Apin05
4	S7 — Apin04
9	S8 — Apin03
5	S9 — Apin02

TABLE I — TRUTH TABLE

D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

I = HIGH LEVEL   0 = LOW LEVEL

BCD INPUTS — D C B A — CD4028B — 9 8 7 6 5 4 3 2 1 0 — 1 OF 10 NUMERALS — V_T

TUBE REQUIREMENTS

Type		V_T (Vdc)	mA/numeral
Burroughs	B4081	170	14
	B4336/718	170	7
	B4032	170	14
	B4021	120	14

TRANSISTOR CHARACTERISTICS

Leakage with transistor cutoff — 0.05mA

$V_{(BR)CEO}$ < 70V

92CS-29413

▲(Trademark) Burroughs Corp.

Fig. 14 — Neon readout (Nixie Tube▲) display application.

by Miki

Sheet: /DemultiplexerArray/
File: demux.kicad_sch

Title: BCD-to-Decimal Demux

Size: A5 | Date: 2024-12-29 | Rev: 1.0
KiCad E.D.A. 8.0.7 | Id: 3/3

U3
SN75468

- COM — 9 ✕
- Apin02 — 1 I1 — O1 16 — Cath_Apin02
- Apin03 — 2 I2 — O2 15 — Cath_Apin03
- Apin04 — 3 I3 — O3 14 — Cath_Apin04
- Apin05 — 4 I4 — O4 13 — Cath_Apin05
- Apin06 — 5 I5 — O5 12 — Cath_Apin06
- Apin07 — 6 I6 — O6 11 — Cath_Apin07
- Apin08 — 7 I7 — O7 10 — Cath_Apin08
- 8 GND
- GND

U4
SN75468

- COM — 9 ✕
- Bpin05 — 1 I1 — O1 16 — Cath_Bpin05
- Bpin06 — 2 I2 — O2 15 — Cath_Bpin06
- Bpin07 — 3 I3 — O3 14 — Cath_Bpin07
- Bpin08 — 4 I4 — O4 13 — Cath_Bpin08
- Bpin09 — 5 I5 — O5 12 — Cath_Bpin09
- Bpin10 — 6 I6 — O6 11 — Cath_Bpin10
- Bpin11 — 7 I7 — O7 10 — Cath_Bpin11
- 8 GND
- GND

U2
SN75468

- COM — 9 ✕
- Apin09 — 1 I1 — O1 16 — Cath_Apin09
- Apin10 — 2 I2 — O2 15 — Cath_Apin10
- Apin11 — 3 I3 — O3 14 — Cath_Apin11
- ✕ 4 I4 — O4 13 ✕
- Bpin02 — 5 I5 — O5 12 — Cath_Bpin02
- Bpin03 — 6 I6 — O6 11 — Cath_Bpin03
- Bpin04 — 7 I7 — O7 10 — Cath_Bpin04
- 8 GND
- GND

The SN75468 has a 2700-Ω series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS. The SN75469 has a 10.5-kΩ series base resistor to allow its operation directly with CMOS or PMOS that use supply voltages of 6 to 15 V. The required input current is below that of the SN75468.

Q4 circuit

- Cath_Apin12
- Apin12 — R22 1k — 1 — Q4 BSS131H6327XTSA1
- R25 100k — GND
- GND GND

Q3 circuit

- Cath_Bpin12
- Bpin12 — R23 1k — 1 — Q3 BSS131H6327XTSA1
- R24 100k — GND
- GND GND

COM
C
B — R_B
SN75468: R_B = 2.7 kΩ
SN75469: R_B = 10.5 kΩ
7.2 kΩ 3 kΩ
E

All resistor values shown are nominal.

TODO: CONSIDER HIGHER VOLTAGE VERSION (SN75469)

by Miki

Sheet: /OutTransistorArray/
File: TranArray.kicad_sch

Title: 2x11 Darlington Array for Nixie Tubes

Size: A5   Date: 2024-12-29   Rev: 1.0
KiCad E.D.A. 8.0.7   Id: 3/3