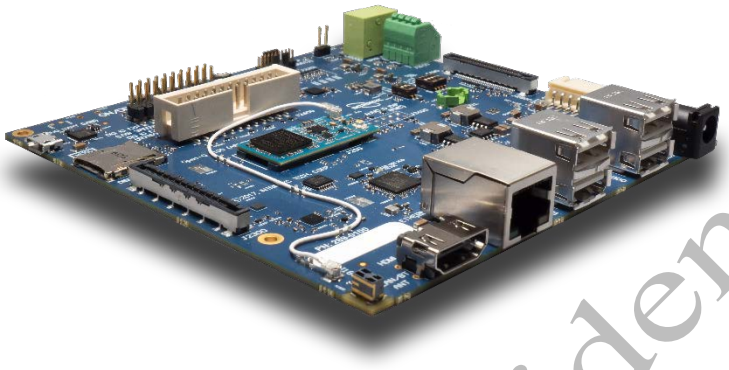

Intrinsyc Open-Q™ 2100 SOM Development Kit Technical Note 23:

Display Board Design Guide

[Document: ITC-01RND1260-TN-023 Revision: 1.1]

Identification

Document Title	Intrinsyc Open-Q™ 2100 SOM Development Kit Technical Note 23: Display Board Design Guide
Document Number	ITC-01RND1260-TN-023
Version	1.1
Date	07/06/2017 11:38:00 AM

History

REVISION	DATE	DESCRIPTION	PAGES
1.0	May 5, 2017	Initial Draft	All
1.1	June 7, 2017	Updated dev kit photo	Title page

Table of Contents

1. INTRODUCTION

1.1 Purpose

The purpose of this document is to provide guidelines and technical information for any user desiring to design their own Display Board to connect to the Intrinsyc Open-Q™ 2100 SOM Development Kit.

For background information on the kit, refer to
http://www.intrinsyc.com/products/qualcomm/dragonboard-development-kits.aspx

1.2 Scope

This document presents guidelines and technical information for designing a user specific Display Board for the Open-Q™ 2100 SOM Development Kit.

1.3 Intended Audience

This document is intended for end users who have purchased an Intrinsyc Open-Q™ 2100 SOM Development Kit and wish to design their own custom Display Board.

1.4 Organization

This document is organized as follows:

- **Section 1. Introduction:** This section describes the purpose, scope and structure of this document.
- **Section 2. Documents:** This section lists other documents that are parents of or supplement this document.
- **Section 3. Mechanical Guidelines:** This section identifies the mechanical design guidelines for developing a custom Display Board for the Open-Q™ 2100 SOM Development Kit.
- **Section 4. Electrical Guidelines:** This section identifies the electrical design guidelines for developing a custom Display Board for the Open-Q™ 2100 SOM Development Kit.

2. DOCUMENTS

This section lists any parent and supplementary documents for the Open-Q™ 2100 Development Kit Technical Note. Unless stated otherwise, applicable documents supersede this document and reference documents provide background and supplementary information.

2.1 Applicable Documents

REFERENCE	AUTHOR	TITLE
A-1	Intrinsyc	Intrinsyc Purchase and Software License Agreement for the Open-Q™ 2100 SOM Development Kit

2.2 Reference Documents

REFERENCE	TITLE
R-1	Open-Q™ 2100 SOM Development Kit Schematics
R-2	Open-Q Display Board Schematics
NOTE: Please contact Intrinsyc or visit http://support.intrinsyc.com/ to get access to the reference documents.	

3. MECHANICAL DESIGN GUIDELINES

3.1 Display Board Connector

The Open-Q™ 2100 SOM Development Kit provides a reference design from which customers can design, develop, test, and deploy their product solutions around the popular and powerful Qualcomm APQ8009W processor. The connector on the Open-Q™ 2100 carrier board (J2300) and the display board is a 51-pin connector from JAE (FI-R series, P/N: FI-RE51S-*F, *=V or H) and can be mated using a flex cable (JAE, JF08 Series, P/N: JF08R0R051***MA). It is recommended that a maximum 20cm cable be used (*** = 020). Please see the connector pinouts for the carrier and display board schematics (documents R-1 and R-2) or the connector datasheet for details.

Note: The JF08 series cable is a straight cable, therefore the designer should pay attention to how the pinout order is mirrored between the display board and the carrier board, as shown in the figure below. Pin 1 connects to pin 51 and vice versa.

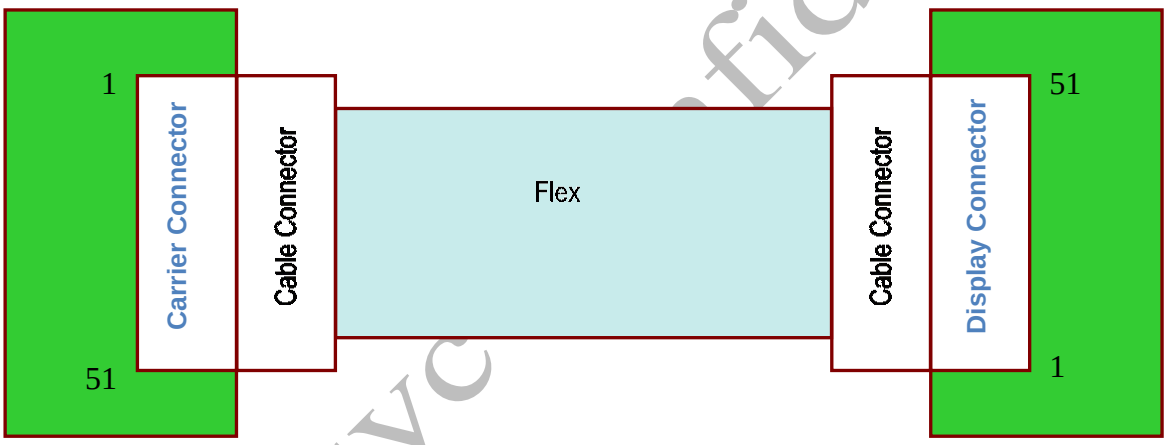

Figure 1 - Pin Mirroring on Cable

4. ELECTRICAL DESIGN GUIDELINES

4.1 Introduction

This section describes the electrical design guidelines for developing a custom Display Board. The section is organized by functionality and it is recommended to refer to the Open-Q™ 2100 SOM Development Kit schematics for more details.

The pin numbers listed in the tables below are referenced to the display connector on the carrier board (J2300). If there are pinout differences between the table below and the Open-Q™ 2100 SOM Development Kit schematics, the latter shall be assumed correct.

Unless otherwise indicated, all CPU GPIO lines listed in the tables below are referenced to the main +1.8V IO power rail, VREG_L4_1P8.

4.2 Power

This section describes the power rails available to the display board.

Table 1 –Power Signal Group

J2300 Pin #	Pin Name	Description	Notes
2	VREG_L4_1P8	This 1V8 rail is driven by VREG_L4_1P8 from the PM8916-1	Intended usage: Touch Panel 1V8 rail
3	VREG_L17_2P85	This 2V85 rail is driven by VREG_L17_2P85 from the PM8916-1	Intended usage: LCD and Touch Panel 2V8 rail
4,5	DC_IN_*	This rail can be driven by either the 12VDC INPUT JACK (J3000) or the VPH_PWR rail on the carrier board	Intended usage: LCD Backlight driver input voltage. Population options exist on the carrier board to select the voltage source.
12	SBC_VREG_1P8	This 1V8 rail is driven by an on-board power supply on the carrier board	Intended usage: LCD 1V8 rail.
1, 25, 28, 31, 34, 37, 40, 43	GND	Ground reference for design	

4.3 MIPI Display Signals

The signals contained in this section are the MIPI display clock and data lines that are connected to the display connector. The MIPI interface is driven by a 2:1 MIPI D-PHY Switch with the APQ8009W GPIO110 (0:MIPI DSI, 1: HDMI Bridge) as the path selector. The designer should be aware of the impedance and trace length matching requirements when routing the MIPI differential pairs.

Table 2 – MIPI Signal Group

J2300 Pin #	Pin Name	Description	Notes
38, 39	MIPI_DSI0_DATA3_CONN_N/P	MIPI Display 0 Data Lane 3 differential pair.	
41, 42	MIPI_DSI0_DATA2_CONN_N/P	MIPI Display 0 Data Lane 2 differential pair.	

J2300 Pin #	Pin Name	Description	Notes
44, 45	MIPI_DSI0_DATA1_CONN_N/P	MIPI Display 0 Data Lane 1 differential pair.	
47, 48	MIPI_DSI0_DATA0_CONN_P/N	MIPI Display 0 Data Lane 0 differential pair.	**_N/P order is different than other data lanes**
50, 51	MIPI_DSI0_CLK_CONN_P/N	MIPI Display 0 Clock differential pair.	**_N/P order is different than data lanes**

4.4 Control Signals

The signals contained in this section are the GPIO lines used for controlling various interfaces on the display board.

Table 3 – Control Signal Group

J2300 Pin #	Pin Name	Description
6	WLED_PWM_MPP_2	Connected to PM8916-1 MPP_02. Intended usage is for backlight PWM. This multi-purpose pin has a configurable IO voltage level.
7	N/C	-
8	GPIO_18_BLSP5_BIT1_TS_I2C_SDA	Connected to APQ8009W GPIO18. Intended usage is touch screen I2C.
9	GPIO_28_DISPLAY_GP1_C	Connected to APQ8009W GPIO1. This is a spare GPIO.
10	N/C	
11	GPIO_19_BLSP5_BIT0_TS_I2C_SCL	Connected to APQ8009W GPIO19. Intended usage is touch screen I2C.
13	N/C	
14	GPIO_13_BLSP4_2_TS_INT_N	Connected to APQ8009W GPIO13. Intended usage is touch screen interrupt.
15	LCD_BKLT_EN	Connected to APQ8009W GPIO37. Intended usage is for backlight on/off control if needed.
16	GPIO_24_LCD_TE	Connected to APQ8009W GPIO24. Intended usage is for display TE output.
17	N/C	-
18	N/C	-
19	N/C	-
20	GPIO_53_TS0_GP1_C	Connected to APQ8009W GPIO53. This is a spare GPIO.
21	N/C	
22	GPIO_12_BLSP4_3_TS_RESOUT_N	Connected to APQ8009W GPIO12. Intended usage is touch screen reset.
46	GPIO_25_LCD_RST_N	Connected to APQ8009W GPIO25. Intended usage is display reset.
49	N/C	