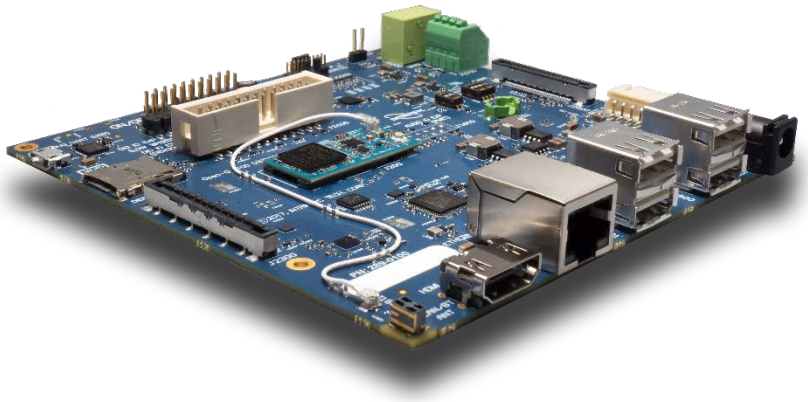

Intrinsyc Open-Q™ 2100 (APQ8009W) Development Kit Technical Note 22:

SOM Carrier Board Design Guide

[Document: ICS-01IMP1260-TN-022 Version: 1.2]

IDENTIFICATION

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1.0	May 01, 2017	Initial Draft	All
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1. INTRODUCTION

1.1 Purpose

The purpose of this document is to provide guidelines and technical information for any user desiring to design their own Carrier Board for the Intrinsyc Open-Q 2100 System On Module (SOM).

For background information on the kit, please refer to https://www.intrinsyc.com/snapdragon-embedded-development-kits/open-q-2100-development-kit/

1.2 Scope

This document presents guidelines and technical information for designing a user specific Carrier Board for the 2100 SOM.

1.3 Intended Audience

This document is intended for end users who have purchased an Intrinsyc Open-Q 2100 (APQ8009W) Development Kit and wish to design their own custom Carrier Board for the SOM.

1.4 Organization

This document is organized as follows:

- **Section 1. Introduction:** This section describes the purpose, scope, and structure of this document.
- **Section 2. Documents:** This section lists other documents that are parents of or supplement this document.
- **Section 3. Mechanical Design Guidelines:** This section identifies the mechanical design guidelines for developing a custom Carrier Board for the Open-Q 2100 (APQ8009W) Development Kit SOM.
- **Section 4. Electrical Design Guidelines:** This section identifies the electrical design guidelines for developing a custom Carrier Board for the Open-Q 2100 (APQ8009W) Development Kit SOM.
- **Section 5. Electrical Specifications:** This section contains the electrical specifications for the Open-Q 2100 SOM.

2. DOCUMENTS

This section lists any parent and supplementary documents for the Open-Q 2100 (APQ8009W) Development Kit Technical Note. Unless stated otherwise, applicable documents supersede this document and reference documents provide background and supplementary information.

2.1 Applicable Documents

REFERENCE	AUTHOR	TITLE
A-1	Intrinsyc	Intrinsyc Purchase and Software License Agreement for the Open-Q 2100 (APQ8009W) Development Kit

2.2 Reference Documents

REFERENCE	TITLE
R-1	Open-Q 2100 Schematics (SOM, Carrier)
R-2	Open-Q 2100 BOM
NOTE: Please contact Intrinsyc or visit http://support.intrinsyc.com/ to get access to the reference documents.	

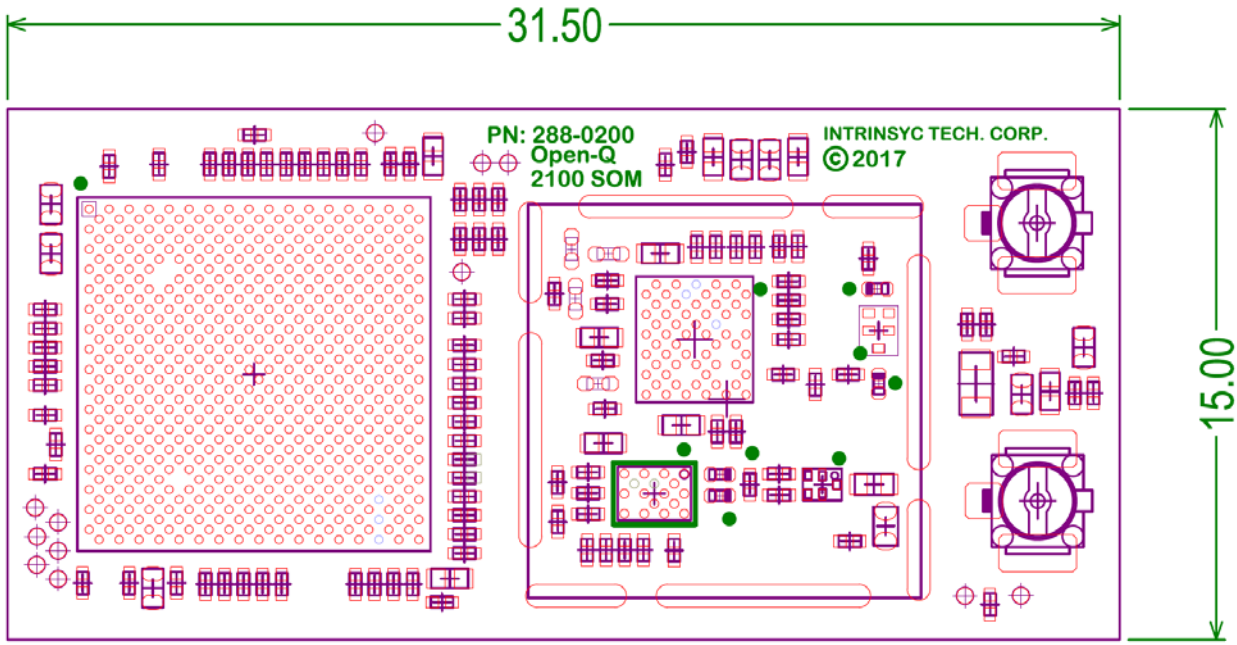
3. MECHANICAL DESIGN GUIDELINES

3.1 Introduction

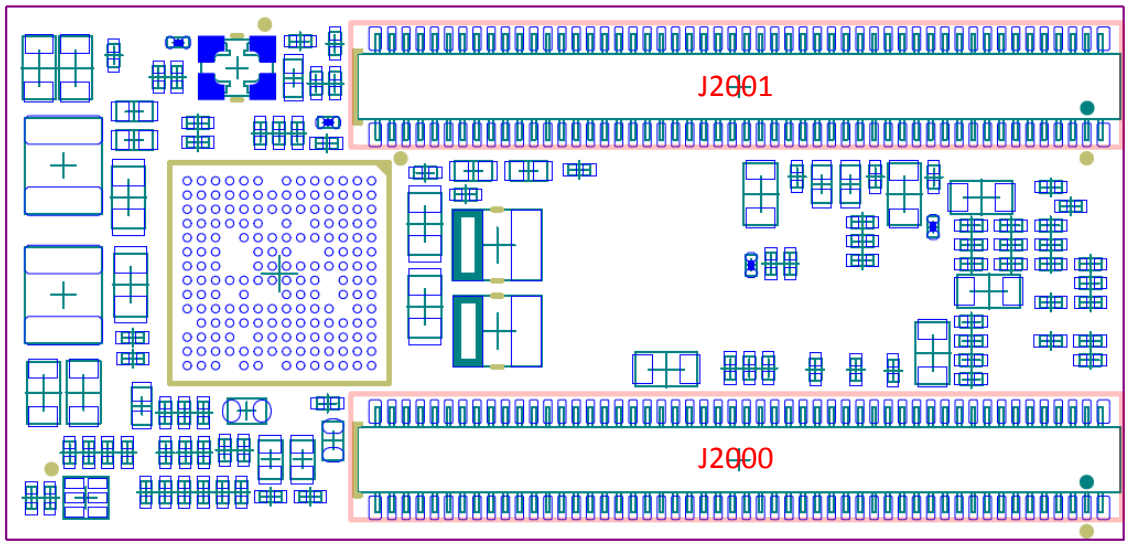
The Open-Q 2100 (APQ8009W) Development Kit provides a reference from which customers can design, develop, test, and deploy their product solutions around the popular and powerful Qualcomm APQ8009W processor. This section describes the mechanical design guidelines for developing a custom Carrier Board for the SOM.

3.2 SOM Mechanical Outline

The physical outline and dimensions of the SOM are shown in the figure below:



(a) SOM Top View



(b) SOM Bottom View

Figure 1 – SOM Mechanical Outline (Dimension in mm)

3.3 Top and Bottom Height Restrictions

The tallest component on the top side and bottom side of the SOM with shield installed are 1.26mm and 1.29mm respectively.

The stacking height between Carrier Board and the SOM depends on the connector used in the Carrier board. Open-Q 2100 Carrier board uses connecter with 1.5mm stacking height. It is recommended that there be no components placed in the area on the Carrier Board underneath the SOM when stacking height between the Carrier Board and SOM is 1.5mm. Please see section 3.4 below for more details.

For 3D design files, please see http://support.intrinsyc.com/

3.4 Carrier Board Connector, Mounting Hole and Thermal Relief Locations

The APQ8009W SOM mounts to the Open-Q carrier board through two 100-pin board to board connectors. Customers that are designing their own carrier board must ensure that their connector pinouts match the ones on the Open-Q 2100 development kit carrier board schematic (see R-1)

The following mechanical features are required to connect the APQ8009W SOM to the carrier board. When designing a custom carrier board, please keep these dimensions in mind. See Figure 2 for further details.

- Board to Board connector: 100-pin, 0.4mm pitch board-board connector. The connector part number is Hirose DF40C-100DS-0.4V(51) which gives a 1.5mm stack-up distance between the carrier board and the SOM.
- Customer can choose connector with different stacking height. Please make sure the connector on the Carrier board mates with the SOM connector part number DF40C-100DP-0.4V(51).

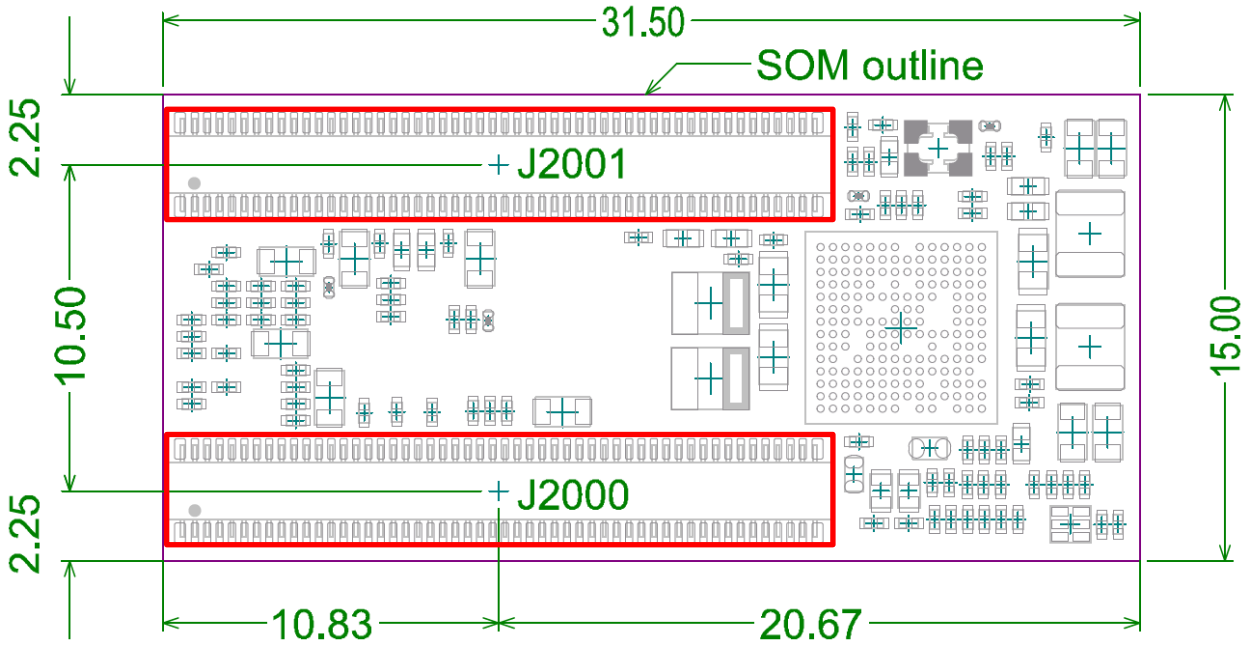


Figure 2 – SOM mating connectors on carrier board (Looking through SOM; dimension in mm)

3.5 Antenna Connectors

The SOM contains two U.FL coaxial receptacles (Hirose U.FL-R-SMT-1 (10)) for connecting to GNSS, and WLAN/ BT RF antennas (see the Open-Q 2100 bill of materials, document R-2, for the mating coaxial cable part numbers).

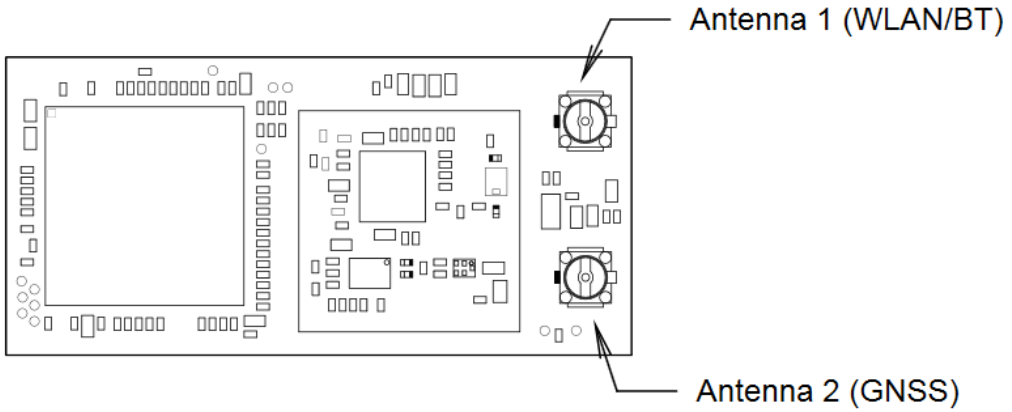


Figure 3 – Antenna connectors on the SOM

4. ELECTRICAL DESIGN GUIDELINES

4.1 Introduction

This section outlines the electrical design guidelines for developing a custom Carrier Board for the Open-Q 2100 SOM. The section below is organized by functionalities and only covers the signals that are available on the board to board connectors. Please refer to the Open-Q 2100 schematics (R-1) for more details.

If there are pinout differences between the tables below and the SOM schematic, the latter shall be assumed correct.

Please see the notes column in the sections below for any critical design guidelines.

4.2 Input Power

The APQ8009W SOM can be powered by a +3.7V DC power source or a single cell Lithium-Ion Polymer (LiPo) battery pack. See tables below for details on how to power the SOM via a power source or a battery. It is recommended that over current and reverse polarity protection circuits be implemented on the carrier board.

4.2.1 Powering SOM with DC Power Source

Table 1 – Critical Input Power Signals when Powering SOM with DC Power Source

Board to board connector pin #	Pin Name	Description	Notes
J2001-75	VCOIN	Optional +3V coin cell backup battery connection to the PM8996 PMIC.	Connect the positive terminal of the coin cell to VCOIN (J2001-75) and the negative terminal to GND.
J2000-[51,53,55,57,59,61,63] J2001-[62,64,66,68,70,72,74]	VPH_PWR	3.8V DC power input to SOM.	Connect to power source input. Place the SOM input power source (3.8V) as close as possible.
J2000-84	BATT_ID	Battery identification input to the PMI8916-1 PMIC on the SOM	Pull BATT_ID to GND with a 100K Ohm resistor. Add a 100K resistor population option from BATT_ID pin to the VREF_BATT_THERM (pin J2000-86).
J2000-88	PM_BATT_THERM	Battery thermistor input to the PMI8916-1 PMIC on the SOM	Pull PM_BATT_THERM to GND with a 100K Ohm resistor, Add a 100K resistor population option from PM_BATT_THERM pin to the VREF_BATT_THERM (pin J2000-86).

Board to board connector pin #	Pin Name	Description	Notes
J2001-84	OPT_1	External charger option	Connect a 0R resistor population option to GND. Pulling OPT_1 to GND enables external charger and leaving it floating enables PMIC charger.
J2000-[98,100]	VDD_EAR_SPKR	Ear and class-D speaker amplifier input supply. Software configurable voltage 5V or VPH_PWR.	Expected use: Audio
J2000-[7,13,19,25,31,37,43,49,79,16,22,28,60,76,78] J2001-[35,61,81,85,95,38,52,60,62,82,94]	GND	Ground reference for design	

4.2.2 Powering SOM with LiPo Battery

Table 2 – Critical Input Power Signals when Powering SOM with LiPo Battery

Board to board connector pin #	Pin Name	Description	Notes
J2000-[51,53,55,57,59,61,63] J2001-[62,64,66,68,70,72,74]	VPH_PWR	3.7V DC power input to SOM.	Connect power rail VPH_PWR to the positive terminal of the battery pack. It is strongly recommended to use over-voltage/under-voltage protection on VPH_PWR rail. Please refer section 5 for electrical specifications.
J2000-84	BATT_ID	Battery identification input to the PMI8916-1 PMIC on the SOM	Connect BATT_ID rail to the battery ID terminal of the battery pack. If battery ID function is not supported by the battery or not used, pull BATT_ID low with a 100K resistor to GND. Add a 100K resistor population option from BATT_ID pin to the VREF_BATT_THERM (pin J2000-86).
J2000-88	PM_BATT_THERM	Battery thermistor input to the PMI8916-1 PMIC on the SOM	Connect PM_BATT_THERM rail to the thermal resistance terminal of the battery pack. If battery pack does not have a thermistor, connect PM_BATT_THERM to GND with a 100K Ohm resistor. Add a 100K resistor population option from PM_BATT_THERM pin to the VREF_BATT_THERM (pin J2000-86).

Board to board connector pin #	Pin Name	Description	Notes
J2001-84	OPT_1	External charger option	Connect a 0R resistor population option to GND. Pulling OPT_1 to GND enables external charger and leaving it floating enables PMIC charger.
J2000-[67,69,71,73,75,77]	USB2_VBUS	USB VBUS input	Connect USB VBUS to this pin to provide USB battery charging feature
J2000-65	VBAT_SNS	VBAT sense input	Connect to the VPH_PWR rail/ battery positive terminal to sense battery voltage
J2000-[98,100]	VDD_EAR_SPKR	Ear and class-D speaker amplifier input supply. Software configurable voltage 5V or VPH_PWR.	Expected use: Audio
J2000-[7,13,19,25,31,37,43,49,79,16,22,28,60,76,78] J2001-[35,61,81,85,95,38,52,60,62,82,94]	GND	Ground reference for design	

NOTE: Users are suggested to consider external charger option when using a battery to power the SOM. Please refer the Open-Q^{tm} 2100 carrier board schematic for the reference design. It is also advised that a minimum three terminal battery with a pin for thermal resistance be used. Select a battery with a thermal resistance (R_{th}) of 100K at 25°C.

4.3 Boot Control Signals

To initiate the SOM boot up sequence, PHONE_ON_N and APQ_RESOUT_N need to be triggered. APQ_RESOUT_N is output reset signal from CPU and PHONE_ON_N and BOOT_CONFIG[X] signals are inputs to the CPU. Figure 4 below illustrates the power on sequence during SOM boot up. Please note that the diagram shown in Figure 4 is not drawn as a timing plot but rather as a sequencing diagram.

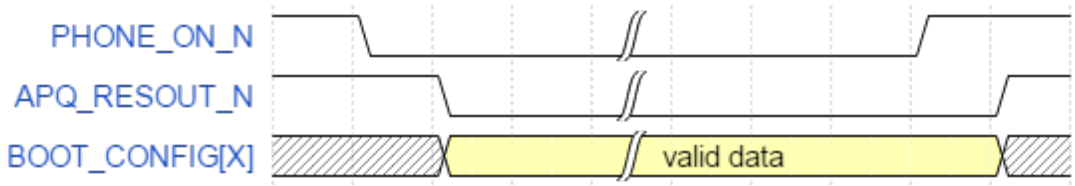


Figure 4 – Power on sequence during SOM boot up

Figure 5 shows an example of how to control the SOM boot signals. It is recommended that users follow this circuitry or implement something similar.

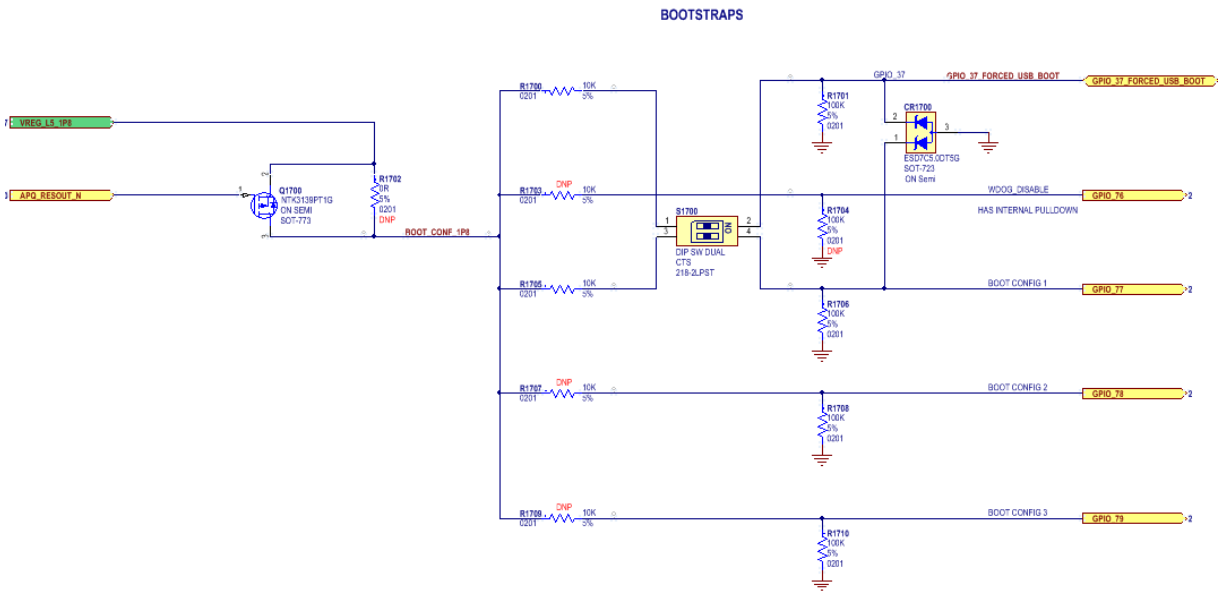


Figure 5 – Example circuitry for boot signals

The table below describes critical signals that are needed for SOM boot up.

Table 3 – Critical Boot Signals

Board to board connector pin #	Pin Name	Description	Notes
J2001-68	PHONE_ON_N	Power on input. Internally pulled up to +1.8V on SOM. Active low.	It is recommended to use a button to control this signal. Ensure that there are NO external pulls on this line
J2001-72	PMIC_RESIN_N	Reset input/Volume down. Internally pulled up to +1.8V on SOM. Active low	Connected to RESIN_N on PM8916-1. It is recommended to use a button to control this signal. Ensure that there are NO external pulls on this line
J2001-40	APQ_RESOUT_N	CPU reset output	APQ_RESOUT_N asserts low upon receiving power on input from PHONE_ON_N. Ensure that there are NO external pulls on this line
J2000-58	GPIO_76	Boot configuration 0/ watchdog disable. Configures external boot device	BOOT_CONFIG[0]/WDOG_DISABLE needs to be pulled low to enable boot options. It has internal pulldown and does not require external pulldown resistor.

Board to board connector pin #	Pin Name	Description	Notes
J2001-36	GPIO_77	Boot configuration 1. Configures external boot device	BOOT_CONFIG[1] needs to be pulled low with 100K ohm resistor (see table below)
J2001-34	GPIO_78	Boot configuration 2. Configures external boot device	BOOT_CONFIG[2] needs to be pulled low with 100K ohm resistor (see table below)
J2001-55	GPIO_79	Boot configuration 3. Configures external boot device	BOOT_CONFIG[3] needs to be pulled low with 100K ohm resistor (see table below)
J2000-47	FORCED_USB_BOOT (APQ_GPIO_37)	Forced USB boot	FORCED_USB_BOOT can be left floating/ pulled low with 100K ohm resistor. Forced USB boot for Intrinsyc internal use only

Table 4 – Boot Configurations

Boot Options/ Sequence	GPIO_79 BOOT_CONFIG[3]	GPIO_78 BOOT_CONFIG[2]	GPIO_77 BOOT_CONFIG[1]	GPIO_37 FORCED_USB
eMMC@SDC1 → HS USB[1]	Pull low to GND	Pull low to GND	Pull low to GND	Pull low to GND
uSD@SDC2 → eMMC@SDC1	Pull low to GND	Pull low to GND	Pull high to 1.8V during boot sequence	Pull low to GND
eMMC@SDC1[2]	Pull low to GND	Pull high to 1.8V during boot sequence	Pull low to GND	Pull low to GND
HS_USB[3]	Pull low to GND	Pull high to 1.8V during boot sequence	Pull high to 1.8V during boot sequence	Pull low to GND
NAND EBI2[4]	Pull high to 1.8V during boot sequence	Pull low to GND	Pull low to GND	Pull low to GND
FORCED USB BOOT[5]	Don't care	Don't care	Don't care	Pull high to 1.8V during boot sequence

[1] Default Boot option
[2][3][4] Optional boot configurations These boot configurations are not currently supported.
[5] This option is for Intrinsyc Software internal use only.

4.4 Power Output

There are several power output rails exposed on the SOM, as shown in the table below. The current capacity for each power rail is as rated from the PMIC.

Table 5 – Power Output Rails

Board to board connector pin #	Pin Name	Description[a]	Notes[b]
J2000-10	VREG_L12_SDC	LDO linear regulator L12 (50mA). Default voltage = 2.95V	Expected use: µSD card

Board to board connector pin #	Pin Name	Description[a]	Notes[b]
J2000-80	VREG_L6_1P8	LDO linear regulator L6 (150mA). Default voltage = 1.8V	Expected use: Camera, display and transducer 1.8V rails
~~J2001 [77,79]~~ [1]	~~VREG_L1_1P0~~	~~LDO linear regulator L1 (250mA). Default voltage = 1.0V~~	
J2001-[89,91]	VREG_L17_2P85	LDO linear regulator L17 (450mA). Default voltage = 2.85V	Expected use: Display, transducers and camera 2.85V rails
J2001-93	VREG_L6_1P8	LDO voltage switch L6 (150mA). Default voltage = 1.8V	Expected use: Camera, display and transducer 1.8V rails
~~J2001 [97,99]~~[2]	~~VREG_L9_3P3~~	~~LDO voltage switch L9 (600mA). Default voltage = 3.3V~~	
J2001-[2,4]	VREG_L8_2P9	LDO linear regulator L8 (400mA). Default voltage = 2.9V	Expected use: eMMC/ NAND core. SOM uses this rail to for eMMC core
J2001-66	VREG_L5_1P8	LDO linear regulator L5 (200mA). Default voltage = 1.8V	Expected use: Codec and memory 1.8V rails, WLAN IO (SOM uses this rail for WLAN IO)
J2001-80	VREG_L18_2P7	LDO linear regulator L18 (150mA). Default voltage = 2.7V	Expected use: Qualcomm RF360 (SOM uses this rail for GNSS antenna bias)
J2001-[96,98]	VREG_L11_SDC	LDO linear regulator L11 (800mA[3]). Default voltage = 2.95V	Expected use: SD/ MMC card

[1][2] This power rail is no longer supported on the SOM
[3] LDO L11 would be able to provide current of 800 mA to support SDR104 mode. The regulation specification of 3% would not be met. Since minimum voltage needed at SD card is only 2.7 V, the accuracy of 8.4% will be sufficient. The LDO L11 can provide current of 600 mA meeting all regulation specification.
[a] Rated current of the LDOs will be less than the specification due to the wire bond package of the PM8916-1.
[b] Some of the power rails are used within SOM itself.

4.5 SDIO Interface Signals

The SDC2 bus is routed out of the SOM via the board-to-board connectors on the bottom of the SOM. This bus is referenced to VREG_L11_SDC, which defaults to 2.95V. Those SDIO interface signals are listed in the table below.

Table 6 – SDIO Interface Signals

Board to board connector pin #	Pin Name	Description	Notes
J2000-1	SDC2_CLK	SDC2 clock signal. Option to pull high to VREG_L12_SDC via 51K resistor in the Open-Q carrier board.	Used by µSD socket on Open-Q
J2000-[3,5,6,4]	SDC2_DATA_[0..3]	SDC2, 4-bit data bus. Option to pull high to VREG_L12_SDC via 51K resistor in the Open-Q carrier board.	Used by µSD socket on Open-Q
J2000-2	SDC2_CMD	SDC2 CMD signal. Option to pull high to VREG_L12_SDC via 51K resistor in the Open-Q carrier board.	Used by µSD socket on Open-Q

Board to board connector pin #	Pin Name	Description	Notes
J2000-8	SD_CARD_DET_N	SD card detect signal. Pulled high to VREG_L5_1P8 via 1M resistor in the Open-Q carrier board.	Carrier board µSD socket should pull line low when card inserted

4.6 I2C Busses

The table below shows the I2C busses that are available on the SOM. There may be other I2C signals available on other GPIO as alternate functions. Please see the APQ8009W device specification for a full listing of GPIO alternate functions. Note that CCI cannot be used as generic I2C lines. These signals are specifically dedicated for camera operations.

Table 7 – I2C Busses

Board to board connector pin #	Pin Name	Description	Notes
J2000-12	BLSP5_1_TS_I2C_SDA	CPU GPIO18. Requires 2.2K resistor pull-up to VREG_L6_1P8 on the carrier board.	Expected use: Touch screen (Display)
J2000-14	BLSP5_0_TS_I2C_SCL	CPU GPIO19. Requires 2.2K resistor pull-up to VREG_L6_1P8 on the carrier board.	
J2000-40	CCI_I2C_SCL	CPU GPIO30. Requires 2.2K resistor pull-up to VREG_L6_1P8 on the carrier board.	Expected use: Camera (CSI0).
J2000-42	CCI_I2C_SDA	CPU GPIO29. Requires 2.2K resistor pull-up to VREG_L6_1P8 on the carrier board.	
J2000-48	BLSP1_1_SENSOR_I2C_SDA	CPU GPIO6. Requires 2.2K resistor pull-up to VREG_L6_1P8 on the carrier board.	Expected use: Sensors
J2000-50	BLSP1_0_SENSOR_I2C_SCL	CPU GPIO7. Requires 2.2K resistor pull-up to VREG_L6_1P8 on the carrier board.	
J2001-10	BLSP4_0_SMB_I2C_SCL	CPU GPIO15. Requires 2.2K resistor pull-up to VREG_L5_1P8 on the carrier board.	Expected use: SMB charger/ Fuel gauge
J2001-12	BLSP4_1_SMB_I2C_SDA	CPU GPIO14. Requires 2.2K resistor pull-up to VREG_L5_1P8 on the carrier board.	
J2001-26	GPIO_112_BLSP2_BIT0_WCD_SCL	CPU GPIO112. Requires 2.2K resistor pull-up to VREG_L5_1P8 on the carrier board.	Expected use: NFC/ Connectivity connector
J2001-28	GPIO_111_BLSP2_BIT1_WCD_SDA	CPU GPIO111. Requires 2.2K resistor pull-up to VREG_L5_1P8 on the carrier board.	

4.7 BLSP Signals

The table below shows BLSP signals that are available on the SOM.

Table 8 – BLSP Signals

BLSP #	BLSP Bit	CPU GPIO #	BLSP assignment[a] SPI	UART	I2C	Non-BLSP use options[a]	B2B pin #	Pin name
1	3	4	MOSI	**TX**	-	BLSP3 SPI CS3, DMIC0_CLK, General purpose	J2000-46	BLSP1_3_UART_TX[1]
	2	5	MISO	**RX**	-	BLSP2 SPI CS3, DMIC0_DATA, General purpose	J2000-44	BLSP1_2_UART_RX[2]
	1	6	CS_N	CTS_N	**SDA**	General propose	J2000-48	BLSP1_1_SENSOR_I2C_SDA
	0	7	CLK	RFR_N	**SCL**	General propose	J2000-50	BLSP1_0_SENSOR_I2C_SCL
2	3	20	MOSI	TX	-	**General Purpose**	J2001-22	BLSP2_3
	2	21	MISO	RX	-	**General Purpose**	J2001-24	BLSP2_2
	1	111	CS_N	CTS_N	**SDA**	General Purpose	J2001-28	GPIO_111_BLSP2_BIT1_WCD_SDA
	0	112	CLK	RFR_N	**SCL**	General Purpose	J2001-26	GPIO_112_BLSP2_BIT0_WCD_SCL
3	3	29	**MOSI**	-	SDA	General Purpose	J2001-15	BLSP3_3_SENSOR_SPI_MOSI
	2	30	**MISO**	-	SCL	General Purpose	J2001-19	BLSP3_2_SENSOR_SPI_MISO
	1	2	**CS_N**	-	-	General Purpose	J2001-17	BLSP3_1_SENSOR_SPI_CS0_N
	0	3	**CLK**	-	-	General Purpose	J2001-21	BLSP3_0_SENSOR_SPI_CLK
4	3	12	MOSI	-	-	**General Purpose**	J2001-8	BLSP4_3_TS_RESOUT_N
	2	13	MISO	-	-	**General Purpose**	J2001-6	BLSP4_2_TS_INT_N
	1	14	CS_N	-	**SDA**	General Purpose	J2001-12	BLSP4_1_SMB_I2C_SDA
	0	15	CLK	-	**SCL**	General Purpose	J2001-10	BLSP4_0_SMB_I2C_SCL
5	3	16	MOSI	-	-	General Purpose	-	-
	2	17	MISO	-	-	BLSP2 SPI CS2, General Purpose	-	-
	1	18	CS_N	-	**SDA**	General Purpose	J2000-12	BLSP5_1_TS_I2C_SDA
	0	19	CLK	-	**SCL**	General Purpose	J2000-14	BLSP5_0_TS_I2C_SCL

[1][2] The BLSP1 bit 3 and 2 are used for debugging (UART) signals.
[a] SOM software default configuration assignments are in bold text.

4.8 GPIO Signals

The table below shows the GPIO signals that are available on the SOM. Please see the APQ8009W and PM8916-1 device specification documents for a full listing of GPIO alternate functions.

Table 9 – GPIO Signals

B2B connector Pin #	Pin Name[1]	CPU GPIO #	Notes
J2000-12	BLSP5_1_TS_I2C_SDA	18	
J2000-14	BLSP5_0_TS_I2C_SCL	19	
J2000-30	GPIO_35_CAM0_RESET_N	35	
J2000-32	GPIO_34_CAM0_STANDBY_N	34	
J2000-34	GPIO_32_FLASH_NOW	32	
J2000-36	GPIO_31_FLASH_EN	31	
J2000-38	GPIO_33_DSI2HDMI_INT_N	33	
J2000-40	CCI_I2C_SCL	30	
J2000-42	CCI_I2C_SDA	29	
J2000-44	BLSP1_2_UART_RX	5	
J2000-45	GPIO_28_DISPLAY_GP1	28	
J2000-46	BLSP1_3_UART_TX	4	
J2000-47	FORCED_USB_BOOT	37	
J2000-48	BLSP1_1_SENSOR_I2C_SDA	6	
J2000-50	BLSP1_0_SENSOR_I2C_SCL	7	
J2000-52	GPIO_90_KPSNS0	90	
J2000-54	USB_HUB_RESET_N	74	
J2000-56	GPIO_73_WSA_EN2	73	
J2000-58	GPIO_76	76	
J2000-8	SD_CARD_DET_N	38	
J2001-1	GPIO_98_BLSP2_SPI_CS1	98	
J2001-10	BLSP4_0_SMB_I2C_SCL	15	
J2001-11	GPIO_94_ALSPG_INT_N	94	
J2001-12	BLSP4_1_SMB_I2C_SDA	14	
J2001-13	GPIO_97	97	
J2001-14	GPIO_55_TS0_GP2	55	
J2001-15	BLSP3_3_SENSOR_SPI_MOSI	0	
J2001-16	GPIO_53_TS0_GP1	53	
J2001-17	BLSP3_1_SENSOR_SPI_CS0_N	2	
J2001-18	GPIO_54_MAG_DRDY_INT_N	54	
J2001-19	BLSP3_2_SENSOR_SPI_MISO	1	
J2001-21	BLSP3_0_SENSOR_SPI_CLK	3	
J2001-22	BLSP2_3	20	
J2001-23	GPIO_49_DISPLAY_GP2	49	
J2001-24	BLSP2_2	21	
J2001-25	GPIO_99_SMB_VCHG_PA_ON	99	
J2001-26	GPIO_112_BLSP2_BIT0_WCD_SCL	112	
J2001-27	GPIO_65_COMP_INT_N	65	
J2001-28	GPIO_111_BLSP2_BIT1_WCD_SDA	111	
J2001-29	GPIO_56_SMB_INOK	56	
J2001-3	GPIO_95_WCD_INT2	95	
J2001-30	GPIO_58_SMB_STAT	58	
J2001-34	GPIO_78	78	
J2001-36	GPIO_77	77	
J2001-42	GPIO_67_FG_ALARM	67	
J2001-51	GPIO_69_USER_LED2	69	
J2001-53	GPIO_87	87	
J2001-54	GPIO_86	86	
J2001-55	GPIO_79	79	

B2B connector Pin #	Pin Name[1]	CPU GPIO #	Notes
J2001-56	GPIO_71	71	
J2001-57	GPIO_36_ACC1_INT2_N	36	
J2001-58	GPIO_68_USER_LED1	68	
J2001-59	GPIO_72_WSA_EN1	72	
J2001-6	BLSP4_2_TS_INT_N	13	
J2001-63	GPIO_83_GYRO_INT_N	83	
J2001-64	GPIO_66_FG_CHARGE_EN	66	
J2001-65	CAM_MCLK0	26	
J2001-67	GPIO_91_KPSNS1	91	
J2001-69	GPIO_92	92	
J2001-7	GPIO_110_DSI_SW_SEL	110	
J2001-71	OLED_RST_N	25	
J2001-73	OLED_TE	24	
J2001-8	BLSP4_3_TS_RESOUT_N	12	
J2001-83	GPIO_70	70	
J2001-87	GPIO_84	84	
J2001-9	GPIO_96_ACC1_INT1_N	96	
		PMIC GPIO/MPP #	
J2001-78	PMIC_GPIO_2	PMIC GPIO 2	
J2001-90	PMIC_MPP_2	PMIC MPP 2	
J2001-92	PMIC_MPP_3	PMIC MPP 3	
J2001-88	WCD_ELDO_EN_PMGPIO4	PMIC GPIO 4	
J2001-74	WLED_PWM_MPP_4	PMIC MPP 4	
[1] GPIO pins can support multiple functions. To assign GPIOs to particular functions, designers must identify all their application's requirements and map each GPIO to its function- carefully avoiding conflicts in GPIO assignments.			

4.9 Audio Input/ Output Interface

The signals contained in this section are used for audio outputs or inputs. All signals originate or travel to the PMIC (PM8916-1) audio codec on the SOM unless specified. Please refer to the PM8916-1 device specifications for more detail.

Table 10 – PMIC Audio Interface Signals

Board to Board Pin #	Pin Name	Description	Notes
J2000-98	VDD_EAR_SPKR	Earphone and class-D speaker amplifier input supply.	Software configurable voltage 5V or VPH_PWR.
J2000-81	SPKR_OUT_P	Class-D loudspeaker + output	
J2000-83	SPKR_OUT_N	Class-D loudspeaker - output	
J2000-90	CDC_MIC_BIAS2	Analog mic-2 bias output[1]	
J2000-92	CDC_MIC_BIAS1	Analog mic-1 bias output[2]	
J2000-91	CDC_MIC3_P	Analog mic-3 input (second mic)	
J2000-89	CDC_MIC1_P	Analog mic-1 input (main mic)	
J2000-85	CDC_HS_DET	Headset detection input	
J2000-97	CDC_HPH_REF	Headphone GND sensing	
J2000-95	CDC_HPH_R	Headphone Right Audio Signal	
J2000-99	CDC_HPH_L	Headphone Left Audio Signal	
J2000-93	CDC_HDS_MIC2_P	Analog mic-2 input (headset mic)	

Board to Board Pin #	Pin Name	Description	Notes
J2000-94	CDC_GND_CFILT	Ground reference for PMIC bias	
J2001-100	FM_HEADSET	FM antenna connection	
[1][2] Microphone bias voltage 1.6V ~ 2.85V at 3mA microphone load			

4.9.1 Analog Microphone Inputs

Qualcomm's PMIC8916-1 audio supports three single ended microphone inputs. The Figure 6 below shows an example of an analog ECM type microphone connected to the PMIC mic input. Note that external 2.2K pull-up resistor is optional and it is recommended to use internal MIC_BIAS 2.2K pull-up (not shown in the figure). It is not recommended to use an external capacitor on the MIC_BIAS line with ECM-type microphone inputs. When using MEMS-type of the microphone, it is recommended to use MIC_BIAS with external 0.1uF capacitors as shown in Figure 7. Any filter capacitors and protection diodes should be placed close to the off-board connector or microphone lines.

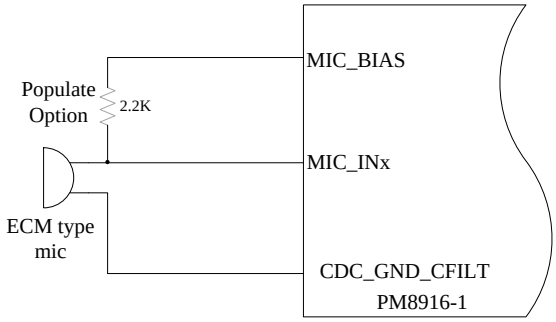


Figure 6 – Analog microphone (ECM type) connected in a single ended configuration

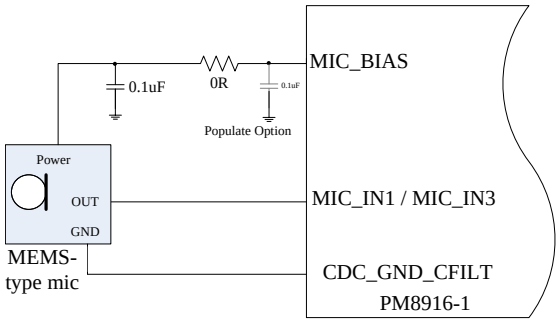


Figure 7 – Analog microphone (MEMS type) connected in a single-ended configuration

4.10 LED Signals

The table below shows the LED signals that are available on the SOM.

Table 11 – LED Signals

B2B connector pin #	Pin Name	Description	Notes
J2000-82	CHG_LED_SINK	PM8916-1 charging indication LED driver output (5mA sink current rated)	This pin cannot be used to drive LED if linear battery charging is not used (OPT_1 is grounded)
J2001-90	PMIC_MPP_2	PM8916-1 Home row LED drive (40mA sink current per MPP)	
J2001-74	WLED_PWM_MPP_4	PMI8996-1 WLED PWM LED output	

4.11 MIPI Display Interface (DSI)

The signals shown in the table below, describe those used for the MIPI display interface that is available on the SOM. When connecting to MIPI differential pair signals, the designer should be aware of the impedance and trace length matching requirements that are necessary for these high-speed signals. Please reference the MIPI standard for additional details.

Table 12 – MIPI Display Interface Group

B2B connector pin #	Pin Name	Description	Notes
J2000-[18,20]	MIPI_DSI0_CLK_N/P	MIPI DSI clock differential pair	
J2000-[21,23]	MIPI_DSI0_LANE0_P/N	MIPI DSI data lane differential pair	
J2000-[24,26]	MIPI_DSI0_LANE1_N/P	MIPI DSI data lane differential pair	
J2000-[15,17]	MIPI_DSI0_LANE2_P/N	MIPI DSI data lane differential pair	
J2000-[9,11]	MIPI_DSI0_LANE3_P/N	MIPI DSI data lane differential pair	
J2000-47	FORCED_USB_BOOT	Backlight Enable	
J2001-71	OLED_RST_N	DSI display reset	

4.12 MIPI Camera Interface (CSI)

The signals shown in the table below, describe those used for the MIPI camera interface that is available on the SOM. When connecting to MIPI differential pair signals, the designer should be aware of the impedance and trace length matching requirements that are necessary for these high-speed signals. Please reference the MIPI standard for additional details.

Table 13 – MIPI Camera Interface Group

B2B connector pin #	Pin Name	Description	Notes
J2000-[33,35]	MIPI_CSI0_CLK_N/P	MIPI CSI clock differential pair	
J2000-[39,41]	MIPI_CSI0_LANE0_N/P	MIPI CSI data lane differential pair	
J2000-[27,29]	MIPI_CSI0_LANE1_P/N	MIPI CSI data lane differential pair	
J2001-65	GPIO_26_CAM_MCLK0	Camera master clock 0	
J2000-36	GPIO_31_FLASH_EN	Camera control interface timer 0	
J2000-30	GPIO_35_CAM0_RESET_N	Camera reset	
J2000-32	GPIO_34_CAM0_STANDBY_N	Camera standby	
J2000-34	GPIO_32_FLASH_NOW	Camera control interface timer 1	

4.13 USB Interface Signals

The table below shows the USB 2.0 signals that are available on the SOM. When connecting to USB differential pair signals, the designer should be aware of the impedance and trace length matching requirements that are necessary for these high-speed signals. Please reference the USB 2.0 standard for additional details.

Table 14 – USB Interface Signals

B2B Conn Pin #	Pin Name	Description	Notes
J2001-[31,33]	USB2_HS_D_N/P	USB port high-speed differential pair	
J2000-[67,69,71,73,75,77]	USB2_VBUS	PM8916-1 USB charger input source.	
J2001-32	USB2_HS_ID	USB port ID signal	

4.14 RF Antenna Connections

The Open-Q™ 2100 SOM has single band WCN3620 Wi-Fi/BT chipset and WGR7640 GNSS receiver. The SOM contains two U.FL coaxial receptacles (Hirose U.FL-R-SMT-1 (10)) for connecting to GNSS, and WLAN/ BT RF antennas as shown in the figure below. Please refer corresponding datasheet for detailed specifications.

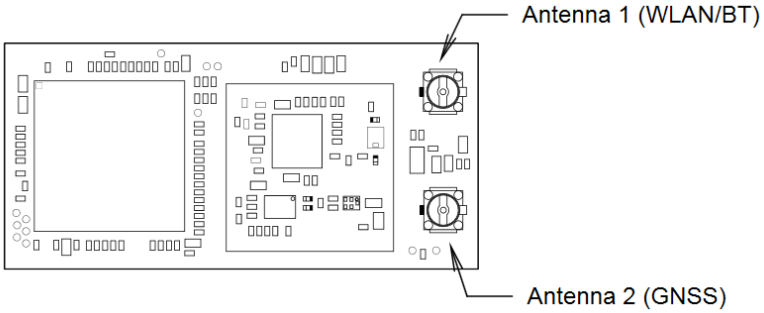


Figure 8 – Physical location of Antenna 1 and Antenna 2 on SOM

Table 15 – RF Signals via U.FL Coaxial Receptacles

Antenna	Description	Notes
Antenna 1	RF signal interface with Qualcomm WCN3620 Wi-Fi/BT chipset	Antenna1 is for WLAN/BT. Use a single band (2.4 GHz) antenna
Antenna 2	RF signal interface with Qualcomm WGR7640	Connect to external GNSS antenna via coax cable. The SOM provides a 2.7V output on the U.FL connector. Therefore, it is recommended that an active GNSS antenna is used.

4.15 Miscellaneous Signals

The table below shows some miscellaneous signals that are available on the SOM via board to board connectors. These signals support different functionalities on the SOM. Please refer to their designated data sheets for more details regarding how these signals are used.

Table 16 – Miscellaneous Signals

B2B Conn Pin #	Pin Name	Description	Notes
J2001-76	BBCLK2	Baseband(low power) 19.2MHz XO output 2	
J2001-84	OPT_1	Option hardware configuration control bit 1	See Table 17 for valid configuration options.
J2001-86	OPT_2	Option hardware configuration control bit 1	
J2001-5	PON_RESET_N	Power-on reset output control connected to CPU	Please place a 10nF/10V capacitor close to the SOM.
J2001-40	APQ_RESOUT_N	CPU reset output	See section 4.3 for usage.
J2001-68	PHONE_ON_N	Keypad power-on detect input	
J2001-70	CBLPWR_N	Cable power-on detect input	Internal pull-up to VDD. Initiates power-on when grounded.
J2001-72	PMIC_RESIN_N	Active low reset input. Also, serves as a volume down (-) button.	

Table 17 – Hardware option configurations

B2B Conn Pin #	Pin Name	Pin logic	Description
J2001-84	OPT_1	Hi-Z	Internal charger is used
		GND	External charger is used
J2001-86	OPT_2	Hi-Z	No vibrator operation during pre-power-on
		GND	One-time vibration for 100ms during pre-power-on

5. ELECTRICAL SPECIFICATIONS

5.1 Absolute Maximum Ratings

The input power to the SOM is provided by a power supply (battery or wall adapter) and also a USB source, for battery charging purposes. All input power sources enter the PM8916-1, which then distributes power via LDOs and switching power supplies. Since these input sources are susceptible to external factors, the table below shows the absolute maximum ratings in which PM8916-1 can be exposed to without experiencing functional failure.

Table 18 – Absolute Maximum Input Power Ratings

Parameter	Min	Max	Units
Battery or DC power input (VPH_PWR / VBAT_SNS)	-0.5	+6	V
5V USB VBUS battery charger input voltage source (USB2_VBUS)	-0.5	+16	V
Earphone and class-D speaker amplifier supply (VDD_EAR_SPKR)	-0.5	+6	V

5.2 Operating Conditions

According to component datasheet values, the operating conditions outline the parameters in which a user can control the behavior of the SOM. If used within the following conditions as outlined in Table 19 and Table 20 below, the SOM will meet all performance specifications listed in section 7, unless otherwise noted (provided the absolute maximum ratings have never been exceeded).

Table 19 – Operating power input conditions

Parameter	Min	Typ.	Max	Units
Battery or DC power input (VPH_PWR)	+3.5	+3.7	+4.2	V
5V USB VBUS battery charger input voltage source (USB2_VBUS)	+3.7	+5	+9	V
Earphone and class-D speaker amplifier supply (VDD_EAR_SPKR)	VPH_PWR	VPH_PWR	+5	V

The DC electrical characteristics for the SOM voltage output rails are listed in section 4.5 above.

5.3 Operating Temperature

The SOM operating temperature ratings listed below are based only on the operating temperature grade of the SOM components. Users should consider the specific environmental conditions in which the final product is used in.

Table 20 – Operating temperature conditions

Parameter	Min	Typ.	Max	Units
Overall SOM	-25	+25	+85	°C

Note: If the user is using SOM in extreme environmental conditions, care must be taken from exposing the Wi-Fi/ BT module from exceeding these ratings.

6. POWER CONSUMPTION

Power consumption tests have been done on the SOM under common operational modes. These results are outlined in the table below. All tests were executed at room temperature with Android 7.0 running with the Open-Q 2100 carrier board. Since measurements were taken on the VPH_PWR rail, the power consumed reflects what the SOM consumes during the given scenario.

Table 21 – Power consumptions

Operational Modes	Description	Power
Suspend (Wi-Fi Off)	Power consumption when system placed in standby (Wi-Fi Off)	TBD
Suspend (Wi-Fi On)	Power consumption when system placed in standby (Wi-Fi On)	TBD
Video Record (TBD)	Power consumption when system recording TBD video	TBD
Video Playback (TBD)	Power consumption when system playing back TBD video	TBD
Audio Playback	Power consumption when system playing back MP3[1]	TBD
Wi-Fi Download	Power consumption when system downloading large file via Wi-Fi	TBD
Wi-Fi Upload	Power consumption when system uploading large file via Wi-Fi	TBD
Quad Core	Power consumption when system is running all 4 cores at 100%	TBD
Single core	Power consumption when system is running only 1 core at 100% (others off/ suspend)	TBD

Note: The results above are averages of the power consumed over 30 minutes (may vary depending on test case).

[1] LCD screen has been turned off for this use case