

# Open-Q™ 2100 Development Kit based on the Snapdragon™ 2100 (APQ8009W) Processor User Guide

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## IDENTIFICATION

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# 1. INTRODUCTION

## 1.1 Purpose

The purpose of this user guide is to provide primary technical information on the Open-Q™ 2100 Development Kit based on the Snapdragon™ 2100 (APQ8009W) Processor.

For more background information on this development kit, visit: [www.intrinsyc.com](http://www.intrinsyc.com)

## 1.2 Scope

This document will cover the following items on the Open-Q 2100 Development Kit:

- Block Diagram and Overview
- Hardware Features
- Configuration
- SOM
- Carrier Board
- Display Board for LCD (Optional)

## 1.3 Intended Audience

This document is intended for users who would like to develop custom applications on the Open-Q 2100 Development Kit.

## 2. DOCUMENTS

This section lists the supplementary documents for the Open-Q 2100 Development Kit.

### 2.1 Applicable Documents

REFERENCE	TITLE
A-1	Intrinsyc Purchase and Software License Agreement for the Open-Q Development Kit

### 2.2 Reference Documents

REFERENCE	TITLE
R-1	Hardware Document Set for the Snapdragon APQ8009W based Open-Q Development Kit
R-2	Open-Q 2100 Schematics (SOM, Carrier)

### 2.3 Terms and Acronyms

Term and acronyms	Definition
AMIC	Analog Microphone
ANC	Audio Noise Cancellation
B2B	Board to Board
BLSP	Bus access manager Low Speed Peripheral (Serial interfaces like UART / SPI / I2C/ UIM)
BT LE	Bluetooth Low Energy
CSI	Camera Serial Interface
DSI	MIPI Display Serial Interface
EEPROM	Electrically Erasable Programmable Read only memory
eMMC	Embedded Multimedia Card
FCC	US Federal Communications Commission
FWVGA	Full Wide Video Graphics Array
GPS	Global Positioning system
HDMI	High Definition Media Interface
HSIC	High Speed Inter Connect Bus
JTAG	Joint Test Action Group
LNA	Low Noise Amplifier
MIPI	Mobile Industry processor interface
MPP	Multi-Purpose Pin
NFC	Near Field Communication

RF	Radio Frequency
SATA	Serial ATA
SLIMBUS	Serial Low-power Inter-chip Media Bus
SOM	System On Module
SPMI	System Power Management Interface (Qualcomm® PMIC / baseband proprietary protocol)
SSBI	Single wire serial bus interface (Qualcomm® proprietary mostly PMIC / Companion chip and baseband processor protocol)
UART	Universal Asynchronous Receiver Transmitter
UIM	User Identity module
USB	Universal Serial Bus
USB HS	USB High Speed

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## **3. OPEN-Q 2100 DEVELOPMENT KIT**

### **3.1 Introduction**

The Open-Q 2100 Development Kit provides a reference platform for Qualcomm's latest 2100 series - Snapdragon 2100 processor. This kit is suited for Android / Linux application developers, OEMs, consumer manufacturers, hardware component vendors, video surveillance, robotics, camera vendors, and flash chip vendors to evaluate, optimize, test and deploy applications that can utilize the Qualcomm® Snapdragon 2100 series technology.

### **3.2 Development Platform Notice**

This development platform contains RF/digital hardware and software intended for engineering development, engineering evaluation, or demonstration purposes only and is meant for use in a controlled environment. This device is not being placed on the market, leased or sold for use in a residential environment or for use by the general public as an end user device.

This development platform is not intended to meet the requirements of a commercially available consumer device including those requirements specified in the European Union directives applicable for Radio devices being placed on the market, FCC equipment authorization rules or other regulations pertaining to consumer devices being placed on the market for use by the general public.

This development platform may only be used in a controlled user environment where operators have obtained the necessary regulatory approvals for experimentation using a radio device and have appropriate technical training. The device may not be used by members of the general population or other individuals that have not been instructed on methods for conducting controlled experiments and taking necessary precautions for preventing harmful interference and minimizing RF exposure risks. Additional RF exposure information can be found on the FCC website at <http://www.fcc.gov/oet/rfsafety/>

### **3.3 Anti-Static Handling Procedures**

The Open-Q 2100 Development Kit has exposed electronics and chipsets. Proper anti-static precautions should be employed when handling the kit, including but not limited to:

- Using a grounded anti-static mat
- Using a grounded wrist or foot strap.

### **3.4 Kit Contents**

The Open-Q 2100 Development Kit includes the following:

- Open-Q 2100 SOM with the Snapdragon 2100 (APQ8009W) processor, memory, power management, and WiFi/BT components
- nano-ITX form-factor carrier board
- AC power adapter and HDMI cable

- 4.5" FWVGA (480x854) 16.7 M LCD (Optional Accessory)



**Figure 1 Open-Q 2100 Development Kit**

The development kit comes with Android for Wearables 7.1.1 software pre-programmed on the CPU board (SOM). Please contact Intrinsyc for availability of camera modules, sensor boards, and other accessories: [sales@intrinsyc.com](mailto:sales@intrinsyc.com)

### 3.5 Hardware Identification Label

Labels are present on the CPU board and the nano-ITX form-factor carrier board. The following information is conveyed on these two boards:

CPU board (SOM):

- Serial Number
- WiFi MAC address

Refer to <http://support.intrinsyc.com/account/serialnumber> for more details about locating the serial number, as this will be needed to register the development kit. To register a development kit, please visit: <http://support.intrinsyc.com/account/register>

**Note:** Please retain the SOM and carrier board serial number for warranty purposes.

## 3.6 Getting Started

The instruction in this section explains how to setup the Open-Q 2100 Development Kit.

### 3.6.1 Default DIP switch settings

The DIP switch S3400 and S1700 is by default set to **OFF** positions. This setting corresponds to HDMI display selected, SMB charger enabled, USB forced boot disabled and eMMC boot option selected. See section [3.9.1](#) and [3.9.2](#) for other DIP switch settings. Cable connections and DIP switch positions are shown in figure below:

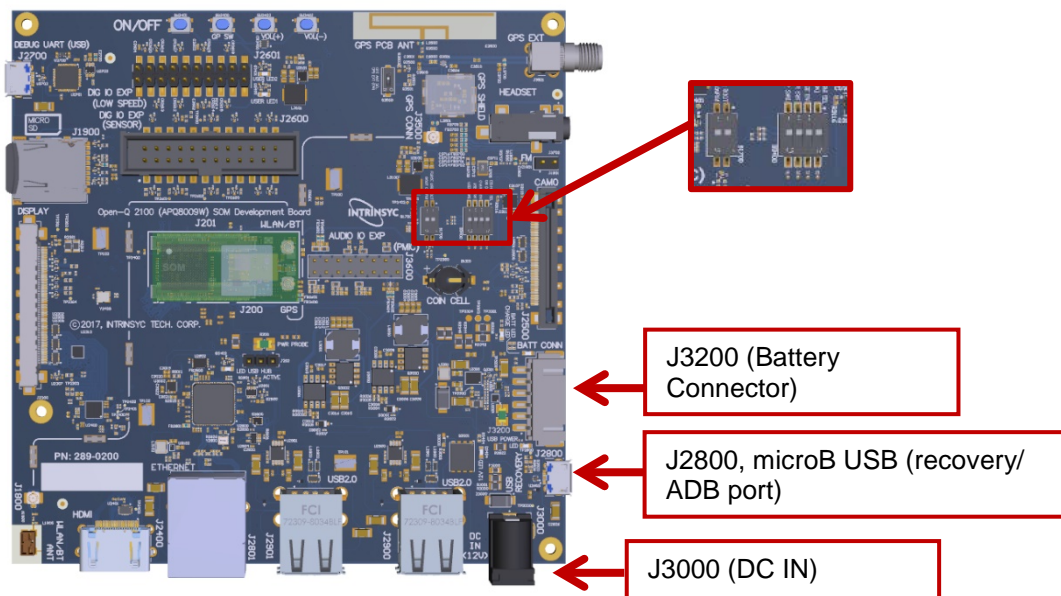


Figure 2 Cable connection and DIP switches on the Open-Q 2100 Dev kit

### 3.6.2 Powering up the Open-Q 2100 Development Kit

To power-up the board, perform the following steps below:

1. At a static-safe workstation, remove the development kit board carefully from the anti-static bag.
2. Connect the HDMI output from the development kit to a display.
3. Connect the Power Adapter to the 12V DC Jack and then press and hold the power button until you see the Intrinsic logo appear on the display (~3 seconds).
4. Plug in a USB mouse to navigate the UI on the HDMI display.
5. If connecting the "Recovery USB" port to a PC for ADB access, make sure to connect this only after the 12V power adapter is connected. Also note that when using the Recovery USB port, the host USB ports and Ethernet port are disabled.

#### WARNING!

The above steps should be followed in exact sequence when battery is not connected to the Dev Kit. Failing to do so prevents system from booting. If a battery is not connected, the user has to always plug in the 12V power source before the USB ADB cable is plugged in.

### 3.7 System Block Diagram

The Open-Q 2100 SOM development platform consists of three major components

- Open-Q 2100 SOM
- Carrier board for I/O and connecting with external peripherals
- Display Adapter Board (optional accessory)

The following diagram explains the interconnectivity and peripherals on the development kit.

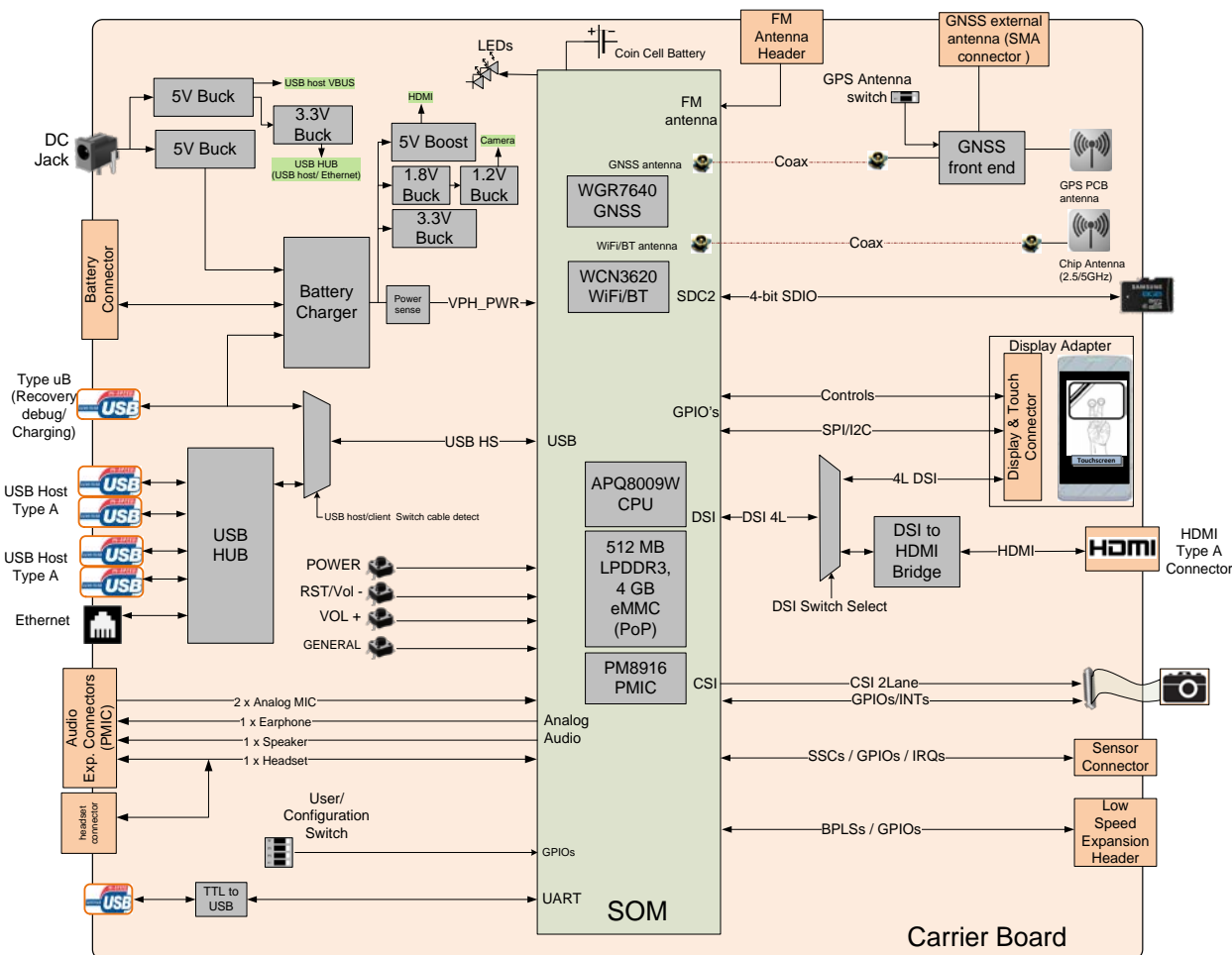


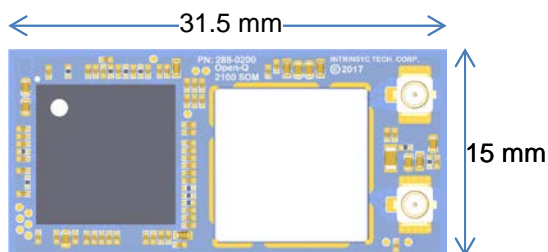
Figure 3 Open-Q 2100 SOM + Carrier Board Block Diagram

### 3.8 Open-Q 2100 SOM

The SOM provides the basic common set of features with minimal integration efforts for end users. It contains the following:

- Snapdragon™ 2100 Series (APQ8009W) main application processor
- LPDDR3 up to 533MHz 512MB RAM (POP)

- 4GB eMMC flash memory (POP)
- PM8916-1 – PMIC for Peripheral LDOs, Boost Regulators
- WCN3620 Wi-Fi + BT combo chip
- GNSS Receiver (GPS, GLONASS, COMPASS)



**Figure 4 Open-Q 2100 SOM**

### 3.8.1 SOM Mechanical Properties

**Table 3.8-1 Open-Q 2100 SOM Hardware Features**

<b>Dimension</b>	31.5 mm x 15 mm
<b>Interface</b>	2 x 100-pin Hirose DF40 connectors (B2B Connector)
<b>Shielding</b>	A top side shield can for the Wi-Fi/GPS RF section is installed by default.

### 3.8.2 SOM Block Diagram

The Open-Q 2100 SOM measuring 31.5mm x 15mm is where all the processing occurs. It is connected to the carrier board via two 100 pin Hirose DF40 connectors. The purpose of these connectors is to bring out essential signals such that other peripherals can be connected to the platform.

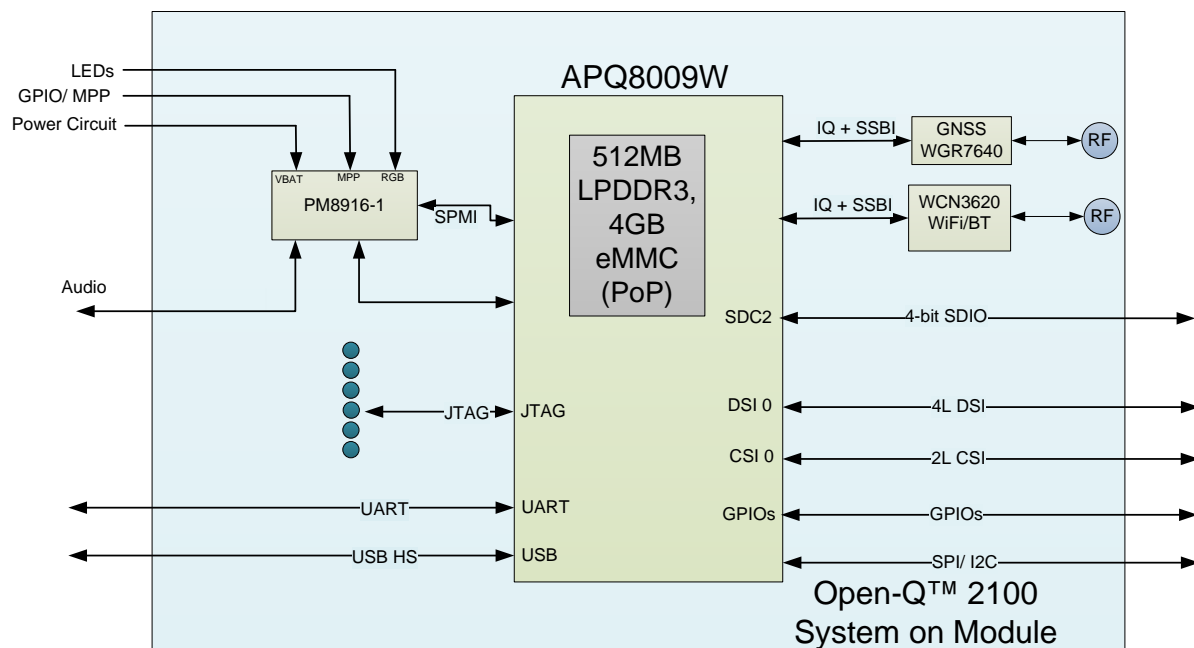


Figure 5 SOM Block Diagram

### 3.8.3 Hardware Specification

The Open-Q 2100 SOM platform encompasses the following hardware features:

Table 3.8-2 Open-Q 2100 SOM Hardware Features

Subsystem / Connectors	Feature Set	Description	Specification
Chipset	APQ8009W	Qualcomm® Snapdragon™ 2100 Processor	ARM Cortex-A7 CPU, quad core, 32-bit up to 1.09GHz
	PMIC (PM8916-1)	Qualcomm® PMIC, Companion PMIC for APQ8009W processor	NA
Memory	512MB LPDDR3, 4GB eMMC	Memory POP	Up to 533MHz LPDDR3 POP on CPU BGA chip. Supports via 4x32bit channels
Connectivity	Wi-Fi 2.4 GHz via WCN3620	Wi-Fi Qualcomm WCN3620 Wi-Fi + BT Combo Chip	802.11a/b/g/n 2.4 GHz via WCN3620. Full 1x1 antenna configuration
	BT 2.4 GHz via WCN3620	WCN3620 Wi-Fi + BT Combo Chip	Support BT 4.0
	GNSS via WGR7640 – SSBI Qualcomm® Proprietary Protocol	GNS Receiver Frontend	GPS, GLONASS, COMPASS

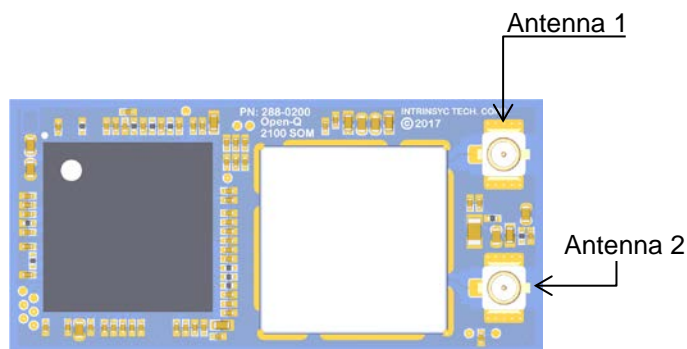


Subsystem / Connectors	Feature Set	Description	Specification
RF Interfaces	1xWLAN / BT U.FL antenna connector	Connect to antenna on carrier board via coax cable	2.4 GHz WLAN antenna
	1x GPS	Connect to external antenna	GPS/GLONASS/COMPASS passive or active antenna
Interfaces	1 x MIPI CSI	Connect to camera Connectors CSI0	MIPI Alliance Specification v1.0
	1 x USB HS	Connect to 2 x dual stack type A USB2.0 via USB line, 1 x micro USB B 2.0 via switch (from USB line)	USB2.0
	1 x MIPI DSI	Connect to 51- pin display connector. Interfaces with Intrinsic Display Adapter Board	MIPI Alliance Specification v1.01, MIPI D-PHY Specification v0.65, v0.81, v0.90, v1.01
Connector	2 x board to board connector	Connectors to interface with carrier board	Hirose DF40C series 100pin connector

### 3.8.4 SOM RF Specification for WIFI, BT, GNSS

The SOM includes the following radio interfaces:

- Wi-Fi + BT: Antenna 1
- GNSS: Antenna 2



**Figure 6 Open-Q 2100 SOM Antenna locations**

**Antenna 1:** Antenna 1 is used for providing Wi-Fi and Bluetooth connectivity to WCN3620. This antenna is meant to be connected to the carrier board via a coaxial cable or to an external antenna. The WCN3620 requires an antenna to be connected here for correct operation.

For details on connecting the Wi-Fi module to the on-board PCB antennas on the carrier board, refer to section 3.9.11 below.



**Antenna 2:** Antenna 2 is for the GNSS receiver. This antenna is meant to be connected to the carrier board via a coaxial cable or to an external antenna. The carrier board includes a GNSS PCB antenna and option to use an external GNSS antenna via SMA connector. A passive or an active antenna may be used and a 2.7V bias is provided on the antenna input for powering an active antenna.

The operating frequencies for WGR7640 are:

GPS: 1574.42 MHz – 1576.42 MHz

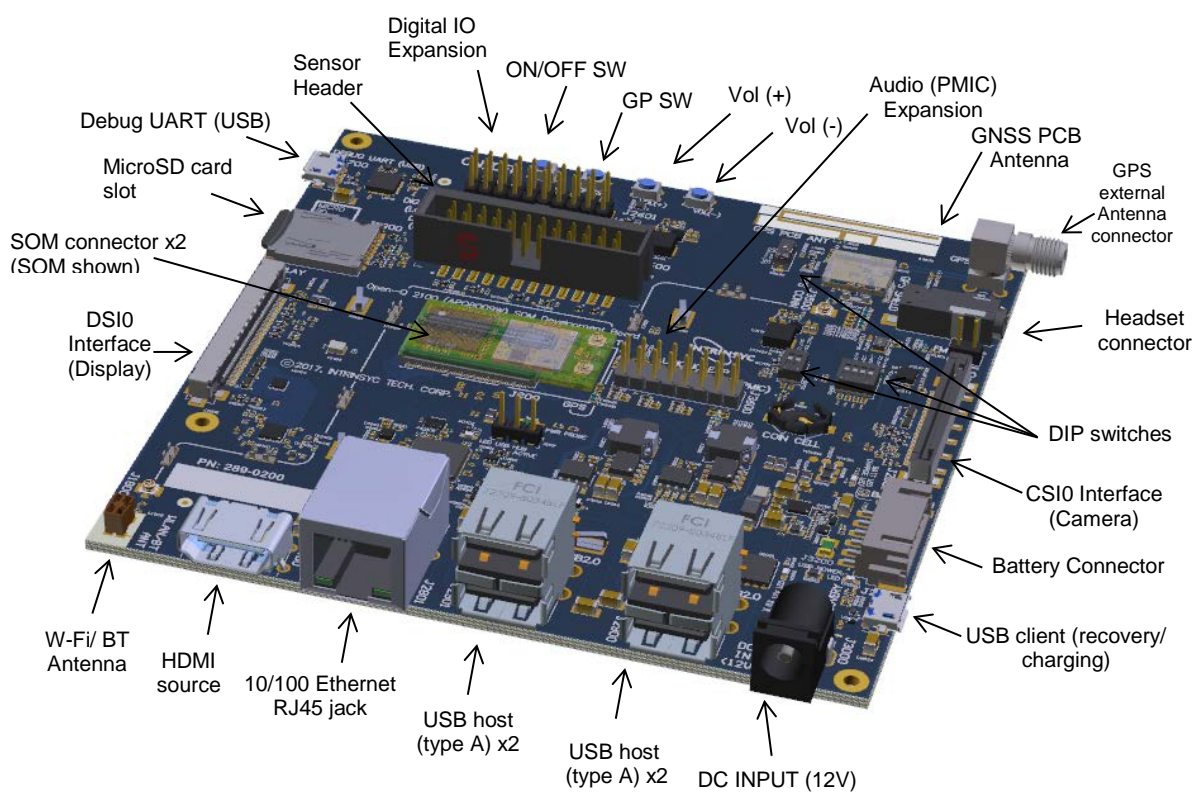
GLONASS: 1598 MHz to 1606 MHz

### 3.9 Open-Q 2100 SOM Carrier Board

The Open-Q 2100 SOM Carrier board is a nano-ITX form factor board with various connectors used for connecting different peripherals. The following are the mechanical properties of the carrier board:

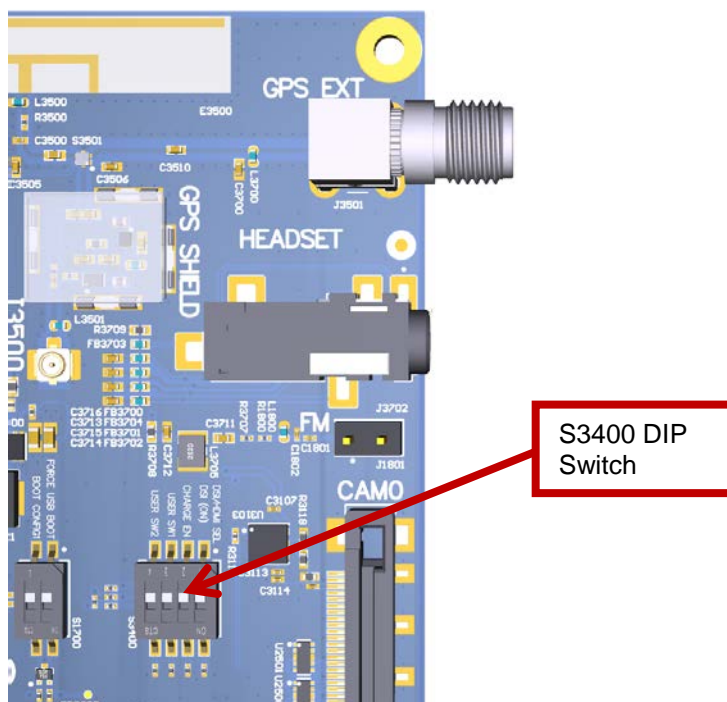
**Table 3.9-1 Open-Q 2100 SOM Carrier Board Mechanical Properties**

Dimensions	120mm x 120mm
Form Factor	nano-ITX
Major Interfaces	SOM: 2 x 100-pin Hirose DF40 connectors (B2B Connector) Display: 51 pin JAE (JF08 series) connector Camera: 41 pin JAE (JF08 series) connector  See <a href="#">section 3.9.3</a> for details regarding carrier board interfaces



**Figure 7 Open-Q 2100 Carrier Board**

### 3.9.1 Dip switch S3400 Configuration Options



**Figure 8 S3400 DIP switch**

There is a DIP switch S3400 on the top side of the Open-Q 2100 SOM carrier board. The 4-bit switch allows the user to control the system configuration. Table 3.9-2 below outlines the pin outs and connections of this DIP switches.

**Table 3.9-2 Dip Switch HW / SW configuration**

Function	DIP Switch	Description	Notes
DSI/HDMI SELECT	S3400-1	Toggles between DSI output and HDMI output mode. Enables DSI output when DIP switch is turned ON	Default out of the box configuration is OFF which is the HDMI output mode
CHARGE EN	S3400-2	Enables battery charging	Default out of the box configuration is OFF
USER SW1	S3400-3	User configurable general-purpose switch	Default out of the box configuration is OFF
USER SW2	S3400-4	User configurable general-purpose switch	Default out of the box configuration is OFF



### 3.9.3 Carrier Board Expansion Connectors

The following table lists the connectors, expansions and their usages on the carrier board:

**Table 3.9-4 Carrier Board Expansion Options and Usage**

Domain	Description	Specification	Usage
Power	DC / Barrel charger	12 V DC Power Supply 3 A	Power Supply
	Battery Connector	6 pin header	For Battery operation and charging development
Debug Serial via USB	Debug Serial UART console over USB for development	USB Micro B connector	Development Serial Connector for debug output via USB
Buttons	General Purpose SW button	SMD Button	Additional button for general purpose (connected to APQ_GPIO87)
	Power Button	SMD Button	Power Button for Suspend / Resume and Power off
Volume Keys	Volume + key	SMD Button	Volume +Key
	Volume – key	SMD Button	Volume –/ RESET Key
Sensor IO Connector	24 pin Sensor Expansion Connectors	Support any user sensor card, Standard 24-pin ST Micro PLCC support via optional daughter card	Available via Intrinsyc optional accessories kit
Digital IO / Low speed Expansion header	20-pin general purpose IO for SPI / I2C / GPIOs/ UART functions and other unused GPIOs from PMIC and APQ	Full BLSP2 (SPI/ UART/ I2C/ GPIO) APQ GPIOs MPPs Power	Useful when user wants to use UART GPIOs pins as BLSP other functions (GPIO/ I2C/ SPI).
Micro SD	Micro SD card	4bit Micro SD card support	External Storage
3-Analog Microphone via audio input expansion header	Audio expansion Supported using PM8916-1	Analog Audio header	For Analog audio input for Analog MIC (differential signal)
1-Loud Speaker via audio output expansion header	Audio expansion Supported using PM8916-1	Analog Audio header	For loud speaker output after signal has been processed
1-Earpiece, 1- headset via audio output expansion header	Audio expansion Supported using PM8916-1	Analog Audio header	For earpiece/ headset output after signal has been processed

Domain	Description	Specification	Usage
HDMI Port	Extended Display ports	HDMI port supports up to 720p at 60Hz	External Display
USB Expansion connector	4 USB2.0 ports via USB-HS through USB switch and Hub	2x Dual Type A connector	Host mode transfer data to and from CPU
USB Recovery	USB 2.0 via USB-HS through USB switch	Micro B connector	USB recovery/ debug with battery charging support
Ethernet	10/100 Ethernet MAC with full-duplex support via USB hub controller	RJ45 Ethernet connector	Supports 10/100 full-duplex Ethernet connection
WLAN Antenna	1X PCB mount Antenna	2.4 – 5.1 GHz	Antenna to SOM Wi-Fi module
Coin Cell Holder	Coin Cell battery (Optional via stuffing)	Coin cell battery for PMIC RTC	RTC
LED	7xLED	2x ORANGE 1x GREEN 1x ORANGE 3x GREEN	User configurable USB hub active Charge indicator 12V DC IN indicator VBATT indicator USB VBUS IN indicator
LCD Display and Touch connector	51 pin for LCD signals via board to cable connector to display adapter board	4-lane MIPI DSI0 I2C/ /GPIO Backlight MIPI Alliance Specification v1.01 MIPI D-PHY Specification v0.65,v0.81, v0.90, v1.01	To interface with optional DSI LCD panel with touch screen
CSI Camera connectors	1 x CSI port connector with CLK, GPIOs, CCI	Supports 1 x Camera interfaces via 41 pin board to cable connector <ul style="list-style-type: none"> <li>1 x 2 Lane MIPI-CSI</li> <li>MIPI Alliance Specification v1.00 for Camera Serial Interface</li> </ul>	Camera maximum resolution 8MP
FM Antenna Connector	2 pin header	Dedicated FM antenna connection to PM8916-1	For connecting an external FM antenna

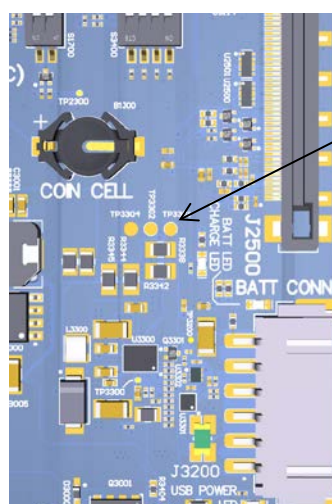
The sections below will provide detailed information on each expansion header and connector on the carrier board. The information listed below is of particular use for those who want to interface other external hardware devices with the Open-Q 2100 SOM. Before connecting anything to the development kit, please ensure the device meets the specific hardware requirements of the processor.

### 3.9.4 DC Power Input J3000

The Open-Q 2100 Development Kit power source connects to the 12V DC power supply jack J3000. Starting from the power jack, the 12V power supply branches off into different voltage rails via step down converters on the carrier board and PMIC on the SOM. The SOM is powered by 3.7V via a Qualcomm battery charger U3300 on the carrier board. To ensure the SOM is getting powered correctly, the user can monitor the voltage going into the SOM via test point TP3301.



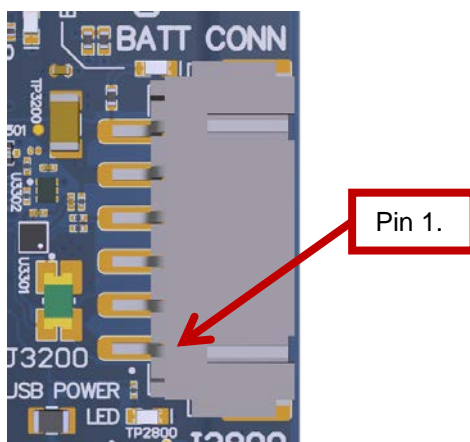
Figure 10 J3000 12V DC Power Jack



Measure voltage going  
into the SOM

Figure 11 TP3301 to measure VPH\_PWR

### 3.9.5 Battery Header J3200



**Figure 12 J3200 Battery Header**

The Open-Q 2100 Development Kit platform can also power the SOM with a single cell Lithium-Ion Polymer (LiPo) battery pack which connects to header J3200. The purpose of this header is to be used by the end user to develop a battery charging solution, including battery characterization. Intrinsyc recommends using the AA Portable Power Corp's CU-J479-V2 / 1ICP7/55/85 Lithium ion battery pack. This is a single cell pack with a nominal voltage of 3.7V and a capacity of 3200mAh (11.8 Wh, 5A rate). If user intends to use a different battery, please note the pin outs on this battery header.

**Table 3.9-5 Battery Connector Header J3200 Pin out**

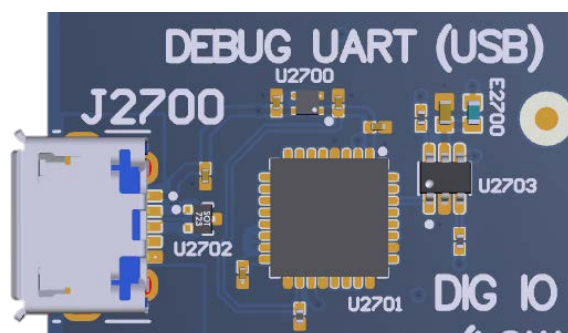
Description	Signal	Pin	Note
SOM Battery negative supply terminal	VBAT Minus(VBAT-)	J3200[1]	
SOM Battery positive supply terminal	VBAT Minus(VBAT-)	J3200[2]	
Internal battery pack temperature	BATT_THERM (The recommended battery has a 10K Ohm thermistor)	J3200[3]	
BATT ID	BATT ID terminal to detect presence of the battery	J3200[4]	Optionally: Depopulate R3201 if selected battery has a 10K ohm battery ID resistor
SOM Battery positive supply terminal	VBAT Plus (VBAT+)	J3200[5]	
SOM Battery positive supply terminal	VBAT Plus(VBAT+)	J3200[6]	

Note that when the dev kit is powered from the battery only, the following carrier board features are non-function – the USB host ports, Ethernet port.

When a battery is not in use, the SMB1357 battery charger U3300 supplies power from the 12V input to the SOM.



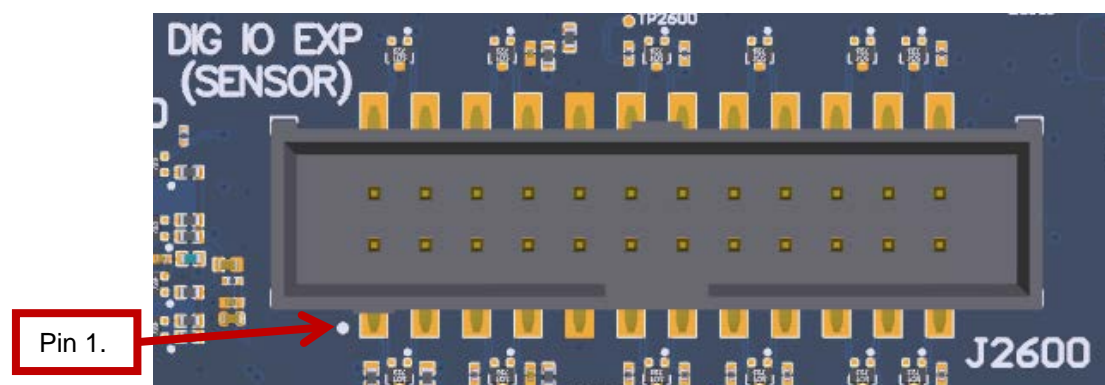
### 3.9.6 Debug Serial UART over USB J2700



**Figure 13 J2700 Debug UART over USB**

The UART connection used on the Open-Q 2100 SOM is a USB micro B connector (J2700). This debug UART is available over USB via the FTDI FT232RQ chip on the carrier board. To get the serial terminal working with a PC, user needs to ensure that the appropriate FTDI drivers are installed.

### 3.9.7 Sensor IO Expansion Header J2600



**Figure 14 J2600 Sensor Expansion Header**

The sensor expansion header J2600 allows for a 24-pin connection to an optional sensor board. If user application does not require a sensor, then this header can be used for other applications that require I2C or GPIO input and output connections.

Following is the pin breakout for sensor expansion header J2600.

**Table 3.9-6 Sensor Expansion Header J2600 Pin out**

Description	Signal	Pin NO	Description	Signal	Pin Number
BLSP1 BIT1 I2C SDA	GPIO_6_BLSP1_BIT1_SN S_I2C_SDA	J2600[1]	Accelerometer interrupt-1 input to	GPIO_96_ACC 1_INT1_N	J2600[2]

Description	Signal	Pin NO	Description	Signal	Pin Number
			processor via GPIO96		
BLSP1 BIT0 I2C SCL	GPIO_7_BLSP1_BIT0_SN S_I2C_SCL	J2600[3]	Accelerometer interrupt-2 input to processor via GPIO36	GPIO_36_ACC1_INT2_N	J2600[4]
Test Point/ GPIO	GPIO_73	J2600[5]	Gyroscope interrupt input to processor via GPIO89	GPIO_89_GYRO_INT_N	J2600[6]
Sensor IO PWR 1.8 V VREG_L6_1P8 power supply regulator (Digital)	SENS_IO_PWR	J2600 [7]	Sensor Analog power supply from VREG_L17_2 P85	SENS_ANA_PWR	J2600[8]
GND	GND	J2600[9]	GND	GND	J2600[10]
Test Point/ GPIO	GPIO_72	J2600[11]	Test Point/ GPIO	GPIO_95 (stuffing option)	J2600[12]
GPIO	GPIO_28_DISPLAY_GP1	J2600[13]	Ambient light sensor interrupt input to processor via GPIO94	GPIO_94_ALSPG_INT_N	J2600[14]
Test Point/ GPIO	GPIO_68	J2600[15]	Digital Compass interrupt input to processor via GPIO65	GPIO_65_COMP_INT_N	J2600[16]
GPIO	GPIO_53_TS0_GP1	J2600[17]	Magnetometer interrupt input to processor via GPIO54	GPIO_54_MAGDRDY_INT_N	J2600[18]
BLSP3 BIT 1, SPI CS0	GPIO_2_BLSP3_1_SNS_CS_N	J2600[19]	BLSP3 BIT3, SPI data master out/ slave in	GPIO_0_BLSP3_3_SNS_MOSI	J2600[20]
BLSP3 BIT0, SPI CLK	GPIO_3_BLSP3_0_SNS_CLK	J2600[21]	BLSP3 BIT2, SPI data master in/ slave out	GPIO_1_BLSP3_2_SNS_MISO	J2600[22]
GPIO	GPIO_84	J2600[23]	GPIO	PMIC_GPIO_2	J2600[24]

In summary, if sensor application is not needed, this expansion header can provide two BLSP1 (BIT0 and BIT 1), full BLSP3 for UART/ SPI/ I2C. Please refer to the schematic and consider the power before connecting anything to this header.

### 3.9.8 Digital IO (Low Speed) expansion header J2601

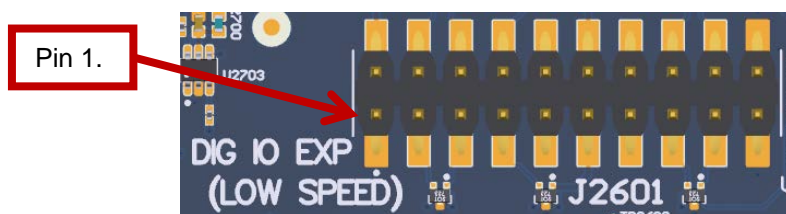


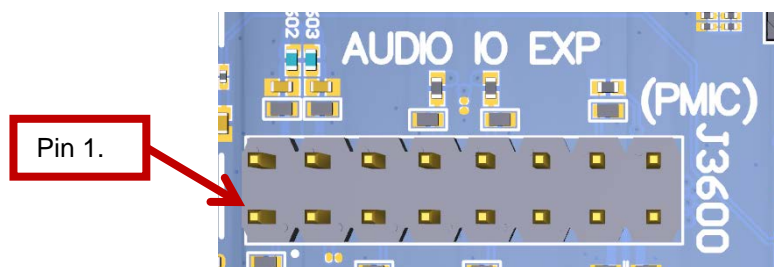
Figure 15 J2601 Digital IO (low speed) expansion header

Digital IO (low speed) expansion header J2601 is a 20-pin connector that provides access to BLSP2/ BLSP1 signals. It is ideally used for connecting external peripherals such as microcontrollers and any other devices that are based on I2C, SPI, UART and GPIO. Please refer to the SOM carrier board schematic for the level shifter, target voltage and current rating depending on stuffing option. The header supports 1.8V, 2.7V and 3.3V power supplies. All signals are referenced to 1.8V rail. The following are the detailed pin out information for digital IO (low speed) header J2601.

Table 3.9-7 Digital IO (low speed) Expansion Header J2601 Pin out

Description	Signal	Pin NO	Description	Signal	Pin Number
GND	GND	J2601[1]	2.7V Supply	VREG_L18_2P7	J2601[2]
BLSP 2 (BIT2) / GPIO 21	GPIO_21_BL SP2_BIT2	J2601[3]	BLSP 2 (BIT3) / GPIO 20	GPIO_20_BLSP2 _BIT3	J2601[4]
BLSP 2 (BIT0) / GPIO 112	GPIO_112_BL SP2_BIT0	J2601[5]	BLSP2 (BIT1) / GPIO 97	GPIO_111_BLSP 2_BIT1	J2601[6]
GPIO 87	GPIO_87_US ER_SW1	J2601[7]	GPIO 91	GPIO_91_USER _SW2	J2601[8]
GPIO 98	GPIO_98_BL SP2_SPI_CS1	J2601[9]	General purpose pin 4 from PMIC	PM_GPIO_4	J2601[10]
1.8V Power supply	SBC_VREG_1 P8	J2601[11]	3.3V Power supply	SBC_VREG_3P3	J2601[12]
GPIO	GPIO_86 (stuffing option)	J2601[13]	GLSP1 (SPI_CS1)	GPIO_97_BLSP1 _SPI_CS1	J2601[14]
Multipurpose pin 4 from PMIC	PMIC_MPP_4	J2601[15]	Multipurpose pin 3 from PMIC	PMIC_MPP_3	J2601[16]
GPIO 49	GPIO_49_US ER_LED1	J2601[17]	GPIO 69	GPIO_69_USER _LED2	J2601[18]
NC	N/C	J2601[19]	GND	GND	J2601[20]

### 3.9.9 Audio IO Expansion (PMIC) Header J3600



**Figure 16 J3600 Audio IO Expansion Header**

This expansion header provides the following audio inputs and outputs:

1. 3 analog mics (including mic in headset)
2. 1 Earphone out
3. 1 Headset out (Optional)
4. 1 Speaker out
5. Voltage rails/ reference to support analog

The table below outlines the pin out information of the audio inputs expansion header J3600:

**Table 3.9-8 Audio IO Expansion (PMIC) Header J3600 Pin out**

Description	Signal	Pin NO	Description	Signal	Pin Number
Analog mic 1 signal	CDC_MIC1_P_C	J3600-1	Speaker out (+)	SPKR_OUT_C_P	J3600-2
GND reference to the PMIC bias	CDC_GND_C_FILT	J3600-3	Speaker out (-)	SPKR_OUT_C_N	J3600-4
Analog mic 3 signal	CDC_MIC3_P_C	J3600-5	GND	GND	J3600-6
GND	GND	J3600-7	Headset out (Left)	CDC_HPH_L_C	J3600-8
Analog mic 2 signal (headset mic)	CDC_HDS_MI_C2_P_C	J3600-9	Headset out (Right)	CDC_HPH_R_C	J3600-10
GND	GND	J3600-11	GND	GND	J3600-12
Earphone out (+)	CDC_EAR_C_P	J3600-13	Headset detect	CDC_HS_DET_C	J3600-14
Earphone out (-)	CDC_EAR_C_N	J3600-15	GND (headphone reference)	CDC_HPH_RE_F	J3600-16
<b>Note:</b> The headset interfaces are option on the header J3600. Please refer to the carrier board schematic for appropriate resistor stuffing necessary to route headset signals to this header.					

### 3.9.10 Headset jack J3702

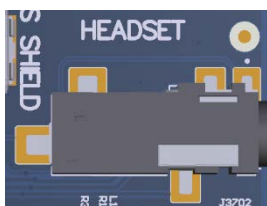


Figure 17 J3702 Audio Line Out Jack

This 3.5mm jack provides the following audio input/outputs:

1. 1 x stereo outputs
2. 1x headset mic
3. Headset detect

### 3.9.11 On Board PCB mount WLAN Antenna

The Open-Q 2100 SOM carrier board has one on-board WLAN PCB mount antenna that connects to the WCN3620 Wi-Fi module on the SOM via a coaxial cable that attaches to the U.FL receptacles. This antenna connects to the SOM in the following configuration:

- J1800 on the carrier board connects to Antenna 1 on the SOM.

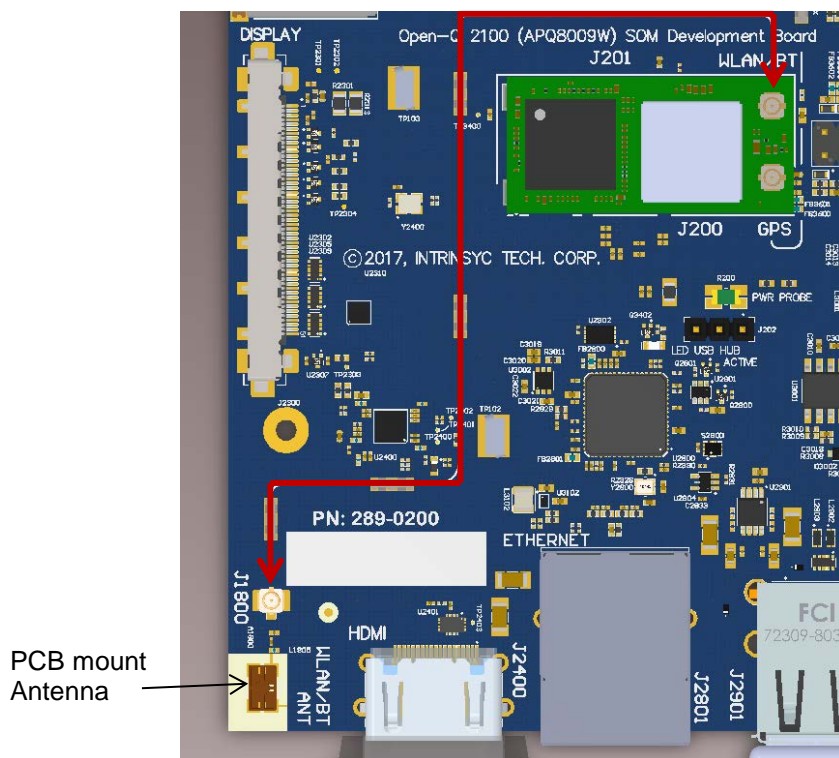


Figure 18 On Board PCB mount antenna connection

### 3.9.12 Open-Q 2100 Display

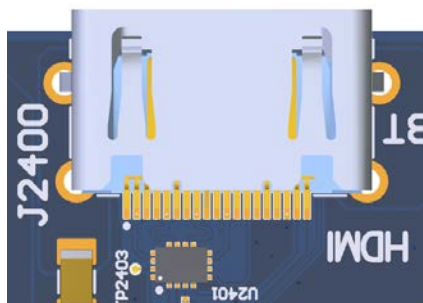
The display output options for the Open-Q 2100 Development Kit consists of:

- An HDMI type A connector
  - HDMI (720p 60Hz)
- A 51-pin display connector J2300 that supports:
  - Single DSI DPHY 0.9 (up to 720p at 60 fps)
  - Touch screen capacitive panel via I2C, and interrupts
  - Backlight LED
    - Can support external backlight driver control and power
    - PM8916-1 backlight driver supports two LED strings of up to 20mA each

The Open-Q 2100 Development Kit platform can support the following display combinations:

MIPI DSI	1 x 4lane DSI0 Display 1280 x 720 at 60fps
HDMI	720p 60Hz

### 3.9.13 HDMI Connector J2400

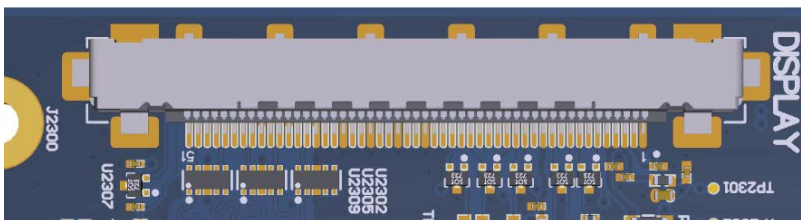


**Figure 19 HDMI Type A Connector**

The on-board HDMI type A connector enables the Open-Q 2100 SOM development platform to connect to an external HDMI monitor/ television via an HDMI cable. As part of a new feature, the Snapdragon™ 2100 Series (APQ8009W) can now support up to 720p HD (1280 x 720 at 60fps)

Please note that the Open-Q 2100 Development Kit is for evaluation purposes only and may not be HDMI compliant.

### 3.9.14 Display Connector J2300



**Figure 20 51-Pin Display Connector**

The 51-pin display connector provides the following features/ pin-outs that enable the development kit to connect to a MIPI DSI panel/ device:

Note: Please refer to the carrier board schematic and display board tech note when designing a custom display board.

- DSI
  - 1 x 4 lane DSI
- Backlight
  - Built-in backlight WLED driver on PM8916-1
  - Primary external backlight (BL0)
    - Backlight control signals
    - External Power
- Additional GPIOs for general purposes available
- Touch Panel
  - Supports one touch screen controller
  - Supports I2C via BLSP5

#### Power specifications

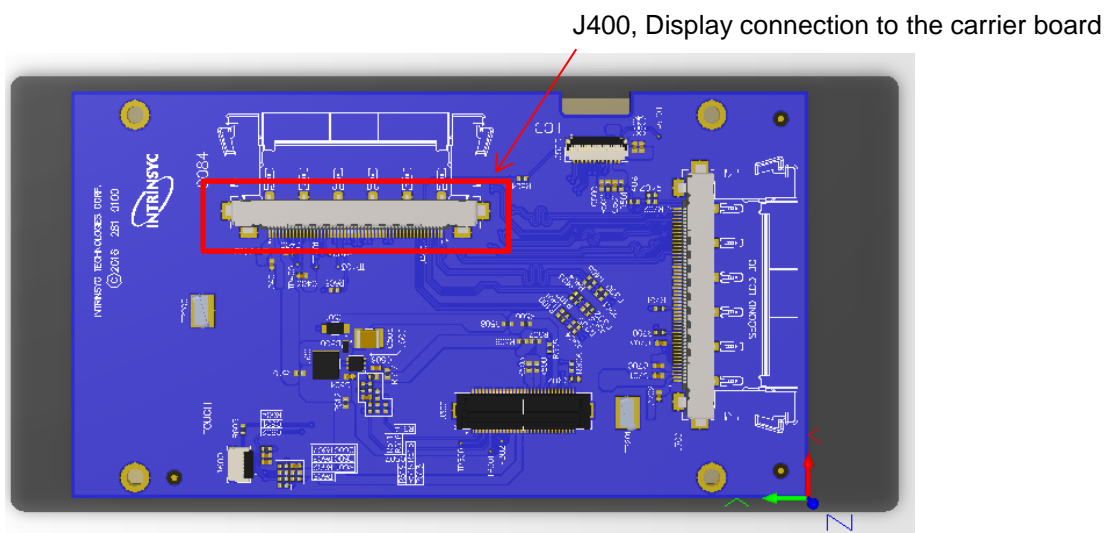
The display connector supports the following power domains:

Display Signal	Power Domain
PM8916-1 LDO4 (1.8V)	TBD
PM8916-1 LDO17 (2.85V)	TBD
Carrier 12V	TBD
Carrier 1.8V	TBD



The Intrinsic Display (Open-Q 210x LCD part number: QC-DB-J00005 ) is an additional display accessory that can be used with the display connector J2400 on the carrier board. Please use 51position flex cable from JAE (JF08 series) to connect display board and carrier board. This board allows users to interface with the development kit via the LCD that comes preinstalled on the display board. The following figure illustrates the interfacing connectors on the display board.

**Note:** The display board comes as an additional add-on to the Open-Q 2100 Development Kit. To purchase this, please visit <http://shop.intrinsyc.com> or contact Intrinsyc at [sales@intrinsyc.com](mailto:sales@intrinsyc.com) for details.

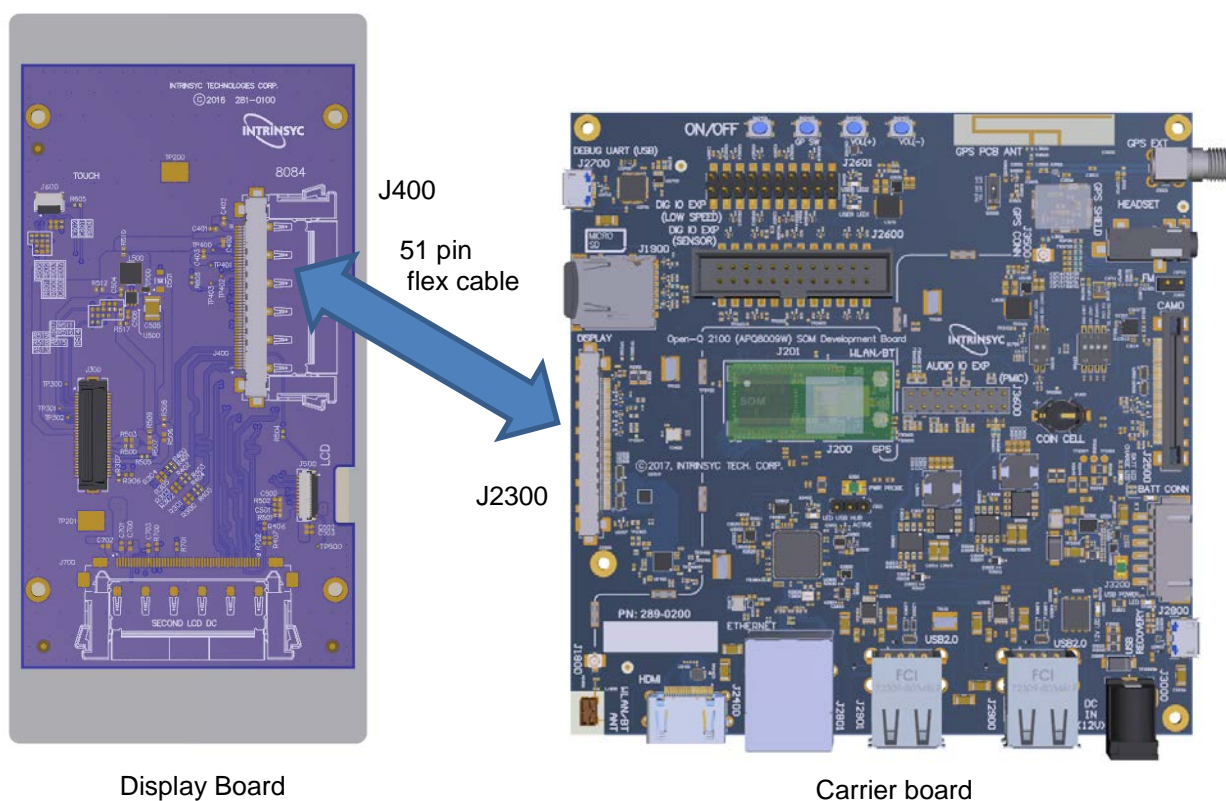


### Figure 21 Display Board



## Connecting the Display Board to the Development Kit

This configuration allows the user to use the LCD display that comes with the display adaptor board. As shown in the picture below, the MIPI DSI0 lines, which come from the 51-pin JF08 connector, directly connects to the LCD panel via flex cable (part number: JF08R0R051020MA). See the section below for more details on this LCD panel. It is important to note that connector J400 on the display board needs to connect to J2300 on the carrier board for this configuration to work.



**Figure 22 Display Board Default Configuration**

### 3.9.14.1 LCD display panel

The LCD panel comes preinstalled on the Intrinsic Open-Q display adaptor board (P/N# QC-DB-J00005). Below are the Panel specifications:

- **Resolution:** 480x854
- **LCD Type:** IPS
- PCAP touch panel with cover glass
- **No of Lanes:** 1 x 2 lane MIPI DSI interface via Display Board.
- **Diagonal Length:** 4.5"
- Contact [sales@intrinsic.com](mailto:sales@intrinsic.com) for more information

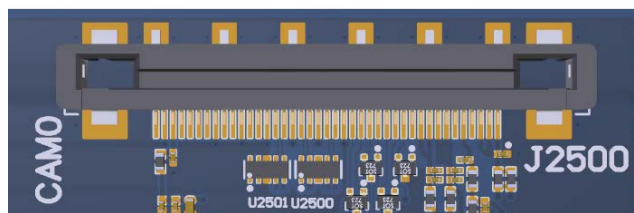
Note: The display above when mounted on the Intrinsic Open-Q Display Adapter is meant to work with the carrier board. Altering the use of this LCD panel is not recommended.

### 3.9.15 Camera Connector J2500

The Open-Q 2100 Development Kit supports one 2-lane MIPI CSI camera interfaces via a JAE 41-pin connector.

The following are some features of the camera connectors:

- 1 x 2 lane MIPI CSI signals
- I2C control (CCI0)
- Camera CSI connector is on the carrier board edge
- Self-regulated camera modules can be powered with 3.3V power (SBC\_VREG\_3P3)
- Uses JAE FI-RE41S-VF connector for exposing MIPI, CLK, GPIOs and Power rails.
- Please use JAE FI-RE41S-HF and corresponding cable to mate with the camera connectors on the carrier board



**Figure 23 J2500 Camera Connector**

The figure above shows the MIPI CAM0 (J2500) connector.

The table below outlines the pin outs of the connector

**Table 3.9-9 MIPI CSI Camera Connector J2500 Pin out**

Pin#	CAM0 (J2500)	Description
1, 2, 3	SBC_VREG_3P3	Power output. Connected to main +3.3V SBC_VREG_3P3 max current 700mA. Default use is for camera flash.
4	GND	Ground
5	VREG_L17A_2P85	Power output. Connected to PM8916-1 VREG_L17A regulator. Default is +2.85V. Maximum current 300mA. Default use is for camera AVDD.
6	SBC_VREG_1P2	Power output. Connected to 1.2V SBC_VREG_1P2. Default use is for camera DVDD.
7, 8	VREG_L8_2P9	Power output. Connected to PM8916-1 VREG_L8 regulator. Default is +2.9V. Maximum current 300mA. Default use is for camera actuator VDD.
9, 10	VREG_L6_1P8	Power output. Connected to PM8916-1 VREG_L6 switch output. Default is +1.8V. Maximum current 300mA. Default use for camera DOVDD.
11	GND	Ground
12	GPIO_31_FLASH_EN (APQ_GPIO31)	Output. Connected to APQ8009W Default use is for camera flash strobe enable
13	GPIO_35_CAM0_RESET_N (APQ_GPIO35)	Output. Connected to APQ8009W GPIO35. Default use is for camera reset
14	GPIO_34_CAM0_STANDBY_N (APQ_GPIO34)	Output. Connected to APQ8009W. Default use is for camera standby
15	GPIO_30_CCI_I2C_SCL (APQ_GPIO30)	Output. Connected to APQ8009W GPIO30. Default use is for camera CCI0 I2C clock interface
16	GPIO_29_CCI_I2C_SDA (APQ_GPIO29)	Input / output. Connected to APQ8009W GPIO29. Default use is for camera CCI0 I2C data interface
17	GPIO_26_CAM_MCLK0 (APQ_GPIO26)	Output. Connected to APQ8009W GPIO26. Default use is for camera master clock. Maximum 24MHz
18	GPIO_32_FLASH_NOW (APQ_GPIO32)	Output. Connected to APQ8009W GPIO32. Default use is for camera flash strobe trigger
19	GND	Ground
20	MIPI_CSI0_LANE0_N	Input. MIPI CSI0 data lane 0
21	MIPI_CSI0_LANE0_P	Input. MIPI CSI0 data lane 0
22	GND	Ground
23	MIPI_CSI0_CLK_N	Input. MIPI CSI0 clock lane
24	MIPI_CSI0_CLK_P	Input. MIPI CSI0 clock lane
25	GND	Ground
26	MIPI_CSI0_LANE1_N	Input. MIPI CSI0 data lane 1
27	MIPI_CSI0_LANE1_P	Input. MIPI CSI0 data lane 1
28	GND	Ground
29, 30	NC	Not Connected
31	GND	Ground
32, 33	NC	Not Connected
34	GND	Ground
35, 36, 37, 38	NC	Not Connected
39	SBC_VREG_1P2	Power output. Connected to 1.2V SBC_VREG_1P2. Default use is for camera DVDD.
40	Ground	Ground
41	NC	Not Connected

**Note:** A 41-pin cable assembly from JAE Electronics (part number JF08R0R041020MA) can be used to connect camera board and carrier camera connector.

### 3.9.16 USB 2.0 Client Port J2800

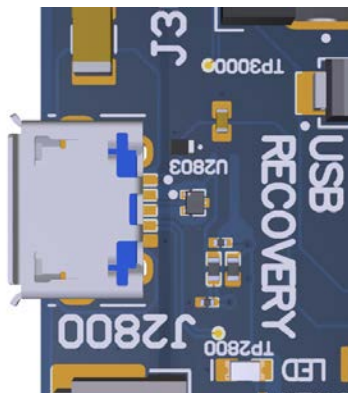


Figure 24 J2800 USB2.0 for ADB

J2800 allows the development kit to communicate with a host PC using the Android Debug Bridge (ADB). This port is a client mode port only. This port is also used for charging battery.

### 3.9.17 USB 2.0 host interface

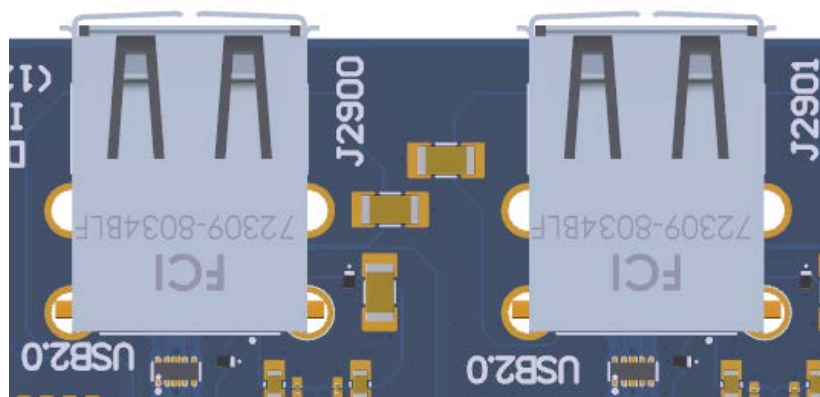
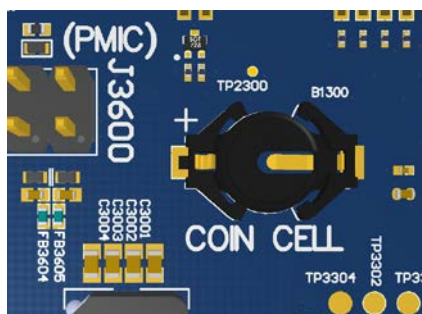


Figure 25 J2900 and J2901 USB2.0 Host Ports

J2900 and J2901 allow the development kit to communicate as a High-speed host. These are dual stacked USB2.0 Type-A connectors. Make sure USB client port (J2800) is not in use when USB 2.0 host interface is active. The USB host ports/ Ethernet and USB client port are mutually exclusive.

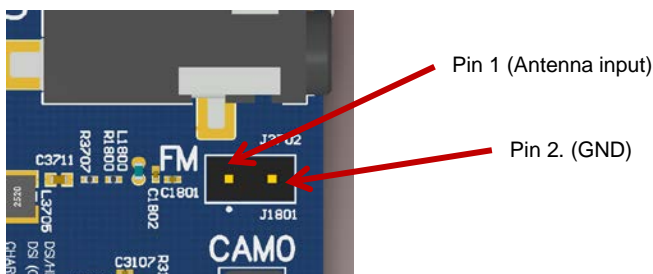
### 3.9.18 Coin cell battery holder



**Figure 26 B1300 Coin cell holder**

B1300 coin cell holder allows user to use ML614 Coin cell (Not shipped with the Open-Q 2100 Development kit) for supplying power to the SOM VCOIN power input.

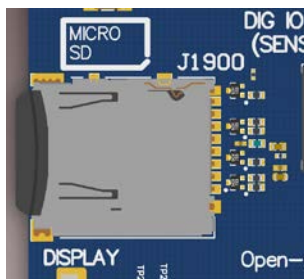
### 3.9.19 FM connector J1801



**Figure 27 J1801 FM antenna connector**

J1801 provides connection to the AC coupled FM antenna. The connector is standard 2.54mm pitch male header with two pins (Molex PN: 22-28-4360). The Pin 1 is the antenna input and pin 2 is ground.

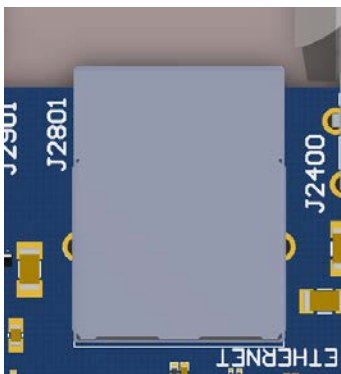
### 3.9.20 Micro-SD card connector J1900



**Figure 28 J1900 micro-SD card connector**

J1900 (Micro-SD card connector) provides 4-bit secure digital (SD) 3.0 interface for external storage.

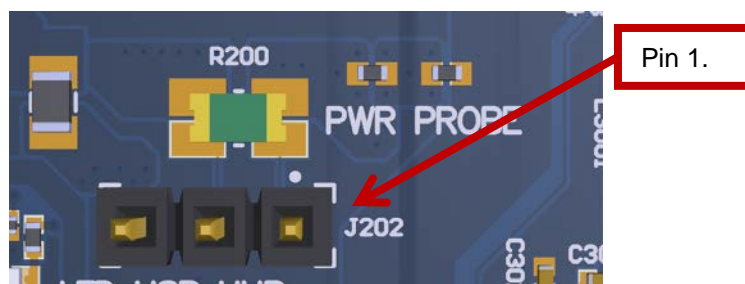
### 3.9.21 Ethernet connector J2801



**Figure 29 J2801 Ethernet connector**

J2801 (Ethernet connector) provides 10/100 Ethernet connectivity to the Open-Q 2100 Development kit via LAN9514 USB-to-Ethernet Hub. Please note that the USB hub and Ethernet features is not available when micro-B USB cable is plugged in the ADB (Recovery) J2800 port.

### 3.9.22 Power probe J202



**Figure 30 J202 Power probe connector**

J202 (Power probe connector) provides method of measuring power consumption of Open-Q 2100 SOM. The 0.01R sense resistor is placed in series on the VPH\_PWR rail to provide method of current consumption measurement. The pin configuration of three pin header is given in the table below:

**Table 3.9-10 Power probe J202 Pin out**

Description	Signal	Pin Number
Current sense negative	CSN	J202[1]
Current sense positive	CSP	J202[2]
Ground	GND	J202[3]

### 3.9.23 GNSS external antenna connector J3501



**Figure 31 J3501 GNSS external antenna connector**

The Open-Q 2100 carrier board has both PCB antenna and external antenna connector (SMA). User can switch between PCB antenna and external antenna by using DIP switch S3500. The configuration of the DIP switch is given in the table below. A passive or an active antenna may be used as external antenna and a 2.7V bias is provided on the antenna input for powering an active antenna.

**Table 3.9-11 DIP switch S3500 configurations**

Function	DIP Switch	Description	Notes
GNSS antenna switch	S3500-1	Toggles between GNSS PCB antenna and external antenna	Default out of the box configuration is OFF which is internal antenna selected.