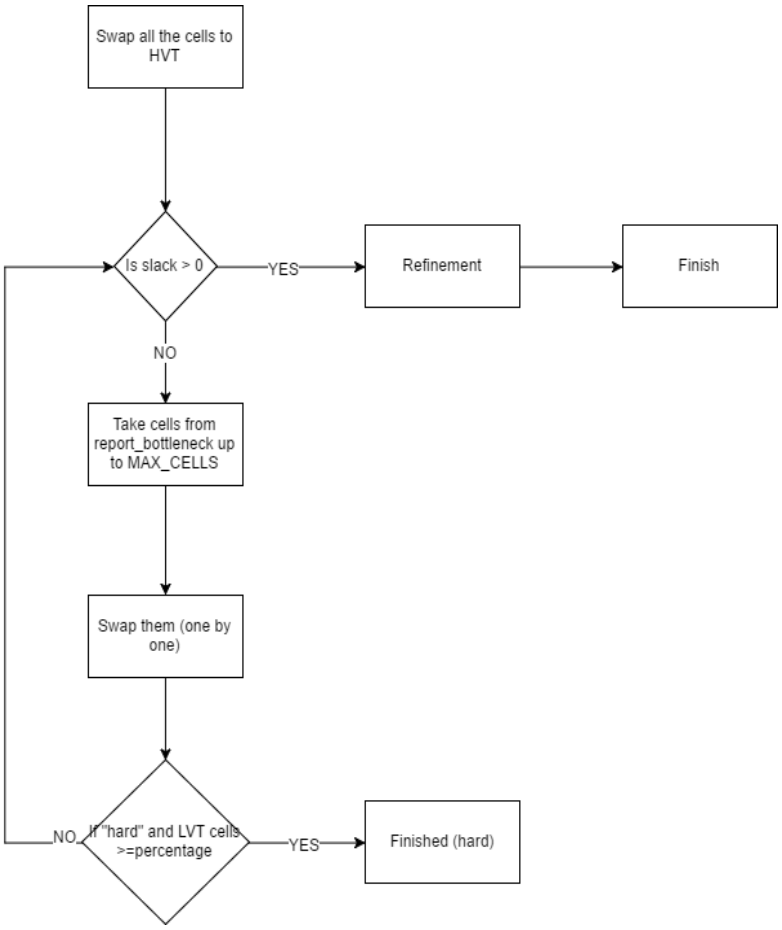
Report contest synthesis and optimization

The objective of our script is to realize a post synthesis optimization of leakage power exploiting the dual Vth technique.
Just to resume, we have two identical libraries available, one with a low Threshold voltage and one with a high Threshold voltage. The former is more efficient from a delay point of view, the ladder the opposite but more efficient from the leakage power point of view.
Our script starts from a synthetized circuit using only the Low Voltage Threshold library, and swap as many cells as possible to the equivalent cell in the HVT library.

How it works:



In order to swap cells without affecting the timing performances, we look for the cells with highest slack so that, swapping them to HVT equivalent, does not affect the slack (or minimally).

For this reason, we reasoned in a complemented way: we first swap all the cells to HVT (this will return us very likely a negative slack as we are worsening every cell in delay), then we select the most common cells found in the most critical paths and we swap them thanks to the **report_bottleneck** function provided by Synopsys. This should improve our slack of as many paths as possible.

As in this way, it is very likely we swap back to LVT unnecessary cells, we perform a **refinement** operation when slack is positive. Here we simply try to swap each cell and if we still have a positive slack, we keep the swapping.

In the Hard configuration, we stop when we swapped back to LVT the maximum number of cells allowed (so eventually this could return us a negative slack), while with the Soft configuration the objective is to get a positive slack even if it violates the maximum number of LVT cells.