YUNING(EMILY) GUI

emilygui2011@gmail.com • (585)-354-3588
1731 Sageland Dr, San Jose, CA 95131

Summary of Qualifications

- Programming skills: HTML, CSS, Javascript, C/C++, Python, Java
- Experience of software and web application development using Python object-oriented programming
- Solid background in computer systems architecture; Experience of logic design and simulation for CPU, cache and memory systems in C/C++ and Verilog HDL
- Familiar with Perl and Unix Shell scripting; Database knowledge on MySQL and GQL
- Development tools experience: Eclipse, PyCharm, Vim, SVN under Linux and Windows platform
- Strong problem solving skills; Work efficiently in a team development environment

Education

University of Rochester, Rochester, NY *September 2012 - May 2014*
Master of Science in Electrical and Computer Engineering GPA: 3.52/4.00

Jiangnan University, Wuxi, China *September 2008 - July 2012*
Bachelor of Engineering in Microelectronics GPA: 84/100; Major GPA: 85.5/100

Technical and Programming Projects

Wiki Development on Google App Engine (Python, PyCharm, GAE) *October 2014 – December 2014*
- Built a wiki page which only logged-in users have editing page privileges, with history version section included; The wiki was developed on GAE platform using Python, GQL and Jinja2 Templates
- The wiki application has caching functionality and includes web API which can return JSON

Mobile Friendly Image Slider Module (HTML5, CSS3 and Javascript) *June 2014 - August 2014*
- Developed image slider with HTML, CSS and Javascript for mobile web app, which supports fast continuous slideshow, real-time response and various CSS3 animations

Train Schedule Search Tool (jQuery Mobile) *March 2014 – May 2014*
- Built a train schedule search web application using jQuery Mobile and Ajax which features adaptive form and reflow table for mobile side

Out of Order MIPS CPU (Verilog, C++) *November 2012 - January 2013*
- Implemented a 2 paths 9 stages out of order processor in Verilog which supports MIPS ISA
- Debugged with C++ testbench under Verilator and Eclipse environment, final design can pass benchmarks with total amount of 100,000+ MIPS assembly instructions

Image Processing Filter using FPGA (Verilog, Xilinx ISE) *October 2013 - January 2014*
- Designed real-time image processing filter in Verilog for edge detection algorithm on Xilinx Virtex5 board

Web page Information Extraction by Web Crawler (Python, PyCharm) *April 2013 – May 2013*
- Parsed HTML page and extracted required information (urls, text, files etc.) by web crawler using Python

Research and Teaching Experience

Research Assistant at Embedded Integrated System-on-Chip Research Lab, Rochester, NY
July 2013 - December 2013
- Participated on modeling embedded DRAM (eDRAM) in NoC router buffer; Did eDRAM's simulation of retention time, area, power parameters under 65nm process with Unix based C/C++ simulators

Tutor at University Tutoring Program, Rochester, NY *January 2014 – May 2014*
- Provided individual tutoring sessions for undergraduates courses "ECE 112 Logic Design" and "ECE 114 Introduction to Programming"