Design of High PSRR Folded Cascode Operational Amplifier for LDO Applications

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***Abstract*— This paper presents a novel CMOS folded cascode operational amplifier that leads to high PSRR and provides gain nearly equal to that of a two stage op-amp. The proposed design is implemented in GPDK 0.18µm CMOS technology. This op-amp uses a folded cascode structure in the output stage combined with the differential amplifier having PMOS input transistors to achieve good input common mode range and lower flicker noise. It has an important feature that it allows the input common mode level close to supply voltage. The proposed topology improves the PSRR of op-amp which can be used for LDO applications. Simulations using Cadence under 1.8 V show a DC gain of 72.0404 dB and a phase margin of 62.4636 degree at a unity gain bandwidth of 13.33 MHz with the power consumption smaller than 0.13 mW along with a PSRR of 72.0966 dB. The layout of the design shows that the area acquired on the chip is approximately equal to 8897.27 µm^2.**

Keywords*— Folded Cascode Op-amp; Power Supply Rejection Ratio (PSRR); Input Common mode range.

I. INTRODUCTION

Operational amplifier is an integral part of analog and mixed signal system. The design of high-performance op-amp has always been one of the hot spots of analog integrated circuit design as its performance directly affects the overall performance of circuits and system [1]. Hence, proper design of the op-amp is necessary according to the application where it is needed. With the continuous development of integrated circuit technology, high-performance op-amp is widely used in high-speed ADC, DAC, switched capacitor filter, band-gap voltage reference circuits, LDO regulators, precision comparators and other electronic devices.

With each generation of CMOS technology, the decrease in supply voltage and transistor length continuously brings more complex issue for the design of the op-amp [2]. Cascode amplifiers can have quite large gains and reduce significantly the Miller effect, which gives them an improved frequency response compared with that of other amplifiers [3].The main aspects of folded cascode op-amp presented here are high DC gain and high PSRR. Therefore, among many op-amp topologies, folded cascode is one of the most common op-amp topologies that has high open-loop DC gain and proper frequency response. In [4, 5] authors have described that the folded cascode op-amp with PMOS input transistors has lower flicker noise than the folded cascode op-amp with NMOS input transistors which results in achieving high PSRR. This advantage makes this op-amp a main choice for LDO applications. MOS transistors provide DC gain and amplification in saturation region only. To ensure the device is working under saturation region, bias potentials are tuned accordingly. Also, the current distribution in input and output stages along with the overdrive voltages of each branch is chosen according to meet the design specifications. The disadvantage of folded cascode op-amp compared with the telescopic cascode op-amp is higher current consumption. But the telescopic op-amp has lower input and output swing.

A complete analysis of fully differential folded cascode circuit along with layout is presented in this paper which shows how this circuit leads to a high PSRR and gain of a two stage op-amp in a single stage. Conventional architecture of folded cascode op-amp is introduced in Section II. In Section III design equations are developed in order to achieve dimensions of transistors and a sequence of design steps is established. Section IV includes simulation results which include graphical representation of gain and phase, slew rate and PSRR to visually illustrate design specifications. The results of simulations are shown to agree very well with the use of our design equations. Obtained results are also compared from previous work. It also describes good layout techniques that are implied for better protection of transistors against unavoidable mismatching issues during the fabrication process. Section V provides concluding remarks and future work that can be implemented on the proposed circuit.

II. FOLDED CASCODE AMPLIFER

Folded cascode op-amp uses a cascoding in the output stage combined with an unusual implementation of differential amplifier to achieve good input common-mode input range. Thus, folded cascode op-amp offers self compensation, good input common mode range, and gain of a two stage op-amp [6]. In case of telescopic and cascode topology, although the current required is less as compared to folded cascode but to ensure every transistor to be in saturation region is quite harder than in folded cascade topology. The name "folded cascode" comes from folding down n- channel cascode active loads of a diff-pair and changing the MOSFETs to p-channels. This op-amp has good PSRR as compared to two-stage op-amp and telescopic op-amp [7].

As shown in Fig. 1 [8], M_1 and M_{1A} form one cascode structure and M_2 and M_{2A} form another. The current mirror converts the differential signal into single-ended output by sending variations in the drain current of M_{1A} to the output. The resulting op-amp is folded cascode op-amp. Bias is realized by making the currents in current sources M_{11} and M_{12} larger than $|I_{D5}|/2$. Thus,

$$I_{D1A} = I_{D2A} = I_{D11} - |I_{D5}|/2 = I_{D12} - |I_{D5}|/2 = I_{BIAS} - I_{TAIL}/2 \quad (1)$$

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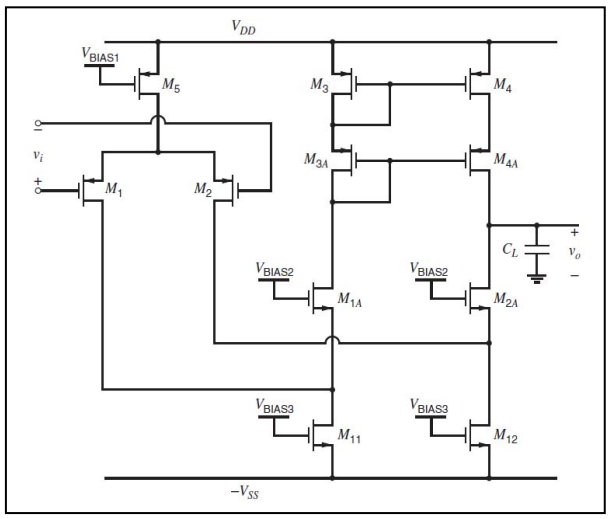

Fig. 1. Folded cascode op-amp with PMOS inputs.

Since M_3 *and* M_{3A} are diode connected, the voltage from V_{DD} to the gate of M_{4A} *is* $2|Vtp| + 2|Vov|$. Therefore, the source-drain voltage of M_4 is $|Vtp| + |Vov|$, and the maximum output for which both M_4 and M_{4A} operate in the saturation region is $V_{OUT(max)} = V_{DD} - |Vtp| - 2|Vov|$. To find minimum output voltage, V_{BIAS2} is assumed such that M_{12} operates at the edge of saturation region. Then V_{DS} of M_{12} is equal to Vov and $V_{OUT(min)} = -V_{SS} + 2Vov$. Small signal voltage gain at low frequencies of this circuit is $A_V = G_m R_o$ where G_m is the transconductance of differential pair and R_o is the output resistance.

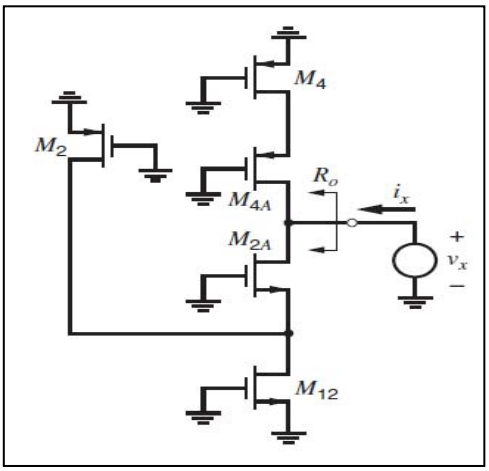

Fig. 2. Circuit for calculating output resistance R_o.

As shown in Fig. 2, the output resistance R_o will be,

$$R_o = (Rout|M_{2A}) \parallel (Rout|M_{4A}) \quad (2)$$

$$Rout|M_{2A} = (ro_2||ro_{12}) + ro_{2A}[1 + (gm_{2A} + gmb_{2A})(ro_2||ro_{12})]$$

$$\approx [gm_{2A}(ro_2 \parallel ro_{12})]ro_{2A} \quad (3)$$

$$Rout|M_{4A} = ro4 + ro_{4A}[1 + (gm_{4A} + gmb_{4A})(ro_4)]$$

$$\approx (gm_{4A}ro_4)ro_{4A} \quad (4)$$

Optimizing the amplifier for minimal power dissipation requires reducing the drain currents through the transistors, yet on the other hand, the gain is proportional to the drain current because,

$$gm = 2I_D / (V_{GS} - V_{TH}) \quad (5)$$

Therefore the only compromise is to reduce the overdrive voltage of each device, but in doing so allow just enough voltage to prevent any devices from leaving the saturation region [9]. Hence trade-off is required between saturation current and overdrive voltage in order to optimize the gain.

III. Proposed Design

The main part of folded cascode op-amp is the differential pair which acts as an input stage. Hence proper matching of the differential pair is quite important. Generally an op-amp consists of a differential pair in the first stage and a common source in the second stage so as to increase the overall gain of op-amp. But this requires an additional capacitance for the frequency compensation. Moreover, additional capacitance introduces a second pole in the amplifier system. The proposed design shown here, is set to achieve overall gain in the first stage. Also this op-amp helps in the rejection of different noise components present in the input signal and in the supply voltage.

Fig. 3 illustrates the complete schematic of the proposed design. It is composed of p-channel differential input pair (M1, M2), followed by common-gate stages (M7, M8) and current sources (M5, M6), and a self-biased cascode current mirror (M9 – M12) that inverts the current signal. M3 and M4 form a current mirror that provides bias current for differential input pair. Bias voltages Vb1 and Vb2 are provided to M5-M6 and M7-M8 respectively in order to meet the current specifications at the cascode stage so as to keep all the transistors in saturation region. The current flowing through M7 and M8 i.e. Ia is Ib – Iref/2. Therefore, Ib must be higher than Iref/2. For proper biasing of differential pair, Iref taken here is equal to 40 µA. A biasing circuit can also be used in this design. As the source terminals of M5 and M6 are grounded, hence there gate voltages i.e Vb1 can be calculated using overdrive voltage of that transistor. Hence, by adjusting the bias potentials Vb1 and Vb2, Ib is set to 30 µA. Ia will be equal to 10 µA. The output current at load will be 2Ia i.e. 20 µA. The W/L ratio of each transistor can be calculated with the help of design specifications given in table I and the saturation current equation given as;

$$I_D = (1/2)\,\mu_{n,p} C_{OX} (W/L)_i (V_{ov})^2 \text{ ; where i = 1, 2, 3...} \quad (6)$$

Allocating appropriate overdrive voltages for each branch the bias voltages Vb1 and Vb2 can be found out. For NMOS and PMOS transistor V_t is chosen to be 470 mV and 450 mV respectively. The device parameters can be found in the cadence library. Calculated values of W/L are not enough to make op-amp work under saturation region and hence need to be tuned accordingly. Tuning is generally done through a series of simulations under different input values. A summary of aspect ratios of the transistors are tabulated in table II.

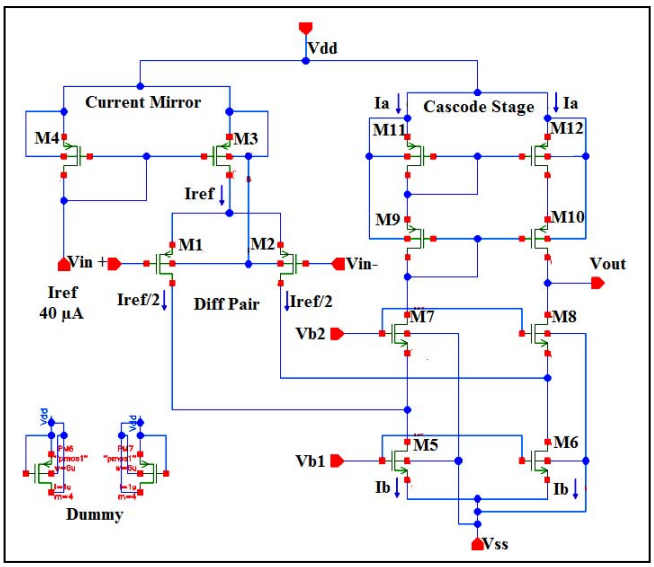

Fig. 3. Schematic of folded cascode op-amp.

TABLE I. DESIGN SPECIFICATIONS

Specifications	Values
Technology	180 nm
Power Supply	1.8 V
Gain	≥ 70 dB
Slew Rate	20 V/µsec
Unity Gain Bandwidth	20 MHz
Phase Margin	> 60 Degrees
Power Consumption1	< 1 mW
PSRR	> 60 dB
Load Capacitance (C_L)	2 pF

Gain can be calculated by finding R_o from equation (2) and transconductance (G_m) of the PMOS differential pair. Dummy transistors are used to achieve good matched layout of M1 and M2 and to reduce production tolerance.

The layout of the circuit is shown in Fig. 3. MOSFETs are fingered to decrease gate resistance. To reduce substrate coupling noise, guard rings are used that surround the MOSFETs. Using common centroid technique, the fluctuations of the device characteristics is also been cancelled. The area acquired by the op-amp is approximately 103.55 µm × 85.9225µm (8897.27 µm^2).

TABLE II. TRANSISTORS ASPECT RATIOS

Transistor's Name	*W/L*	*Bias Current (µA)*	*V_{OV} (mV)*
M1, M2	24µ/1µ	20	-
M3, M4	112µ/1µ	40	100
M5, M6	16µ/4µ	30	200
M7, M8	16µ/4µ	10	100
M9 – M12	32µ/1µ	10	100

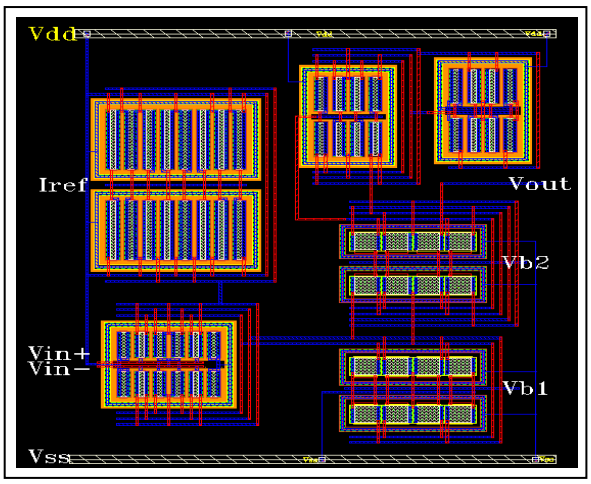

Fig. 4. Proposed folded cascode op-amp layout.

IV. SIMULATION RESULTS AND COMPARISON

Simulation is done using Cadence virtuoso analog design environment using GPDK 180nm library. AC analysis of the circuit depicts a DC gain of 72.0404 dB, UGB of 13.3369 MHz and phase margin of 62.4632 degree. The AC analysis plot is shown in Fig. 5.

Expression to calculate dc gain of the proposed op-amp is given as ;

$$A_V = G_{m(1,2)}R_o \quad (5)$$

Where $G_{m(1,2)}$ is the transconductance of M1 and M2 and can be calculated as;

$$G_{m(1,2)} = GBW \times C_L \times 2\pi \quad (6)$$

$$R_o = (Rout|M_8) \,||\, (Rout|M_{10}) \quad (7)$$

$$Rout|M_8 = (ro_2||ro_6) + ro_8[1 + (gm_8 + gmb_8)(ro_2||ro_6)]$$
$$\approx [gm_8(ro_2 \,||\, ro_6)]ro_8 \quad (8)$$

$$Rout|M_{10} = ro_{12} + ro_{10}[1 + (gm_{10} + gmb_{10})(ro_{12})]$$
$$\approx (gm_{10}ro_{12})ro_{10} \quad (9)$$

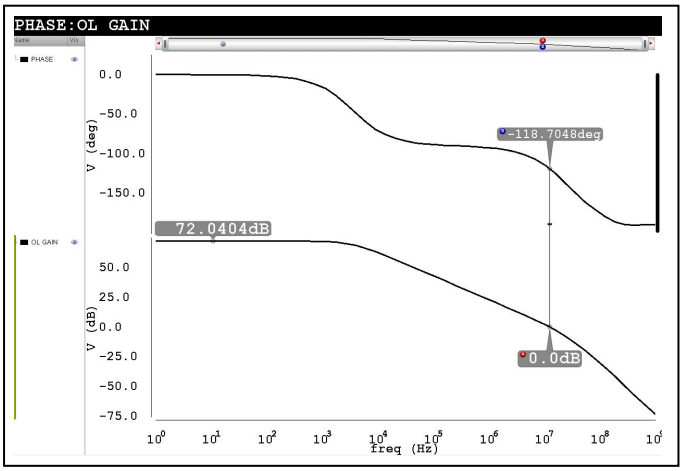

Fig. 5. Gain and Phase plot under typical conditions.

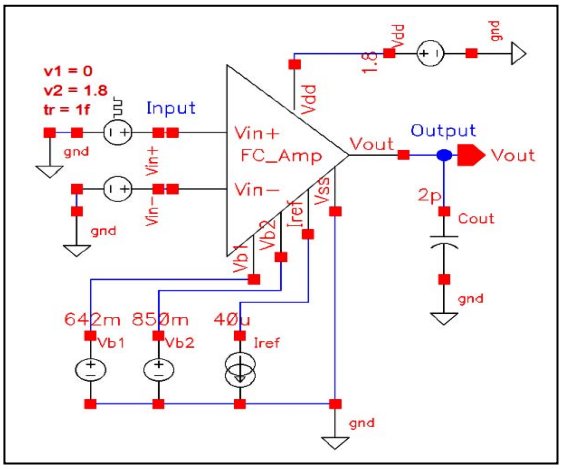

Fig. 6. Test setup for slew rate measurement.

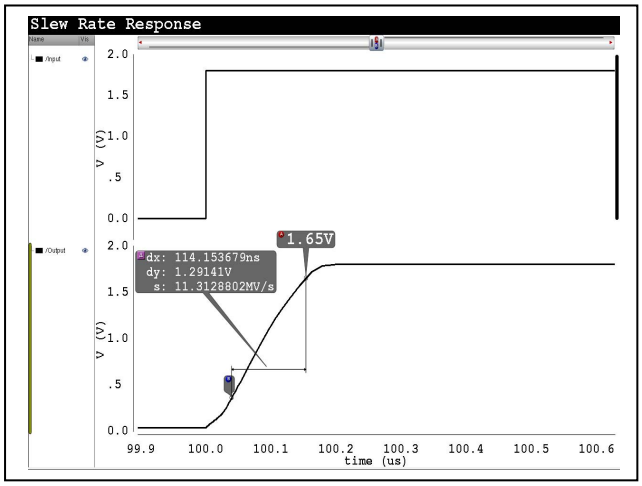

Fig. 7. Plot of slew rate.

The slew rate of the op-amp is calculated as dV_{out} / dt. Using a pulse input with voltage variation from 0 V to 1.8 V the transient response of the circuit as shown in Fig. 6, gives the slew rate of 11.63 V/µsec. The power consumed by the circuit under 1.8 V is 129.553 µW.

PSRR can be calculated by simulating the test circuit as shown in Fig. 7. An AC magnitude of 1 V is fed in the Vdd and Vin- is connected to the output. The AC analysis plot shown in Fig. 8 shows PSRR of -72.0966 dB.

Main sources of noise in an LDO voltage regulator are error amplifier and internal reference voltage. For reduction of flicker noise in this op-amp, PMOS differential pair is used. Achieving such a high PSRR will increase the ability of LDO to reject ripples that occur at the input side. Finally, the performance of proposed folded cascode op-amp is summarized in Table III where a comparison with previous implementations is also shown.

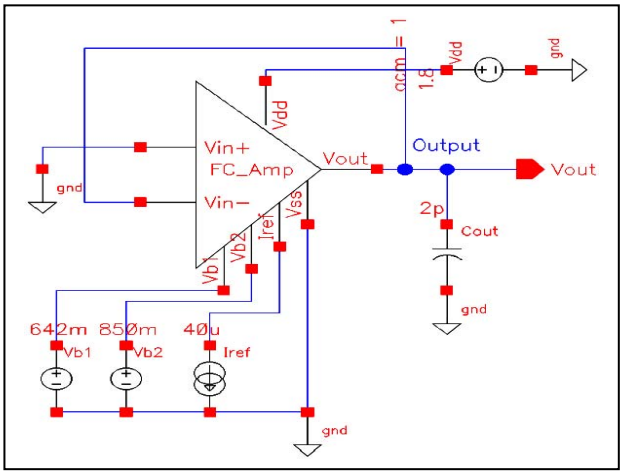

Fig. 8. Test setup for PSRR measurement.

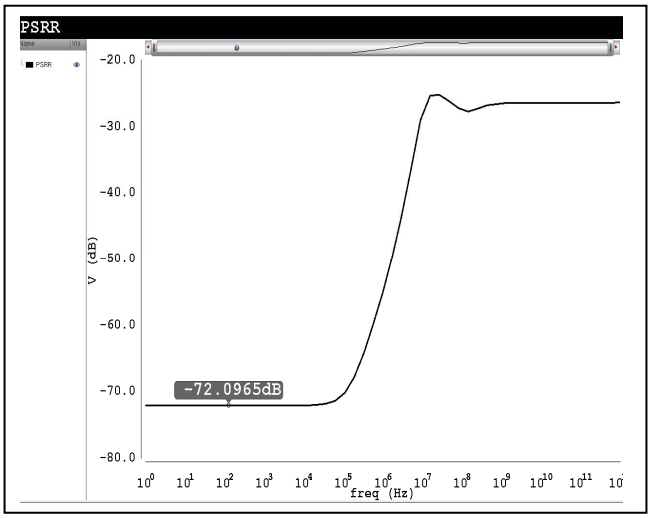

Fig. 9. PSRR curve.

TABLE III. COMPARISON OF THE PROPOSED FOLDED CASCODE OP-AMP WITH PRIOR DESIGNS

Parameters	[2]	[7]	[9]	[10]	[11]	[12]	[13]	Proposed
Technology	0.18 μm	0.35 μm	0.5 μm	0.18 μm	0.18 μm	1.25 μm	0.18 μm	0.18 μm
Supply Voltage (V)	3.3	2	3	1.2	±1.65	±2.5	1	1.8
Gain (dB)	96.29	85	67	50.9	77	73.6	67.81	72.04
PM (deg)	83.5	46	68	77.2	63	-	45.9	62.4
UGB (MHz)	-	230	270	490	140	9.5	0.9643	13.33
PSRR (dB)	-	85	-	-	77	25	-	72.49
Power (mW)	<0.1	-	<2.1	0.661	3.39	-	0.00724	<0.13

V. Conclusions and Future Work

The op-amp proposed in this paper is implemented in GPDK 0.18µm CMOS technology which produces a gain of two stage op-amp in a single stage without the need of frequency compensation. High PSRR of 72.0966 dB is achieved under 1.8 V supply voltage. PMOS inputs used in differential pair are responsible for high PSRR of the amplifier. Results clearly indicate that the proposed design can be used in LDO applications.

To increase input and output swing further the current mirror used here can be replaced with high swing cascode current mirror. Stability of this amplifier can be increased using a common mode feedback circuit. For high gain applications gain boosting technique can be used.

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