Folded Cascode OTA Design for Wide Band Applications

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Abstract—This paper deals with design and optimization of a folded cascode operational transconductance amplifier. First, a detailed description of an optimum OTA topology is done in order to optimize MOS transistor sizing. Second, the design of folded cascode OTA, which works for frequencies that lead to a base band circuit design for RF application, is based on transistor sizing methodology. Third, folded cascode OTAs generally find several applications that are well developed. Simulation results are performed using SPICE software and BSIM3V3 model for CMOS 0.35µm process, show that the designed folded cascode OTA has a 85dB DC gain and provides a gain bandwidth product of around 332MHz.

***Keywords*—**CMOS IC design, optimization, folded cascode OTA, g_m/I_D methodology, base band RF application.

I. INTRODUCTION

Microelectronic development since these 30 last years is truly spectacular. This success results mainly of a knowledge-make and a technological master of a fundamental element: the silicon. The MOS transistor is the principle actor and the vector of this technological development. It is the base of integrated circuit design with large scale of integration. With the passing of years, the complexity of integrated circuit has continuously increased, mainly thanks to the rising performance of MOS transistors new generations. The reduction component sizing is the engine of this race to the performance. Our goal was to design a folded cascode OTA using CMOS process in order to use it in the design of a wide band Sigma Delta analog-to-digital converter. Moreover, we validate the design by some applications.

This paper is organized as follows. An optimum architecture of the folded cascode OTA was introduced in section II and its function was analyzed to extract the circuit performances. Section III describes an approach for designing this OTA, clarifies specific design issues. Section IV presents some applications while section V provides concluding remarks.

II. OPTIMUM TOPOLOGY OTA ARCHITECTURE

Several fundamental issues exist when selecting an optimal architecture for the operational transconductance amplifier. This choice aimed both at large gain and large bandwidth performances.

In order to achieve high gain, the differential telescopic topologies can be used. This topology cascodes both the differential pair transistors and current mirror to increase load resistance (Fig. 1) [1].

The telescopic architecture is a better candidate for a low power consumption and low noise OTA.

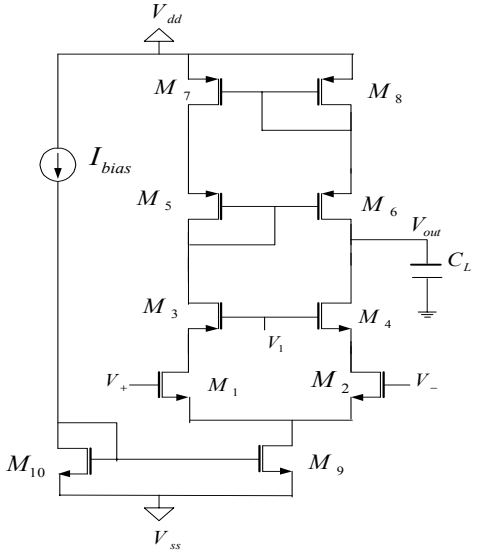

Figure 1. Telescopic OTA

Although, telescopic OTA has a limited input and output swing. In order to alleviate some of the drawbacks of telescopic operational amplifier, a folded cascode OTA based on Wilson mirror can be used.

II.I. Basic configuration CMOS folded cascode OTA

The folded cascode OTA is shown in Fig. 2 [2 - 4]. The name "folded cascode" comes from folding down n-channel cascode active loads of a diff-pair and changing the Mosfets to p-channels. This OTA, like all OTAs, has good PSRR compared to the operational amplifier. To understand the operation of the folded cascode OTA, this last has a differential stage consisting of PMOS transistors M_9 and M_{10} intend to charge Wilson mirror. Mosfets M_{11} and M_{12} provide the DC bias voltages to M_5-M_6-M_7-M_8 transistors. The open-loop voltage gain is given by:

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$$A_v = \frac{g_{m9}\, g_{m4}\, g_{m6}}{I_D^{\,2}\left(g_{m4}\,\lambda_N^{\,2} + g_{m6}\,\lambda_P^{\,2}\right)} \quad (1)$$

Where g_{m9}, g_{m4} and g_{m6} are respectively the transconductances of transistors M_9, M_4 and M_6. I_D is the bias current flowing in Mosfets M_4, M_6, and M_9. Like, C_L is the capacitance at the output node.

λ_N and λ_P are the parameters related to channel length modulation respectively for NMOS and PMOS devices. Taking the complementarity between the transistors M_4 and M_6 into account:

$$gm_4 = gm_6 \quad (2)$$

The gain expression becomes:

$$A_v = \frac{g_{m9}}{I_D}\frac{g_{m4}}{I_D}\left(\frac{1}{\lambda_N^{\,2} + \lambda_P^{\,2}}\right) \quad (3)$$

The unity gain frequency of the OTA is given by the expression:

$$w_u = \frac{g_{m9}}{I_D}\frac{I_D}{C_L} \quad (4)$$

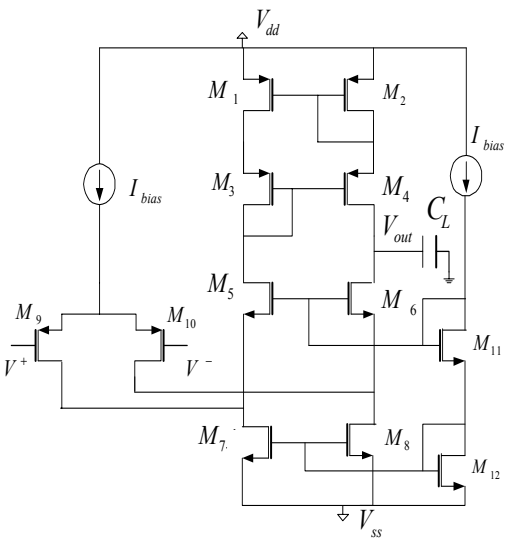

Figure 2. Folded cascode OTA

III. FOLDED CASCODE OTA DESIGN METHODOLOGY

To show folded cascode OTA performances, this paper is interested in OTA design carrying. This design follows a synthesis procedure based on the g_m/I_D methodology [5].

III.1. Sizing algorithm

We present a top-down synthesis methodology for CMOS OTA architectures illustrated by a design plan (Fig. 3) [6]. In fact, this last starts by fixing the specifications to optimize for example: gain and transition frequency in order to determine the unknowns that are MOS devices sizes.

The universal g_m/I_D as a function of I_D/W_L characteristic of the NMOS and PMOS transistors of the CMOS technology under consideration (0.35µm of AMS) is exploited in order to apply the method quoted previously and compute the design parameters from the specifications as a result of top-down synthesis flow.

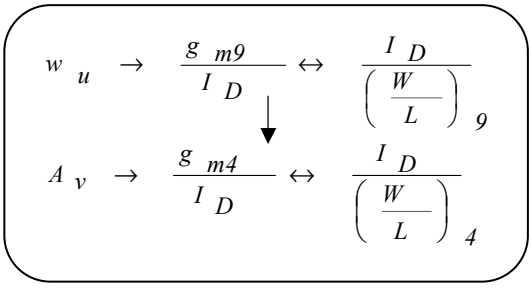

Figure 3. Design plan

III.2. OTA design

We subjected the circuit of fig 2 to specifications schedule presented by table 1.

After applying the design strategy clarified previously, we obtained the parameters computed and summarized in table 2.

Table 1. Specifications

Specifications	Values
A_v (dB)	82
f_T (MHz)	340
C_L (pF)	0.1
I_D (µA)	30
$\pm V_{dd}$ (V)	± 2
Channel length (µm)	1

Table 2. Design parameters

Parameters	Values
$g_{m\ 9,10}/I_D$ (V^{-1})	8
$I_D/(W/L)_{9,10}$ (µA)	0.86
$g_{m\ 4}/I_D$ (V^{-1})	6
$I_D/(W/L)_4$ (µA)	1.65
$W_{9,10}$ (µm)	35
$W_{1,2,3,4}$ (µm)	18
$W_{5,6,7,8,11,12}$ (µm)	6

The designed folded cascode OTA was biased at 2V power supply voltage using CMOS technology of 0.35 µm of AMS with the BSIM3V3 MOSFET model.

The circuit denotes an offset voltage of 1mV, a Slew Rate of 104V/µs, an input common-mode range of ± 1.9V and an output common-mode range between 1.9V and -1.4V. Moreover, our device is able to achieve a higher DC gain of 85dB and a wide bandwidth of 332 MHz with phase margin of 46 degrees (Fig.4). Its transconductance is about of 0.24mS (Fig .5).

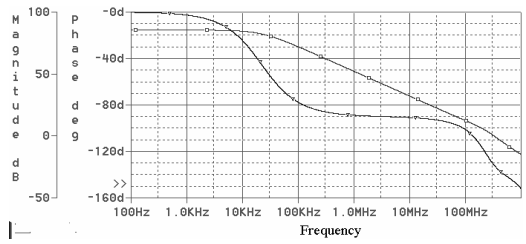

Figure 4. Phase/magnitude response of the OTA

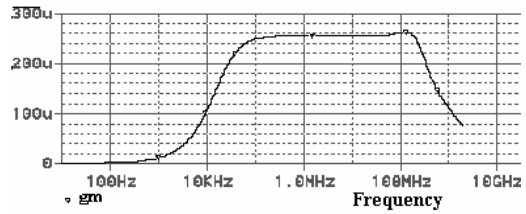

Figure 5. Transconductance curve

III.3. Improved OTA design

Since the folded cascode OTA based on Wilson mirror has a limited output swing, we attempt to solve this problem. So, we propose to improve the current mirror (Fig.6). For the folded cascode OTA using a Wilson mirror, the maximum output voltage is set lower than: $V_{dd}+V_T+2V_{ds,sat}$, so, we use cascode mirror in order to restore this fall to $+2V_{ds,sat}$. The improved circuit yield to specifications schedule presented by table 1 follows the same design strategy explained previously; we obtain the same transistors sizes of the last circuit.

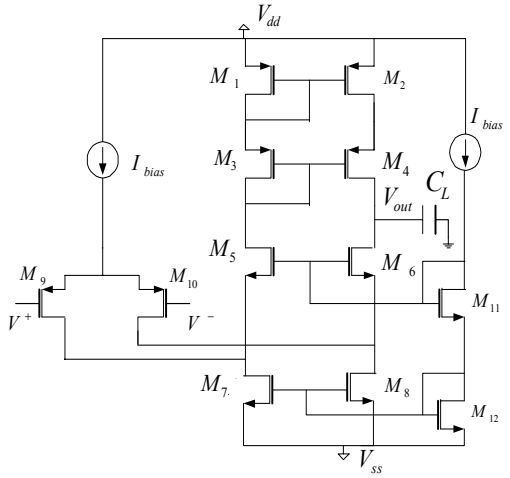

Figure 6. Folded cascode OTA improved

The simulated circuit has a 85dB DC gain and a transition frequency of 230MHz. The degradation of the bandwidth was due to the first pole weakening of the OTA without increasing the DC gain.

Furthermore, the circuit illustrates an offset voltage of 0.1mV, an output and input common-mode range near of $\pm V_{dd}$, and a Slew Rate of 100V/µs. The common-mode and the power supply rejections took the same values found for the circuit based on Wilson mirror. Folded cascode OTA specifications are listed in table 3.

Table 3. Folded cascode OTA specifications

Specifications (C_{Load} = 0.1pF)	Folded cascode OTA	Folded cascode OTA improved
Gain DC	85 dB	85 dB
GBW	332 MHz	230 MHz
Phase margin	46 deg	46 deg
CMRR	164 dB	164 dB
PSRR p, n	85 dB	85 dB
Offset voltage	1 mV	0.1 mV
Output swing	[-1.9 V; 1.4 V]	[-1.9 V; 1.85 V]
Input swing	±1.9 V	±1.9 V
Slew Rate	±104 V/µs	±100 V/µs
Supply voltage	2 V	2 V
Input noise specter density	1.7 µV/$\sqrt{H}$	1.7 µV/$\sqrt{H}$
Output noise specter density	35 mV/$\sqrt{H}$	35 mV/$\sqrt{H}$

IV. APPLICATIONS

To demonstrate the feasibility and the performance of folded cascode OTA, we simulated several applications. We have treated current mode and voltage mode filters. Recently, analog filters design using G_m-C integrators has acquired a great popularity. Tranconductance cells are relatively simple circuits which allow to operate for high frequencies.

The ideal OTA has the properties: the differential input-voltage is bypassed directly to the conductance g_m, where the output current becomes $i_{out} = g_m (V_{in}^+ - V_{in}^-)$. Let's consider the OTA-C filter circuit shown in figure 7, which works in current mode. In figure 8, it is shown the equivalent circuit of the OTA-C filter.

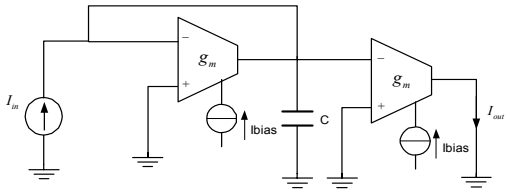

Figure 7. OTA-C filter working in current mode

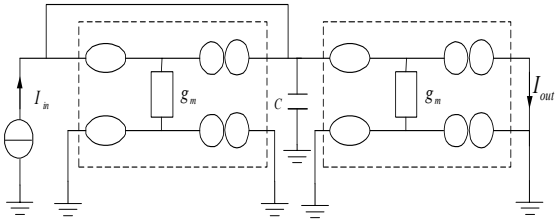

Figure 8. Equivalent circuit for the OTA-C

The computation of the symbolic transfer function has the following relation ship:

$$\frac{I_{out}}{I_{in}} = \frac{1}{1 + p\left(C \frac{1}{g_m}\right)} \quad (5)$$

From the last equation, we represent the transfer characteristic for the filter, using MAPLE tool.

The low pass filter approximated by eq 5 has a cut frequency of around 140MHz; as shown in figure 9. In order to check the filter transfer characteristic, as well as its cut frequency, we simulate the circuit working in current mode on PSPICE simulator. This is depicted in figure 10 for a cut frequency of 110MHz.

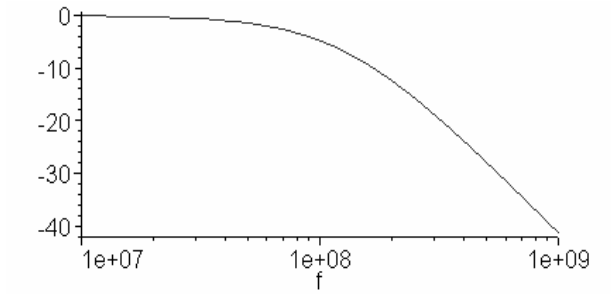

Figure 9. Characteristic of the filter

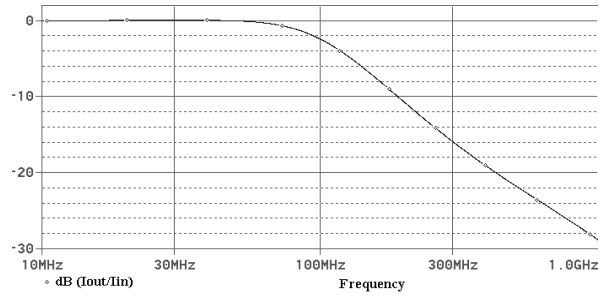

Figure 10. Magnitude response of the filter

Compared to figure 9, we obtained the same curve; nevertheless, the two frequencies are different. Likewise, the OTA-C filter working in voltage mode (Fig. 11) presents the circuit equivalent in figure 12.

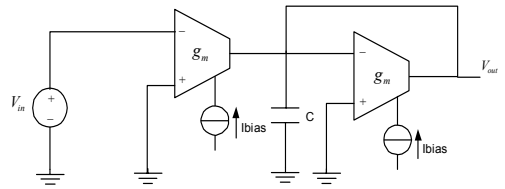

Figure 11. OTA-C filter working in voltage mode

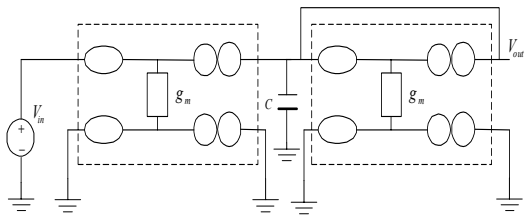

Figure 12. Equivalent circuit for the OTA-C

Its transfer function is given by:

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 + p\left(C \frac{1}{g_m}\right)} \qquad (6)$$

As one sees, both transfer functions in voltage and current mode are similar, so, MAPLE provides the same frequency behavior for each kind of filter.

For the same target mentioned previously, the cut frequency shown in figure 13 is 130MHz. Simulation results lead us to conclude about the dynamic performances abasement.

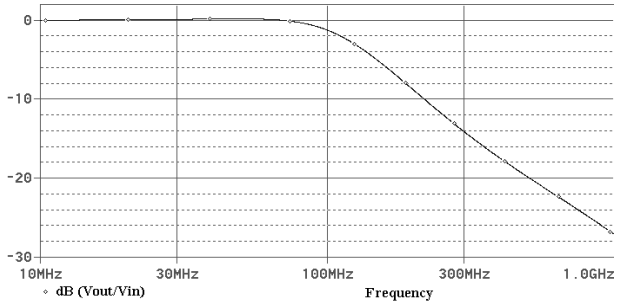

Figure 13. Magnitude response of the filter

V. CONCLUSIONS

This contribution presents an efficient methodology for OTA design, so, the goal to reach high gain and large bandwidth has been fulfilled. Therefore, it has been shown that folded cascode OTA based on Wilson mirror points out a wide transition frequency escorted of output swing limitation. We mention here OTA dynamic performances abasement due to the use of parameters with different values compared to those forecasted since OTA design.

Future work would involve the search of low-consumption and low-supply voltage structure, an update to nano technology-process and Sigma Delta modulator design application

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