# Design and Implementation of CMOS Rail-to-Rail Operational Amplifiers

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***Abstract*–The paper presents the design and implementation of six operational amplifiers with rail-to-rail input and output capability. The study characterizes several rail-to-rail input and output stages and the dependence of the op-amp's operation on different design parameters to formulate a standard design methodology that can serve as a guide for future researches and projects in the area of rail-to-rail amplifiers. The report shows the effects of the rail-to-rail stages on the op-amp's input common-mode range and output voltage swing range. The op-amps are implemented in 0.25um CMOS process and the simulation results achieve specifications such as gain, bandwidth, offset voltages and common-mode rejection ratio comparable with commercially available circuits.**

## I. Introduction

Rail-to-rail operational amplifiers allow signals to swing from the negative supply rail to the positive supply rail. Rail-to-rail operation is a realization of ideal op-amps, providing the entire voltage range as mode for normal operation.

Input common-mode voltage specifies the range of input for which normal operation is assured. Output voltage swing is defined as the range of maximum negative to positive peak output voltage without waveform clipping [1]. By making this voltage ranges approach the supply rails as close as possible, we maximize the operating region of the amplifier. Rail-to-rail high-swing op-amps have highly linear response when used as buffer or voltage-follower [2].

Rail-to-rail operation is based on the op-amp topology. The rail-to-rail input stage allows the op-amp to operate with input voltages near the voltage supply rails. The output stage minimizes the voltage drops at the output to achieve high swing. This study builds upon the basic knowledge on rail-to-rail op-amps and focuses on designing the circuits from several input and output blocks to attain target specifications.

Section 2 and section 3 of this paper presents the input stages and output stages characterized for the rail-to-rail amplifiers, respectively. The schematic design of the six op-amps designed is discussed in section 4. The layout implementation is presented in section 5. Section 6 presents the simulation results and the conclusions and recommendations are summarized in section 7.

## II. Rail-to-Rail Input Stage

Traditional input stages for differential op-amps consist of either PMOS differential input pairs or NMOS differential input pairs. Using PMOS transistors in the input terminals allows the input voltage to operate near the negative supply rail although it is off near the positive supply. In contrast with PMOS, NMOS differential input pairs operate near the positive rail [3].

Parallel-connected PMOS and NMOS differential stage achieves operating mode at both rails by combining the benefits of both configurations. At least one of the differential inputs is still active at either rail, and the input common-mode voltage includes both power supply rails [4]. Two load variations are implemented for the input stage in this study as presented below.

### *A. Complementary Differential Pair with Active Load*

This topology is based on a differential pair with an active current mirror load. The effect of the active load is to realize a single-ended output for both NMOS and PMOS pairs. Each output is then connected as inputs to a push-pull inverter stage as shown in Fig. 1.

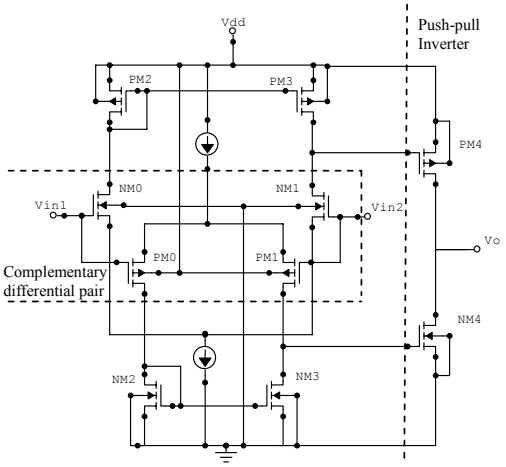


Fig. 1. Complementary differential pair with active load

The output of the NMOS pair biases the PMOS in the push-pull inverter and the PMOS pair biases the NMOS. This push-pull inverter stage integrates the outputs of the previous stage into a single output.

The Comdiff-Act (Complementary differential pair w/ active load) topology uses less transistors and less biasing network compared to the input stage with cascode load. Consequently, the fewer branches consume lower supply current for this topology. However, with the addition of an output stage after the push-pull inverter, the multiple stages lead to an issue of op-amp stability and compensation.



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*B. Complementary Differential Pair with Cascode Load*

The topology shown in Fig. 2 is based on the folded-cascode op-amp with a PMOS differential pair and NMOS cascode load. As a shorthand notation for this project, this topology is referred to as Comdiff-CascPN. Another implementation of the cascode load is based on the folded-cascode op-amp with an NMOS differential pair and a PMOS cascode load, referred to here as Comdiff-CascNP.

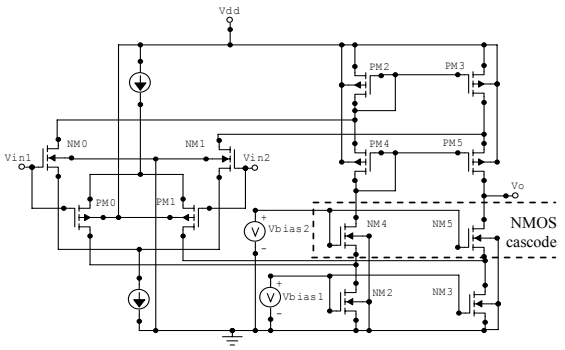


Fig. 2. Complementary differential pair with NMOS cascode load

Having more transistors compared to the input stage with active load, this topology is more complex but could also offer more flexibility in design. The topology has fewer stages making op-amp compensation for stability manageable.

## III. Rail-to-Rail Output Stage

The rail-to-rail output stage minimizes voltage drops at the output branch allowing the output to reach the rails. The output stage also increases the op-amp's voltage gain. Two output stages are characterized and implemented in this study.

*A. Push-pull Inverter Output Stage*

This configuration, also known as complementary common-source output stage, uses a common-source NMOS and PMOS connected at the drain as shown in Fig. 3. It is called the push-pull inverter output stage due to the behavior of the topology with each device conducting for alternate half-cycles at the input [5].

The push-pull inverter output stage uses only two transistors. The bias of this stage is the voltage output from the previous stage. It is therefore important to ensure that both transistors are at the saturation region at this voltage.

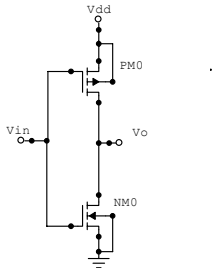


Fig. 3. Push-pull inverter output stage

Since there is no current bias network, the current in the output branch is dependent on the size of the transistors. This could lead to a limitation in the design of the transistor sizes to meet all the requirements such as the gain, the offset operating point and the current supply for this output stage.

*B. Common-source Output Stage*

This is a commonly used op-amp output stage composed of a common-source amplifier with a current driver. The implementation can either be a common-source PMOS, with an NMOS current mirror load shown or a common-source NMOS, with a PMOS current mirror load shown in Fig. 4.

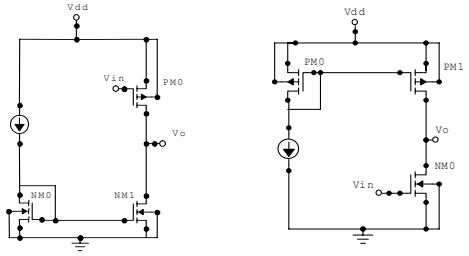


Fig. 4. Common-source output stage: (a) PMOS; (b) NMOS

The current source is mirrored to provide the current bias for the common-source transistor. The supply current consumption of the common-source output stage is therefore more controllable compared to the push-pull inverter.

## IV. Schematic Design

Initial sizes and bias are set and hand-calculated using the MOS current equation in the saturation region. The gm/Id efficiency of the transistors is targeted to 10 and the corresponding width over length ratios (W/L) are calculated depending on the current flow in the different branches. A single length is employed for all transistors to provide ease in the layout implementation. To maximize the output swing of the op-amp, the differential-mode voltage gain is targeted to be in the mega ($10^6$) range. The target is 30,000 for the input stage and 50 for the output stage. Aside from rail-to-rail input and output operation requirement, other constraints are set to achieve high-quality circuits. The design requires a maximum supply current of 250uA, input offset voltage less than 1mV and unity-gain bandwidth greater than 100 kHz.

Six circuits are implemented from the combination of the 3 input stages, (complementary differential pair with active load, NMOS cascode load and PMOS cascode load) and 2 output stages (common-source and push-pull inverter). Two of the circuit designs are detailed below. The others follow a similar design pattern with different combinations of the input and output stages.

*A. Comdiff-Act with common-source output stage*

The input stage requires no further adjustments to the sizes and bias based on the hand calculations to achieve the target

gain of the circuit. Transistors are grouped into pairs and implemented with equal ratios to reduce mismatches.

The tail current source of the complementary differential pair is set to 20uA. The push-pull inverter in the input stage is sized to pass a current of 10uA. The low current in this branch gives the input stage of the topology a gain around 36k.

To minimize the current consumption, the currents on the tail sources are generated using only one current bias network. To minimize the area of the amplifier in the layout implementation, the resistor for biasing is realized using a properly-sized diode-connected transistor. Since the six topologies in this project are implemented with 20uA tail current sources, all use the same current bias network.

There are two main considerations for the design of the common-source output stage. First is the operating point. The output voltage of the previous stage is the input to this stage. A PMOS common-source is implemented instead of an NMOS because the operating point required is nearer to the normal operating points of a PMOS common-source than an NMOS. This inference is based on the characterization done on the common-source output stage. The ideal current source for the bias of the common-source output stage is realized using transistors. Two identical diode-connected transistors are used because a single transistor must have a width smaller than its length to generate the required current.

The multiple stages of the op-amp make it unstable and therefore compensation is necessary. A lead compensation network using a lead resistor in series with a compensating capacitor is used to compensate the instability of the op-amp. However, since this is still insufficient, mirror-pole compensation is done to further stabilize the circuit. The final schematic of the Comdiff-Act with common-source output stage is shown in Fig. 5.

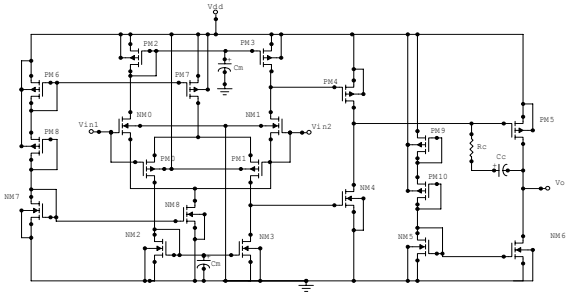


Fig. 5. Final schematic of the *Comdiff-Act* with common-source output stage

### *B. Comdiff-CascPN push-pull output stage*

Initial transistor sizes, bias currents and voltages are set based on the hand calculations. The schematic requires necessary adjustments to achieve the target gain for the circuit and these are directly implemented in the design tool.

The widths of the complementary differential pair are increased to increase the transconductance of the input transistors and improve the gain. The widths of the voltage bias NMOS and the upper current mirror PMOS (NM2, NM3, PM2 and PM3) are decreased resulting in a lower current passing through it. This results in a lower current in the output branch and increased output resistance. The widths of the cascode load and the lower current mirror (NM4, NM5, PM4 and PM5) are increased leading to increased current, both contribute to an increase in their transconductance. Sizes are implemented with all transistors ensured to be operating in the saturation region.

The bias voltages are adjusted to put the transistors at the edge of saturation to further increase the gain. The input stage achieves the 30k target gain. The voltage bias network is implemented using diode-connected transistors.

The main consideration in the design of the push-pull inverter output stage is the operating point. The voltage input of this stage is the output from the previous stage. The second consideration is the supply current of the output stage. Since there is no current bias network, the current is highly dependent on the size of the transistors. Based on the characterization results, to achieve the highest possible gain and still be within the limits of the supply current, the transistor sizes are maximized.

The compensation network of this topology uses the lead compensation network with lead resistor and compensating capacitor. Smaller capacitor values are implemented since the *Comdiff-CascPN* input stage topology has fewer stages compared to the *Comdiff-Act* input stage. The final schematic is shown in Fig. 6.

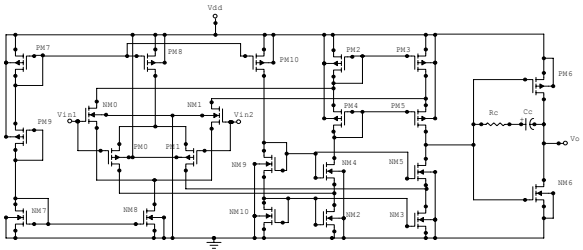


Fig. 6. Final schematic of the *Comdiff-CascPN* with push-pull inverter output stage

## V. LAYOUT IMPLEMENTATION

For the layout implementation, several analog CMOS IC layout techniques are implemented to generate high quality circuits [6], [7]. The pair groupings of the transistors are maintained and the pairs are multifingered and interdigitated to avoid mismatches and offsets. Symmetry is employed in the layout to lessen sensitivity to process variations. Dummy transistors are used at the end of the rows to improve matching by providing the same boundary conditions for the transistors in the circuit operation. Matching improves common-mode rejection and supply noise rejection. Guard rings are implemented as close as possible around the transistors for isolation. A consistent routing direction is used in the connections for clearer and uniform implementation.

Routing within the circuit is minimized to avoid parasitics between metals and active devices.

The lead resistor for the compensation network is implemented using polysilicon in multi-finger configuration which provides fairly accurate resistance and matching.

The vertical parallel-plate capacitor using metal layers is chosen for the compensating capacitor implementation because of the relative simplicity in implementation and high capacitance density.

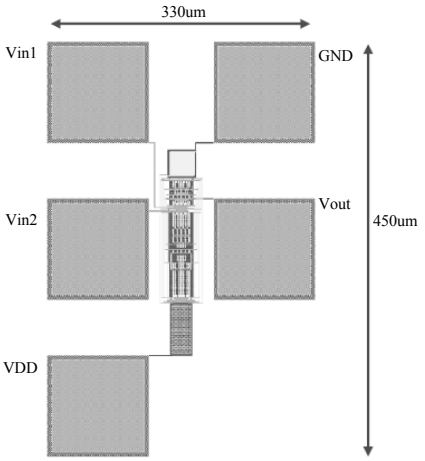


Fig. 7. Layout of *Comdiff-CascPN* and push-pull inverter output stage with probe pads

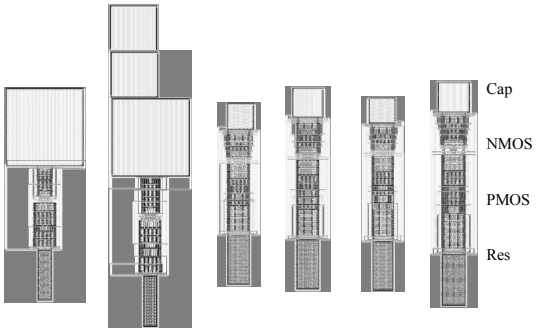


Fig. 8. Layout of six rail-to-rail op-amps

The layout of the six rail-to-rail op-amps are shown in Fig. 8 with relative sizes to each other. It is evident that the C*omdiff-Act* topologies have larger areas since larger compensating capacitors are used.

## VI. Simulation Results

The design constraints for the op-amps are achieved for the six rail-to-rail op-amps except for some target specifications due to limitations of the common-source output stage topology. Rail-to-rail operation is observed for the topologies implemented. The op-amps are implemented in 0.25um CMOS process and simulated using *CADENCE Design Systems Software*. A single supply of 2.5V is employed.

The op-amps with push-pull inverter output stage have higher gain than those using a common-source output stage as shown in Fig. 9. The gain of the common-source output stage was sacrificed so that its operating point matches the output of the rail-to-rail input stage.

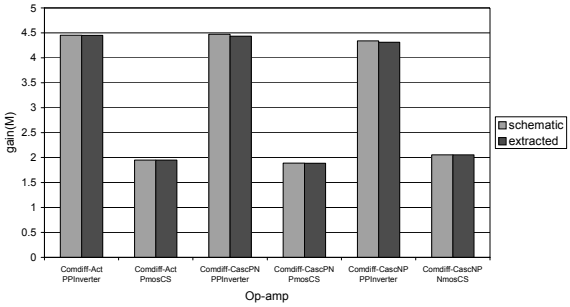


Fig. 9. Differential-mode voltage gain comparisons

The OVSR and ICMR of the op-amps with common-source output stage is relatively far from one of the supply rails as shown in Fig. 10 and Fig. 11. This is due to the fact that the active load of the common-source output stage causes a voltage drop on the output. Consequently, the input offset voltage of these op-amps is larger than those with a push-pull inverter output stage.

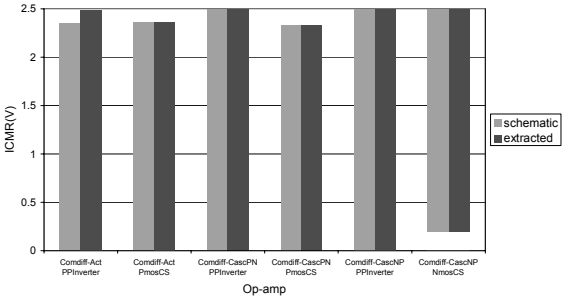


Fig. 10. ICMR comparisons

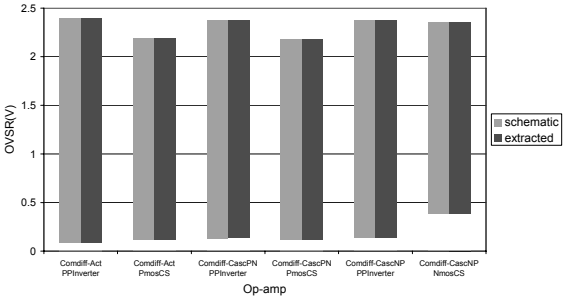


Fig. 11. OVSR comparisons

The multiple stages of the op-amps using complementary differential pair with active load results in lower phase margin as shown Fig. 12. The topology requires larger compensation for stability of operation.

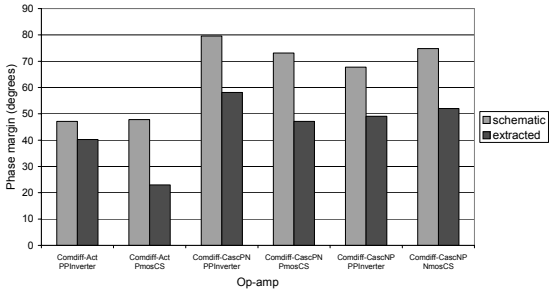


Fig. 12. Phase-margin comparisons

The extracted layouts performed closely to the schematic design in terms of DC parameters with about 1% error. AC parameters declined due to parasitic resistance and capacitance unavoidably present in the layout. Phase margin decreased by an average of 20 degrees and unity-gain bandwidth decreased by 20%. Transient parameters decreased by an average of 15% for the six circuits which can also be attributed to the op-amps degraded response to high frequency components of input signals. Table 1 summarizes the parameters of the op-amp topologies acquired from the tests performed on the extracted layouts.

Fig. 13 and Fig. 14 displays the ICMR and a sample input and output waveform for a voltage follower configuration for the Complementary differential pair with NMOS cascode load input stage and push-pull inverter output stage.

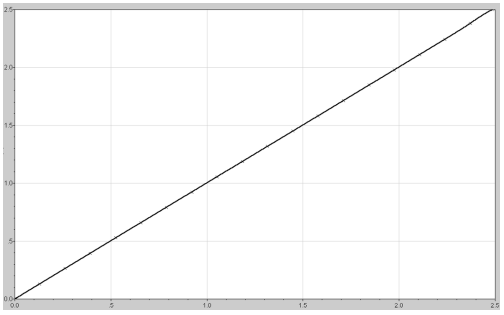

Fig. 13. ICMR of the Op-amp

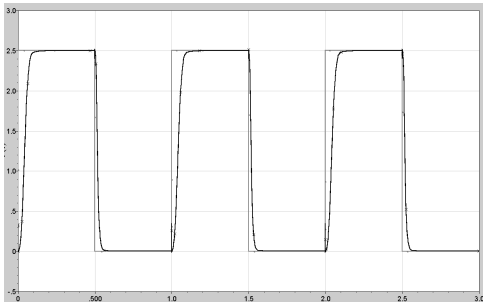

Fig. 14. Input and output waveform

## VII. Conclusions and Recommendations

It is verified that rail-to-rail input and output stages are necessary for rail-to-rail input and output operation. Through characterization of the rail-to-rail input and output stages, a standard design methodology is formulated for the different topologies. It is also significant to consider layout issues during schematic design to aid in achieving high quality circuits.

Table I
Summary of Op-amp Specifications

| Op-amp topology | Comdiff-Act PP inverter | Comdiff-Act PMOS CS | Comdiff-CascPN PP inverter | Comdiff-CascPN PMOS CS | Comdiff-CascNP PP inverter | Comdiff-CascNP NMOS CS |
|---|---|---|---|---|---|---|
| $A_{V,dmMAX}$ | 4.45M | 1.95M | 4.435M | 1.887M | 4.312M | 2.0567M |
| $V_{ID}$ @ $A_{V,dmMAX}$ | -3.395uV | -3.63uV | 11.215uV | 11.36uV | -2.445uV | -2.145uV |
| OVSR @ $A_V$=20k | 84.28mV to $V_{DD}$ – 109mV | 105.76mV to $V_{DD}$ – 314mV | 125.4mV to $V_{DD}$ – 126mV | 114.61mV to $V_{DD}$ – 322mV | 130mV to $V_{DD}$ – 127mV | 379.9mV to $V_{DD}$ – 143mV |
| ICMR (90%) | 6.55mV to $V_{DD}$ – 18mV | 6.684mV to $V_{DD}$ – 137mV | 0.4984mV to $V_{DD}$ – 5.1mV | 0.5428mV to $V_{DD}$ – 166mV | 1.233mV to $V_{DD}$ – 1.5mV | 194.58mV to $V_{DD}$ – 1.6mV |
| Input offset voltage | -0.781mV | -4.189mV | 0.0192mV | -4.256mV | -0.0047mV | 6.222mV |
| $I_{SUPPLY}$ | 226.29uA | 239.21uA | 237.353uA | 236.93uA | 246.506uA | 242.03uA |
| $A_{V,cm}$ | 1.434 | 1.009 | 3.9m | 2.196m | 21.5m | 18.6m |
| CMRR | 129.84 dB | 125.72 dB | 181.12 dB | 176.22 dB | 165.7 dB | 160.87 dB |
| Phase margin | 40.24° | 23° | 58.091° | 47.155° | 49.096° | 52.018° |
| Unity GB | 101.72MHz | 51.723MHz | 87.201MHz | 64.675MHz | 115.04MHz | 87.494MHz |
| PSRR @ 60Hz | 96.413 dB | 114.05 dB | 118.13 dB | 97.738 dB | 114.38 dB | 101.78 dB |
| Settling Time | 671.17 ns | 524.46 ns | 544.91 ns | 557.82 ns | 523.46 ns | 530.77 ns |
| Slew Rate | 144.32 V/us | 87.459 V/us | 43.465 V/us | 33.972 V/us | 95.606 V/us | 68.34 V/us |

The multiple stages of the op-amps lead to a stability issue which should be a main design consideration since passive components for the compensation network consumes a large amount of chip space.

Among the rail-to-rail topologies implemented in the study, several rail-to-rail stages are more recommended. The complementary differential pair with cascode load input stage is recommended because it has less stability issues. Furthermore, it is recommended to use the push-pull inverter output stage since its required input for maximum gain is close to the output of the rail-to-rail input stages. It also does not limit the output voltage swing range of the op-amp.

The design and implementation presented in the study can be succeeded by future works focusing on improving performance through incorporating op-amp topology design optimizations such as constant transconductance biases and several others presented by related works. Also, many other different implementations of rail-to-rail op-amps are worth including in future characterizations, comparisons, design and implementation.

## ACKNOWLEDGMENT

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