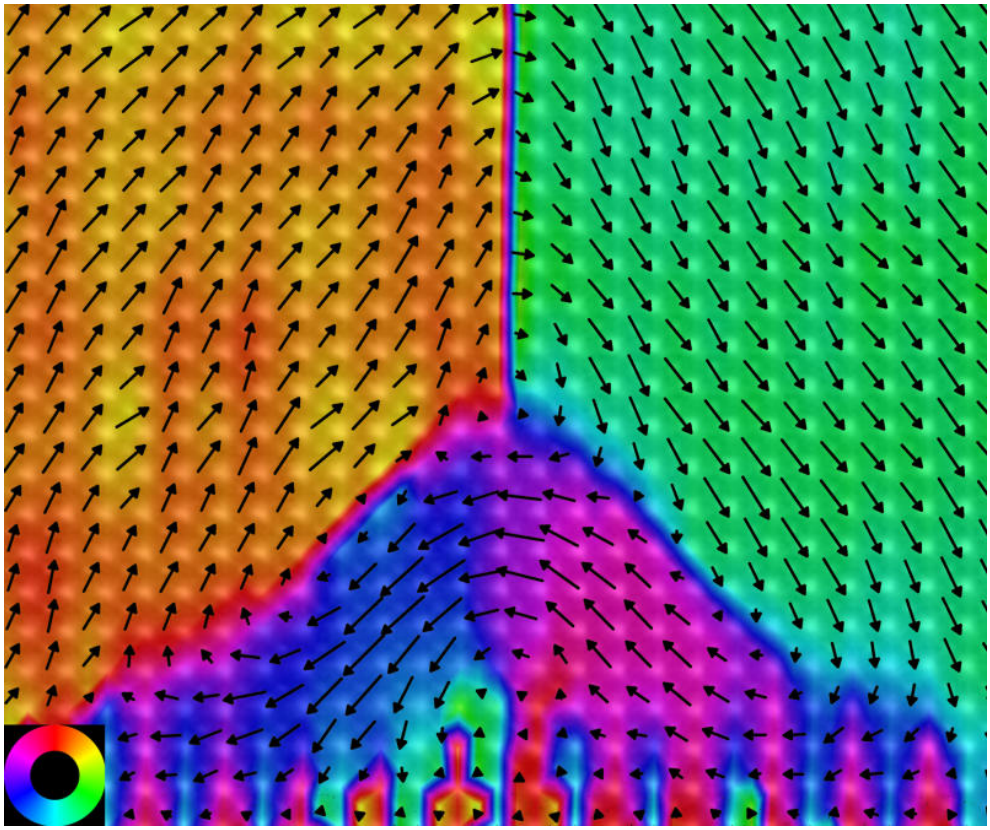
Ferroelectric Memory Devices

How to store the information of the future?



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Abstract

Now that we entered the age of information technology, storage is one of the key issues. Upon scaling down and lowering the operating voltage, FLASH will no longer work. In this paper one of the alternatives is being reviewed; ferroelectric memory devices. Ferroelectrics show non-volatility and can operate at low voltage thresholds. Ferroelectricity shows a P-V hysteresis on which the two level logic scheme of a memory device can be based. PZT and BST are among the materials already in use as prototypes. Ferroelectricity is believed to be preserved down to several unit cells and this makes ferroelectric materials interesting for nanoscience. However at low thickness depolarizing fields and strain come into play. Ferroelectrics can be used as capacitors and field-effect-transistors. The FeRAM shows fast writing and low-power consumption. However the read-out is destructive which leads to high fatigue. FeFETRAM does not show this problem, but no materials have yet been found with retention times higher than a couple of days. Comparing these devices with other memory technologies, FeRAM and FeFETRAM are still lacking behind on capacity and high density arrays. However their writing speed is faster and they are low-power consuming. Economically speaking they can be very productive. In order for ferroelectric devices to become the storage technology of the future adequate knowledge, good design models and the ongoing search for materials with better properties is required.

Frontpage picture: mapping of polarization on an atomic scale[1]. Spontaneous small-size nano-vortices were found to occur at ferroelectric hetero interfaces of $BiFeO_3$. Image comes from a sub-angstrom resolution transmission electron microscope[2].

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Introduction

Can you imagine; your entire movie-collection or library on a single memory device? Now that we entered the age of information technology, storage is one of the key issues. For over 45 years Moore's law has been the driving force behind the memory chip market, which is estimated at 20-30 billion a year. The number of transistors on a chip is expected to double approximately every two years, while costs are decreased and functionality and performance improved. Due to the invention of integrated circuits this trend was maintained but physical limitations are expected to be reached in the near future. The key is to look beyond the current complementary metal-oxide semiconductor (CMOS) materials, since miniturazing the devices will not do the trick. Besides the electronic industry has agreed on decreasing the Si-logic level from 5V, 3.3V, 1.1V to 0.5V. Current FLASH memory will not work at the 0.5V operation voltage, also when charge pumps are inserted.

Therefore new materials and functionalities are searched to be integrated within the current CMOS process flow or which can act as standalone memory devices. A high storage density and signal-to-noise ratio are the essential characteristics; however the reliability, costs, fatigue and fast reading and writing the problems to overcome. Nowadays several options exists. One of them exploits the characteristics of ferroelectrics. Ferroelectrics show non-volatility and their thin film devices can operate at low voltagetresholds. Fuijtsu even incorporated a 32kbit ferroelectric memory device in the SONY playstation 2. Currently also nano-ferroelectrics are considered for device applications as well as multiferroics. Looking at Moore's law it will be those nano memory devices which will become important in the near future. Perhaps even one day the dream of Feynman will come true, and we will be able to write the entire Encyclopedia Britannica on the head of a pin.

In this paper the phenomena of ferroelectricity is discussed and the memory devices based on it. Our aim is to give an overview of the physics behind it, so that one can understand the current research performed on thin film ferroelectric and nano-ferroelectric memory devices. Within the field of nanoscience, ferroelectric devices are not only of special interest because of their possible industrial applications but also to study the phenomena of ferrroelectricity itself, especially when scaling down. Because of this interest, this topic was selected and reviewed in this paper.

0.1 Outline

In chapter 1 a theoretical background about ferroelectricity is given. Mainly answering the question what is ferroelectricity and what are the origin and characteristics of this phenomena. Also the different ferroelectric material classes are introduced with a focus on thin films. For a more thorough study of structural phase transitions and ferroelectricity concepts the reader is referred the textbooks such as that of Lines and Glass [3] and a modern variant by Rabe et al[4]. Chapter 2 discusses the physics of memory devices with an emphasize on ferroelectric memories. This is followed by discussing competing memory technologies, such as DRAM and MRAM. Finally in chapter 3 an outlook is given on future innovations with regards to scaling down ferroelectric memory devices and a new type of materials; multiferroics.

Chapter 1

Ferroelectricity

1.1 Historical Overview

Ferroelectricity was first discovered by Valasek[5] in 1920. He found that the polarization of sodium potassium tartrate tetrahydrate ($NaKC_4H_4O_6.4H_2O$), better known as Rochelle salt, could be reversed by the application of an external electric field. A hysteresis effect, which is characteristic for ferroelectricty, was seen and switching between the two different polarized states was possible. However for two decays this discovery and that of the same phenomena in the KDP series[6] was considered as mere artifact. Only in 1949 the ferroelectric research field emerged, due to the discovery of ferroelectricity in ceramics ($BaTiO_3$). It belonged to what was soon to become the biggest class of ferroelectrics: perovskite oxides[7], with general formula BO_6. This falsified the assumption that hydrogen bonds were essential for ferroelectricity. Now over more than 700 ferroelectrics have been found, most of them not hydrogen bounded or oxide.

Another assumption that needed to be falsified was the critical size. Up until the 90s ferroelectricity was believed to be destroyed below 10nm. But measurements on PZT films, showed switchable polarization down to thicknesses of a few nanometer[8]. Also theoretical predictions showed that PbTiO3 will maintain a switchable spontaneous polarization down to three unit cells as long as the depolarization field was fully compensated[9]. In 1948 the first device was made [10], but it took some years before the field of ferroelectric memory devices flourished. Especially because it required techniques which could make thin films. Bulk ferroelectrics need coercive fields of 50kv are needed for reversing their polarization while below the submicronmeter scale the silicon level of 5V can be reached. So when deposition techniques enabled the making of thin films this lead to the integration of ferroelectric material in silicon chips. Current research on these integrated ferroelectrics involve finite size effects, interfaces and strain.

The name ferroelectricty is a reference to the earlier discovered ferromagnetism. Analogy can be found between the electric properties of ferroelectrics and the magnetic properties of ferromagnets. However were mechanical coupling can be neglected in ferromagnets this is not the case for ferroelectrics. Ferroelectricty arises because of strain and displacement of charge. While ferromagnetism is a reordering of the spinstates of the electrons.

1.2 Characteristics

A material is ferroelectric when it has two distinct polarization states, which can be maintain in the absence of an electric field and between which one can switch by applying an electric field. Key in defining whether a material is ferroelectric is the experimental set-up, since one must be able to determine the switching even when a small difference is observed. For most known ferroelectrics the onset of ferroelectricity occurs as a function of decreasing temperature. It is a structural phase transition and the transition can be either displacive or order-disorder in nature. Displacive transitions involve a small distortion of the bonds between the atoms, while

in order-disorder transition the atoms rearrange from a random occupation of the lattice sites to specific define ones for each atomtype.

The order parameter for ferroelectrics is the spontaneous polarization which is caused by the atomic arrangement of ions in the crystal structure. This can either depend on the position of the ions (conventional ferroelectrics) or on the charge ordering of multiple valences (electronic ferroelectrics). A polar displacement of the atoms in an unit cell results in ferroelectricity. These displacements might be coupled to strain or other nonpolar atomic displacements. Thus ferroelectric crystals need a polar space group. Also their structure should have several polar variants with discrete states of polarization. The latter is ensured by the principle that a ferroelectric crystal structure is a small symmetry-breaking distortion of a higher-symmetry reference state, called the paraelectric state.

At the critical temperature (T_c) the material transits from the ferroelectric state to the nonpolar paraelectric phase upon increasing temperature. However sometimes the ferroelectric breakdowns before its transition temperature is reached and no paraelectric state is found. Ferroelectric transitions can be characterized by phonon spectroscopy. X-ray and neutron diffraction can be used to get the crystal structure of the material and determine its polarization switching origin.

Most of the ferroelectric transitions are second order and can be described by Landau theory. With help of the Lyddane-Sachs-Teller relation the link is made with the vanishing frequency of a polar mode. This lead to the theoretical description of ferroelectricity which is given by the so-called soft-mode description[11]. Upon cooling a material from above the transition temperature, a normal mode of vibration of the crystal decreases to zero frequency. Hence a ferroelectric transition can usually be associated with the condensation of a soft (or low-frequency) mode. This condensation distorts the crystal structure and leads to the appearance of a long-range polar order. For this transition the anharmonic interaction between the phonos is important. Also polar phonons are temperature dependent, and thus ferroelectricity as well. The distinction between displacive and order-disorder transitions can be made by looking at the dynamics of the transition; whether the soft mode is propagating of diffusing in character.

With aid of this soft-mode concept and the assumption that a ferroelectric state is only a small distortion of a higher-symmetry state, first principle studies can be done. Phonons related to the paraelectric reference structure are computed and the unstable modes used as guides to identify energy-lowering distortions. These models can predict crystal structure and polarization.They are especially of interest for the behavior of ultrathin films, which are build up of a few layers of atoms. Together with experimental structural determinations first principle studies form a powerful way to determine atomic arrangements and electronics states in the crystal on an atomic-scale[12].

Polarization and hysteresis

The appearance of a hysteresis cycle is essential for ferroelectricity. But not all solids with electrical hysteresis are ferroelectric. Hysteresis can have extrinsic causes due to mobile charge defects and pn-junctions. For an ideal ferroelectric the P-E hysteresis loop is symmetric. From it one can define the remanent polarization states and the coercive fields. This coercive field must be lower than the breakdown field of the material, to enable switching. To measure the electric

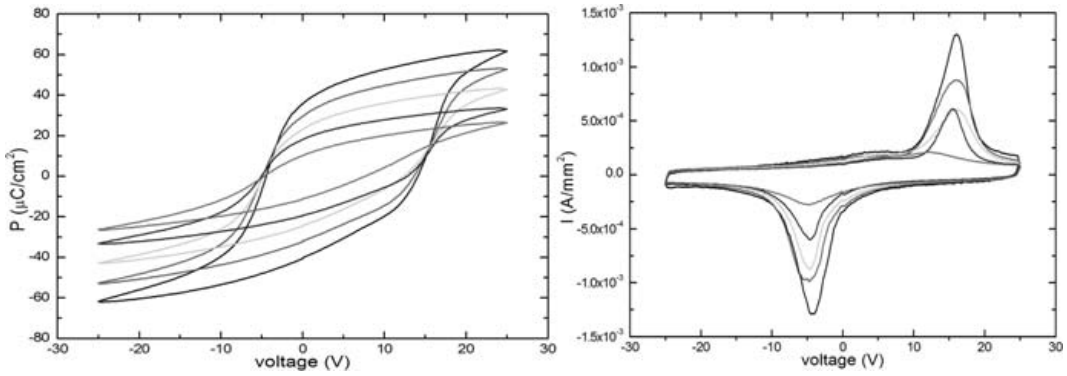

Figure 1.1: a) hysteresis loop for $PbTiO_3/SrTiO_3$ samples with different polarization b) corresponding current-voltage loops[13]

properties of a ferroelectric we need to include it in a device, the simplest one being a capacitor. This device where a ferroelectric is sandwiched between two metal electrodes, is discussed in more detail in chapter 2. This means that in measurements the system as a whole including all its components is involved. So one needs to distinguish between ferroelectric response and electrical responses dominated by the system. For an overview of how measurements with limitless artifacts can be performed the reader is referred to the textbook of Rabe et al [13]. one trick is to vary the frequency since artifacts are usually highly frequency dependent.

In figure 1.1 the P-V hysteresis loop for several $PbTiO_3/SrTiO_3$ samples with different polarizations is visualized. The corresponding I-V characteristic shows clear switching peaks at the coercive voltage, another characteristic of ferroelectricity. From these switching currents the polarization can be determined. For a infinite crystal the polarization is defined as an integrated current though the transformation from one ferroelectric variant to another. By measuring the switched charge/current versus the voltage, one can obtain the P-V hysteris loop and determine the remnant polarization with the aid of integration techniques. Nowadays most of these measurements are carried out by commercial apparatus of Radiant technologies or AixAcct, but previously the Sawyer-Tower circuit was used[14]. For most devices the polarization values and time that the material remains switched are the values of most interest. Also current measurements to determine the leakage current and dielectric permittivity of the device are common.

Domains and Switching

Switching between the two remnant polarization requires the growth and shrinking of domains. Domains occur in materials in order to minimize the depolarizing fields within the material itself. Different regions with the crystal polarization in difference directions are formed and result in a nearly complete compensation of the polarization. Each volume of uniform polarization is called a domain and is defined by domain walls. When an electric field is higher then the coercive fields nucleation of domains and domain wall movement occurs. It is this growth and

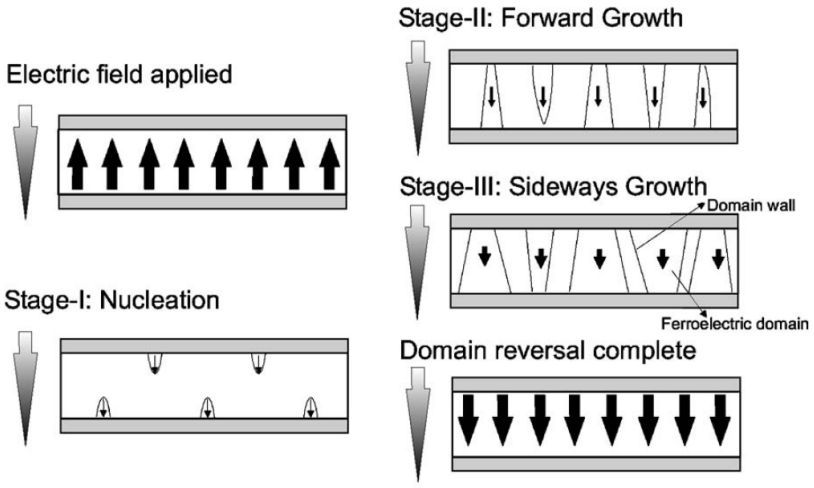

Figure 1.2: Mechanism of domain switching by application of an external field[12]

shrinking of domains which leads to poling; orientation of all domains in the same direction. A polarization state is formed and by applying an opposing high enough field switching can occur to the other polarization variant by the same mechanism (figure1.2). With the aid of Atomic Force Microscopy domain wall motion can be observed. The stages of domain evolution after applying a field are: 1) nucleation of new domains near edges of electrodes, 2)forward growth, 3) plane domain wall motion and 4) stabilization. The nucleation of domains is considered to be random and are ratelimiting for switching in thin films. The driving force behind the growth is the local electric field.

Materials

All ferroelectrics are pyroelectrics and all pyroelectrics are piezoelectric.In pyroelectrics the polarization of the material is changed upon heating, while in piezoelectrics polarization changes upon applying strain. However not all pyro- and piezoelectrics are ferroelectrics. This means that ferroelectrics can not have a center of symmetry nor can they be glasses. Furthermore ferroelectrics need to have a polar space group which can have multiple - at least two - polarization states. The atomic arrangement within the crystal structure lies at the heart of ferroelectricity.

Two main classification can be made depending on whether the transition is displacive or order-disorder. The latter includes those ferroelectric crystals with hydrogen bonds, while the first corresponds to ionic crystal structures. Besides ceramics and the hydrogen bond containing KD_2PO_4 series also electronic ferroelectrics exists. In those materials a symmetry-breaking instability of the electronic ground state, due to multiple valency of the atoms, causes the ferroelectricity, while the ions are kept fixed. Examples are Fe_2BO_4 and $LuFe_2O_4$. But here we will focus on one special class used for thin films applications: the perovskite family.

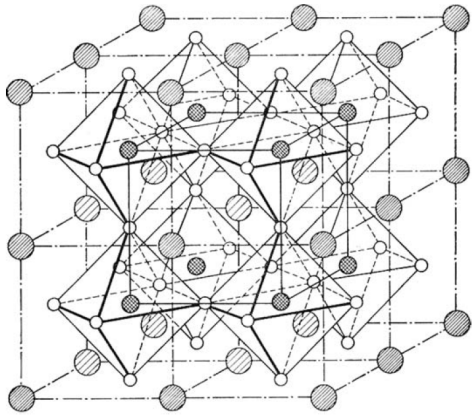

Figure 1.3: Cubic crystal structure of ideal perovskite[13]

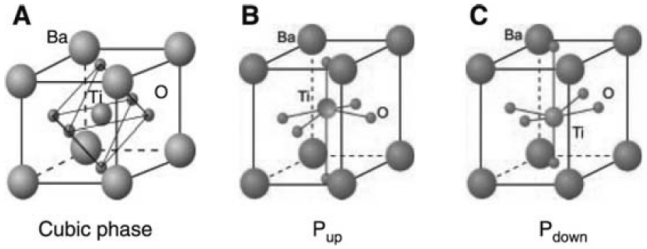

Figure 1.4: Crystal structure of $BaTiO_3$ unit cell. A) Paraelectric cubic phase. B) and C) ferroelectric tetragonal phases with $\pm P$ states[15]

Perovskite Oxides

$BaTiO_3$ was the first to be discovered of this class of ferroelectrics. It consists not only of perovskite compounds but also of ordered- disordered solid solutions such as $Sr/BaTiO_3$. The name comes from the mineral perovskite $CaTiO_3$ and the general formula is ABO_3 with A and B each representing a cation element or mixture of two or more elements. They show a variety in physical properties mainly depending on the composition and cations involved. Changes in strain also influence the ferroelectricity of perovskites. Most perovskites are cubic above Tc and distort below. The transition is weakly first order.

In the ideal case the high-symmetry structure has space group $Pm\bar{3}m$ with a simple cubic lattice and a basis of 5 atoms. B is at the center of an octahedron with 6 oxygens as nearest neighbors. These octahedrons are packed in a simple-cubic network, where the large holes are filled by A atoms. The A atoms have 12 nearest neighbors (figure1.3. Structural frustration of the cubic structure due to misfit of B/A in the holes leads to a small polar distortion.

For example $BaTiO_3$ transforms to a ferroelectric tetragonal phase upon temperature low-

ering and even further to an orthorombic and finally rhomobohedral ferroelectric state. Each ferroelectric structure forms a subgroup of the cubic paraelectric structure. The first transition to the tetragonal state ($P4mm$) is depicted in figure1.4. This state occurs below 393K and is stable until 278 K. It has a polarization of $27\mu C/cm^2$[16]. Each transition in $BaTiO_3$ is accompanied by small atomic displacement, dominated by the displacement of the Ti ion relative to the oxygen octahedron network and a macroscopic strain. Closely related to $BaTiO_3$ is $PbTiO_3$, in which also the Pb atoms contribute to the polar displacement. Not for all perovskites the cubic para electric structure is the right one. In $LiNbO_3$ a trigonal paraelectric structure is formed.

Other examples of the perovskite family are the solid solutions of Lead Zircone Titanate (PZT) with a general formula of ($PbZr_{1-x}Ti_xO_3$). The endpoint is an antiferroelectric state but by adding small amounts of Ti, distortion into two ferroelectric phases occurs. Another special type are are the layered oxide ferroelectrics, such as SBT and the ferroelectric hexagonal manganites YMnO3. The latter also show magnetic properties. Magnetism is produced by Mn cations which are relatively passive in the ferroelectric transition. The layered perovskites are made by a regular stacking of Bi_2O_2 with perovskite building block such as ($SrBi_2Ta_2O_9$) for Strontium Bismuth Tantalate (SBT.

Those perovskites of interest for thin film random access memory are PZT and SBT. Most of the ferroelectric materials are integrated as polycrystalline films, but some are also epitaxially grown on silicon. The properties of Lead Zircone Titanate (PZT) depend strongly on its Ti/Zr composition and its alloys show clear switching and a high polarization. Adding Ti reduces the leakage current, but also reduces the capacitance. Strontium Bismuth Tantalate ($SrBi_2Ta_2O_9$) shows a smaller polarization than PZT but it shows less fatigue. Fatigue is the decrease in the amount of charge switched as a function of switching cycles. However the growing of BZT occurs at higher temperatures and imprint is mores likely to occur. Imprint refers to the tendency of a ferroelectric layer to revert to a preferential polarization direction once it has been switched to the opposite one. The imprint is depending on the growing conditions, temperature and time. PZT films have a polarization axis that can be aligned in several orthogonal directions, while SBT shows a fixed polar axis and random film texture[17].

Size Effects

Scaling down from bulk to thin film ferroelectrics changes the properties of system. Although much of the physics can be derived from bulk, differences can be found. Bulk materials can be considered to be insulating while thin films are semiconducting and are influence by their environment and strain within the material. Strain is imposed by growing the thin films epitaxially on their substrates. When scaling down from thin films to nanoparticles or even dots, most of the bulk physics can still be used. However now we should consider the asymmetry of the environment and the fact that only dynamically a ferroelectric-paraelectric transition can be defined.

It is often hard to distinguish between true size effects from effects that are caused by other factors that change with film thickness which are either extrinsic or processing-related. The nature of size effects depends strongly on the electrical boundary conditions that limit the ferroelectric phase, such as screening charges in the electrodes and depolarizing fields. Sources of

size effects, reviewed in[17], can be the microstructure, domain structure and dynamics, mobile ion defects and Schottky barrier formation between electrode and ferroelectric.

Strain

Spontaneous strain is a universal characteristic of ferroelectrics, since they all are piezoelectric. But when growing thin films strain is also obtained by the lattice mismatch between the film and the substrate and by defects grown within the film. Strain therefore affects the ferroelectric structure and the transition temperature. Unfortunately for the current thin films devices ($120nm$) defect effects can not be ruled out. But when film sizes of twice the critical thickness can be reached, one is able to grown coherent films. Then we will be able to change temperature and polarization by using the right strain, as was shown for epitaxially strained $BaTio_3$ by Choi et al[11]. This means that mechanical boundary conditions for the material can also effect the stability of the ferroelectric phase.

1.3 Applications

Thin film ferroelectrics can be used for non-volatile memory devices. The two-level logic needed for these devices relies on the two remanent polarization states, their non-volatility on the constant the remnant polarization even at zero field. However ferroelectrics can also be used in other applications such as micromechanics (actuators and MEMS) and electro-optics, since their refractive index changes with the voltage applied. These applications mainly rely on the fact that ferroelectrics are also pyro- and piezoelectrics. Furthermore ferroelectrics can also be used for cooling and electron emission[18].

Chapter 2

Device Physics

Memory devices make use of material properties that show hysteresis. Application of an external stimulus is makes it possible to switch between the hysteresis states, while theses states are maintain when no stimulus is applied. In the case of ferroelectrics it is the application of an external field/voltage which enables switching between to polarized states.

Requirements of memory devices are fast reading/writing speed, stability for more than 10^12 writing cycles, retention of data for a least a decade and low fabrication costs. Preferably the material should show no degradation at all. Although ferroelectrics are considered to be non-volatile, it is the retention time that causes most problems, since leakage occurs at interface with electrodes/semiconductors. Most of the ferroelectrics are used as part of an integrated memory device, but ferroelectrics can also be used as standalone high-capacitance non-volatile memory devices. Commercial ferroelectric applications exist but not on a large scale. Samsung for instance has developed a 64MB FeRAM and Toshiba one of 32 MB.

In this chapter the two basic memory device concepts of ferroelectricity are introduced; FeCapacitor and FeFET and their integration into multi-bit memories, FeRAM and FeFETRAM respectively, is discussed.

2.1 FeCapacitor

A ferroelectric capacitor is the simplest device possible to perform electrical measurements on ferroelectrics. It consists of a ferroelectric material sandwiched in between to metal electrodes. In this design interfaces and screening effects come into the picture. With regards to memory applications a ferroelectric capacitor can be used to represent a bit. By applying a high electric field the polarization of the ferroelectric can be switched between $\pm P$. Thus one can write a 1 or 0 corresponding to the different polarization states. To read out your bit a switching voltage is applied, which is higher than the coercive voltage. When the polarization is aligned with the field no switching occurs. However in the other case, the polarization is switched. This leads to a switching charge which is given by the following expression in the case of a semiconductor or lossy dielectric:

$$Q = \sigma AVt/d + 2PA \tag{2.1}$$

Where P is the polarization, A the electrode area, σ the conductivity, V voltage across the capacitor, t the time and d the thickness. This read-out process is destructive, since it changes the polarization of your bit. Afterwards an reset electric field needs to be applied to maintain the initial polarization. From this switched charge (or measured as current) the hysteresis cycle can be obtained. For ideal capacitors $\sigma = 0$ and no leakage should be taken into account[12].

Depolarizing Fields and Critical Thickness

Consider a short-circuited ferroelectric capacitor. The spontaneous polarization of the ferroelectric film is then compensated by the charge residing at the electrode-ferroelectric interface.

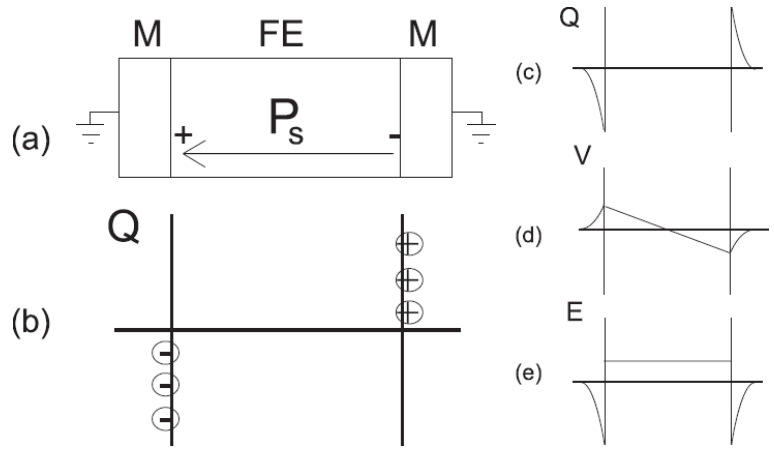

Figure 2.1: A)schematic diagram of a short-circuited ferroelectric capacitor with metal electrodes. B) charge distribution in ideal case and c) for real electrodes. D) and E) show the voltage and the field profiles along the device[19].

Ideally this charge resides on an infinite thin plane and depolarizing fields can be ignored. In that case the coercive field needed to reverse the polarization, increases with decreasing thickness and follows the semi-empirical law $E_c(d) \propto d^{-2/3}$. This law holds for thin films of $100\mu m$ down to $200nm$ and can expanded down to $1nm$ when depolarizing corrections are taken into account[19]. The charge at the interface is then considered to be distributed over a finite small region in the metal and this leads to incomplete charge compensation (screening effect). To maintain the equipotential across the film a depolarizing field is necessary, since the metal electrodes show a voltage drop2.1. This leads to an effective electric field (E_f) in the film which is dependent on the polarization itself according to:

$$E_f = \frac{V + 8\pi P_s a}{d + \epsilon_{f(2a)}} \tag{2.2}$$

Where V is the voltage drop across the total capacitor, d the film thickness, P_s the polarization, $a = \frac{\lambda}{\epsilon_e}$, λ the screening length and ϵ_e and ϵ_f are the dielectric constants of the electrodes and the film, respectively. The thin film is considered to be a perfect insulator.

The measured coercive field $E_c = V/d$ is smaller than the actual field (E_f) for materials were the spontaneous polarization is larger than the dielectric constant of the film. Knowing the dependence of the coercive field on the thickness of the film is of special interest when scaling down memory devices. From the derivation above it can be concluded that devices should preferably be design in the regime where $E_{meas} > E_f$, but before the polarization instability is reached. This point is achieved when the depolarizing field and the real coercive field are equal and determines the minimum film thickness. The critical thickness can be regulated since the coercive field depends on the polarization of the ferroelectric and screening length of the electrodes. These results show that the maximal capacitance ($\propto E_meas$) of the device is limited

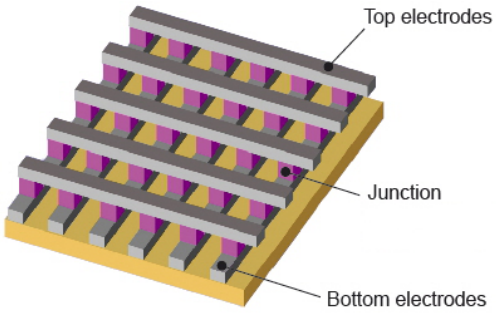

Figure 2.2: Cross bar geometry

by the screening effects of the electrode. So in order to improve the capacitance one should improve the resistivity of the film and screening properties of the electrodes.

2.2 FeRAM

The create a memory one needs to integrate multiple device into a larger array, with each device corresponding to one bit. Although multibit device can exist. In the ferroelectrics, we can thus create memories by making arrays of FeCapacitors or FeFETs. The latter is discussed in the next section.

The simplest way to obtain a ferroelectric Random Ac

$$R = \frac{V}{I} \tag{2.3}$$

$$R = \frac{V}{I} + \frac{dP}{dt} \tag{2.4}$$

Where R is the resistivity, V the voltage, I current and P the polarization.

The major problem of this design is cross-talk. Applying a voltage to one bit, also influences the polarization of its nearest neighbors since there is no sharp threshold voltage for switching. In better designs the capacitors are isolated from one another by means of a pass-gate transistor. Two designs exist: 1T-1C and 2T-2C. The operation principle stays the same; a sufficient strong E-field, bigger than the coercive field of the ferroelectric is applied to write a bit, by changing the polarization state. The same field can be used to read-out the device by determining the resistivity response which indicates whether the polarization was aligned along or opposite to the field. However this is still a destructive read-out and after reading the bit should be rewritten.

1T-1C

In this design each capacitor is separated from the others by a pass-gate transistor and a single reference cell is used for the entire memory device. The advantage is a high density of integration,

but the disadvantage of having only one reference cell leads to a higher failure rate. Upon scaling down the response should still be measurable and that's why current research focus on 3D capacitors. In these capacitors the area is increased without increasing the lateral cell size. Thus creating a measurable polarization/capacitance signal. Another way could be to use BFO, which is a multiferroic material with twice the polarization of PZT.

2T-2C

Here also the capacitor is separated by a pass-gate transistor, but even more each bit consists of 2 capacitors and 2 transistors. One capacitor for writing and the other as a reference cell. This leads to a high reliability of the device, but limits its density.

Properties of the FeRAM are high speed writing, low power consumption and long rewriting endurance, and nowadays FeRAM devices are being industrially developed. Matsushita created a prototype of 32 Mb with SBT, while Samsung used PZT to create one of 64Mb. Toshiba reported a chip of 128 Mb in 2009, which uses a different design. Fujitsu is leading in commercial use. They embedded a 32-kbit FeRAMs in the SONY playstation 2 which was manufactured with 0.5 micron CMOS process. The capacitor is 1.6 x 1.9 microns with cell size of 27.3 μm^2 for 2T-2C and 12.5 μm^2 for 1T-1C design[12].

2.3 FeFET

Ferroelectric capacitors have the disadvantage that their capacity scales with their surface area. So scaling down lowers their switching current until it can no longer be detected. Ferroelectric Field Effect Transistors (FeFET) do not have this problem, are more space efficient and show non-destructive read-out. However their retention times are shorter and no good material combinations and designs have been found yet for commercial applications.

In a FeFET the gate dielectric is replaced by a ferroelectric material. The polarization of the ferroelectric, aligned by applying a gate voltage, modifies the conductivity of the semiconductor channel between source and drain. A positive voltage, larger than the coercive voltage, directs the polarization along the semiconducting channel. This polarization results in a positive charge in the ferroelectric layer. When considering a p-type semiconductor accumulation of electrons at the interface occurs to compensate this ferroelectric charge. A low resistivity channel is created. When switching the polarization to its other stable state, the ferroelectric charge becomes negative and the electrons close to the gate in the semiconductor close to the gate get depleted. This leads to a high resistivity.

The preference for high an low conductance, invoked by the ferroelectric polarization state, remains after removal of the gatevoltage. The status of the channel can be read by applying a small drain voltage which does not disturb the ferroelectric polarization. One either obtains a source-drain current or not, corresponding to a 1 or 0. It was found that this ferroelectric transistor drain current is a function of the applied voltage history, geometry, and material properties. The thus created memory device can be considered to be non volatile for as long as the polarization is sufficiently large to maintain the charge accumulation/depletion at the gate. After depletion of the semiconductor the ferroelectric can act in two ways. It can either switch

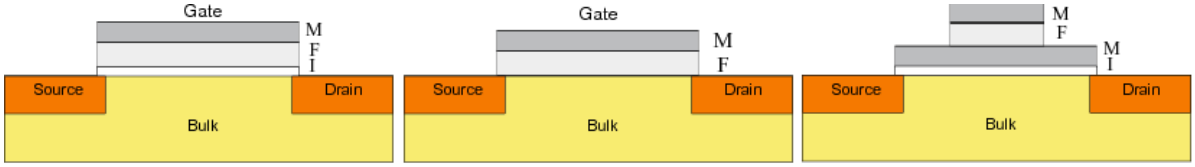

Figure 2.3: Three schematic designs of feFETs

to the reverse polarization to keep the semiconductor depleted or the ferroelectric might depolarized. The latter occurs due to the lack of free electrons that can compensate the polarization charge at the semiconductor-ferroelectric interface[20].

In this device the metal-ferroelectric-semiconductor interfaces are of importance and can lead to depolarization effects, decreasing the retention time. Also problems of interdiffusion between the ferroelectric layer and the semiconductor and injection of charge from the semiconductor to the ferroelectric occur. Especially Pb, Ti and Ta difusse easily into silicon. Several designs have been created to find the best device, see figure 2.3. When the ferroelectrics is in direct contact with the drain to source channel the device performance is largely affected by the interface properties. Adding a insulating layer decreases the depolarization effects and by using a gate stack of $Pt/SBT/HfO_2/Si$ retentions time of 30 days were reached[21]. This buffer layer act as a diffusion barrier, however current injection still occurs. A Metal Ferroelectric Metal Insulator Semiconductor (MFMIS) is another alternative. Basically a capacitor as described for FeRAMs is used and by adjusting the area ratio the charge between the MFM and insulator layer can be matched.

2.4 FeFETRAM

These so-called 1T memory devices consist of arrays of ferroelectric field-effect-transistors. Polarization of the gate alters the source drain current intensity which is monitored and thus depending on the polarization state of your ferroelectric a 1 or 0 can be read-out. This design provides non-destructive read-out and a high density. However no commercial products are yet available, mainly due to the very short retention times of the device. Retention is lost due to depolarizing fields and leakage current. Depolarizing fields always exist due to the finite dielectric constant of the semiconductor. Leakage current is caused at the Metal-Ferroelectric-Semiconductor interfaces. Ferroelectric polarization attracts the injection of electrons from both the electrode as well as the semiconductor. These injections lead to charge trapping with the ferroelectric. Because of this charge compensation occurs and the effective field reduces. Roughly the retention time is given by 2.5:

$$t = \frac{Pr}{I\alpha} \tag{2.5}$$

where t is the retention time, Pr the remnant polarization, I the leakage current and α the trapping probability.

Using a buffer to prevent charge injection from the semiconductor leads to lower leakage current but enhances the depolarizing fields. It also increases the operating voltage. A solution could be to look at single crystal with single domains. Then no trapping is suppose to occur[22]. Another one could be to use a 1T-2C scheme were the capacitors are poled in opposite states, suppressing the depolarizing fields[23].

A material that can be used in feFETRAMs is YMO. It has no interaction with the Si substrate, and may lead to low-energy consuming, high data storaging devices. However it requires temperatures below 70 K to operate. Maybe with the use of strain the ferroelectricity can be obtained at room temperature. Also PZT and SBT with several buffer layers can be used as gate materials together with other perovksites such as $LiNBO_3$[23]

2.5 Competing Memory Technologies

At the moment FLASH-based memory technology is leading in the field of memory devices. Flash is based on a array of transistors were the gate is made-up of two parts. The first part is the control gate which is used to write. Below it is a dielectric completely insulated, the floating gates. The conduction in the electron-conducting channel is completely determined by the gate voltage. When applying a voltage the electrons get trapped in the floating gate and a permanent bit is formed. This makes FLASH non-volatile, but also requires a high voltage to rewrite the bit, since the charge trapped must be able to float away through the insulating barrier. FLASH memory is processing optimally at 5V. Decreasing the voltage as was agreed upon by the electronic industry to 0.5V will set aside this technique. Even when charge pumps are inserted. Furthermore quantum effects such as electron tunneling will influence FLASH upon miniturazing. Hence FLASH is limited in endurance, scalability and voltage requirements. Several memory design are considered to replace FLASH and the competing ones for feRAM and feFETRAMs are discussed below.

- **Magnetic Random Access Memory** (MRAM)is in development since the 90s and is considered to be a fast and easy to control memory device. Its operation principle is based on the tunneling current through a thin layer sandwiched between two ferromagnetic layers. This current depends on parallel or anti-parallel being of the two ferromagnets with regard to one another. The read-out is non-destructive and the memory non-volatile. But the writing requires relatively high powers to switch the magnetization. However the main problem lies in cross-talk. When the magnetization of one cell is changed, this tends the affect that of the others surrounding it, which is undesirable for high density arrays. Until now devices of 32mb have been made.

- **Phase-Change Random Access Memory** (PCRAM) is especially of interest for scaling down. It uses the atomic structure to write information in. A material is held in between to electrodes and can either have an amorphous insulating phase or a crystalline conducting one. Upon application of an electric current the materials melts and depending on the time of exposure it cools back to an amorphous or crystalline phase. This is used to write bits. However heating requires quite some power and fast switching will destabilize the crystalline phase. Recently Samsung developed a 512mb PCRAM chip, indicating the

advantage of high densities arrays that can be created with this technique. Only a few dozen of atoms are needed to distinguish between the two phases.

- Another way to use atomic structure to store information on is **Resistive Random Access Memory** (RRAM). It use electrochemical reactions to change the phase of a material. Although this is a fast operating, low-power technique stability is the main issue. When scaling down electrical currents will tend to by-pass the regions of high resistance making it hard to read-out your memory properly. No prototypes have been commercially produced.

- Dynamic Random Access Memory is a non-volatile capacitor based memory technology, which just like FLASH entered the gigabit area. Bits are written by charging/discharging the capacitor. However capacitors have the tendency to leak current and thus the memory needs to be refreshed every millisecond. Hence the non-volatility of the device, since removing the current will lead to memory loss. In these DRAMS ferroelectrics can be used because of their high permitivity in the vicinity of the ferroelectric transition.These DFeRAMs need only to be refreshed every 100s and reduces the power consumption. Thin film perovskite ferroelectrics offer some of the largest dielectric constants attainable in their paraelectric state. IBM for instance already researched the use of BST for DRAM applications [24].

Chapter 3

Future Prospects

Currently the research to improve the ferroelectric devices is focused on scaling down and finding materials or designs that can circumvent the problems of low retention times and destructive read-out. In this chapter a short overview is given on two main directions of the research; those multiferroics and nanoscale devices.

3.1 Multiferroics

A way to overcome destructive read-out is by using separate mechanisms for reading and writing. For instance ferroelectric read-out while the bit is magnetically written. This can be achieved when considering multiferroic thin layers in stead of ferroelectric thin films in the device. Multiferroic materials show a coexistence and coupling of ferromagnetism and ferroelectricity. Ferroelectricity can thus be controlled by application of a magnetic field or an electric field can influence the ferromagnetism.

There exists two types of multiferroics. In type I a weak coupling is seen between ferromagnetism and electricity, which are independent in origin. While for type II a strong coupling does the trick, leading to magnetically driven ferroelectricity. Examples of these types with multiferroicity at room temperature are respectively $BiFeO_3$ (type I) and $YMnO_3$(type II). Multiferroicity can occur because of lone-pairs ($BiFeO_3$), charge-ordering or due to geometrical frustration. $YMnO_3$ is believed to belong to the latter although these spin-frustrated systems require more research. Especially geometrically frustrated systems are of interest for four-state memory devices, since the dielectric properties change with a magnetic phase transition. In type 2 multiferroics the magnetic order can either be formed by magnetic frustration or alignment of magnetic moments. In either case the polarization is believed to occur because of exchange striction between the ions with (different) valences[23].

The challenge for the field of multiferroics is to find materials with good physical properties at room temperature. This do not have to be oxides, recently also fluorides come into attention. For type I the magnetocoupling needs to be enhanced artificially without losing the multiferroicity. Especially $YMnO_3$ is considered to be a great potential for device applications because of its strong coupling between ferroelectricity and ferromagnetism. Of course multiferroics can just be incorporated like ferroelectrics in memory devices. BFO, a multiferroic, for instance shows twice the polarization of PZT. However being able to use both characteristics at room temperature will enhance the device possibilities.

A device design that exploits both ferroelectric and magnetic properties of an multiferroelectric is the four-state memory. It can be seen as a combination between a MRAM and FeRAM. Bits can be written by applying a voltage, while a magnetic filed can be used for read-out. The writing voltage scales down with thickness and magnetic field, enabling a high capacity of the device. This has been demonstrated for $La_{0.1}Bi_{0.9}MnO_3$ (LMBO)[25].

3.2 Nanoscale Devices

Ferroelectric nanoparticles have been found to remain ferroelectric to sizes of at least 20 nm[26]. Forming arrays of those particles will lead to high density, thus high capacity memory devices. However the production costs and time should be improved and one of the ways suggest is by self-patterning. In self-patterning the ordering is obtained by interactions between islands in a substrate. These islands can be formed by adding a small amount of material to a substrate with a substantial mismatch. In this way one can produce nano electrode arrays or arrays of the ferroelectric material themselves.

Another interesting approach in scaling down is the use of nanotubes. These can be used to increase the dielectric surface, in order to get 3D capacitors. These tubes can be incorporated into silicon substrates, as has been shown for $BaTiO_3$ and $PbTiO_3$[12]. The idea is to deposit electrode/ferroelectric/electrode inside the nanotube. Thus creating 3D FeRAMs with high density and improved read/writing. However still a lot needs to be found out, especially a theoretical framework which would enable the design of commercial devices.

Conclusions

Starting as a mere artifact, ferroelectricity has opened the way to create a non-volatile, low-power consuming memory device. This phenomena is related to the polar displacements within a crystal structure upon application of an external field. A hysteresis can be seen and this is the basis for the two-level logic scheme. Especially the family of perovskite oxides have led to materials such as PZT and BST which are currently integrated as thin films in industrial prototypes. Ferroelectricty is believed to be preserved down to several unit cells and thus scaling down the devices should be possible. However depolarizing fields and cross-talk needs to be considered, although being able to control strain at low thickness might lead to surprising effects.

From the device design point of view, ferroelectrics can be used as capacitors and field-effect-transistors. The FeRAM 2T-2C has the best prospects, although its lack of high capacity might become a problem once the retention time is increased for the 1T-1C device. 3D designs, such as nanotubes, might be an answer to the low capacity problem and multiferroics are looking good to tackling the destructive read-out. However as in the case with FeFETRAM a material with good properties at room temperature is still lacking.

Comparing the in chapter 2 described memory technologies with FeRAM and FeFETRAM, it is still hard to see the road ahead. While DRAM and FLASH have already entered the region of gigabits, upon scaling down they are mostly likely to be replaced. PCRAM and RRAM look favorable with regards to high density areas but their stability and processability still need a lot of research. FeRAMS show more storage capacity then magnetic harddisks and faster writing speed and longer lifetime than FLASH memory. However their retention times are not yet that good, let along their non-destructive read-out. The advantages of ferroelectric devices is that they show non-volatility and low-power consumptions. Although their capacity can be questioned. Economically speaking, ferroelectric devices, can be quit productive. Due to their low-power consumption, relatively easy design and implementation in a standard CMOS process, their cost might win from their lack of capacity. However in order for it to replace FLASH, ferroelectric memories still requires adequate knowledge of the device, good design models and the ongoing search for materials with better properties.

In conclusion in this paper an overview has been given of the important ferroelectric characteristics and device designs, needed to understand ferroelectric memory devices. This field has a real potential for the future of memory technology and who knows to what it might lead.

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