Design and Implementation of Operational Amplifiers with Programmable Characteristics in a 90nm CMOS Process

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Abstract—**Operational amplifiers (op-amps) serve as the basic building blocks in almost every analog and mixed-signal electronic circuit. However, one of the most common problems in op-amp design is the variation in the op-amp's performance caused by process variations during fabrication. As such, it is of utmost importance that provisions be made on the op-amp to compensate for possible deviations in performance after chip fabrication. In this paper, a procedure on integrating programmable bias networks into an operational amplifier is developed. The programmable network driven by digital input words makes the output bias currents and voltages variable, thus making the op-amp tunable for proper operation even after chip fabrication. Furthermore, the programmability of other op-amp parameters such as gain, slew rate, and compensation are explored to increase the capability and flexibility of the op-amp. The programmability schemes are employed on two base op-amp topologies namely, the Two-stage Miller and the Folded Cascode. The project is implemented in a standard 90nm CMOS process.**

I.INTRODUCTION

Analog CMOS design becomes more difficult especially in the present age of nanometer technology. This is mainly because CMOS technology has been greatly optimized for digital circuits while analog circuit design cannot fully utilize the technology. Digital circuit design only depends on the tradeoff between speed and power dissipation while analog circuit design has other factors to consider such as noise rejection and interference. This, in itself, poses major problems in design and with the emergence of the nanometer technology, more problems arise. These problems make design process and implementation more difficult than it is in previous CMOS technologies.

Smaller transistor area means more transistors can be packed in a single chip. This makes a single chip smaller in physical size but more powerful in performance in terms of speed and bandwidth. But this also makes a single chip more intricate because of the increased complexity in the layout and fabrication rules, making chip manufacturability a great challenge. Minor process variations and parameter drifts become major problems due to the chip's high sensitivity to physical defects. As a result, old design techniques are no longer applicable to the present technology. Fundamentals like power management, circuit integrity, rule-based physical verification, and parasitic extraction may not just be enough. A designer's strategy must shift from basic and fundamental design techniques to new and optimal design methods which may require changing the design itself.

During chip fabrication, there are unavoidable permanent variations in the parameters of the design. Because of this, solutions are being developed on how to minimize the effects of the variations. One possible solution is to incorporate programmable blocks into the chip. This makes certain parameters variable even after chip fabrication. In this paper, digital input words (i.e. logic high or logic low) control the switches of the programmable blocks, making these parameter variations in discrete levels only.

II.BASE OP-AMPS

Part of this project is the development of two op-amps which are used as base amplifiers for the programmable blocks. The two base op-amps are the Two-stage Miller and the Folded Cascode op-amps. These op-amps are necessary to measure the performance of the programmable blocks during integration.

Figure 1 shows the schematic diagram used for the implementation of the Two-stage Miller op-amp.

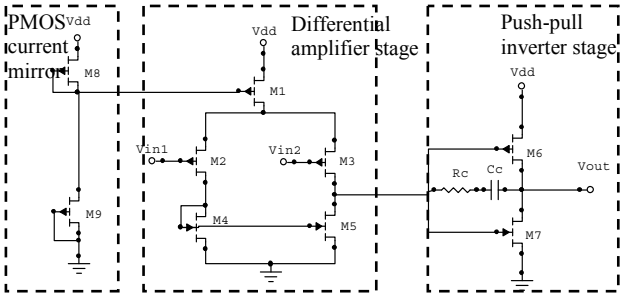


Fig. 1. Two-stage Miller op-amp schematic diagram

Figure 2 shows the schematic diagram used for the implementation of the Folded Cascode op-amp.

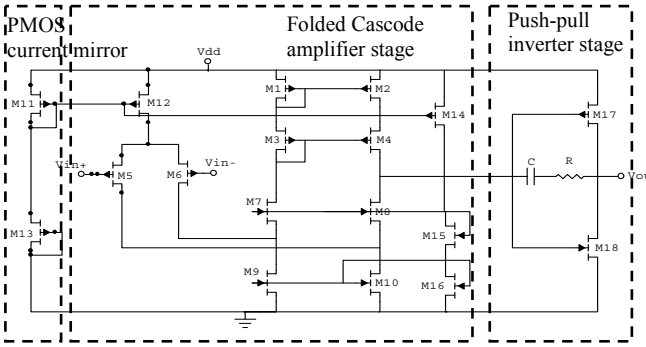
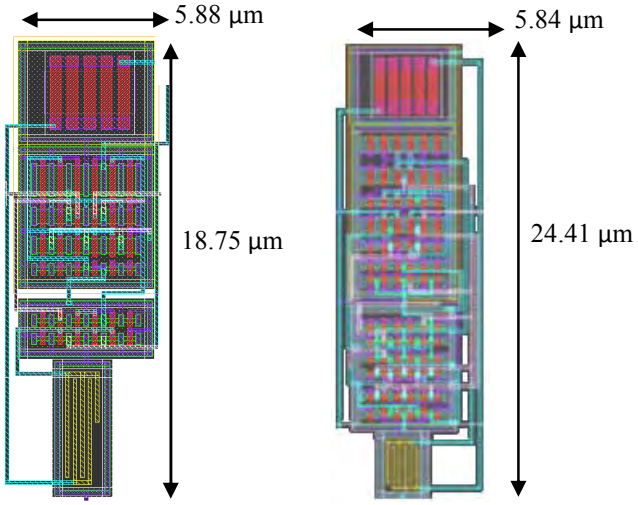


Fig. 2. Folded Cascode op-amp schematic diagram

Snapshots of the layout of the two base op-amps are shown in Figure 3.



(a) (b)

Fig. 3. Layout of (a) Two-stage Miller and (b) Folded Cascode op-amps

Table 1 summarizes the obtained specifications for the Two-stage Miller and Folded Cascode op-amp.

TABLE 1
SUMMARY OF OBTAINED SPECIFICATIONS FOR THE BASE OP-AMPS

Parameter	Two-stage Miller	Folded Cascode
A_{dm}	52.37 dB	65.66 dB
CMRR	88.64 dB	103.23 dB
GBWP	1.014 GHz	539.4 MHz
PM	47.4°	7.721°
SR	697.53 V/µs	556.42 V/µs

III.Programmable Bias Networks

It is very critical for every op-amp to function properly and correctly. During simulation, an ideal op-amp's accuracy is mainly dependent on how accurate its biasing is. However, during chip fabrication, the technology parameters of the transistors such as threshold voltage V_T, length L, and width W vary from the values used during schematic and layout simulations. These deviations usually result in a change in the bias voltages and bias currents; thus affecting other op-amp characteristics. One way of solving this problem is to include programmable bias networks driven by digital inputs to the op-amp design and implementation. This makes the bias currents and voltages tunable to the desired value for correct op-amp operation even with process variations after chip fabrication.

Three programmable bias network topologies are implemented in this project namely: Programmable Current Attenuator (PCA), Programmable Current Reference Circuit (PCRC), and Programmable Current Source (PCS).

Programmable Current Attenuator (PCA)[1]

Figure 4 shows a 4-bit digitally-programmed current attenuator circuit. It is based from the conceptual scheme of an R-2R ladder network. The value of the current passing through the legs of the circuit is determined by two major factors: the division factor, D, introduced by the scheme itself, and the input digital word at the gates of the transistor pairs. Two complementary outputs, I_1 and I_2 are produced at the output node which is mainly dependent on the reference current, I_{ref}.

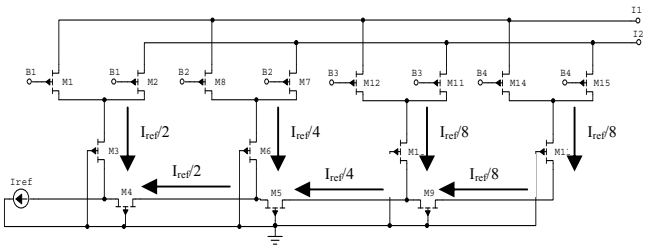


Fig. 4. PCA schematic diagram[1]

Programmable Current Reference Circuit (PCRC)[3]

Figure 5 shows a 4-bit digitally-programmed current reference circuit taken from a patent[3]. The architecture of the circuit shown in this figure is composed of transistor pairs with each pair connected in parallel with resistors of different values. The circuit works by varying the total resistance seen at the output node using the transistor pairs as switches, thus changing the P- and N- bias voltages or V_P and V_N, respectively.

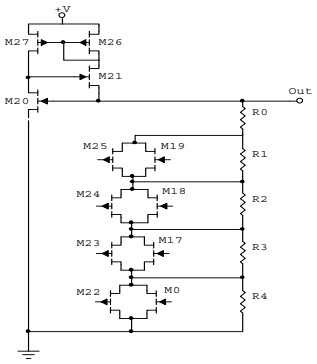


Fig. 5. PCRC schematic diagram[3]

Programmable Current Source (PCS)[2]

Figure 6 shows a 4-bit digitally-programmed current source circuit. Equally sized NMOS transistors are connected either

in series or in parallel to achieve the needed current, I_{out}. This type of transistor connection effectively increases or decreases the total W/L ratio of each leg: increasing the number of transistors in serial connection decreases the current flowing through it while parallel connection increases the leg current. The architecture delivers pre-programmed binary weighted current levels at every current leg which are all summed up at the I_{out} node. The number of bits on logic high contributes to the additive nature of the current I_{out}.

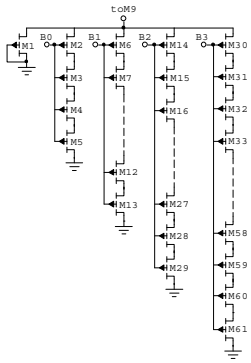


Fig. 6. PCS schematic diagram[2]

Figure 7 summarizes the obtained specifications for the integration with Two-stage Miller op-amp and Figure 8 for the integration with the Folded Cascode op-amp.

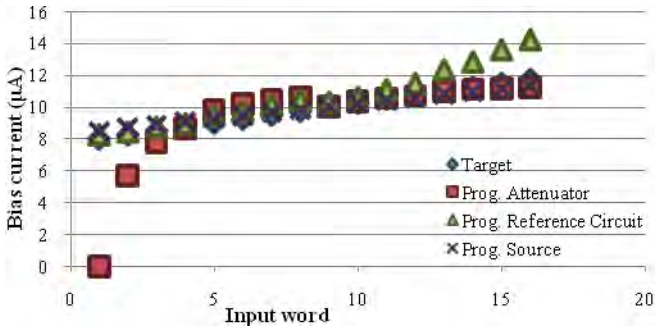


Fig. 7. Obtained results for the integration of PCA, PCRC, and PCS with the Two-stage Miller op-amp

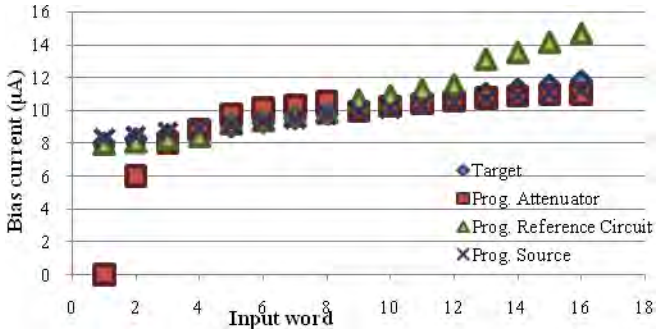


Fig. 8. Obtained results for the integration of PCA, PCRC, and PCS with the Folded Cascode op-amp

IV. Other Programmable Topologies

To further increase the programmability and capability of our op-amps, other programmable topologies are implemented such as Programmable Gain Amplifier, Programmable Slew Rate, and Programmable Compensation.

Programmable Gain Amplifier (PGA)[5]

Figure 9 shows a 4-bit digitally-programmed gain amplifier. The PGA consists of a negative feedback g_m-boosted source degenerated differential pair with resistive loads, R_{LOAD} = 50kΩ. The main concept of this approach is to change the value of the resistance R so that the gain of the amplifier will also change. The PGA has a fixed dominant pole at $\omega = 1/R_L C_L$ thus having a constant GBWP at all sweeps of the degenerated resistance. It is a stand-alone amplifier; therefore no integration with the base op-amps was done.

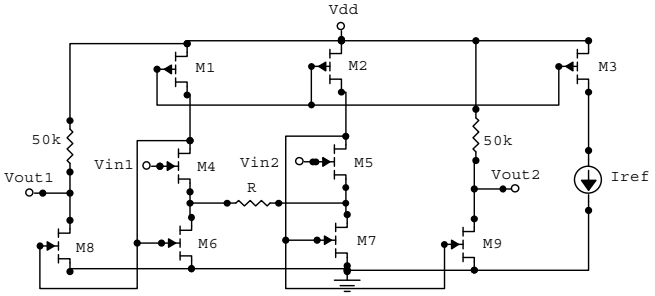


Fig. 9. PGA schematic diagram[5]

Figure 10 shows a graph of the obtained results for the PGA.

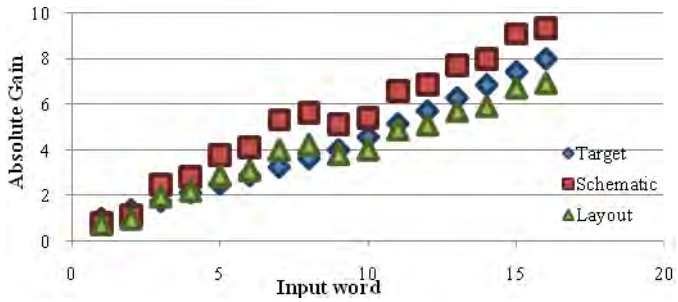


Fig. 10. Obtained results for PGA

Programmable Slew Rate (PSR)[4]

Figure 11 shows a 4-bit digitally-programmed slew rate. This topology uses programmable current source in order to make the currents within the op-amp variable. Every variation to the bias current affects the output slew rate of the base op-amp.

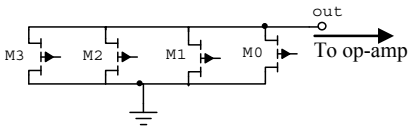


Fig. 11. PGA schematic diagram[4]

Figure 12 shows a graph of the obtained results for the integration with the Two-stage Miller op-amp and Figure 13 for the integration with the Folded Cascode op-amp.

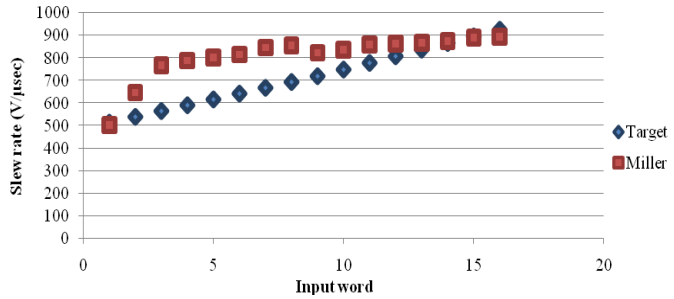


Fig. 12. Obtained results for the integration of PSR with the Two-stage Miller op-amp

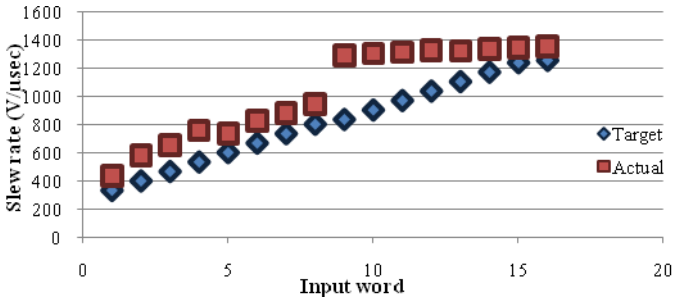


Fig. 13. Obtained results for the integration of PSR with the Folded Cascode op-amp

Programmable Compensation (PC) [6]

Figure 14 shows a 4-bit digitally-programmed compensation. The PC is implemented using MOS capacitors which are ideally connected in between the input and output stages of an uncompensated op-amp. Varying values of capacitances effectively varies the compensation of the circuit.

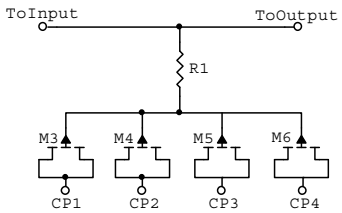


Fig. 14. PC schematic diagram [6]

Figure 15 shows a graph of the obtained results of the PC integrated with the Two-stage Miller op-amp and Figure 16 for the integration with the Folded Cascode op-amp.

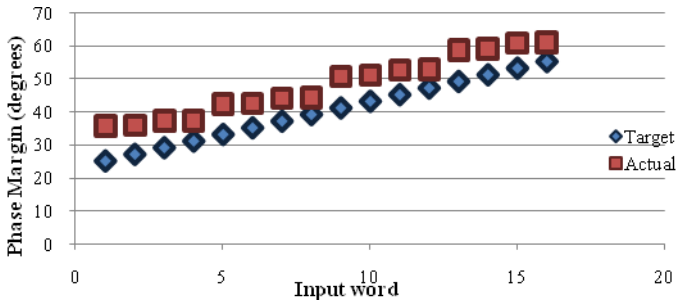


Fig. 15. Obtained results for the integration of PC with the Two-stage Miller op-amp

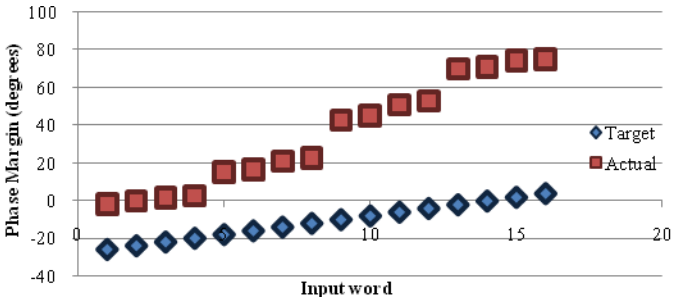


Fig. 16. Obtained results for the integration of PC with the Folded Cascode op-amp

V. Conclusions and Recommendations

Using the presented methodologies, it is possible to design and implement op-amps with programmable characteristics. The three programmable bias network topologies were all able to vary the input current driving the base op-amps with a range of 8µA to 12µA (I_{BASE} +/-20%). However, PCRC and PCA suffer from poor linearity. Only PCS was able to produce a linear output current which closely follows a linear step increase.

The PGA attained a range of 0-17 dB. A constant GBWP of 11.5 GHz is maintained at all sweeps of gain. The PSR also was able to vary the slew rate for the integration with both op-amps. The integration with the Two-stage Miller and Folded Cascode op-amp attained a slew rate range of 504 V/µs to 895 V/µs and 434 V/µs to 1,354 V/µs respectively. Finally, the PC was able to increase the phase margin from 35.8° to 61.2° and from 0° to 75.31° for the integration with the Two-stage op-amp and Folded Cascode op-amp respectively.

References

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