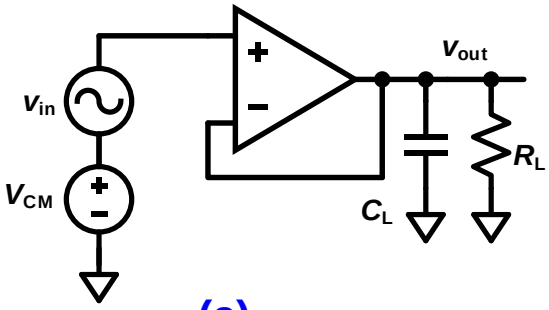
ECE 415/515 –ANALOG INTEGRATED CIRCUIT DESIGN

FULLY-DIFFERENTIAL OPAMP DESIGN AND SIMULATION

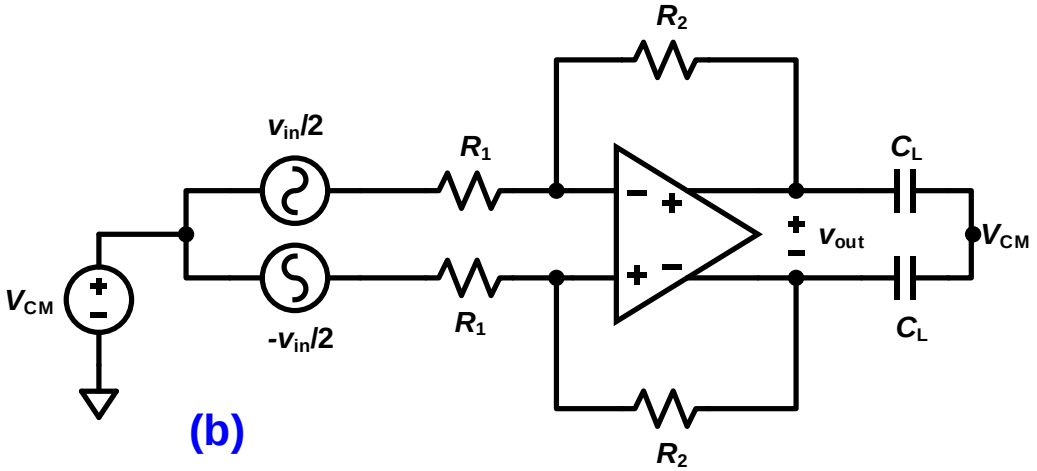
University of Idaho
College of Engineering

OPAMP DESIGN PROJECT



(a)

ECE415/EO

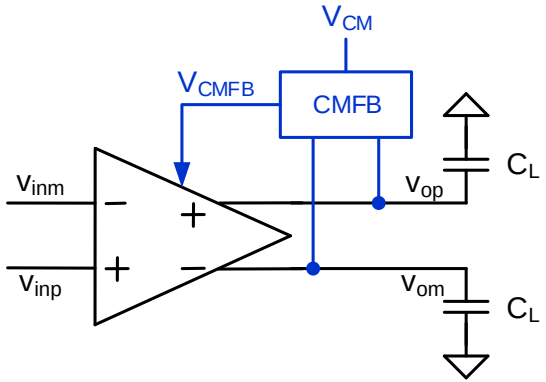


(b)

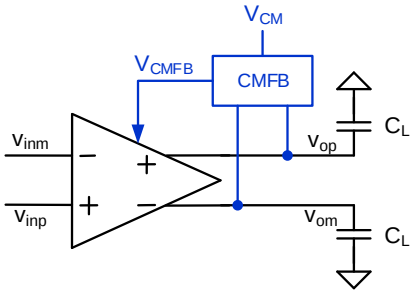
ECE515

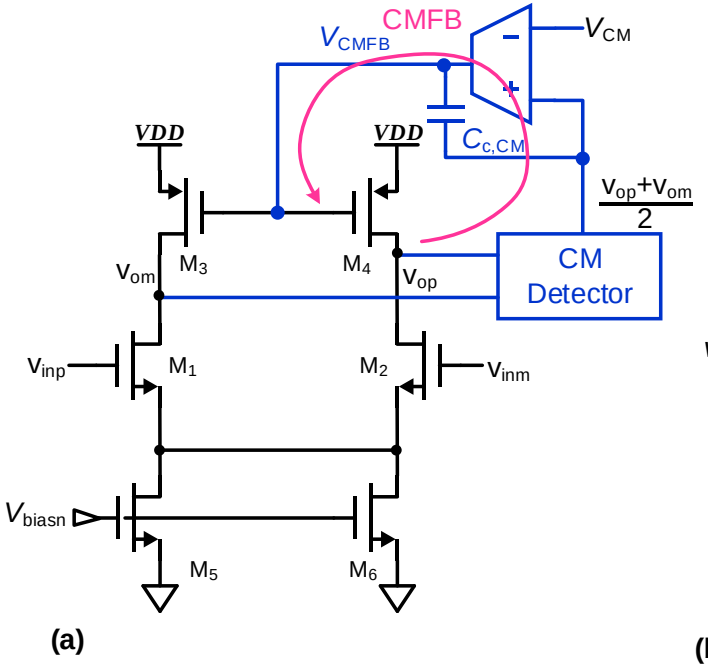
FULLY-DIFFERENTIAL (FD) OPAMPS

- Differential output is $v_{out} = v_{op} - v_{om}$ for differential input $v_{in} = v_{inp} - v_{inm}$
- Common-mode (CM) output is $v_{out,CM} = \frac{v_{op}+v_{om}}{2}$
- Output CM-level must be held constant to a well-defined value (V_{CM})
  - Common-mode feedback (CMFB) loop to control the output CM-level
  - Implemented using continuous-time (CT) or using switched-capacitor (SC) circuits

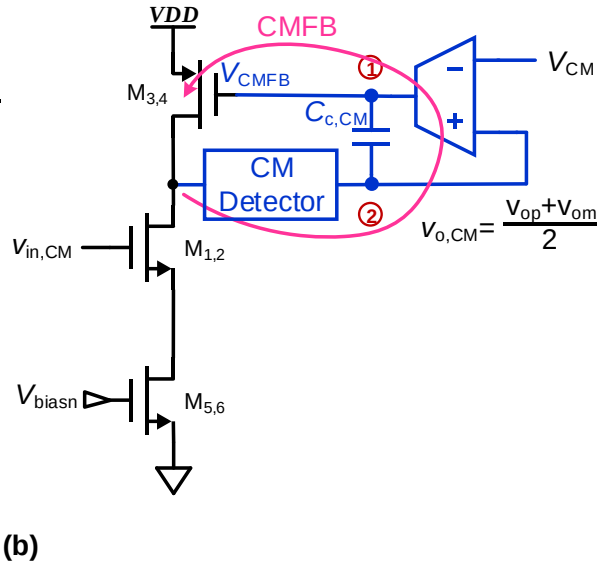


CMFB: BASIC IDEA





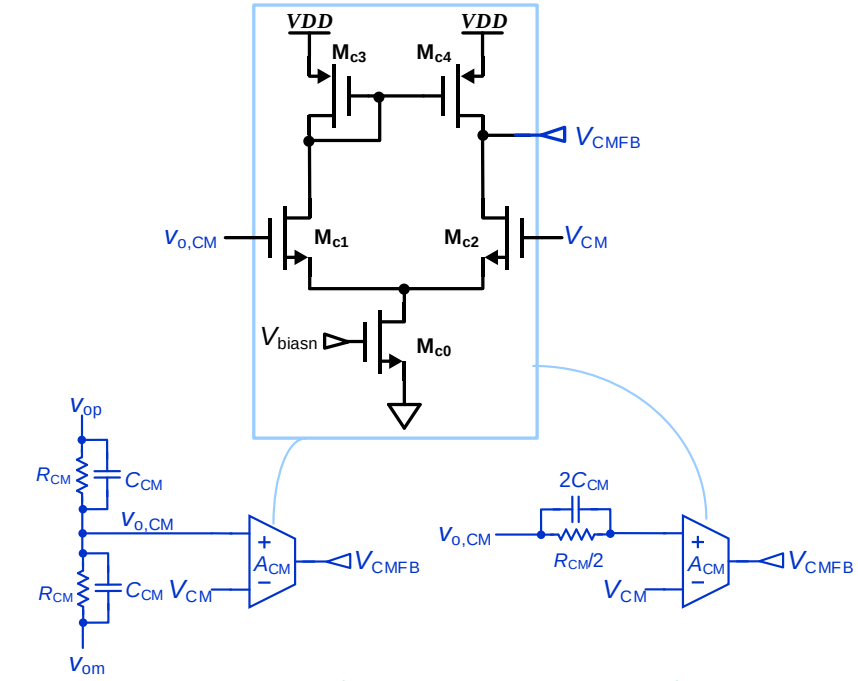
CMFB loop compensation



CM equivalent circuit

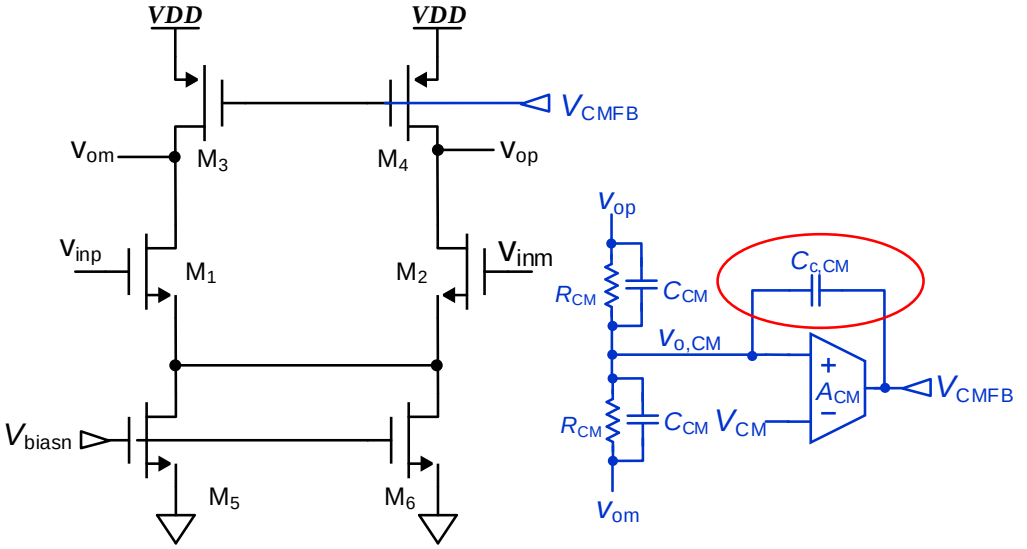
RESISTIVE CM-DETECTOR

- Resistance (R_{CM}) averaging circuit senses $v_{out,CM} = \frac{v_{op}+v_{om}}{2}$
- A capacitive averaging network (C_{CM}) in parallel for high-frequency averaging
  - Mitigates bandwidth limitation due to $R_{CM}C_{in,p}$
- $v_{o,cm} = \left(\frac{v_{op}+v_{om}}{2}\right)\left(\frac{2C_{CM}}{2C_{CM}+C_1}\right)$
- $i_{c1} = \frac{g_{mc1}}{2} v_{o,cm} - V_{CM}$



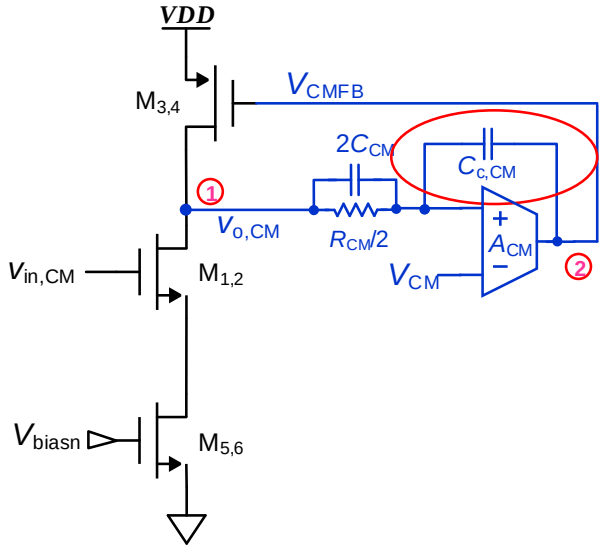
(a) Resistive CM-detector (b) CM equivalent circuit with error amplifier

RESISTIVE CM-DETECTOR: COMPENSATION 1



(a) Unlabeled NMOS are 10/2. Unlabeled PMOS are 22/2.

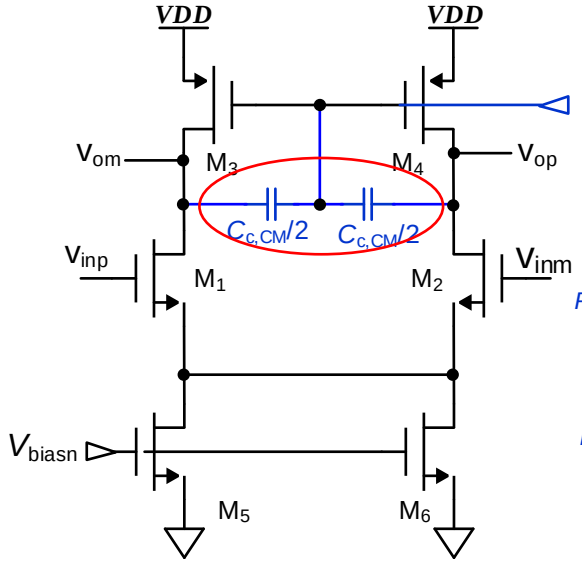
CMFB loop compensation



(b) CM equivalent circuit

- Miller compensation of the CMFB loop using $C_{c,CM}$
- Two ways to place the compensation cap between nodes 1 and 2.

RESISTIVE CM-DETECTOR: COMPENSATION 2



(a)

Unlabeled NMOS are 10/2.
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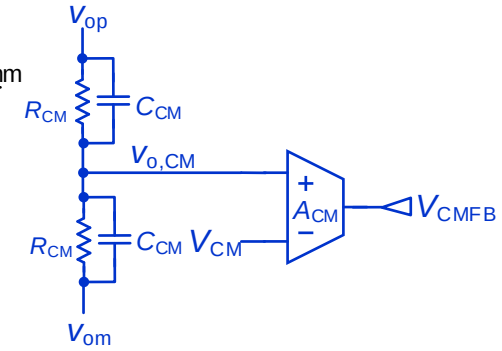
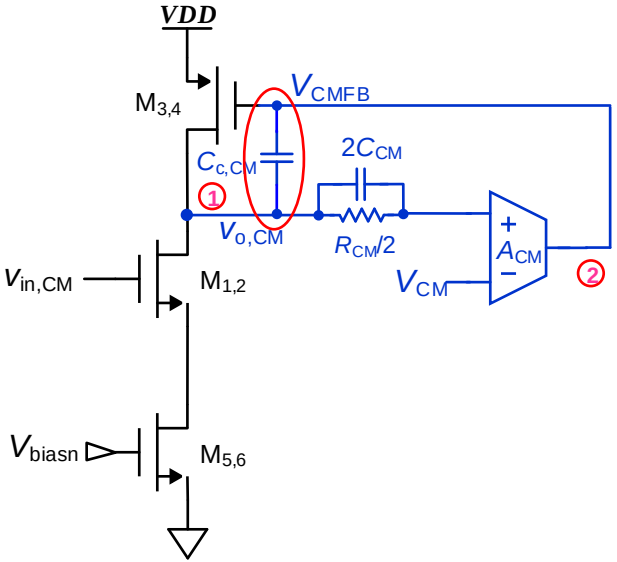


CMFB loop compensation

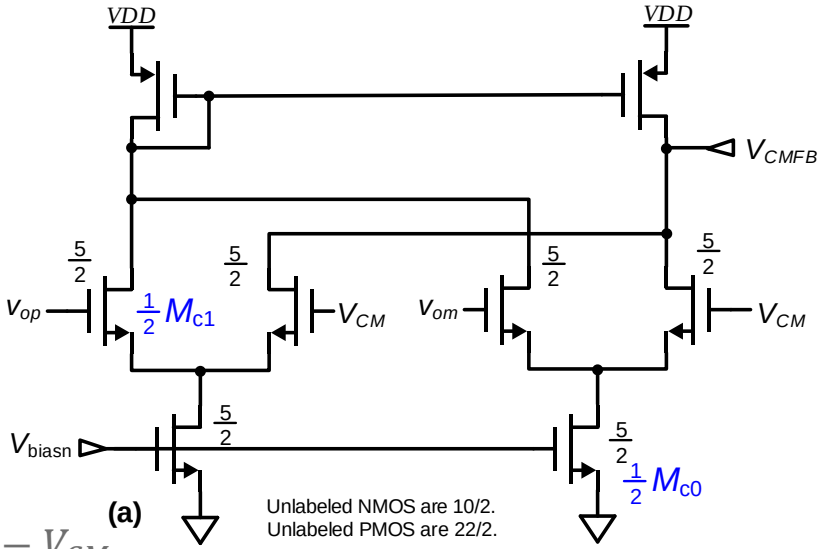


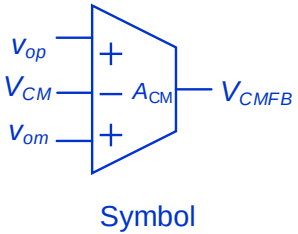
(b)

CM equivalent circuit

- Note that zero-nulling resistor is not shown in these slides, but is used in designs

DUAL-DIFF-PAIR (DDP) CM-DETECTOR



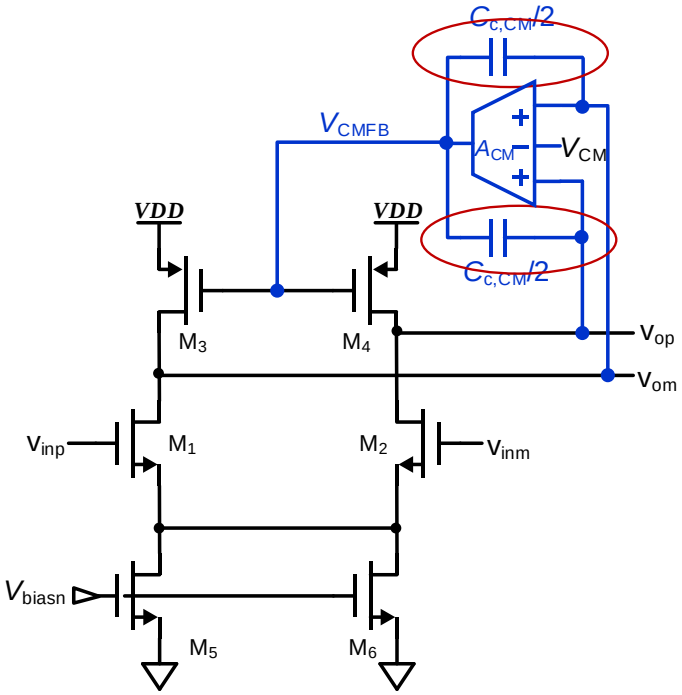


- $i_{c1} = \frac{g_{mc1}}{2}\left(\frac{v_{op}+v_{om}}{2}\right) - V_{CM}$
- $= \frac{g_{mc1}}{2}\left(\frac{v_{op}}{2} - \frac{V_{CM}}{2}\right) + \frac{g_{mc1}}{2}\left(\frac{v_{om}}{2} - \frac{V_{CM}}{2}\right)$
- $= \frac{g_{mc1}}{4}\left(v_{op} - V_{CM}\right) + \frac{g_{mc1}}{4}\left(v_{om} - V_{CM}\right)$

Diff-pair Diff-pair

Quiz: Diff-How does the dual diff-pair (DDP) look in CM-equivalent circuit?

DUAL-DIFF-PAIR CMFB COMPENSATION



(a)

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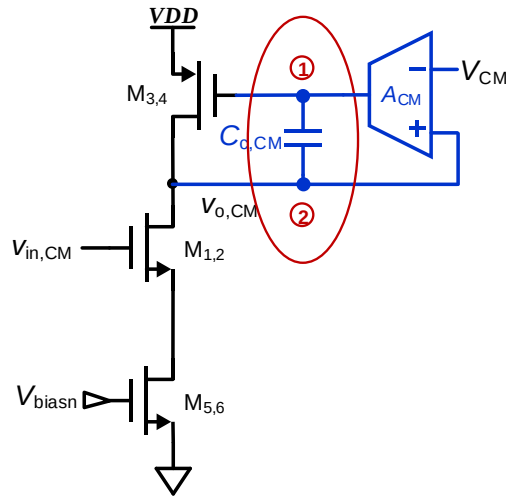
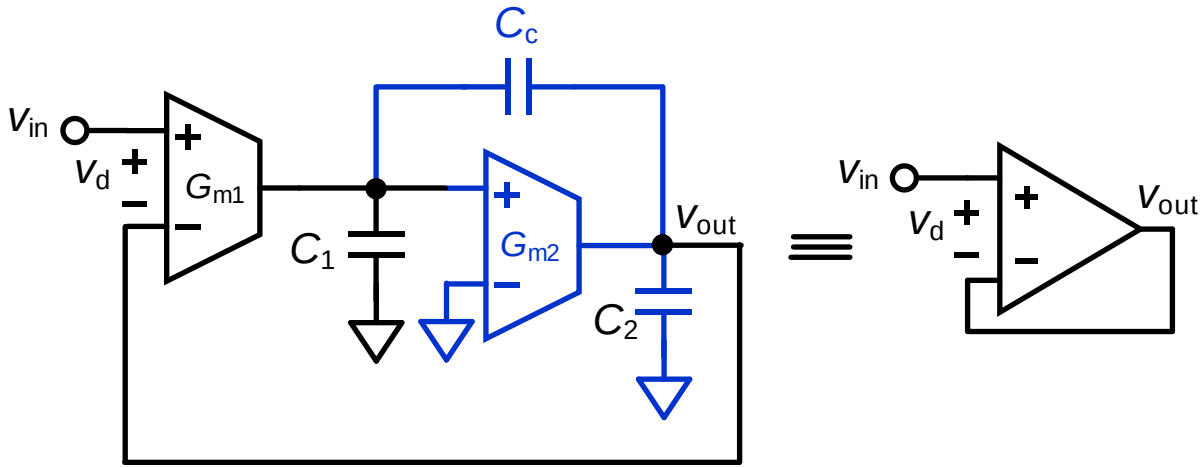
CMFB loop compensation



(b)

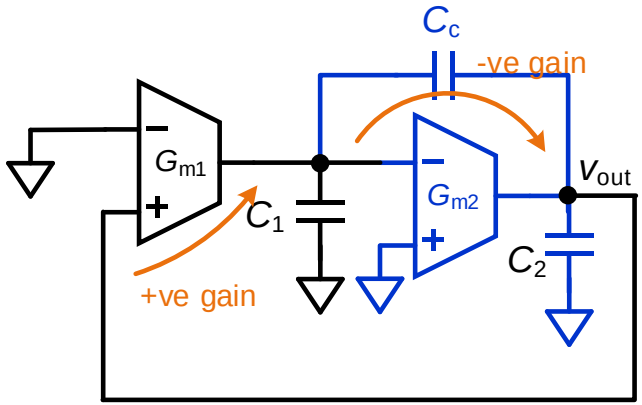
CM equivalent circuit

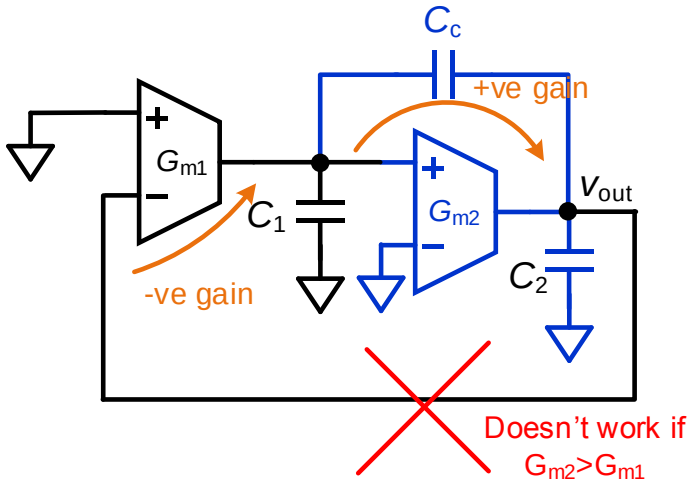
ASIDE: TWO-STAGE LOOP STABILITY (1)



- Two-stage feedback loop should ensure overall negative feedback
- Only one gain-stage can be negative
  - Two possible configurations by interchanging polarities

ASIDE: TWO-STAGE LOOP STABILITY (2)



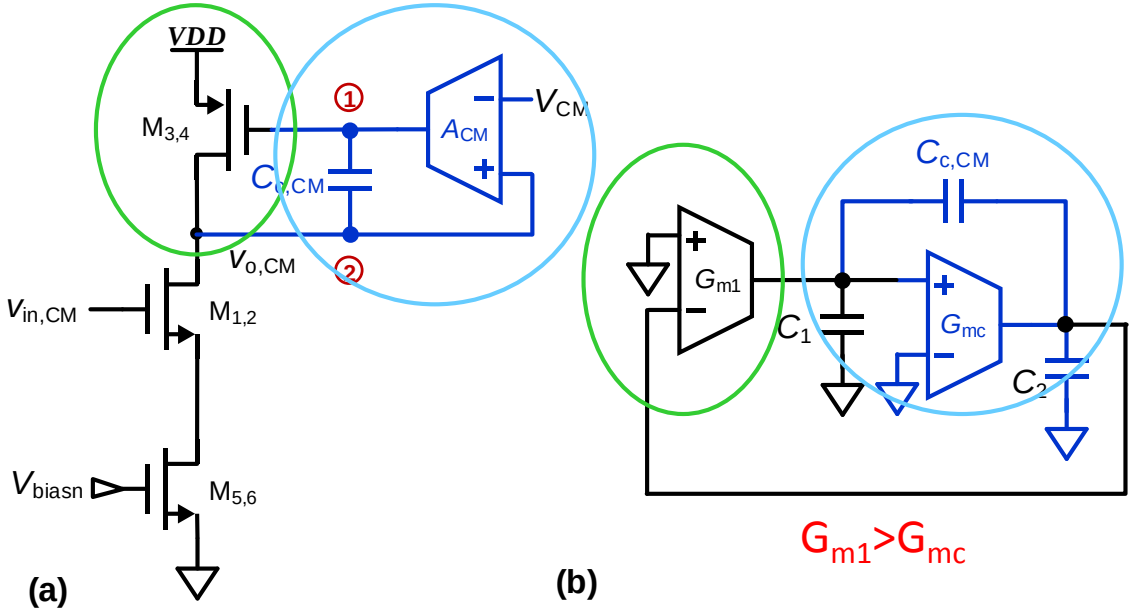


- Results in LHP poles if $G_{m2}>G_{m1}$
- Results in RHP pole(s) if $G_{m2}>G_{m1}$. Unstable!

- From loop-analysis, the negative transconductance should have larger G_m for stability (Important!)

CMFB LOOP STABILITY (1)

- We have $G_{mc} < G_{m1}$ by design ($I_{c0}=I_0/n$)
- G_{m1} should have negative polarity for stability!
  - G_{mc} would have positive gain across it
  - Overall negative feedback in the CMFB loop



CM equivalent circuit

Reduced circuit

CMFB LOOP STABILITY (2)

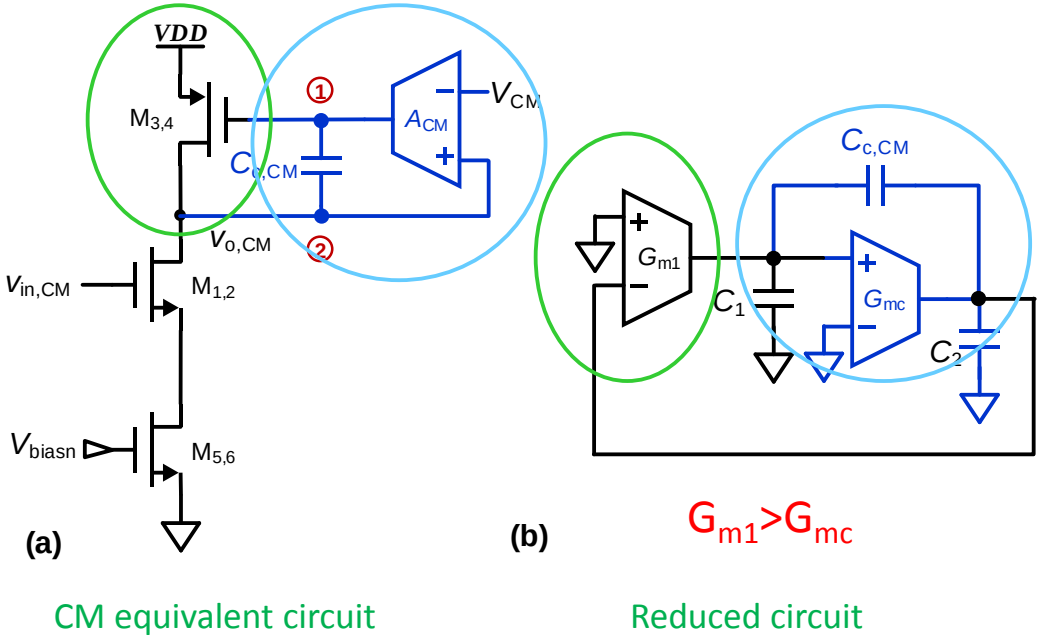
- CMFB unity-gain frequency

$$\omega_{u,CMFB} \approx \frac{G_{mc}}{C_{C,CM}}$$

- Note that here $G_{mc} \equiv g_{m1}$ and $G_{m1} \equiv g_{m2}$ in the pole-splitting equations, as we had $g_{m2} > g_{m1}$ in the pole-splitting derivation
- The CMFB loop-gain

$$A_{v,CM} = G_{mc} R_c G_{m1} R_1$$

  - Should be large enough to ensure small DC error

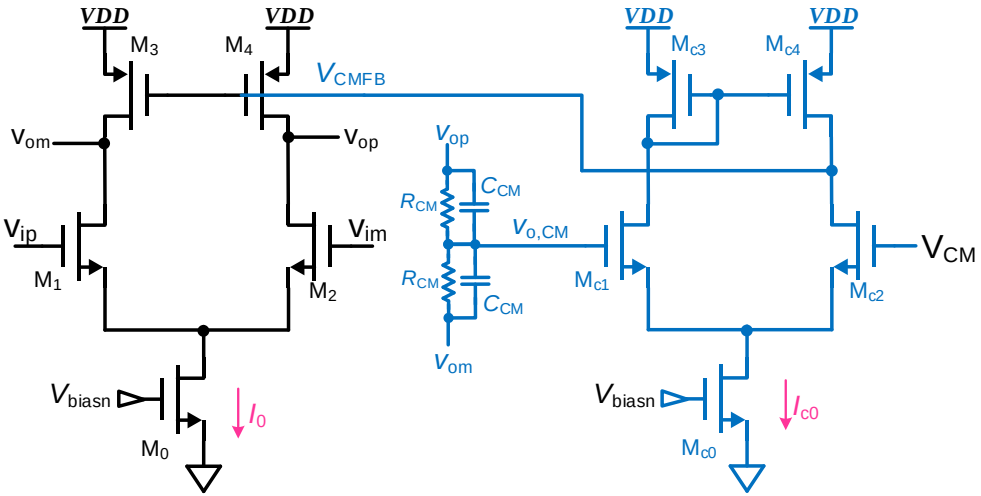


CM equivalent circuit

Reduced circuit

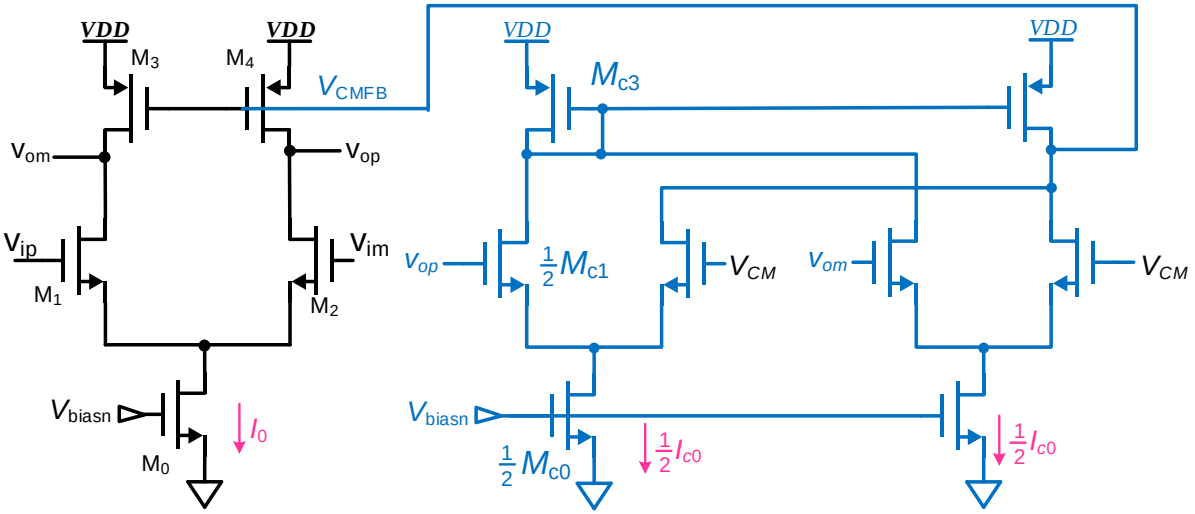
SIZING OF THE CMFB ERROR AMPLIFIER

- The error amplifier circuit should be a replica of the gain stage
- Bias current I_{c0} and widths are scaled down to save power ($I_{c0}=I_0/n$)
- Both the stages should have the same current density
  - $\frac{I_0/2}{W_{3,4}} = \frac{I_{c0}/2}{W_{c3,4}}$
  - Ensures that $M_{3,4}$ and $M_{c3,4}$ will have the same V_{SG} values
  - Otherwise, any mismatch in bias voltages will lead to systematic offset in the CMFB loop ☹



SIZING OF THE DDP CM-DETECTOR

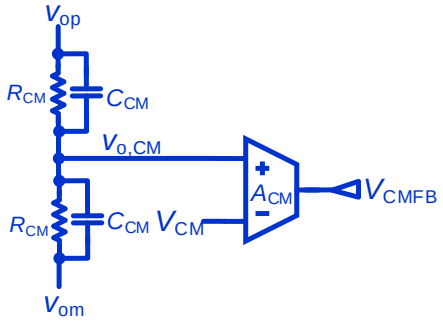
- Same ideas for the DDP CM-detector
- Both stages should have the same current density
  - $\frac{I_0/2}{W_{3,4}} = \frac{I_{c0}/2}{W_{c3,4}}$
  - Ensures that $M_{3,4}$ and $M_{c3,4}$ will have the same V_{SG} values
  - Otherwise, any mismatch in bias voltages will lead to systematic offset in the CMFB loop ☹



COMPARISON

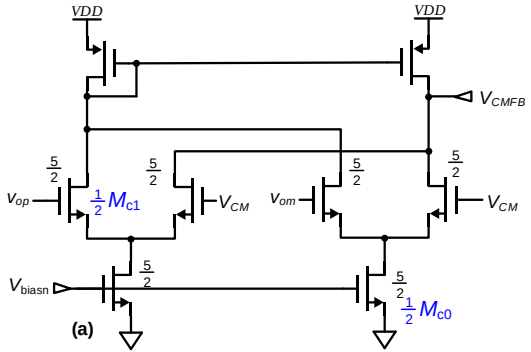
Resistive CM Detector

- Unrestricted input range
  - Rail-to-rail operation ☺
- R_{CM} loads the differential gain stage and reduces its gain ☹



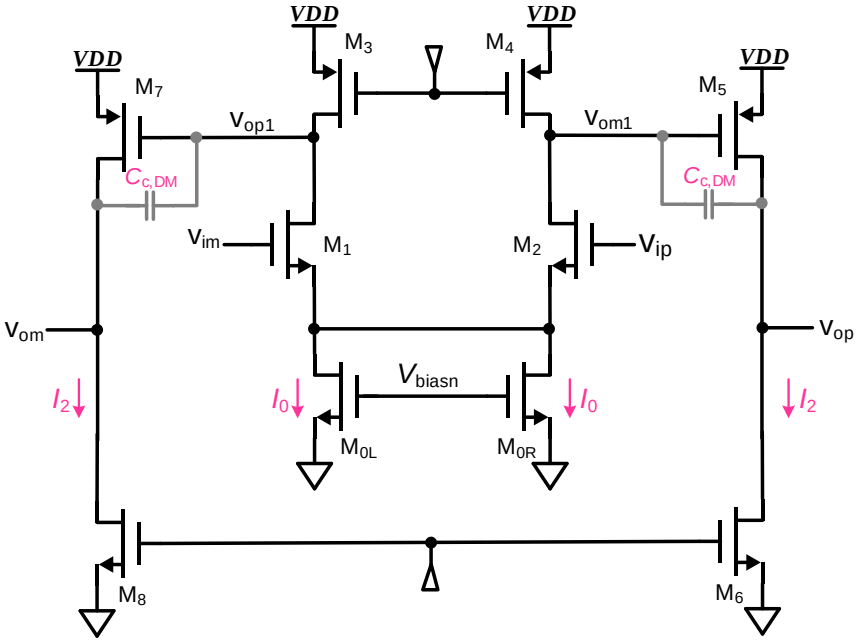
Dual-Diff-Pair CM Detector

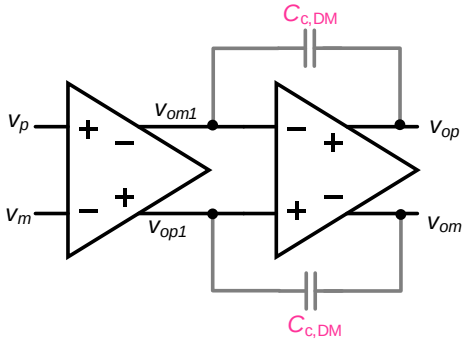
- Limited by input CMR of the diff-pair
  - Allows very limited voltage swing ☹
- Only small capacitive load ☺



TWO-STAGE FULLY-DIFFERENTIAL OPAMPS

TWO-STAGE FD OPAMP

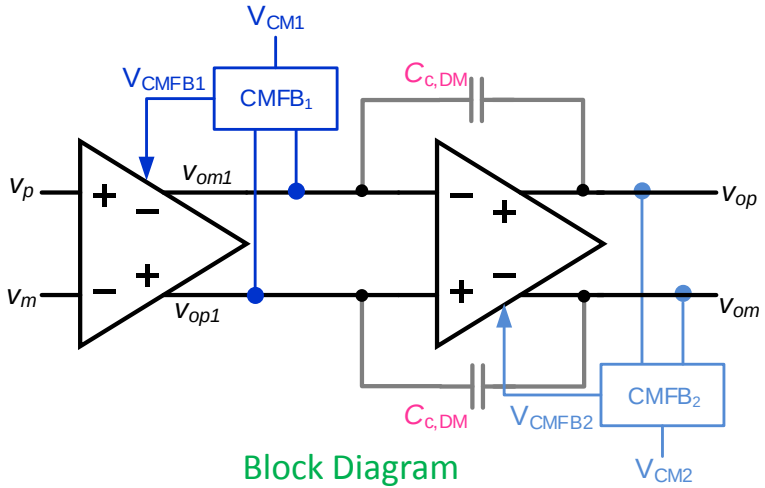




Block Diagram

- What is the best strategy to set the CM-level at the output of both gain stages?

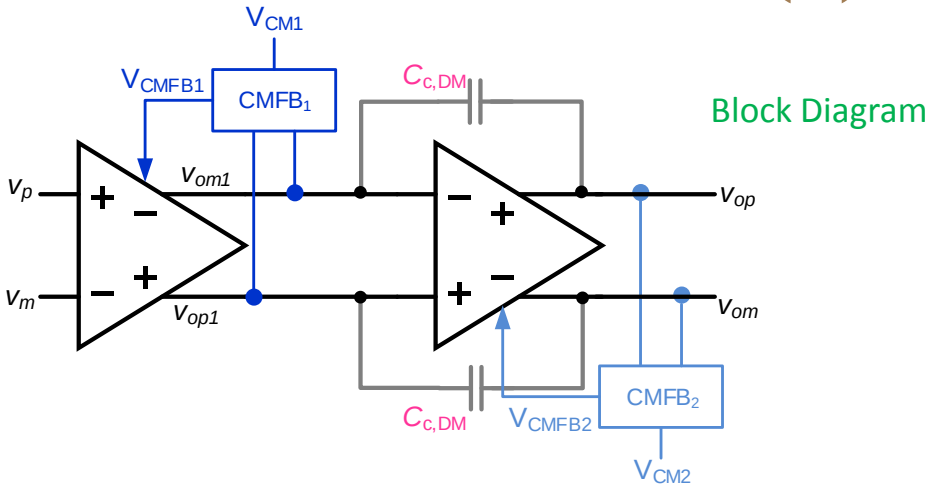
TWO-STAGE FD OPAMP CMFB (1)



Block Diagram

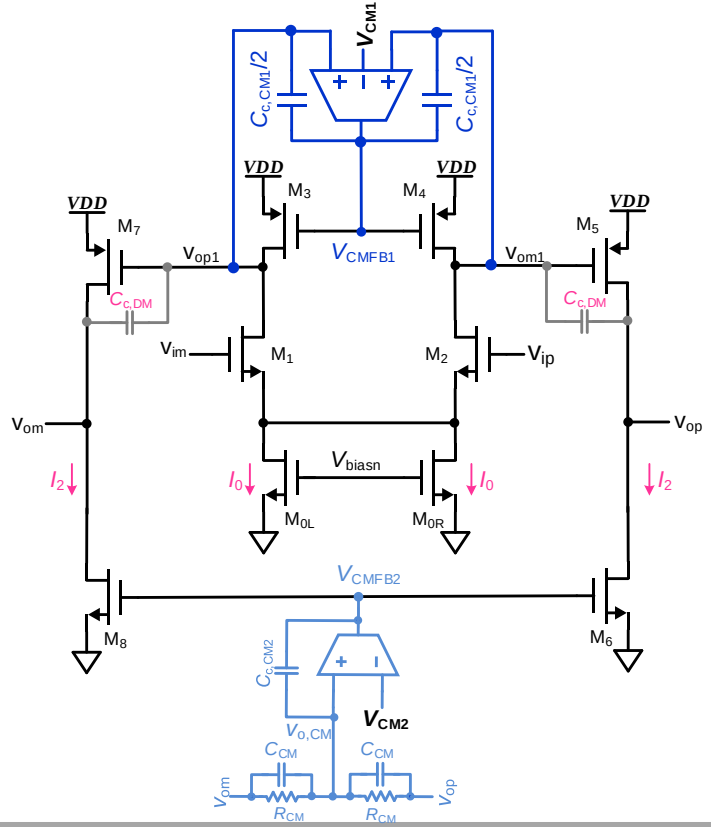
- Employ individual CMFB loops for each of the gain stages (robust scheme)
- 1st stage (high-gain) mustn't be loaded → Dual diff-pair CM-detector
- 2nd stage should allow large output swing → Resistive CM-detector

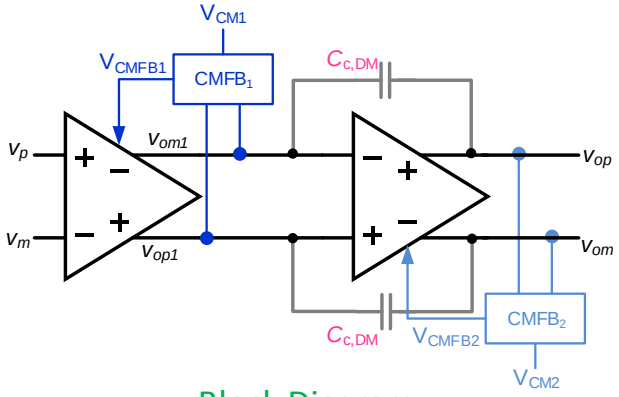
TWO-STAGE FD OPAMP CMFB (2)



- What are the reasonable voltages for V_{CM1} and V_{CM2}?
- V_{CM1} sets the bias for the second gain stage (=V_{biasp} in our example)
- V_{CM2} is the output CM-level and is dictated by the overall application circuit
  - $V_{DD}/2$ is commonly used to allow maximum output swing

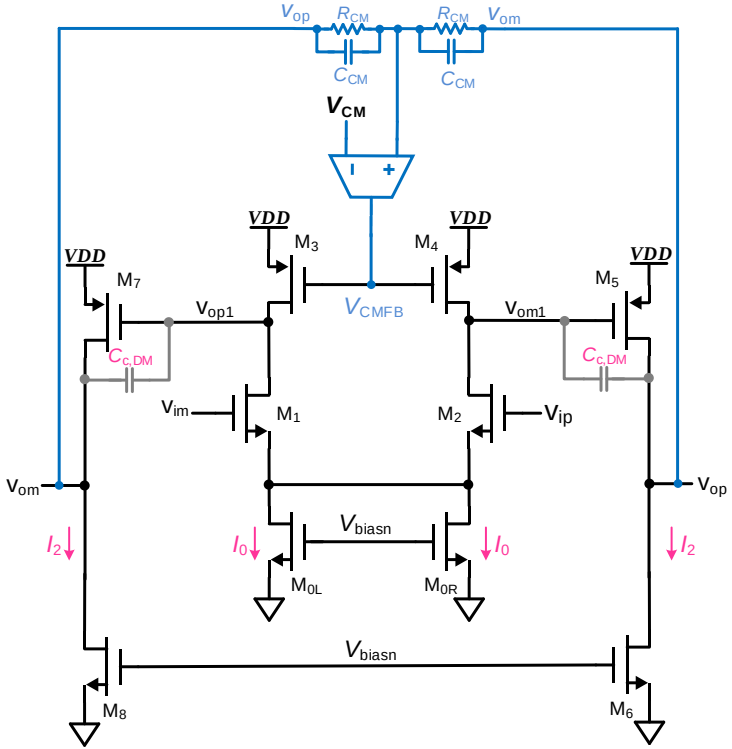
TWO-STAGE FD OPAMP CMFB (3)

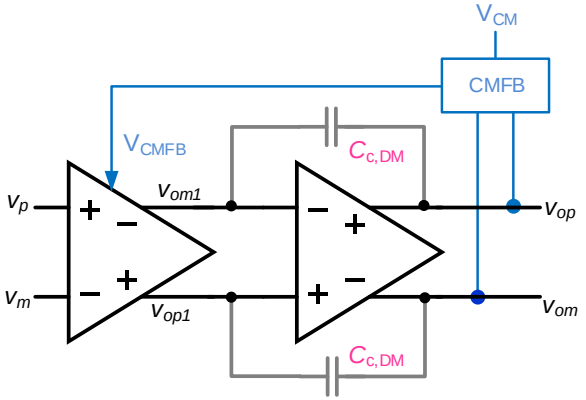




Block Diagram

TWO-STAGE FD OPAMP: SINGLE-LOOP CMFB (1)



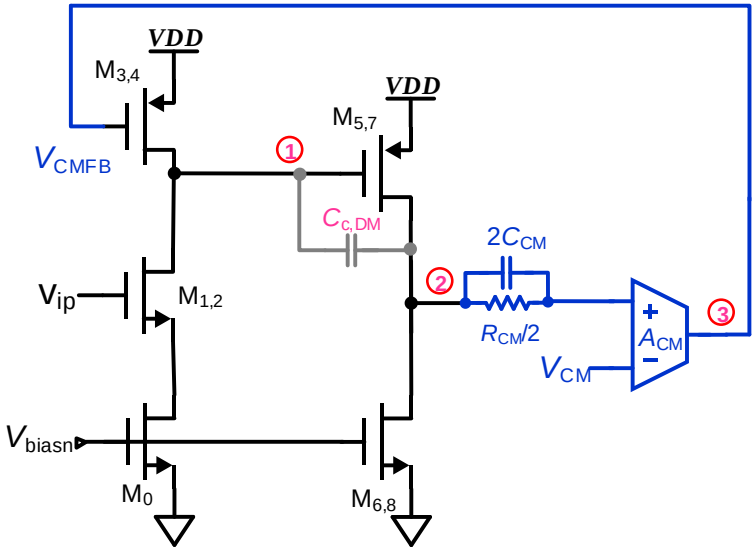


Block Diagram

- What if we just have one CMFB loop wrapped around both the gain stages?

TWO-STAGE FD OPAMP: SINGLE-LOOP CMFB (2)

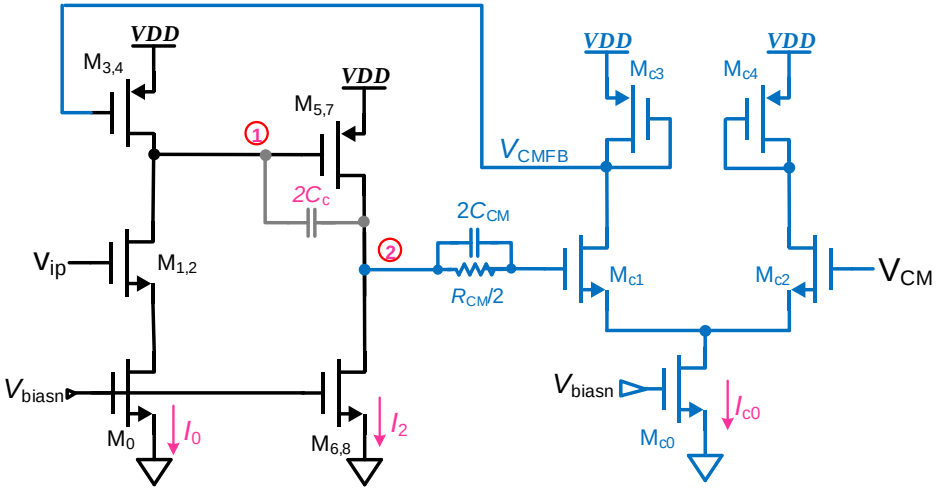
- 3 low-frequency poles in the CM-equivalent circuit ☹
- Need to compensate like a three-stage Opamp (higher complexity)
- Solution: Get rid of one of the high-impedance nodes to move the pole to higher frequencies



Common-mode Equivalent Circuit

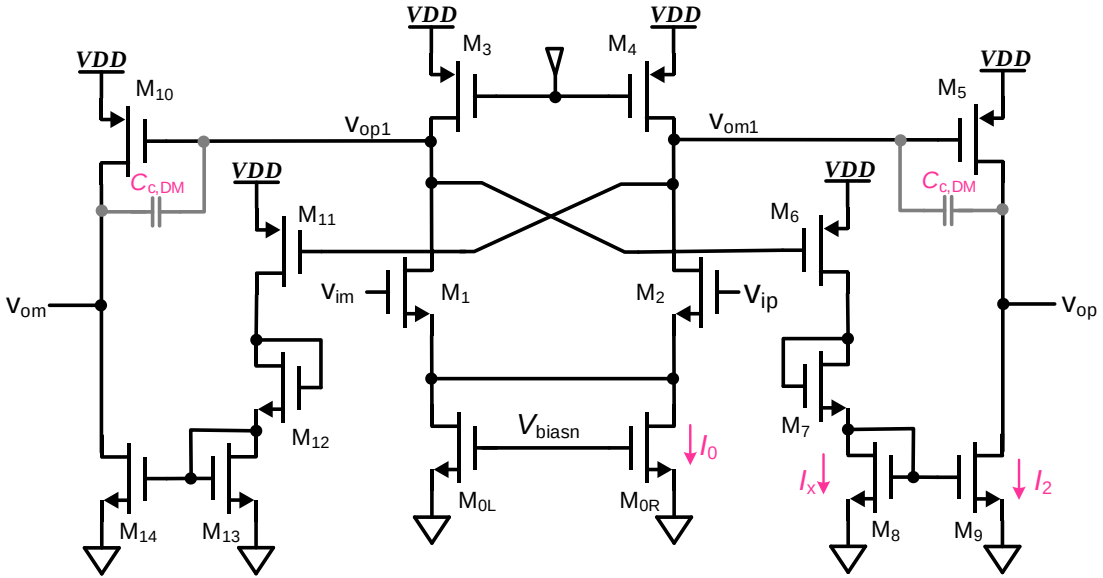
TWO-STAGE FD OPAMP: SINGLE-LOOP CMFB (3)

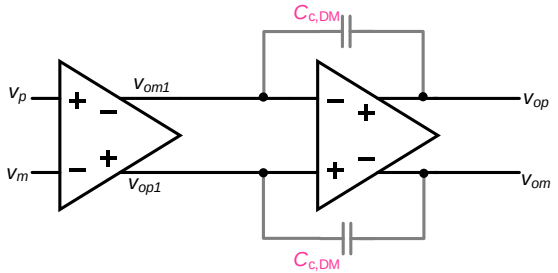
- Use diode-connected load in the error amp
  - low gain, A_{CM}~1
  - Only two low-f poles ☺
- Loop provides large CMFB gain
- DM compensation caps compensate the CMFB as well
  - Only control knob is n: $I_{c0}=I_0/n$
  - See notes for detailed analysis
- Use same current density in the error amp, as the two gain stages
- Not as robust against PVT variations



Common-mode Equivalent Circuit

TWO-STAGE CLASS-AB FD OPAMPS (1)



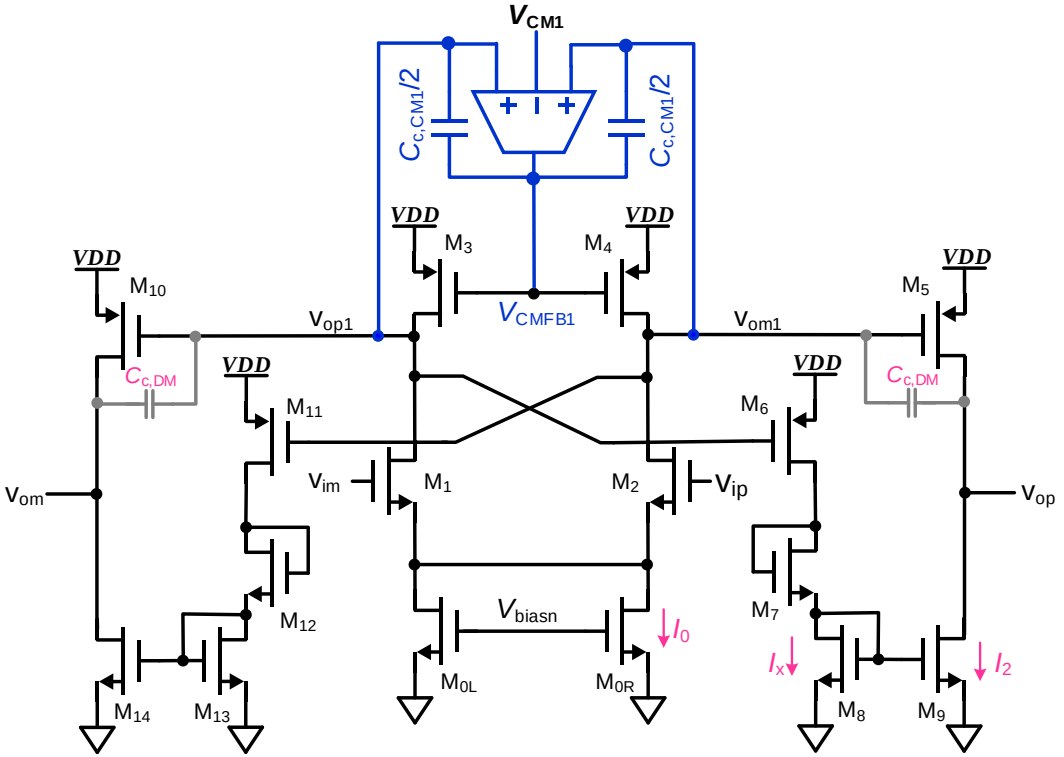


Block Diagram

- Note the crisscross biasing for the pseudo Class-AB (push-pull) output stage
- Diode-connected $M_{7,12}$ are added to decouple $V_{GS9,14}$ from $M_{6,11}$
- I_x is minimized to save power (but use same current density in all branches)

TWO-STAGE CLASS-AB FD OPAMPS (2)

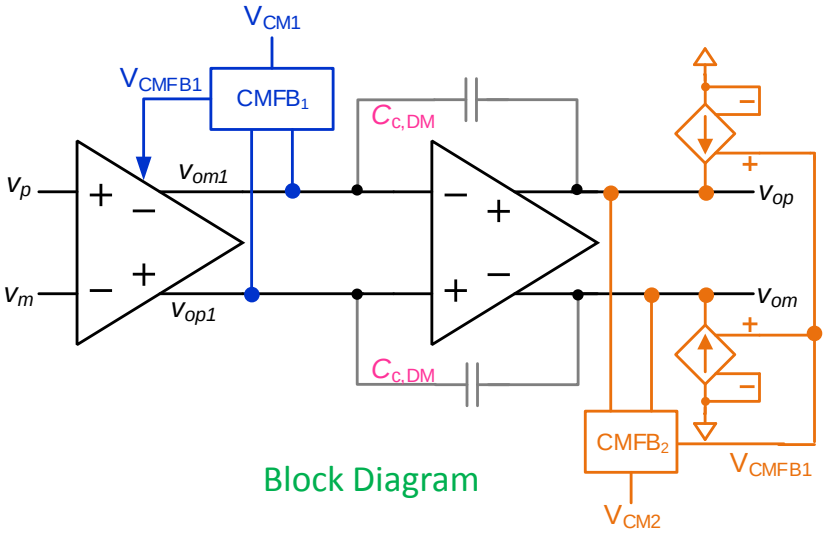
- 1st stage CM-level can be set using the DDP CM-detector
- How to set the output CM-level for the 2nd stage?
- Note that the previous CMFB method was suitable only for Class-A stage!
  - Need creative ways of controlling the output CM-level



CLASS-AB STAGE CMFB METHODS

- Several methods have been developed and tried
  - Passive feedback using resistors
  - CMFB based on Current-injection
  - Triode-device based CMFB
- You can come up with your own!

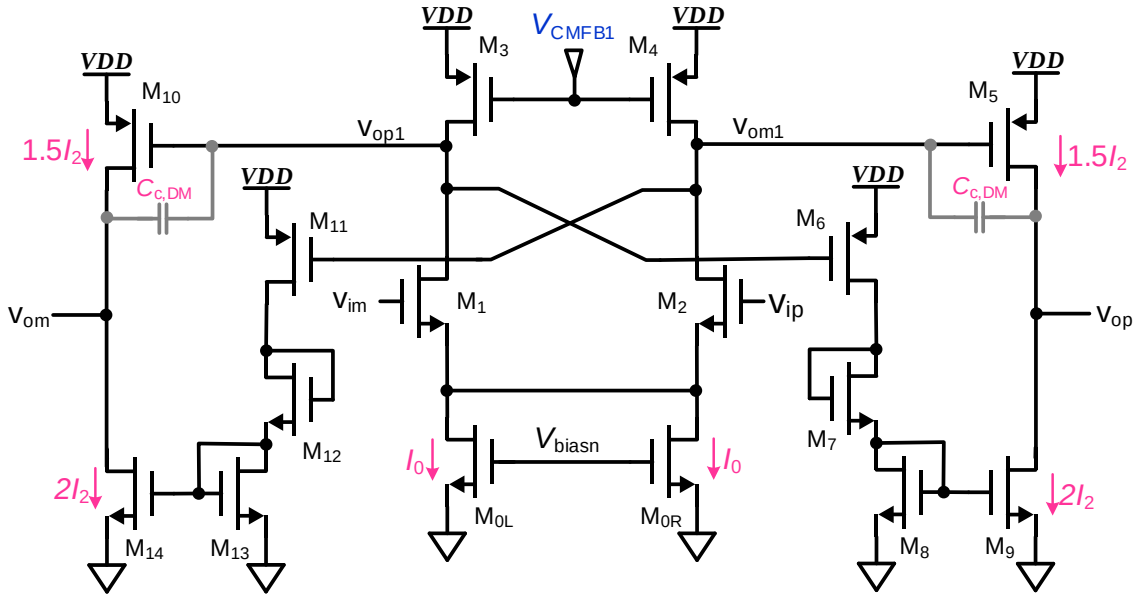
CLASS-AB CMFB: CURRENT INJECTION (1)

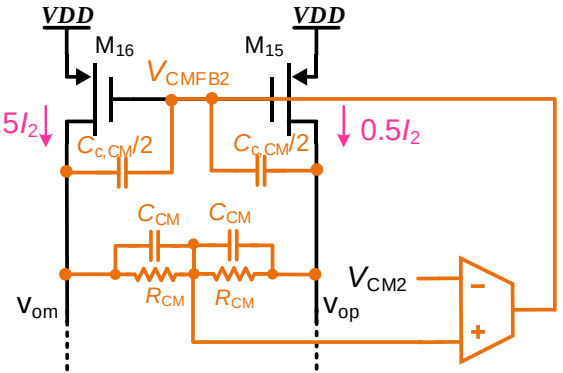


Block Diagram

- Two-independent CMFB loops
- Inject or remove DC current from the output stage to set its out CM-level
- Elegant scheme

CLASS-AB CMFB: CURRENT INJECTION (2)





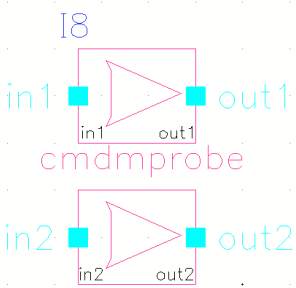
- A ¼ current branch injects/removes current into/from the output nodes to control their CM-level
- 3:1 DC current split for I_2 used to avoid potential instability (see paper)

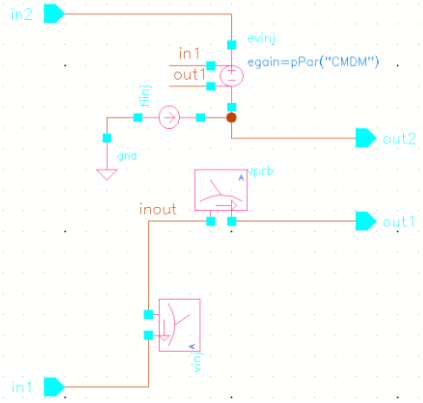
CLASS-AB CMFB: TRIODE-DEVICE (1)

- TBD

FULLY-DIFFERENTIAL OPAMP SIMULATION

CMDM PROBE

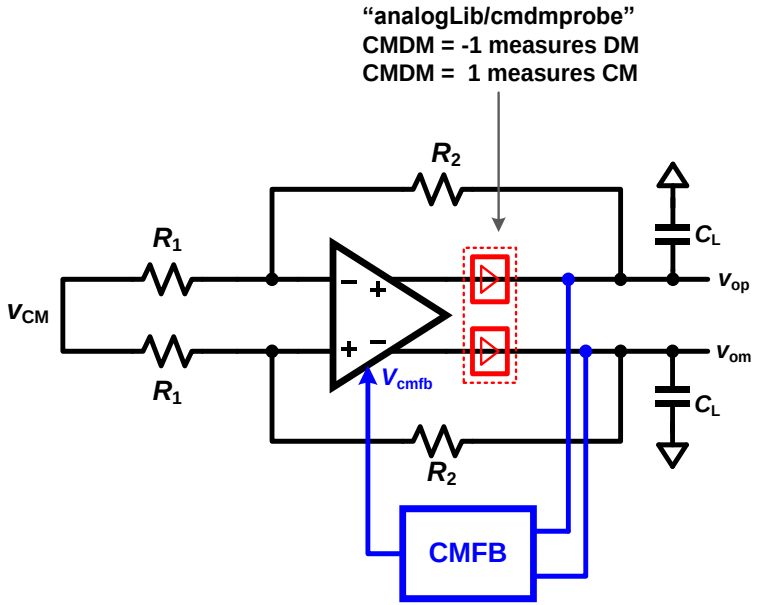




- Located in Spectre library: AnalogLib→cmdmprobe
- Variable CMDM needs to be set in he model
  - -1 measures differential mode response
  - +1 measures common mode response
- In IC615, diffstbprobe is available which handles unbalanced differential circuits better than the cmdmprobe.
- More information on the differential probes and the STB analysis algorithm can be found in [4].

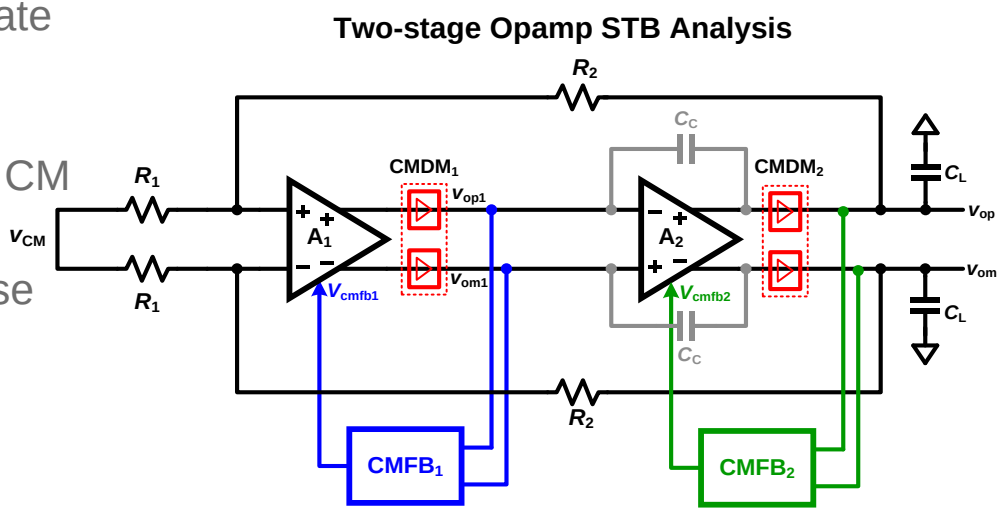
FULLY DIFFERENTIAL CIRCUIT ANALYSIS

- Use CMDM probe for differential analysis [1, 3]
- Placement of the CMDM probe should break the differential as well the common-mode loop(s).



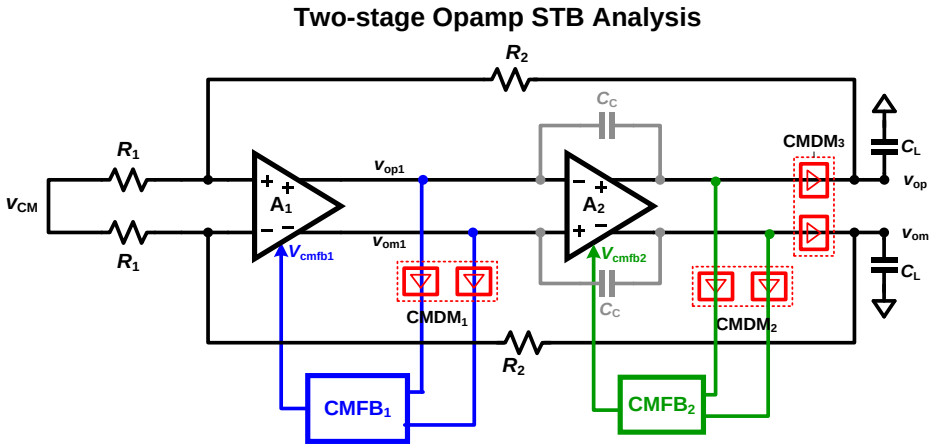
FD CIRCUIT ANALYSIS SETUP 1

- For internal loops, isolate those loops individually and perform STB analysis
  - Ensure overall DC feedback for accurate biasing, and ensure that all loops are compensated
  - $CMDM_1$ measures only the first-stage CM response
  - $CMDM_2$ measures overall DM response and second-stage CM response

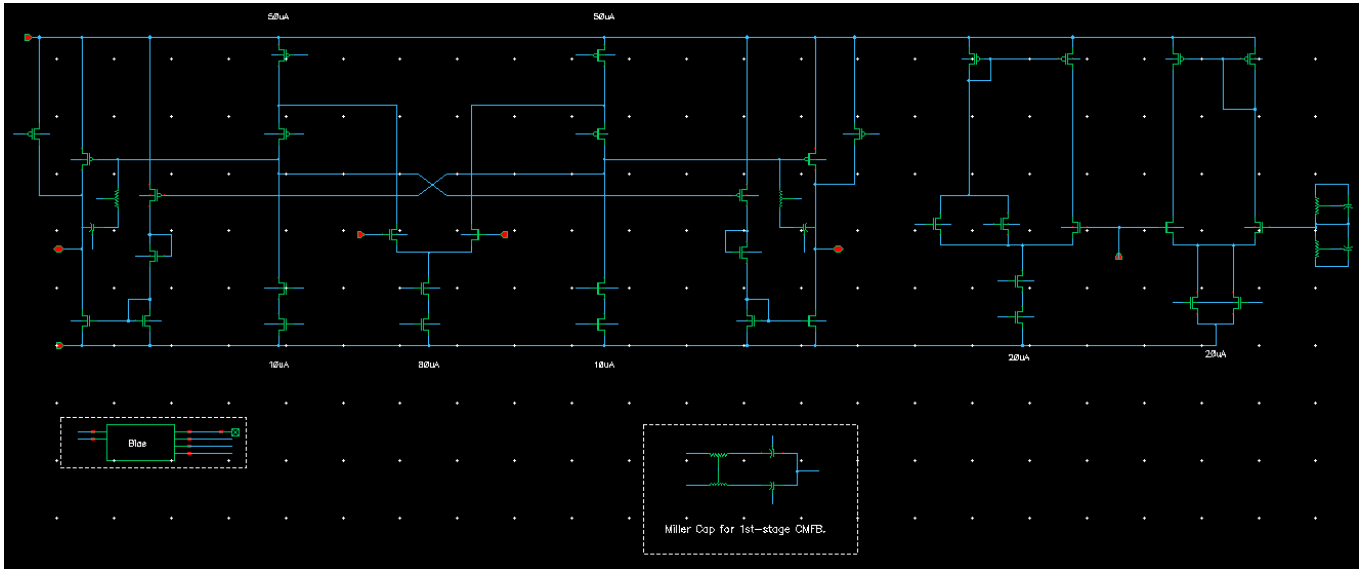


FD CIRCUIT ANALYSIS SETUP 2

- cmdmprobes placed outside DM loop, only in CMFB loops
  - $CMDM_1$ measures only the first-stage CM response
  - $CMDM_2$ measures only the second-stage CM response
  - But need another $CMDM_3$ probe to measure DM loop stability
  - Results match with iprobe results very well.

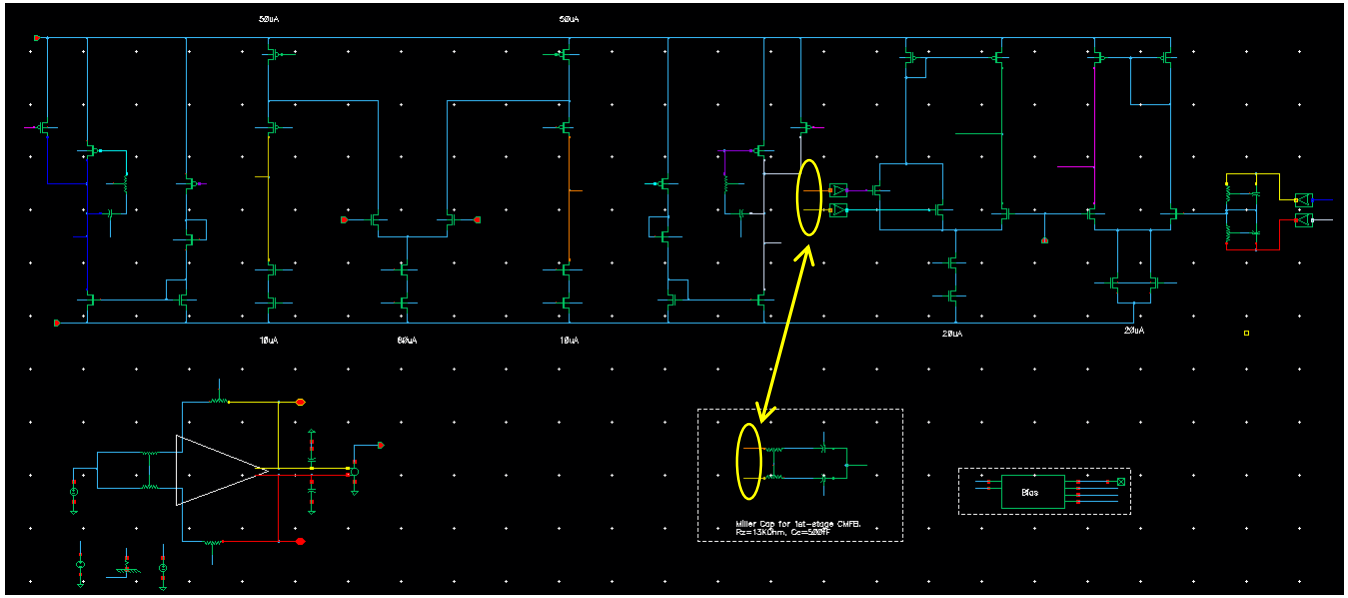


Fully Differential Opamp Schematic



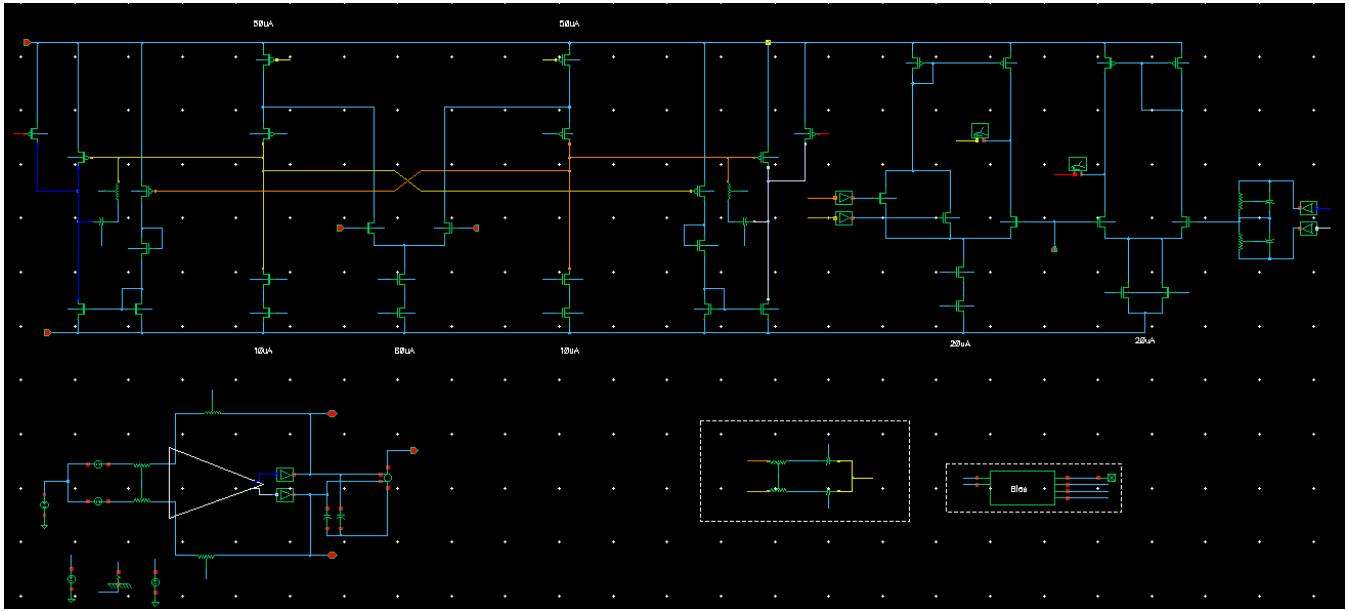
- Two-stage fully differential opamp
- Class AB output stage for large voltage swing
- With individual CMFB.
- 1st stage CMFB compensated

STB Analysis Using Method 1



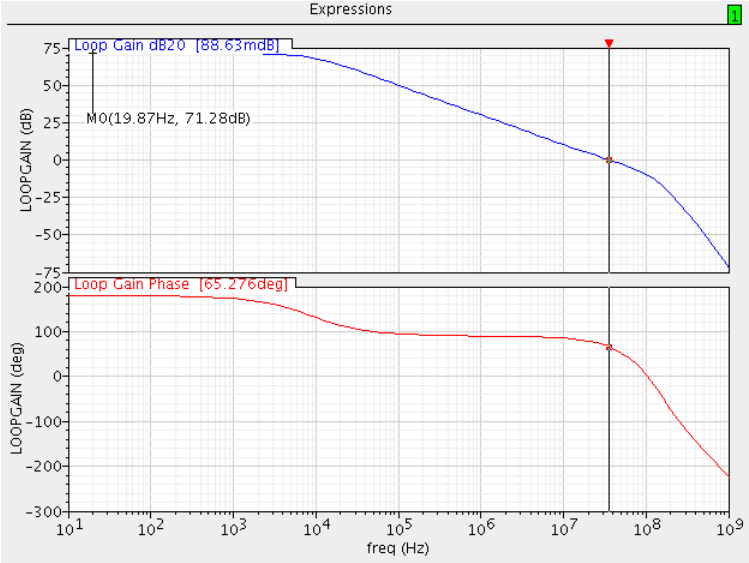
- Be noted that the nulling resistors should be connected before the inputs of cmdmprobe in the 1st CMFB loop, or it will generate incorrect results.

STB Analysis Using Method 2



- Need one extra cmdmprobe to measure DM loop comparing to method 1.

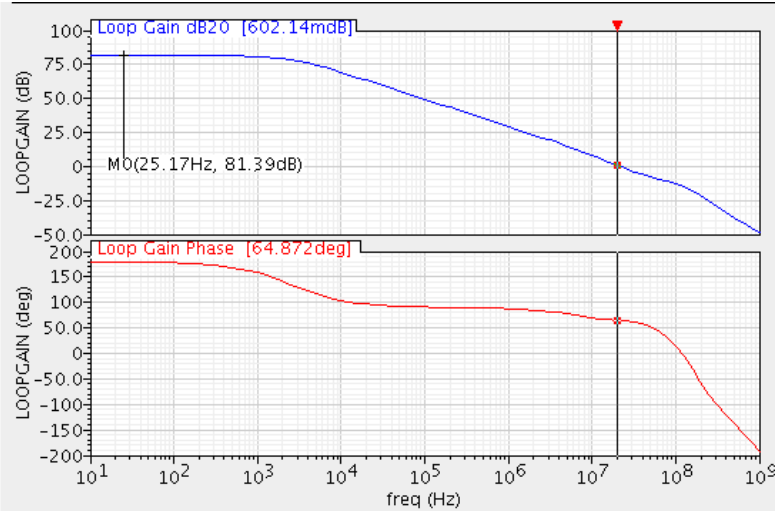
DM LOOP BODE PLOTS M1&M2




```
Phase margin = 65.1422 Deg at frequency = 36.1282 MHz.
```

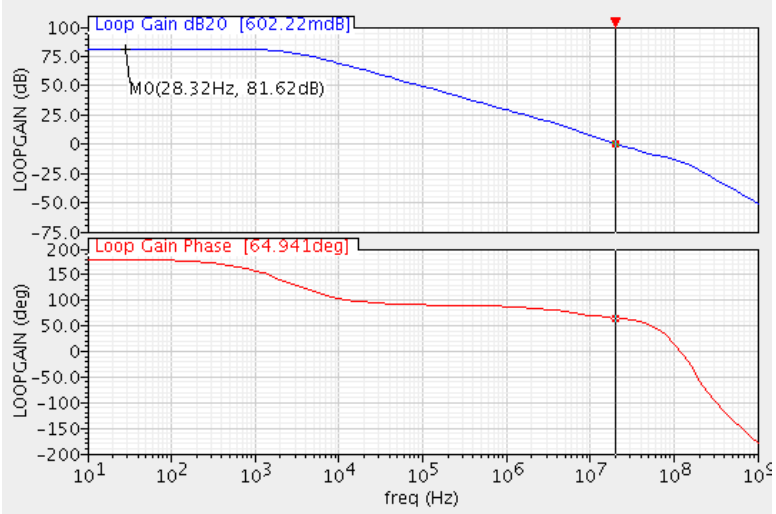
- Differential Mode loop gain and phase margin plots
- Same results obtained by using Method 1 and Method 2

1st Stage CMFB Loop Bode Plots



Phase margin = 64.5059 Deg at frequency = 21.2729 MHz.

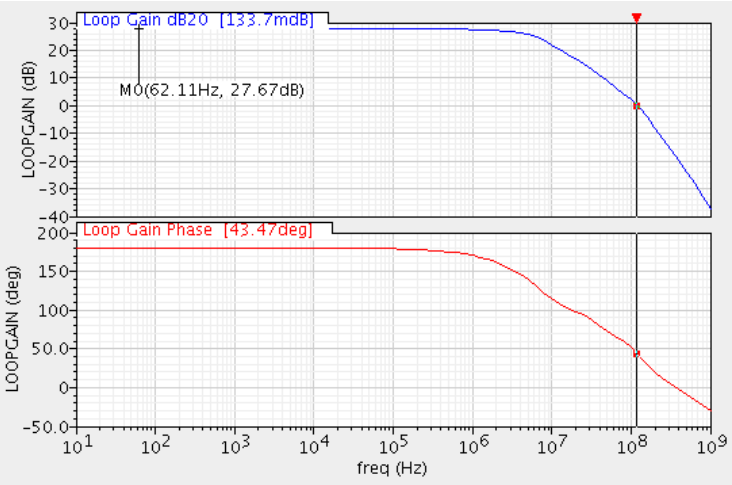
Method 1

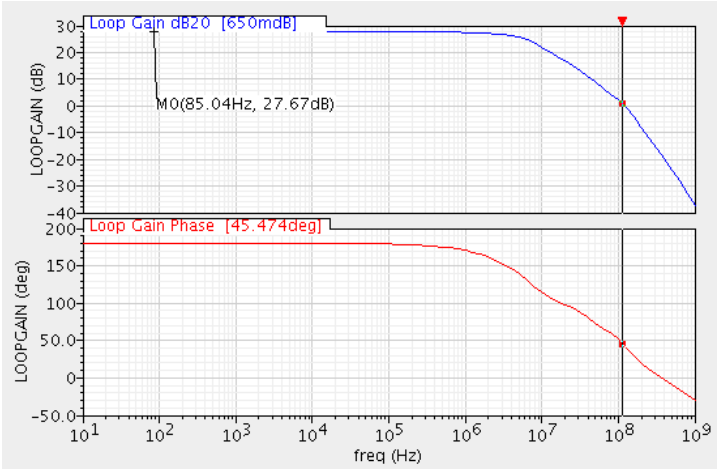


Phase margin = 64.5788 Deg at frequency = 21.2722 MHz.

Method 2

2ND STAGE CMFB LOOP BODE PLOTS





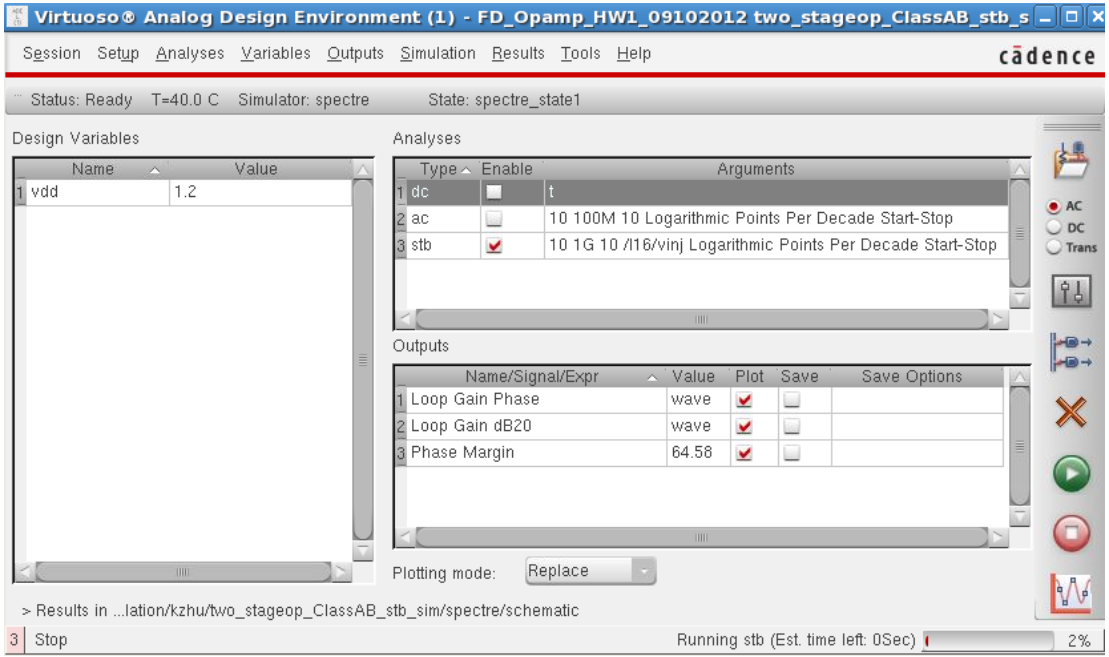

```
Phase margin = 42.6336 Deg at frequency = 119.604 MHz.
```

Method 1

```
Phase margin = 42.376 Deg at frequency = 119.867 MHz.
```

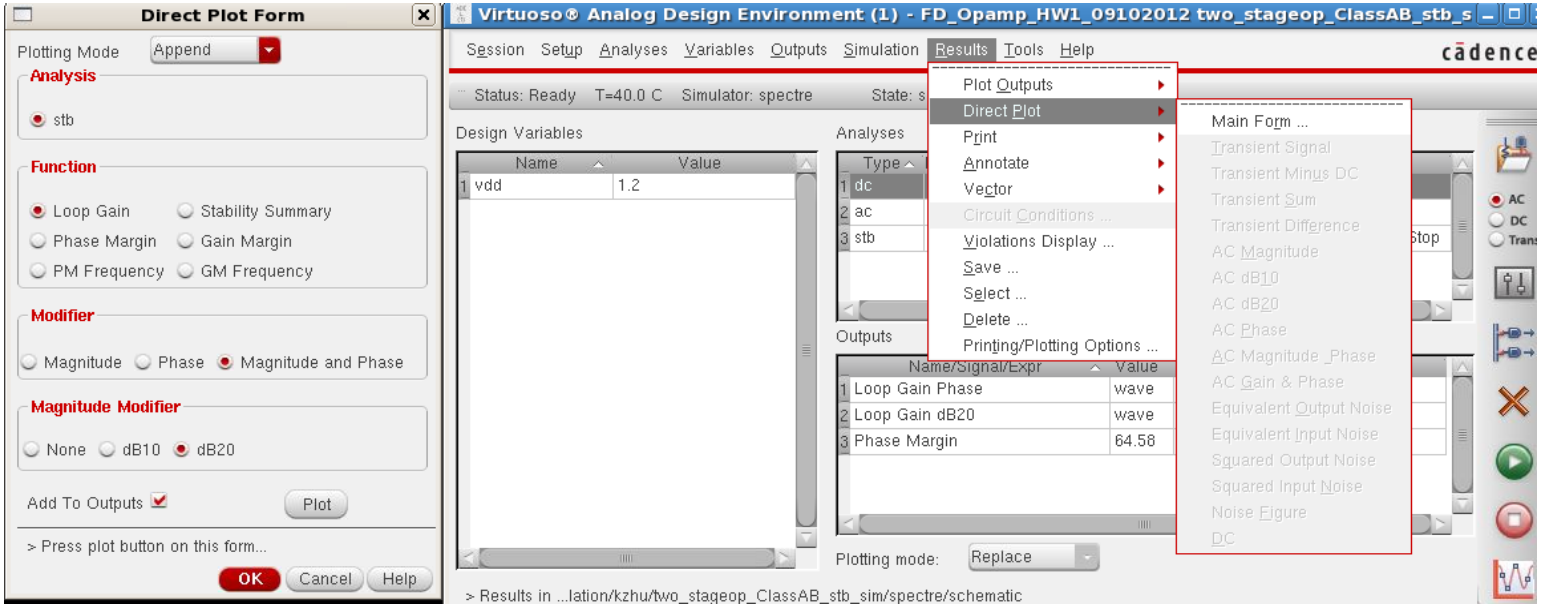
Method 2

SIMULATION SETUP



Use previous oppt (operating point) in the stb analysis

BODE PLOT SETUP

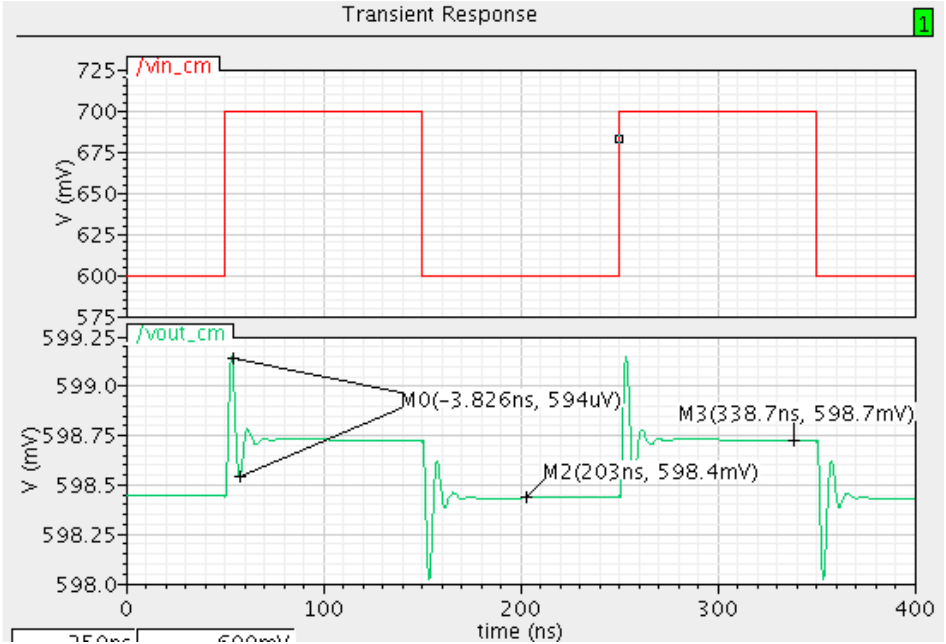


Results ⟶ Direct Plot ⟶ Main Form

DM TRANSIENT

Unity- gain inverting amplifier transient response with a 200mV differential step (rise/fall time=0.1ns, pulse with=100ns)

CM TRANSIENT

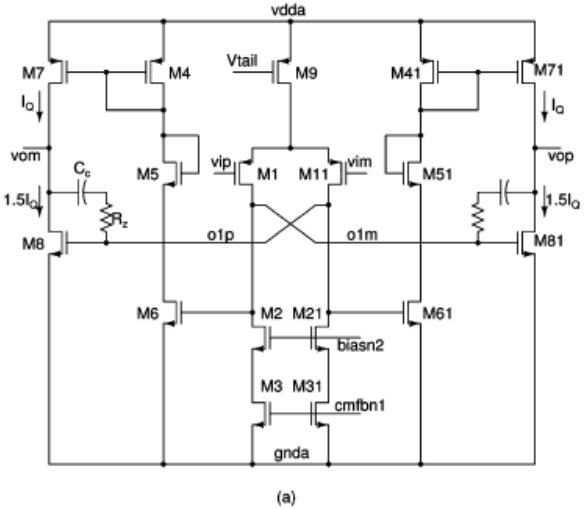


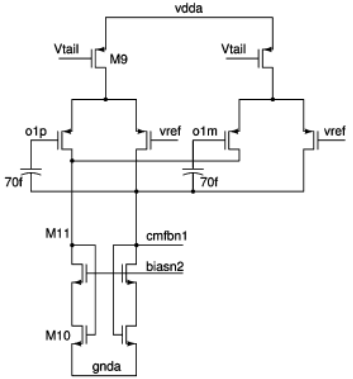
Unity- gain inverting amplifier transient response with a 100mV common mode step (rise/fall time=0.1ns, pulse with=100ns)

FULLY-DIFFERENTIAL OPAMP CMFB EXAMPLES

A Power Optimized Continuous-Time ΔΣ ADC for Audio Applications

Shanthi Pavan, Nagendra Krishnapura, Ramalingam Pandarinathan, and Prabu Sankar





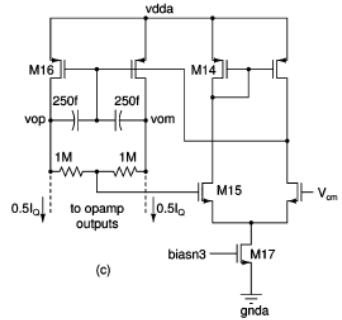


Fig. 8. Operational amplifier used in the first integrator. (a) Main amplifier. (b) Common-mode feedback (CMFB) for the first stage. (c) Second-stage CMFB circuit.

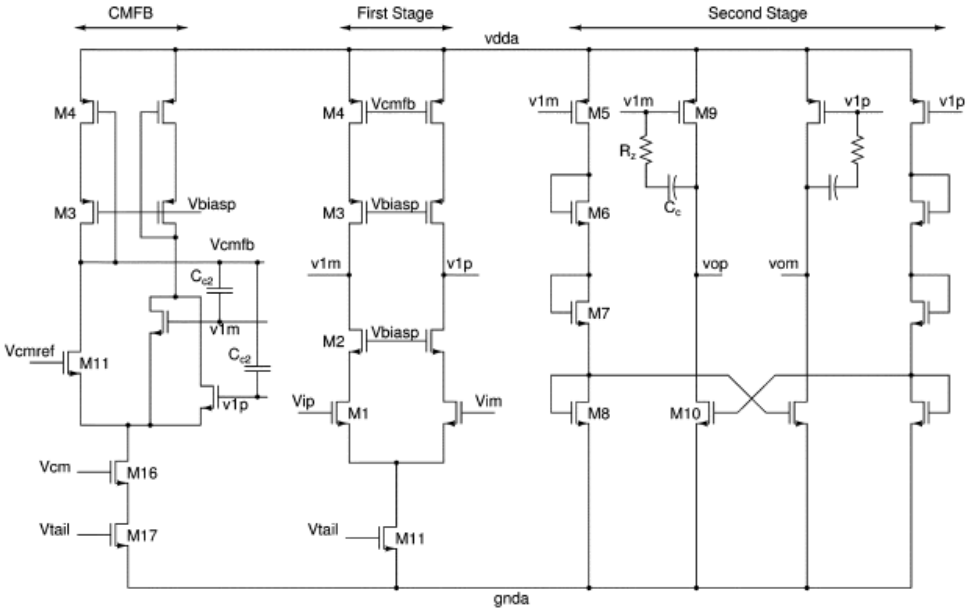
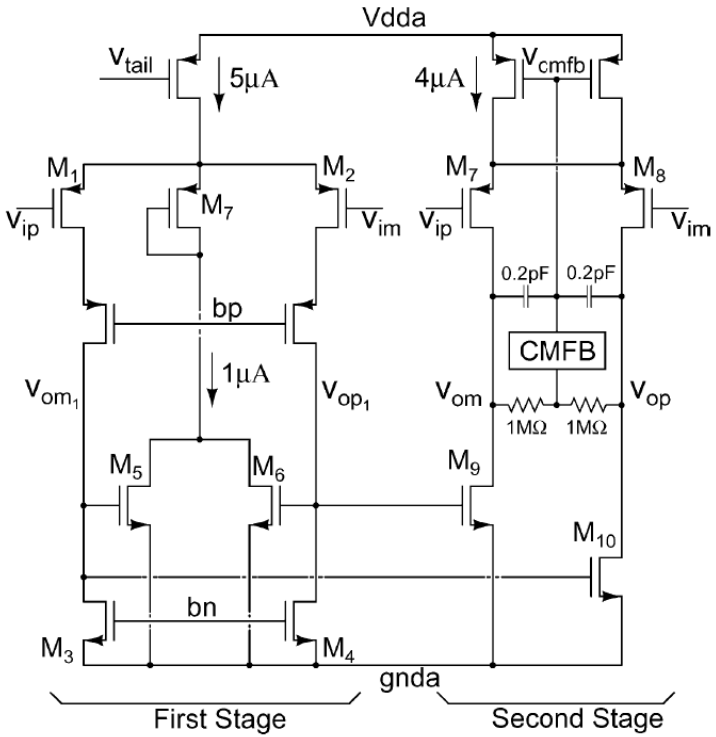


Fig. 9. Schematic of the operational amplifier used in the second and third integrators and the summing amplifier.

University of Idaho
College of Engineering

Power Reduction in Continuous-Time Delta-Sigma Modulators Using the Assisted Opamp Technique

Shanthi Pavan, *Member, IEEE*, and Prabu Sankar



A 16 MHz BW 75 dB DR CT ΔΣ ADC Compensated for More Than One Cycle Excess Loop Delay

Vikas Singh, Nagendra Krishnapura, Shanthi Pavan, Baradwaj Vigraham, Debasish Behera, and Nimit Nigania

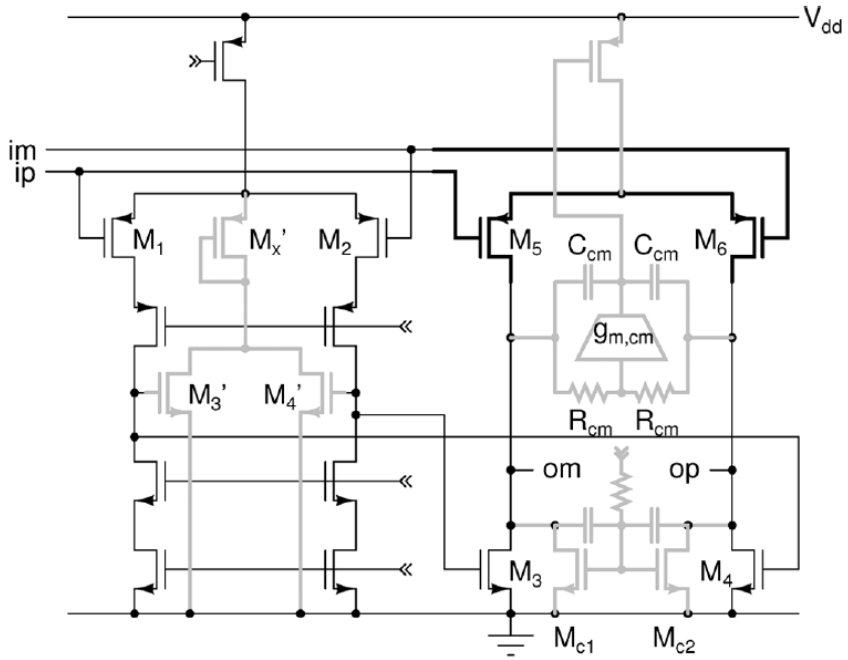
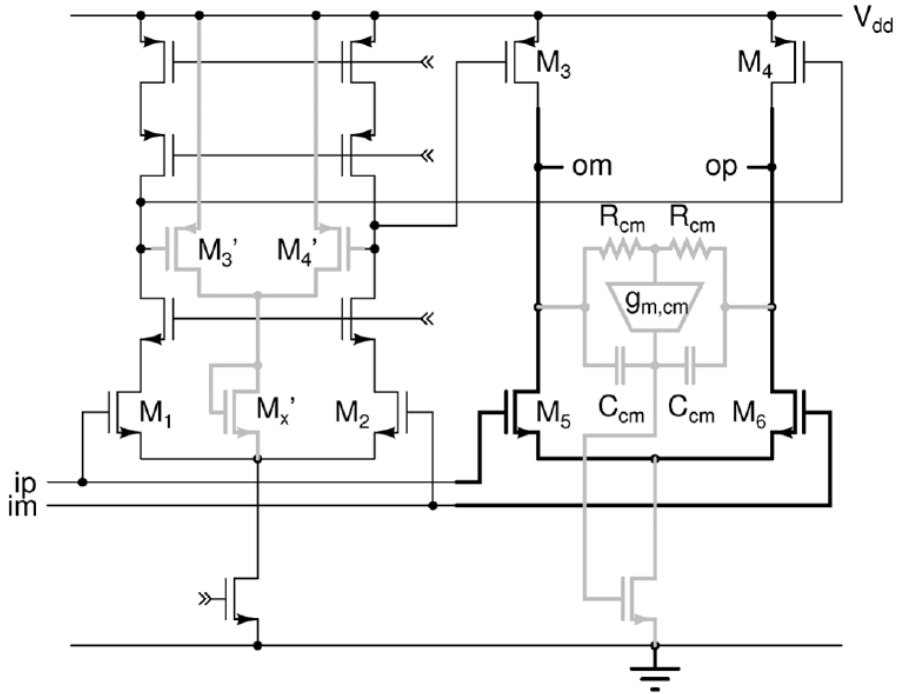


Fig. 12. Feedforward compensated opamp used in the first integrator. Feedforward path is shown in bold, and CMFB paths are shown in gray.


Vdd
M3
M4
om
op
Rcm
Rcm
M3'
M4'
gm,cm
M1
Mx'
M2
M5
Ccm
Ccm
M6
ip
im

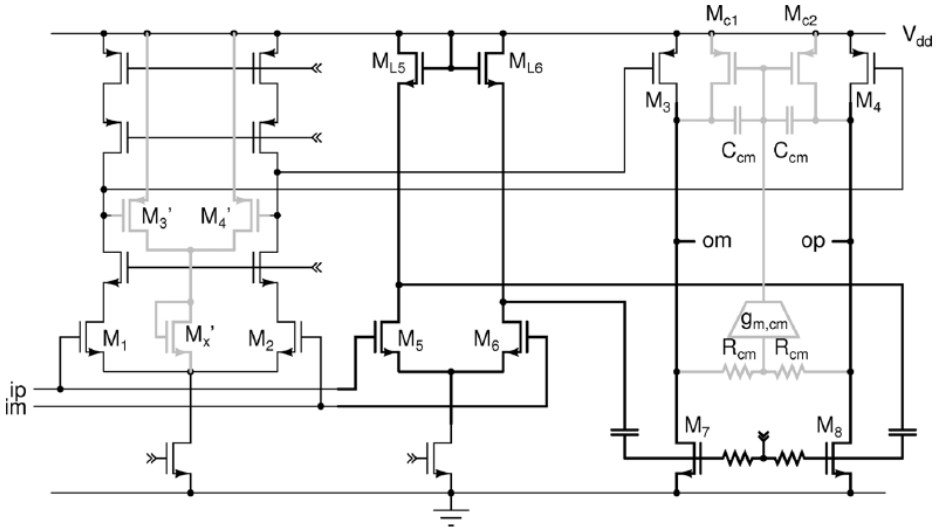
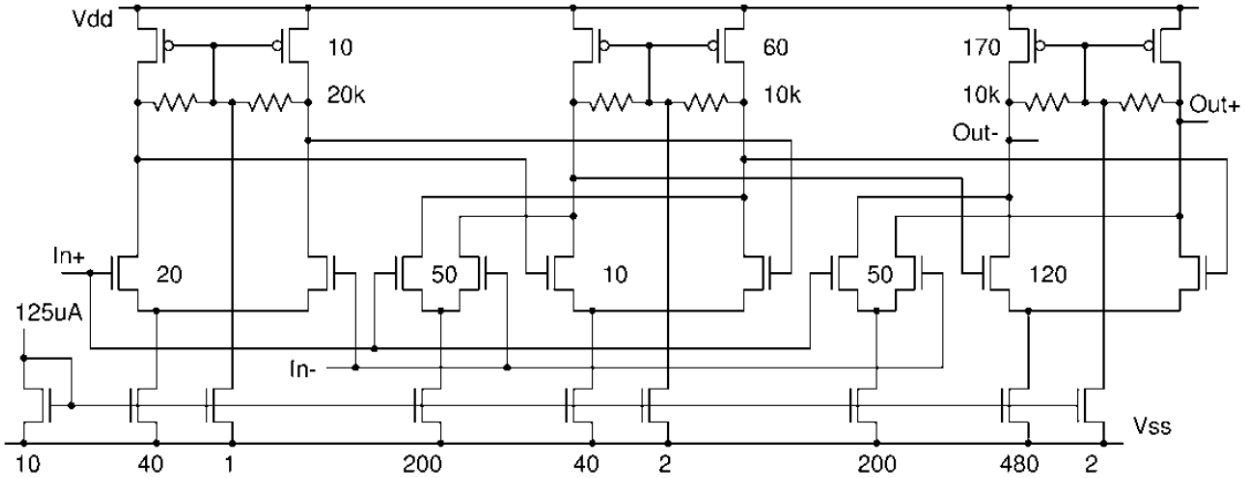


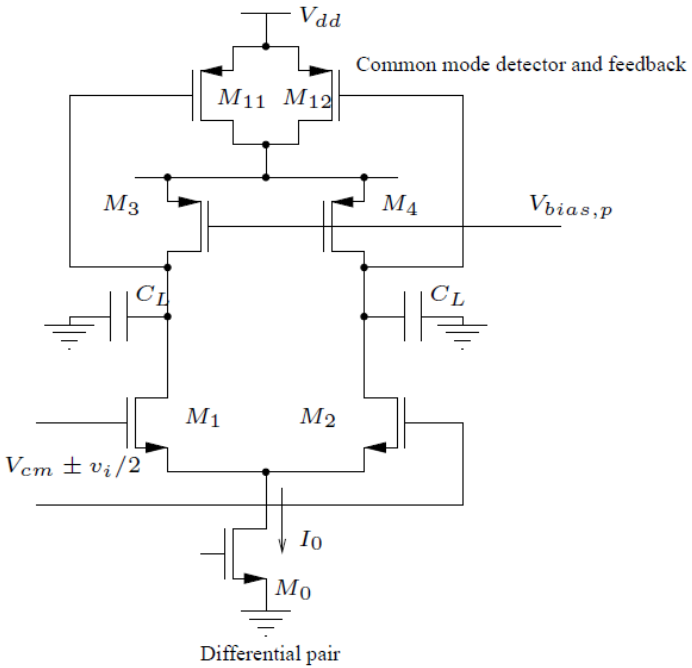
Fig. 14. Feedforward compensated opamp used in the summing amplifier. Feedforward path is shown in bold, and CMFB paths are shown in gray.

7.4 A 500MHz CMOS Anti-Alias Filter using Feed-Forward Op-amps with Local Common-Mode Feedback

Jeffrey Harrison, Neil Weste

Department of Electronics, Macquarie University, Marsfield, Australia




V_{dd}
Common mode detector and feedback
M_{11} M_{12}
M_3
M_4
$V_{bias,p}$
C_L
C_L
M_1
M_2
$V_{cm} \pm v_i/2$
I_0
M_0
Differential pair

REFERENCES

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2. Spectre User Simulation Guide, pages 160-165: http://www.designers-guide.org/Forum/YaBB.pl?num=1170321868
3. M. Tian, V. Viswanathan, J. Hangtan, K. Kundert, "Striving for Small-Signal Stability: Loop-based and Device-based Algorithms for Stability Analysis of Linear Analog Circuits in the Frequency Domain," *Circuits and Devices*, Jan 2001. http://www.kenkundert.com/docs/cd2001-01.pdf
4. https://secure.engr.oregonstate.edu/wiki/ams/index.php/Spectre/STB