Robust Design of Rail-to-Rail CMOS Operational Amplifiers for a Low Power Supply Voltage

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***Abstract*—New bias circuits which provide currents to n- and p-channel differential pairs placed in parallel are introduced. The bias currents are a function of the input common mode voltage in such a way that the total transconductance, g_{mT}, of the differential pairs is constant over the entire common mode range. The bias circuits, together with the differential pairs, are used to design input stages of low-voltage ($\leq$3.3V) complementary metal-oxide-semiconductor (CMOS) operational amplifiers (opamps). The new circuits are robust in that they do not require transconductance parameter matching of n- and p-channel transistors for proper operation. A simple rail-to-rail common source output stage with class AB control is also developed and used in the design of two-stage opamps.**

Experimental results of MOSIS test chips containing a family of low-voltage opamps fabricated in 2μm p-well process are provided. The results demonstrate the effectiveness and robustness of the proposed constant transconductance input stages in achieving constant opamp unity gain frequency with very low levels of total harmonic distortion (THD) and with 3.3 V and 2.5 V power supply voltage.

I. Introduction

In recent years, low voltage VLSI circuits have received considerable attention in the field of microelectronics [1] [2]. With the reduction of power supply voltage to 3 V, many of the existing complimentary metal-oxide-semiconductor (CMOS) analog building blocks, designed to operate from higher supply voltages, will lose a significant amount of operating range. CMOS opamps will be affected by this change, especially at their input stage [3], [4]. Thus, circuit design techniques which regain the operating range while maintaining good performance must be developed.

Many CMOS opamps [5] evolved from their bipolar counterparts [6] and hence possess similar characteristics. However, since metal-oxide-semiconductor (MOS) transistors require larger turn on and saturation voltages for active region operation, the signal swing of a CMOS circuit is usually more limited than that of the bipolar version for a given circuit topology. For the usual differential pair used as an input stage of an opamp, with 1-V V_T and a 3-V power supply, the input common mode range is less than 2 V. This is a significant limitation, especially if the opamp is intended for use as a general purpose one, e.g., used as a unity gain buffer. The output swing is also decreased, although not as severely as the input stage swing. However, one can no longer use circuit techniques such as a low output resistance source follower in the design of low-voltage opamps.

In a simple rail-to-rail input stage, an n-channel differential pair and a p-channel differential pair are used in parallel as shown in Fig. 1, which also shows the bipolar version. There are basically three operation regions; when the common mode voltage, V_{CM}, is near the negative power supply, V_{SS}, only the p-channel pair operates. For V_{CM} near the positive power supply, V_{DD}, only the n-channel pair operates. For V_{CM} around mid-rail, both differential pairs operate. That is, at least one of the two differential pairs will be operating for any V_{CM} between the rails.

In opamp design, one of the most important circuit parameters is the transconductance, g_m, of the input stage. The total input stage transconductance, g_{mT} of the circuits in Fig. 1 is given by the sum of the transconductance of the n- and p-channel (or -type) differential pairs, g_{mn} and g_{mp}, respectively. Since there are three regions of operation for the input stage, there are three different regions for g_{mT} which is given, in strong inversion, by

$$\begin{aligned} g_{mT} &= g_{mn} + g_{mp} \\ &= \sqrt{2K_nI_n} + \sqrt{2K_pI_p} \end{aligned} \tag{1}$$

where K_n and K_p are the transconductance parameters of the n- and p-channel input transistors. If I_n and I_p are provided by constant current sources consisting of n- and p-channel transistors, respectively, the variation in g_{mT} as a function of V_{cm} can be as much as 100%. This change is not desirable because it complicates the frequency compensation of opamps and also results in harmonic distortions as described below.

Assuming that the second pole, P_2, of an opamp is located at a sufficiently high frequency, the unity gain frequency, ω_U, or the gain-bandwidth product is given by

$$\omega_U = A_V P_1 = \frac{g_{mT}}{C_C} \tag{2}$$

where A_V is the dc gain, and P_1 is the first (or dominant) pole. In order to maintain a good amount of phase margin, P_2 must be placed at about two and half times ω_U. In other words, for a given g_{mT} and a second pole, P_2, C_C should be chosen such that $\omega_U = P_2/2.5$ to maximize the opamp gain-

Manuscript received July 15, 1994; revised July 6, 1995. This work was supported in part by a Semiconductor Research Corporation research contract.

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Publisher Item Identifier S 0018-9200(96)01290-5.

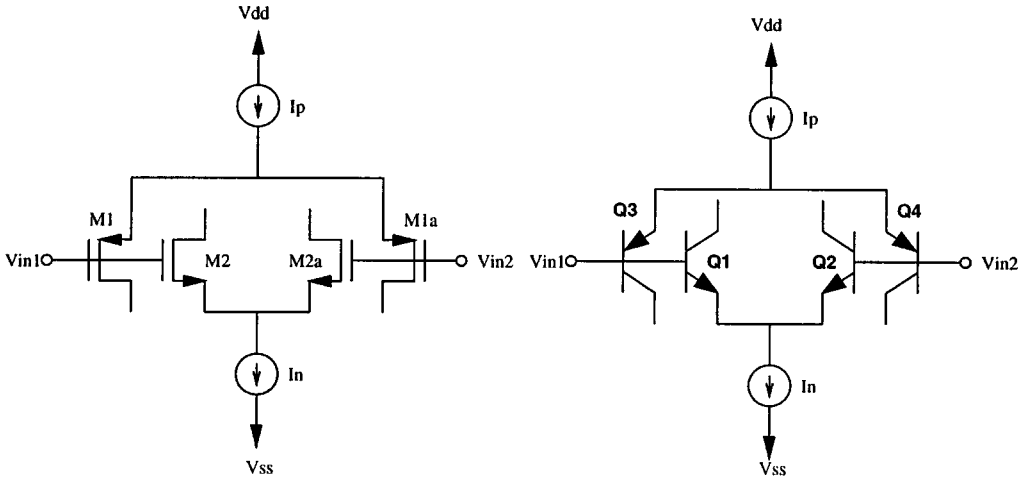


Fig. 1. Rail-to-rail input stage in CMOS and bipolar implementations.

bandwidth while maintaining a good opamp performance. All this would be possible provided that g_{mT}, which is a small signal parameter, is constant regardless of the value of the large signal, V_{CM}.

It can also be shown [7] that the higher order Fourier coefficients in the output expression of a buffer connected opamp are proportional to the first and higher order derivatives of the opamp open loop gain with respect to the input voltage. Since the input voltage of a buffer connected opamp is the common mode voltage and since the open loop gain is proportional to g_m, a constant-g_m will reduce these derivatives to zero resulting in very low distortion level.

In this paper, we describe robust CMOS circuit techniques in strong inversion for the design of constant-g_m complementary input stages. We also describe a simple CMOS rail-to-rail output stage with class AB control. We then use the proposed stages in the design of high performance low-voltage opamps and verify their performance experimentally. We will first investigate briefly the issue of matching MOS transistors of the opposite types and then proceed to describe the new circuit techniques and their implementation in silicon.

II. Constant-g_m Input Stages, $K_n = K_p$

When the input stage is constructed using bipolar transistors, it is not very difficult to make g_{mT} constant because the transconductance of a bipolar transistor is proportional to the collector current. Hence the only task needed is to keep the sum of the collector currents of the input pairs constant, i.e., when one of the differential pairs is turned off, the bias current is redirected to the pair which is operating. A similar argument can be made about an MOS implementation in weak inversion.

This is not so simple, however, for the MOS case in strong inversion because the transconductance of an MOS transistor is proportional to the square root of the drain current. Furthermore, g_m also depends on the type of transistor used, i.e., n- or p-channel. A solution was suggested recently [3], [4], [8], [9] under the assumption that an n-channel MOSFET can be matched to a p-channel MOSFET.

Assuming that n-channel transistors can be matched to p-channel transistors, i.e., $K_n = K_p = K$, (1) can be rewritten as follows:

$$g_{mT} = \sqrt{2K}(\sqrt{I_n} + \sqrt{I_p}). \tag{3}$$

Then $\sqrt{I_n}+\sqrt{I_p}$ must be kept constant to obtain a constant-g_m input stage. To our knowledge, this constitutes the basis for all previously published work in this area. Circuits that achieve this relationship based on the assumption that $K_n = K_p$ have been discussed by several authors, see e.g., [3] and [4].

Since

$$K_n = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_n \tag{4}$$

and

$$K_p = \frac{1}{2}\mu_p C_{OX}\left(\frac{W}{L}\right)_p \tag{5}$$

with prior knowledge of the ratio of the electron mobility to the hole mobility, μ_n/μ_p, the assumption $K_n = K_p$ should be made possible by proper design of $(W/L)_n$ and $(W/L)_p$. In general, different processes will have different values of μ_n/μ_p ratio. Furthermore, even in the same process the ratio can change considerably from run to run. To acquire more realistic information on the variation of the μ_n/μ_p ratio, several process parameter sets from vendors used by the MOSIS service were obtained. The μ_n/μ_p ratios obtained from the following processes: 1.2 μm HP, 1.2 μm HP-NID, 2.0 μm Orbit, and 2.0 μm VTI, are plotted in Fig. 2. The variations in the ratio can be as much as 30% for a particular process, that is if the design is carried out using the median value of the ratio, the final value may have a $\pm$15% deviation.

III. Constant-g_m Input Stages, $K_n \neq K_p$

In this section, robust design solutions for a rail-to-rail CMOS input stage with a constant-g_m and without the need for matching n-channel transistors to p-channel transistors are presented [10], [11].

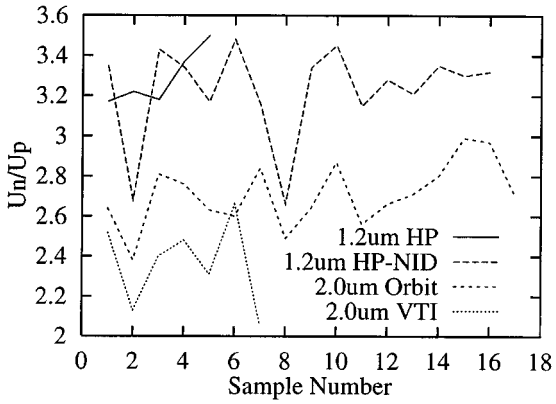


Fig. 2. Ratios of μ_n to μ_p for different runs and processes.

Constant-g_m bias circuit 1 is shown in Fig. 3(a). The input to the circuit is I_p; this is the monitored value of the current which is biasing the p-channel differential pair. The output of this circuit is I_n, and this biases the n-channel differential pair. Since V_C is constant, the sum of the gate to source voltages of M_3 and M_4 is always constant. Assuming that all transistors are operating in the saturation region in the strong inversion region, we have

$$V_C = V_{SG4} + V_{GS3} = V_{T4} + \sqrt{\frac{I_4}{K_p}} + V_{T3} + \sqrt{\frac{I_3}{K_n}}. \quad (6)$$

However, since $I_3 = I_p$ and $I_4 = I_n$, (6) can be rewritten as

$$V_C - V_{T3} - V_{T4} = \sqrt{I_p/K_n} + \sqrt{I_n/K_p}. \quad (7)$$

Multiplying the above by $\sqrt{K_n K_p}$, we have the following:

$$\sqrt{K_n K_p}(V_C - V_{T3} - V_{T4}) = \sqrt{K_n I_n} + \sqrt{K_p I_p}. \quad (8)$$

Since the source terminals of M_3 and M_4 are connected to fixed voltages, the threshold voltage of these transistors are constant to the first order, and the left side of (8) is constant. Since the currents I_p and I_n in the constant-g_m bias circuit are the same currents that are used to bias the input differential pairs, the right side of (8) is the total transconductance, g_{mT}, of the input stage (off by a factor of $\sqrt{2}$). Therefore, the circuit shown in Fig. 3(a) can be used to construct a constant-g_m input stage without matching n-channel MOS transistors to p-channel MOS transistors.

Constant-g_m circuit 2 is shown in Fig. 3(b). The drain current in M_4 is I_n, and this current is fed back into the source terminals of M_4 and M_5; a constant current I_d is also fed into this terminal and thus the current in M_5 equals I_d. A constant current I_c is fed into a diode connected M_6, then since both M_5 and M_6 are carrying constant currents, their gate-to-source voltages are constant. This establishes a constant voltage node at the source terminal of M_4 as it was in the constant-g_m bias circuit 1 shown in Fig. 3(a). Since the source terminals of M_3 and M_6 are both grounded, the following is always true:

$$V_{SG5} + V_{GS6} = V_{SG4} + V_{GS3}. \quad (9)$$

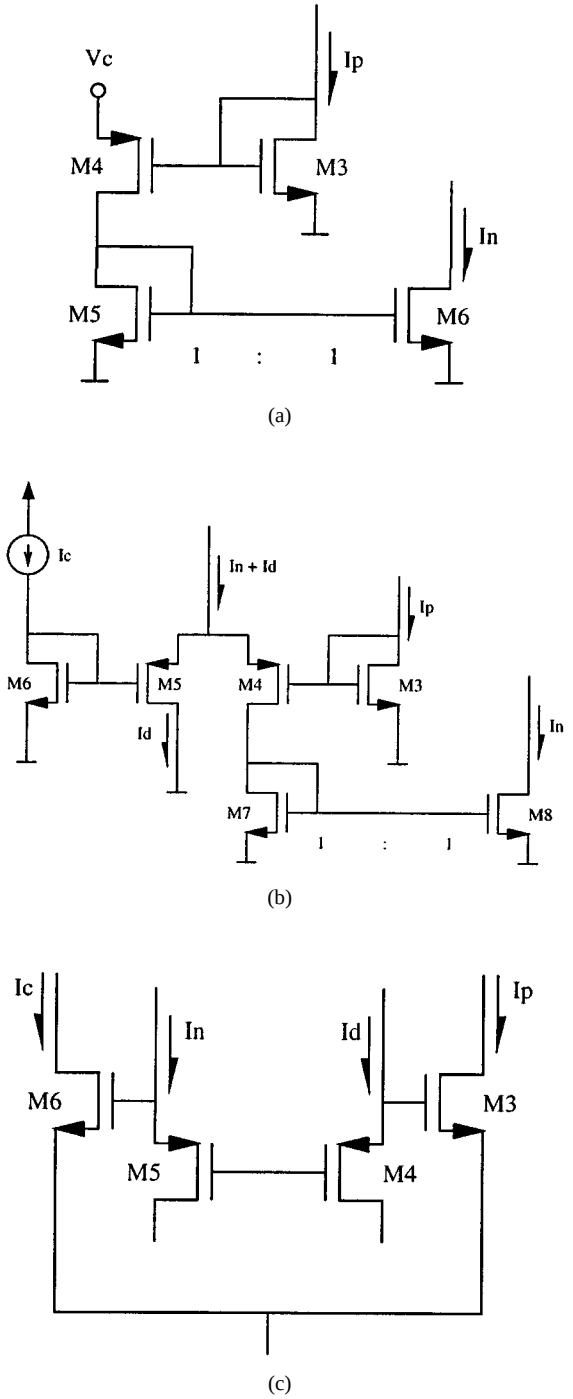


Fig. 3. New constant-g_m bias circuits. (a) Using a bias voltage, V_C, (b) using bias currents, I_c and I_d, and (c) an alternate realization using bias currents.

Assuming that all the transistors are operating in the saturation region (in strong inversion), (9) can be written as

$$\sqrt{\frac{I_c}{K_n}} + V_{T6} + \sqrt{\frac{I_d}{K_p}} + V_{T5} = \sqrt{\frac{I_n}{K_p}} + V_{T4} + \sqrt{\frac{I_p}{K_n}} + V_{T3}. \quad (10)$$

Since the p-channel transistors M_4 and M_5 have the same source terminals, the body effect on these transistor should cancel to the first order, that is, we can assume $V_{T4} = V_{T5}$. This is true for the n-channel transistors M_3 and M_6 and then

$V_{T3} = V_{T6}$ is also assumed. Using these facts, (10) becomes

$$\sqrt{\frac{I_c}{K_n}} + \sqrt{\frac{I_d}{K_p}} = \sqrt{\frac{I_n}{K_p}} + \sqrt{\frac{I_p}{K_n}}. \tag{11}$$

Multiplying both sides of (11) by $\sqrt{2K_nK_p}$, we get

$$\sqrt{2I_cK_p} + \sqrt{2I_dK_n} = \sqrt{2I_nK_n} + \sqrt{2I_pK_p} \tag{12}$$

where the right side of the equation equals g_{mT} of the input differential pairs. The minimum voltage drop required to operate this circuit is the sum of the gate-to-source voltages of M_5 and M_6 plus the minimum saturation voltage for the current source which provides $I_n + I_d$ into the sources of M_4 and M_5.

Constant-g_m circuit 3 is shown in Fig. 3(c). Note that the operation is similar to the constant-g_m bias circuit 2. Equation (9) is true for this circuit as well. Again if we assume that all transistors are operating normally, we can show that this circuit achieves the relation given in (10). Unlike the circuit shown in Fig. 3(b) the source terminals of the p-type transistors are not connected to each other. Then V_{T4} is only approximately equal to V_{T5}. Then (12) is only approximately true. However, this alternate circuit topology requires only one gate-to-source voltage drop, either V_{SG5} or V_{GS6}, whichever is larger, plus the minimum saturation voltage for the current source.

In the remainder of this paper, constant-g_m bias circuit 2 will be used as the bias circuit for the input differential pairs. This is due to its independence of the transistor threshold voltage and because it is free from body effects. The target minimum power supply voltage is 3 V, and the minimum voltage required for the operation of the constant-g_m bias circuit 2 is well below this value.

Current Monitor Circuits

In the above circuits, it was assumed that the input to the bias circuit is a copy of the common mode current in the p-channel differential pair and the output of the bias circuit is the bias current for the n-channel pair. The roles of I_n and I_p can, of course, be interchanged but we will keep I_p as the current that needs to be monitored. Next, we discuss two schemes for monitoring I_p and feeding it into the constant-g_m bias circuit.

Monitor Circuit 1 is shown in Fig. 4(a). The set of transistors M_3, M_{3a}, and M_q are an exact replica of the input transistors M_1, M_{1a}, and M_p so that these two sets behave in exactly the same manner as a function of V_{CM}. The differential input signals applied to M_3 and M_{3a} cancels at their drains and they will not affect the operation of the constant-g_m bias circuit.

When V_{CM} is small enough, transistors M_p and M_q are operating in the saturation region and thus the current mirror is working properly; then $I_p = I_{\text{ref}}$. As V_{CM} is increased toward the upper rail, M_p and M_q start to go into the triode region; since their gates are at a fixed voltage, I_p becomes less than I_{ref} and becomes a function of V_{CM}.

Monitor Circuit 2 is shown in Fig. 4(b). In monitor circuit 1, M_p, which provides a bias current to the p-channel differential pair, is biased with a fixed voltage. An alternate method for monitoring I_p is to actively bias M_p. The gate terminal of transistor M_b is biased with a constant voltage V_b.

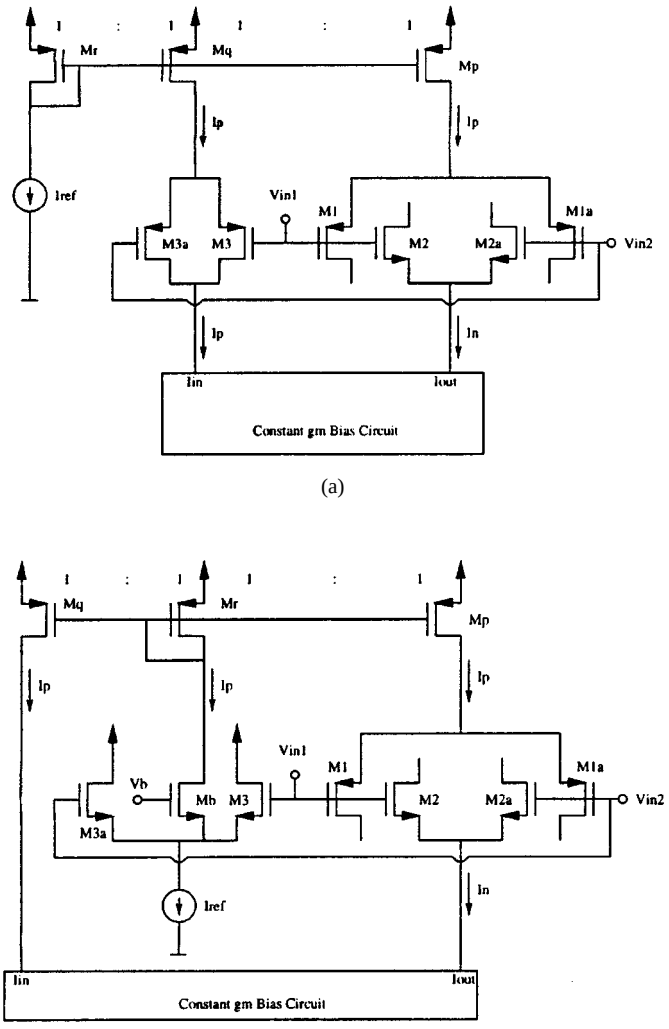


Fig. 4. CMOS implementation of (a) monitor circuit 1 and (b) monitor circuit 2.

As V_{in1} and V_{in2} and, hence, V_{CM} are increased, a larger portion of I_{ref} is consumed by M_3 and M_{3a}. Then the drain current in M_b decreases and I_p decreases with increasing V_{CM}. The value of V_{ref} depends on V_b, I_{ref}, and the sizes of M_3, M_{3a}, and M_b.

Weak Inversion Operation

To reach (12), we made an assumption that all the transistors are operating in the saturation region. When V_{CM} becomes close to V_{DD}, I_p that flows into M_3 becomes very small and the assumption is only half true, i.e., M_3 is still operating in saturation region, but it is no longer in the strong inversion. If I_p becomes zero, according to (10) V_{GS3} is represented by V_{T3} which is a constant; However, when the transistor is in weak inversion, V_{GS} decreases below V_T. Since the sum of V_{SG4} and V_{GS3} is guaranteed to be constant, when V_{GS3} becomes less than its intended value (V_{T3}), V_{SG4} becomes larger than its maximum intended value. This of course makes I_n and hence g_{mn} larger than what they should be when I_p is very small and g_{mT} is no longer constant.

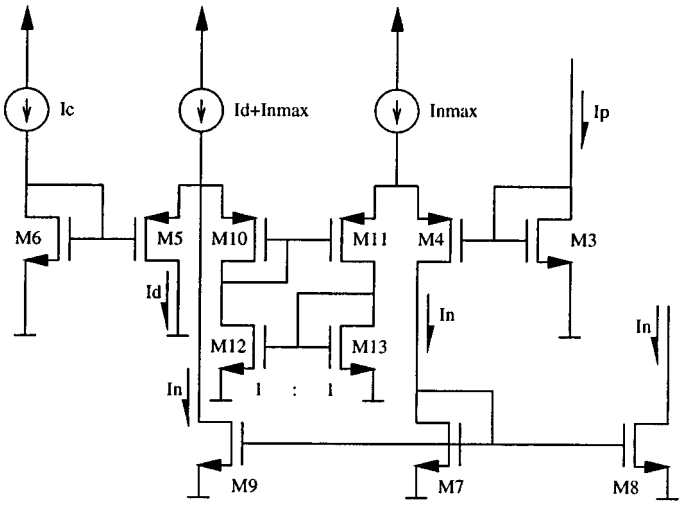


Fig. 5. Modified version of the bias circuit 2. This implementation overcomes the problem caused by M_3 going into the weak inversion region.

One way to overcome the problem caused by the weak inversion region operation of M_3 is to hard limit the value of I_n just as I_p is limited to I_{ref}. The circuit shown in Fig. 5 is a modified version of the bias circuit 2 which is shown in Fig. 3(b). The source terminals of M_4 and M_5 are separated, and the voltages at these nodes are maintained equal by the circuit consisting of M_{10}, M_{11}, M_{12}, and M_{13}. Note that these devices can be recognized as part of a current conveyor [12]. Because of the current mirror $M_{12} - M_{13}$, the drain currents in M_{10} and M_{11} are equal. Then their gate-to-source voltages should be the same; since their gate terminals are connected, the source terminals of M_{10} and M_{11}, or similarly, the source terminals of M_4 and M_5, are at the same potential as desired. A constant current source I_{nmax} supplies currents to the sources of M_4 and M_{11}, and no matter how small V_{GS3} becomes, I_n is limited to $I_{n\max}$.

Before we place the modified bias circuit of Fig. 5 into the input stage, there is one more aspect that needs to be taken care of. Because I_{ref} is the maximum value for I_p, let us rename I_{ref} as $I_{p\max}$; then when only the p-channel differential pair is operating, we have

$$g_{mT} = g_{mp} = \sqrt{2I_{p\max}K_p}. \tag{13}$$

This will be the case for V_{CM} small enough such that $I_p = I_{p\max}$. When V_{CM} is increased so that I_p becomes less than $I_{p\max}$ and the n-channel pair is also contributing to g_{mT}, we have

$$\begin{aligned} g_{mT} &= g_{mn} + g_{mp} \\ &= \sqrt{2K_nI_d} + \sqrt{2K_pI_c}. \end{aligned} \tag{14}$$

When V_{CM} is large enough such that I_p becomes zero and only the n-channel pair is operating, we have

$$g_{mT} = g_{mn} = \sqrt{2I_{n\max}K_n}. \tag{15}$$

In order to have a constant-g_m input stage, (13), (14), and (15) must be made the same. To make (13) and (15) equal, we must have

$$I_{p\max}K_p = I_{n\max}K_n. \tag{16}$$

Notice that if we chose $I_c = I_{p\max}/4$ and $I_d = I_{n\max}/4$, (14) will be the same as (13) and (15). The circuit that realizes the condition of (16) is shown in Fig. 6. The circuit is supplied with a constant bias current $(1 + a)I_{n\max}$. The main part of the circuit consists of transistors M_{B1}, M_{B2}, M_{B3}, and M_{B4} which are used in the exact same configuration as the constant-g_m bias circuit 2, and we have

$$V_{SGB3} + V_{GSB2} = V_{SGB4} + V_{GSB1}. \tag{17}$$

Since all the currents are constant, there is no need to be concerned with transistors going into the weak inversion region. Then assuming the square-law characteristics, (17) becomes

$$\sqrt{\frac{I_{p\max}}{K_n}} + \sqrt{\frac{aI_{n\max}}{K_p}} = \sqrt{\frac{I_{n\max}}{K_p}} + \sqrt{\frac{aI_{p\max}}{K_n}} \tag{18}$$

which, after some algebra, becomes the same as (16). At this point, we have all the necessary subcircuits to construct constant-g_m input stages.

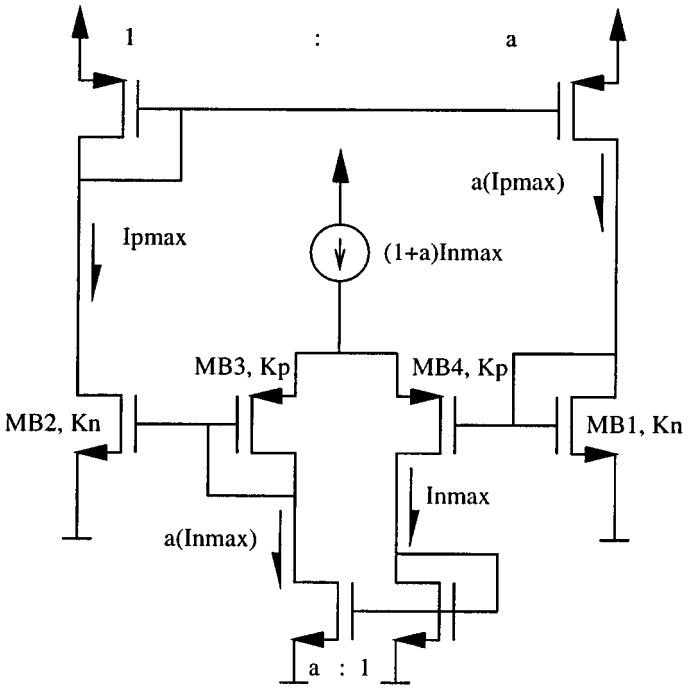


Fig. 6. A CMOS circuit that satisfies the condition $I_{p\max}K_p = I_{n\max}K_n$.

Constant-g_m Input Stage 1 is shown in Fig. 7. This circuit uses the first monitor circuit (monitor circuit 1). Since M_6 (not shown) and M_{B1} are both biased with $I_{p\max}/4$, their gate voltages are the same. Since the purpose of M_6 is to bias the gate terminal of M_5, it can be eliminated simply by connecting the gate of M_5 to the gate of M_{B1}. Simulation results of this input stage are shown in Fig. 8(a). The variation in g_{mT} as V_{CM} is swept from 0 to 3 V is less than 10%; although this is not perfectly constant, it is much better than the 100% deviation which results from input stages without any novel

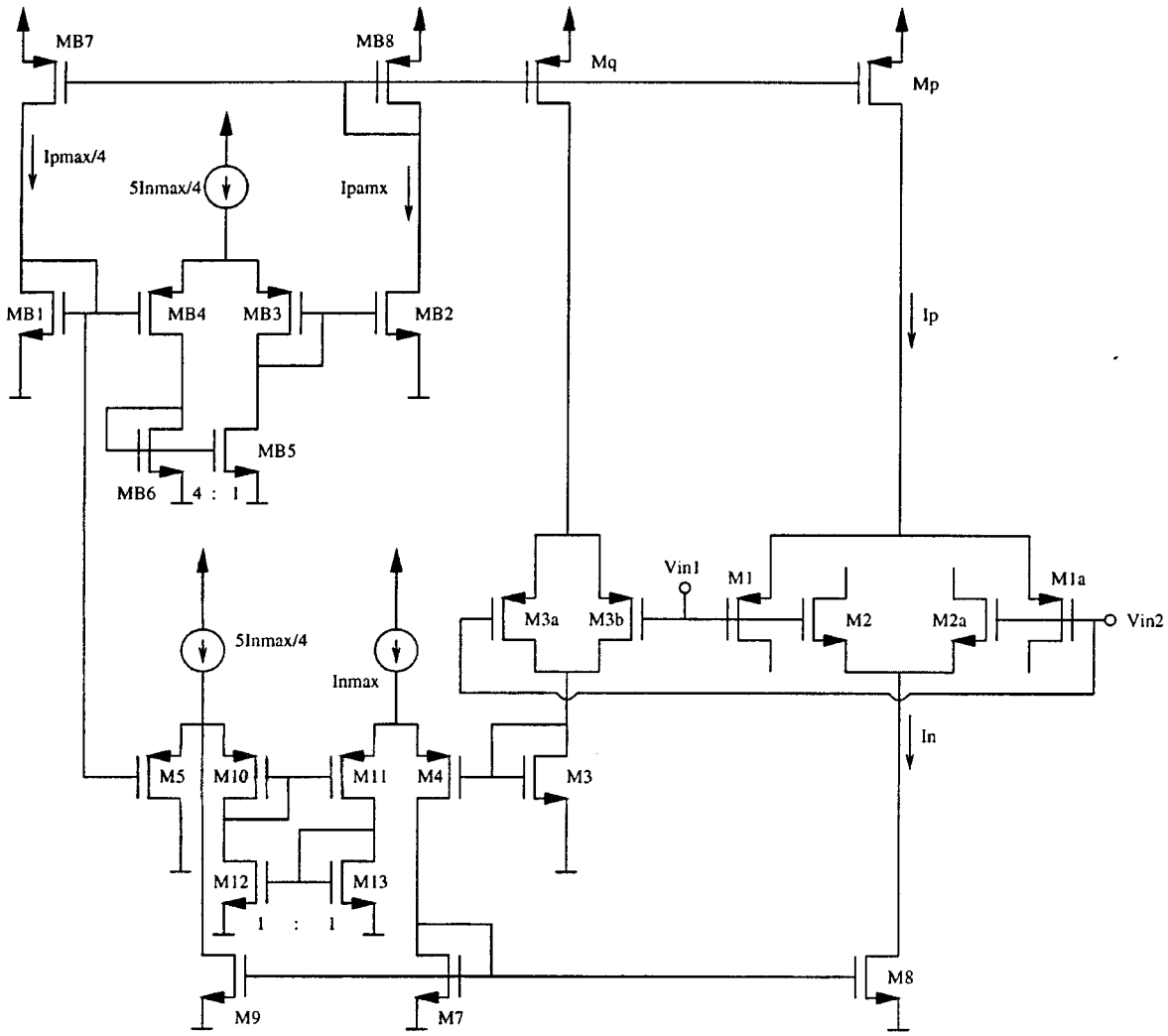


Fig. 7. Constant-g_m input stage 1.

biasing schemes. Furthermore, the circuit shown in Fig. 7 does not require matching between n- and p-channel transistors.

Constant-g_m Input Stage 2 is exactly the same as the constant-g_m input stage 1 except that monitor circuit 2 is used instead of monitor circuit 1. The bias voltage, V_b, which is the gate voltage of M_b is set to 1.7 V. The simulation results are shown in Fig. 8(b); the curves are similar to those obtained for the constant-g_m circuit 1 except that they are slightly shifted to the left. This is due to the reference voltage V_b which determines the point at which g_{mn} and g_{mp} are the same.

Note that the CMRR of opamps utilizing rail-to-rail input stage of the type shown in Fig. 1 degrades when V_{cm} is such that one of the differential pairs is just turning on or off. Indeed, we noticed this behavior in the simulation of the new input stages.

IV. Silicon Implementations

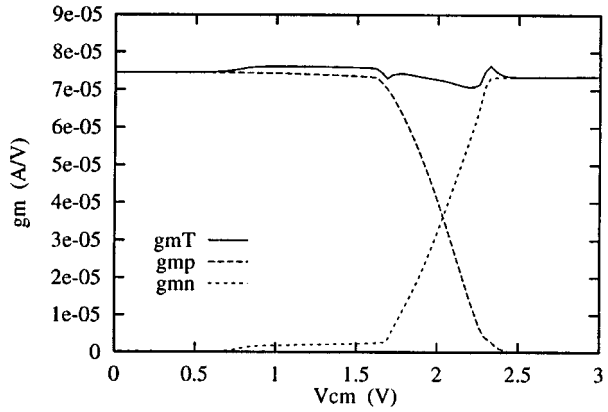
Eight opamps were implemented onto two MOSIS Tiny chips. Each chip was fabricated in a 2 μm p-well process on the same run. The photomicrographs of the two Tiny chips containing 3-V operational amplifiers are shown in Fig. 9. The size and the estimated power consumption of each opamp is listed in Table I. Opamps 1 and 2, which do not possess a constant-g_m, were biased by $I_{n\max}$ and $I_{p\max}$ generated by the bias circuit of Fig. 6. Next, experimental results of opamps 1, 2, 2a, and 2b are discussed.

K_n and K_p

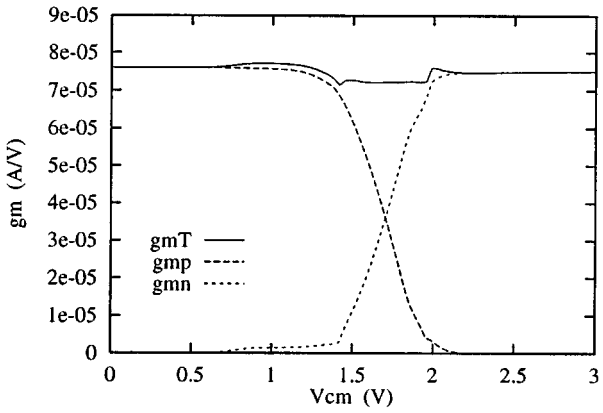
The results given in this section were obtained with input stages biased with $I_{n\max} = 18\mu$A and powered with $V_{DD} = 3\,V$ and $V_{SS} = 0\,V$. Transistor sizes of the differential pairs are $W/L = 75\,\mu$m$/8\,\mu$m and $30\,\mu$m$/8\,\mu$m for the p- and n-channel transistors, respectively. The ratio of 2.5 for the size of p- to n-channel transistors was chosen because it is the typical ratio of the n-type to the p-type transconductance parameters provided by Orbit. Note that the ratio was the same on the model parameter set provided by Orbit for this particular wafer. Thus, the measured K_p to K_n ratio is supposed to be close to one. We found, however, that $K_n = 52\,\mu$A$/V^2$ and

TABLE I
AREA AND ESTIMATED POWER CONSUMPTION, AT 3.3 V, OF EACH OPAMP

Name	Input Stage	Architecture	Area $\mu m \times \mu m$	Power (mW)
Opamp 1	rail-to-rail	single stage, single-ended	750 × 250	0.5
Opamp 1a	input stage 1	single stage, single-ended	870 × 250	0.8
Opamp 1b	input stage 2	single stage, single-ended	760 × 340	0.8
Opamp 2	rail-to-rail	two stage, single-ended	650 × 510	0.8
Opamp 2a	input stage 1	two stage, single-ended	705 × 560	1.1
Opamp 2b	input stage 2	two stage, single-ended	670 × 590	1.1
Opamp 3a	input stage 1	two stage, fully differential	705 × 630	1.2
Opamp 3b	input stage 2	two stage, fully differential	745 × 590	1.3



(a)



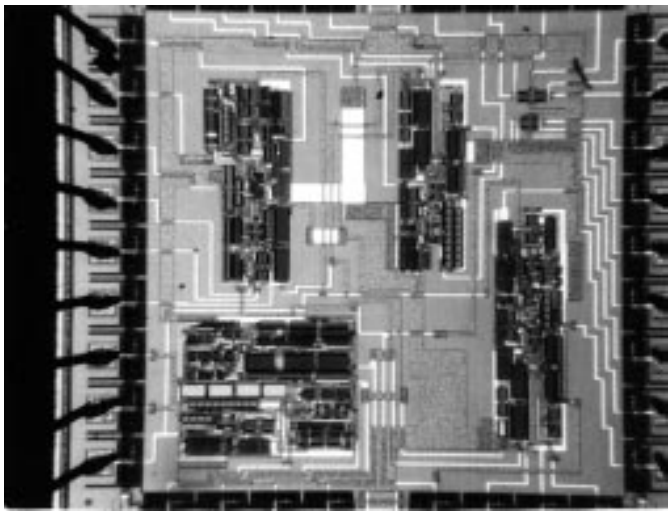
(b)

Fig. 8. Simulation results of the constant-g_m input stages (a) 1 and (b) 2.

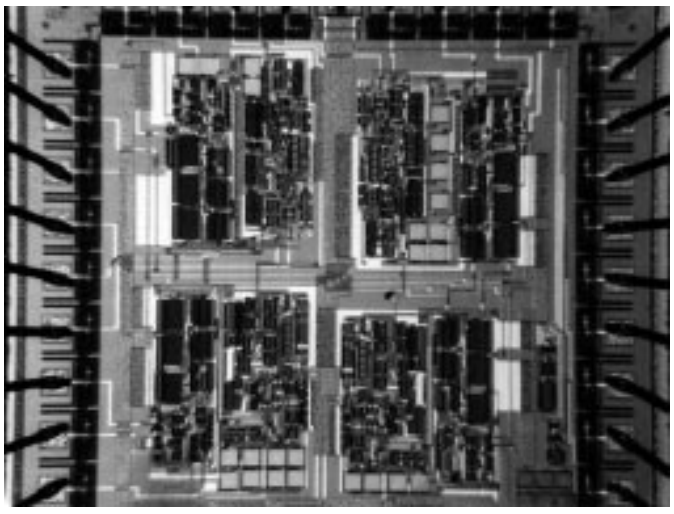
$K_p = 87\,\mu\text{A}/V^2$, and the K_p/K_n ratio is 1.67 instead of the expected value of one.

The uncertainty of the K_p/K_n ratio is precisely the reason that we are developing the constant-g_m input stages which do not require the matching of K_p and K_n.

The input stage used in opamp 1 does not have the constant-g_m characteristics. However, the bias currents of the differential pairs are provided by the circuit in Fig. 6 and, hence, satisfy the condition given by (16) such that $g_{mT}(= g_{mp})$ when V_{CM} is near V_{SS} would be equal to $g_{mT}(= g_{mn})$ when V_{CM} is near V_{DD}. Fig. 10(a) shows the differential pair currents. Note that $I_{p\max}$ is significantly less than $I_{n\max}$ because K_p is larger than K_n. Fig. 10(b) shows the measured g_m of the input stage which does not possess the constant-g_m characteristics. We see that g_{mT} varies by a factor of two as



(a)



(b)

Fig. 9. Photomicrographs of the fabricated chips. (a) Chip 1: showing, clockwise from the top left-hand corner, opamps 1b, 1, 1a, and 2. (b) Chip 2 showing, clockwise from the top left-hand corner, opamps 2a, 3a, 2b, and 3b.

expected; moreover, because of the bias circuit of Fig. 6, g_{mT} is the same for V_{CM} near the two rails despite the fact that K_p/K_n is not close to one.

Constant-g_m Input Stage

Fig. 11(a) shows the measured g_m of the constant-g_m input stage 1. g_{mT} is constant within about 10% for the entire

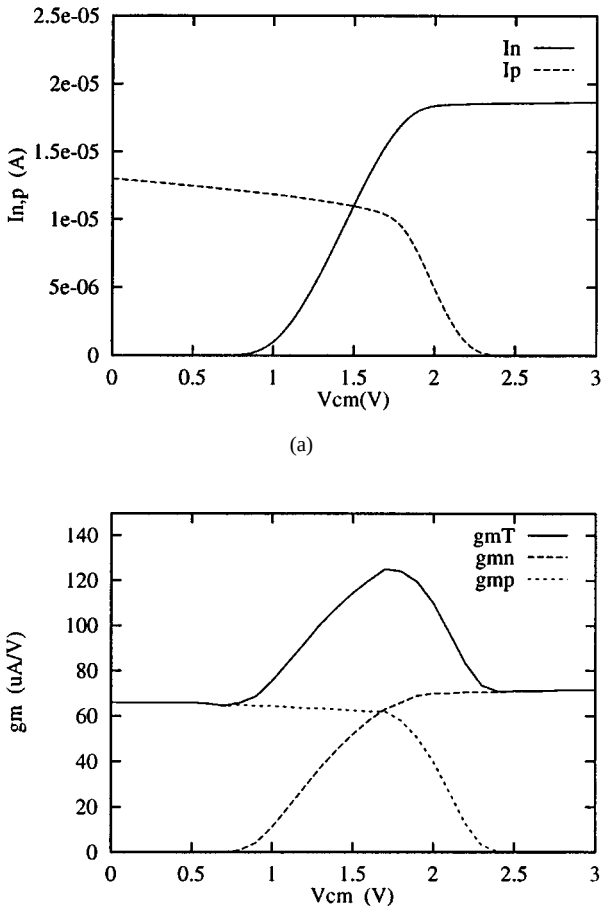


Fig. 10. Measurements taken on the input stage of opamp 1. (a) Differential pair currents. (b) Differential pair transconductance.

common mode range. Were it not for this circuit, which does not require n- to p-channel matching, $g_{mT}(V_{cm} = 0)$ and $g_{mT}(V_{cm} = 3)$ would have been different by 29%, i.e., $(\sqrt{1.67} - 1)$.

We have measured the constant-g_m input stage 2 for three different values of V_b. They are shown in Fig. 11(b), and we can clearly see the dependence of the input stage characteristics on the value of V_b. Even though the results provided here are obtained using $V_{DD} - V_{SS} = 3$ V, we observed that both constant-g_m input stages operate properly also with $V_{DD} - V_{SS} = 2.5$ V. This observation should come as no surprise since, as discussed earlier, the minimum supply voltage required is two gate-to-source voltage drops (in strong inversion) plus V_{DSsat}. This makes the new input stages more attractive, especially since the use of a 2.7 V power supply is to follow that of a 3 V supply in the near future.

Two-Stage Operational Amplifiers

Opamp 2a, which is a two-stage opamp with constant-g_m input stage 1, is shown in Fig. 12. The bottom part of this figure shows a rail-to-rail common source amplifier output stage with class AB control circuit. In the presence of a large signal at the output node, we would like V_{1+} and V_{1-} to move toward V_{SS} in order to prevent M_{O1} or M_{O2} from turning off.

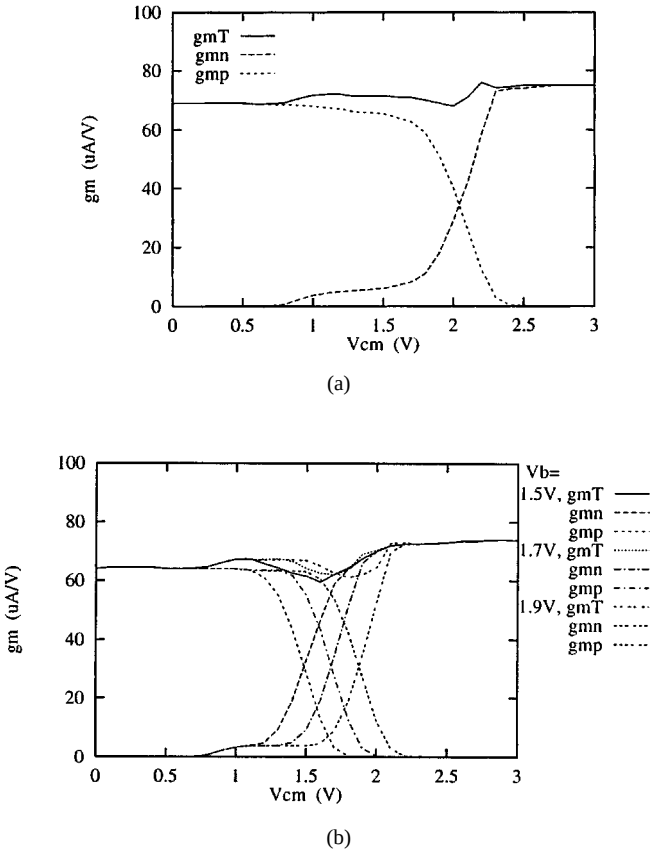


Fig. 11. Measured g_m of (a) input stage 1 and (b) input stage 2.

Then V_b and V_c should also move toward V_{SS}, and this will happen if $V_d - V_a$ is decreased. Starting from V_d and summing the gate to source voltages of M_{O13}, M_{O14}, M_{O11}, and M_{O12} and going to V_a, we can write

$$V_d - V_a = V_{SGO13} + V_{SGO11} - V_{SGO14} - V_{SGO12}. \quad (19)$$

The currents flowing in the transistors M_{O11}, M_{O12}, M_{O13}, and M_{O14} are given by

$$I_{O11} = I_{\text{on}} \quad (20)$$

$$I_{O12} = I_{\text{min}} \quad (21)$$

$$I_{O13} = I_{\text{op}} \quad (22)$$

$$I_{O14} = I_{\text{on}} + I_{\text{op}} \quad (23)$$

then (19) can be written as

$$\sqrt{K_p}(V_d - V_a) = \sqrt{I_{\text{op}}} + \sqrt{I_{\text{on}}} - \sqrt{I_{\text{min}}} - \sqrt{I_{\text{op}} + I_{\text{on}}}. \quad (24)$$

At the quiescent condition $I_{\text{op}} = I_{\text{on}} = I_Q$ and (24) becomes

$$\sqrt{K_p}(V_d - V_a) = (2 - \sqrt{2})\sqrt{I_Q} - \sqrt{I_{\text{min}}}. \quad (25)$$

If the output voltage swings close to V_{DD}, I_{op} becomes very large and then $I_{op} >> I_Q > I_{on}$ is true and the last term in the right-hand side of (24) is dominated by I_{op} and hence it will approximately cancel the first term. Then (24) becomes

$$\sqrt{K_p}(V_d - V_a) = \sqrt{I_{\text{on}}} - \sqrt{I_{\text{min}}}. \quad (26)$$

Thus, when $\sqrt{I_{\text{on}}}$ becomes smaller than $(2 - \sqrt{2})\sqrt{I_Q}$, (26) becomes smaller than (25), and this implies that when I_{on}

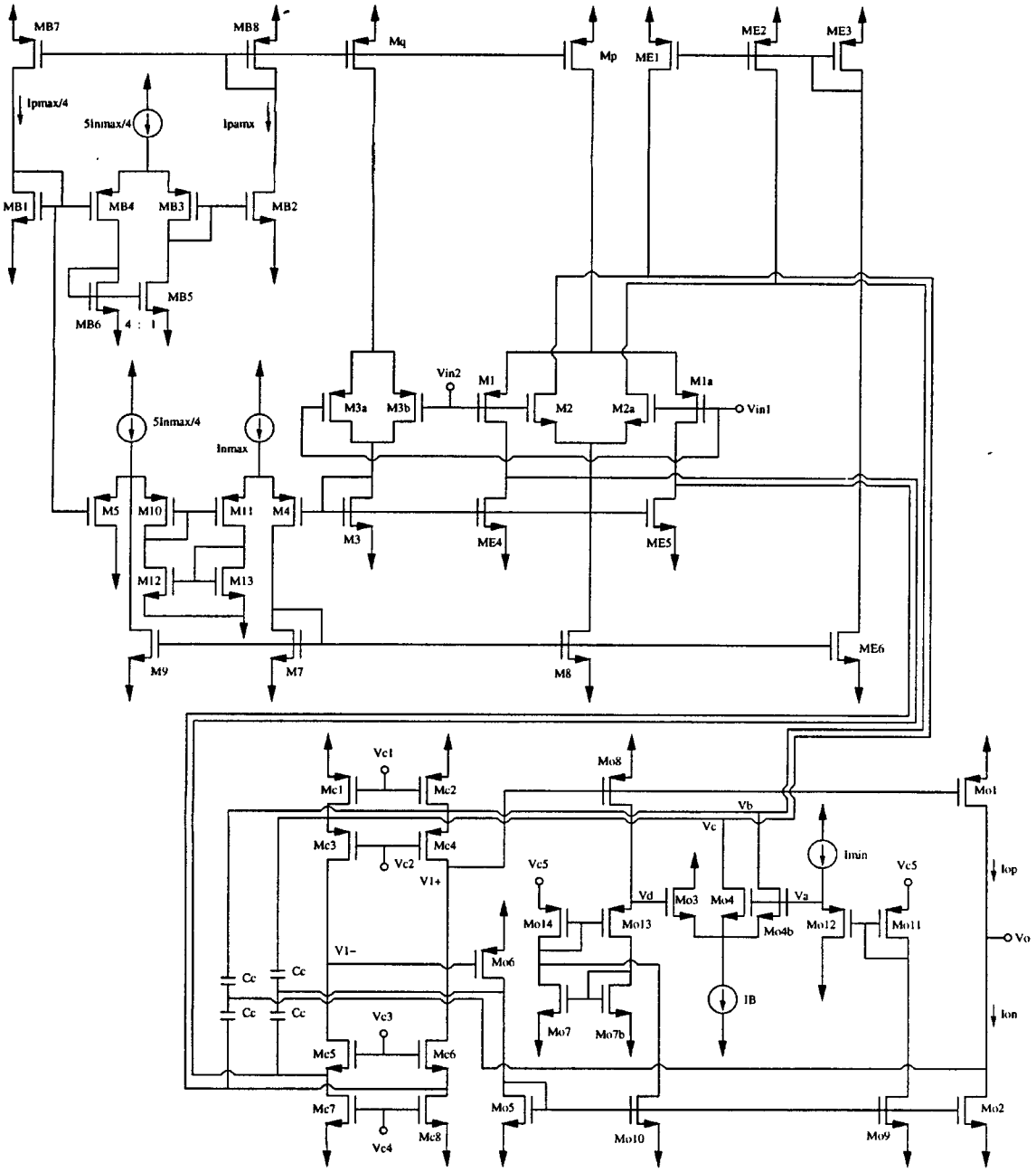


Fig. 12. Opamp 2a: A rail-to-rail two-stage opamp with the constant-g_m input stage 1 and a common source output stage (bottom part) with class AB control.

reaches some minimum level of current, $(V_d - V_a)$ is decreased as desired. The same action will take place when I_{on} becomes large and I_{op} reaches the minimum value. The feedback mechanism tries to maintain the expressions given in (24)–(26) equal to zero. Then from (25) and (26), we can find that $I_Q \approx 3I_{\min}$ and the minimum value of I_{op} and I_{on} is $I_{\min}$.

The input–output transfer characteristics of opamp 2 in a unity gain configuration is shown in Fig. 13, and we can see that the rail-to-rail output swing is achieved. The results from opamp 2a and opamp 2b ($V_b = 1.7$ V) are identical to that of opamp 2. Fig. 14 shows the currents flowing in the output transistors of the common source amplifier of opamp 2. Class AB characteristics of the output stage are clearly seen. Estimated quiescent power dissipation of the opamps are 0.8 mW and 1.1 mW for opamp 2 and opamps 2a and 2b, respectively. Fully-differential versions of the two-stage opamps are obtained by simply adding four transistors and four capacitors to each of the output stages [11]. The circuits were powered with $V_{DD} - V_{SS} = 3.3$ V. The results demonstrate rail-to-rail differential operation at both input and output.

Two-stage opamps 2, 2a, and 2b were powered with $V_{DD} - V_{SS} = 3.3$ V for the frequency and time domain measurements. We obtained the expected gain (80 to 90 dB) from the two-stage opamps. Fig. 15 shows f_U of the three opamps as a function of the common mode input voltage. f_U of opamp 2a and opamp 2b stays almost constant at 1.5 MHz and 1.4

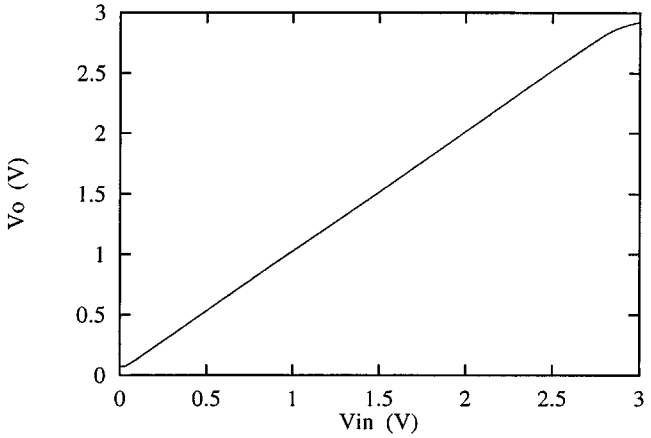


Fig. 13. Experimental $V_{in} - V_o$ characteristics of two-stage single-ended-output opamps in a unity gain configuration ($V_{DD} - V_{SS} = 3$ V, $R_L = 10k\Omega$).

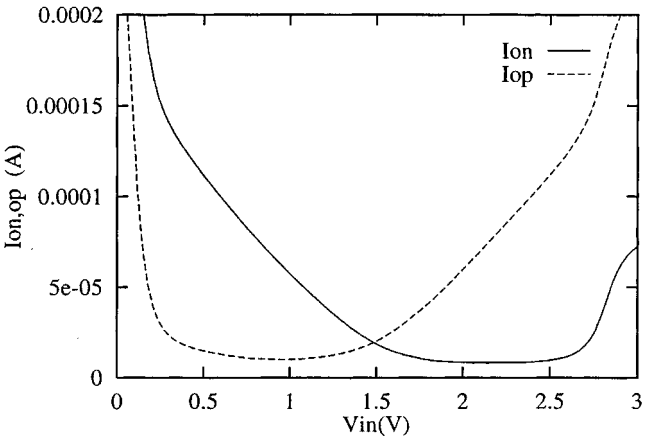


Fig. 14. Current flow in the output transistors of the output stage of opamp 2.

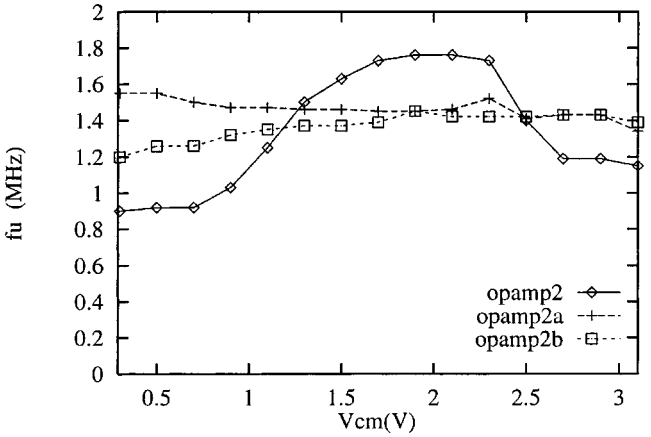


Fig. 15. The unity gain frequency of the two-stage opamps as a function of V_{CM}.

MHz, respectively, while f_U of opamp 2 changes between 0.9 MHz and 1.8 MHz. This demonstrates the effectiveness of the constant-g_m input stages pertaining to f_U of both the single and the two-stage opamps.

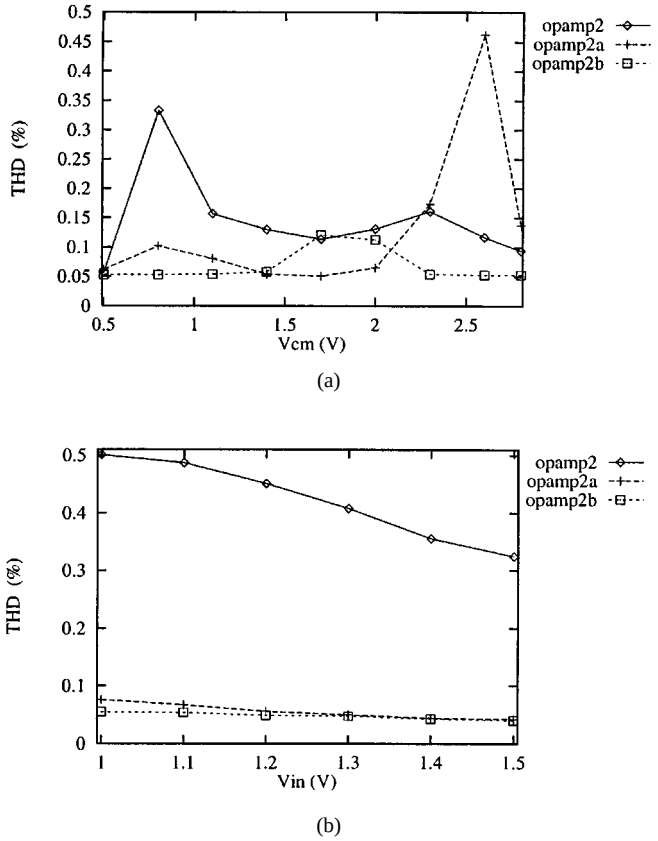


Fig. 16. Measured total harmonic distortion of the two-stage opamps: (a) as a function of V_{CM}, $v_{\rm in} = 0.2 \sin 20\,000\pi t$, (b) as a function of $v_{\rm in}$, $V_{CM} = 1.65$ V.

Fig. 16(a) shows the total harmonic distortion (THD) of the opamps as a function of V_{cm}. Since even the g_{mT} of the opamp with constant-g_m input stage is slightly "bumpy," especially when observed for a small V_{cm} range, THD is not expected to significantly improve for small input signals. Nonetheless, we do observe a slight improvement. Fig. 16(b) shows the THD of the opamps as a function of the amplitude of the input voltage where the dc component was fixed at mid-rail. In this case, the input signal amplitude is large enough such that the small variation in g_{mT} of opamp 2a and 2b are effectively averaged out. We can clearly see the improvements in the distortion performance resulting from using a constant-g_m input stage.

We noticed, through measurements, that the input stages with constant-g_m bias circuit may not operate properly depending on the power supply conditions, possibly due to a transient problem at the power up [11]. However, note that once a good set of supply voltages was found, it was used for the entire measurements of a particular opamp.

V. Conclusion

New circuit techniques which can be used as bias circuits for constant-g_m input stage without the necessity for matching n- and p-channel transistors were introduced. The bias circuits take in the current, I_p, flowing in the p-channel differential pair as an input current and deliver I_n, which is to be used as the bias current for the n-channel differential pair.

Measured results of opamps fabricated in a MOSIS 2 μm p-well process were given. Constant-g_m input stage exhibited approximately 10% deviation as the common mode input was swept between $V_{SS} = 0$ and $V_{DD} = 3$ V. The unity gain frequency of the opamps with constant-g_m input stages was accordingly constant. Measured THD of the opamps with constant-g_m input stage was better than those without it, especially for large input signals. Thus, we have successfully designed and implemented rail-to-rail opamps with a constant-g_m input stage and demonstrated their superior performance.

The techniques discussed here and those previously reported in the literature are based on manipulating dc bias currents to achieve constant-g_m. Recently, new techniques [13] based on handling small-signal or output currents, rather than dc tail currents, to achieve constant-g_m have been described. These techniques still require matching of devices of opposite types and therefore methods to circumvent the need for such matching should be investigated.

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