1.8 - MOSFET MODELS

INTRODUCTION

Objective

The objective of this presentation is:

1.) Understand how the MOS transistor works

2.) Understand and apply the simple large signal model

3.) Understand and apply the small-signal model

Outline

- MOS Structure and Operation
- Large Signal Model
- Small-Signal Model
- Capacitance
- Short Channel Large Signal Model
- Subthreshold Large Signal Model
- Summary

MOS STRUCTURE AND OPERATION

Metal-Oxide-Semiconductor Structure

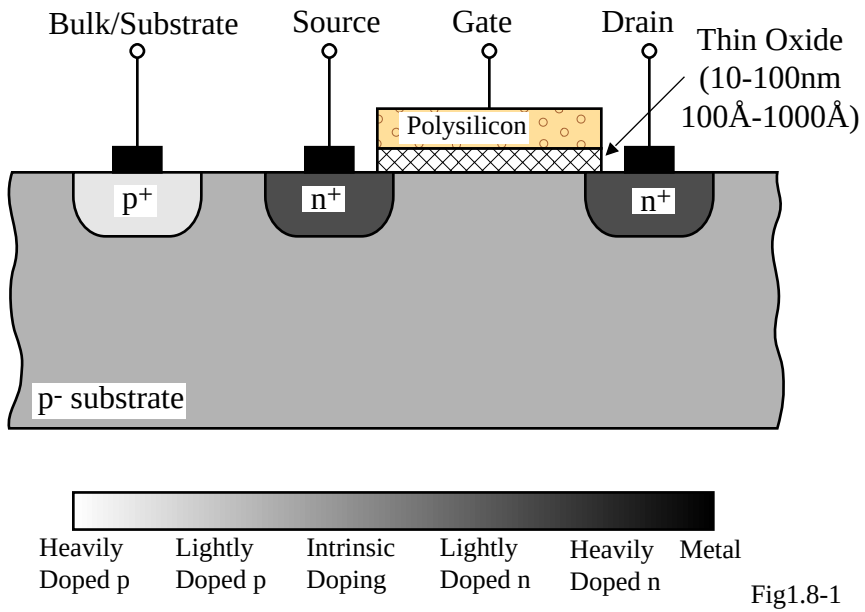


Fig1.8-1

Terminals:

- Bulk - Used to make an ohmic contact to the substrate
- Gate - The gate voltage is applied in such a manner as to invert the doping of the material directly beneath the gate to form a channel between the source and drain.
- Source - Source of the carriers flowing in the channel
- Drain - Collects the carriers flowing in the channel

Formation of the Channel for an Enhancement MOS Transistor

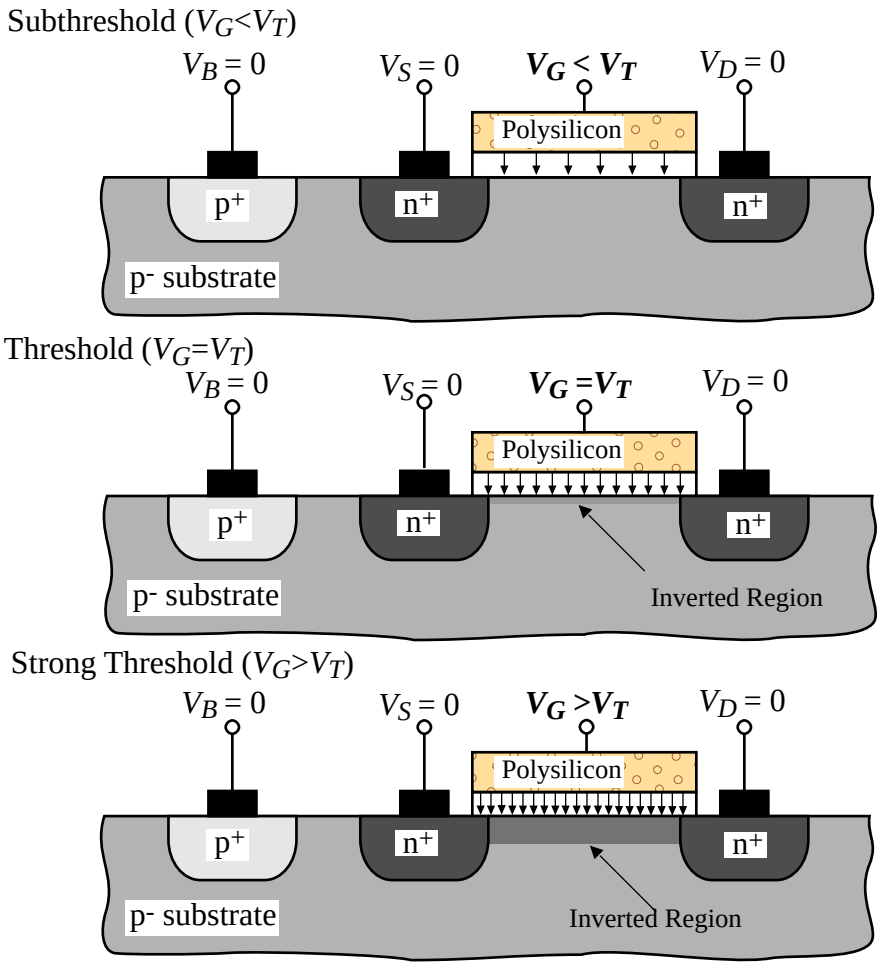


Fig1.8-2

The MOSFET Threshold Voltage

When the gate voltage reaches a value called the *threshold voltage* (V_T), the substrate beneath the gate becomes inverted (it changes from p-type to n-type).

$$V_T = \phi_{MS} + \left(-2\phi_F - \frac{Q_b}{C_{ox}}\right) + \left(\frac{Q_{SS}}{C_{ox}}\right)$$

where

$\phi_{MS} = \phi_F(\text{substrate}) - \phi_F(\text{gate})$

ϕ_F = Equilibrium electrostatic potential (Femi potential)

$$\phi_F(\text{PMOS}) = -\frac{kT}{q} ln(N_A/n_i) = -V_t\, ln(N_A/n_i)$$

$$\phi_F(\text{NMOS}) = \frac{kT}{q} ln(N_D/n_i) = V_t\, ln(N_D/n_i)$$

$$Q_b \approx \sqrt{2q\mathrm{N}_A\varepsilon_{si}(|-2\phi_F+v_{SB}|)}$$

Q_{SS} = undesired positive charge present in the interface between the oxide and the bulk silicon

Rewriting the threshold voltage expression gives,

$$V_T = \phi_{MS} - 2\phi_F - \frac{Q_{b0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_b - Q_{b0}}{C_{ox}} = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + v_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

where

$$V_{T0} = \phi_{MS} - 2\phi_F - \frac{Q_{b0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} \qquad \text{and} \qquad \gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$$

Signs for the Quantities in the Threshold Voltage Expression

Parameter	N-Channel	P-Channel
Substrate	p-type	n-type
ϕ_{MS}		
Metal	−	−
n^+ Si Gate	−	−
p^+ Si Gate	+	+
ϕ_F	−	+
Q_{b0},Q_b	−	+
Q_{ss}	+	+
V_{SB}	+	−
γ	+	−

Example 1 - Calculation of the Threshold Voltage

Find the threshold voltage and body factor γ for an n-channel transistor with an n^+ silicon gate if t_{ox} = 200 Å, $N_A = 3 \times 10^{16}$ cm^{-3}, gate doping, $N_D = 4 \times 10^{19}$ cm^{-3}, and if the positively-charged ions at the oxide-silicon interface per area is 10^{10} cm^{-2}.

Solution

From above, ϕ_F(substrate) is given as

$$\phi_F(\text{substrate}) = -0.0259 \ln\left[\frac{3\times 10^{16}}{1.45 \times 10^{10}}\right] = -0.377 \text{ V}$$

The equilibrium electrostatic potential for the n^+ polysilicon gate is found from as

$$\phi_F(\text{gate}) = 0.0259 \ln\left[\frac{4 \times 10^{19}}{1.45 \times 10^{10}}\right] = 0.563 \text{ V}$$

Therefore, the potential ϕ_{MS} is found to be

$$\phi_F(\text{substrate}) - \phi_F(\text{gate}) = -0.940 \text{ V}.$$

The oxide capacitance is given as

$$C_{ox} = \varepsilon_{ox}/t_{ox} = \frac{3.9 \times 8.854 \times 10^{-14}}{200 \times 10^{-8}} = 1.727 \times 10^{-7} \text{ F/cm}^2$$

The fixed charge in the depletion region, Q_{b0}, is given as

$$Q_{b0} = -[2 \times 1.6 \times 10^{-19} \times 11.7 \times 8.854 \times 10^{-14} \times 2 \times 0.377 \times 3 \times 10^{16}]^{1/2} = -8.66 \times 10^{-8} \text{ C/cm}^2.$$

Example 1 - Continued

Dividing Q_{b0} by C_{ox} gives –0.501 V. Finally, Q_{ss}/C_{ox} is given as

$$\frac{Q_{ss}}{C_{ox}} = \frac{10^{10} \times 1.60 \times 10^{-19}}{1.727 \times 10^{-7}} = 9.3 \times 10^{-3} \text{ V}$$

Substituting these values for V_{T0} gives

$$V_{T0} = -0.940 + 0.754 + 0.501 - 9.3 \times 10^{-3} = 0.306 \text{ V}$$

The body factor is found as

$$\gamma = \frac{\left[2 \times 1.6 \times 10^{-19} \times 11.7 \times 8.854 \times 10^{-14} \times 3 \times 10^{16}\right]^{1/2}}{1.727 \times 10^{-7}} = 0.577 \quad \text{V}^{1/2}$$

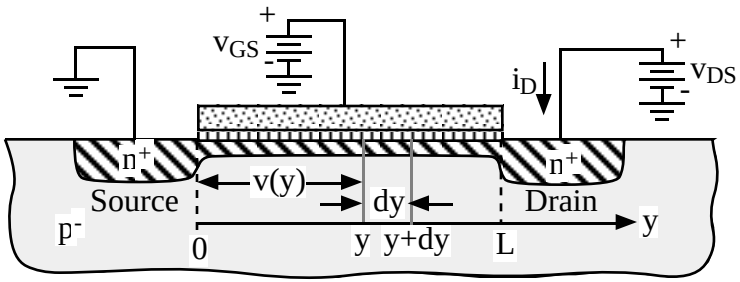
SIMPLE LARGE SIGNAL MOSFET MODEL

Large Signal Model Derivation

Derivation-

1.) Let the charge per unit area in the channel inversion layer be

$$Q_I(y) = -C_{ox}[v_{GS} - v(y) - V_T] \quad \text{(coulombs/cm}^2\text{)}$$



2.) Define sheet conductivity of the inversion layer per square as

$$\sigma_S = \mu_o Q_I(y) \quad \left(\frac{\text{cm}^2}{\text{v}\cdot\text{s}}\right)\left(\frac{\text{coulombs}}{\text{cm}^2}\right) = \frac{\text{amps}}{\text{volt}} = \frac{1}{\Omega/\text{sq.}}$$

3.) Ohm's Law for current in a sheet is

$$J_S = \frac{i_D}{W} = -\sigma_S E_y = -\sigma_S \frac{dv}{dy} \quad \rightarrow \quad dv = \frac{-i_D}{\sigma_S W}\, dy = \frac{-i_D dy}{\mu_o Q_I(y) W} \quad \rightarrow \quad i_D\, dy = -W\mu_o Q_I(y) dv$$

4.) Integrating along the channel for 0 to L gives

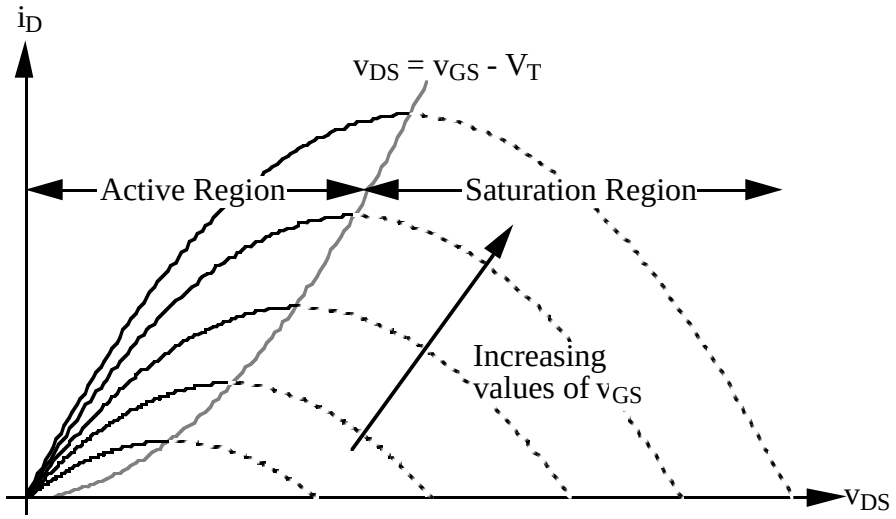
$$\int_0^L i_D dy = -\int_0^{v_{DS}} W\mu_o Q_I(y) dv = \int_0^{v_{DS}} W\mu_o C_{ox}[v_{GS} - v(y) - V_T]\, dv$$

5.) Evaluating the limits gives

$$i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS} - V_T)v(y) - \frac{v^2(y)}{2}\right]_0^{v_{DS}} \rightarrow \boxed{i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}\right]}$$

Saturation Voltage - V_{DS}(sat)

Interpretation of the large signal model:



The saturation voltage for MOSFETs is the value of drain-source voltage at the peak of the inverted parabolas.

$$\frac{di_D}{dv_{DS}} = \frac{\mu_o C_{ox} W}{L}[(v_{GS}-V_T) - v_{DS}] = 0 \qquad \rightarrow \qquad \boxed{v_{DS}(\text{sat}) = v_{GS} - V_T}$$

Useful definitions:

$$\frac{\mu_o C_{ox} W}{L} = \frac{K'W}{L} = \beta$$

Complete Large Signal Model

Regions of Operation of the MOS Transistor:

1.) Cutoff Region:

$$i_D = 0, \qquad v_{GS} - V_T < 0 \qquad \text{(Ignores subthreshold currents)}$$

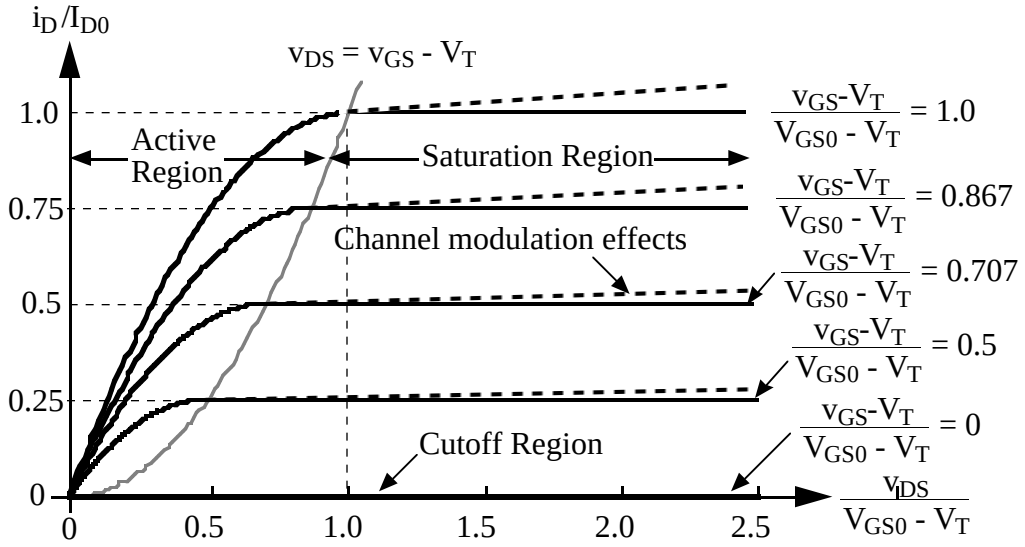
2.) Active Region

$$i_D = \frac{\mu_o C_{ox} W}{2L}\left[2(v_{GS} - V_T) - v_{DS}\right] v_{DS}, \qquad 0 < v_{DS} < v_{GS} - V_T$$

3.) Saturation Region

$$i_D = \frac{\mu_o C_{ox} W}{2L}(v_{GS} - V_T)^2, \qquad 0 < v_{GS} - V_T < v_{DS}$$

Output Characteristics of the MOSFET:



Influence of V_{DS} on the Output Characteristics

Channel modulation effect:

As the value of v_{DS} increases, it causes the effective L to decrease which causes the current to increase.

Illustration:

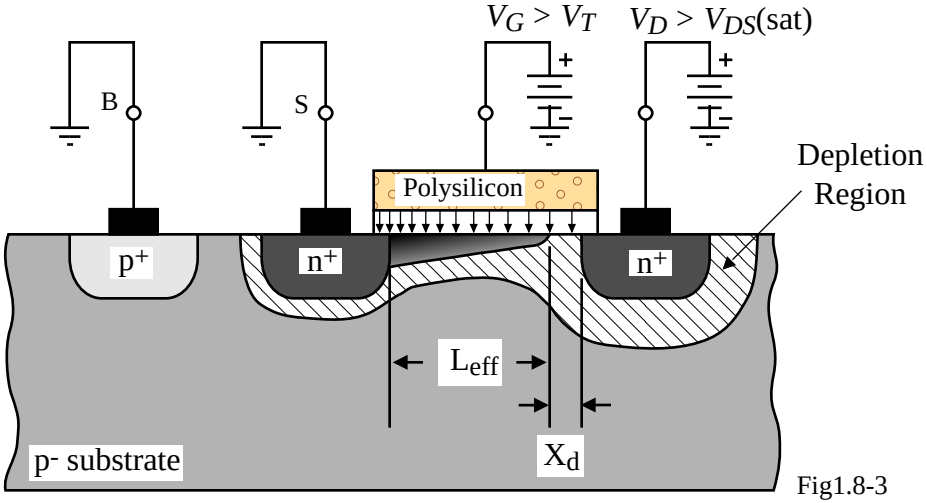


Fig1.8-3

Note that $L_{\text{eff}} = L - X_d$

Therefore the model in saturation becomes,

$$i_D = \frac{K'W}{2L_{\text{eff}}}(v_{GS}-V_T)^2 \quad \rightarrow \quad \frac{di_D}{dv_{DS}} = -\frac{K'W}{2L_{\text{eff}}^2}(v_{GS}-V_T)^2\frac{dL_{\text{eff}}}{dv_{DS}} = \frac{i_D}{L_{\text{eff}}}\frac{dX_d}{dv_{DS}} \equiv \lambda i_D$$

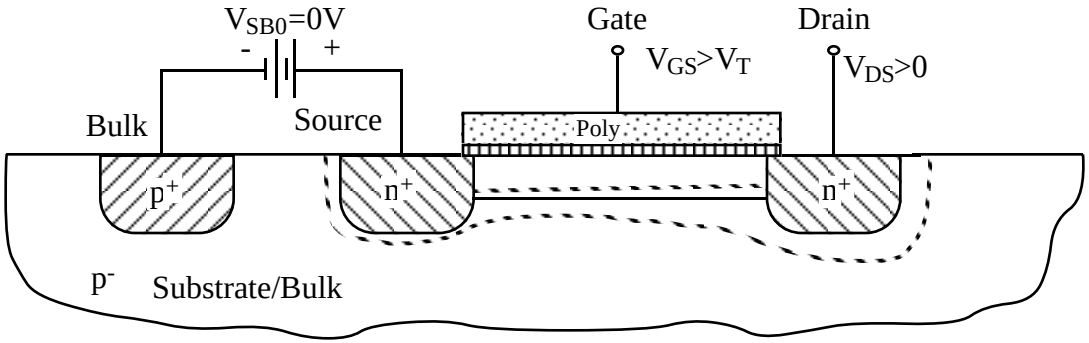
Therefore, a good approximation to the influence of v_{DS} on i_D is

$$i_D \approx i_D(v_{DS}=0) + \frac{di_D}{dv_{DS}}v_{DS} = i_D(v_{DS}=0)(1+\lambda v_{DS}) = \frac{K'W}{2L}(v_{GS}-V_T)^2(1+\lambda v_{DS})$$

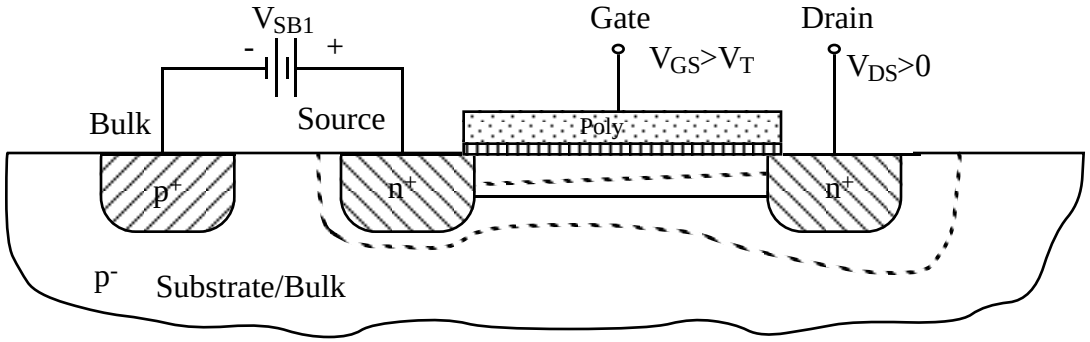
Influence of the Bulk Voltage on the Large Signal MOSFET Model

Illustration of the influence of the bulk:

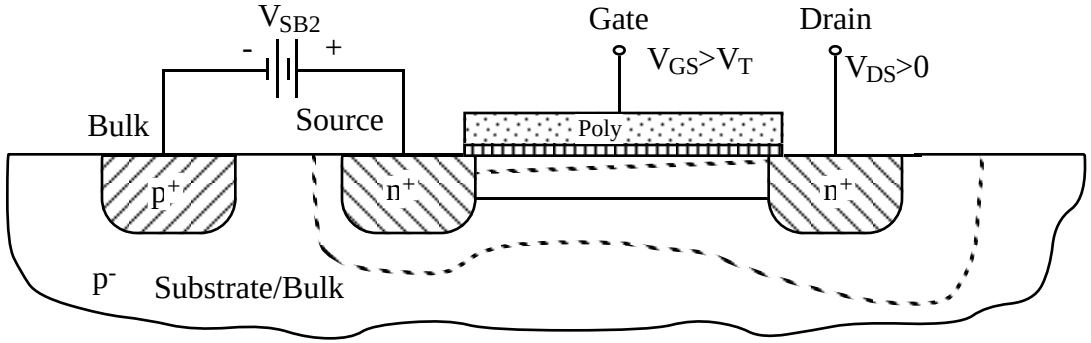
V_{SB0} = 0V:



V_{SB1}>0V:

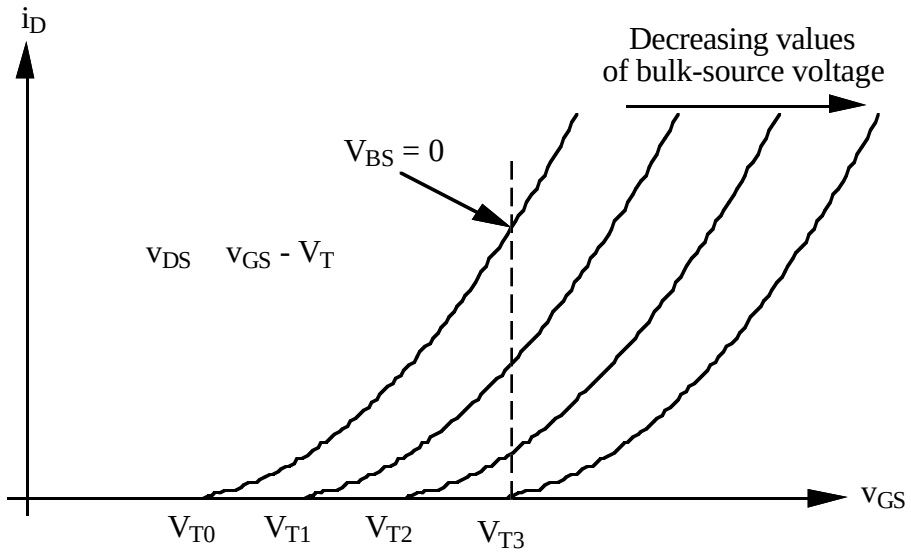


$V_{SB2} > V_{SB1}$:



Influence of the Bulk Voltage on the Large Signal MOSFET Model - Continued

Bulk-Source (v_{BS}) influence on the transconductance characteristics-



In general, the simple model incorporates the bulk effect into V_T by the following empirically developed equation-

$$V_T(v_{BS}) = V_{T0} + \gamma\sqrt{2|\phi_f| + |v_{BS}|} - \gamma\sqrt{2|\phi_f|}$$

MOSFET Schematic Symbols

Enhancement:

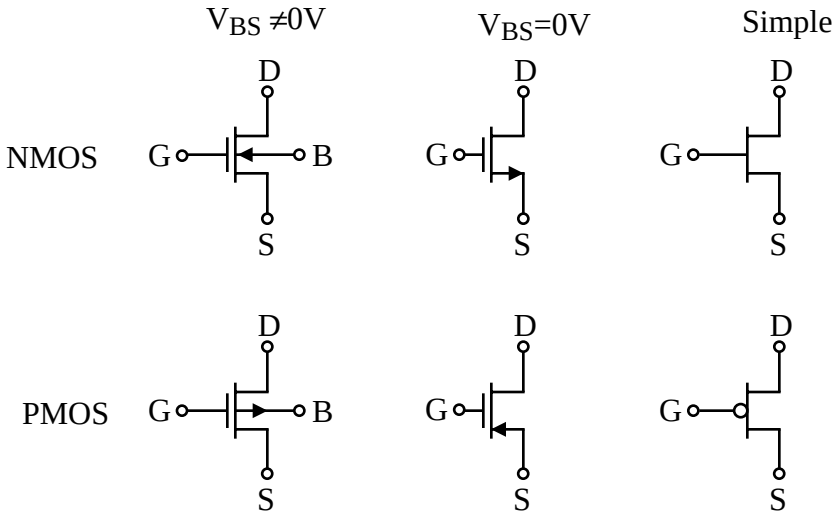
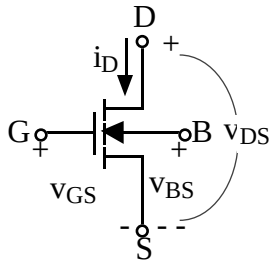


Fig1.8-4

Summary of the Simple Large Signal MOSFET Model

N-channel reference convention:



Non-saturation-

$$i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}\right](1 + \lambda v_{DS})$$

Saturation-

$$i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS} - V_T)v_{DS}(\text{sat}) - \frac{v_{DS}(\text{sat})^2}{2}\right](1 + \lambda v_{DS}) = \frac{W\mu_o C_{ox}}{2L}(v_{GS} - V_T)^2(1 + \lambda v_{DS})$$

where:

μ_o = zero field mobility (cm^2/volt·sec)

C_{ox} = gate oxide capacitance per unit area (F/cm^2)

λ= channel-length modulation parameter ($volts^{-1}$)

$$V_T = V_{T0} + \gamma\left(\sqrt{2|\phi_f| + |v_{BS}|} - \sqrt{2|\phi_f|}\right)$$

V_{T0} = zero bias threshold voltage

γ= bulk threshold parameter ($volts^{-0.5}$)

$2|\phi_f|$ = strong inversion surface potential (volts)

For p-channel MOSFETs, use n-channel equations with p-channel parameters and invert current.

MOSFET

Constants for Silicon:

Constant Symbol	Constant Description	Value	Units
V_G	Silicon bandgap (27°C)	1.205	V
k	Boltzmann's constant	1.381×10^{-23}	J/K
n_i	Intrinsic carrier concentration (27°C)	1.45×10^{10}	cm^{-3}
ε_0	Permittivity of free space	8.854×10^{-14}	f/cm
ε_{si}	Permittivity of silicon	$11.7\ \varepsilon_0$	F/cm
ε_{ox}	Permittivity of SiO_2	$3.9\ \varepsilon_0$	F/cm

Model Parameters for a Typical CMOS Bulk Process (0.8µm CMOS n-well):

Parameter Symbol	Parameter Description	Typical Parameter Value N-Channel	P-Channel	Units
V_{T0}	Threshold Voltage ($V_{BS} = 0$)	0.7 ± 0.15	–0.7 ± 0.15	V
K'	Transconductance Parameter (in saturation)	110.0 ± 10%	50.0 ± 10%	$\mu A/V^2$
γ	Bulk threshold parameter	0.4	0.57	$(V)^{1/2}$
λ	Channel length modulation parameter	0.04 (L=1 μm) 0.01 (L=2 μm)	0.05 (L = 1 μm) 0.01 (L = 2 μm)	$(V)^{-1}$
$2\lvert\phi_F\rvert$	Surface potential at strong inversion	0.7	0.8	V

MOSFET SMALL SIGNAL MODEL

Small-Signal Model

Complete schematic model:

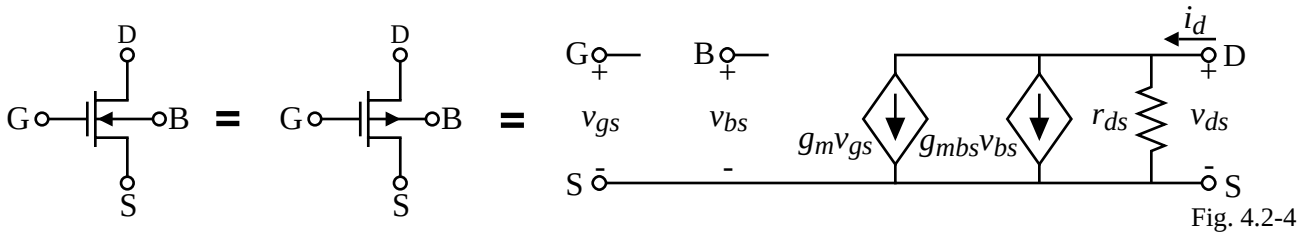


Fig. 4.2-4

where

$$g_m \equiv \left.\frac{di_D}{dv_{GS}}\right|_Q = \beta(V_{GS}-V_T) = \sqrt{2\beta I_D} \qquad g_{ds} \equiv \left.\frac{di_D}{dv_{DS}}\right|_Q = \frac{\lambda i_D}{1 + \lambda v_{DS}} \approx \lambda i_D$$

and $$g_{mbs} = \left.\frac{\partial i_D}{\partial v_{BS}}\right|_Q = \left(\frac{\partial i_D}{\partial v_{GS}}\right)\left(\frac{\partial v_{GS}}{\partial v_{BS}}\right)\Bigg|_Q = \left(-\frac{\partial i_D}{\partial v_T}\right)\left(\frac{\partial v_T}{\partial v_{BS}}\right)\Bigg|_Q = \frac{g_m \gamma}{2\sqrt{2|\phi_F| - V_{BS}}} = \eta g_m$$

Simplified schematic model:

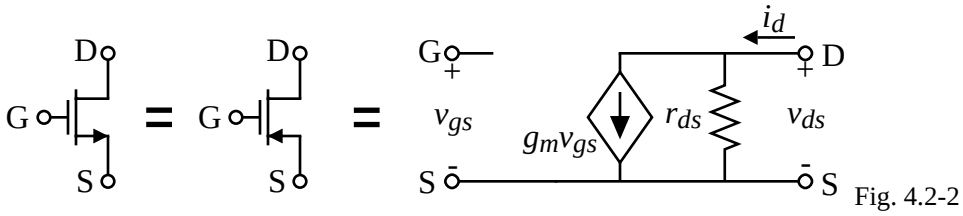


Fig. 4.2-2

Extremely important assumption:

$$\boxed{g_m \approx 10 g_{mbs} \approx 100 g_{ds}}$$

Illustration of the Small-Signal Model Application

DC resistor:

$$\text{DC resistance} = \frac{v}{i}\Big|_Q = \frac{V}{I}$$

- Useful for biasing - creating current from voltage and vice versa

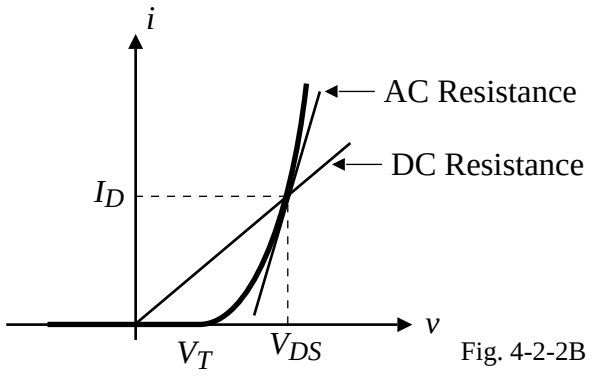


Fig. 4-2-2B

Small-Signal Load (AC resistance):

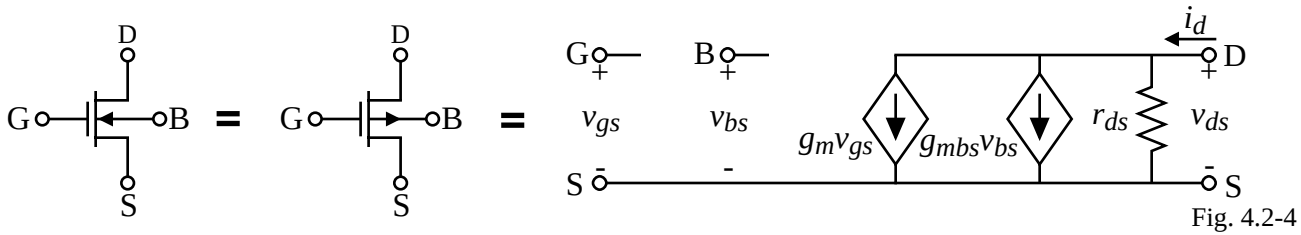


Fig. 4.2-4

$$\text{AC resistance} = \frac{v_{ds}}{i_d} = \frac{1}{g_m + g_{ds}} \approx \frac{1}{g_m}$$

Example 2 - Small-Signal Load Resistance

Find the small signal resistance of the MOS diode shown using the parameters of Table 3.2-1. Assume that the W/L ratio is 10μm/1μm.

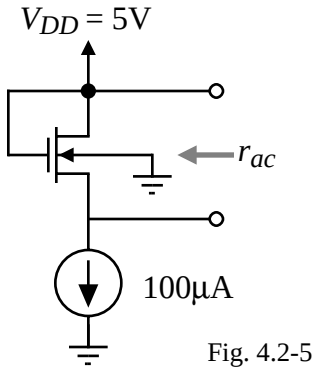


Fig. 4.2-5

Solution

If we are going to include the bulk effect, we must first find the dc value of the bulk-source voltage. Unfortunately, we do not know the threshold voltage because the bulk-source voltage is unknown. The best approach is to ignore the bulk-source voltage, find the gate-source voltage and then iterate if necessary.

$$\therefore\ V_{GS} = \sqrt{\frac{2I}{\beta}} + V_{T0} = \sqrt{\frac{2\cdot 100}{110\cdot 10}} + 0.7 = 1.126\text{V}$$

Thus let us guess at a gate-source voltage of 1.3V (to account for the bulk effect) and calculate the resulting gate-source voltage.

$$V_T = V_{T0} + \gamma\sqrt{2|\phi_F| - (-3.7)} - \gamma\sqrt{2|\phi_F|} = 0.7 + 0.4\sqrt{0.7+3.7} - 0.4\sqrt{0.7} = 1.20\text{V} \Rightarrow V_{GS} = 1.63\text{V}$$

Now refine our guess at V_{GS} as 1.6V and repeat the above to get V_T = 1.175V which gives V_{GS} = 1.60V.

Therefore, V_{BS} = -3.4V.

Example 2 - Continued

The small signal model for this example is shown.

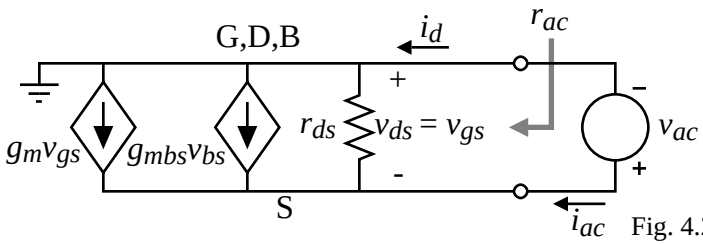


Fig. 4.2-6

The ac input resistance is found by,

$$i_{ac} = g_{ds}v_{ac} - g_m v_{gs} - g_{mbs}v_{bs}$$

$$= g_{ds}v_{ac} + g_m v_s + g_{mbs}v_s = v_{ac}(g_m + g_{mbs} + g_{ds})$$

$$\therefore \; r_{ac} = \frac{v_{ac}}{i_{ac}} = \frac{1}{g_m + g_{mbs} + g_{ds}}$$

Now we must find the parameters which are,

$$g_m = \sqrt{2\beta I_D} = \sqrt{2 \cdot 110 \cdot 10 \cdot 100}\ \mu S = 469\mu S, \; g_{ds} = 0.04V^{-1} \cdot 100\mu A = 4\mu S,$$

$$\text{and } g_{mbs} = \frac{469\mu S \cdot 0.4}{2\sqrt{0.7+3.4}} = 0.0987 \cdot 469\mu S = 46.33\mu S$$

Finally,

$$r_{ac} = \frac{10^6}{469 + 46.33 + 4} = 1926\Omega$$

If we had used the previous approximations of $g_m \approx 10g_{mbs} \approx 100g_{ds}$, then we could have simply let

$$r_{ac} \approx \frac{1}{g_m} = \frac{1}{469} = 2132\Omega$$

Probably the most important result of this approximation is that we would not have to find V_{BS} which took a lot of effort for little return.

Small-Signal Model for the Active Region

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q = \frac{K'WV_{DS}}{L}(1+\lambda V_{DS}) \approx \left(\frac{K'W}{L}\right)V_{DS}$$

$$g_{mbs} = \left.\frac{\partial i_D}{\partial v_{BS}}\right|_Q = \frac{K'W\gamma V_{DS}}{2L\sqrt{2\phi_F - V_{BS}}}$$

$$g_{ds} = \left.\frac{\partial i_D}{\partial v_{DS}}\right|_Q = \frac{K'W}{L}(V_{GS} - V_T - V_{DS})(1+\lambda V_{DS}) + \frac{I_D\lambda}{1+\lambda V_{DS}} \approx \frac{K'W}{L}(V_{GS} - V_T - V_{DS})$$

MOSFET CAPACITANCES

Types of Capacitance

Physical Picture:

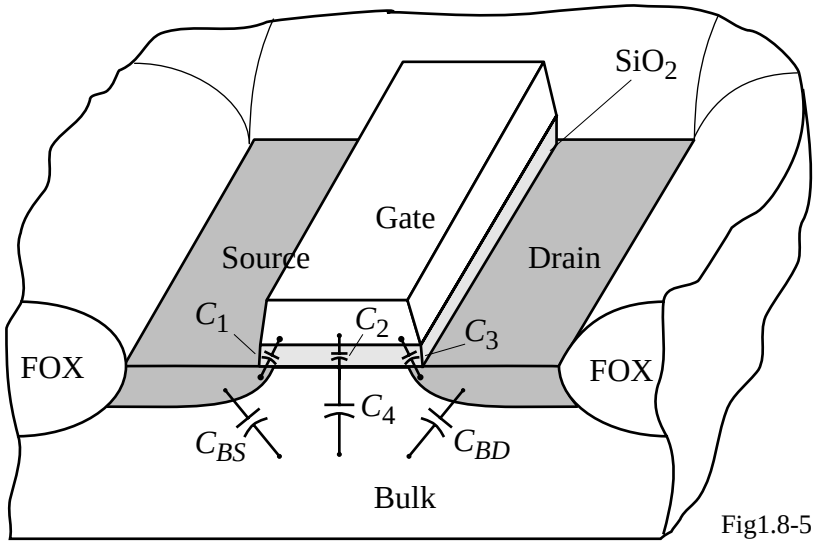


Fig1.8-5

MOSFET Capacitances consist of:

- Depletion capacitance
- Charge storage or parallel plate capacitance

MOSFET Depletion Capacitors

Model:

$$C_{BS} = \frac{CJ \cdot AS}{\left(1 - \frac{v_{BS}}{PB}\right)^{MJ}} + \frac{CJSW \cdot PS}{\left(1 - \frac{v_{BS}}{PB}\right)^{MJSW}}, \quad v_{BS} \le FC \cdot PB$$

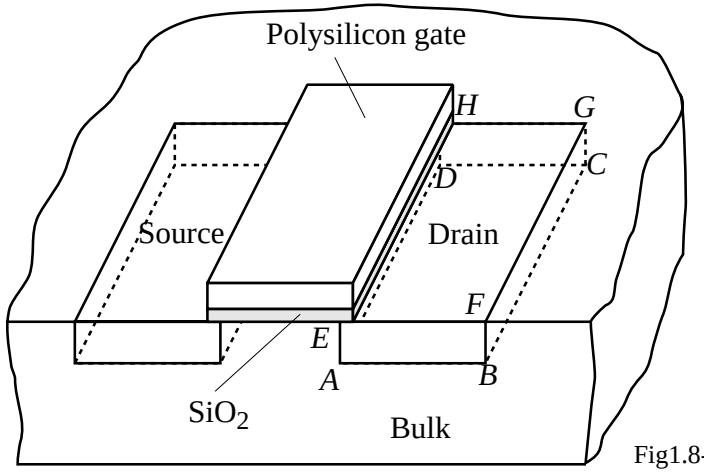


Fig1.8-6

Drain bottom = *ABCD*
Drain sidewall = *ABFE* + *BCGF* + *DCGH* + *ADHE*

and

$$C_{BS} = \frac{CJ \cdot AS}{(1 - FC)^{1+MJ}}\left(1 - (1+MJ)FC + MJ\,\frac{V_{BS}}{PB}\right)$$

$$+ \frac{CJSW \cdot PS}{(1 - FC)^{1+MJSW}}\left(1 - (1+MJSW)FC + MJSW\,\frac{V_{BS}}{PB}\right),$$

$v_{BS} > FC \cdot PB$

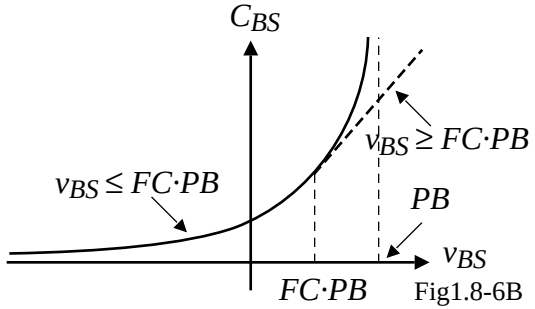


Fig1.8-6B

where

AS = area of the source
PS = perimeter of the source
CJSW = zero bias, bulk source sidewall capacitance
MJSW = bulk-source sidewall grading coefficient

For the bulk-drain depletion capacitance replace "*S*" by "*D*" in the above.

Charge Storage (Parallel Plate) MOSFET Capacitances - C_1, C_2, C_3 and C_4

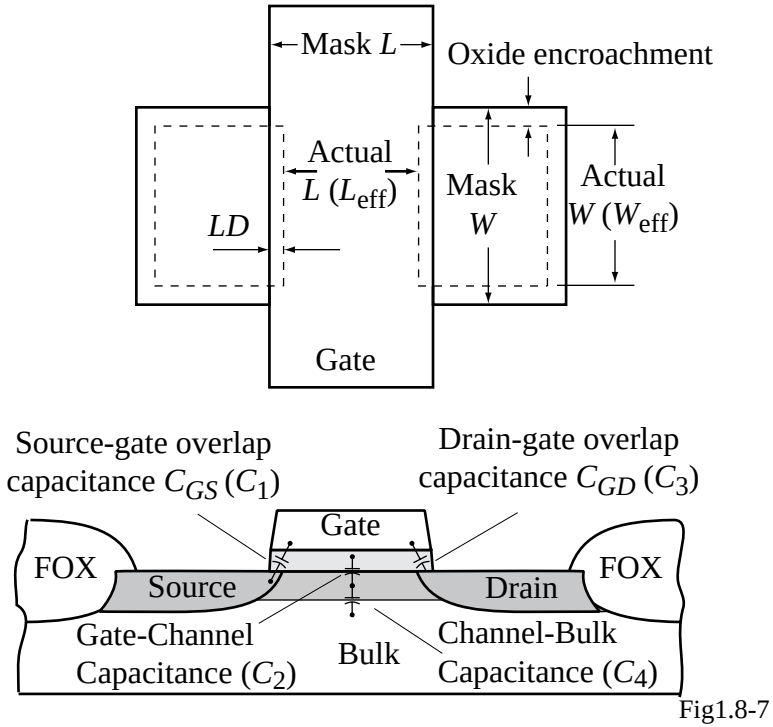


Fig1.8-7

Overlap capacitances:

$C_1 = C_3 = \text{LD}\cdot W_{\text{eff}}\cdot C_{ox}$ = CGSO or CGDO (LD ≈ 0.015 μm for LDD structures)

Channel capacitances:

C_2 = gate-to-channel = $C_{ox}W_{\text{eff}}\cdot(L\text{-}2\text{LD}) = C_{ox}W_{\text{eff}}\cdot L_{\text{eff}}$

C_4 = voltage dependent channel-bulk/substrate capacitance

Charge Storage (Parallel Plate) MOSFET Capacitances - C_5

View looking down the channel from source to drain

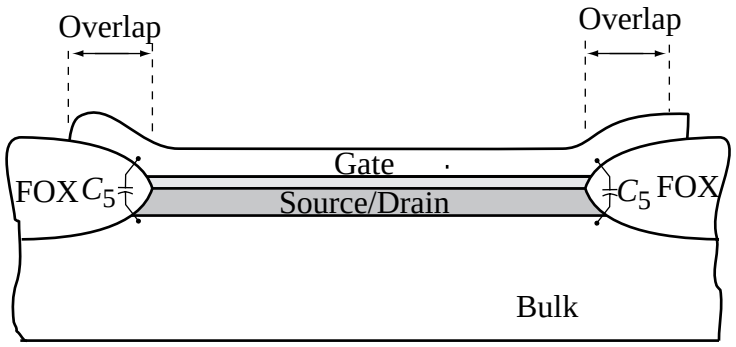


Fig1.8-8

C_5 = CGBO

Capacitance values and coefficients based on an oxide thickness of 140 Å or Cox=24.7 × 10^{-4} F/m^2:

Type	P-Channel	N-Channel	Units
CGSO	220×10^{-12}	220×10^{-12}	F/m
CGDO	220×10^{-12}	220×10^{-12}	F/m
CGBO	700×10^{-12}	700×10^{-12}	F/m
CJ	560×10^{-6}	770×10^{-6}	F/m^2
CJSW	350×10^{-12}	380×10^{-12}	F/m
MJ	0.5	0.5	
MJSW	0.35	0.38	

Expressions for C_{GD}, C_{GS} and C_{GB}

Cutoff Region:

$$C_{GB} = C_2 + 2C_5 = C_{ox}(W_{eff})(L_{eff}) + 2CGBO(L_{eff})$$

$$C_{GS} = C_1 \approx C_{ox}(LD)W_{eff}) = CGSO(W_{eff})$$

$$C_{GD} = C_3 \approx C_{ox}(LD)W_{eff}) = CGDO(W_{eff})$$

Saturation Region:

$$C_{GB} = 2C_5 = CGBO(L_{eff})$$

$$C_{GS} = C_1 + (2/3)C_2 = C_{ox}(LD+0.67L_{eff})(W_{eff})$$

$$= CGSO(W_{eff}) + 0.67C_{ox}(W_{eff})(L_{eff})$$

$$C_{GD} = C_3 \approx C_{ox}(LD)W_{eff}) = CGDO(W_{eff})$$

Active Region:

$$C_{GB} = 2C_5 = 2CGBO(L_{eff})$$

$$C_{GS} = C_1 + 0.5C_2 = C_{ox}(LD+0.5L_{eff})(W_{eff})$$

$$= (CGSO + 0.5C_{ox}L_{eff})W_{eff}$$

$$C_{GD} = C_3 + 0.5C_2 = C_{ox}(LD+0.5L_{eff})(W_{eff})$$

$$= (CGDO + 0.5C_{ox}L_{eff})W_{eff}$$

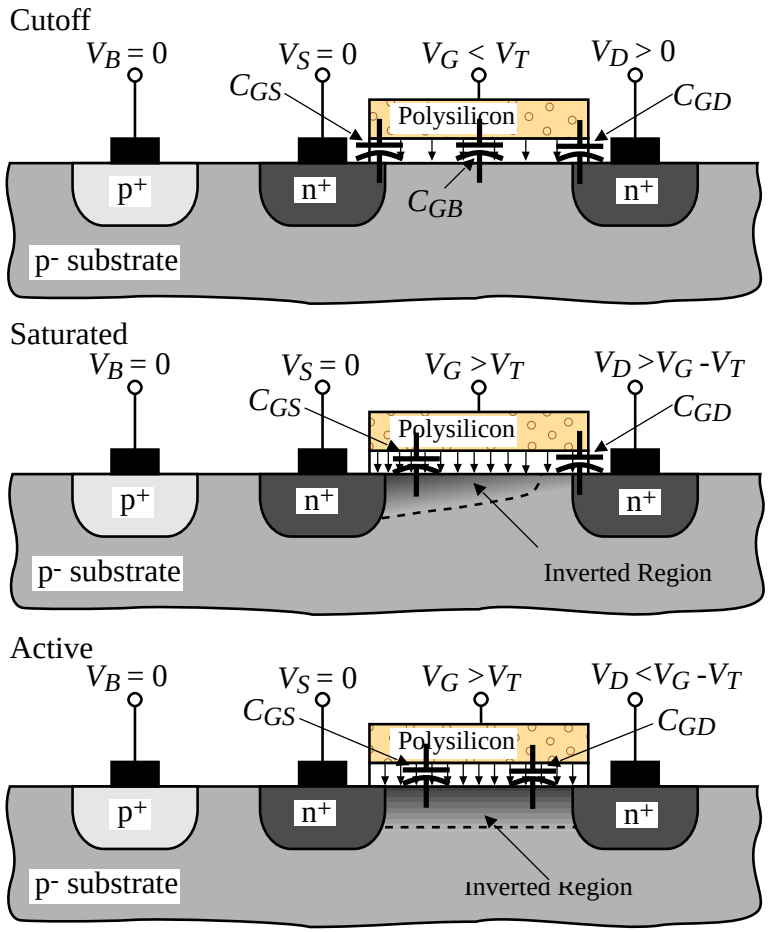


Fig1.8-9

Illustration of C_{GD}, C_{GS} and C_{GB}

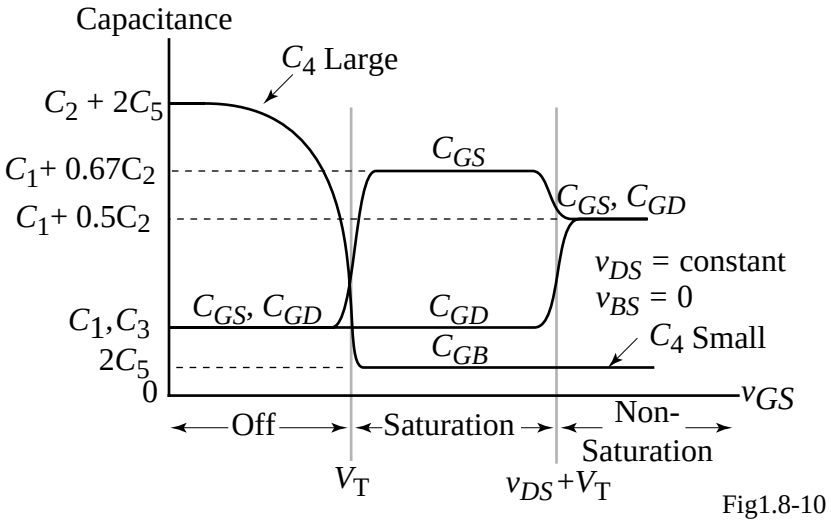


Fig1.8-10

Comments on the variation of C_{BG} in the cutoff region:

$$C_{BG} = \frac{1}{\frac{1}{C_2} + \frac{1}{C_4}} + 2C_5$$

For $v_{GS} \approx 0$, $C_{GB} \approx C_2 + 2C_5$

(C_4 is large because of the thin inversion layer in weak inversion where V_{GS} is slightly less than V_T))

For $0 < v_{GS} < V_T$, $C_{GB} \approx 2C_5$

(C_4 is small because of the thicker inversion layer in strong inversion)

Small-Signal Frequency Dependent Model

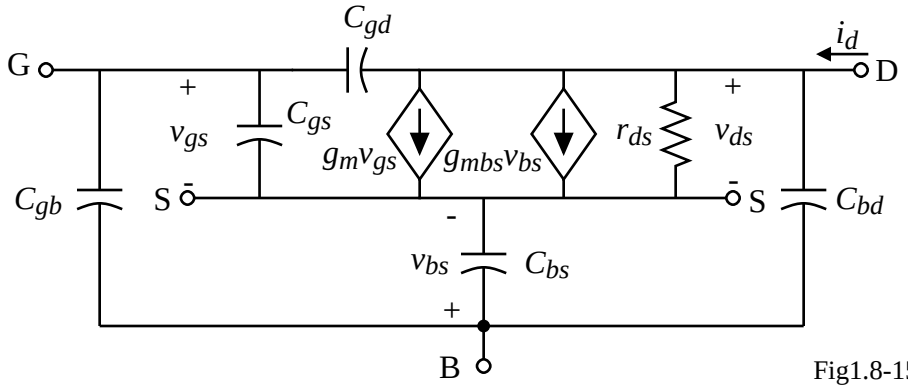


Fig1.8-15

The depletion capacitors are found by evaluating the large signal capacitors at the DC operating point.

The charge storage capacitors are constant for a specific region of operation.

Gainbandwidth of the MOSFET:

Assume $V_{SB} = 0$ and the MOSFET is in saturation,

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_{gs} + C_{gd}} \approx \frac{1}{2\pi}\frac{g_m}{C_{gs}}$$

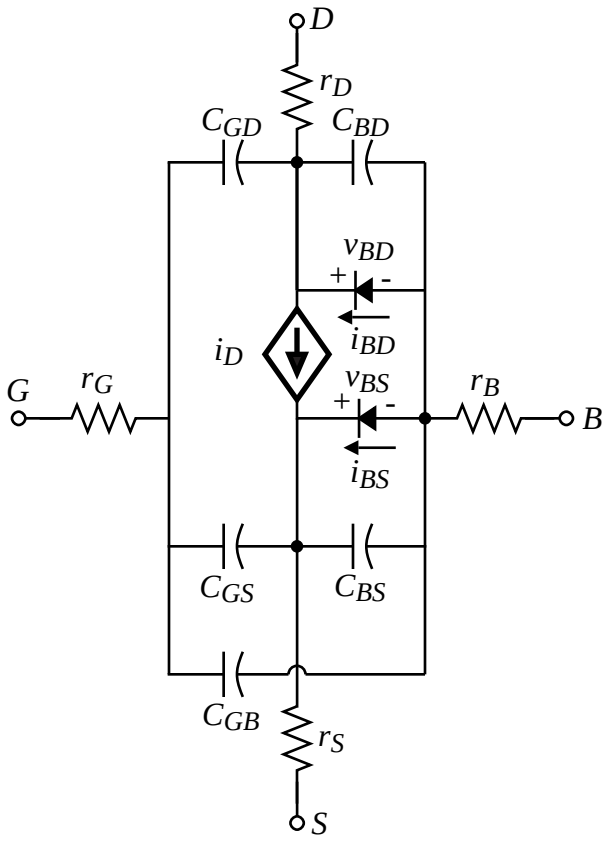
Recalling that

$$C_{gs} \approx \frac{2}{3} C_{ox} WL \qquad \text{and} \qquad g_m = \mu_o C_{ox}\frac{W}{L}(V_{GS}\text{-}V_T)$$

gives

$$f_T = \frac{3}{4\pi}\frac{\mu_o}{L^2}(V_{GS}\text{-}V_T)$$

Summary of the MOSFET Large Signal Model



where,

r_G, r_S, r_B, and r_D are ohmic and contact resistances

$$i_{BD} = I_s\left[exp\left(\frac{v_{BD}}{V_t}\right) - 1\right] \text{ and } i_{BS} = I_s\left[exp\left(\frac{v_{BS}}{V_t}\right) - 1\right]$$

SHORT-CHANNEL MOSFET MODEL

Velocity Saturation

The most important short-channel effect in MOSFETs is the velocity saturation of carriers in the channel. A plot of electron drift velocity versus electric field is shown below.

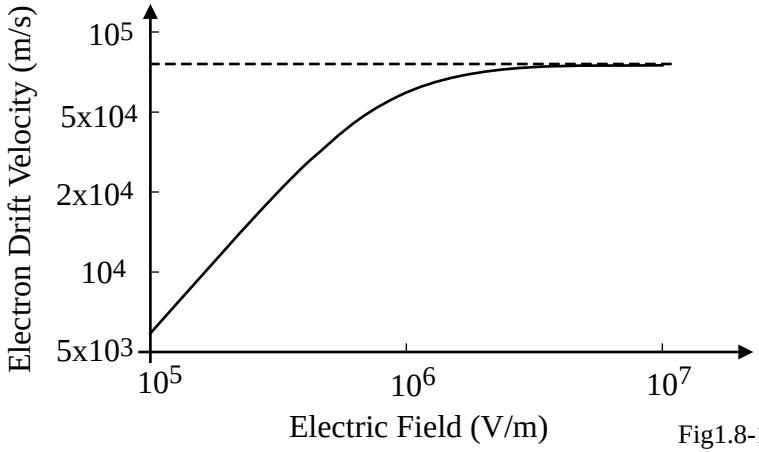


Fig1.8-11

An expression for the electron drift velocity as a function of the electric field is,

$$v_d \approx \frac{\mu_n E}{1 + E/E_c}$$

where

v_d = electron drift velocity (m/s)

μ_n = low-field mobility ($\approx 0.07 m^2/V \cdot s$)

E_c = critical electrical field at which velocity saturation occurs

Short-Channel Model Derivation

As before,

$$J_D = J_S = \frac{i_D}{W} = Q_I(y)v_d(y) \quad \rightarrow \quad i_D = W\,Q_I(y)v_d(y) = \frac{WQ_I(y)\mu_n E}{1 + E/E_c} \quad \rightarrow \quad i_D\left(1 + \frac{E}{E_C}\right) = WQ_I(y)\mu_n E$$

Replacing E by dv/dy gives,

$$i_D\left(1 + \frac{1}{E_C}\frac{dv}{dy}\right) = WQ_I(y)\mu_n\frac{dv}{dy}$$

Integrating along the channel gives,

$$\int_0^L i_D\left(1 + \frac{1}{E_c}\frac{dv}{dy}\right)dy = \int_0^{v_{DS}} WQ_I(y)\mu_n dv$$

The result of this integration is,

$$i_D = \frac{\mu_n C_{ox}}{2\left(1 + \frac{1}{E_c}\frac{v_{DS}}{L}\right)}\frac{W}{L}\left[2(v_{GS} - V_T)v_{DS} - v_{DS}^2\right] = \frac{K'}{2[1 + \theta(v_{GS}-V_T)]}\frac{W}{L}\left[2(v_{GS} - V_T)v_{DS} - v_{DS}^2\right]$$

where $\theta = 1/LE_c$ with dimensions of V^{-1}.

The saturation voltage has not changed so substituting for v_{DS} by v_{GS}-V_T gives,

$$i_D = \frac{K'}{2[1 + \theta(v_{GS}-V_T)]}\frac{W}{L}\left[\,v_{GS} - V_T\right]^2$$

Note that the transistor will enter the saturation region for $v_{DS} < v_{GS} - V_T$ in the presence of velocity saturation.

The Influence of Velocity Saturation on the Transconductance Characteristics

The following plot was made for K' = 110μA/V^2 and W/L = 1:

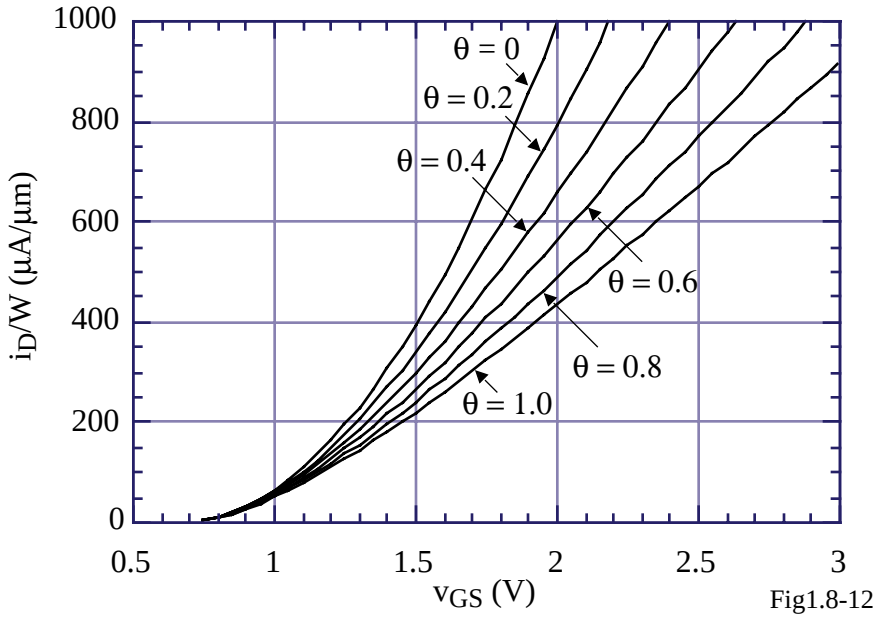


Fig1.8-12

Note as the velocity saturation effect becomes stronger, that the drain current-gate voltage relationship becomes linear.

Circuit Model for Velocity Saturation

A simple circuit model to include the influence of velocity saturation is the following:

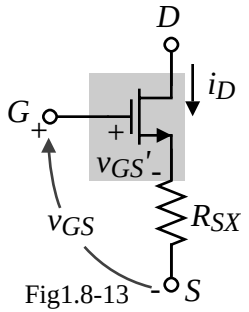


Fig1.8-13

We know that

$$i_D = \frac{K'W}{2L}(v_{GS}' - V_T)^2 \quad \text{and} \quad v_{GS} = v_{GS}' + i_D R_{SX} \quad \text{or} \quad v_{GS}' = v_{GS} - i_D R_{XS}$$

Substituting v_{GS}' into the current relationship gives,

$$i_D = \frac{K'W}{2L}(v_{GS} - i_D R_{SX} - V_T)^2$$

Solving for i_D results in,

$$i_D = \frac{K'}{2\left[1 + K' \frac{W}{L} R_{SX}(v_{GS} - V_T)\right]} \frac{W}{L}(v_{GS} - V_T)^2$$

Comparing with the previous result, we see that

$$\theta = K' \frac{W}{L} R_{SX} \quad \rightarrow \quad R_{SX} = \frac{\theta L}{K'W} = \frac{1}{E_c K'W}$$

Therefore for $K' = 110\mu A/V^2$, $W = 1\mu m$ and $E_c = 1.5 \times 10^6 V/m$, we get $R_{XS} = 6.06k\Omega$.

Output Characteristics of Short-Channel MOSFETs[†]

IBM, 1998, t_{ox} = 3.5nm

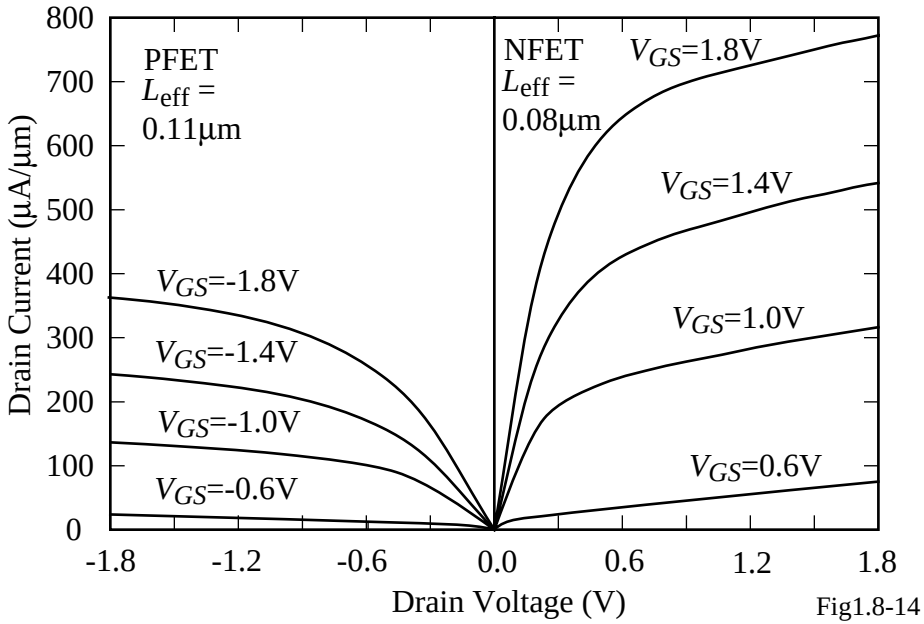
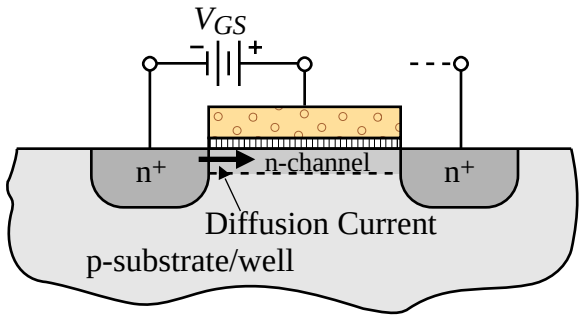


Fig1.8-14

[†] Su, L., et.al., "A High Performance Sub-0.25μm CMOS Technology with Multiple Thresholds and Copper Interconnects," *1998 Symposium on VLSI Technology Digest of Technical Papers*, pp. 18-19.

SUBTHRESHOLD MOSFET MODEL

Weak inversion operation occurs when the applied gate voltage is below V_T and pertains to when the surface of the substrate beneath the gate is weakly inverted.



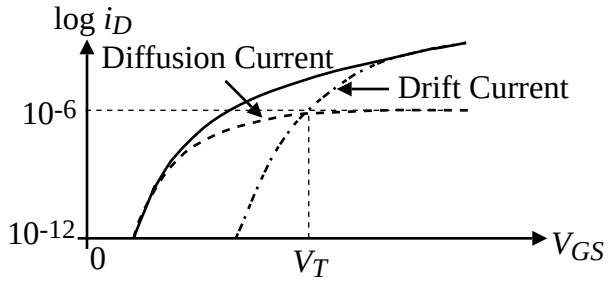
Regions of operation according to the surface potential, ϕ_S.

$\phi_S < \phi_F$: Substrate not inverted

$\phi_F < \phi_S < 2\phi_F$: Channel is weakly inverted (diffusion current)

$2\phi_F < \phi_S$: Strong inversion (drift current)

Drift current versus diffusion current in a MOSFET:



Large-Signal Model for Subthreshold

Model:

$$i_D = K_x \frac{W}{L} e^{v_{GS}/nV_t}(1 - e^{-v_{DS}/V_t})(1 + \lambda v_{DS})$$

where

K_x is dependent on process parameters and the bulk-source voltage

$n \approx 1.5 - 3$

and

$$V_t = \frac{kT}{q}$$

If $v_{DS} > 0$, then

$$i_D = K_x \frac{W}{L} e^{v_{GS}/nV_t}(1 + \lambda v_{DS})$$

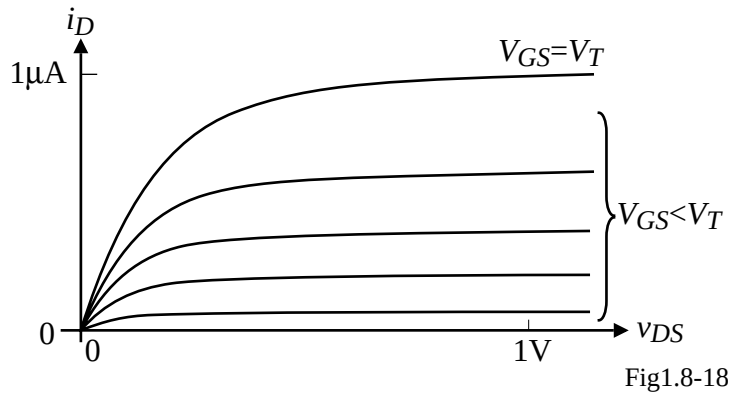


Fig1.8-18

Small-signal model:

$$g_m = \frac{\partial i_D}{\partial v_{GS}}\bigg|_Q = \frac{qI_D}{nkT}$$

$$g_{ds} = \frac{\partial i_D}{\partial v_{DS}}\bigg|_Q \quad \frac{I_D}{V_A}$$

SUBSTRATE CURRENT FLOW IN MOSFETS

Impact Ionization

Impact Ionization:

Occurs because high electric fields cause an impact which generates a hole-electron pair. The electrons flow out the drain and the holes flow into the substrate causing a substrate current flow.

Illustration:

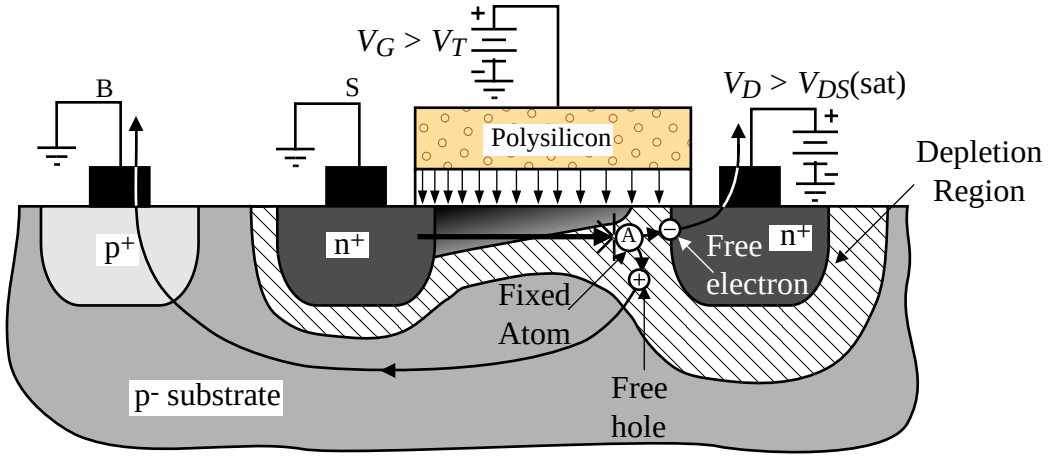


Fig1.8-16

Model of Substrate Current Flow

Substrate current:

$$i_{DB} = K_1(v_{DS} - v_{DS}(\text{sat}))i_D e^{-[K_2/(v_{DS}-v_{DS}(\text{sat}))]}$$

where

$K1$ and $K2$ are process-dependent parameters (typical values are $K_1 = 5\text{V}^{-1}$ and $K_2 = 30\text{V}$)

Schematic model:

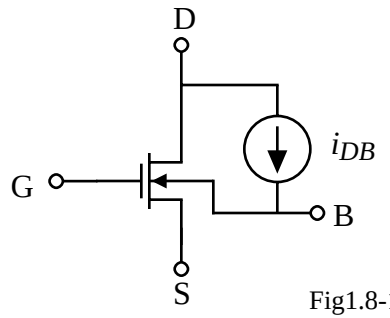


Fig1.8-17

Small-signal model:

$$g_{db} = \frac{\partial i_{DB}}{\partial v_{DB}} = K_2 \frac{I_{DB}}{V_{DS} - V_{DS}(\text{sat})}$$

This conductance will have a negative influence on high-output resistance current sinks/sources.

SUMMARY

Simple Large-Signal Model

Non-saturation-

$$i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}\right](1 + \lambda v_{DS})$$

Saturation-

$$i_D = \frac{W\mu_o C_{ox}}{2L}(v_{GS} - V_T)^2 (1 + \lambda v_{DS})$$

Small-Signal Model

$$g_m \equiv \frac{di_D}{dv_{GS}}\Big|_Q = \beta(V_{GS}-V_T) = \sqrt{2\beta I_D} \quad g_{ds} \equiv \frac{di_D}{dv_{DS}}\Big|_Q = \frac{\lambda i_D}{1 + \lambda v_{DS}} \approx \lambda i_D \quad g_{mbs} = \frac{g_m \gamma}{2\sqrt{2|\phi_F| - V_{BS}}}$$

Capacitances

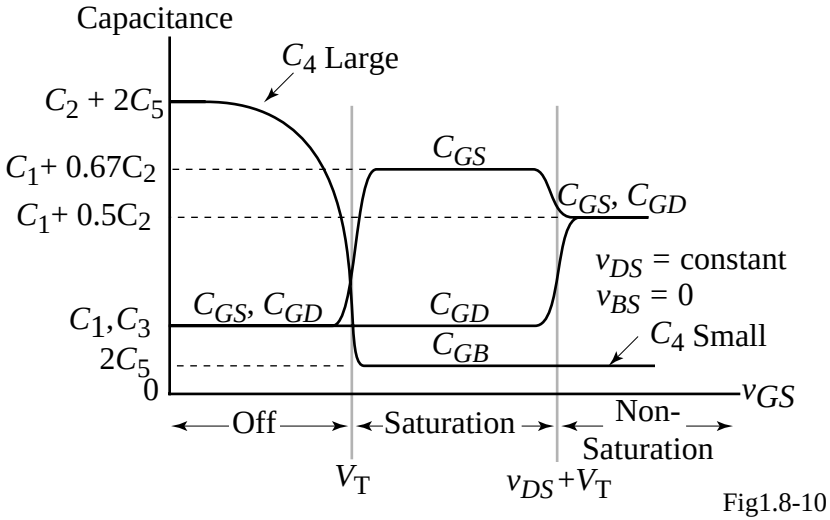


Fig1.8-10