Design of a Fully Differential Gain-Boosted Folded-Cascode Op Amp with Settling Performance Optimization

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ABSTRACT – **A single stage fully differential operational amplifier was designed in SMIC 0.25um mix-signal CMOS technology with 2.5V power supply. The designed op amp utilizes gain-boosting technique. The main op amp is a fully differential folded-cascode op amp with switched-capacitor CMFB. Two fully differential folded-cascode op amps with continuous-time CMFBs are used as auxiliary op amps to increase the open-loop gain of the main op amp. In addition, a simulation-based optimization method for the high-speed design of gain-boosted op amp was also presented. The simulation results show that the designed op amp achieves a dc gain of 102dB with a unity-gain frequency of 822 MHz. With the high-speed optimization, the 0.0488% settling time is 3.5ns.**

I. INTRODUCTION

In high performance analog integrated circuits, such as switch-capacitor filters, delta-sigma modulators and pipeline A/D converters, op amps with very high dc gain and high unity-gain frequency are needed to meet both accuracy and fast settling requirements of the systems. However, as CMOS design scales into low-power, low-voltage and short-channel CMOS process regime, satisfying both of these aspects leads to contradictory demands, and becomes more and more difficult, since the intrinsic gain of the devices is limited [1]. It is well known that active cascode gain-boosting technique can be used to increase the dc gain of an operational amplifier without degrading its high frequency performance. Unfortunately, the existence of pole-zero doublet will unfavorably affect the settling performance of the gain-boosted op amp [1], [2] and the effort of pushing up the doublet can raise stability problem [3], [4]. Based on that, this paper presents a simple but robust optimization design method; a sample fully differential gain-boosted folded-cascode op amp was also designed in SMIC 0.25um mix-signal CMOS process with 2.5V power supply. The organization of this paper is as follow: in section 2, the design process of the op amp and the optimization method are presented. Section 3 gives the simulation results. The summary is presented in section 4.

II. THE DESIGN AND OPTIMIZATION OF THE OP AMP

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Three fully differential folded-cascode op amps have been adopted in this design, one for main op amp, and the others for auxiliary op amps. The complete implementation is shown in Fig. 1.

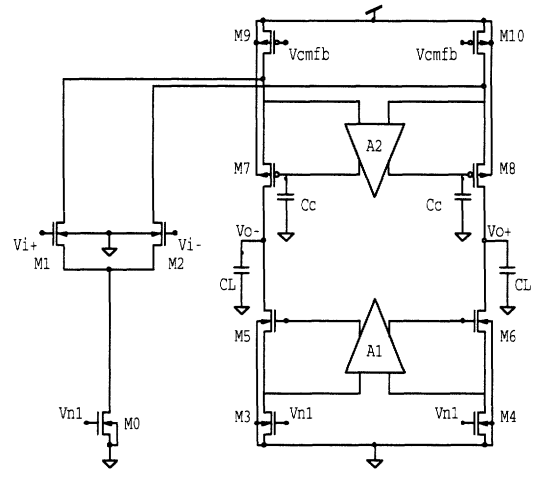

Fig. 1 Fully differential gain-boosted folded-cascode op amp

Because the gain-boosted op amp will be used in a closed-loop configuration, in order to minimize the virtual ground parasitic that reduces feedback factor, a NMOS differential pair is chosen as input stage in the main op amp. As for the two auxiliary op amps, there is not any difference except their input stages. The auxiliary op amp A_2 is shown in Fig. 2, and A_1 is not shown again for its similarity to A_2.

The ideal effect of the auxiliary op amp is to increase the output impedance of the main op amp by A_{auxi} times so as to improve the dc gain of the main op amp by the same times. At the same time, the dominant pole of the main op amp is pushed down by A_{auxi} times, where A_{auxi} is the dc gain of the auxiliary op amp. As long as the unit-gain bandwidth of the auxiliary op amp is designed to be larger than the -3dB bandwidth of the main op amp, the high-frequency performance of the main op amp will be unchanged, i.e. the gain-boosted op amp has the same high-frequency performance as that of the main op amp.

In fact, the gain-boosting technique can potentially raise two significant problems for the time-domain performance of the gain-boosted op amp, i.e. doublet and instability. Doublet, which can introduce slow-settling component, exists around the unity-gain frequency of the

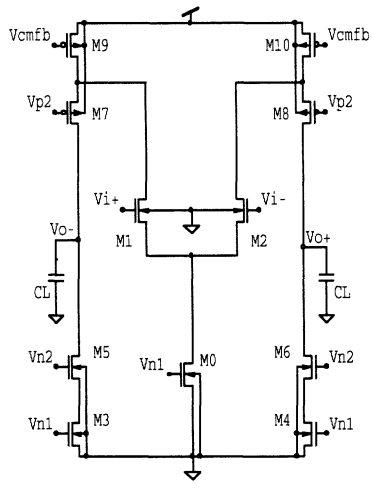

Fig. 2 Fully differential folded-cascode amplifier A_2

auxiliary op amp; a common solution is to increase the doublet up to a higher frequency [1]. However, if the doublet is pushed near the non-dominant pole of the main op amp, a pair of complex poles appears and the system is susceptible to instability [3], [4]. As a rule [1], the unity-gain frequency of the auxiliary op amp should be between the closed-loop dominant pole of the system and the second pole of the main op amp. In high-speed design with deep feedback, the former is often not much smaller than the latter. Therefore, selecting the unity-gain frequency of the auxiliary op amp becomes difficult. Fortunately, compensation capacitors can be placed at the output ends of the auxiliary op amps to fine-tune its unity-gain frequency [5]. However, it is difficult to select the optimal compensation capacitors when the gain-boosted op amp is used in different configurations (different feedback factor). In this paper, a very simple and simulation-based optimization method is presented:

a. After designing the main op amp, the unity-gain frequency of the two auxiliary op amps can be selected to be slight higher than that of the main op amp so that the pole-zero doublet will not cause the slow settling even the gain-boosted op amp is used in a closed-loop with unity-gain feedback.

b. Simulating the open-loop frequency response and the step response of the preliminarily designed gain-boosted op amp so as to make the choice of adding compensation capacitors at the output ends of each auxiliary op amp or not.

c. According to the parasitic capacitances at the gates of M5-M8 in Fig. 1, the appropriate range of the compensation capacitors C_c can be chosen.

d. When we simulate the step response of the gain-boosted op amp, the optimal C_c can be selected by sweeping them in the range given above.

CMFB circuit is indispensable in fully differential operational amplifier. Conventional dynamic SC-CMFB circuit, which is shown in Fig. 3, is adopted in the main op amp, for this CMFB circuit can save static power consumption and the common mode voltage sense circuit does not limit the output swing of the op amp. However,

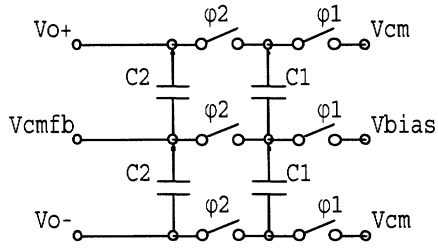

Fig. 3 SC-CMFB for the main op amp

the capacitors in SC-CMFB should be elaborately selected such that these capacitors will not over-load the main op amp or be affected by the charge injection of the switches.

Although the SC-CMFB circuit has many advantages described above, it is not appropriate for the two auxiliary op amps. On the one hand, the load capacitances of the two auxiliary op amps are small, as a result, the capacitors in SC-CMFB will smaller than them, and the charge injection of the switches will decrease the accuracy of the circuit. One the other hand, the output of each auxiliary op amp does not need high swing. Therefore, two continuous-time CMFB circuits are used. The CMFB circuit for A_2 is shown in Fig. 4. The CMFB circuit of A_1 is not shown, for it is similar to the one of A_2.

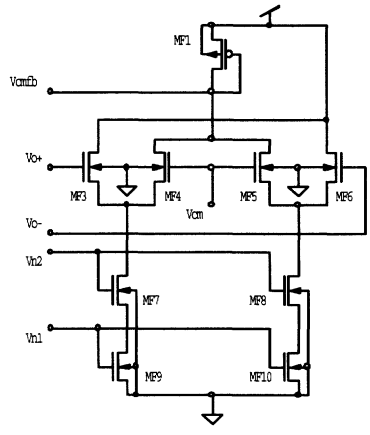

Fig. 4 Continuous-time CMFB for auxiliary op amp A_2

III. THE SIMULATION RESULTS

With the design process described above, a single stage fully differential gain-boosted folded-cascode op amp was designed and implemented in SMIC 0.25um mix-signal process with 2.5V power supply. The step response is simulated by a closed-loop configuration shown in Fig. 5. Here, both input capacitor C_i and feedback capacitor C_f are 1pF, while load capacitor C_L is 4pF. The C_p represents parasitic capacitances at the input of the op amp, which is 0.185pF. A 1V differential

step-signal is applied between Vin+ and Vin-. From the preliminary simulation results, we have found that the capacitances at the gates of M5 and M6 in the main op amp can provide enough phase margin for the auxiliary op amp A_1 and have less effects on the settling performance of the gain-boosted op amp, therefore, only two identical capacitors C_c are placed between the gates of M7-M8 and the ground as shown in Fig. 1. Sweeping the C_c from 0.1pF to 1.2pF during transient simulation, the optimal C_c can be found, as shown in Fig. 6, it is 0.5pF. In Fig. 6, we can also find that the settling time is insensitive to C_c in a wide range. Fig. 7 shows the settling performance with three different Cc. When C_c is 0.5pF, the corresponding differential step response of the gain-boosted op amp is shown in Fig. 8. Obviously,

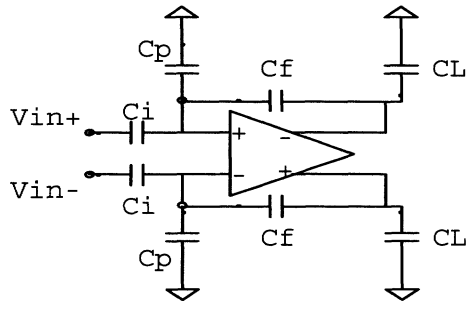

Fig. 5 The configuration for simulating the step response

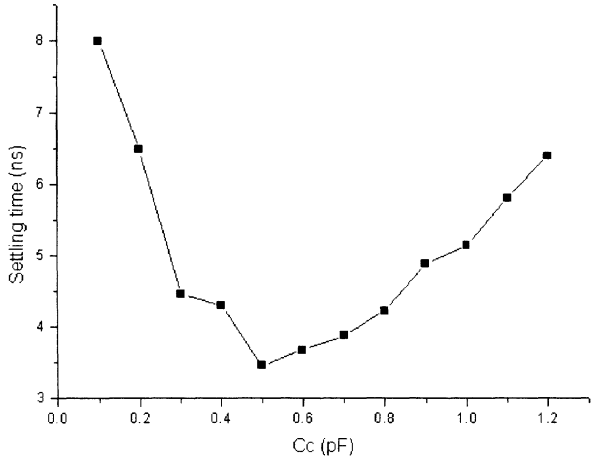

Fig. 6 Relationship between the settling time and C_c

there is no slow settling component and the output quickly settles to its final-state without any ringing and overshoot. When the load capacitance is 4pF and the compensation capacitors at the output ends of the auxiliary op amp A_2 are 0.5pF, the Hspice AC simulation results of the final designed op amp are shown in Fig. 9, form the figure, we can see that the gain-boosted op amp achieves a dc gain of 102dB, a unity-gain frequency of 822MHz with 62.5° phase margin. The major characteristics of the gain-boosted op amp are summarized in Table 1.

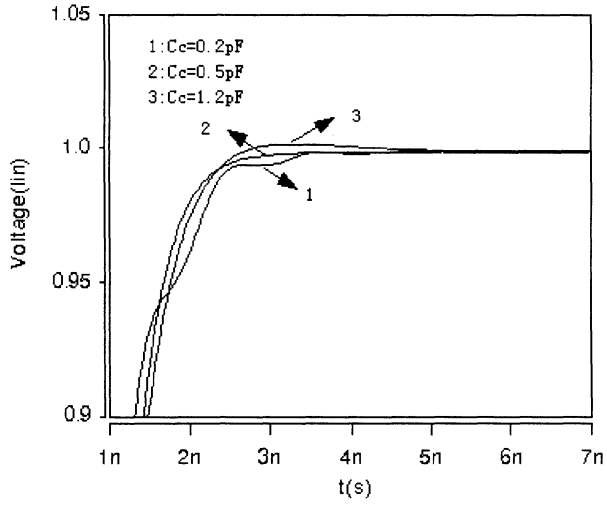

Fig. 7 settling performance with different Cc

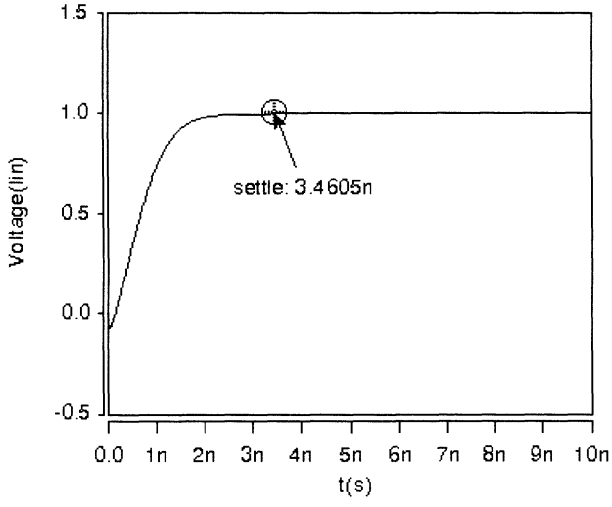

Fig. 8 Step response of the op amp (C_c is 0.5pF)

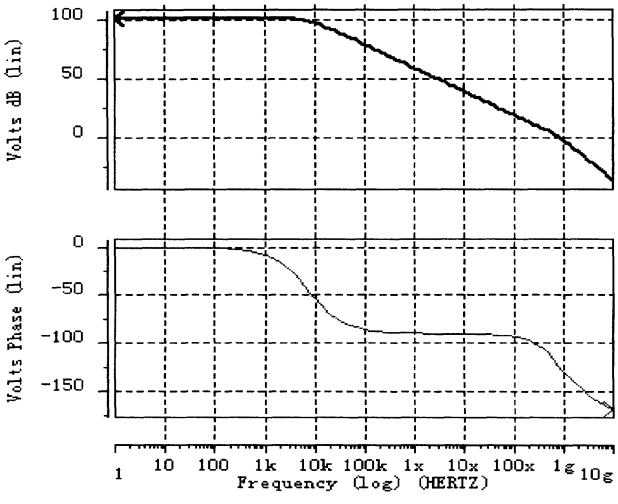

Fig. 9 Open-loop frequency response of the op amp (C_c is 0.5pF)

Table 1 The Specifications of the Op Amp

DC Gain	102dB
Unity-Gain Frequency	822MHz
Phase Margin	62.5°
Settling-Time (0.0488%)	3.5ns
Slew Rate	839V/us
Differential Output Swing	$2V_{pp}$
Power Supply	2.5V
Power dissipation	35mW
Load Capacitor	4pF

IV. SUMMARY

A simulation-based optimization method for the high-speed design of gain-boosted op amp was presented. A single stage fully differential gain-boosted folded-cascode op amp was designed and optimized with this method. The simulation results show that the slow settling component arising from the pole-zero doublet due to gain-boosting technique is avoided and the method provides a simple and robust scheme of gain-boosted op amp optimization in terms of settling performance. The exact characteristics of the op amp are shown in Table 1. This op amp will be used in a 10-bit pipeline ADC.

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