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Design of Rail-to-Rail Operational Amplifier with Offset Cancelation in 90nm technology

Daniel Arbet, Gabriel Nagy, Gábor Gyepes and Viera Stopjaková
Department of IC Design and Test
Institute of Electronics and Photonics, Slovak University of Technology
Bratislava, Slovakia
daniel.arbet@stuba.sk

***Abstract* – This paper deals with the design of a rail-to-rail operational amplifier (OPAMP) for a digital-to-analog converter. To achieve a low input offset of the OPAMP, a digital offset cancelation method has been proposed and used. The offset voltage in the range from -1.4 mV to 1 mV can be achieved. The OPAMP and additional hardware were designed in 90nm CMOS technology.**

Keywords – rail-to-rail operational amplifier; digital offset cancelation;

I. INTRODUCTION

Recent nanometer scaled technologies bring many new problems and issues in analog and mixed-signal design. Use of standard design techniques is very limited, and designers have to look for appropriate design methods and new approaches to facilitate the design of analog integrated circuits in nanometer technology. The main problem is rapid decrease of the transistor channel length that causes higher sensitivity to process variations. Thus, design of robust analog circuits in nanotechnologies might be a real challenge.

The most commonly used mixed-signal circuits are digital-to-analog and analog-to-digital converters. These devices are part of any complex circuit or system, which contains both digital and analog signal domains. Thus, for example, a binary weighted DAC is often used in mixed-signal integrated circuits. The basic building block of such converter is an operational amplifier. The important DC parameters of the OPAMP used in DACs are mainly input and output voltage ranges as well as the offset voltage. Process variation can cause deviation in all important parameters of the design. To solve this problem and make the design more robust, the programmable bias network was introduced and used in [1]. The second solution is a digital calibration of the OPAMP essential parameters [2].

In this paper, a rail-to-rail OPAMP design with digitally trimmed input offset for use in a binary weighted DAC is presented. In Section 2, the selected rail-to-rail input and output stage topologies are described. Consequently, a circuit for digital offset cancelation is presented in Section 3. In the last section, the simulation results and achieved parameters of the proposed OPAMP are presented and discussed.

II. RAIL-TO-RAIL OPAMP DESIGN

A. Rail-to-rail input stage

The rail-to-rail input stage allows the OPAMP to operate within the input voltage near to the voltage supply rails [3]. Traditional differential OPAMP may have either NMOS or PMOS input transistor pair, which allow the input voltage to operate near to positive (NMOS) or negative (PMOS) supply rail, respectively. Complementary topology with PMOS and NMOS differential stages, connected in parallel, achieves operating mode at both supply rails by combining the benefits of both previous configurations [3]. In our design, the rail-to-rail input stage topology using additional transistors (Mpx0, Mpx1, Mnx0, Mnx1) to stabilize input transistors' (Mp0, Mp1, Mn0, Mn1) transconductance, was used [4]. For simplicity, the common bias voltage (Vdd_half) for the stabilizating transistors has been used. Fig. 1 shows the input rail–to-rail stage used in the design of the proposed operational amplifier.

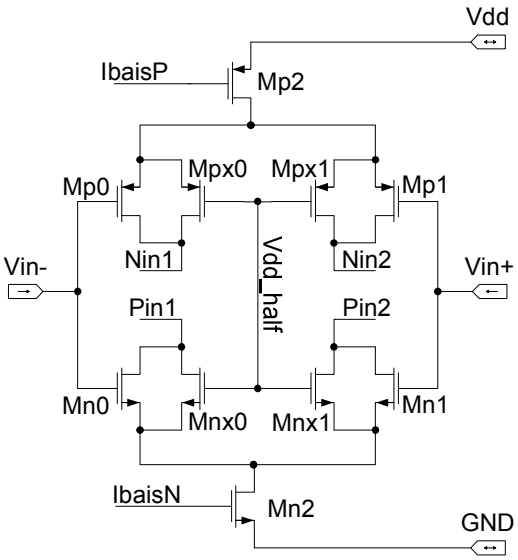

Figure 1. Rail-to-rail input stage

Simulation results shown in Figure 2 prove a relatively constant transconductance in the whole input voltage range from 0 V to 2.5 V.

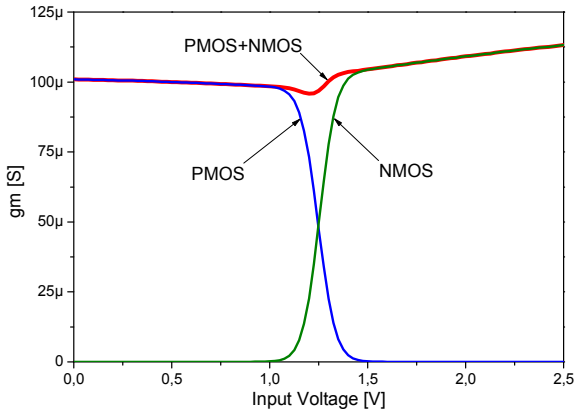

Figure 2. Tansconductance of the input stage

B. *Rail-to-rail output stage*

As an output stage, the push-pull inverter composed of transistors Mn7-Mp7 (Fig. 3) was employed. This configuration also known as complementary common-source allows the output to operate within a voltage range near to that given by supply rails. To achieve a high gain of the output stage, the input bias voltage (in the node Out1) must be set to half the supply voltage. In the output stage, both transistors are in saturation that causes current continually flowing from positive to negative rail [3]. To limit the uncontrolled steady-state bias current in the output stage, resistors R1-R4 were connected between the drain of transistors Mp5-Mp6, Mn5-Mn6 and respective output nodes (Fig. 3.) that shifts the bias voltage of the transistors in the output stage.

Between the input and output stages, a folded cascode stage was connected. To stabilize the operational point of the folded cascode and the output stage, and to achieve a high gain of the output stage, the Common-Mode Feedback (CMFB) network was employed [5]. CMFB network sets voltage at the cascode stage output nodes (Out1, Out2) to half the supply voltage.

Figure 3 shows the circuit diagram of the designed OPAMP. The input stage together with the folded cascode represents the first stage, while the push-pull inverter is the second stage of the designed amplifier.

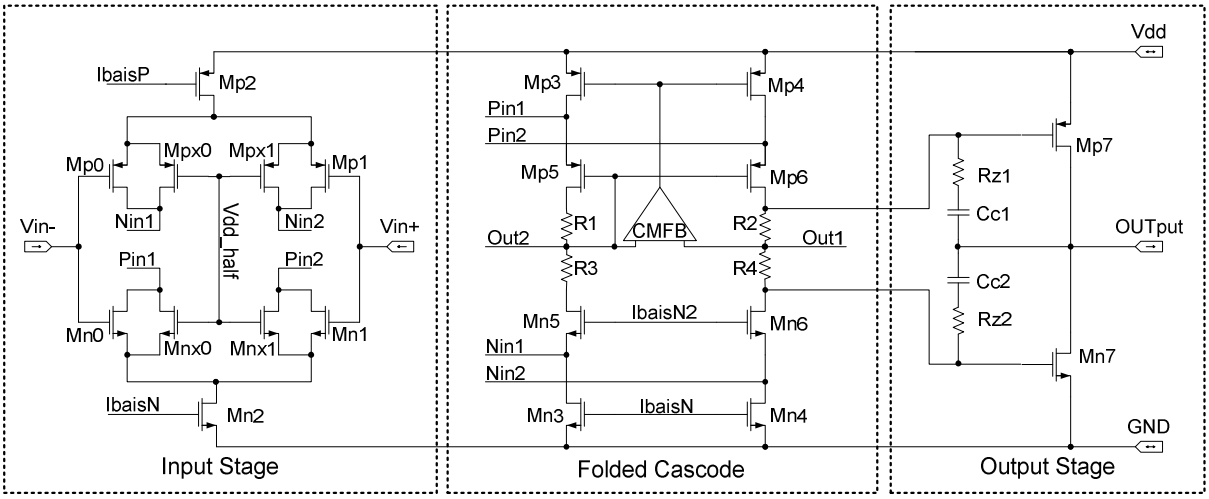

Figure 3. Schematic diagram of the whole designed amplifier

III. DIGITAL CIRCUIT FOR OFFSET CANCELATION

Device mismatch may influence (shift) the operation point of all transistors forming the amplifier. Therefore, it has to be taken into account that for the intended application of the proposed amplifier, the input offset voltage represents a critical parameter.

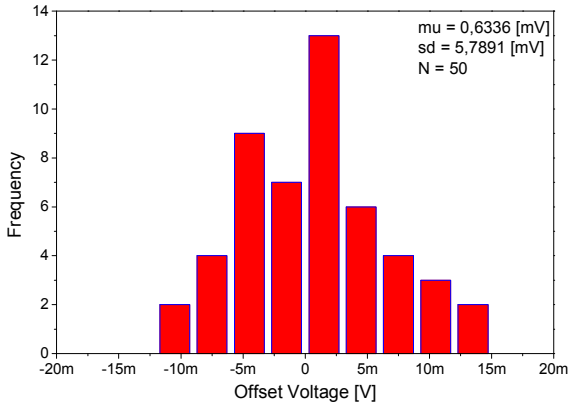

Figure 4. Offset voltage of the OPAMP from Fig. 3

Figure 4 shows the offset voltage of the OPAMP obtained from Monte Carlo analysis. One can observe that the offset voltage is kept within the range from -12 mV to 15 mV. Such high value of the offset voltage is due to the different currents flowing through the input stage and folded cascode.

A. *Offset cancelation circuitry*

To improve the undesired value of offset voltage, a 6-bit R/2R ladder was used to compensate the current difference in the folded cascode. The ladder is realized by the implementation of R/2R structure using MOS transistor to realize a pseudo-resistor of unit value R [2]. The main drawback of this structure is an imbalance in the current division [2]. To compensate this imbalance in R/2R ladder, the compensatory 3-bit R/2R ladder was used (Figure 5).

B. *Offset cancelation process*

The schematic diagram of the trimming circuit is show in Figure 5. Control signals for T-gates have been generated by the control logic, which is depicted in Figure 6. The counter starts count CLK pulses when

signal *TrimmingSig* is active. Frequency of CLK signal is 10 kHz. Counter's output signals (DT1 to DT6) turn-on T-gates in the corresponding branch of R/2R ladder. Then, the current collected from all open T-gates is pumped into the respective branch of the folded cascode stage (Nin1, Nin2), through the current mirrors. When the OPAMP output voltage is equal to VDD/2, the control logic generates signal *TrimEnd*, and the counter stops counting. The value, at which the counter stops, is held until the supply voltage is turned off. Thus, disadvantage of this offset compensation method is that the trimming process must be performed each time the power supply turns on.

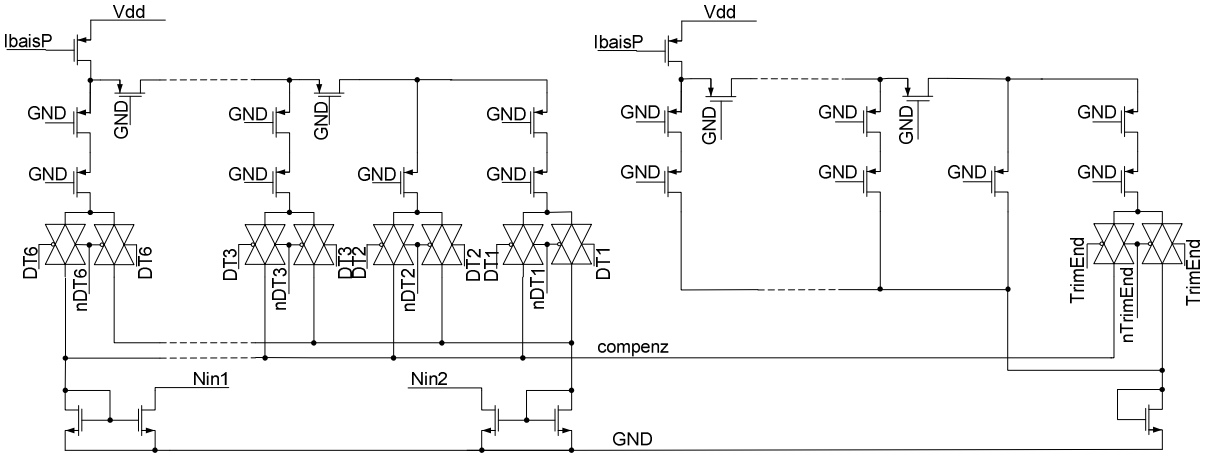

Figure 5. Offset compensation circuit

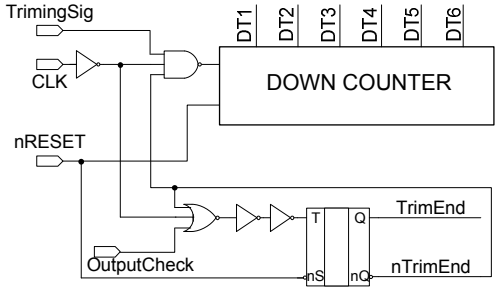

Figure 6. Control logic for the offset compensation circuit

IV. ACHIEVED RESULTS AND DISCUSSION

For design verification and evaluation of the main characteristics of the designed OPAMP, Corner Analysis (CA) and Monte Carlo (MC) analysis have been carried out using CADENCE design tools. Corner Analysis was performed for temperature range from -20 °C to 80 °C and for the supply voltage of 2.5 V, while performing 50 runs of MC analysis.

The trimming time (time needed to complete the offset cancelation process) obtained from MC analysis is depicted in Fig. 7. It depends mainly on the value of the offset voltage in the corresponding technology corner. For the best case, the calibration time of about 700 µs was achieved, while in the worst case, about 1.4 ms is required to complete the trimming process.

Figure 8 shows MC analysis results on the offset voltage after applying the trimming process. It can be observed that the input offset voltage has been reduced significantly, and it is kept within the range from -0.513 mV to 0.628 mV. This is an excellent result with respect to the high mismatch of the transistors.

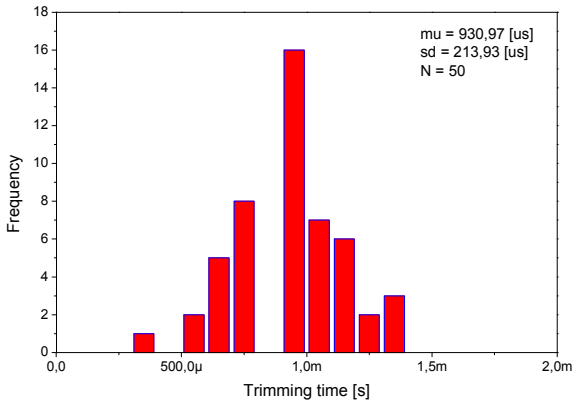

Figure 7. Trimming time

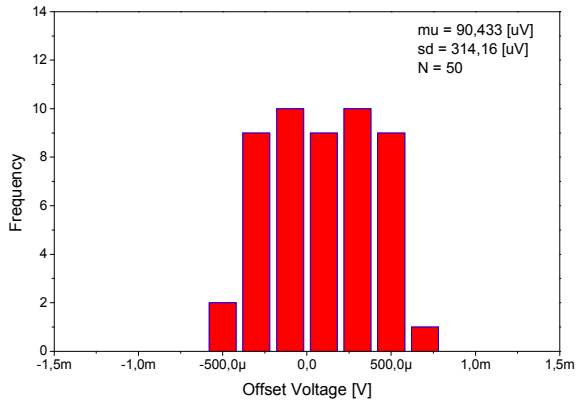

Figure 8. Offset voltage after applying the trimming

Dependence of the amplifier output voltage on the input voltage, obtained from CA, is depicted in Figure 9. One can observe that the input stage as well as the output rail-to-rail stage work correctly within all corners.

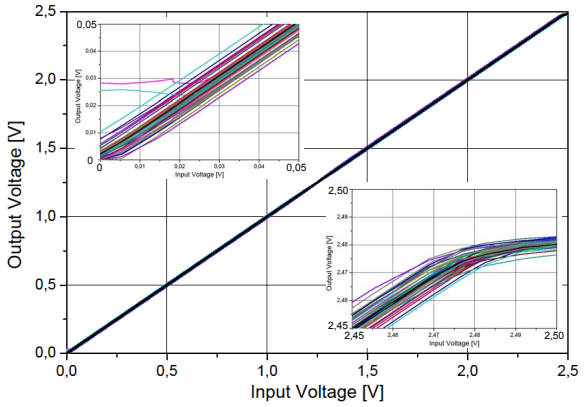

Figure 9. Ouput voltage dependence on input voltage

Figure 10 shows frequency and phase response of the designed OPAMP, obtained from corner analysis. It can be seen that the designed amplifier has bandwidth from 26 MHz to 70 MHz. Phase response characteristics prove a good OPAMP stability with the phase margin range from 42 to 83 degree.

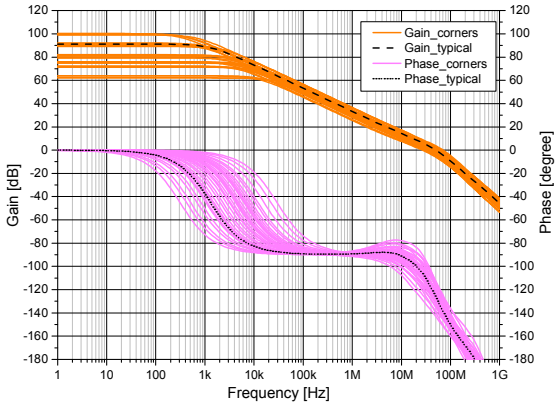

Figure 10. Frequency and phase response

The main parameters and its ranges obtained from MC analysis with 2.5 V supply voltage after the calibration are summarized in Table 1.

TABLE I. ACHIEVED OPAMP PARAMETERS

Parameter	min	typ	max
V_{DD} [V]	2.1	-	2.5
I_{SUPPLY} [µA]	52	74	105
ICMR [V]	0	0	0.027
Output voltage [V]	2.4765	2.481	2.4830
V_{OFFSET} [mV]	-0.513	0.090	0.628
A_V [dB]	62.2	91.1	100.1
f_{0dB} [MHz]	26.6	50.1	70.8
Phase Margin [°]	42	54	83
Gain Margin [dB]	-35	-27	-20
SR [V/µs]	22.6	39.8	68.4
$PSRR_{100kHz}$ [dB]	-54	-58	-62

As already mentioned, the designed operational amplifier will be used in a more complex circuit, where may be an interference in the supply voltage rail. Therefore, it is important to have a high power supply rejection ratio (PSRR). Power supply rejection ratio at frequency of 100 kHz may vary in the range from -54 dB to -62 dB.

V. CONCLUSION

Design of rail-to-rail (input and output) operational amplifier in 90nm CMOS technology is presented. Problem with mismatch of transistors in 90 nm process, which causes undesired scattering of the OPAMP parameters, was solved by employing the offset trimming circuit. Time required for the offset compensation process depends on the offset voltage in the corresponding technology corner and varies in the range from 700 µs to 1.4 ms. The compensated value of the offset voltage is in the range from -0.513 mV to0.628 mV, which represents about 4.2 % of the offset voltage before calibration.

The OPAMP current consumption, obtained from Corner Analysis is kept within the range from 52 µA to 105 µA. This relatively high current is mainly due to bias current sources for biasing the current source in the input stage as well as the cascode mirrors in the folded cascode stage. About 20 % of overall current consumption is the current drawn by the output stage. The achieved input voltage range is from 0 V to 127 mV, while the output voltage range is from 2.47 V to 2.48 V.

Future work will be focused on the implementation of the proposed OPAMP in an 8-bit binary-weighed R-2R D/A converter in 90 nm CMOS technology.

ACKNOWLEDGMENT

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