A Low-Voltage Low-Power Fully Differential Rail-to-Rail Input/Output Opamp in 65-nm CMOS

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***Abstract*— A new fully differential rail-to-rail input/output opamp with constant small- and large-signal behavior fabricated in 65-nm digital CMOS technology is proposed. A novel current-mode common-mode feedback circuit is introduced to regulate the signal behavior. Measurements are done when the supply voltage is ±0.5V and the load is 15pF. The opamp attains a DC gain of 100dB, a unity-gain frequency of 40MHz, a phase margin of 64° and a low power consumption of 720μW. The small-signal behavior variation is only ±2.2%. The large-signal behavior is also verified to be constant.**

I. Introduction

To achieve a better price-to-performance ratio for a system-on-chip design which integrates both analog and digital circuits, contemporary CMOS technologies are optimized for the digital parts and keep downscaling the device geometry and supply voltage. Hence, as a basic analog building block, opamp has a limited voltage headroom due to the low supply voltage, and it thereby needs rail-to-rail input/output signal swing to maximize the signal-to-noise ratio (SNR). Moreover, the signal behavior should be constant over the entire input common-mode (CM) range, not only to get a stable and power-efficient frequency compensation of the entire opamp, but also for the behavioral modeling in the system level design.

The conventional realization of constant signal behavior rail-to-rail input stage is to stack PMOS and NMOS transistors in the supply rail [1]. It suffers the matching problem between the mobility of electrons and holes. Recently developed solutions include floating-gate transistors [2], bulk-driven transistors [3], feedforward canceling [4] and CM adapter [5]. Floating-gate transistors have large capacitors connected to the input, so they greatly load the previous stage and create an extra pole in closed-loop applications. They will also be charged by the increasing gate leakage current due to technology downscaling. Bulk-driven transistors have low transconductance, bad AC performance, big input capacitance and huge noise. Feedforward canceling requires a strict matching between the amplification transistors and the input CM level sensing transistors. CM adapter has no full rail-to-rail input range and can only be used in unity-gain buffer. It also has large input offset and finite input impedance.

On the other hand, nanometer CMOS devices have very poor DC properties and more power is to be consumed to maintain the same analog performance [6]. Transistors in 65-nm CMOS technology possess extremely large output conductance, gate leakage and tunneling current and Early voltage (e.g., 4V for L=360nm, 1V for L=65nm). These issues make a low-power high-gain opamp difficult to implement, especially when the voltage headroom is also small.

A novel fully differential rail-to-rail input opamp with constant signal behavior implemented in 65-nm digital CMOS process is presented in this paper. An innovative current-mode common-mode feedback circuit is developed to enable the constant signal behavior rail-to-rail operation. A proper opamp architecture is established to overcome the poor DC properties of the used 65-nm CMOS technology. A very good overall performance is reached for the opamp.

II. Opamp Architecture

Three-stage structure is widely used for opamp design, because most of the popular power-efficient frequency compensation schemes are optimized for three stages [7]. However, as stated before, low-power high-gain opamp design is challenging in 65-nm CMOS technology owing to the inherited poor DC properties, and a three-stage topology cannot reach sufficient gain. So more stages are needed. If an opamp has more than three cascaded stages, multipath topology is normally employed [8], [9], in which the nested-feedforward stages consumes plenty of power though.

According to the problems discussed above, a four-stage nested-Miller compensation with a nulling resistor is designed for our work. No feedforward stage is used such that power is saved. The single-sided block diagram of the fully differential opamp is depicted in Fig. 1. R_n and C_n are the output resistance and capacitance of the n-th stage. R_L and C_L are the load resistance and capacitance plus the output resistance and capacitance of the last stage. C_{m1}–C_{m3} are the compensation capacitors, R_m is the nulling resistor. g_{m1} is the rail-to-rail input stage, which will be addressed more deeply in section

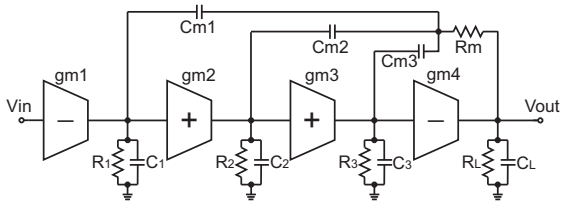

Fig. 1. Four-stage nested-Miller compensation with nulling resistor.

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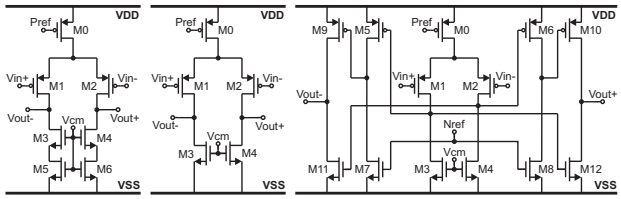


(a) (b) (c)

Fig. 2. The schematics of the (a) g_{m2} stage, (b) g_{m3} stage, (c) g_{m4} stage.

III. The g_{m2}, g_{m3} and g_{m4} stages are exhibited in Fig. 2(a), (b) and (c), respectively. Separate common-mode feedback blocks (CMFB) are built for each stage to get a more reliable fully differential topology. The CMFBs are not shown for brevity. V_{cm} is controlled by the CMFB of each corresponding stage. P_{ref} and N_{ref} are the bias voltages of the current sources. g_{m2} is a fully differential telescopic-cascode stage. The g_{m3} stage is a simple fully differential pair, which has larger output swing than the g_{m2} stage.

The output stage g_{m4} is designed as a fully differential rail-to-rail push-pull class-AB topology with high bandwidth, high output drive ability and high power transfer efficiency. The bias current in M0 in Fig. 2(c) is set as 40μA. A strong class-AB behavior is designed, such that the output stage possesses high power transfer efficiency. As a result, the class-AB quiescent current is only 15μA while the peak output current can be up to 40mA. This current is high enough to drive heavy loads. The transconductances of the output transistors M9(M10) and M11(M12) are set to be equal, therefore the positive and negative large-signal behavior are kept identical, and the push-pull performance is enhanced.

The values of g_{m1}, g_{m2}, g_{m3} and g_{m4} are 117.7μS, 286.9μS, 615.8μS and 13.57mS, respectively. The values of C_{m1}, C_{m2}, C_{m3} and R_m are 600fF, 300fF, 100fF and 7.5KΩ. Based on the analysis of the opamp transfer function and BSIM4 model simulation as well as the preference of adopting very small capacitors to save chip area, these values are chosen for the removal of the right-half-plane zeros and in-band pole-zero doublets to guarantee the opamp stability and a fast settling performance.

III. Rail-to-Rail Input Stage

As indicated in Fig. 3, the newly designed input stage consists of the g_{m1} stage of the opamp, an input CM level sensing block and the novel current-mode common-mode feedback mechanism.

In the g_{m1} stage, M1–M4 are two identical amplification pairs. Selecting P-type amplification transistors offers a better noise performance than N-type transistors in the used technology. N_{ref}, P_{ref} and V_{b1}, V_{b2} are the bias voltages of the current sources and cascode transistors. V_{cm} is driven by the CMFB of the g_{m1} stage. The constant signal behavior regulation is applied on the amplification pairs M1–M4. The voltage gain before regulating the signal behavior on M1–M4 are equalized by complementary voltage level shifters M7–M14, so as to get a more constant signal behavior. A folded-cascode stage composed by M17–M22 with two gain-boosting amplifiers A1–A2 is added, serving as a current summation stage to gather the regulated currents from different amplification pairs. Besides, the folded-cascode stage provides enough gain for the g_{m1} stage as well as a correct DC operating point for the next stage. Gain-boosting strategy is used to further improve the gain in 65-nm CMOS technology.

The input CM level is sensed by M35–M37. The rail-to-rail function is accomplished by alternating the operation between different amplification pairs, so there is a takeover region where both amplification pairs are working. Normally the voltage level of this takeover region is automatically defined by the amplification pairs themselves, and the input CM level sensing circuitry should generate the regulation signal correspondingly at different input CM levels. So the mismatch between the input CM level sensing transistors and the amplification transistors degrades the quality of signal behavior regulation. In our design, the voltage level of the takeover region is solely defined by V_{ref} via a comparator. The comparator has the same structure as the g_{m3} stage in Fig. 2(b). This innovation offers the advantage that the mismatch mentioned above, which is even more dramatic in 65-nm CMOS technology, no longer interferes the signal behavior regulation and the signal behavior constancy. The gain of the comparator only changes the width of the takeover

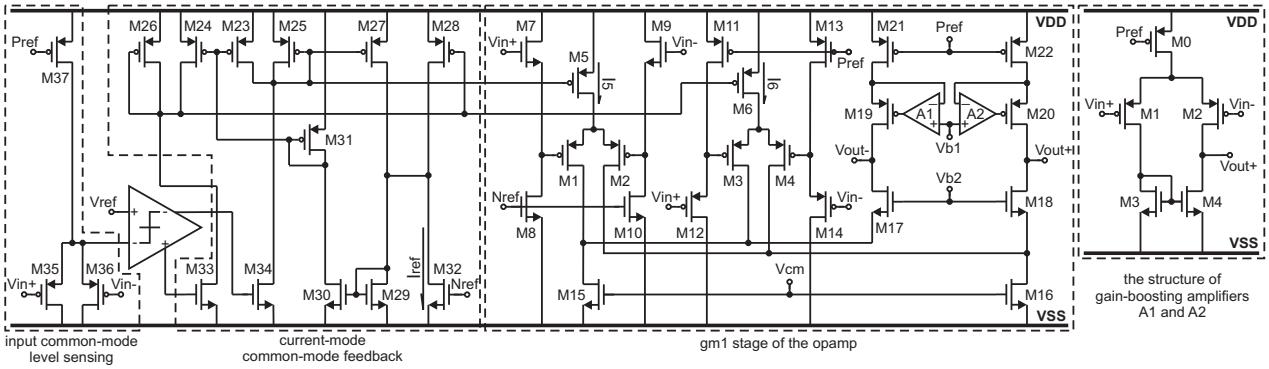


Fig. 3. Rail-to-rail input stage with constant signal behavior. The comparator structure is the same as the g_{m3} stage as shown in Fig. 2(b).

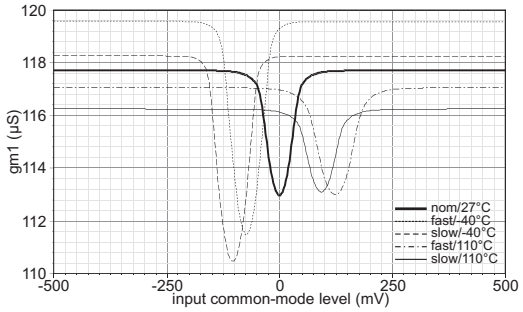


Fig. 4. Simulated g_{m1} versus input common-mode level at different temperatures and process corners.

region, so high gain is not compulsory.

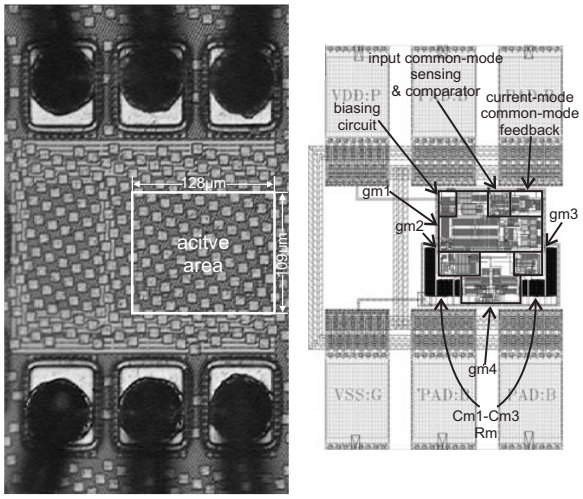
Let us denote the current in M5 as I_5, the current in M6 as I_6 and their summation I_5+I_6 as I_b. I_b is actually the total bias current of the amplification pairs M1–M4. The constant signal behavior over the input rail can be achieved by sustaining a constant I_b over the entire input rail [4].

The constant I_b is obtained by the innovative current-mode common-mode feedback mechanism, which is analogous to a common-mode feedback block for fully differential circuits. A pair of complementary current signals is generated in M33 and M34 by the comparator after sensing the input CM level. Hence, at different input CM levels, M33 and M34 provide I_5 and I_6 via current mirrors M25–M5 and M26–M6. The values of I_5 and I_6 are also duplicated in M27 and M28, so the confluence of I_5 and I_6 can be compared with a reference current I_{ref} flowing in M32. The comparison difference is captured by M29, and further subtracted from the currents in M33 and M34 by M23 and M24, such that the current-mode negative feedback is created. Thus, the currents in M25 and M26 as well as I_5 and I_6 are adjusted with respect to the input CM level. Consequently, I_b is always kept equal to I_{ref}, despite the change of the input CM level. When the input CM level is near the negative supply, M5 and M7–M10 are switched off, only M3 and M4 are active. I_b is supplied by M6. When the input CM level is approaching the positive supply, M6 and M11–M14 are turned off, only M1 and M2 are amplifying. I_b is contributed by M5. When the input CM level is in the middle of input rail, the input stage is in the takeover region and M1–M14 are all working. The performance of the signal behavior regulation has been simulated in different process corners and temperatures, as displayed in Fig. 4. The g_{m1} variation is 4.0% in typical condition and 6.6% in the worst case, which shows a good constancy and robustness.

IV. Experimental Results

The chip is fabricated in standard 65-nm digital CMOS technology. Fig. 5(a) is the chip micrograph, which is not clear owing to the passivation, so the layout is shown in Fig. 5(b), too. The active area occupies 0.014mm^2. All the measurements are done under ±0.5-V supply voltage and 15-pF load.

Fig. 6 is the measured nominal open-loop frequency response. The unity-gain frequency is 40MHz and the phase



(a) (b)

Fig. 5. (a) Chip micrograph. (b) Chip layout.

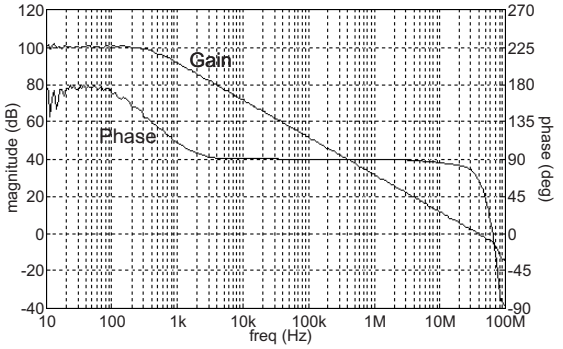


Fig. 6. Measured open-loop frequency response.

margin is 64°. Fig. 7 demonstrates 21 measured frequency responses in noninverting unity-gain configuration while the input CM level is swept from V_{SS} to V_{DD} with a step of 50mV. The minimum and maximum -3dB frequencies are 38.8MHz and 41.6MHz, indicating a small-signal behavior fluctuation

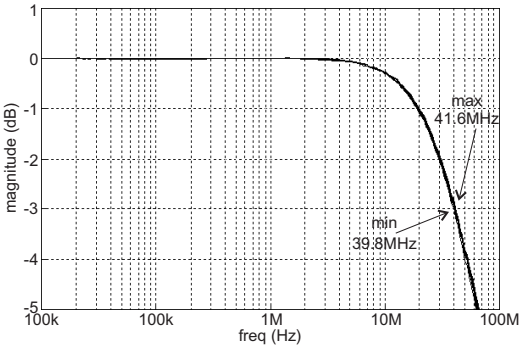


Fig. 7. Measured frequency response in a noninverting unity-gain buffer configuration when input common-mode level is swept from V_{SS} to V_{DD} with a step of 50mV, 21 curves included.

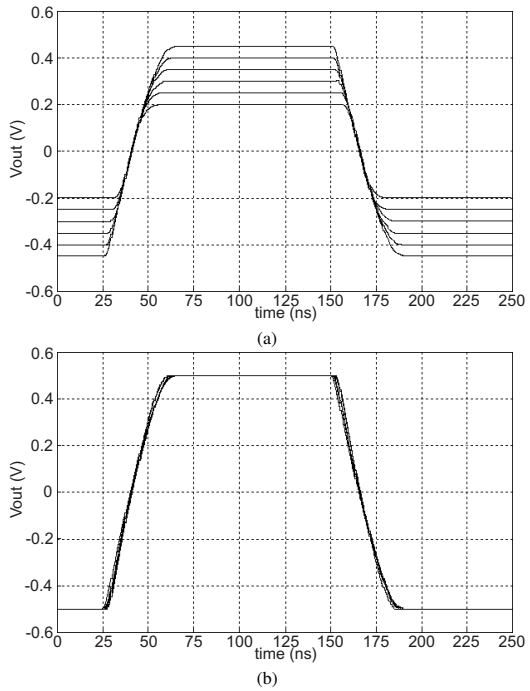


Fig. 8. Measured transient responses for (a) six step signals in noninverting unity-gain configuration, with amplitude varying from $\pm$0.2V to $\pm$0.45V by a step of 0.1V, middle point at 0V; (b) one differential output from seven differential input step signals with differential amplitude of $\pm$0.4V in open-loop and input CM level changing between $\pm$0.3V by a step of 0.1V.

TABLE I

SUMMARY OF THE MEASURED OPAMP PERFORMANCE

(TECHNOLOGY: 65-NM CMOS, SUPPLY VOLTAGE: $\pm$0.5V, LOAD: 15PF.)

DC open-loop gain	100dB
Unity-gain frequency	40MHz
Phase margin	64°
Power consumption	0.72mW
g_m-variation	$\pm$2.2%
SR+/-	33.71/33.82V/μs
Settling time 1%+/-	39/40ns
Input offset voltage	3.7mV
Input noise@100kHz	186nV/$\sqrt{\text{Hz}}$
IM3,0.8V$_{pp}$@4MHz	-53dB
THD,0.9V$_{pp}$@4MHz	-66dB
CMRR@10Hz	74dB
PSRR@10Hz	65dB
Active area	0.014mm^2

over the entire input CM range of only $\pm$2.2%, which can be regarded as constant for general analog applications, especially in such a technology with significant mismatch.

The large-signal behavior is inspected in both closed- and open-loop configuration. Fig. 8(a) exhibits the measured transient responses for six step signals in noninverting unity-gain configuration, with amplitude varying from $\pm$0.2V to $\pm$0.45V by a step of 0.1V. The middle points are all at 0V. Fig. 8(b) is the measured open-loop transient responses at one differential output from seven differential input step signals with differential amplitude of $\pm$0.4V and input CM level changing between $\pm$0.3V by a step of 0.1V. Both tests show a very constant large-signal behavior in the whole input CM range. The measurements also show a fast settling, proving an adequate stability of the opamp. The slew-rate+/- is 33.71/33.82V/μs and the settling time+/- for 1% accuracy is 39/40ns.

The performance of the chip is summarized in Table I. Both 3rd-order intermodulation (IM3) and total harmonic distortion (THD) measurements are done in a noninverting unity-gain configuration at 4MHz. IM3 is acquired from a 2-tone signal at 3.9/4.1MHz with the amplitude of 0.8Vpp at each output, while THD is measured with the amplitude of 0.9Vpp at each output. The noise measurement result manifests that the chip has a comparable input noise performance to other relevant designs, even if it is fabricated in a noisier technology.

V. CONCLUSION

A novel 65-nm CMOS rail-to-rail input/output opamp with constant signal behavior is described in this paper. The innovations to get constant signal behavior include a newly designed current-mode common-mode feedback system as well as allocating the input common-mode level sensing and the amplification to two separate circuitries. An efficient four-stage nested-Miller nulling-resistor structure is suitably composed to achieve a high gain with small power consumption and decent stability, despite the extremely poor DC properties of the used technology. Measurement results show that the implemented opamp has very constant small- and large-signal behavior as well as good overall performance.

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