MIM CAPACITOR

1. PURPOSE OF CURRENT RELEASE

A new fringe capacitance modelization is applied with the taken into account of the conform transformations theory. The corresponding Schwarz-Christoffel methodology is developed in order to calculate the accurated fringe contributions of the plates device.

2. GENERAL VIEW

According to the metallization option, the MIM device is placed above the M_i level (i=6,...,9) (Figures). The proposed MIM models take into account the metal 6 to metal 9 MIM option devices.

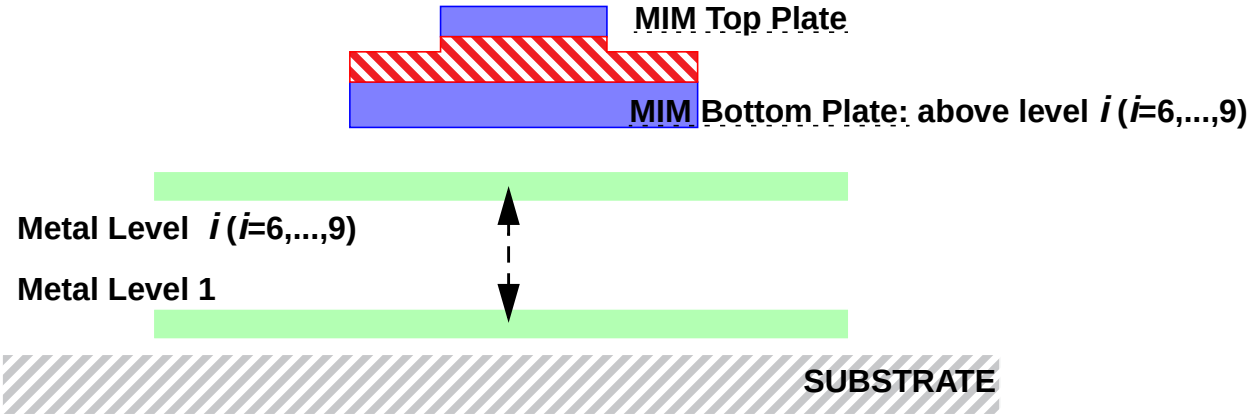

figure 1: Schematic of the CMOS090 MIM metallization options

3. MODEL FEATURES

Each device is composed of two description levels (M1, M2) coupled with the two pin model definitions. Each one is managed by the LPE flag option, which permits to select the Resistor/ Capacitor access modeling mode. See the following table to describe the proposed options :

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flag use to switch on/off device access modeling (for post layout simulation)

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lpe	Body	Access_R	Access_C	Extraction_mode
0	yes	yes	yes	--
1	yes	yes	no	C
2	yes	no	yes	R
3	yes	no	no	RC

The Front-End Models (F-E) :

- **M1**, a simple model which accounts for intrinsic and parasitic capacitances (between the top/ bottom plates and bottom_plate/substrate), but it excludes parasitic series resistances

(LPE=0).

- **M2**, a more comprehensive model which accounts for intrinsic and parasitic capacitances and series resistances (LPE=0).

The Back-End models (B-E) :

- The **M1** B-E model is identical to the M1 F-E model concerning the top/bottom plates contributions, but it excludes the bottom_plate/substrate components (LPE=1,2 or 3 according to the user choice).
- The **M2** B-E model is identical to the M2 F-E model concerning the top/bottom plates contributions, but it excludes the bottom_plate/substrate components (LPE=1,2 or 3).

Both capacitor models calculate the parasitic capacitances which are accounted between the top and the bottom plates. It concerns the following contributions (Fig 1):

- the intrinsic capacitance between the top/bottom plate surfaces.
- the fringe contributions caused between the top plate sides and the bottom plate surface (C_{side}, C_{top}, C_{bottom}).

M2 models include two series resistances:

- one for the top plate, to account for the via contact resistance and these of the top plate resistance.
- one for the bottom plate, to take into account the corresponding bottom plate components.

4. MODEL NOMENCLATURE

2fF/µm^2 Front-End MIM capacitor (Metal Option level 6 to 9): **CMIMMK**, **CMIMMK_ACC**.

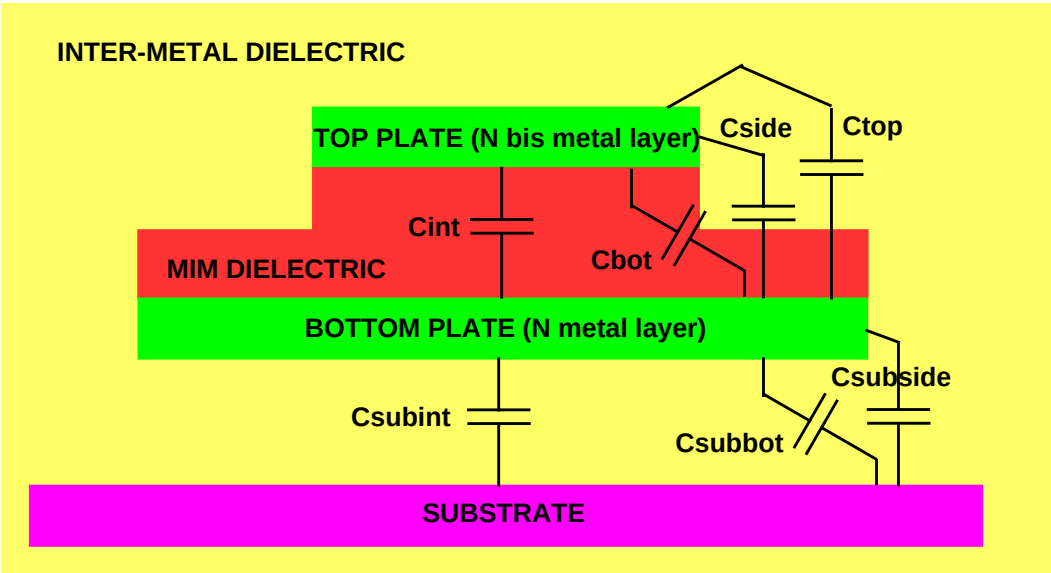

figure 2: Schematic of the capacitance calculated components

5. MIM CAPACITANCE MODEL INSTANTIATION

Cxx **ModelName First_Pin Second_Pin B** Carea=**Carea** Cperi=**Cperi** lpe=**lpe_value**

where First_Pin is the node connected to the top plate, Second_Pin the node connected to the bottom plate and B the node connected to the substrate.

For both types of the MIM capacitors, **Carea** is the desired capacitor area value and **Cperi** is the desired capacitor perimeter.

lpe is the flag used to switch on/off the device access modeling for the post-layout simulation.