Sample and hold circuits for low-frequency signals in analog-to-digital converter

Article · July 2015

DOI: 10.1109/ICTRC.2015.7156415

2 authors:

Soliman A. Mahmoud
University of Sharjah
204 PUBLICATIONS **1,533** CITATIONS
SEE PROFILE

Tasnim Nazzal
University of Sharjah
8 PUBLICATIONS **31** CITATIONS
SEE PROFILE

Sample and Hold Circuits for Low-Frequency Signals in Analog-to-Digital Converter

Soliman A. Mahmoud and Tasnim B. Nazzal
Department of Electrical and Computer Engineering
University of Sharjah
Sharjah, UAE
{solimanm, U00041020}@sharjah.ac.ae

Abstract*—Different sample and hold (S/H) circuits are introduced, analyzed and simulated in this paper. It aims to illustrate the suitable sample and hold (S/H) circuit technique that is used in low voltage operation. In addition to that, a suitable sample and hold (S/H) circuit for electrocardiogram (ECG) signal is presented. A modified versions of passive free op-amp sample and hold (S/H) circuit is discussed in order to compensate the induced error. These different sample and hold (S/H) circuits were simulated using 90nm CMOS technology on LT Spice IV. According to the simulation results, the passive free op-amp sample and hold circuit has a signal to noise and distortion ratio (SNDR) of 54.34 dB. On the other hand, the differential passive free op-amp sample and hold circuit has 56.31 dB for a 250 Hz-500 mV_{p-p} input sinewave and ECG signals. The sampling rate is 10 KS/sec, and the supply voltage is 1V. The simulation results show that the differential passive free op-amp sample and hold (S/H) circuit is the best candidate for low-frequency signals.

Keywords*—S/H; ECG; Bootstrapped; ADC; Differential.

I. INTRODUCTION

Analog to digital converter (ADC) is considered a significant data converter system. It is one of the main building blocks of electrocardiogram (ECG) detection system [1][2]. It consists of sample and hold (S/H) circuit that has an important effect on its overall performance. There are many types of S/H circuits. A suitable S/H circuit will be chosen based on the required application. The desired sampling rate are balanced with the strengths and weakness such as signal to noise and distortion ratio (SNDR), speed and power consumption. In addition to that, operating at low voltage should be considered in selecting the suitable S/H where the device reliability should be achieved.

Fig. 1, shows passive free op-amp S/H circuit. It is considered one of the simplest S/H circuits that can be realized using a CMOS technology. It consists of single transistor M_1 and a sampling capacitor C_S. It operates in a simple way by tracking the analog input signal while the transistor is on. In the off phase, it samples the input signal across the sampling capacitor [3].

The objective of this paper is to choose the best S/H circuit candidate for an ECG signal among the introduced types. Section II discusses passive free op-amp S/H circuit problems. Section III illustrates passive free op-amp S/H circuits without bootstrapping. Passive free op-amp S/H circuits with bootstrapping are presented in section IV. The simulation results is in section V. Section VI concludes the paper.

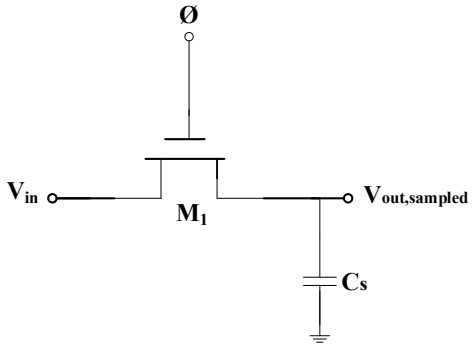

Fig. 1. Passive free op-amp S/H circuit [3]

II. PASSIVE FREE OP-AMP SAMPLE AND HOLD CIRCUIT PROBLEMS

Charge injection and clock feedthrough are considered two major problems occur in passive free op-amp S/H circuit. It is happening when a transistor is used as a switch in a switched capacitor circuit. This section introduces these two problems briefly [4].

A. Charge Injection Problem

This problem occurs when the clock Ø goes high. The NMOS transistor turns on, and the input voltage is sampled by the capacitor C_S. Due to the inverted channel, a charge under the gate oxide is produced, and it is given as follows:

$$Q_{ch} = W\ L\ C_{ox}\ (V_{dd} - V_{in} - V_{tn}) \quad (1)$$

Then, when the clock Ø goes low, The NMOS transistor turns off. The created channel charge will flow out from the NMOS gate into its source and drain creating an error in the sampled voltage. If all the charges are injected on the sampling capacitor C_S, the sampled output voltage is given by the following equation:

$$V_{out} = Vi_n\ (1+ (W\ L\ C_{ox})/\ C_S) - (W\ L\ C_{ox}\ /\ C_S\ )(V_{dd} - V_{tn}) \quad (2)$$

Therefore, the sampled output voltage is affected by two parameters. These parameters are a non-unity gain $(1+ (W\ L\ C_{ox})/\ C_S)$ and a constant offset voltage $- (W\ L\ C_{ox}\ /\ C_S\ )(V_{dd} - V_{tn})$ [4].

B. Clock Feedthrough Problem

It is defined as the coupling between the clock transitions and the sampling capacitor by the MOS transistor through its gate-drain or gate-source overlap capacitances. When the clock Ø goes high, an overlap capacitance is fed through the gate-source, the gate-drain, or both. While in the off state of the transistor, a capacitive divider is created. This operation result in an offset voltage which is given as follows:

$$\Delta V_{offset} = (C_{ov} / (C_{ov} + C_S)) V_{dd} \quad (3)$$

Where C_{ov} is the overlap capacitance [4].

III. Passive Free Op-amp Sample and Hold Circuit without Bootstrapping

This section presents passive free op-amp S/H circuit with some modified versions of it. These modified versions help in minimizing charge injection and clock feedthrough effect and compensate the errors.

A. Passive Free Op-amp Sample and Hold Circuit with Dummy Switch

This method is considered one of the most common methods that is used to overcome the charge injection and clock feedthrough effect. Fig. 2, shows a passive free op-amp S/H circuit with dummy switch. M_2 is a dummy switch with its source and drain shorted. It is placed in series with M_1 having a complement clock of Ø. When M_1 turns off, and M_2 turns on, M_2 will absorb the channel charge deposited on C_S. The following equations express the injected charge Δq_1 and the absorbed charge Δq_2 respectively as follows:

$$\Delta q_1 = W_1 L_1 C_{ox} (V_{dd} - V_{in} - V_{tn1}) / 2 \quad (4)$$

$$\Delta q_2 = W_2 L_2 C_{ox} (V_{dd} - V_{in} - V_{tn2}) \quad (5)$$

In order to achieve $\Delta q_1 = \Delta q_2$, the channel width of M_2 should be half that of M_1 assuming the channel length of both transistors is equal. Thus, the charge injection and clock feedthrough will be suppressed [4].

B. Differential Passive Free Op-amp Sample and Hold Circuit

This circuit plays role in minimizing the charge injection and clock feedthrough effect. It has a principle of applying differential balanced input with two matched sampling capacitors C_{S1} and C_{S2} as shown in Fig. 3 [5].

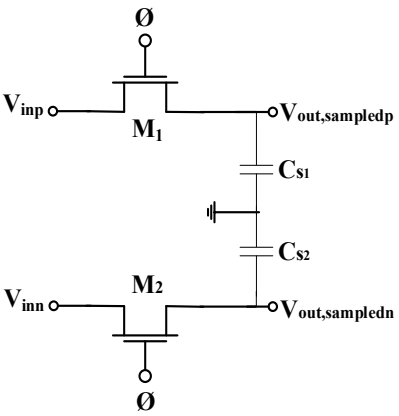

Fig. 3. Differential passive free op-amp S/H circuit [5]

C. Passive Free Op-amp Sample and Hold Circuit using Transmission Gate

This technique is based on replacing the single transistor in Fig. 1, with a transmission gate as shown in Fig. 4. If the size of PMOS transistor M_P is taken to be the same as NMOS transistor M_N. Then, the charge injection due to each transistor will be canceled when the transmission gate turns off. PMOS transistor M_P have the advantage in enhancing the on-conductance between the input and output when the input is close to the supply voltage [3][6].

However, at the circuit level, the conventional analog switches consist of transmission gates in the low voltage operation may not be fully turned on as they are under a higher voltage operation. It is happening when the sum of the absolute value of the PMOS threshold voltage and that of the NMOS is greater than the supply voltage. The MOSFETs expected to be turned on may now have extremely poor conductance and would limit the bandwidth of the circuits. Therefore, a bootstrapped technique was required [6].

IV. Passive Free Op-amp Sample and Hold Circuit with Bootstrapping

Two types of bootstrapping techniques have been introduced in this section. One of them is using single bootstrapped switch with bootstrapped circuit. The other one is using transmission gate with boosted driver circuit. These techniques are convenient in low voltage operation.

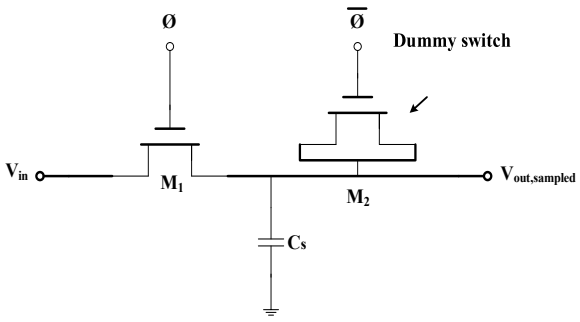

Fig. 2. Passive free op-amp S/H circuit with dummy switch [4]

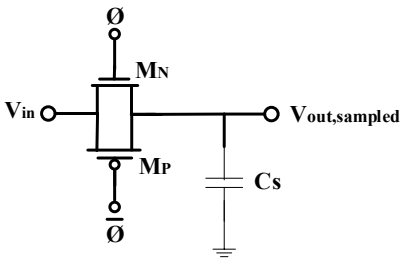

Fig. 4. Passive free op-amp S/H circuit using transmission gate [3]

A. *Passive Free Op-amp Sample and Hold Circuit with Boosted Driver*

Fig. 5, shows passive free op-amp S/H circuit with boosted driver using transmission gate. The goal of this circuit is to achieve both low power and a wide bandwidth. The gate of the transistor M_N is connected to the boosted driver output. It has a periodical signal switching between ($2V_{dd}$ - ΔV) and the ground. (ΔV) results from the charge sharing between the capacitor C_2 and the parasitic capacitance at the gate of M_N. It is done by applying a square wave input signal of (V_{dd}). When Ø is high, the bottom plate of C_2 and the top plate of C_1 are charged to (V_{dd}). When Ø goes low, the supply voltage is applied to each second capacitor plates. Then, the charge stored in C_2 is transferred to the gate of M_N by M_3 with an inverted square wave output which is generated according to:

$$V_{gate\ MN} = 2V_{dd}\ (C_2 / (C_{gate\ MN} + C_2 + C_{parasitic})) \qquad (6)$$

The bandwidth of this circuit is ($1/2 \prod R_{on}\ C_S$), where R_{on} is the on-resistance of the M_N switch. In this technique, the on-resistance of the sampling switch is small and varying due to (V_{GS}) variation [6][7]. A simulation result shows a zoomed ($V_{out,sampled}$) with inverted boosted clock of 2V in Fig. 6. The supply voltage is 1V.

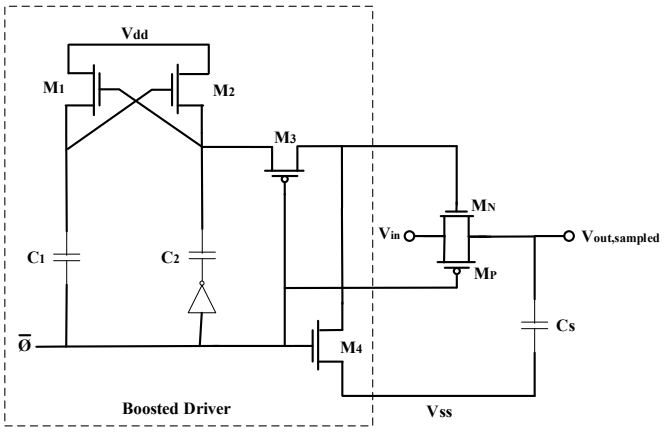

Fig. 5. Passive free op-amp S/H circuit with boosted driver [6]

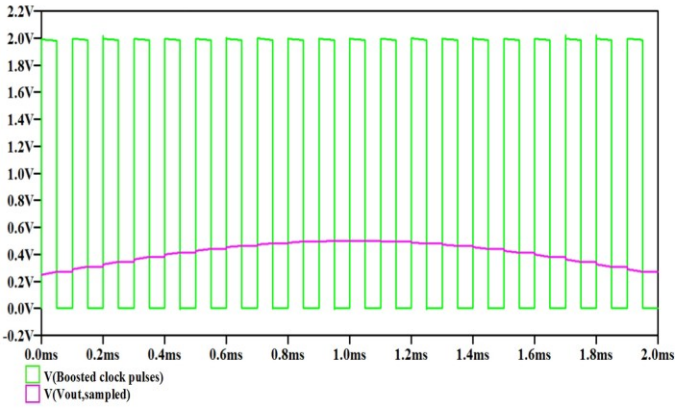

Fig. 6. Zoomed (Vout,sampled) with inverted boosted clock pulses formed on the gate of M_N

B. *Passive Free Op-amp Sample and Hold Circuit with Bootstrapped Switch*

This technique is used to maintain the device reliability constraints at low voltage. It does not subject the device to large terminal voltage, and it keeps the device voltages within the rated supply voltage. It is done by keeping the gate-source voltage of the sampling switch constant and equal to (V_{dd}) regardless of the input signal. Fig. 7, illustrates passive free op-amp S/H circuit with bootstrapped switch. It operates on a single phase clock Ø that turns M_{11} on and off. In the off state (Ø is low), M_7 and M_{10} discharge the gate of M_{11} to ground. In this phase, (V_{dd}) is applied across capacitor C_3 by M_3 and M_{12}. This capacitor will act as the battery across the gate and source during the on phase. The job of M_8 and M_9 is to isolate the switch from C_3 while it is charging. In the on state (Ø is high), the gate of M_8 will be pulled down by M_5. It will allow the charge to flow from the battery capacitor C_3 onto gate G. This turns on both M_9 and M_{11}. M_9 enables gate G to track the input voltage S shifted by (V_{dd}). M_7 and M_{13} are not functionally necessary but to improve the circuit reliability. Device M_7 reduces the (V_{DS}) and (V_{GD}) experienced by device M_{10} when Ø is low. The channel length of M_7 can be increased to improve its punch further through voltage. Device M_{13} ensures that (V_{GS8}) does not exceed (V_{dd}). M_1, M_2, C_1, and C_2 form a clock multiplier that enables M_3 to charge C_3 during the off phase. C_3 must be sufficiently large to supply charge to the gate of the switching device in addition to all parasitic capacitances in the charging path. Otherwise, charge sharing will significantly reduce the boosted voltage according to equation (7), where C_P is the total parasitic capacitance connected to the top plate of C_3 while it is across the main switching device M_{11}.

$$V_G = V_S + ((C_3 / (C_3 + C_P))\ V_{dd}) \qquad (7)$$

As a result, this technique keeps the on-resistance small and constant, improve the switch linearity, reduce the charge injection, and increase the settling speed and input bandwidth [8][9].

Fig. 8, illustrates a simulation result of the input signal with the clock pulses formed on G. It can be noticed that (V_{GS11}) has a constant value equals to the supply voltage of 1V independent of the input signal.

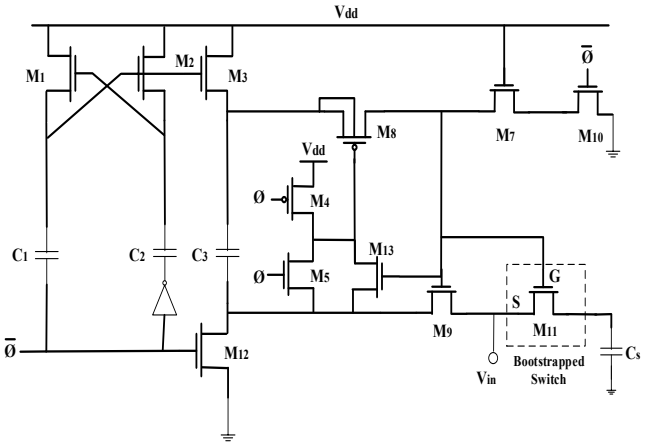

Fig. 7. Passive free op-amp S/H circuit with bootstrapped switch [8]

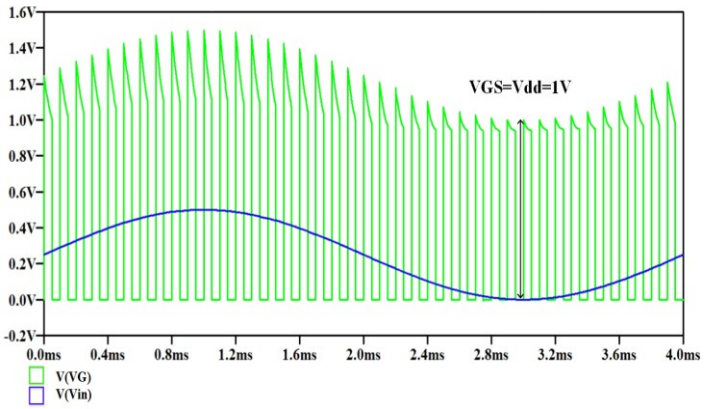

Fig. 8. Input signal with the clock pulses formed on G

V. Simulation Results

A simulation was done for the introduced S/H circuits using 90nm CMOS technology on LT Spice IV for low-frequency signals. The input signal has a frequency and amplitude of 250 Hz and 500 mV_{p-p} respectively. The clock frequency is 10 KHz, and the supply voltage is 1V. Fig. 9, displays the output sampled voltage of a real recorded ECG signal. A zoomed of the selected part in Fig. 9, is shown in Fig. 10. The SNDR was calculated for the different introduced S/H circuit. Furthermore, the average power consumption over one period is measured for the presented S/H circuits. Table.1 shows the simulation results.

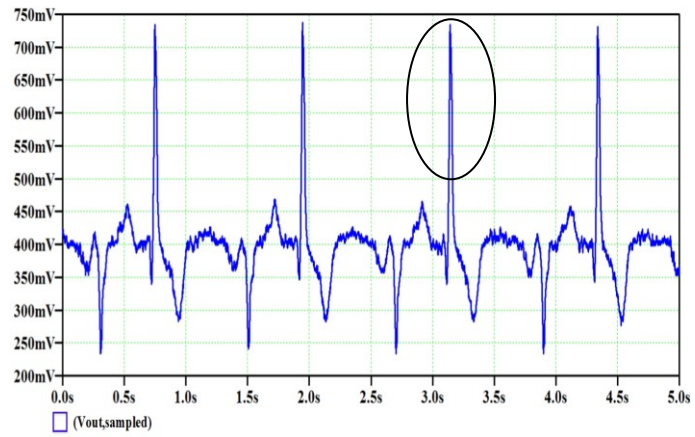

Fig. 9. Sampled output voltage (Vout,sampled) of a real recorded ECG signal with sampling frequency of 10 KHz

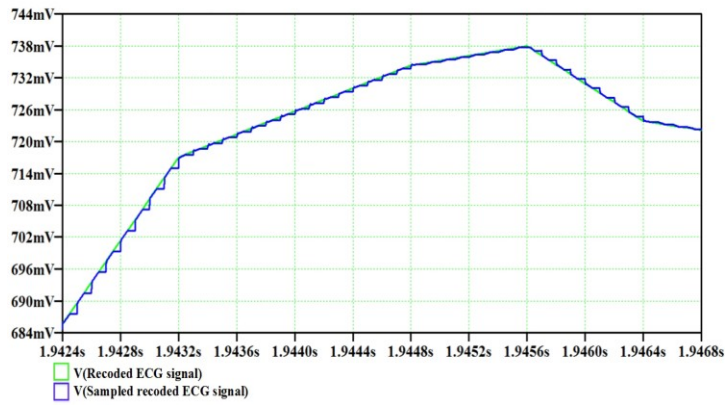

Fig. 10. Zoomed sampled output voltage (Vout,sampled) of a real recorded ECG signal

TABLE. 1. SNDR and average power consumption for different S/H circuits

S/H Circuit Type	SNDR (dB)	Power Consumption
Simple S/H	54.34	-
Differential S/H	56.31	-
S/H with Dummy Switch	54.39	-
S/H using Transmission Gate	54.42	1.4 pW
S/H with Boosted Driver	54.65	1.09 nW
S/H with Bootstrapped Switch	54.63	29.82 nW

VI. Conclusion

Various S/H circuits were discussed in this paper. It presents passive free op-amp S/H circuit with and without bootstrapping technique. The bootstrapping technique is the suitable method for low voltage operation. According to the simulation results that are shown in Table. 1. The differential passive free op-amp S/H circuit is the best candidate for low-frequency signals. It is noticed that all the S/H circuits' types have a closest value of SNDR. This means that for low-frequency signals, there is no significant effect of the presented S/H circuits on the SNDR value.

References

[1] S. A. Mahmoud, A. Bamakhramah, S. A. Al-Tunaiji, "Low noise Low Pass Filter for ECG Portable Detection Systems with Digitally Programmable Range," in Circuits, Systems, and Signal Processing (CSSP9478), published online: 20 Fab. 2013, doi: 10.1007/s00034-013-9564-9), vol. 32, no. 5, pp. 2029-2045, Aug. 31, 2013.

[2] S. A. Mahmoud, A. Bamakhramah, S. A. Al-Tunaiji, "Six Order Cascaded Power Line Notch Filter for ECG Detection Systems with Noise Shaping," in Circuits, Systems, and Signal Processing (CSSP9478), doi: 10.1007/s00034-014-9761-1, vol. 33, no. 8, pp. 2385-2400, Aug. 2014.

[3] S. A. Mahmoud, T. B. Nazzal, "Sample and Hold Circuits for Analog-to-Digital Converters," in UAE Graduate Students Research Conference, pp. 223-224, Mar. 2015.

[4] S. A. Mahmoud, H. A. Salem, H. M. Albalooshi "An 8-bit, 10KS/s, 1.87µW Successive Approximation Analog to Digital Converter in 0.25µm CMOS Technology for ECG Detection Systems," in Circuits, Systems, and Signal Processing, puplished online: doi: 10.1007/s00034-015-9973-z, vol. 34, no. 2, Feb. 2015.

[5] J. Craninckx, G. Plas, "A 65fJ/Conversion-Step 0-to-50MS/s 0-to-0.7mW 9b Charge-Sharing SAR ADC in 90nm Digital CMOS," IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 246-600, Feb. 2007.

[6] H. C. Hong, G. M. Lee, "A 65-fJ/Conversion-Step 0.9-V 200-KS/s Rail-to-Rail 8-bit Successive Approximation ADC," IEEE journal of Solid-State Circuits, vol. 42, no. 10, pp. 2161-2168, Oct. 2007.

[7] T. B. Cho, P. R. Gray, "A 10 b, 20 Msample/s, 35mW Pipeline A/D Converter," IEEE journal of Solid-State Circuits, vol. 30, no. 3, pp. 166-172, Mar. 1995.

[8] A. M. Abo, P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," IEEE journal of Solid-State Circuits, vol. 34, no. 5, pp. 599-606, May. 1999.

[9] C. C. Liu, S. J. Chang, G. Y. Huang, Y. Z. Lin, "A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure," IEEE journal of Solid-State Circuits, vol. 45, no. 4, pp. 731-740, Apr. 2010.