

# CMOS090 50A MOS VARACTORS

## N+POLY/NWELL MOS VARACTORS

Devices name:

- var\_sg\_nmos25

Developer:

Jean-Francois LARCHANCHE, July 2004

Maturity:

Preliminary data

### 1.MEASUREMENT AND PARAMETER EXTRACTION OF TYPICAL MODEL

They are preliminary models based on CMOS090 GP 50 ang measurements.

Parameter extraction was performed in the following conditions:

Test structure reference:

ZVMA rev A0 to ZVMM rev A0

Device Selection:

Lot: Q406EGE wafer 10

Characterization domain:

Vpoly form -3V to 3V, 0.1V step

High frequency measurements from 45 MHz to 50 GHz.

Extrapolation:

Interconnection resistance and capacitance values recalculated from Cmos065 back-end.

### 2.BEST/WORST CASE

Statistical and Best/Worst case simulations available

The criteria is the capacitance value. Best/Worst are constructed with DRM values for parasitic capacitance and mapping on one wafer at low frequency for mos capacitance statistical behav-

our. So statistical simulations concern mainly variations observed on serial capacitance and back-end variation extracted from DRM.

### 3.SIMULATION WITH TEMPERATURE

Not available

### 4.MODEL APPLICATION GUIDELINES

#### Layout & Model:

- T cell model
- The model takes into account:
  - \* Deep depletion or non thermo-dynamic equilibrium high-frequency model. A high frequency thermal-equilibrium capacitance versus voltage is under developpement
  - \* Parasitic capacitance (fringing, STI, metal interconnection). A voltage dependant fringing capacitance has been observed, influencing the depletion capacitance model precision. This work is under development. Today this effect is taken into account bias the substrate doping in min and max cases.
  - \* Parasitic inductance are included.
  - \* Serial resistance are voltage dependant.
- Serial capacitance is extracted from low frequency measurements

#### Model Call :

- Scalable varactor model
- Input parameters:
  - **c** : capacitance value in accumulation mode in F (from 20fF to 10pF)
  - or W** : N+poly fingers width in um (from 3 to 40)
  - **l** : N+poly fingers length in um (from 0.35 to 2)
  - **nbfp**: N+poly fingers number (from 1 to 50)

#### Frequency validity:

From DC to resonance frequency if resonance frequency is below 20 GHz.

## P+POLY/PWELL MOS VARACTORS

Devices name:

- var\_sg\_pmos25

Developer:

Jean-Francois LARCHANCHE, July 2004

Maturity:

Preliminary data

List of changes for current version:

2004/07: initial revision - tentative data

2005/04: first release - Preliminary data

2006/07: DK6.1 - No change

## **1.MEASUREMENT AND PARAMETER EXTRACTION OF TYPICAL MODEL**

They are preliminary models based on CMOS090 GP 50 ang measurements.

Parameter extraction was performed in the following conditions:

Test structure reference:

ZVPA rev A0 to ZVPM rev A0

Device Selection:

Lot: Q406EGE wafer 10

Characterization domain:

Vpoly from 3V to -3V, 0.1V step

High frequency measurements from 45 MHz to 50 GHz.

Extrapolation:

Interconnection resistance and capacitance values recalculated from Cmos065 back-end.

## **2.BEST/WORST CASE**

Statistical and Best/Worst case simulations available

The criteria is the capacitance value. Best/Worst are constructed with DRM values for parasitic capacitance and mapping on one wafer at low frequency for diode capacitance statistical behaviour. So statistical simulations concern mainly variations observed on serial capacitance and back-end variation extracted from DRM.

### 3.SIMULATION WITH TEMPERATURE

Not available/work on progress

### 4.MODEL APPLICATION GUIDELINES

#### Layout & Model:

- T cell model
- The model takes into account:
  - \* Deep depletion or non thermo-dynamic equilibrium high-frequency model. A high frequency thermal-equilibrium capacitance versus voltage is under developpement
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