# Design and simulation methodology for switch-cap circuits used in data converter applications

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# Design and Simulation Methodology for Switch-Cap Circuits Used in Data Converter Applications

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*Abstract*— **This paper provides a full methodological approach to designing and verifying differential sample and hold switched-capacitor circuits used in A/D converters. It provides a step-by-step process for translating system requirements such as signal-to-noise ratio (SNR) and sampling frequency into A/D requirements and subsequently into op-amp specifications. It also includes the design process of a switched-capacitor common mode feedback circuit (CMFB) to control the common mode output voltage. Furthermore, this paper provides practical methods for verifying the stability of the system. A design and simulation example for a differential sample and hold switched-capacitor circuit operating in a system requiring 5 MHz sampling frequency and a 6-bit A/D converter is provided. Mentor Graphics CAD tools were used in the design and simulations process using 180nm CMOS device models. This paper can be used as a resource for design engineers in the industry as well as universities teaching graduate level advanced electronics and data converter courses.**

***Keywords-component; sample and hold; A/D ; op-amp; switched-capacitor ; common mode feedback ; stability***

## I. INTRODUCTION

Sample and hold circuits are considered the core components of A/D converters [1]. Their main role is tracking an analog input and storing its value at sampling frequency instances for a specific time length until the A/D converter can complete the conversion of the input value [2]. Due to their critical role in proper and stable data conversion, care must be taken in the design of each of their components. The op-amp used in the circuit must be stable and capable of operating within system requirements. The common mode feedback circuit and the sample and hold circuit itself are switched-capacitor circuits. Due to their non-linear nature, they require special attention in their design and stability verification methods.

The paper is organized as follows. Section II discusses a general sample and hold circuit. Section III contains a design flowchart and explains how to translate system requirements into A/D specifications. Section IV explains the design of an open-loop amplifier capable of satisfying system requirements as well as DC and AC design parameters. Section V explains the common mode feedback design, whereas section VI shows the sample and hold system. Section VII explains in detail how to check the system's stability. To illustrate the design process, an example sample and hold circuit is designed to operate in a 6-bit pipeline A/D converter. The A/D converter will be used in a system requiring 37dB SNR and 5MHz sampling frequency. It has a maximum differential input of 1V peak to peak. Each section contains the corresponding design example. Simulation results are shown in section VIII.

This paper provides a detailed resource for design engineers and universities teaching graduate level advanced electronics courses. It guides engineers and students starting with system requirements in choosing and designing all components of a sample and hold circuit. It also provides two clear methods for checking the stability of the system in transient simulations.

## II. SAMPLE AND HOLD CIRCUIT

For any A/D system to work properly, a sample and hold circuit is likely used as the first stage. Fig. 1 below shows a block diagram of a switched-capacitor sample and hold circuit, including common mode feedback circuitry. During the sample stage ($\phi 1$), capacitor $C_{IN}$ will hold a charge equal to the product of its value and the input voltage. During the hold stage ($\phi 2$), the charge stored on $C_{IN}$ will be transferred to $C_F$ due to charge conservation. This causes the output to track the input with a closed-loop gain as shown in (1). The bias block provides bias currents and voltages for the op-amp, whereas the CMFB controls the common mode output voltage.

$$v_{o,differential} = \frac{C_{IN}}{C_F} v_{in,differential} \quad (1)$$

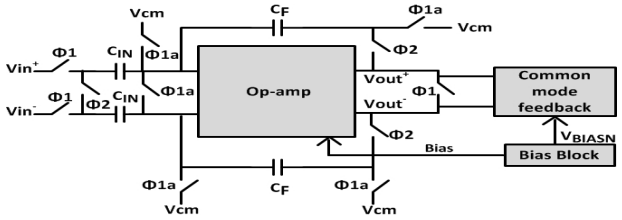


Figure 1: System block diagram

## III. DESIGN PROCEDURE

Design engineers are usually given system specifications in terms of SNR, sampling frequency and input voltage range. It is vital to know how to translate these requirements into a specific A/D topology and resolution. Subsequently op-amp specifications, like open-loop gain and unity-gain frequency are determined.

Fig. 2 below is a full design flowchart, showing a step-by-step guide of the design process. The first step is determining

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the number of bits, which is determined by the minimum SNR requirement of the system.

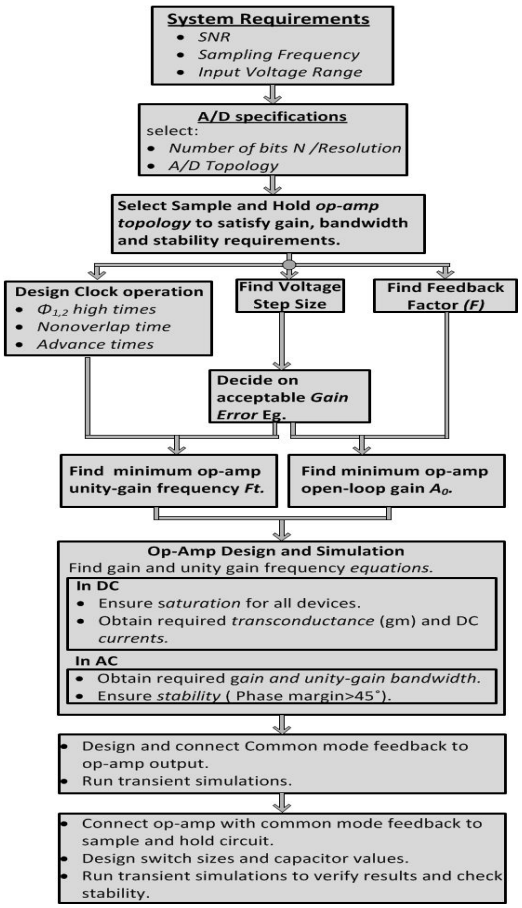


Figure 2: Design procedure flowchart

Equation (2) relates the system SNR requirement directly to the number of bits N [2]. Following that, an A/D topology is selected based on the required resolution and sampling frequency as shown in Fig. 3 [3]. For the example in this paper, a 6-bit pipeline A/D converter is used, because of its ability to satisfy system requirements.

$$SNR(dB)=6.02N+1.76dB \qquad (2)$$

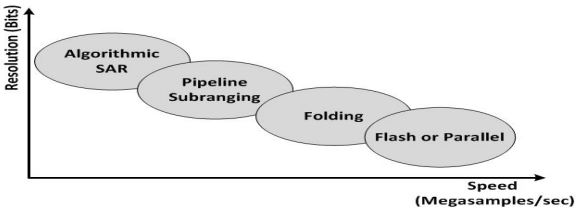


Figure 3: A/D topology selection

## IV. OP-AMP DESIGN

### A. Topologies

The first step in op-amp design is to select a topology that is capable of satisfying gain and bandwidth requirements. Commonly used topologies include the two-stage amplifier and the folded cascode amplifier. For the design example, the folded cascode shown in Fig. 4 was used. This is due to its ability to provide high gain while easily maintaining stability without the use of any additional compensation circuitry. It is also necessary at this point to select a current source to provide bias currents and voltages for both the op-amp and the CMFB. The wide-swing cascode current mirror in [4] was used in the example. It provides the bias voltages $v_{BIASP}$, bp2 and bn1 to the op-amp and therefore determines the currents passing through its branches. It also provides bias voltage $v_{BIASN}$ to the CMFB circuit to be discussed in Section V.

After selecting topologies and deriving gain and bandwidth equations for the selected circuits, a key step in the design is to translate the system and A/D requirements into minimum open-loop op-amp specifications. This must start with proper clocks operation.

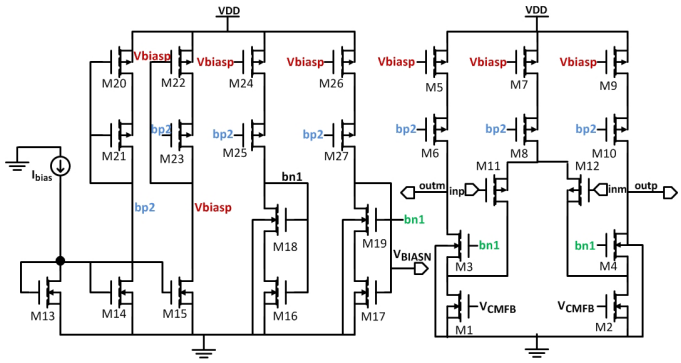


Figure 4: Folded Cascode op-amp with biasing

### B. Clocks Operation

There are three clocks operating the circuit: $\phi 1$, $\phi 1_A$ and $\phi 2$. $\phi 1$'s high time is the sampling (tracking) time, whereas $\phi 2$'s high time is the hold time. $\phi 1_A$ is an advanced $\phi 1$ clock and is used to minimize non-ideal charge sharing issues. The circuit operates in an entirely different way between these two stages. Therefore, it is the designer's job to make sure $\phi 1$ and $\phi 2$ never overlap. $\phi 1$ high time is calculated according to (3) below. Suitable non-overlap and advanced times are selected.

$$t_{\Phi 1\text{-high}} = \frac{t_{period}}{2} - t_{non\text{-}overlap} - t_{advanced\ time} - t_{rise\ and\ fall} \qquad (3)$$

### C. Open-loop amplifier specifications

After determining the sampling time, the least significant bit (LSB), the gain error (Eg) and the feedback factor (F) must be calculated. The LSB is calculated according to (4), where N is the number of bits and $V_{pp\text{-}differential}$ is the maximum differential input voltage. Following that, Eg must be defined as a fraction (1/x) of the LSB. The value selected for x depends on speed and accuracy requirements of the system. The next step is using (5) to calculate $\tau_{max}$ as shown in (6). Then, the minimum unity-gain bandwidth ($ft_{min}$) can be found using (7). It must be noted that the time (t) in (5) and (6) is the settling time of the sample stage only, and is considered to be 80% of $t_{\Phi 1\text{-high}}$ found in (3) (i.e. excluding 20% for slew time). $A_0$ is the open-loop op-amp gain.

Finally, using the right side of (5), and substituting F from (8), the minimum op-amp open-loop gain $A_o$ can be calculated. For the design example, a closed-loop gain of 2 is desired, and x in (5) is selected to be equal to 2. $t_{\Phi 1\text{-high}}$= 96.8nS, LSB= 15.625mV and F=0.3125. $A_{o,min}$ and $ft_{min}$ were then calculated to be 46.2dB and 19.94 MHz respectively.

$$LSB=\frac{V_{PP\text{-dfferential}}}{2^N} \quad (4)$$

$$e^{-\frac{0.8t_{\Phi 1-high}}{\tau}} \leq Eg=\frac{1}{A_0F}=\frac{1}{x}LSB \quad (5)$$

$$\tau_{max}=\frac{-0.8\ t_{\Phi 1-high}}{\ln\left(\frac{1}{x}lsb\right)} \quad (6)$$

$$ft_{min}=\frac{1}{2\pi\tau_{max}} \text{ x Closed-loop gain} \quad (7)$$

$$F=\frac{Cf}{Cf+ Cs+ Cparasitic} \quad (8)$$

### *D. Design and Simulations*

Now that the op-amp specifications are set, the design process must start at DC. The FETS are sized to ensure all devices are operating in saturation, and obtain the required transconductances and DC currents. At first, devices M5-M10 in Fig. 4 are sized such that their ratios to the corresponding FETS in the current mirror can set the current passing through each branch. The rest of the FETS are sized afterwards. Following that, AC simulations are performed, and the design is tweaked to obtain the required gain and bandwidth. It is important to verify that the open-loop system is stable by verifying that the phase margin is above $45^o$ at the unity-gain frequency. In order to obtain a valid AC simulation, the CMFB must not be connected at this stage of the design process for the reasons explained in section VII. To properly bias the op-amp without including the CMFB, the gates of M1 and M2 in Fig. 4 should be connected directly to the bias voltage $V_{BIASN}$. Example AC simulations are shown in section VIII.

## V. COMMON MODE FEEDBACK DESIGN

The op-amp and the sample and hold design will affect the differential signal, but will not set common mode voltages. Therefore, it is necessary to add additional common mode feedback circuitry to control the common mode output voltage at a required value, usually halfway between the power supplies [2]. An example of a switched-capacitor CMFB circuit is shown in Fig. 5. The switched capacitor Cs is switched between fixed bias voltages $V_{CMREF}$ and $V_{BIASN}$ during $\phi 1$ and being in parallel with the non-switched capacitor Cc during $\phi 2$. This allows Cs to determine the DC voltage across Cc by altering the control voltage $V_{CMFB}$ to keep the common mode output voltage constant [2]. The bias voltage $V_{CMREF}$ is a low impedance reference voltage that sets the value of the common mode output voltage. $V_{BIASN}$ is a fixed bias voltage supplied by the bias block. The switched capacitor along with the switches on its sides will operate as an equivalent resistance determined by (9), where fs is the sampling frequency. As a result, the equivalent circuit shown in Fig. 6 will effectively act as an RC circuit. The common mode feedback may possibly control the dominant pole of the system. Therefore, care must be taken when selecting capacitor values. The 3-dB bandwidth of the common mode feedback is given in (10), where $f_S$ is the sampling frequency.

$$R_{equivalent}=\frac{1}{fsCs} \quad (9)$$

$$f_{3\text{-dB}}=\frac{fs\ Cs}{2\pi Cc} \quad (10)$$

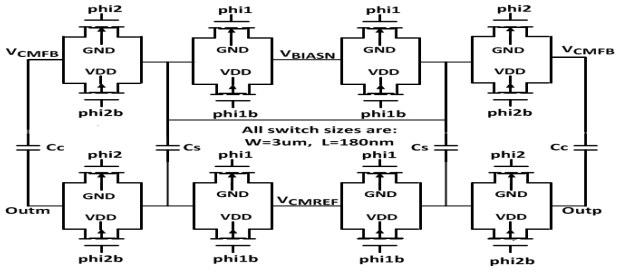


Figure 5: Common mode feedback circuit

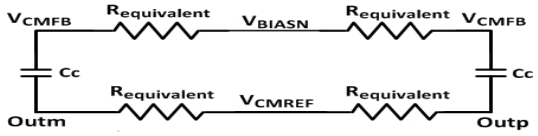


Figure 6: Common mode feedback equivalent circuit

## VI. FINAL SAMPLE AND HOLD CIRCUIT

The current mirror, op-amp and common mode feedback should now be inserted into the sample and hold configuration. Fig. 7 below is the final sample and hold schematic used in the design example. The Capacitors' values must be selected to satisfy (1).

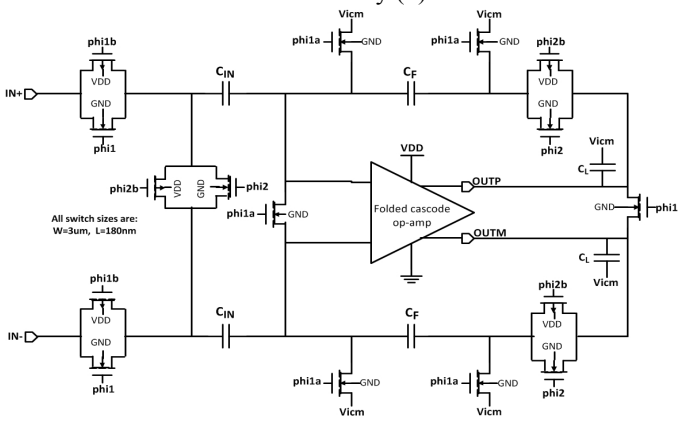


Figure 7: Sample and Hold schematic

## VII. SYSTEM STABILTY

Stability describes the ability of a system to withstand variations in the conditions under which the circuit is operating [5]. Stability is typically checked using AC simulations [6]. However, such methods cannot provide correct stability information about sample and hold circuits because AC simulations do not account for the switching operation in the switched-capacitor circuits. Moreover, the AC simulation stability check used in [6] will face an issue with the capacitors in the feedback loop, since these capacitors will block the DC signal. To verify the stability of the switched-capacitor sample and hold circuit, two methods are presented

using transient simulations. The first method is applying a step voltage to the power supply (VDD). The second method is applying a pulse step current at the input of the op-amp. In both methods, the system is considered stable if the output responds smoothly to the changes in the operating conditions, i.e., without overshooting and ringing. In order to differentiate between the system's response to variations in the input and its response to the applied changes, the inputs are replaced with DC voltage sources. Section VIII includes simulations for the first method verifying the stability of the design example.

## VIII. SIMULATIONS

### A. Open-Loop Simulations

Fig. 8 shows the differential input connected directly to the op-amp as should be done for open-loop simulations. Fig. 9 shows the AC simulations of the open-loop op-amp's output magnitude and phase. The gain and unity-gain frequency are 53.59dB and 68.24MHz respectively. The phase margin is 48.21$^{o}$ indicating the stability of the open-loop op-amp.

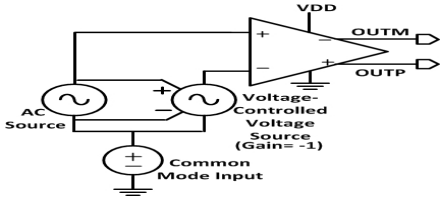


Figure 8: Open-loop Simulation Schematic

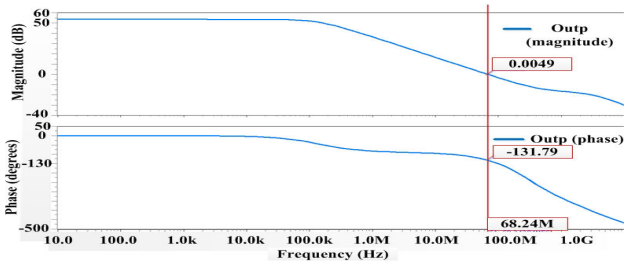


Figure 9: AC simulation of open-loop op-amp output magnitude and phase

### B. Closed-loop Simulations

Fig. 10 shows transient simulations for the sample and hold differential and single ended outputs. The circuit is operating at 5MHz and provides a closed-loop gain of 2. Fig. 11 graphically represents both stability methods on the sample and hold schematic. An arrow on the output waveform indicates where the stability verification methods should be applied and observed. Fig. 12 shows the effect of the VDD step on the output. Stable and less stable responses are shown.

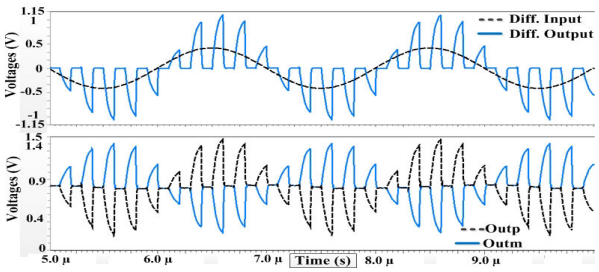


Figure 10: Differential input and output superimposed (top), single ended outputs superimposed (bottom)

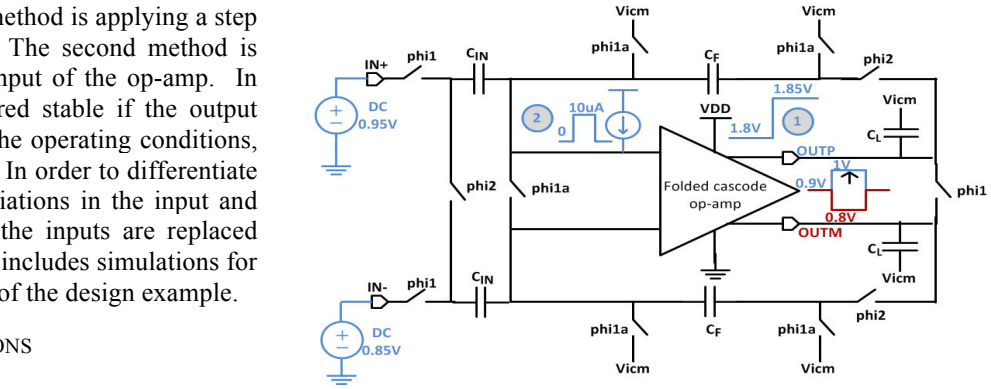


Figure 11: Stability verification methods

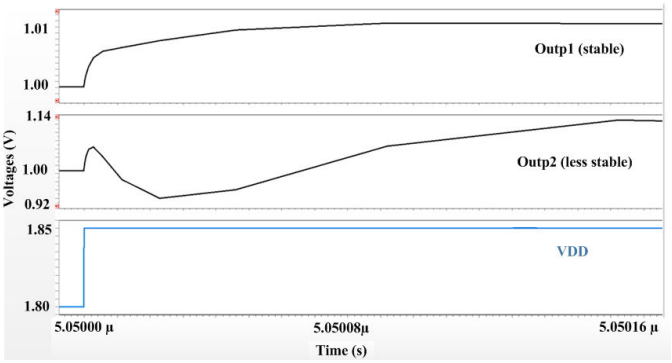


Figure 12: VDD step (bottom), stable (top) and less stable responses (middle)

## IX. CONCLUSIONS

In this paper, the design process of a sample and hold circuit was fully presented. A/D topology selection and translation of system requirements into op-amp specification were discussed. In addition, the design of the op-amp, the common mode feedback and the sample and hold circuit were detailed. Furthermore, two methods for checking the stability of the closed-loop system using transient simulations have been implemented. Finally, a design example including simulations has been provided. This paper provides a guide for design engineers and graduate students on how to approach non-linear switched-capacitor circuit design.

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