

11-1-1990

# The design, fabrication, and test of a CMOS operational amplifier

Edward P. Sayre

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The Design, Fabrication, and Test  
of a  
**CMOS Operational Amplifier**  
by

**Edward P. Sayre III**

A Thesis submitted  
in  
Partial Fulfillment  
of the  
Requirements for the Degree of

MASTERS OF SCIENCE  
in  
Electrical Engineering

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Rochester Institute of Technology  
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November, 1990

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## Chapter 1 Introduction

The topic of this thesis is the design, fabrication, and testing of a CMOS operational Amplifier. This Operational Amplifier was first realized as a class design project for Advanced Analog IC design. Specifications for the device performance were determined by Dr. Fuller and Edward Sayre to enable the op-amp to be incorporated into a larger more complex design. The specifications of the operational amplifier were made to enable design integration into an amplifier which would operate in the audio frequency range. The main constraints placed on the design of the op-amp were low power consumption and a relatively moderate gain.

The following four chapters will discuss the design of the operational amplifier, (chapters 2 and 3), the fabrication of the op-amp, (chapter 4), and the testing of the op-amp, (chapter 5). Chapter 2 will deal with the initial design approach deriving pertinent equations for the different modes of operation of the individual stages of the op-amp. The design approach of the operational amplifier divides the op-amp into its components enabling the circuit derivation to be easily simplified into a manageable solution. The equations derived in chapter 2 for the different modes of operation of each stage, differential pair and output stage, will be presented in both small signal parameters as well as process and device parameters. Large and small signal analysis will be performed on the op-amp to insure compliance with the specifications also to determine the robustness of the design.

The frequency analysis of the operational amplifier will prove that the system can be represented as a first order system. The parasitic capacitors of the differential and output stages dictate the frequency response of the devices without any compensation capacitances. Chapter 2 will demonstrate that for a compensated system the singularities introduced by the parasitic capacitors can be ignored enabling us to model it as a first order system. The derivation of each stage's frequency transfer function will be able to be utilized to determine the full transfer function of the operational amplifier, in chapter 3, since it is a linear system.

Chapter 3 will integrate the individual sections of the op-amp, discussed in chapter 2, into the whole CMOS operational amplifier. The investigations of the various modes of operation derived in chapter 2 for the particular stages of the amplifier are completed to a final system level which will describe the operation and performance of the op-amp system. A compensation scheme will be implemented to achieve the desired frequency response for the system. The frequency response of the uncompensated operational amplifier will be compared to the compensated system. Thus demonstrating the need of compensation.

In Chapter 3 the actual device sizes will be determined from the performance specifications along with the process parameters. These values are substituted into the equations derived in chapter 2 and previously in chapter 3. Simulation's of the op-amp are performed using the S.P.I.C.E simulation tool. Both the large signal, DC, and small signal, AC, parameters will be evaluated. The models used in the simulation are either extracted from process

simulations, expected process data, or researched values. The simulations of the large signal behavior of the op-amp will demonstrate the ability of the design to meet the DC performance criteria. The AC data will show that the operational amplifier can be modeled as a first order system over the frequencies of operation. The frequency response of the the op-amp will be evaluated to determine the robustness of the system for closed loop applications from the open loop characteristics.

The layout of the CMOS operational amplifier is the final section of chapter 3. The CMOS op-amp is layed out for a Pwell CMOS process with both the VAX resident Integrated Circuit Editor, I.C.E., and with Chipgraph, on the Apollo workstations, written by Mentor Graphics. The operational amplifier is to be layed out as a whole circuit except for the compensation capacitor due to area constraints of the device die size. The individual stages making up the op-amp will also be layed out to allow the investigation into effects or design particularities that my be isolated to one of the stages.

Chapter 4 will discuss the Pwell CMOS fabrication process chosen to construct the CMOS operational amplifier. The CMOS process developed at Rochester Institute of Technology was modeled after the Berkeley 3 $\mu$ m Pwell CMOS process developed at the University of California, Berkeley. The RIT process modifies the Berkeley process to suit the manufacturing facilities of the Microelectronic Engineering fabrication laboratory. A description of the pertinent processing steps along with the processing difficulties and modifications experienced are include in chapter 4.

The impact of any processing errors or problems on the performance of the devices created is important in the development of a process and are addressed in this chapter. Finally the end process results of the first complete polysilicon gate Pwell CMOS process will be summarized.

Chapter 5 will discuss the testability of the CMOS operational amplifier and the integration of the op-amp into some typical elementary applications. The testability of any analog circuit encompasses two regions of operation and the performance in both is crucial to the determination of the functionality of the device. Chapter 5 will discuss the methods of test for both the DC and AC behavior of the op-amp. The testability approach of the operational amplifier will be to first test the DC behavior then the AC region of operation. This scheme reduces the time for testing thus increasing the throughput.

The second section of chapter 5 will concern itself with the integration of the CMOS operational amplifier into some typical amplifier designs. The particular circuits will be used to demonstrate the ability for the op-amp to be used in a closed loop system and thus can be used as a final method of test for the functionality of a device. The circuits that will be designed are a unity gain amplifier, and amplifier with gain of 100, an integrator amplifier, and a differentiator amplifier. All of these are commonly used in signal processing applications thus testing the operational amplifier in actual applications.

## Chapter 2 Design Derivation

### 2.0 Introduction

This chapter will discuss the method of design and division of the CMOS operational amplifier into its components or stages. The stages of the op-amp are the differential amplifier, the output stage and the bias stage. A significant amount of the behavior of an op-amp is introduced by the differential amplifier stage, and so the various regions of operation of the dif-amp will be derived. The frequency responses of both the dif-amp and the output stage will be derived which will prove the CMOS operational amplifier can be modeled as a first order linear system. The circuit configuration of the bias stage of the op-amp will be derived to yield the appropriate voltage and current levels. This chapter will concern itself with the derivation of the components and their behavior as individual circuits so the complete operational amplifier be evaluated in the following chapter.

### 2.1 Differential Amplifier

The differential Amplifier is the input device of the CMOS operational Amplifier. It has two inputs which are used for the differential input pair and a single output referred to as a single sided output. Ideally the differential amplifier will only amplify the difference between the inputs and not the common component of the

two signals. The two types of gain of the differential amplifier are the Common mode and Differential mode voltage gains. Ideally the common mode gain is zero and the differential mode gain is infinite.

### 2.1.1 Large Signal Analysis

The performance parameters of the operational Amplifier are directly related to those of the differential amplifier. Some of the criteria for performance of the dif-amp are the Frequency response for both the differential and common modes of operation, Common Mode Rejection Ratio (CMRR), Common Mode Range (CMR), Input Offset Voltage, and the Output Voltage Range. These are easily upgraded to the performance criteria of the op-amp since the following stage after the dif-amp is the output gain stage. The CMRR is a ratio between the differential gain and the common mode gain, shown in equation 1.

$$\text{CMRR} = \frac{A_{vdm}}{A_{vcm}} \quad \text{eq. (2.1)}$$

The CMR is the range over which the inputs can vary in the common mode and output the proper differential gain. The ideal common mode range is found to be the full swing of the input voltage which is typically close to the power supply voltages. The input offset voltage is simply the voltage at the output, of either the differential amplifier or op-amp, when both inputs are grounded to zero (0) volts. The cause of a divergence of the output from zero is due to the

mismatches in the differential pair, further explanation of this phenomena is discussed later in this chapter. Ideally the input offset voltage, of the op-amp and dif-amp, is zero (0) since ideally the two legs of the differential pair are identical but, typically the offset is in the millivolt range.

The general differential amplifier structure consists of a current source, a differential pair input and a current mirror. A schematic of this structure can be seen in figure 2.1 below.

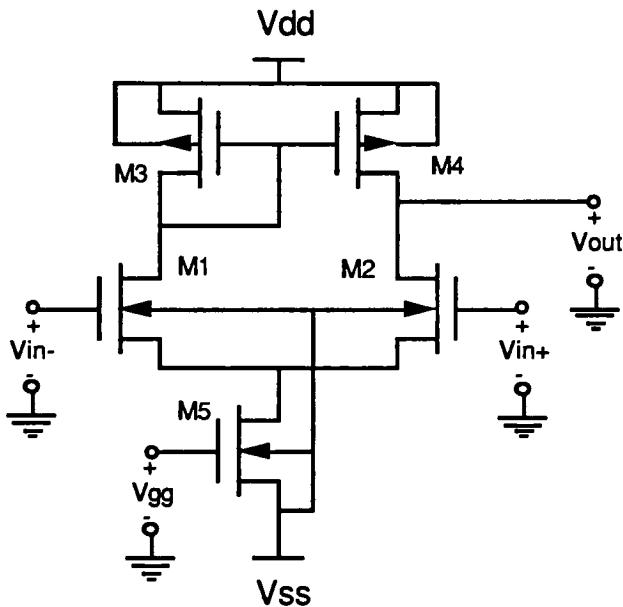


Figure 2.1 (Dif-amp with N channel Input)

The CMOS differential amplifier shown above consists of two N channel or NMOS input transistors,  $M_1$  and  $M_2$ , a P channel or PMOS, current mirror,  $M_3$  and  $M_4$ , and an NMOS current source  $M_5$ . The current source will supply a DC bias current  $I_{ss}$  required by each side of the differential amplifier and is applied at the sources of the N

channel input devices. The drains of M1 and M2 are connected to M3 and M4, respectively, which make up the current mirror. This current mirror is the source of many of the non-ideal behavior of the dif-amp structure. The single sided output is at the node between transistors M2 and M4. Figure 2.1 is used for the preliminary expressions and circuit derivations of the large and small signal models.

For this first order large signal evaluation of the behavior of the CMOS differential Amplifier we will assume the the branches of the dif-amp are symmetric. From this assumption it can be seen that the drain to source current through M3 will be mirrored in M4. The current in M3 is controlled by the drain current through M1 which is related to the input voltage of M1. The current through M4,  $i_{ds4}$ , will also be the same as  $i_{ds3}=i_{ds1}$ . If  $V_{in+}=V_{in-}$  then  $V_{gs1}=V_{gs2}$  and the current  $i_{ds2}$  will be equivalent to the current through M1,  $i_{ds1}$ . This condition is strictly in the common mode range of operation of the dif-amp and thus for the whole operational amplifier.

Now, if the gate voltages applied to M1 and M2 are not equivalent the large signal behavior changes for differing conditions. If the gate voltage,  $V_{gs1}$ , on M1 increases and becomes larger than  $V_{gs2}$  then the current through M1,  $i_{ds1}$ , will be proportionally larger than the current  $i_{ds2}$ , through M2. The sum of the current through M1 and M2 are equivalent to  $I_{ss}$  by Kirchhoff's current law. Since  $i_{ds1}$  increases so must  $i_{ds3}$  but this current is matched in  $i_{ds4}$  but  $i_{ds2}$  decreases due to the reduced gate voltage on M2. By Kirchhoff's current law, the current at any node sums to zero, the output shows

the difference in the current between  $i_{ds2}$  and  $i_{ds4}$ . This current equations (2.2) and (3) are written at the drain of M5;

$$i_{ds2} = -i_{ds1} + I_{ss} \quad \text{eq. (2.2)}$$

$$i_{ds4} = i_{ds3} = i_{ds1} \quad \text{eq. (2.3)}$$

Therefore the current flowing out of the output is;

$$i_{out} = 2i_{ds1} - I_{ss} \quad \text{eq. (2.4)}$$

For the case where  $V_{gs2}$  is larger than the gate voltage  $V_{gs1}$  the current will be in the opposite direction at the output node. The magnitude of the current will be that shown in equation (4). The value for  $i_{out}$  under this condition will yield a negative value which is due to the nomenclature of the current directions.

### 2.1.2 Small Signal Analysis

The small signal model that is used to calculate the small signal behavior of the dif-amp is shown in figure 2.2. The complete small signal model shown below is simplified for the first order analysis of this section. Figure 2.2 does not include all of the parasitics and small signal parameters that would greatly complicate the hand calculations of this section. The purpose of a simplified small signal model is to show the gross behavior of the

differential amplifier circuit. The dominant parameters are shown, in figure 2.2, to be the channel conductances,  $g_{ds}$ , and transconductances,  $g_m$ .

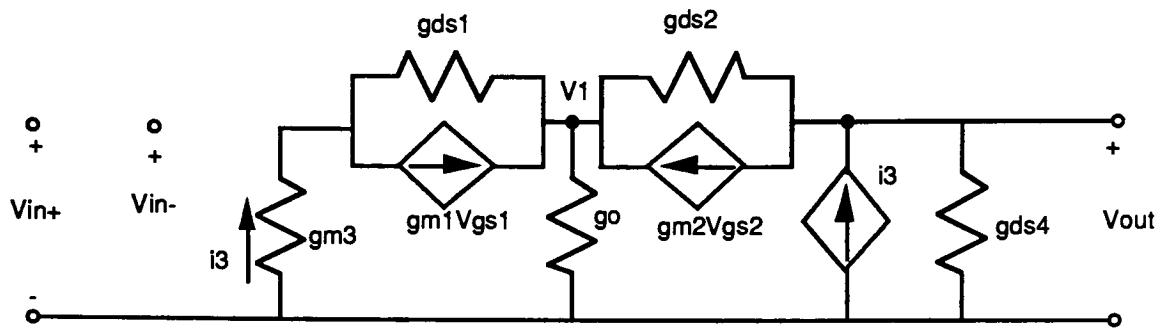


Figure 2.2 (Differential Amplifier Small Signal Model)

The small signal parameters are related to the device parameters in equations 2.5 through 2.8. The assumption which must be made is all of the transistor devices are in the saturated or non-linear region of operation.

$$g_{m1} = g_{m2} = \frac{\partial i_{ds}}{\partial v_{gs}} = \left[ 2K' \frac{W}{L} |i_{ds}| \right]^{\frac{1}{2}} \quad \text{eq. (2.5)}$$

$$g_{ds1} = g_{ds2} = \frac{\partial i_{ds}}{\partial v_{ds}} = i_{ds}(\lambda) \quad \text{eq. (2.6)}$$

$$g_{m3} = g_{m4} = \frac{\partial i_{ds}}{\partial v_{gs}} = \left[ 2K' \frac{W}{L} |i_{ds}| \right]^{\frac{1}{2}} \quad \text{eq. (2.7)}$$

$$g_{ds3} = g_{ds4} = \frac{\partial i_{ds}}{\partial v_{ds}} = i_{ds}(\lambda) \quad \text{eq. (2.8)}$$

At this point we must break up the derivation of the small signal into two sections, the differential mode of operation, and the other section for the common mode region of operation.

### 2.1.3 Differential Mode

The differential mode of operation for the differential amplifier assumes that the two legs of the dif-amp are symmetric. This assumption ignores the major components which can contribute to the common mode gain. The differential mode gain of the differential amplifier will be calculated as;

$$A_{dv} = \frac{V_{out}}{V_{id}} \quad \text{eq. (2.9)}$$

where  $V_{id}$  is defined as the difference between the input voltages,

$$V_{id} = V_{in1} - V_{in2} \quad \text{eq. (2.10)}$$

We will define that the inputs are equal and opposite in magnitude which will lead us to the derivation of a purely differential mode gain. This definition leads to the determination that the current,  $i_{d2}$ , through M2 is equal and opposite to the current,  $i_{d1}$ , through M1. Now, if we sum the currents into the current source conductance  $g_o$ , it can be seen that the a virtual ground occurs at V1, refer to figure 2.2. The current through  $g_o$  has a net magnitude of zero thus

allowing us to let the transconductance approach infinity or the resistance approach a short circuit. The simplified small signal differential model is shown in figure 2.3.

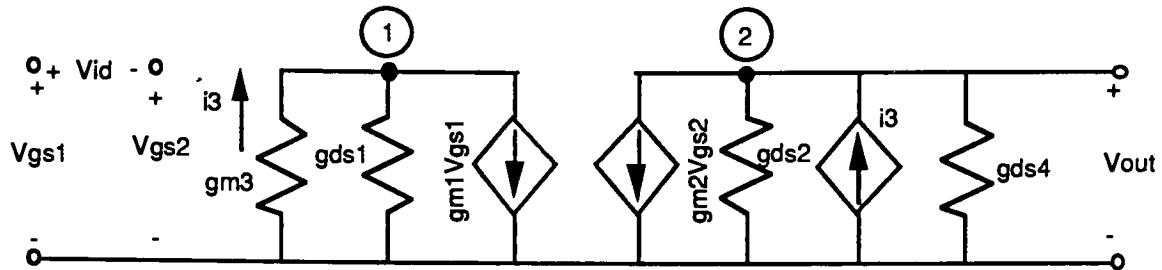


Figure 2.3 ( Simplified Differential mode model )

From figure 2.3 we can derive the first order equation for the differential mode voltage gain,  $A_{dv}$ . Summing the currents at nodes 1 and 2 gives;

$$V_1(g_{m3} + g_{ds1}) = g_{m1} V_{gs1} \quad \text{eq. (2.11)}$$

$$V_{out}(g_{ds2} + g_{ds4}) + V_1 g_{m3} = g_{m2} V_{gs2} \quad \text{eq. (2.12)}$$

Solving equation 2.11 for  $V_1$  and substituting into equation 2.12 results in equation 2.13 and is further simplified to equation 2.14.

$$V_{out}(g_{ds2} + g_{ds4}) + \left( \frac{g_{m1} g_{m3}}{(g_{m3} + g_{ds1})} \right) V_{gs1} = g_{m2} V_{gs2} \quad \text{eq. (2.13)}$$

Now, simplifying

$$V_{out} = \frac{\left( \frac{g_{m1}g_{m3}}{(g_{m3} + g_{ds1})} \right) V_{gs1} + g_{m2}V_{gs2}}{(g_{ds2} + g_{ds4})} \quad \text{eq. (2.14)}$$

We previously defined that both legs of the differential pair be symmetric thus allowing us to equate the conductances of like devices. Since the input pair are both N channel and symmetric;

$$g_{ds2} = g_{ds1} = g_{dsn} \quad \text{eq. (2.15)}$$

and,

$$g_{m2} = g_{m1} = g_{mn} . \quad \text{eq. (2.16)}$$

Similarly, the P channel devices in the current mirror are again the same size, thus we can also define;

$$g_{ds3} = g_{ds4} = g_{dsp} \quad \text{eq. (2.17)}$$

$$g_{m3} = g_{m4} = g_{mp} \quad \text{eq. (2.18)}$$

Substituting these definitions, eq. 2.15 - 2.18, into equation 2.14 and simplifying gives eq. 2.19

$$V_{out} = \frac{\left( \frac{g_{mn}g_{mp}}{(g_{mp} + g_{dsn})} \right) V_{gs1} + g_{mn}V_{gs2}}{(g_{dsn} + g_{dsp})} \quad \text{eq. (2.19)}$$

To further reduce equation 2.19 the assumption that  $g_{mp} \gg g_{dsn}$ , which it typically is, can be introduced. From the simplified small signal differential pair model, figure 2.3, it can be defined that  $V_{in1} = V_{gs1}$  and  $V_{in2} = V_{gs2}$  and by the definition of the differential input  $V_{id} = V_{in1} - V_{in2}$ . Now if we substitute these identities and assumptions into equation 2.19 it will yield the first order small signal differential voltage gain shown in equation 2.20.

$$A_{vd} = \frac{V_{out}}{V_{id}} = \frac{g_{mn}}{(g_{dsn} + g_{dsp})} \quad \text{eq. (2.20)}$$

As can be seen the differential gain is written in terms of conductances but for design purposes we can write the gain in terms of device sizes and process parameters. Substituting equations 2.5 through 2.8 appropriately equation 2.20 can be rewritten to get a relation between the device parameters and the differential gain.

$$A_{vd} = \frac{2}{(\lambda_p + \lambda_n)} \left[ \frac{K'_n W_n}{I_{ss} L_n} \right]^{\frac{1}{2}} \quad \text{eq. (2.21)}$$

where,  $K'_n = \frac{\mu_0 \epsilon_0 \epsilon_{rox}}{t_{ox}}$

## 2.1.4 Common Mode

The differential amplifier is ideally intended to amplify the difference between the signals applied at the inputs. The output of the dif-amp is the input difference amplified by some gain. For

every differential signal there is a common mode component, ie. the carrier signal of an audio signal is in phase for each of the differential inputs but the information within the signal is not. For the ideal differential amplifier the common mode gain is zero and the differential gain is very large or infinite. The common mode operation of the ideal dif-amp has equal current flowing through each leg of the dif-amp for the entire input range. Thus, the output will not change which allows us to state that the common mode gain is ideally zero.

The ideal case can only be realized for an ideal device, realistically the common mode gain is not zero but has a small non zero value. The non-ideal behavior is due to the manufacturing induced asymmetries between the two legs of the dif-amp. These are seen as geometry mismatches of the input devices, channel length modulation, threshold voltage offsets, and geometric mismatches in the current mirror. The geometric mismatches of the current mirror and input pair are not as prominent for devices with lengths  $10\mu\text{m}$  and larger. This is the case for the differential amplifier section of the CMOS operational amplifier. The two other nonuniformities, channel length modulation ( $\lambda$ ), and threshold voltage offset  $\Delta V_t$  can be predicted by the actual measurement and statistical analysis of these parameters. Both parameters are extremely dependant on the process and layout of the circuit. To accurately predict the effects of these parameter values would be beyond the scope of a first order approximation, except to say that the threshold voltage will effect the common mode gain with the

most impact since it has the highest variability across a single wafer.

The small signal model of the common mode gain can still be attained in spite of the lack of parameter extraction. The small signal model for the common mode is identical to the differential mode case except it can not exclude the conductance of the current source  $g_o$ . The common mode small signal model can be seen below in figure 2.4

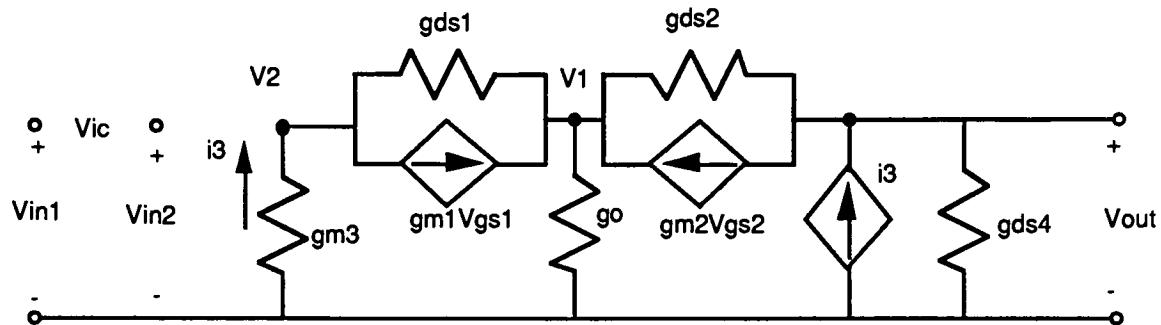


Figure 2.4 (Common Mode small signal model)

By nodal analysis at  $V_1$ ,  $V_2$ , and  $V_{out}$  three simultaneous equations can be written.

$$V_1g_{ds1} - V_2(g_{ds1} + g_{m3}) = V_{gs1}g_{m1} \quad \text{eq. (2.22)}$$

$$V_1(g_{ds1} + g_{ds2} + g_o) - V_2g_{ds1} = V_{gs1}g_{m1} + V_{gs2}g_{m2} + V_{out}g_{ds2} \quad \text{eq. (2.23)}$$

$$V_1g_{ds2} - V_2g_{m3} = V_{gs2}g_{m2} + V_{out}(g_{ds4} + g_{ds2}) \quad \text{eq.(2.24)}$$

Since the devices of the differential amplifier are "symmetric" the N-type devices, M1 and M2 will have parameters;

$$g_{m1} = g_{m2} = g_{mn} \quad \text{eq. (2.25)}$$

$$g_{ds1} = g_{ds2} = g_{dsn} \quad \text{eq. (2.26)}$$

And similarly for the P-type devices;

$$g_{m3} = g_{mp} \quad \text{eq. (2.27)}$$

$$g_{ds4} = g_{dsp} \quad \text{eq. (2.28)}$$

Also substituting for the voltage  $V_1$  in figure 2.4 from the DC circuit in figure 2.1.

$$V_{gs1} = V_{in1} - V_1 \quad \text{eq. (2.29)}$$

$$V_{gs2} = V_{in2} - V_1 \quad \text{eq. (2.30)}$$

Substituting the simplifications from equation 2.25 through 2.30 into equations 2.22, 2.23, and 2.24 yields equations 2.31, 2.32, and 2.33.

$$V_1(g_{dsn} + g_{mn}) - V_2(g_{dsn} + g_{mp}) = V_{in1}g_{mn} \quad \text{eq. (2.31)}$$

$$V_1(2g_{dsn} + 2g_{dsn} + g_o) - V_2g_{dsn} = (V_{in1} + V_{in2})g_{mn} + V_{out}g_{dsn} \quad \text{eq. (2.32)}$$

$$V_1g_{dsn} - V_2g_{mp} = V_{in2}g_{mn} + V_{out}(g_{dsp} + g_{dsn}) \quad \text{eq. (2.33)}$$

Solving equations 2.31-2.34 for an expression relating  $V_{out}$  to the input voltages,  $V_{in1}$  and  $V_{in2}$ , gives:

$$V_{out} = \frac{g_{mn}g_{mp}}{D} [2(g_{dsn}+g_{mn})(V_{in1}-V_{in2}) + g_o[V_{in1} - \left(\frac{g_{dsn}}{g_{mn}} + 1\right)V_{in2}]] \quad \text{eq.(2.35)}$$

where;

$$D = (g_{dsn} + g_{mn})[g_{dsp}g_{dsn} + 2g_{mp}(g_{dsp} + g_{dsn})] + g_o(g_{dsn} + g_{mp})(g_{dsp} + g_{dsn})$$

The general expression for  $V_{out}$  in terms of the conductances and input voltages can be simplified for the common mode by setting both inputs  $V_{in1}$  and  $V_{in2}$  to be equivalent. Thus reducing equation 2.35 to equation 2.36

$$V_{out} = \frac{-g_{mn}g_{dsn}g_o}{D} V_{inc} \quad \text{eq. (2.36)}$$

Where  $V_{inc}$  is defined as;

$$V_{inc} = \frac{V_{in1} + V_{in2}}{2} \quad \text{eq. (2.36a)}$$

Which can be simplified even further by the assumption of  $g_{mn}, g_{mp} \gg g_o, g_{dsp}$  and  $g_{dsn}$ .

$$A_{v,cm} = \frac{-g_o g_{dsn}}{2g_{mp}(g_{dsp} + g_{dsn})} \quad \text{eq. (2.37)}$$

If we relate the common mode voltage gain equation to the device process parameters defined in equations 2.5, 2.6, 2.7, and 2.8. The result is equation 2.38

$$A_{v,cm} = \frac{-\lambda_p \lambda_n}{(\lambda_p + \lambda_n)} \left( \frac{I_{ss} L_p}{K' p W_p} \right)^{\frac{1}{2}} \quad \text{eq. (2.38)}$$

Typically the common mode voltage gain is small, close to zero, which can be demonstrated by equation 2.38. Since the product of the  $\lambda$ 's is much less than one and then divided by a relatively large number, the sum of the channel length modulations, the result will be small. The effect of the second term does not contribute significantly to the magnitude of the gain. This supports the ideal case where the common mode voltage gain is assumed to be neglectable or zero.

### 2.1.5 Frequency Response

The Frequency of the Operational Amplifier can be determined by calculating the product of the frequency response of each stage of the op-amp. Since the op-amp is modeled as a linear system this statement will hold its validity. The dominant and secondary poles of the op-amp along with a method of frequency compensation needed can be determined during this section. The capacitive components of a MOS device which determine the frequency response are the parasitic capacitors between the gate and the source, the drain and bulk, and the bulk and source and drain regions.

If the parasitics of the MOSFET small signal model are included into the model of the differential amplifier including any compensation capacitance on the output, a relation for the frequency response as a function of the device parameters can be determined. The model with parasitic capacitors can be seen in figure 2.5

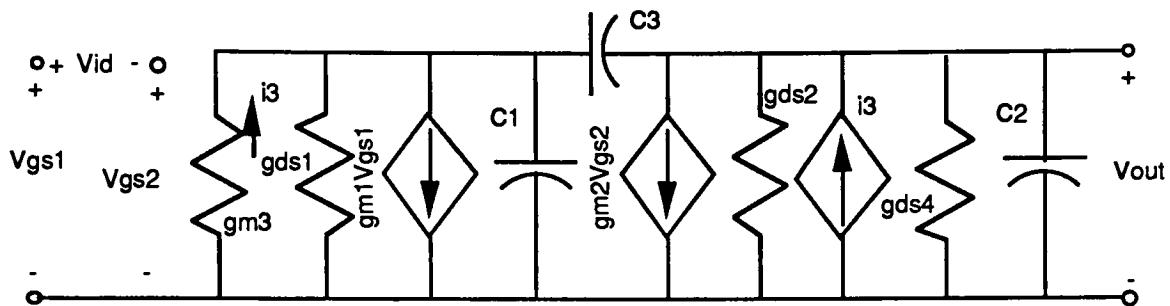


Figure 2.5 (dif-amp small signal model with parasitic capacitors)

Capacitor C1 consists of  $C_{gd1}$ ,  $C_{gb1}$ ,  $C_{gs1}$ ,  $C_{gb3}$ ,  $C_{gs4}$ ,  $C_{bd1}$ ,  $C_{bd3}$ ,  $C_{gs3}$  and  $C_{gs4}$ , capacitor C2 consists of  $C_{bd2}$ ,  $C_{bd4}$ ,  $C_{gd2}$ ,  $C_{gb2}$ ,  $C_{gs2}$ ,  $C_{bd2}$  and the compensation capacitor  $C_c$  and lastly C3 is  $C_{gd4}$ . The load capacitor includes the parasitic capacitances of the input of the next stage and the compensation capacitance seen by the differential amplifier output. Interconnect capacitance of the layout are not considered in this derivation. Also in order to simplify this derivation we will allow capacitor C3 to be ignored since it is of a relatively small magnitude. The voltage transfer function of the differential amplifier is written as;

$$V_{out}(S) \approx \frac{g_{mn}}{g_{dsn} + g_{dsp}} \left[ \frac{g_{mp}}{SC1 + g_{mp} + g_{dsn}} V_{gs1}(S) - V_{gs2}(S) \right] \frac{\omega_2}{(s + \omega_2)} \quad \text{eq. (2.39)}$$

$$\text{where, } \omega_2 = \frac{g_{dsn} + g_{dsp}}{C2} \quad \text{eq. (2.40)}$$

Equation 39 can be further simplified by the determination of the locations of the singularities of the function, specifically the poles. If we assume that the pole introduced from C1 is further from the Y axis in the s-plane than the pole from C2 or more simply;

$$\frac{g_{mp}}{C1} \gg \frac{g_{dsn} + g_{dsp}}{C2} \quad \text{eq. (2.41)}$$

Then revising the frequency response of the differential amplifier;

$$V_{out}(S) \approx \frac{g_{mn}}{g_{dsn} + g_{dsp}} [V_{gs1}(S) - V_{gs2}(S)] \frac{\omega_2}{s + \omega_2} \quad \text{eq. (2.42)}$$

by the identity,  $V_{id} = V_{in1} - V_{in2}$ ,  $V_{gs1}$  and  $V_{gs2}$  and substitution of equation 2.20 we can simplify further, giving;

$$A_{vd}(S) \approx A_{vd} \left( \frac{\omega_2}{s + \omega_2} \right) \quad \text{eq. (2.43)}$$

To confirm the assumption in equation 2.41 the location of the poles must be determined as stated earlier. To properly determine whether we can ignore the pole introduced by C1 we must insure that the pole location be three (3) octaves larger than the pole from C2. This is a standard approximation method used to model an nth

order system by its dominant pole giving a first order solution. The validity of the assumption can be determined by using device parameters of the actual designed differential amplifier.

Initially we must regress to the point at which we implemented the small signal model for the differential amplifier with parasitic capacitors. The capacitors C1 and C2 in figure 2.5 are made up of the series and parallel combinations of the parasitic capacitors seen by the inputs to each leg of the dif-amp. If we examine the full small signal model for the dif-amp, an expression for each capacitor can be reached in terms of the parasitics.

$$C_1 = \frac{C_{gd1}(C_{gb1} + C_{gs1})}{C_{gd1} + C_{gs1} + C_{gb1}} + C_{db1} + C_{gb3} + C_{gs3} + C_{db3} + C_{gs4} \quad \text{eq. (2.44)}$$

$$C_2 = \frac{C_{gd2}(C_{gs2} + C_{gb2})}{C_{gd2} + C_{gs2} + C_{gb2}} + C_{db2} + C_{db4} + C_c + C_L \quad \text{eq. (2.45)}$$

Where  $C_c$  is equivalent to the compensation capacitance, and  $C_L$  is the parasitic capacitances of the following stage's input. Typically the parasitic capacitors are in the pico Farad range. The capacitance  $C_2$  will be dominated by the compensation capacitance  $C_c$ , since it is much greater than the parasitics, as can be seen by inspection of equation 2.45. To compare  $C_2$  and  $C_1$  we must determine the magnitudes of each of the parasitic capacitors by equations 2.46 and 2.47.

$$C_{gb} = \frac{\epsilon_0 \epsilon_{rox} \text{Area}}{t_{ox}} = C_{gd} = C_{gs} \quad \text{eq. (2.46)}$$

$$C_{db} = \text{Area} \left[ \frac{\epsilon_0 \epsilon_{rox} q}{2(V_{bi} - V_A) \frac{(N_A + N_D)}{N_{A\bar{D}}}} \right]^{\frac{1}{2}} = C_{sb} \quad \text{eq. (2.47)}$$

where  $N_A$  and  $N_D$  are relative to the type of devices we are looking at for each capacitor.

Returning to the confirmation of the assumption we made earlier. The determination of each of the pole locations of equation 2.41, to give equations 2.42 and 2.43, must be made. We will call the first singularity or pole  $\omega_1 = \frac{g_{mp}}{C_1}$  and the second pole  $\omega_2 = \frac{(g_{dsn} + g_{dsp})}{C_2}$ . Now if we use approximate values for the process parameters, device sizes, and biasing we can get a first order approximation suitable to prove our assumption.

$$\omega_1 = 42.5164 \text{ GHz} \qquad \qquad \omega_2 = 1.68095 \text{ GHz}$$

Note : These values are determined by estimates of the approximate sizes and process dependencies of the devices. A numerical proof of the pole values can be made once the complete op-amp and process have been designed.

By inspection it is obvious that the pole  $\omega_2$  is Four (4) decades larger than that of  $\omega_1$ . Therefore the assumption made in equation 4 is valid for the dominant pole approximation.

## 2.2 Output Stage

The Output stage of the operational amplifier is an inverter stage with an active-resistor load . Only one stage is used for the output buffer gain stage, which will result in a relatively large output resistance. A second inverter or buffer can be placed after the first output stage to improve the output impedance in addition to increasing the output voltage swing. For simplicity purposes a single output stage was chosen and is shown in figure 2.6.

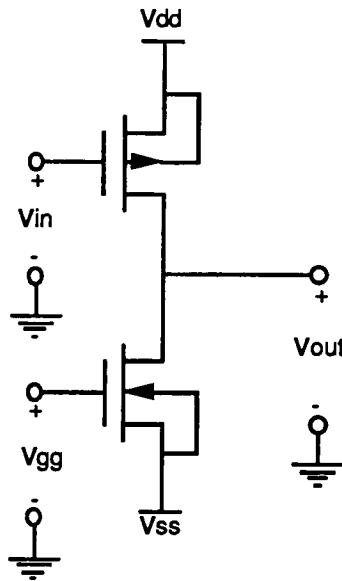


Figure 2.6 (Output stage of operational amplifier)

The supply voltages  $V_{dd}$  and  $V_{ss}$  are equal and opposite in magnitude as throughout the whole op-amp. The bias voltage  $V_{gg}$  is used to bias M2, the current source, to set the operating point of the output. The

current is related to the gain of the device as will be seen in the small signal model gain.

### 2.2.1 Small signal analysis

The small signal model of the output inverter with current source load is relatively simplistic. The implementation and simplifications of the model result in a schematic shown in figure 2.7. As can be seen in figure 2.7 there is only one dependent current source in the model as a result of the P-type device, M1. The current source, M2, is assumed to have a constant bias voltage thus the gate to source voltage is also assumed constant. The dependent current source provided in the small signal model of M2 is dependent upon  $g_{mn}$  and  $V_{gs2}$  which are both dependent on  $V_{gg}$ , the bias voltage.

$$g_{mn} = \frac{\partial I_d}{\partial V_{gs}} \quad \text{eq. (2.48)}$$

But the voltage  $V_{gg}$  is a DC voltage which for the small signal is assumed to be ground, thus we can ignore this dependent current source.

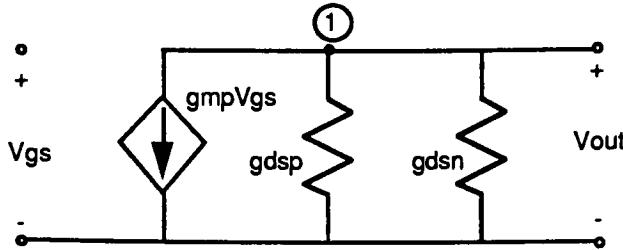


Figure 2.7 (Small Signal Model of output stage)

By writing the equation at point 1, a relation between the output voltage and the gate to source voltage can be realized, equation 2.49.

$$V_{gs1}g_{mp} + V_{out}(g_{dsp} + g_{dsn}) = 0 \quad \text{eq. (2.49)}$$

Now, substituting equation 2.50 into equation 2.49 gives equation 2.51, the small signal gain of the output stage.

$$V_{in}=V_{gs1} \quad (\text{For the small signal case only}) \quad \text{eq. (2.50)}$$

Substituting;

$$Av = \frac{-g_{mp}}{gd_{sp} + g_{dsn}} \quad \text{eq. (2.51)}$$

Each of the conductances of equation 2.51 is related to the device parameters by the equations 2.5 - 2.8 defined previously in this

chapter. Rewriting equation 2.51 in terms of the device parameters reveals equation 2.52.

$$A_v = -\frac{1}{\lambda_n + \lambda_p} \left[ \frac{2K'pW_p}{I_D L_p} \right]^{\frac{1}{2}} \quad \text{eq. (2.52)}$$

From equation 2.52 the dependency of the small signal gain upon the current  $I_D$  is proportional to the inverse square root to the current from source, M2. The current is therefore proportional to the large signal bias voltage  $V_{gg}$ .

## 2.2.2 Frequency Response

The frequency response of the output inverter stage is a relatively simple derivation for the first order response. Initially the parasitic capacitors must be identified and integrated into the small signal model. Figure 2.8 shows the parasitic capacitances as they would appear in the large signal model. Figure 2.9 shows the small signal model of the output inverter with the lump parasitic capacitor,  $C_{\text{Leq}}$ .

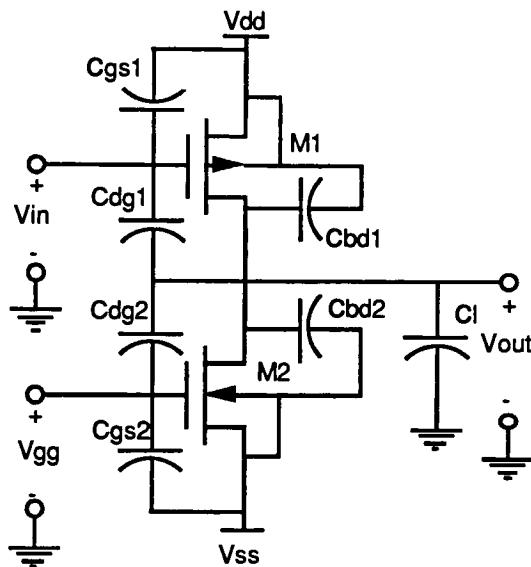


Figure 2.8 (Output Inverter stage with parasitic capacitances)

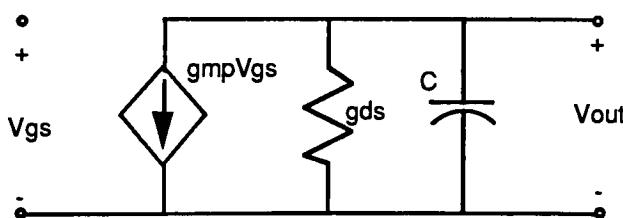


Figure 2.9 (Output stage small signal model of figure 2.8)

The capacitor, C, represents the simplification of the parasitic and load capacitances, elaborated in equation 2.53.

$$C = \frac{C_{gdp}(C_{gsp} + C_{dbp})}{C_{gdp} + C_{gsp} + C_{dbp}} + C_{dpn} + C_{dbp} + C_{gdN} + C_L \quad \text{eq. (2.53)}$$

$$g_{ds} = g_{ds1} + g_{ds2} \quad \text{or} \quad g_{ds} = g_{dsN} + g_{dsp} \quad \text{eq. (2.54)}$$

The analysis of figure 2.9 to obtain a transfer function of the output stage can be accomplished by inspection. The transfer function is;

$$A_v(S) = \frac{V_{out}(S)}{V_{in}(S)} = \frac{-g_m p}{SC + g_{ds}} \quad \text{eq. (2.55)}$$

which will have a single pole at;

$$\text{Pole @ } S = \frac{-g_{ds}}{C} \quad \text{eq. (2.56)}$$

The above equations are all in terms of the parasitic and small signal parameters which can be related to the device and process parameters so an estimation of the frequency response can be performed. Chapter 3 will define the full op-amp frequency response from this along with the actual device dimensions which will allow us to estimate the frequency response of the system.

## 2.4 Voltage Bias Circuitry

The components of the CMOS operational Amplifier require particular bias voltages other than that of the power supply voltages. The bias voltage is used for the DC current sources in the differential amplifier and output stages of the op-amp. The bias voltage is created with a voltage divider chain of active load transistors. A bias structure of diffused or polysilicon resistors instead of active load devices is also suitable, if area is not crucial. The use of transistors for resistive loads will reduce the area for the same size resistor but nonlinearities are introduced due to the transistor effects. For some applications, such as ours, the divergence from this linear resistive behavior can be acceptable for the sake of area.

The design of the active load voltage divider chain can be done with two devices, as can be seen in figure 2.10, one P-type and the other N-type. The DC current sources of the op-amp are in a current mirror configuration with the bias structure shown in figure 2.11. The different currents for the differential and output stages are created by varying the device sizing to suit the requirements of that stage. The transistors of the active load voltage divider circuit are always in the saturation region of operation due to the circuit configuration. Connecting the gate and drain of the transistors forces the gate to source voltage and drain to source voltage to be equivalent. By the use of two devices to divide the power supply voltages down to the required voltage, one or both of the active loads can become rather large in area. To combat this problem a

short derivation can be made to show that the aspect ratio of a single device is much larger than that of multiple devices.

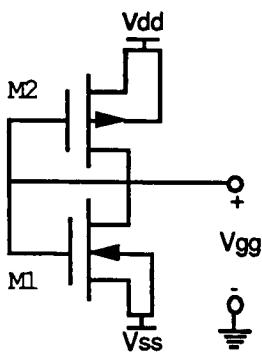


Figure 2.10 (active load voltage bias)

For figure 2.10 a current of  $I_{SS} = 1.5 \mu A$  is required, with power supply voltages  $V_{dd} = 6$  volts,  $V_{ss} = -6$  volts and a suggested transconductance parameters (in saturation)  $K'n = 17 \mu A/V^2$  and  $K'p = 8 \mu A/V^2$  what will the W/L ratios for each device be? By the saturation equation for a MOS transistor,

$$I_d = \frac{K'nW}{2L} [V_{gs} - V_t]^2 \quad \text{eq. (2.58)}$$

and the fact that the current  $I_d$  through, and voltage across each device are equivalent, the width to length ratio of M1 is  $1/17$  and  $1/8$  for M2. Therefore the total active area needed for this device is 25 square units. Now, if a chain of active loads are used instead of a single device, figure 2.11, under the same constraints, the aspect ratios will be different.

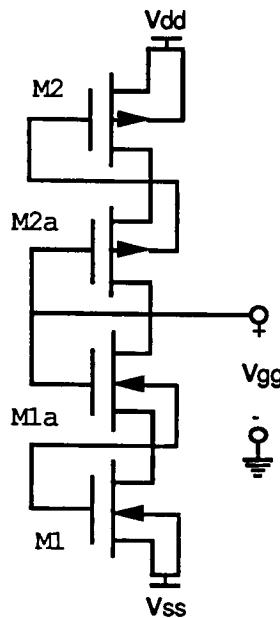


Figure 2.11 (Active load voltage bias)

The output voltage of the bias chain is 0 volts, thus 2.5 volts is dropped across each gate to source for both the N and P type devices. For the same  $K'$  values and using equation 2.58 the width and length are  $64/153$  respectively for M2 and  $8/9$  for M1. Calculating the aspect ratio of the devices for a width of one unit yields a total of 7.03 square units used for the active areas of these devices. This demonstrates the previous statement which dictates that a single active load device will occupy more area, thus a larger aspect ratio, than a chain of active loads to create the same output voltage and current.

Returning to the bias structure used for the CMOS operational amplifier. Unlike the example/derivation above the bias voltage needed for the op-amp is a negative voltage within 2 volts of Vss (-

6 Volts). A circuit configuration, seen in figure 2.12, which has a single N-type device and Four(4) P-type devices is chosen for the initial hand calculations.

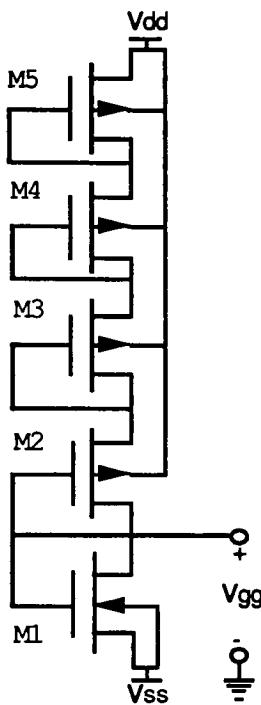


Figure 2.12 (Bias circuit for op-amp)

The device sizes will be determined in chapter 3 through hand calculations then checked by computer simulations for the calculated bias voltage,  $V_{gg}$ .

## Chapter 3 Design Realization

### 3.0 Introduction

In the previous chapter we defined the three stages of the CMOS operational amplifier and pertinent operating equations for each. In this chapter the pieces of the op-amp will be integrated and the whole response of the operational amplifier will be derived. This method of analysis is valid for the op-amp since it is modeled as a linear first order system as proved in chapter 2.

In addition to the determination of the equations describing the behavior of the amplifier, the device sizes will be determined from the specifications of performance and process parameters. Once the device geometries are determined simulations of the DC and AC responses will be performed using the S.P.I.C.E. circuit simulation tool. The device dimensions will be modified to achieve the operating parameters for the operational amplifier which match those set in the specification. The proof of the fact that the op-amp is a first order system will again be supported with the simulations of the open loop frequency responses.

### 3.1 Small Signal Gain

A representation of the operational amplifier in block form is shown in figure 3.1 below. Since the design of the op-amp is a two stage design, the analysis of the whole system is easily attained once the individual responses of each stage are defined.

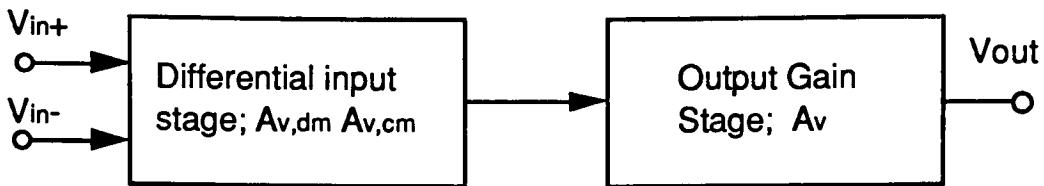


Figure 3.1 (Operational Amplifier stage representation)

The differential mode voltage gain of the op-amp can be calculated by multiplying the voltage gain of the output stage by the differential voltage gain of the dif-amp stage. Using equations 2.21 and 2.52 of chapter 2 an expression for the entire voltage gains and frequency responses of the op-amp can be written. The differential voltage gain is

$$Av_{dm} = \frac{-g_{mn} g_{mpo}}{(g_{dsn} + g_{dsp})(g_{dsno} + g_{dsp})} \quad \text{eq.(3.1)}$$

substituting equations 5 through 8 from chapter 2 gives

$$Av_{dm} = \frac{2 g_{mn} g_{mpo}}{I_{sslo}(\lambda_n + \lambda_p)^2} \quad \text{eq.(3.2)}$$

where;  $g_m = \left[ 2K' \frac{W}{L} |Id| \right]^{\frac{1}{2}}$

The conductances  $g_{mn}$  and  $g_{mp}$  are relative to the widths and lengths of the devices they represent. The conductance of the P-type device

is for the PMOS device in the output stage and the conductance of the N-channel device is that of the input device in the differential pair. The two currents in equation 3.1 are  $I_{ss}$  of the differential stage and  $I_o$  of the output stage. These currents are created by the current mirror bias structure discussed in section 2.4.

The common mode voltage gain of the operational amplifier is calculated in the same manner as the differential gain. The common mode gain is the product of equations 2.38 and 2.52 in chapter 2.

$$A_{v,cm} = \frac{g_o g_{dsn} g_{mpo}}{2g_{mp}(g_{dsn} + g_{dsp})(g_{dsno} + g_{dspo})} \quad \text{eq.(3.3)}$$

Substituting equations 2.5-8 again gives;

$$A_{v,cm} = \frac{2\lambda_n \lambda_p}{(\lambda_n + \lambda_p)^2} \left[ \frac{I_{ss} L_p K'_p W_{po}}{K'_p W_{plo} L_{po}} \right]^2 \quad \text{eq.(3.4)}$$

Where  $I_o$  and  $K'_{op}$  are parameters of the P-channel device in the output stage. The channel length modulation parameter  $\lambda$  is constant for the various devices in the op-amp and will be assumed to be independent of size for the first order analysis.

The common mode rejection ratio, CMRR, is a ratio describing the ability of the amplifier to discriminate between the common and differential modes. For most applications the common mode component of the output response is not desired and will appear as an error in the output signal. The goal for most amplifier designs is to maximize the CMRR which will minimize the common mode component.

$$CMRR = \left| \frac{A_{vdm}}{A_{vcm}} \right| \quad \text{eq.(3.5)}$$

Substituting equations 3.2 and 3.4 into the CMRR gives equation 3.6.

$$CMRR = \frac{1}{I_{ss}\lambda_n\lambda_p} \left[ \frac{2K'_nW_nK'_pW_p}{L_n L_n} \right]^{\frac{1}{2}} \quad \text{eq.(3.6)}$$

The common mode rejection ratio is ideally infinite, with the common mode gain ideally zero and the differential gain infinite. Since amplifier design will attempt to approach the ideal case the CMRR is very large, typically in the 1E+6 range. From equation 3.6 the CMRR will be rather large as a result of the product of the channel length modulation, which is much less than one, in the denominator. By inspection of equation 3.6 we can see that the output gain has no effect on the CMRR since it is common to both of the voltage gains. Therefore the CMRR occurs only as a result of the differential amplifier stage of the op-amp.

### 3.2 Output Resistance

The first order calculation of the output resistance is relatively simple and can be derived virtually by inspection of the output stage small signal model.

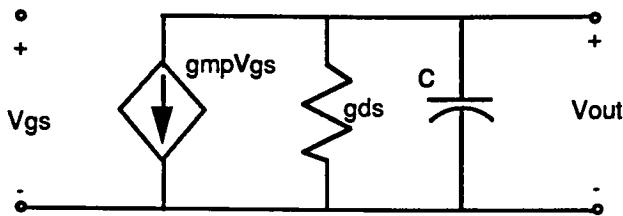


Figure 3.2 (Small signal model of output stage)

In Figure 3.2, which has been repeated from chapter 2, if we apply a 1 volt voltage source to the output and calculate the current  $I_{out}$  in terms of the device parameters an expression is obtained, equation 3.7.

$$I_{out}(S) = g_{mp}V_{in}(S) + V_{out}(S)(g_{dsp} + g_{dsn} + CS) \quad \text{eq.(3.7)}$$

Now if we let the frequency,  $\omega$ , approach zero Hertz (Hz), and define  $V_{out}$  to be 1 Volt, equation 3.7 reduces to equation 3.8

$$R_{out} = \frac{1}{(g_{dsp} + g_{dsn})} \quad \text{eq.(3.8)}$$

### 3.3 Frequency Response and compensation

The frequency response of the operational amplifier will determine the singularities and zeroes of the system as well as the system's stability. Once the transfer function of the op-amp is attained, the gain bandwidth product along with a compensation scheme can be calculated. The transfer function is derived in the same manner as the differential and common mode gains in the previous section. In chapter 2 the small signal models as well as expressions for the frequency response of each stage of the operational amplifier were derived. A simplified version of the AC model with parasitic components can be seen in figure 3.3.

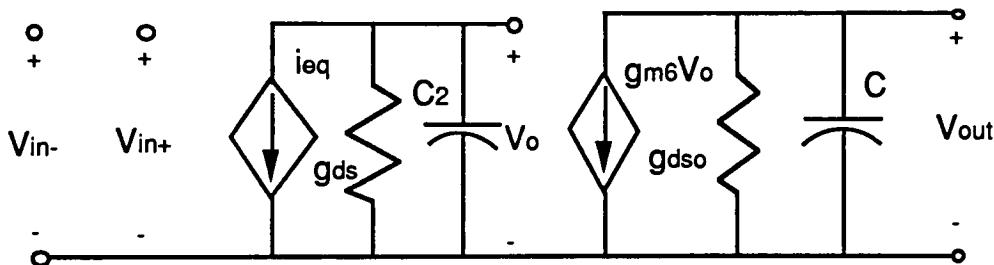


Figure 3.3 (op-amp small signal model)

The transfer function of the operational amplifier will determine the poles and zeroes of the system and express them parametrically. Writing the current equations for the model of figure 3.3 gives;

$$A_v(S) = \frac{g_{mpo} g_{mn} \omega_2}{(g_{dsn} + g_{dsp})(SC + g_{dso})(S + \omega_2)} \quad \text{eq.(3.9)}$$

where,  $\omega_2 = \frac{(g_{dsn} + g_{dsp})}{C_2}$  and

$$C = \frac{C_{gdp}(C_{gsp} + C_{dbp})}{(C_{gdp} + C_{gsp} + C_{dbp})} + C_{dpn} + C_{dbp} + C_{gd} + C_L \quad \text{eq.(3.10)}$$

$$C_2 = \frac{C_{gd2}(C_{gs2} + C_{gb2})}{(C_{gd2} + C_{gs2} + C_{gb2})} + C_{db2} + C_{db4} + C_c + C_o \quad \text{eq.(3.11)}$$

$$g_{dso} = g_{ds6} + g_{ds7} \quad \text{eq.(3.12)}$$

The poles of the op-amp are located at;

$$P_1 = -\omega_2 \quad \text{eq.(3.13)}$$

$$P_2 = \frac{-g_{dso}}{C} \quad \text{eq.(3.14)}$$

The primary pole of the op-amp is  $P_1$  since it contains the compensation capacitance which is large with respect to the parasitic capacitors of the transistors. The load capacitance,  $C_L$ , is a small value, typically  $0.001C_L$ , and thus the compensation capacitor,  $C_c$ , will dominate the frequency response for the first order system.

The gain bandwidth product of the operational amplifier is calculated by the determination of the unity gain point of the frequency magnitude response. For the first order calculation pole  $P_2$  will be ignored thus simplifying the calculations. The bandwidth is simply;

$$\omega_c = \frac{g_{mn}}{C_2} \quad \text{eq.(3.15)}$$

The value of the capacitor C2 is dominated by the compensation capacitance,  $C_c$ , thus allowing equation 3.13 to be rewritten as;

$$\omega_c = \frac{g_{mn}}{C_c} \quad \text{eq.(3.16)}$$

### 3.4 Device Sizing

Now that the majority of parameters used to characterize an operational amplifier have been derived, the device dimensions can be defined to optimize as many of the specification of operation for the op-amp as possible.

#### 3.4.1 Operational Amplifier specification

Differential mode gain	$A_{v,dm} > 1000$
Common mode gain	$A_{v,cm} = 0$
Gain bandwidth product	$GB \geq 1\text{MHz}$
Common mode range	$CMR = \pm 5 \text{ volts}$
Common Mode Rejection Ratio	$CMRR = \infty$
Output Range	$\pm 5 \text{ volts}$
Power dissipation	$< 0.96 \text{ mW}$
Power supply voltages	$\pm 6 \text{ volts}$
Input resistance	$R_{in} \approx \infty \Omega$
output resistance	$R_{out} \approx 0 \Omega$

The process parameters which are determined by specifications and simulation are;

Gate oxide thickness

$$t_{ox} = 500\text{\AA}$$

Threshold voltages

$$V_{thn} = |V_{thp}| = 1 \text{ volt}$$

Channel length modulation

$$\lambda_n = \lambda_p = 0.02$$

Channel Mobilities

$$\mu_p \approx 450 \text{ cm}^2/\text{V}\cdot\text{sec}$$

$$\mu_n \approx 800 \text{ cm}^2/\text{V}\cdot\text{sec}$$

As with the previous sections of this paper the device dimension definitions will be divided into the two stages of the op-amp. By dividing the operational amplifier up into two sections the gains for each section are allocated to be  $A_{v,dm} = 100$  for the differential amplifier stage and  $A_v = 50$  for the output gain stage. This will yield an overall differential gain of 5000, which is well within the specifications.

Before the devices are defined the constants  $K'_n$  and  $K'_p$  must be calculated from equations 3.17 and the above process parameters.

$$K' = \frac{\mu_0 \epsilon_0 \epsilon_{rox}}{t_{ox}} \quad \text{eq.(3.17)}$$

$$K'_n = 5.5224 \text{ E-5 A/V}^2 \quad K'_p = 3.10635 \text{ E-5 A/V}^2$$

The minimum geometry design rule of the op-amp will be set at 10  $\mu\text{m}$  for ease of processing and lithography. Using equation 2.21 of chapter 2 we can define the device sizes for the differential pair.

$$A_{vd} = \frac{2}{(\lambda_p + \lambda_n)} \left[ \frac{K'_n W_n}{I_{ss} L_n} \right]^{\frac{1}{2}} \quad \text{eq. (2.21)}$$

If we let  $I_{ss} = 20 \mu\text{A}$  and apply constants and specified values the width of the input N-type transistors is found to be;

$$W_n \approx 15 \mu\text{m}$$

To determine the sizes of the P-channel devices in the current mirror of the dif-amp the CMR must be investigated. Equation 3.18 describes the input common mode range in terms of worst case threshold voltages, the widths and lengths of the P-type devices M3 and M4 in the current mirror, the supply current ( $I_{ss}$ ) and supply voltage ( $V_{ss}$ ).

$$V_{g3(\min)} = V_{ss} + \left( \frac{I_{ss}}{\beta_p} \right)^{\frac{1}{2}} + V_{tno} - |V_{tpo}| \quad \text{eq.(3.18)}$$

where;  $\beta_p = \frac{K'_p W_p}{L_p}$  eq.(3.19)

$$V_{tno} = 1.2 \text{ V} \quad \text{and,}$$

$$V_{tpo} = -0.8 \text{ V}$$

solving for  $W_p$  will give a P-type channel width of;

$$W_p = 20 \mu\text{m}.$$

Since the two legs of the differential amplifier are symmetric the dimensions of transistors M1 through M4 have been defined. The final transistor of the dif-amp, M5, is the current source for the differential amplifier, which will supply an  $I_{ss}$  current of  $20\mu\text{A}$ . The dimensions of M5 can be defined by equation 3.20 which is simply the saturation equation of an N-channel MOSFET.

$$I_{ds} = \frac{\beta_n}{2} (V_{gs} - V_t)^2 \quad \text{eq.(3.20)}$$

The supply current  $I_{ss}$  is equivalent to the drain to source current  $I_{ds}$ , and  $\beta_n$  is described by equation 3.19 for the N-channel device. If the width of M5 is solved for with equation 3.20 a relation between the gate voltage  $V_{gs}$  and the device width can be attained. The gate voltage of M5 is equivalent to the bias voltage, thus a bias voltage should be chosen which will yield an appropriate width and an attainable voltage magnitude that will yield the correct operating point for the operational amplifier stages. The voltage  $V_{gg}$  needed to bias the current sourcing transistors will also require that they supply a  $20\mu\text{A}$  current. For this design a gate voltage  $V_{gs}=-4.4$  volts is defined, giving in the width of M5 to be,  $W_n = 20 \mu\text{m}$ . At this point a schematic of the differential amplifier section will appear as figure 3.4.

The sensitivity of the current  $I_{ss}$  through M5 on the gain of the differential amplifier is significant. Equation 2.21 shows that  $I_{ss}$  is

inversely related to the differential gain of the dif-amp. The bias circuitry used to set up the DC currents are the main source of divergence from the designed bias values. S.P.I.C.E. simulations of the op-amp will isolate these problems which can then be compensated by the variance of the device geometries. For future designs a different method of biasing the current sourcing transistors should be determined. One such method being a band gap reference current source.

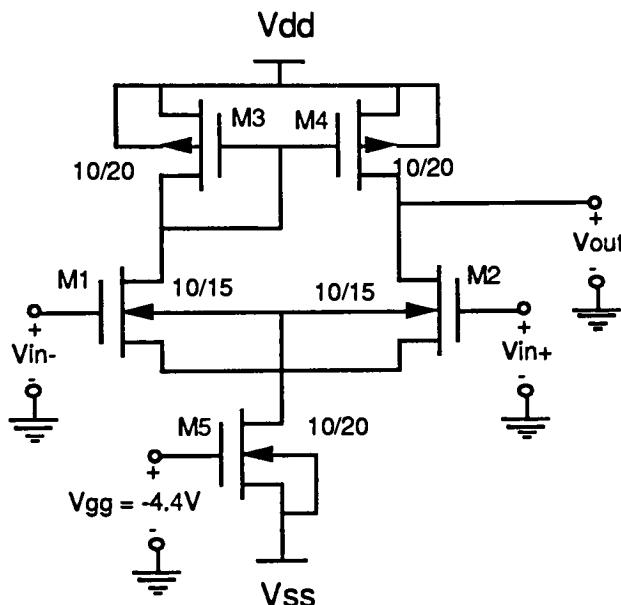


Figure 3.4 (Differential stage with device dimensions)

The definition of the devices sizes for the output stage is much like that of the differential amplifier stage. The gain of the output stage is defined in equation 2.52 in chapter 2 but is repeated here for convenience;

$$A_v = \frac{1}{(\lambda_p + \lambda_n)} \left[ \frac{2 K_p W_p}{I_d L_p} \right]^{\frac{1}{2}} \quad \text{eq.(2.52)}$$

The output stage will be designed to a voltage gain of 50 and a bias current of 20  $\mu\text{A}$ . Substituting values into equation 2.52 and solving for the width of the P-channel device will give;

$$W_p = 15 \mu\text{m}$$

The definition of the current sourcing transistor in the output stage is identical to the method of solution for the differential amplifier. Since we previously defined the bias voltage to be,  $V_{gg} = -4.4$  voltage which will give a gate to source voltage,  $V_{gs} = 1.6$  volts, the device size of M7 will be straight forward using equation 3.20.

$$W_n = 20 \mu\text{m}$$

A schematic of the output stage of the operational amplifier is shown in figure 3.5 below.

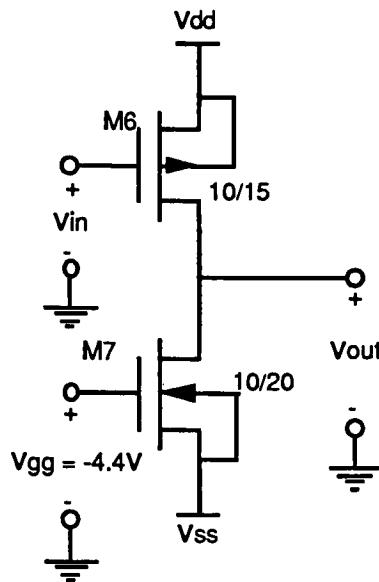


Figure 3.5 (Output stage with device dimensions)

The final stage of the operational amplifier which requires device geometry definition is the voltage bias section. As discussed in the previous chapter the voltage bias needed for the current sources is created by an active load voltage divider chain. To implement the bias structure the current through the voltage divider will be  $I_{ss} = 20 \mu\text{Amps}$  which creates a output voltage  $V_{gg} = -4.4$  volts.

The device dimensions are specified by equation 3.20, only one N-channel device will be used between the output and the negative supply voltage,  $V_{ss}$ . By substitution of the variables into the saturation equation the width of,  $W_n = 20 \mu\text{m}$ , and a length of,  $L_n = 10\mu\text{m}$ . The sizes of the P-type devices depends on the number used to drop a voltage of 10.4 volts. By a trial and error solution of equation 3.20 an appropriate width will be obtained. For the bias

needed by the op-amp only three PMOS transistors of equal dimensions are used for the hand calculations, each having a voltage drop of,  $V_{sd} = 3.4667$  Volts. The width and length of these devices are,  $W_p = 10\mu\text{m}$  and  $L_p = 40\mu\text{m}$  respectively.

At this point the op-amp resembles its final form as calculated by hand techniques and can be seen in figure 3.6 below.

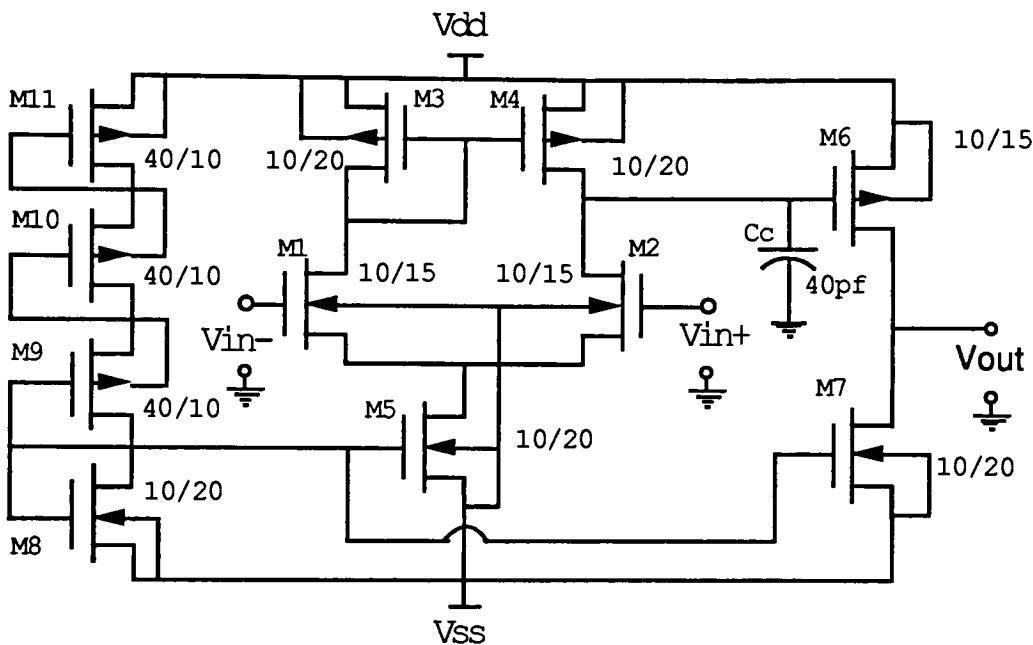


Figure 3.6 ( CMOS Operational Amplifier)

Figure 3.6 includes the frequency compensation capacitor which is calculated using, equation 3.16, the gain bandwidth product. From the specification, a gain bandwidth product of,  $GB = 1\text{MHz}$ , and the transconductance of the N-type input devices are used to determine the first order hand calculated compensation capacitance to be ;

$$C_c = 40 \text{ pF}$$

### 3.5 Simulated Results

Simulations of the CMOS Operational Amplifier design were performed using S.P.I.C.E., Simulator Program with Integrated Circuit Emphasis, version 2G.5. Simulations of the various AC and DC responses, input and output impedances, Input offset voltage, Input Common Mode Range, and Total Power dissipation are used to characterize the performance of the op-amp. The model parameters used to simulated the op-amp were either researched from literature, extracted from Suprem 3 simulations of the CMOS process, and hand calculated values. A detailed list of the S.P.I.C.E. input deck which includes the model parameter values is found in Appendices 1 and 4.

#### 3.5.1 Input offset voltage

The simulation of the input offset voltage is rather simple. If a simulation of the operational amplifier is performed with the configuration of figure 3.7, then the input offset voltage can be measured at the output. The cause of an offset voltage is any asymmetries in the differential amplifier stage of the op-amp.

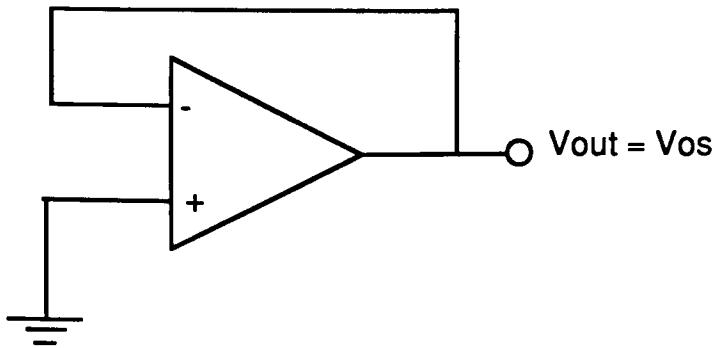


Figure 3.7 (Configuration for measuring input offset voltage)

The final input offset voltage after spice level 2 simulations of the op-amp in figure 3.11 is found to be;

$$V_{os} = 0.00797044 \text{ Volts}$$

### 3.5.2 DC Mode gain simulations

The simulations for both the common mode and differential mode voltage gains can be performed in both the large and small signal analysis. The DC gains can be measured by inspection of the transfer curves of  $V_{in}$  verse  $V_{out}$  for the particular input configurations. The simulation of the differential gain will vary the non-inverting input, letting the inverting input be grounded, and observing the output voltage swing, see graph 3.1. This is also known as the single sided differential voltage gain. By data extraction of the output response a value for the maximum gain can be attained.

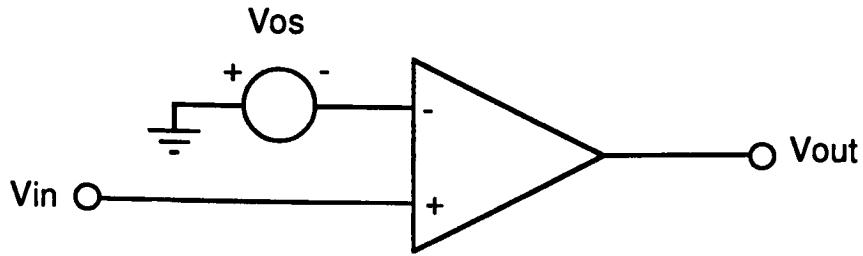
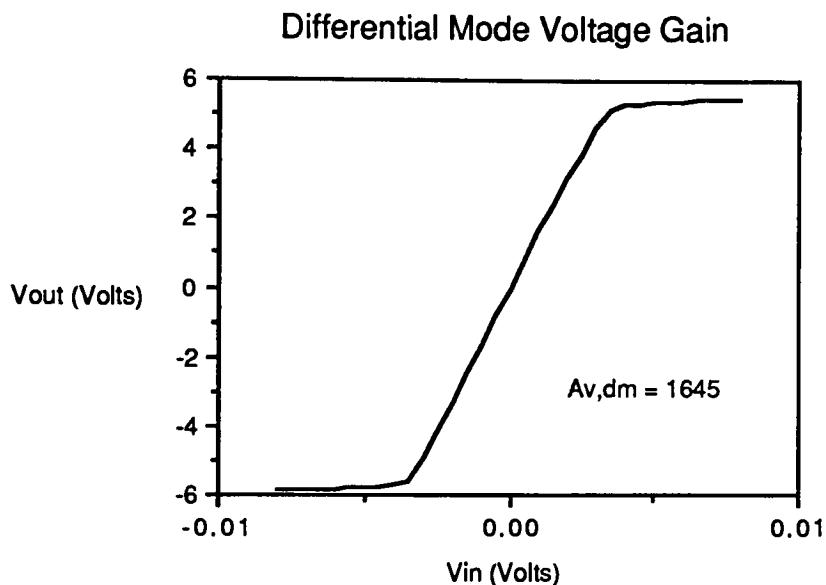


Figure 3.8 (Open loop differential mode voltage gain configuration)



Graph 3.1

From graph 3.1 the maximum differential mode voltage gain is;

$$Av_{dm} = 1645$$

This value can be compared to the A.C. open loop differential mode voltage gain at low frequencies for confirmation

The Common mode voltage gain utilizes the circuit configuration of figure 3.9. By interconnecting the positive voltage node of the offset voltage source to the non-inverting input and the positive node of the input voltage source, the common mode operation of the op-amp can be determined. The common mode response can be seen in graph 3.2.

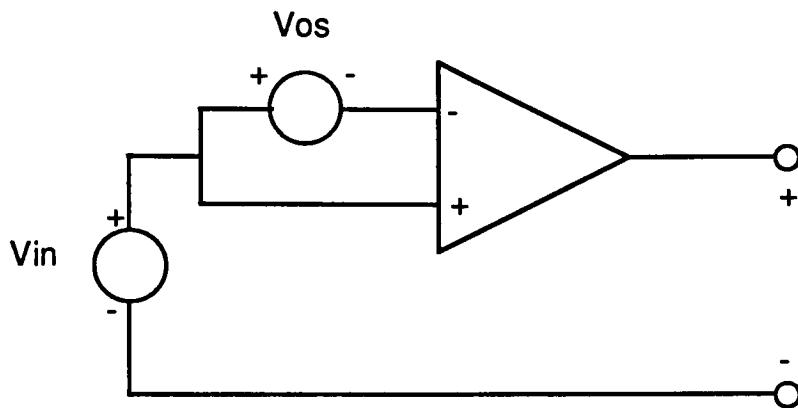
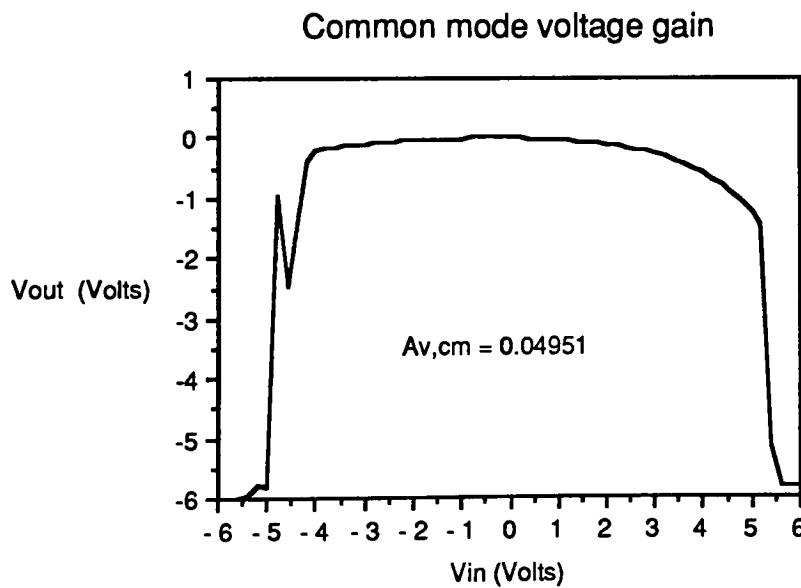


Figure 3.9 ( Common mode voltage gain configuration)



Graph 3.2

Graph 3.2 of the common mode response shows a range of approximately  $\pm 4$  volts where the common mode gain is minimized;

$$A_{v,cm} = 0.04951$$

The calculation of the common mode gain from graph 3.2 is simply the slope of the line between the input voltage of  $\pm 4$  volts. The common mode response actually has a positive and negative slope over this range but for a first order analysis of this parameter the method of measurement of the common mode gain is sufficient for our purposes. A comparison may be made to the common mode voltage as calculated from the A.C. analysis.

The two extreme conditions when the input voltage is near the supply voltages is due to the current sources of the output and differential stages. As the input voltage approaches the supply voltages the operating point of the current sourcing transistors, particularly in the dif-amp, move towards the origin of the I-V transfer characteristic for the devices. Simply the drain to source voltage approaches zero thus forcing the current,  $I_{ds}$ , to approach zero producing the effects seen in graph 3.2.

### 3.5.3 Input Common Mode Range

The input common mode range (CMR) of the operational amplifier is the range of common mode values where the differential amplifier continues amplify the difference between the inputs with

the same gain. The SPICE simulation of figure 3.10 will yield a plot which is used to define the CMR of the op-amp.

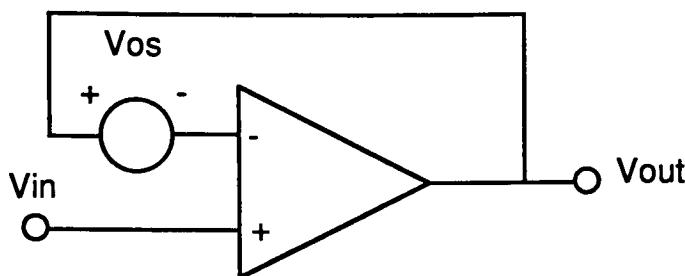
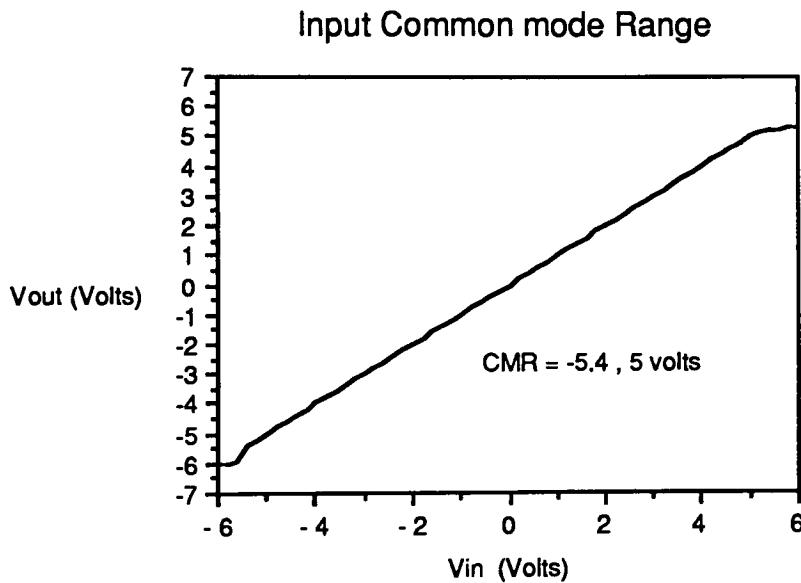


Figure 3.10 (Input common mode range simulation configuration)



Graph 3.3

From graph 3.3 the CMR is found by determination of the range in which the slope is unity, this is the input common mode range. The range is:

$$\text{CMR} = -5.4 \text{ to } 5 \text{ Volts}$$

### 3.5.4 Input and Output Resistance

The simulation of the input and output resistances is in the small signal region of the analysis of the operational amplifier. The input resistance is simulated simply by measurement of the input current at a particular input voltage, by Ohm's Law the input resistance can be found to be;

$$R_{in} = 48.5 \text{ G}\Omega$$

The actual SPICE input deck and output data are given in appendix 1.

To properly determine the output resistance the independent voltage and current sources are grounded and a small signal current with a magnitude of  $1\mu\text{A}$  is forced into the output of the op-amp. By measurement of the output voltage to current ratio the output resistance can be measured. To properly measure the output resistance with a simulation the supply voltages must be left on, thus leaving the devices at their quiescent operating points.

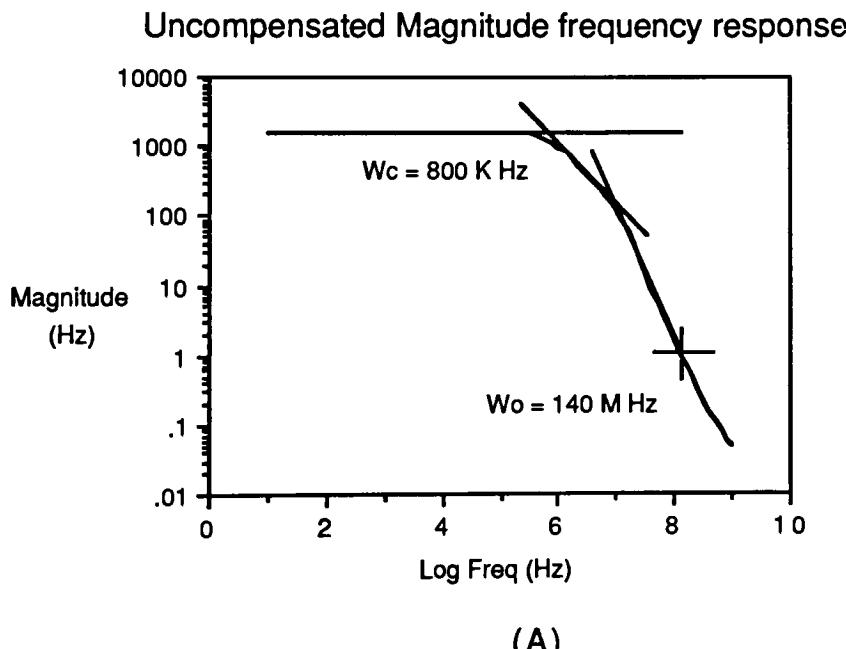
The magnitude of the output resistance will be measured as the frequency approaches zero Hertz. From the SPICE simulation for output resistance in Appendix 1 the output resistance is found to be;

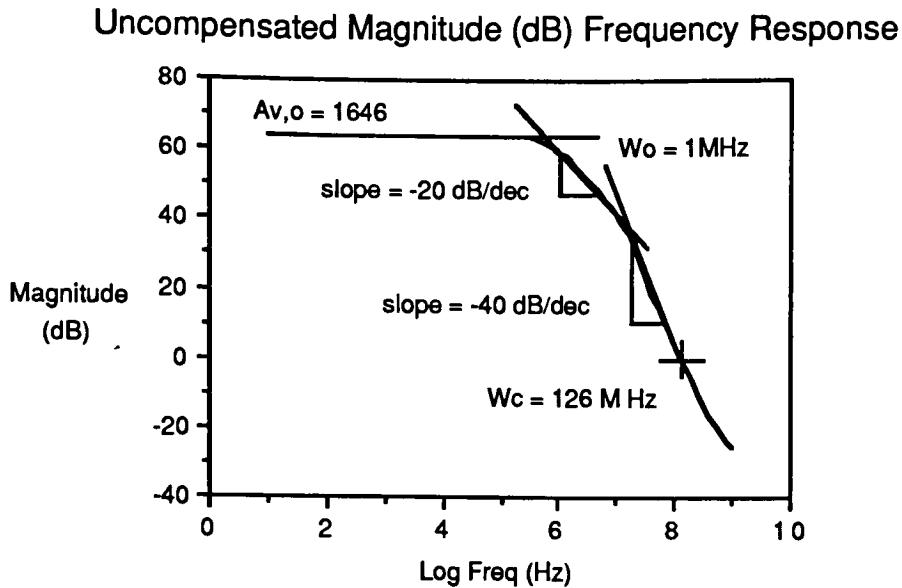
$$R_{out} = 23.9 \text{ K}\Omega .$$

This value is rather large for an operational amplifier, but was expected for the device sizes of the output stage. The solution to a large output resistance is a second output buffer stage of unity gain with large enough device geometries to have small output resistance.

### 3.6 Frequency Response

The frequency response is broken up into two (2) sections, the first the response of the uncompensated operational amplifier, and the second is with frequency compensation. The frequency response of the uncompensated op-amp depends upon the parasitic capacitances of the individual devices. These capacitive values are in the sub-pico farad range which would give an extremely high frequency bandwidth and break frequency, in addition to an unstable closed loop system. The uncompensated frequency magnitude response is shown below.

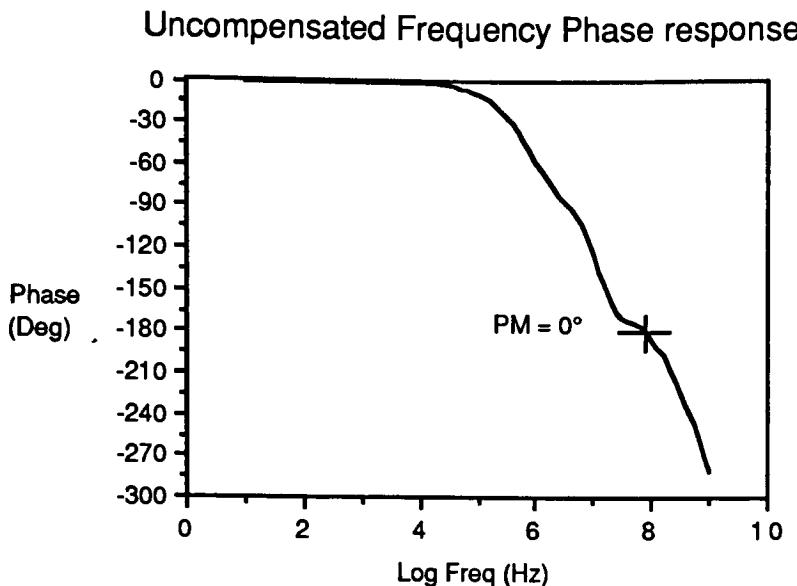




(B)

Graph 3.4 A and B (Magnitude frequency Response)

The frequency magnitude plots for the uncompensated op-amp show a system which does not conform to all the specified operation criteria in the frequency domain. The break frequency also known as the half power point frequency is at  $\omega_o = 1 \text{ MHz}$  which will give a cross over frequency of  $\omega_c = 126 \text{ M Hz}$ . The cross over frequency, also known as the bandwidth and unity gain frequency, is one full decade above the specified value needed for the operational amplifier frequency response. A further look into the frequency response of the op-amp phase response shows that the op-amp is not stable, shown in graph 3.5



Graph 3.5

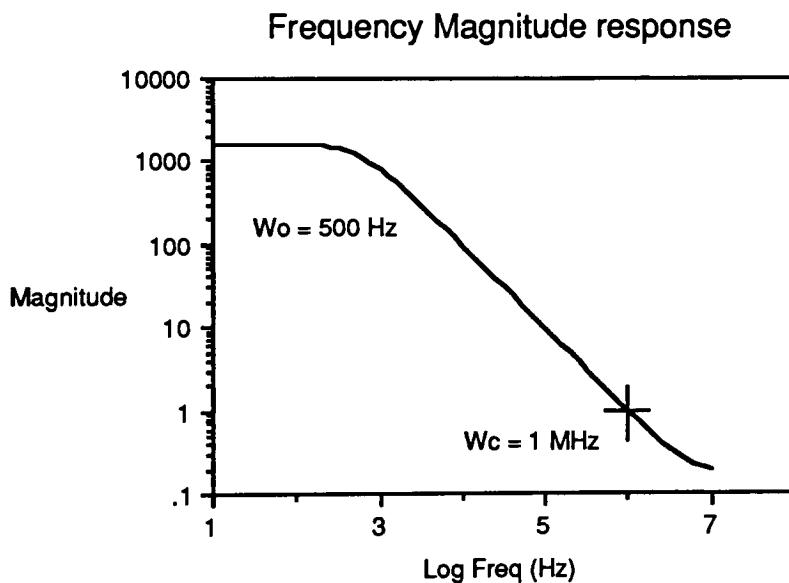
By inspection of graph 3.5 the phase margin is determined to be  $0^\circ$ . The phase margin is the difference between  $180^\circ$  and the phase of the output at the unity gain point. The phase margin of  $0^\circ$  will not yield a closed loop stable system, which is unacceptable. A system with a phase margin of less than  $60^\circ$  is not a robust and closed loop stable system, thus the requirement of a compensation scheme.

By the uncompensated op-amp frequency response it can be seen that the operational amplifier does not behave as a first order system. If a method of compensation is developed to give a bandwidth of 1 MHz the system will behave with a first order frequency response due to the first order approximation method discussed in chapter 2. The compensation scheme needed to achieve the proper response is known as lead compensation. This method introduces a pole well before any parasitic poles of the system, thus leading the system response. For the compensation a capacitor

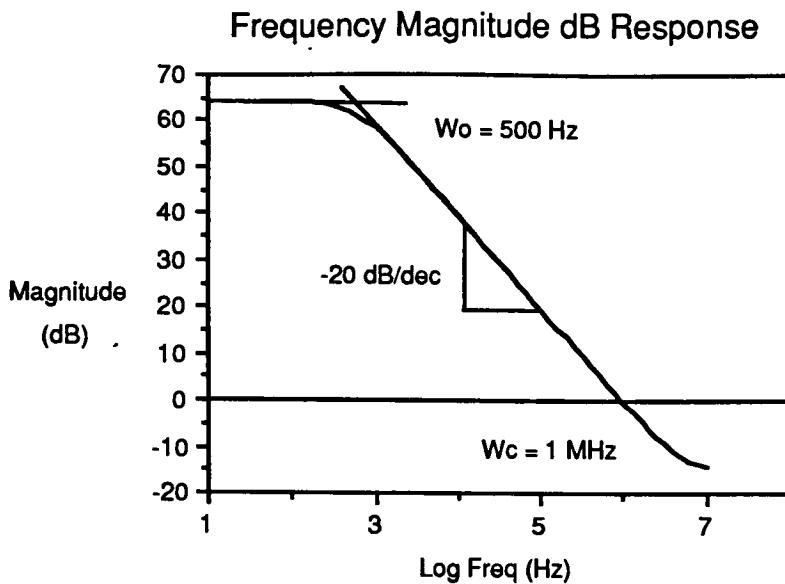
placed on the output of the differential amplifier between the output and ground will provide the needed variation.

By simulation of the frequency response using the hand calculated value of  $C_c = 40\text{pF}$  as a start/reference point a final compensation capacitance of  $C_c = 200\text{pF}$  was determined. The frequency response and the specific data is provided further on in this section.

The magnitude response of the operational amplifier was simulated over a range of 10 - 1G Hz. This will allow the calculation of the Gain-Bandwidth product, the half power frequency, and the validation that the op-amp behaves as a first order system.



Graph 3.6A

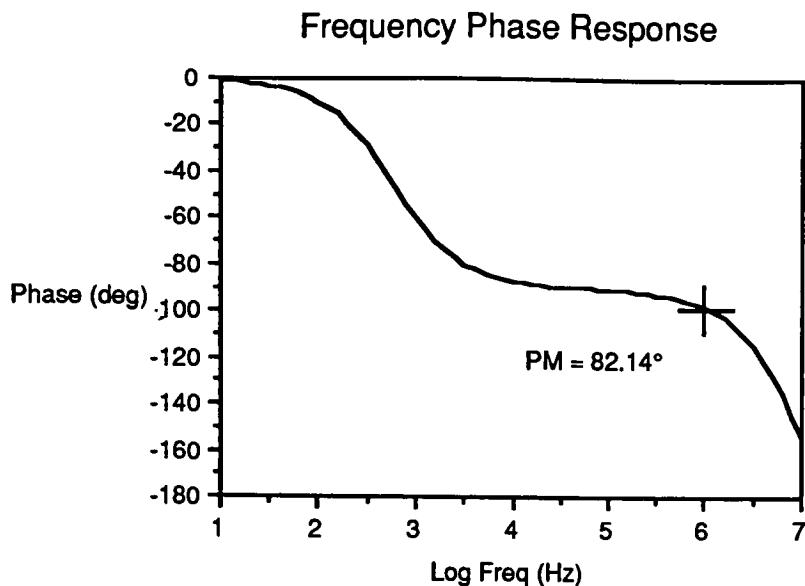


Graph 3.6B

By inspection of Graphs 3.6 A and B a crossover frequency of  $\omega_c = 1 \text{ MHz}$  can be seen at the unity gain point. In addition the op-amp frequency response is a first order system since the response breaks with a -20 dB/decade slope. The a break frequency is at  $\omega_o \approx 500 \text{ Hz}$  which is also known as the half power frequency. The differential voltage gain is found to be  $A_{v,o} = 1645$  from both graph 3.6 A and 3.4 A

The frequency Phase response was simulated over the same frequency range as the magnitude response. The Phase response will show that the operational amplifier is a stable and robust design from the determination of the Phase Margin, (PM). The simulated Phase Margin is found to be;

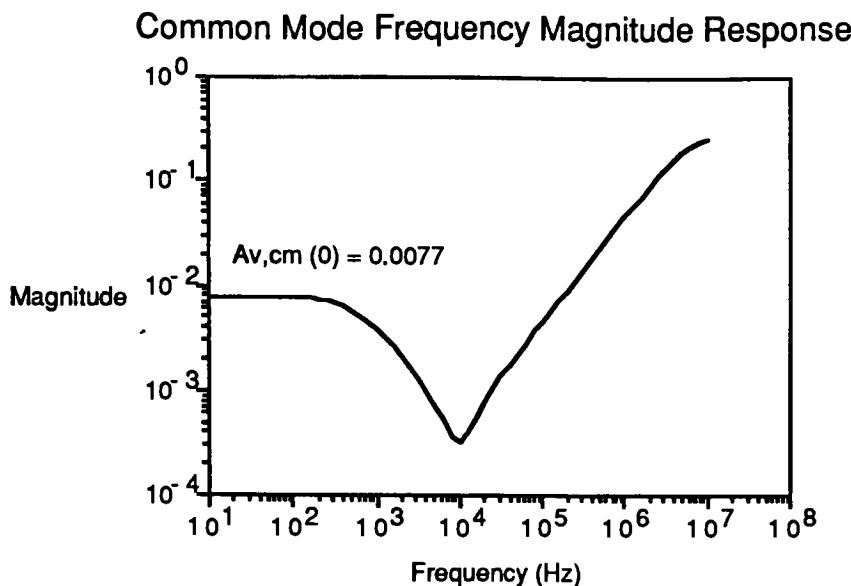
$$\text{PM} = 82.14^\circ.$$



Graph 3.7

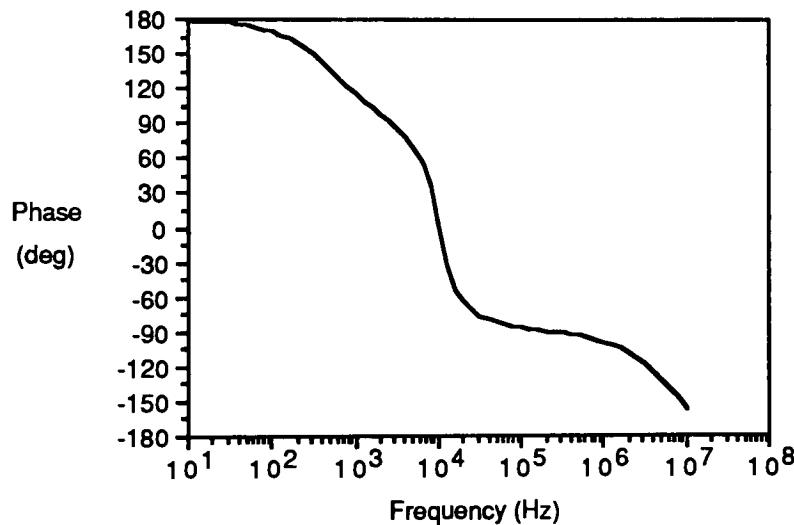
Previously in this section the frequency response that have been presented are for the differential mode of operation of the op-amp. The other mode of operation, the common mode, is also dependent on frequency. The property of the CMRR is a frequency depended value and thus we will need to investigate the common mode frequency response.

By simulation of the op-amp with a single small signal source applied to both inputs a frequency response of the magnitude and phase can be generated.



(A)

Common mode Phase Response



(B)

Graph 3.8 (A) and (B)

By inspection of graph 3.8A, the common mode voltage gain is small for frequencies near DC. The increasing magnitude of graph 3.8A is not a problem since the magnitude is much less than one. The unity gain point of the common mode frequency magnitude is much larger

than the operation frequency of the device and thus is not a concern. The phase response also appears to be good and can be seen in graph 3.8B

### 3.7 Comparison of results

The hand calculations and derivations were performed, modeling the CMOS Operational Amplifier as a first order system. The Small signal hand analysis only considered the first order effects of the transistors in the op-amp. Therefore a comparison between the hand calculations and the SPICE results will not necessarily be identical but should be within the same order of magnitude. Table 3.2 shows each of the performance parameters of the op-amp calculated and their simulated values.

Table 3.2

Parameters	Hand	Spice
$A_{v, dm}$	5500	1645
$A_{v, cm}$	0.1531	0.04951
CMRR	35,924	33,225
$V_{os}$	0.0	0.00797044 V
CMR	$\pm 5$	- 5.4, 5 V
$V_{or}$	$\pm 6$ V	-5.9, 5.5 V
$R_{in}$	$\infty$	48.5 G $\Omega$
$R_{out}$	1.25 M $\Omega$	23.9 K $\Omega$
$P_{Tot}$	0.72 mW	0.842 mW
$W_o$	200 Hz	500 Hz
$W_c$	1M Hz	1M Hz
PM	$\sim 60^\circ$	$\sim 82.14^\circ$

By inspection of table 3.2, the variance between the hand and spice parameter values of the operational amplifier are small. Thus models developed by hand are valid for the design and rough estimates of an operational amplifier performance.

The magnitude of the output resistance was expected from the hand calculations and is the only parameter which violates the specifications. This value is inversely proportional to the current through the output stage of the op-amp as shown earlier. In addition CMOS device sizes are indirectly related to the output impedance of a particular device. Both types of devices are not large and so a high output resistance is expected. A reduction in the output impedance would impact upon other performance parameters such as the common, and differential mode gains, but the greatest impact would be felt in the total power dissipated by the op-amp.

### 3.8 Layout

The layout of the CMOS operational amplifier was performed on the circuit that was fully simulated. The simulated op-amp has some modifications to the devices sizes and the bias structure, but the overall circuit was not radically changed. The greatest variation from the hand derived op-amp is the compensation capacitance value. All changes made on the simulated device are a result of the second order effects which SPICE is able to isolate. A schematic of the CMOS op-amp with device sizes is provided in figure 3.11.

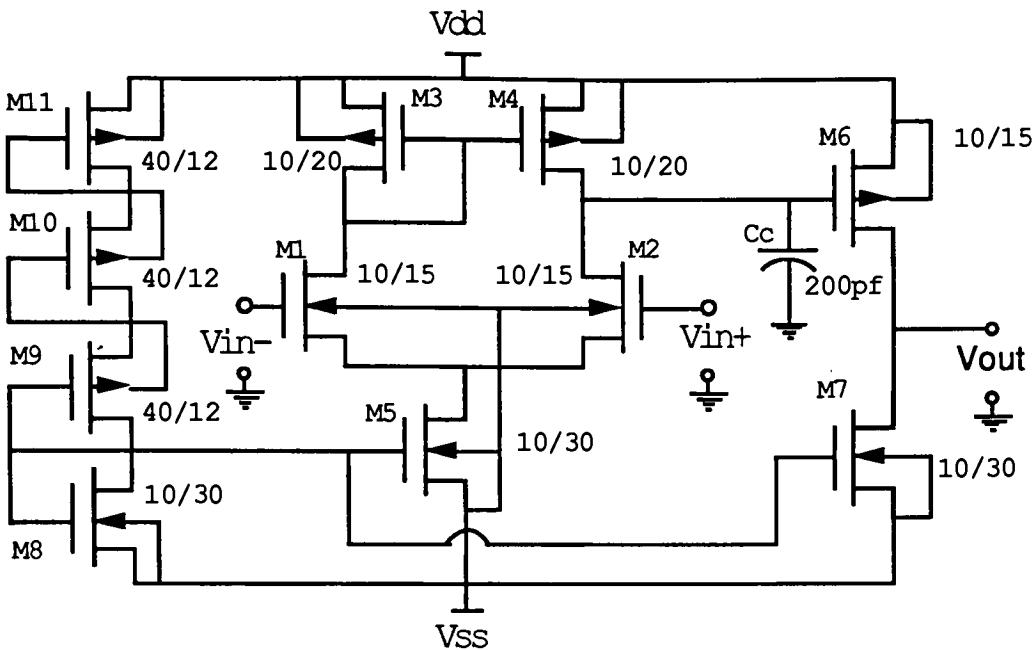


Figure 3.11 (Final realization of CMOS Operational amplifier)

The layout of the CMOS Operational Amplifier as well as the CMOS Test Chip was performed using the I.C.E. layout tool. Subsequent revisions have been layed out using Chipgraph, a Mentor graphics software package. The layout of the op-amp involved careful layout methods to prevent asymmetries in the differential amplifier introduced by the effects of the circuit layout. Final layout plots are shown on the following pages plot 3.1 thru 3.3. Note, that for testing purposes the three stages of the op-amp are separated to isolate errors introduced by a single stage of the device. These are shown on plots 3.4, 3.5, 3.6.

The three different plots of the op-amp are for the Pwell CMOS process, plots 3.1 and 3.2 and the Nwell CMOS process plot 3.3. The

different processes will still yield similar operational amplifiers if the same parameters for processing, listed earlier, are met.

## Chapter 4 Processing

### 4.0 Introduction

The fabrication of the CMOS test chip and Operational Amplifier was performed at the Microelectronic Engineering fabrication facility at RIT, by Edward Sayre and Robert Pearson. The CMOS process was adapted to RIT using an existing CMOS process developed at the University of California, Berkeley. The use of an existing process with some modifications to suit RIT's manufacturing constraints would enable the comparison and provide the guidance of a working process. The modifications made to the process were to simplify and to adapt it to RIT's fabrication facilities. This chapter will discuss the fabrication of RIT's CMOS process along with any difficulties and results. The cross sections which will pictorially describe the CMOS process are provided in Appendix 2. In addition the detailed descriptions of the process steps that will be discussed further on in this chapter are presented in Appendix 3.

### 4.1 Process

The CMOS process is a P type well CMOS process also known as P-WELL CMOS. It is one type of the three CMOS processing configurations, the other two types are N-Well and Twin tube CMOS. The Nwell is simply the inverse of the Pwell structure and Twin Tube CMOS is the definition of both an N well and a P well in an

intrinsic or very lightly doped substrate, usually an epitaxial layer on a heavily doped substrate.

The RIT Pwell CMOS process starts with an N type phosphorous doped substrate with a resistivity of 5-8  $\Omega\text{-cm}$ . After an initial oxide growth of approximately 1000 $\text{\AA}$  the N- punch through implant is performed at an energy of 145Kev and a dose of 1E12 atoms/cm $^2$ . The exposure and development of the first level mask, clear field, of the Pwell uses a photoresist coat of 1 to 1.5 $\mu\text{m}$  thick. The resist will be used as an implant block over the regions outside of the Pwell. The Pwell implant uses the Boron 11 ion of the boron ion species, with an implant energy of 80 Kev and a dose of 3E12 atoms/cm $^2$ . The photoresist is striped in an oxygen plasma, cleaned, and the wafers are annealed at 1000°C in a Nitrogen environment. The sacrificial oxide layer originally grown is removed with a buffered hydrofluoric acid, BHF, dip before the drive in of the Pwell. The drive in begins with a 4 hour step in dry oxygen environment at 1150° C, then 5 hours in nitrogen at the same temperature. This should yield a P-type region with a sheet resistivity of,  $p_s = 14\text{K} \Omega/\text{i}$  and a junction depth of 3-3.5  $\mu\text{m}$ . The oxide layer, over the Pwell is targeted for a thickness of 3000 $\text{\AA}$  and over the N substrate at 3200 $\text{\AA}$ , is etched in the BHF until the surface becomes hydrophobic.

A pad oxide of 200 $\text{\AA}$  is needed before the silicon nitride SiN<sub>3</sub> layer is deposited. The nitride layer is deposited by Low Pressure Chemical Vapor Deposition, LPCVD, at a temperature of approximately 800° C with a temperature gradient of 5°/inch across the furnace tube. The target thickness of the nitride layer is 1000 $\text{\AA}$ .

The second masking level of the process is the definition of the active areas in the Silicon nitride layer for the LOCOS process step. The Active level is patterned on the nitride with photoresist then dry etched in a plasma of CF<sub>4</sub>. Immediately following the nitride etch resist is applied to the wafers and imaged with the third level mask, identical to mask level 1.

The P- field adjust implant of Boron (11) at an energy of 100 Kev and a dose of 1E13 atoms/cm<sup>2</sup> is implanted into the active areas outside of the remaining nitride layer. The strip of the two (2) photoresist coats is performed in an oxygen plasma followed by another photoresist coat and exposure of the N- field areas. The fourth level mask is the inverse of mask level 3 which is a dark field mask. The N- field adjust implant is performed with an implant energy of 40 Kev and a dose of 4E12 phosphorous (31) atoms per square centimeter.

The Localized oxidation step or LOCOS is performed after masking level four's resist is striped. The LOCOS step defines the field oxide from the active areas by thick and thin oxide regions. The thick oxide is grown during the LOCOS oxidation of 5 minutes in a dry oxygen, 4 hours 40 minutes in steam, 5 minutes again in dry oxygen, and a final anneal of 20 minutes in nitrogen and is targeted at a thickness of 6500Å. The junction depth of the Pwell will move deeper into the wafer from the thermal process steps to about 3.7 µm. The nitride is striped by first etching any oxy-nitride layer formed on the nitride with a short BHF dip, then the complete removal of the nitride layer in a CF<sub>4</sub> plasma. The pad oxide grown under the nitride layer is removed in BHF and a Kooi oxide layer of

200Å thick is grown which will also be used during the threshold adjust implant to protect the silicon surface. The Threshold voltage adjust implant is a blanket implant of Boron 11 at an energy of 35Kev with doses ranging from 3-5E11 atoms/cm<sup>2</sup> across the lot. This variance of the implant dose will allow the RIT CMOS process to pin point the threshold voltages at 1 and -1 for the N and P channel devices respectively.

Following the kooi oxide strip in BHF the gate oxide is grown in dry oxygen at 950°C for 1.5 hours with a target thickness of 500Å. It is recommended that a TCA clean of the oxide tube be performed before this and the other oxide growth steps. Immediately following the gate oxide growth the polysilicon layer should be deposited. It is important to either process the gate oxide and poly in the same tube if possible or move the wafers from the oxide tube directly into the polysilicon deposition tube or chamber.

The polysilicon layer is deposited by a Low Pressure Chemical Vapor Deposition process at a temperature of 610°C with a target thickness of 4500Å. The poly is doped by a N type spin on dopant, since RIT does not have insitu-doping of the poly layer during deposition, and ion implantation would result in a long throughput time for a normal lot of 25 wafers. The spin on dopant is predeposited at 1000°C for 20 minutes in an oxygen environment. This should yield a poly sheet resistivity of approximately 22 Ω/È.

The gate definition mask, level 5, used to pattern the poly layer is imaged onto the polysilicon with photoresist. The poly is etched in a dry plasma of SF<sub>6</sub> and oxygen. The resist is then striped and the wafers are cleaned in the RCA clean solutions. During the

clean the wafers should not be dipped in the 10:1 HF for more than 10 second so as not to contaminate or undercut the gate oxide.

Following the clean a thermal oxide is grown over the polysilicon and the silicon substrate with target thicknesses of 800Å and 500Å respectively. This oxide will help protect both surfaces from the subsequent drain/source implants for the active devices. The P type drain/source implant mask, dark field, is the sixth masking level of the process. It masks out all regions except for the active areas where the B+ and BF<sub>2</sub>+ ions are to be implanted. Since this process is self aligning the poly gate will be exposed to the implant thus some minor counter doping will occur during the Boron implant in the heavily doped N type poly. The P+ type drain/source implant has an energy of 50Kev and a dose of 2E15 atoms/cm<sup>2</sup>.

The N+ type drain/source implant occurs after the photoresist has been striped, coated and the inverse image of mask level 6, level 7 is transferred to the wafers. The N+ implant is a phosphorous implant with a energy of 50 Kev and a dose of 3E15 atoms/cm<sup>2</sup>. As with the P+ implant the devices are self aligning but the poly gate will be more heavily doped for the N channel devices. The sheet resistances of the N+ and P+ source/drain implants are 24 Ω/È and 46 Ω/È respectively.

Spin on glass, SOG, is used as a dielectric layer between the polysilicon layer and the metal one. The densification of the SOG is also used to drive in the source and drain regions of the two device types along with annealing the wafers from the recent implant. A

densification of 1 hour at 1000° C should yield a target SOG thickness of 6000Å.

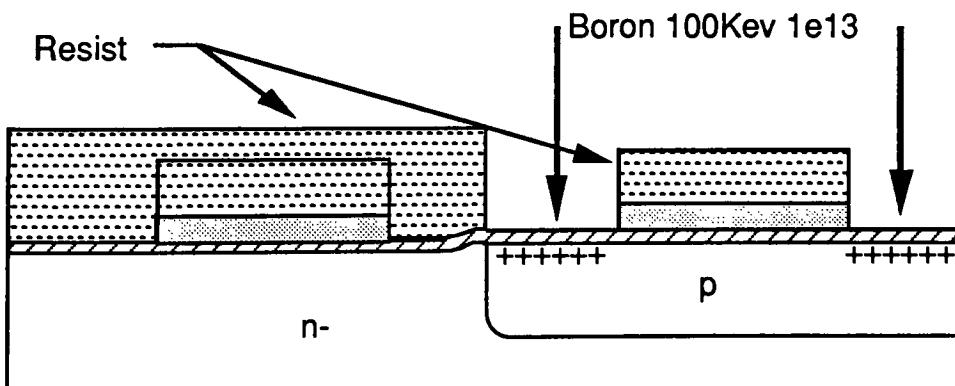
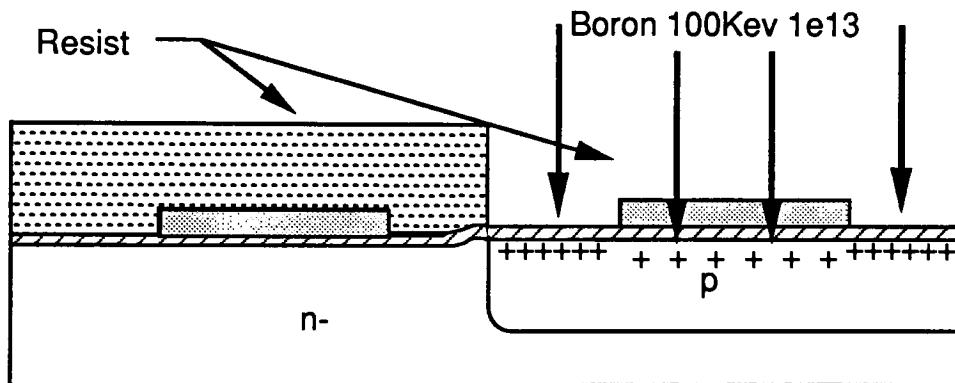
Mask level eight is utilized to pattern the SOG with the contact cut pattern before etch. The SOG is etched in BHF to create the contact holes for the interconnection of the various devices in metal one. The evaporation of 3 pellets of Aluminum and 2% silicon should be sufficient to yield a thickness of 3500Å of metal on the wafer surfaces. The metal is then patterned with mask level 9, clear field, and etched in a wet aluminum etch solution. Finally the wafers are striped of photoresist, sintered at 425°C for 40 minutes, and are ready for testing.

#### 4.2 Results

The results of the first Pwell CMOS process did not show that a successful processing run had been manufactured. The erroneous behavior of the electrical structures used to characterize the CMOS process did not point to one single problem with the process or processing but perhaps several problems. It was difficult to isolate the process problems based exclusively on test structures. Upon closer inspection of the laboratory process data sheets some process steps which were not identical to the correct process steps adapted from the Berkeley process.

#### 4.2.1 Field Adjust Implant

The first divergence from the designed process was during the P- field threshold adjust implant. After the initial nitride pattern and etch the photoresist was stripped from the wafers. The following process step was to coat, expose and then implant with the P- type field implant. The photo resist that was strip was needed to block the implant over silicon nitride layer in the Pwell. The area under which is where the N- channel devices will reside. A cross sectional view of the processing error is shown in figure 1a, the correct cross section is shown in figure 1b.



Figures 1a and b ; divergence from process cross sections

The end result was that the implant penetrated the nitride layer and increased the impurity profile within the active area in the Pwell. The impact of this process error would be to shift the threshold voltage of the NMOS device to a more positive voltage. The error in device performance caused by a variance in the threshold voltage will be minimal and should not cause catastrophic failure.

#### 4.2.2 Polysilicon Doping

The process developed to dope polysilicon would prove to be a crucial procedure and effect the device performance significantly. In the RIT CMOS process an intrinsic polysilicon layer is deposited by LPCVD which must be doped for use in the various circuits as an interconnect and gate material. The Doping of this layer utilized a spin on N type dopant. The dopant, N-250, was spun on prebaked and a predeposit at 1000° C for 20 minutes. The doping of polysilicon initially occurs along the grain boundaries of the film then diffusing into the grains of the polysilicon. The initial diffusion along the boundaries of the grains will occur within the first few minutes of the predepostion step, thus exposing the thermal gate and field oxides to a high level of impurities.

An in process study which doped polysilicon to create MOS capacitors did not yield working capacitor structures. Various times and temperatures were investigated all yielding unsatisfactory results. The leakage current of the capacitors did not satisfy the criteria that at DC a capacitor is an open circuit. The results from this study were not investigated fully due to the

time constraints and materials needed for processing. It is believed that the high temperature allowed the phosphorous to diffuse through the thermal oxide layer used for a gate dielectric in the MOS structures. The final result of any subsequent high temperature process steps would also allow this behavior which will cause catastrophic failure of both types of transistor structures.

The process of polysilicon doping had not been utilized by any of the existing processes at RIT. In addition the process defined by Berkeley, which was being used as a reference, introduced the impurities during the deposition of the polysilicon layer which is known as an insitu-polysilicon doping process.

The error introduced by the long high temperature predeposition step could lead to a catastrophic failure of the transistor devices. This conclusion is substantiated by the brief study mentioned. In addition any subsequent high temperatures would continue the degradation of the thermal oxides immediately under the poly and continue to redistribute impurities already in the oxide layer.

#### 4.2.3 Phosphorous D/S doping

The drains and sources of the CMOS devices were created by ion implantation of either Boron and BF<sub>2</sub>, for the P-channel devices, or phosphorous, for the N channel devices. The N type D/S ion implant energy was altered from the specified value during the processing. An implant energy of 50 Kev was specified but 100 Kev was actually used during the processing. The impact of this upon the

operation of the transistor devices could result in further degradation of the oxide under the N channel device. The isolation and detection of is error in the process steps is difficult when compounded with the polysilicon doping problems.

#### **4.2.4 Photo resist scumming**

During the source and drain implants of the two types of devices a photo resist layer is used to block the implant from areas where no impurities are specified. The importance of a descum process step is made evident by the problem discovered after the final resist strip following the N type S/D implant. As seen in figure 2 the polysilicon layer was covered by a layer of "scum". This scum layer was determined to be a result of residual photoresist layer which when heated from the high energy of an ion implant baked on to the polysilicon. This difficulty during processing will not greatly effect the device performance but will effect any subsequent lithography or possibly etch steps. If the scumming reduces the etch rate for some of the contact cuts then good contacts not effected by the scumming will be over etched. This will present a problem for small geometry devices but will not impact upon those used in the design of the CMOS operational amplifier.

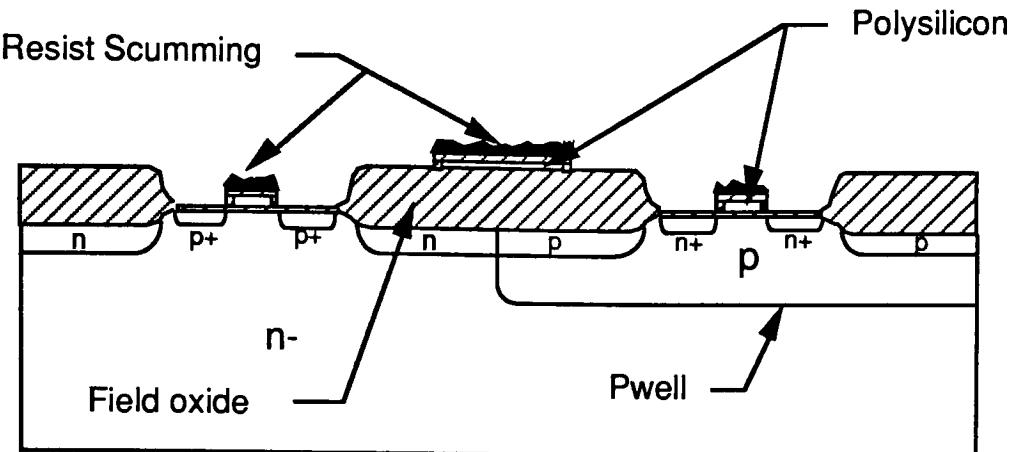


Figure 2; polysilicon scumming

#### 4.2.5 Non uniform Spin on glass

The RIT CMOS process utilizes a spin on glass layer as a dielectric material to separate the metal layer from the polysilicon layer. This SOG layer acts as a planarizing layer in addition to its dielectric qualities. During the processing of the spin on glass, which required a single application, and densification at 1000° C, the uniformity of the SOG film could be seen to be subject to non uniformity problems. Results of previous processing at RIT had shown that the uniformity problem existed but the film provides constant etch rates which other spin on glasses that were more uniform could not provide. This phenomena will not cause a catastrophic failure of a large device since the contact dimensions are not critical, but use of this type of film for small geometry devices will not yield satisfactory results.

#### 4.2.6 Large leakage currents

The testing of the CMOS test chip first examined any test structures used to characterize the process and extract parameters to determine the robustness of the process. Included in the structures are the N and P channel discrete devices, capacitors, Van der Pauw structures, etc. The preliminary results of the discrete devices show a significant leakage current through the gate of the MOS structures. When the capacitors which are the same type structure as the gate of a MOS field effect transistor were tested a significant current, of the order of milli amperes, was found to be leaking across the poly to substrate capacitors. This problem involved both the thin gate oxide and thick field oxide devices. Plots of this behavior are shown in Appendix 3.

### 4.3 Process results

In lieu of the processing difficulties experienced and some of the preliminary results the final results of the RIT CMOS process are shown in table 1. These values can be incorporated into hand calculations and circuit simulators for a more accurate estimation of device performance of any designs places on subsequent revised processing runs

Table 1: Process summary

Pwell Junction depth	3.6 $\mu\text{m}$
Pwell Sheet resistance	14 $\text{K}\Omega/\text{E}$
P+ D/S junction depth	1.1 $\mu\text{m}$
P+ D/S sheet resistance	45 $\Omega/\text{E}$
N+ D/S Junction depth	0.87 $\mu\text{m}$
N+ D/S Sheet Resistance	24 $\Omega/\text{E}$
Polysilicon Thickness	4500 $\text{\AA}$
Polysilicon Sheet Resistance	22 $\Omega/\text{E}$
Field Oxide Thickness	6000 $\text{\AA}$
Gate Oxide Thickness	500 $\text{\AA}$
Spin On Glass thickness	5000 $\text{\AA}$

Upon comparison of the process results to those extracted from the process developed by Berkeley the values in table 1 are satisfactory. Table 1 does not show the problems of the processing and thus can not be used as a measure of the success or failure of a fabrication run.

## Chapter 5 Testing

### 5.0 Introduction

This chapter will address the testability of the CMOS Operational amplifier and the integration of the op-amp into some common circuit configurations. The op-amp is replicated over one hundred times per silicon wafer in the manufacturing processes thus an expedient method of testing the operational amplifier for functionality is justified. A testing scheme can be developed from the final version of the circuit design, but for proper development of the tests for the op-amp the design for testability of the op-amp is performed at the first level of the designing process.

### 5.1 Testing

The testing of the operational amplifier will be divided into two (2) sections, the first will be the evaluation of the DC conditions, the second is the frequency response behavior of the op-amp. This testability scheme determines any devices which are defective due to a gross manufacturing difficulties, such as lithography errors and particle defects with the first section of testing. The AC operation of the op-amp is then determined from the devices which are not defective, thus reducing testing time.

### 5.1.1 DC conditions

The test to determine the proper DC operation of the op-amp will be, the Input Offset voltage, Input Common Mode Range, Common Mode Gain, and proper voltages and currents extracted from either the op-amp or individual stages.

### 5.1.2 Input Offset Voltage

The Input Offset Voltage will configure the operational amplifier into a voltage follower feedback configuration as shown in figure 5.1.

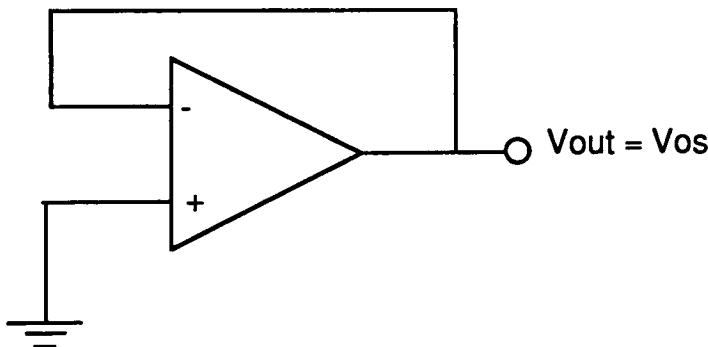


Figure 5.1 (Input Offset Voltage configuration)

The offset voltage is measured at the output of the op-amp and the negative magnitude of the measured voltage should be applied to the inverting input or the positive voltage to the non-inverting input. The goal of the input offset voltage is to achieve a condition of zero voltage applied resulting in a zero output voltage. The op-amp will incorporate the offset voltage within one of its inputs, so for

example the new inverting input is the positive node of the offset voltage source, see figure 5.2 . Typically the offset voltage is in the milli volt range but may be as large as a volt but not a great as the supply voltages, ( $\pm 6$  V).

### 5.1.3 Input Common Mode Range

The next DC test of the operational amplifier is the Input Common Mode Range, CMR. The circuit uses a similar configuration to that of figure 5.1 except the offset voltage is utilized along with an applied voltage to the non-inverting input. This can be seen in figure 5.2;

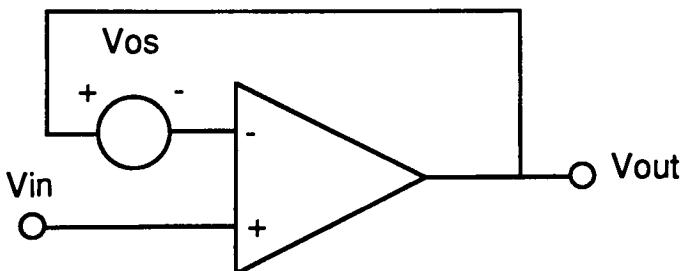


Figure 5.2 (Input Common mode range Configuration)

The voltage  $V_{in}$  is varied in a linear fashion from the negative supply voltage of -6 volts to the positive supply of +6 volts. The output should have a section in which a unity gain occurs. This region can be found by a plot of the output voltage verses the input voltage, as seen in the simulations of chapter 3. The generation of the the output voltage verse the input voltage can be performed by

measurement of the discrete output voltage for a particular input voltage. This method of data collection is automated within the parameter analyzer, HP 4145, where a plot can be generated, collected and analyzed.

#### 5.1.4 Common Mode Gain

The Common mode gain of the operational amplifier will show the asymmetries of the differential amplifier section of the device. As mentioned previously in chapters 2 and 3 the common mode gain of the amplifier should be as small as possible, preferably much less than one. The circuit configuration for measurement of the common mode gain is shown in figure 5.3.

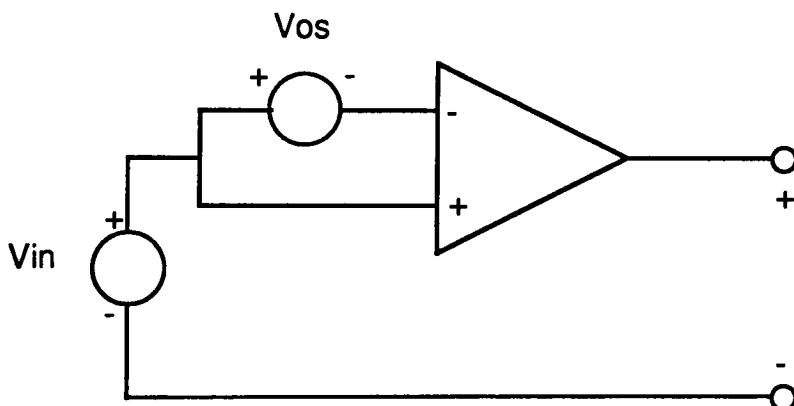


Figure 5.3

The Common Mode Voltage Gain is can be determined in a similar manner to that of the Input Common Mode Range. The test for the common mode voltage gain ties both inputs together and applies a voltage  $V_{in}$  which increases from the negative supply

voltage to the positive supply voltage, this is identical to the CMR measurement. A typical common mode gain is much less than 1, since an operational amplifier is designed to amplify the difference between the inputs and not the common component. If the common mode gain is greater than unity, the proper operation of the amplifier will be suspect. In addition to the method of determining the common mode gain in the DC region the common mode frequency response can be utilized to determine the gain and a comparison can be made.

The Common mode voltage gain is a measure of the quality of the amplifier design, in particular the differential amplifier section. In addition, the common mode gain provides a process engineer with information about the variations in the manufacturing process. The common mode component of the amplifier occurs as a result of any asymmetries in the differential pair, as discussed in chapters 2 and 3, and thus can show any variations across a wafer and through a wafer lot.

### 5.1.5 Power dissipation

The design specification of the CMOS op-amp limits the amount of power that can be dissipated by the device. As one of the performance criteria of the amplifier, the total power consumed by the operational amplifier must be less than 0.96 mW. The total power is also a measure of the quiescent operating point of the amplifier since the power is directly related to the current flowing through the device. The simulated power dissipated with supply

voltages of  $\pm 6$  volts is 0.842 mW which is equivalent to a supply current of  $\approx 70 \mu\text{A}$ .

The measurement of the supply current can be performed by either a hall effect current probe or a power supply with the capability of power or output current measurement.

### 5.1.6 Output Voltage Range

The output voltage range of the operational amplifier can be tested within the DC domain. The output voltage range is the maximum output swing that can be obtained without a significant amount of distortion for a typical load resistance. The magnitude of a typical load is in the mega ohm range for a resistive load and in the pico farad range for a capacitive load.

The method of testing the output voltage swing is relatively simple since only two states need be addressed for the test. Grounding the non-inverting input and applying a positive voltage at the upper bound of the input common mode range to the inverting input will determine the lower bound of the output range. Similarly, applying the negative voltage at the lower bound of the CMR will find the upper limit on the output range.

## 5.2 Frequency Response

The CMOS operational amplifier frequency response should be measured on those devices which passed the DC criteria for operation. Both the frequency verse magnitude and the the frequency

verses phase should be tested so the stability of the open loop system can be determined. Both input conditions of the op-amp should be measured to ensure proper operation. The frequency response of the CMOS operational amplifier can and should be tested with and without the compensation capacitance. The layout of the op-amp does not include the compensation capacitance since it requires an area that is larger than the die of the CMOS test chip containing the op-amp. An external node for the compensation is provided and labeled in the layout of the op-amp. For our purposes the operational amplifier should be tested with and without the compensation capacitor, which will allow direct comparison to the simulated data. Both methods of test are identical to one another. Also this will enable an investigation into the frequency behavior of the amplifier for different compensation capacitance values.

To properly test the open loop frequency magnitude and phase responses a high input impedance oscilloscope and a 1G Hz frequency signal generator are desired. The frequency response data is to be compared to the simulated Bode plots which cannot be generated directly with an oscilloscope but an indirect method of comparison can be developed. The differential frequency response measurement applies a small signal, within the small signal input range of  $\pm 3\text{mV}$ , to the non inverting input and channel 1 of the oscilloscope, and the output of the op-amp is connected to channel 2, shown in figure 5.4

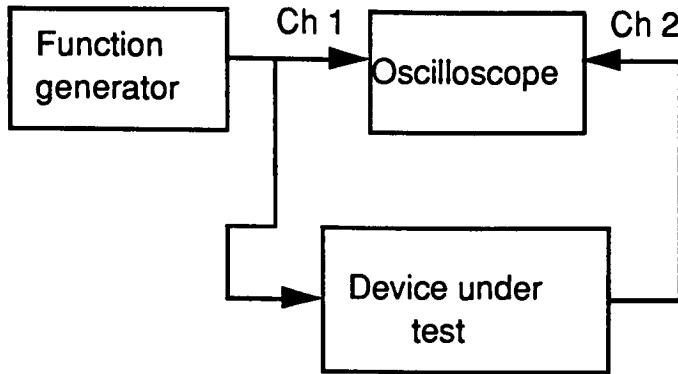
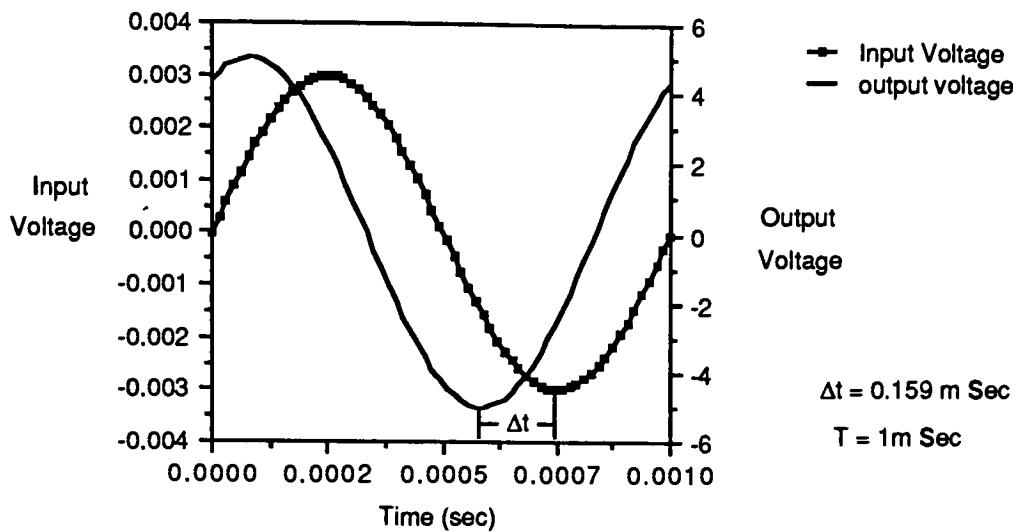


Figure 5.4

For a particular frequency and magnitude input signal the gain and phase of the amplifier can be measured from the scope, once the data is collected over the range of desired frequencies a frequency response can be formulated. The open loop common mode frequency response is measured in much the same manner the open loop differential mode is found. Instead of applying a differential type input, the input nodes will see the same input wave form and frequency thus placing the op-amp in the common mode. A demonstration of the method of frequency response data collection is documented in section 5.2.1.

### 5.2.1 Demonstration



Plot 5.1 represents the wave forms which could be displayed on an oscilloscope screen. By inspection the wave forms are out of phase and of differing magnitudes. The gain of the system at the particular input frequency can easily be determined by measurement of the peak voltages of the input and output wave forms.

$$|V_{\text{out}}| = 5 \text{ Volts} \quad \text{eq. (5.1)}$$

$$|V_{\text{in}}| = 3 \text{ m Volts} \quad \text{eq. (5.2)}$$

The gain of the system at this frequency is;

$$Av = \frac{V_{\text{out}}}{V_{\text{in}}} = 1666.67 \quad \text{eq. (5.3)}$$

The analysis of the wave forms to determine the phase of the system is not as trivial as for the gain calculation. The phase of the system is a relative measure which is made with respect to the

input wave form. The data needed from the oscilloscope is; the total period of the output and/or input wave form, assumed to be of the same frequency, and the difference in time of the two wave forms at a particular magnitude. The zero point or the difference at the peaks are typically used to obtain the shift in time of the wave forms. In this case the difference is determined to be;  $\Delta t = -0.159 \text{ m Sec}$ ; and a period of;  $T = 1 \text{ m Sec}$ . If the period is converted into frequency in Hertz, then into frequency in radians/sec, and finally multiplied by the difference,  $\Delta t$ , a phase shift in radians is established which can be converted to degrees. This method is shown below.

$$F (\text{Hz}) = \frac{1}{T} \text{ Hz} \quad \text{eq. (5.4)}$$

$$\omega = 2\pi F \frac{\text{rad}}{\text{sec}} \quad \text{eq. (5.5)}$$

$$\emptyset = \omega(\Delta t) \text{ rad} \quad \text{eq. (5.6)}$$

$$\Phi = \emptyset \frac{180}{2\pi} \text{ deg} \quad \text{eq. (5.7)}$$

By substitution into equations 5.4 through 5.7 a phase shift of  $\approx -60^\circ$  is determined for the input frequency of 1K Hz.

The methods of testability of the CMOS operational amplifier discussed are effective for the determination of the functionality of the op-amp. By comparison of the data collected from the testing to the data from the simulations and hand calculations a formulation can be made upon the success of the design and the operational

amplifier's performance. In addition the op-amp can be integrated into some basic analog circuits which also give an indication to the success of the design.

### 5.3 Individual stages

During the testing of the CMOS operational amplifier erroneous behavior can occur in either the DC or AC ranges or both. For this occurrence the op-amp layout is also divided into the three stages making up the CMOS operational amplifier; differential amplifier, output stage, and bias. The division of the op-amp will promote complete methods of fault isolation in either the design but more likely the manufacturing.

The bias section of the op-amp is susceptible to variations in the power supplies and therefore the bias current is also susceptible. The bias current is matched in the two gain stages of the op-amp and thus the overall gain of the circuit is dependant upon the proper operation of the bias stage. The testing of the bias section is strictly within the DC region of operation of the devices. By applying the supply voltages a measurement of the output voltage,  $V_{gg}$ , can be compared to the expected value of  $V_{gg} = -4.4$  V from the simulations.

The differential stage of the op-amp can be tested with the same methods as the entire operational amplifier for both AC and DC behavior. The bias voltage  $V_{gg}$  must be supplied externally for the current source of the differential stage. The variation of  $V_{gg}$  can be

used to optimize the gain of the differential stage for the particular design specifications of the operational amplifier design.

The output stage of the operational amplifier is similar to the testing strategy of an inverter. Again, as with the differential stage, the bias voltage  $V_{gg}$  can be varied to optimize the gain of the output stage. Individually the optimum gains of the two stages can be attained for different bias voltages. But since only one bias can be supplied in the final op-amp design,  $V_{gg}$  must be set to optimize both the dif-amp and the output stage with the same voltage. The optimized bias voltage can then be integrated into further design revisions and processing runs. Both the DC and AC regions of operation of the output stage should be investigated to determine any erroneous behavior that this stage can introduce.

#### 5.4 Common Circuits

In any analog type circuit the most vital element of the design is an amplifier which is made up of an operational amplifier. As a final method of test the op-amp is integrated into commonly used analog amplifier circuits. To demonstrate the validity of the design and operation of the CMOS operational amplifier a variety of elementary amplifier circuits have been designed and simulated using S.P.I.C.E. These simulations can be measured using existing test methods for the operational amplifier discussed previously in this chapter. The circuits comprise of an integrator, differentiator, unity gain amplifier, and a amplifier with gain of 100. All but the differentiator are commonly used in design of an analog systems.

The SPICE input decks used for the simulations are provided in Appendix 4.

### 5.4.1 Integrator

The analog integrator is very useful when used in signal processing applications. The integrator shown in figure 5.5 employs a miller capacitance feed back scheme and the operational amplifier. For a small signal input,  $V_{in}$  the output will be the integral of the input.

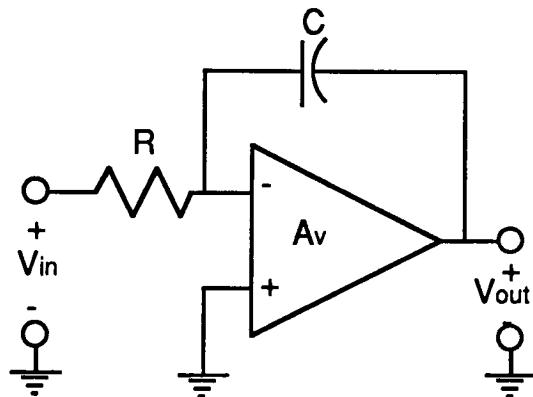


Figure 5.5

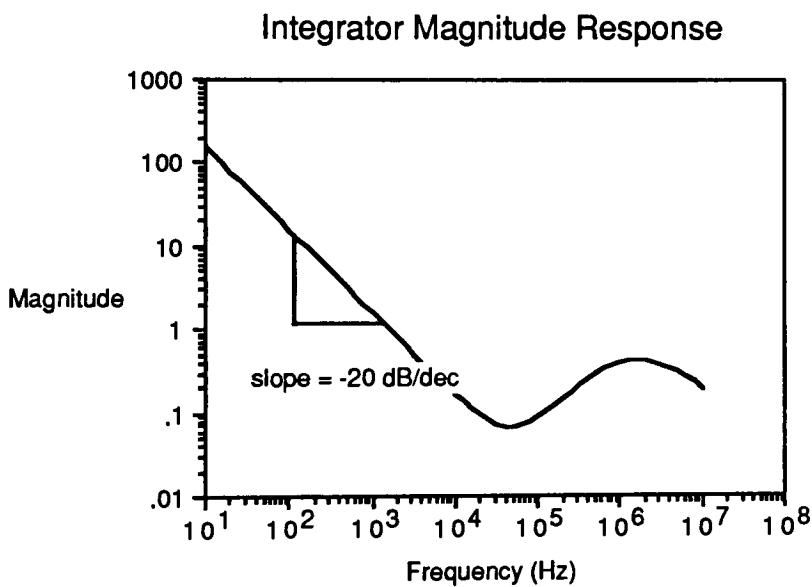
By circuit analysis a relation between the input and output voltages can be derived to be;

$$V_o = \frac{-1}{RC} \int V_{in} dt \quad \text{eq. (5.8)}$$

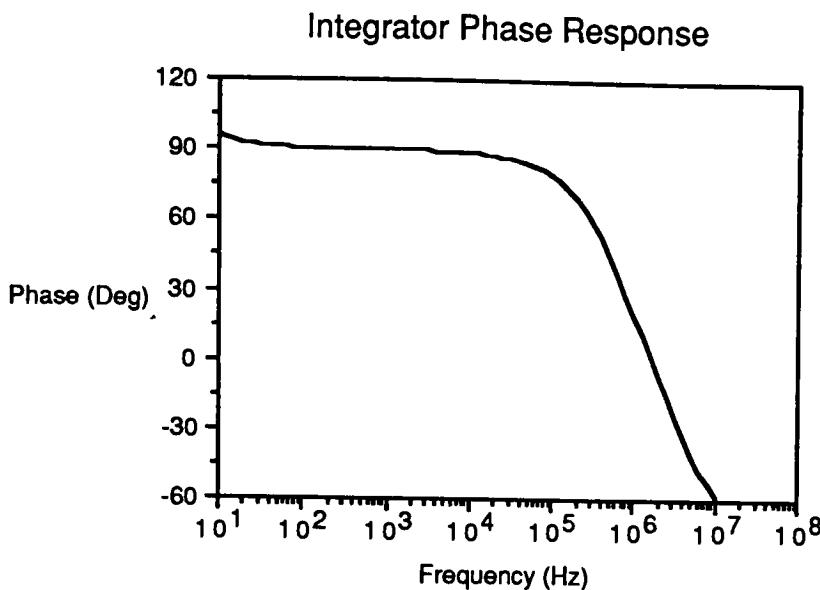
By inspection of equation 5.8 the output voltage can be seen to be the time integral of the input voltage, thus an integrator. The transfer function of the integrator is shown in equation 5.9

$$Av = \frac{V_o}{V_{in}} = \frac{-1}{RCS} \quad \text{eq. (5.9)}$$

Now, if values for the gain and either the resistor R or capacitor C a simulation of the integrator can be performed. If we chose a DC gain of  $Av(0) = 10,000$  and a capacitor value of  $C = 100$  pico Farads a value for the resistor is found to be ;  $R = 1E6 \Omega$ .



Graph 5.1



Graph 5.2

Graphs 5.1 and 2 show the simulated frequency responses of the integrator circuit. The Magnitude response does not include the DC gain but by extrapolation the simulated DC gain is approximately 10,000. Another comparison to the hand calculations is the determination of the gain at a particular frequency. If we chose a frequency of 10 Hz the gain is calculated to be  $A_v(10) = 159.2$  as compared to the simulated gain of  $A_v(10) = 158.0$ . By inspection of graph 5.1 the magnitude response of the integrator behaves as expected with a -20dB/decade slope. At 10 KHz the circuit no longer behaves as an integrator due to poles introduced by the non ideal op-amp. Thus for frequencies below 10 KHz a predictable response can be determined for this integrator circuit in figure 5.5. The phase response of the integrator in graph 5.2 shows expected results within the frequency of 10 KHz. The phase response also

demonstrates that the integrator is a stable system and thus the CMOS op-amp can be used in a closed loop stable system.

#### 5.4.2 Differentiator

The reciprocal circuit element to the integrator is the differentiator. The differentiator is not as widely used in analog designs as the integrator but it is a primitive element that will add to the demonstration of the CMOS operational amplifier as a circuit element. The differentiator circuit is of the form shown in figure 5.6.

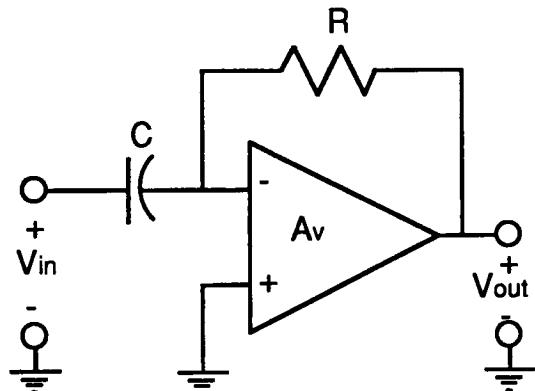


Figure 5.6

By nodal analysis of figure 5.6 a relation in the time domain can be attained to be;

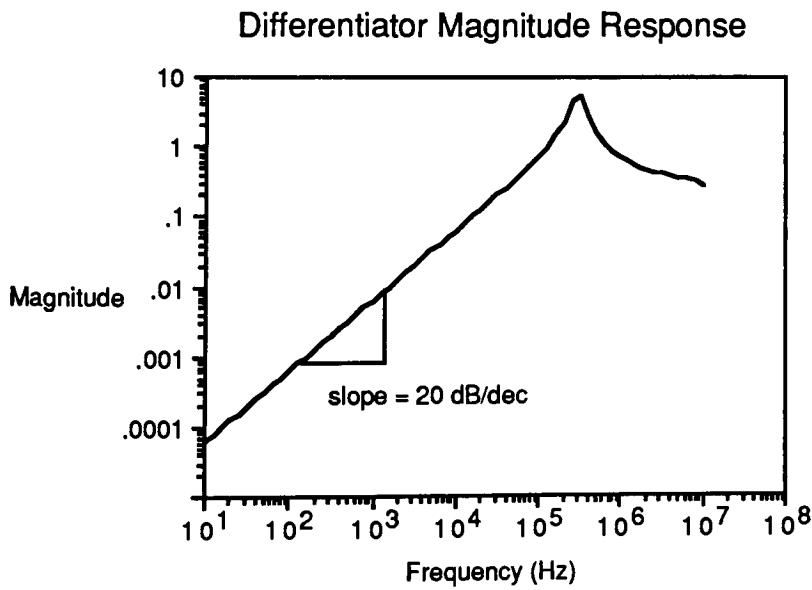
$$V_o = -RC \frac{dV_{in}}{dt} \quad \text{eq. (510)}$$

By inspection of equation 5.10 it can be seen that the output of the circuit is the derivative of the input voltage, thus a differentiator

circuit. The transfer function of the differentiator is simply expressed in equation 5.11

$$\frac{V_o}{V_{in}} = -RCS \quad \text{eq.(5.11)}$$

To simulate the differentiator circuit values for the resistor, R, and capacitor, C, can be specified. If we chose  $R = 1E6\Omega$  and  $C = 1$  pico Farad a DC gain of  $A_v=1E-6$  is obtained from equation 5.11. This gain is extremely small but to exploit a higher bandwidth the gain of the circuit must suffer by preservation of gain the bandwidth product. The solution to a small gain is an amplifier of a sufficient gain to resolve the output to a suitable level. The simulation of the frequency response of the differentiator is shown in graphs 5.3 and 5.4.



Graph 5.3

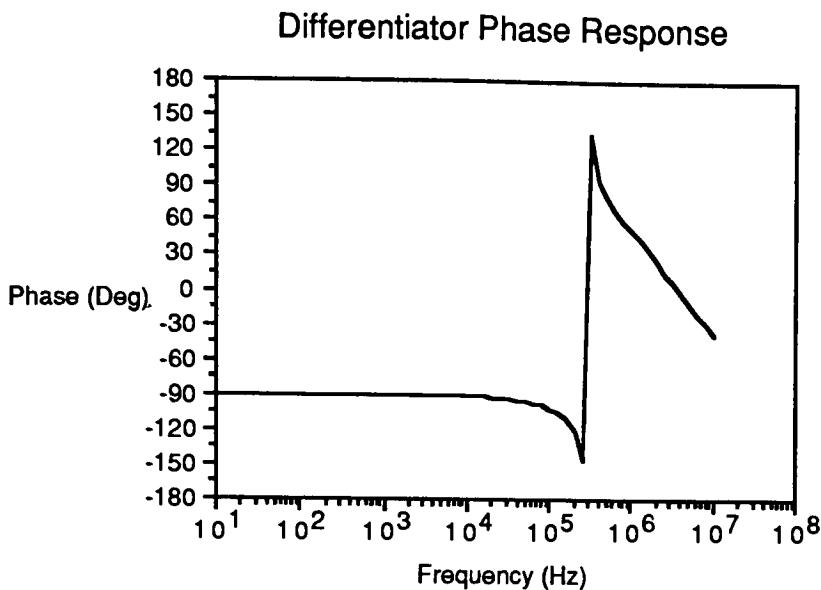


Figure 5.4

By calculation of the magnitude of the differentiator from the transfer function, eq. 5.11, at 10 Hz a comparison can be made between the hand calculations and the simulated results. The hand calculations obtains a value of,  $A_v(10) = 6.28E-5$ , and the simulated results show,  $A_v(10) = 6.277E-5$ , thus the simulations are valid estimates of the circuits performance.

The phase response of the differentiator shows a system whose stability is susceptible to noise perturbations of frequencies greater than 0.25 M Hz. This is not unusual for the type of direct feedback chosen for the differentiator.

#### 5.4.3 Gain Stages

As previously mentioned the use of a gain stage in an amplifier is very useful for signal processing applications, such as the

differentiator circuit which requires a large gain. The gain stage can be used to isolate one stage from another by the use of a unity gain stage, or to amplify an output to proper voltage levels for any subsequent inputs. The unity gain amplifier and an amplifier with some gain greater than one, are of the same circuit configuration as shown in figure 5.7.

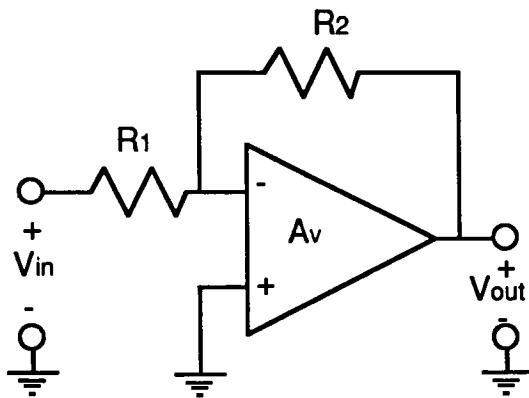


Figure 5.7

The derivation of the transfer function must concern itself with the fact that the operational amplifier is not ideal thus there is some error introduced. By nodal analysis at the inverting input and equation 5.12 the transfer function is derived and shown as equation 5.13.

$$V_o = V A_v \quad \text{eq.(5.12)}$$

Where  $V$  is the voltage at the inverting input of the op-amp.

$$\frac{V_o}{V_{in}} = \frac{-\frac{R_2}{R_1}}{1 - \left(\frac{R_2}{R_1}\right)\left(\frac{1}{A_v}\right)} \quad \text{eq.(5.13)}$$

The transfer function shown in equation 5.13 shows the error term in the numerator to be;

$$\text{Err} = \left(\frac{R_2}{R_1}\right)\left(\frac{1}{A_v}\right) \quad \text{eq.(5.14)}$$

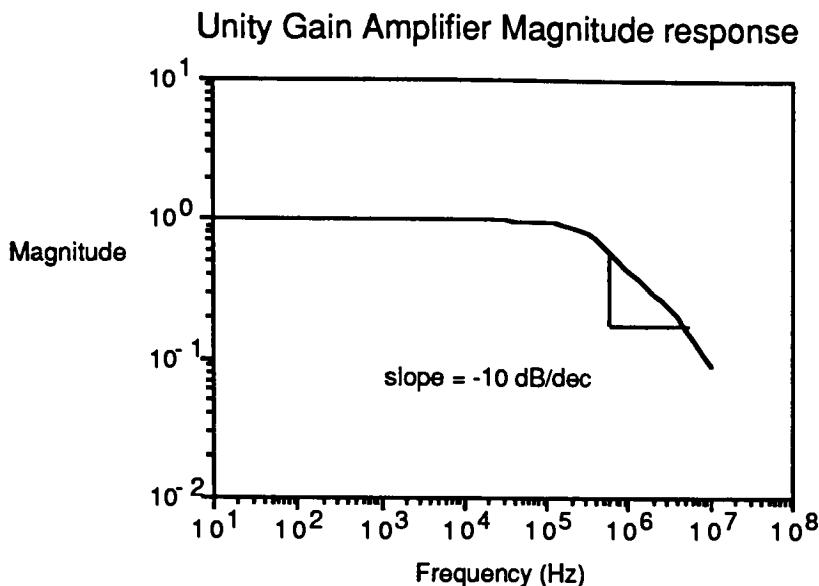
For the case where the operational amplifier is ideal the gain is much large than  $\frac{R_2}{R_1}$  and will force the error term to zero and the gain of the transfer function to the ideal case of;

$$\frac{V_o}{V_{in}} = -\frac{R_2}{R_1} \quad \text{eq.(5.15)}$$

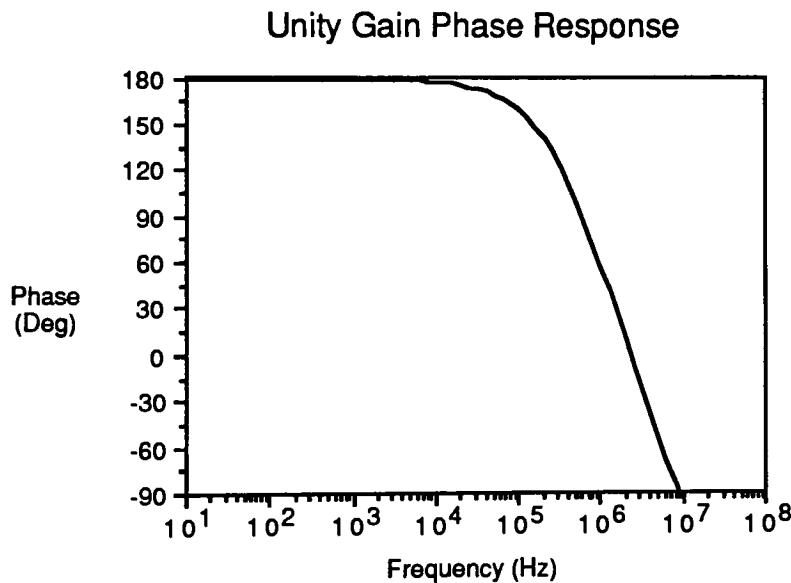
The simulations of the gain amplifier will be performed for a unity gain amplifier and an amplifier with a gain of 100. The forward differential open loop gain of the operational amplifier is  $A_{v,d} = 1645$  as determined in chapter 3. The calculation of the resistor values for the unity gain amplifier simplifies equation 5.12 to equation 5.16.

$$R_2 = R_1 \quad \text{eq.(5.16)}$$

If we choose  $R_1$  and  $R_2$  to be 1 Mega  $\Omega$  the frequency response is simulated and shown in graphs 5.5 and 6.



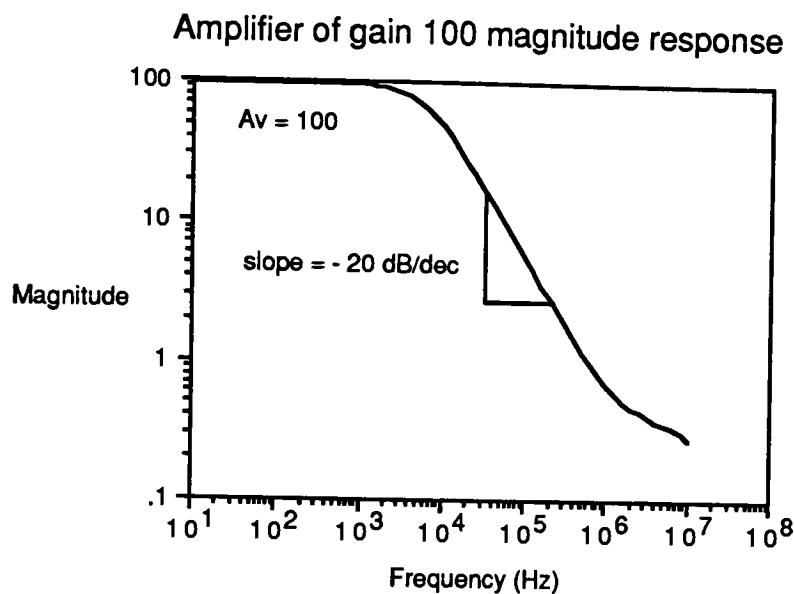
Graph 5.5



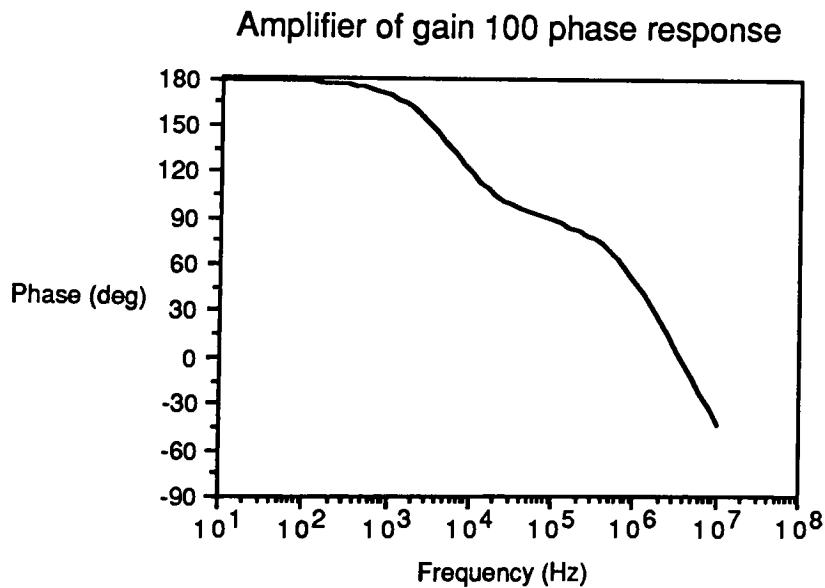
graph 5.6

For the amplifier of gain 100 the derivation for the resistor values will not yield resistor  $R_2 = 100 R_1$  due to the error factor. For a gain of 100 and a resistor  $R_1 = 10 \text{ k}\Omega$ ,  $R_2$  is equivalent to  $1.07 \text{ M}\Omega$

from equation 5.14. The simulated frequency response of the the amplifier is shown in graphs 5.7 and 8 below.



Graph 5.7



Graph 5.8

By comparison of graphs 5.7 and 5.8 it can be seen that the bandwidth of the unity gain response is larger than that of the gain of 100. This can again be attributed to the preservation of the gain bandwidth product for amplifiers which are the same circuit configuration.

## 5.5 Summary

Within this chapter a testability scheme was developed for the CMOS operational amplifier. By interconnection the op-amp in various open and closed loop configurations of the DC and AC behavior can be tested. All of the simulated data of chapter 3 can be confirmed with the use of these test structures. In addition to the testability scheme for the operational amplifier, various elementary analog circuit applications were developed to ensure the functionality of the op amp in a closed loop system. The simulations performed show a high level of confidence in the op-amp for applications in the audio frequency ranges.

## Chapter 6 Conclusions

The goal of this thesis was the design, fabrication and test of a CMOS operational amplifier. The design of the op-amp included the evaluation of the individual stages of the amplifier and the impact of their behavior on the whole operational amplifier circuit. The CMOS process was originally developed by University of California at Berkeley and adapted for Rochester Institute of Technology's Microelectronic Fabrication Facilities. The testability scheme implemented for the operational amplifier gives the ability for the performance parameters of the op-amp to be tested and easily compared to the specified and simulated values.

The division of the CMOS operational amplifier into the individual stages allows for simple and easily handled derivations of the parameters for each stage. Within chapters 2 and 3 it was determined the performance of the operational amplifier for both the large and small signal analysis. The majority of the important data and parameters such as the differential and common mode voltage gains were derived in the small signal analysis. The equations describing the different modes of operation of the amplifier were presented in both the small signal parameters as well as the device parameters which can be seen in both chapters 2 and 3.

The overall response of the operational amplifier from the individual stages is formulated within chapter 3. Also, the frequency response for the magnitude and phase of the op-amp were derived and simulated in chapter 3. The results show that the

frequency response of operational amplifier is determined by the parasitics of the individual transistors making up the amplifier. From the Bode plots it can be seen that the uncompensated op-amp needed a compensation scheme to allow the amplifier to conform with the operating specification. The method of compensation was a lead compensator which is realized as a capacitor on the output of the dif-amp stage. The use of compensation is vital to the stability of the amplifier to be utilized in the closed loop stable configuration.

The fabrication of the CMOS operational amplifier was performed at RIT with an adapted process originally designed by University of Cal. Berkeley. The CMOS process is described as a P type Well process with polysilicon gate material. A detailed description of the process steps has been provided in chapter 4 and appendix 2 and 3. The results of the first complete run produced non working devices. The testing of the discrete transistor test structures yielded devices which had extremely high gate leakage currents. Resistive behavior was also seen between the sources and drains of devices with no gate voltage. Upon review of the processing steps, errors in the processing were found and can be held responsible for this erroneous behavior. The success of functional operation and testing of the CMOS operational amplifier is very slim for the fabricated devices of the first CMOS processing run. Although active transistor devices could not be tested many passive structures such as resistors, sheet resistivity structures, and various capacitors could be. These structures enabled the extraction of data for use in the simulation models for

future simulations of a CMOS device created with a similar working process.

The final aspects of this thesis are the testing of the CMOS operational amplifier and the testability scheme developed. The simulations of the operational amplifier were broken into two regions, the DC or large signal and the AC or small signal. The testing of the op-amp is broken into these two regions for simplicity and ease of comparison to the simulated data.

The method of testing the op-amp is to first test the device for the large signal parameters such as Input Common Mode Range, Input Offset Voltage, the Common Mode Gain, and the power dissipation of the amplifier. This will allow the isolation of those devices which do not operate correctly from the second pass of tests in the small signal AC range. The AC analysis of the operational amplifier is divided into two areas again the first studies the open loop behavior of the op-amp. The second is the closed loop behavior of those devices which pass both the DC and the open loop specifications. The operational amplifier is then integrated into a number of elementary analog circuit configurations. If the operational amplifier performs correctly the device can be considered a working device and the design a success. This has been accomplished in chapter 5 at the simulation level with much success; thus supporting the fact that the CMOS operational Amplifier design is robust and within specifications.

## **Appendix I**

### **Simulations of open loop DC and AC response**

TITLE OPAMP VOS

## \*\*\*\*\* CIRCUIT DESCRIPTION

```

* INPUT OFFSET VOLTAGE
* TRANSISTORS ARE DRAIN GATE SOURCE SUBSTRATE
*
*.SUBCKT OPAMP 1 2 3 4 9
*
* DIFFERENTIAL AMP
R1 6 20 7 7 NDEV L=10U N=15U
R2 5 4 7 7 NDEV L=10U N=15U
R3 6 6 1 1 PDEV L=10U N=20U
M4 5 6 1 1 PDEV L=10U N=20U
R5 7 8 2 2 NDEV L=10U N=30U
*
Ccomp 5 6 200PF
*
* OUTPUT STAGE
M6 1 5 9 1 PDEV L=10U N=15U
M7 9 8 2 2 NDEV L=10U N=30U
*
*
* VOLTAGE DIVS
R8 10 10 1 1 PDEV L=10U N=12U
R9 11 11 10 10 PDEV L=10U N=12U
R10 8 8 11 11 PDEV L=10U N=12U
R11 8 8 2 2 NDEV L=10U N=30U
*
*
*
VOS 3 20 DC 0
*
.ENDS
*
* POWER SUPPLIES
*
VDD 1 0 DC 6
VSS 2 0 DC -6
*
* INPUT SIGNALS
*
VINP 4 0 DC 0
*
*
X1 1 2 9 4 9 OPAMP
*
.OPTIONS LINPTS=6000 ITLI=5000 PIYOL=1E-15
*
*.NODTH OUT=80
*
* MODELS
*
.MODEL NDEV NMOS LEVEL=2 LD=0.4U TOX=500E-10 NSUB=1E+16 UTO=1.0
+GMIN=1.3379 PH1=0.6 W0=600 MEXP=0.0 UCrit=1.0E6 UTRA=0.0
+DELTA=1.2405 WMAX=1E+5 NJ=0.87U LAMBDA=0.02 MFS=2E+11 MEFF=1.001E-2
+MSS=0.0 TFB=1.0 RSH=22 C000=350E-12 C000=200E-12 C000=350E-12 CJ=300E-6
+NJ=0.5 CJSU=500E-12 NJSU=0.3
*
.MODEL PDEV PMOS LEVEL=2 LD=0.5U TOX=500E-10 NSUB=1E+15 UTO=-1.0
+GMIN=0.070003 PH1=0.6 W0=450 MEXP=0.0 UCrit=1.0E6 UTRA=0.0
+DELTA=1.53031 WMAX=1E+5 NJ=1.0U LAMBDA=0.02 MFS=1.5E+11 MEFF=1.002E-2
+MSS=0.0 TFB=1.0 RSH=65 C000=550E-12 C000=200E-12 C000=550E-12 CJ=150E-6
+NJ=0.5 CJSU=400E-12 NJSU=0.25
*
.END

```

TITLE OF INPUT VOS

\*\*\*\*\* MOSFET MODEL PARAMETERS

	MDEV	PDEV
LEVEL	MNDS	PDNS
TPG	2	2
LB	-1	
UTG	100.00000E-09	500.00000E-09
KP	1	-1
SSMM	55.236300E-09	31.876290E-09
SSMH	1.3596	.879003
PHI	.6	.6
LAMBDA	.02	.02
RSH	.22	.75
CJ	300.00000E-06	150.00000E-06
CJSR	500.00000E-12	400.00000E-12
NLSH	.9	.25
CCFO	350.00000E-12	350.00000E-12
CCDO	250.00000E-12	250.00000E-12
CCSD	200.00000E-12	200.00000E-12
NEUB	10.00000E+15	10.00000E+15
NEC	0	0
NEF	200.00000E+00	150.00000E+00
TOK	50.00000E-09	50.00000E-09
TLJ	870.00000E-09	1.00000E-06
UD	000	130
UCIT	1.00000E+06	1.00000E+06
VMRR	100.00000E+03	100.00000E+03
MEFF	.01001	.01002
DELTA	1.2405	1.53031

\*\*\*\*\* 11/07/90 \*\*\*\*\* PSpice 4.04 - July, 1990 \*\*\*\*\* 20:19:57 \*\*\*\*\*

TITLE OF PSPICE VOS

\*\*\*\*\* SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

---

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
( 1)	0.0000	( 2)	-6.0000	( 4)	0.0000	( 9)	-0.0000
( XI.5)	3.9065	( XI.6)	4.3146	( XI.7)	-1.6018	( XI.8)	-1.3923
(XI.10)	2.5358	(XI.11)	-0.9289	(XI.20)	-0.0000		

VOLTAGE SOURCE CURRENTS  
NODE CURRENT

VDD	-7.014E-05
VSS	7.014E-05
VINP	0.000E+00
XI.VOS	0.000E+00

TOTAL POWER DISSIPATION 0.42E-04 WATTS

JOB CONCLUDED

TOTAL JOB TIME 5.17

TITLE SPWPF.CIR

CIRCUIT DESCRIPTION

```

***** INPUT COMMON MODE RANGE
*
* TRANSISTORS HAVE DRAIN GATE SOURCE SUBSTRATE
*
* .SUBCKT SPWPF 1 2 3 4 9
*
* DIFFERENTIAL AMP
R1 6 20 T 7 NDEU L=10U N=15U
R2 5 4 7 7 NDEU L=10U N=15U
R3 6 6 1 1 PDEV L=10U N=20U
M4 5 6 1 1 PDEV L=10U N=20U
M5 7 8 2 2 NDEU L=10U N=30U
*
Ccomp 3 8 200PF
*
* OUTPUT STAGE
M6 1 5 9 1 PDEV L=10U N=15U
M7 9 8 2 2 NDEU L=10U N=30U
*
* VOLTAGE BIAS
M8 10 10 1 1 PDEV L=40U N=12U
M9 11 11 10 10 PDEV L=10U N=12U
M10 6 6 11 11 PDEV L=40U N=12U
M11 8 8 2 2 NDEU L=10U N=30U
*
M12 3 20 DC 0.00797044
*
.ENDS
*
* POWER SUPPLIES
*
VDD 1 0 DC 0
VSS 2 0 DC -6
*
* INPUT SIGNALS
*
VINP 4 0
*
X1 1 2 9 4 9 SPWPF
*
.OPTIONS LINPTS=6000 ITL1=3000 PIVTOL=1E-15
.AC VINP -6.0 6.0 0.2
.PLOT AC V(9) (-6,6)
*
.WIDTH OUT=00
*
* MODELS
*
.MODEL NDEU NMOS LEVEL=2 LD=0.4U TD=500E-10 NSUB=1E+16 VT0=-1.0
+NMN=0.3596 PHI=-0.6 UD=800 UEXP=0.0 UCINIT=1.0E6 UTRA=0.0
+DELTR=1.2405 URH=1E+5 IL=0.07U LRD0A=0.02 MFS=2E+11 NEFF=1.001E-2
+MSS=0.0 TP0=-1.0 RSH=22 CGD0=350E-12 CGDO=200E-12 CGBO=350E-12 CJ=300E-6
+RL=0.5 CSH=500E-12 RSH=0.9
*
.MODEL PDEV PMOS LEVEL=2 LD=0.3U TD=500E-10 NSUB=10.0E+15 VT0=-1.0
+NMN=0.079023 PHI=-0.6 UD=450 UEXP=0.0 UCINIT=1.0E6 UTRA=0.0
+DELTR=1.53531 URH=1E+5 KJ=1.0U LRD0A=0.02 MFS=1.3E+11 NEFF=1.002E-2
+MSS=0.0 TP0=-1.0 RSH=95 CGD0=350E-12 CGDO=200E-12 CGBO=350E-12 CJ=150E-6
+RL=0.5 CSH=400E-12 RSH=0.23
*
.END

```

TITLE: SPICE.CIR

## \*\*\*\*\* MOSFET MODEL PARAMETERS

	MDEV	PDEV
	M103	P103
LEVEL	2	2
TP0	-1	
LD	400.000000E-09	300.000000E-09
UT0	1	-1
RF	30.250000E-06	31.070230E-06
MINA	1.2500	.870003
PHI	.6	.6
LAMBDA	.02	.02
NSH	.22	.95
CJ	500.000000E-06	150.000000E-06
CJSR	500.000000E-12	400.000000E-12
CLSR	.9	.25
RS0	350.000000E-12	350.000000E-12
CR00	350.000000E-12	350.000000E-12
CR00	200.000000E-12	200.000000E-12
RS00	10.000000E+15	10.000000E+15
RS0	0	0
NFS	500.000000E+00	150.000000E+00
TON	30.000000E-09	30.000000E-09
BL	870.000000E-06	1.000000E-06
NO	000	100
ICR11	1.000000E+06	1.000000E+06
WTRH	100.000000E+03	100.000000E+03
NEFF	.01001	.01002
DELTR	1.2405	1.53831

TITLE SWPWR.CIR

\*\*\*\*\* DC TRANSFER CURVES

TEMPERATURE = 27.000 DEG C

VINP	V(0)
(V)	-6.0000E+00
-4.0000E+00	-6.0000E+00
-3.8000E+00	-6.0000E+00
-3.6000E+00	-5.8100E+00
-3.4000E+00	-5.1940E+00
-3.2000E+00	-5.2010E+00
-3.0000E+00	-5.0000E+00
-2.8000E+00	-4.7990E+00
-2.6000E+00	-4.5980E+00
-2.4000E+00	-4.3970E+00
-2.2000E+00	-4.1960E+00
-2.0000E+00	-3.9950E+00
-1.8000E+00	-3.7940E+00
-1.6000E+00	-3.5930E+00
-1.4000E+00	-3.3920E+00
-1.2000E+00	-3.1910E+00
-1.0000E+00	-2.9900E+00
-8.0000E+00	-2.7890E+00
-6.0000E+00	-2.5880E+00
-4.0000E+00	-2.3870E+00
-2.0000E+00	-2.1860E+00
0.0000E+00	-1.9850E+00
1.0000E+00	-1.7840E+00
2.0000E+00	-1.5830E+00
3.0000E+00	-1.3820E+00
4.0000E+00	-1.1810E+00
5.0000E+00	-9.8000E-01
6.0000E+00	-7.7900E-01
7.0000E+00	-5.7800E-01
8.0000E+00	-3.7700E-01
9.0000E+00	-1.7600E-01
1.0000E+01	4.4940E-02
1.1000E+01	-7.9550E-01
1.2000E+01	-5.9940E-01
1.3000E+01	-3.9930E-01
1.4000E+01	-1.9920E-01
1.5000E+01	0.9910E-01
1.6000E+01	1.9900E-01
1.7000E+01	2.9900E-01
1.8000E+01	3.9900E-01
1.9000E+01	4.9900E-01
2.0000E+01	5.9900E-01
2.1000E+01	6.9900E-01
2.2000E+01	7.9900E-01
2.3000E+01	8.9900E-01
2.4000E+01	9.9900E-01
2.5000E+01	1.0000E+00
2.6000E+01	1.0000E+00
2.7000E+01	1.0000E+00
2.8000E+01	1.0000E+00
2.9000E+01	1.0000E+00
3.0000E+01	1.0000E+00
3.1000E+01	1.0000E+00
3.2000E+01	1.0000E+00
3.3000E+01	1.0000E+00
3.4000E+01	1.0000E+00
3.5000E+01	1.0000E+00
3.6000E+01	1.0000E+00
3.7000E+01	1.0000E+00
3.8000E+01	1.0000E+00
3.9000E+01	1.0000E+00
4.0000E+01	1.0000E+00
4.1000E+01	1.0000E+00
4.2000E+01	1.0000E+00
4.3000E+01	1.0000E+00
4.4000E+01	1.0000E+00
4.5000E+01	1.0000E+00
4.6000E+01	1.0000E+00
4.7000E+01	1.0000E+00
4.8000E+01	1.0000E+00
4.9000E+01	1.0000E+00
5.0000E+01	1.0000E+00
5.1000E+01	1.0000E+00
5.2000E+01	1.0000E+00
5.3000E+01	1.0000E+00
5.4000E+01	1.0000E+00
5.5000E+01	1.0000E+00
5.6000E+01	1.0000E+00
5.7000E+01	1.0000E+00
5.8000E+01	1.0000E+00
5.9000E+01	1.0000E+00
6.0000E+01	1.0000E+00
6.1000E+01	1.0000E+00
6.2000E+01	1.0000E+00
6.3000E+01	1.0000E+00
6.4000E+01	1.0000E+00
6.5000E+01	1.0000E+00
6.6000E+01	1.0000E+00
6.7000E+01	1.0000E+00
6.8000E+01	1.0000E+00
6.9000E+01	1.0000E+00
7.0000E+01	1.0000E+00
7.1000E+01	1.0000E+00
7.2000E+01	1.0000E+00
7.3000E+01	1.0000E+00
7.4000E+01	1.0000E+00
7.5000E+01	1.0000E+00
7.6000E+01	1.0000E+00
7.7000E+01	1.0000E+00
7.8000E+01	1.0000E+00
7.9000E+01	1.0000E+00
8.0000E+01	1.0000E+00
8.1000E+01	1.0000E+00
8.2000E+01	1.0000E+00
8.3000E+01	1.0000E+00
8.4000E+01	1.0000E+00
8.5000E+01	1.0000E+00
8.6000E+01	1.0000E+00
8.7000E+01	1.0000E+00
8.8000E+01	1.0000E+00
8.9000E+01	1.0000E+00
9.0000E+01	1.0000E+00
9.1000E+01	1.0000E+00
9.2000E+01	1.0000E+00
9.3000E+01	1.0000E+00
9.4000E+01	1.0000E+00
9.5000E+01	1.0000E+00
9.6000E+01	1.0000E+00
9.7000E+01	1.0000E+00
9.8000E+01	1.0000E+00
9.9000E+01	1.0000E+00
1.0000E+02	1.0000E+00

JOB CONCLUDED

TOTAL JOB TIME

12.63

TITLE SPWIP.CN

## \*\*\*\*\* CIRCUIT DESCRIPTION

```

***** CIRCUIT DESCRIPTION

* OPEN LOOP COMMON MODE BIAS AND FREQUENCY RESPONSE
* TRANSISTORS ARE BRAIN DATE SOURCE SUBSTRATE
*
* GROCKT SPWIP 1 2 3 4 5
*
* DIFFERENTIAL AMP
M1 6 20 7 7 NDEV L=10U U=15U
R2 5 4 7 7 NDEV L=10U U=15U
M3 6 6 1 1 PDEV L=10U U=20U
M4 5 5 1 1 PDEV L=10U U=20U
IS 7 8 2 2 NDEV L=10U U=30U
*
Ccomp 5 9 200PF
*
* OUTPUT STAGE
M6 1 3 9 1 PDEV L=100 U=15U
M7 9 8 2 2 NDEV L=10U U=30U
*
* VOLTAGE BIAS
M8 10 10 1 1 PDEV L=10U U=12U
M9 11 11 10 10 PDEV L=40U U=12U
M10 8 8 11 11 PDEV L=40U U=12U
M11 6 6 2 2 NDEV L=10U U=30U
*
MOS 3 20 DC 0.00797044
*
.ENDS
*
* POWER SUPPLIES
*
VDD 1 0 DC 6
VSS 2 0 DC -6
*
* INPUT SIGNALS
*
VINP 4 0 DC 0 AC 1
*
XI 1 2 4 4 9 SPWIP
*
.OPTIONS LINPTS=6000 ITL1=5000 PIUTOL=1E-15
.DC VINP -0E-3 0E-3 0.0005
.PLOT DC V(9) (-6,6)
.AC DEC 10 10 10NEG
.PLOT AC VH(9)
.PLOT AC VP(9)
.probe
*
.M10TN OUT=00
*
* MODELS
*
.MODEL NDEV NMOS LEVEL=2 LD=0.4U TOX=500E-10 NSUB=1E+16 VT0=1.0
+GMN=1.3506 PHI=0.6 UD=800 UEXP=0.0 UCINIT=1.0E6 UTAN=0.0
+DELTA=1.2403 UNDR=1E+3 XJ=0.07U LAMBDA=0.02 MFS=2E+11 NEFF=1.001E-2
+M3=0.0 TFS=-1.0 RSH=22 CSD0=350E-12 CSD0=200E-12 CSD0=350E-12 Cj=300E-6
+NJ=0.5 CJSU=300E-12 RJSH=0.3
*
.MODEL PDEV PMOS LEVEL=2 LD=0.5U TOX=500E-10 NSUB=1E+15 VT0=-1.0
+GMN=0.879003 PHI=0.6 UD=150 UEXP=0.0 UCINIT=1.0E6 UTAN=0.0
+DELTA=1.93831 UNDR=1E+5 XJ=1.0U LAMBDA=0.02 MFS=1.5E+11 NEFF=1.002E-2
+M3=0.0 TFS=1.0 RSH=93 CSD0=350E-12 CSD0=350E-12 CSD0=200E-12 Cj=150E-6
+NJ=0.5 CJSU=100E-12 RJSH=0.25
*
.END

```

\*\*\*\*\* 11/07/90 \*\*\*\*\* PSplus 1.04 - July, 1990 \*\*\*\*\* 19:51:49 \*\*\*\*\*

TITLE OF MPW CH

\*\*\*\*\* MOSFET MODEL PARAMETERS

	NDEV	PDEV
	NRDS	PRDS
LEVEL	2	2
TP0	-1	
L0	500.00000E-09	500.00000E-09
UT0	1	-1
KP	39.230300E-00	31.070290E-00
AVRR	1.3594	.879003
PHI	.6	.6
LAMBDA	.02	.02
RSH	22	75
CJ	500.00000E-06	150.00000E-06
CJSU	500.00000E-12	400.00000E-12
CJSU	.9	.25
CSG0	350.00000E-12	350.00000E-12
CSB0	350.00000E-12	350.00000E-12
CSB0	200.00000E-12	200.00000E-12
NSUB	10.00000E+15	10.00000E+15
MEG	0	0
MFS	200.00000E-09	150.00000E+09
TTR	50.00000E-09	50.00000E-09
XJ	870.00000E-09	1.00000E-06
VO	000	150
WCRT	1.00000E+06	1.00000E+06
WWK	100.00000E+03	100.00000E+03
NEFF	.01001	.01002
DELTR	1.2405	1.93631

\*\*\*\*\* 11/20/00 10:12:53 1:00 - 544 1000 999999 10:51:49 \*\*\*\*\*

TITLE SETTLED

2020 EC TWEETED CUMES

TEMPERATURE = 27,000 DEG C

<b>WIP</b>	<b>(%)</b>	<b>-0.500E+00</b>	<b>-3.000E+00</b>	<b>0.500E+00</b>	<b>3.000E+00</b>	<b>0.800E+00</b>
-6.000E-03	1.864E-05	.	.	.	+	.
-7.500E-03	3.261E-05	.	.	+	.	.
-7.000E-03	2.085E-05	.	.	+	.	.
-6.500E-03	2.508E-05	.	.	+	.	.
-6.000E-03	2.132E-05	.	.	+	.	.
-5.500E-03	1.755E-05	.	.	+	.	.
-5.000E-03	1.379E-05	.	.	+	.	.
-4.500E-03	1.334E-05	.	.	+	.	.
-4.000E-03	1.208E-05	.	.	+	.	.
-3.500E-03	-3.841E-04	.	.	+	.	.
-3.000E-03	-2.791E-04	.	.	+	.	.
-2.500E-03	2.730E-04	.	.	+	.	.
-2.000E-03	1.524E-05	.	.	+	.	.
-1.500E-03	1.149E-05	.	.	+	.	.
-1.000E-03	7.707E-06	.	.	+	.	.
-5.000E-04	7.297E-06	.	.	+	.	.
0.000E+00	6.947E-06	.	.	+	.	.
5.000E-04	8.944E-07	.	.	+	.	.
1.000E-03	-2.654E-06	.	.	+	.	.
1.500E-03	-3.186E-04	.	.	+	.	.
2.000E-03	-6.291E-04	.	.	+	.	.
2.500E-03	-4.791E-05	.	.	+	.	.
3.000E-03	2.556E-04	.	.	+	.	.
3.500E-03	1.155E-06	.	.	+	.	.
4.000E-03	7.186E-07	.	.	+	.	.
4.500E-03	-5.215E-06	.	.	+	.	.
5.000E-03	-8.951E-06	.	.	+	.	.
5.500E-03	-1.246E-05	.	.	+	.	.
6.000E-03	-1.842E-05	.	.	+	.	.
6.500E-03	-3.940E-04	.	.	+	.	.
7.000E-03	-6.463E-04	.	.	+	.	.
7.500E-03	-1.149E-04	.	.	+	.	.
8.000E-03	-8.137E-05	.	.	+	.	.

\*\*\*\*\* 11/07/90 \*\*\*\*\* PSpice 1.04 - July, 1990 \*\*\*\*\* 19:31:49 \*\*\*\*\*

TITLE SWAMP CR

\*\*\*\*\* SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

\*\*\*\*\*

MODE	VOLTAGE	MODE	VOLTAGE	MODE	VOLTAGE	MODE	VOLTAGE
( -1)	6.0000	( -2)	-6.0000	( -4)	0.0000	( -9)	-32.39E-00
( X1.5)	3.7983	( X1.6)	4.3146	( X1.7)	-1.6818	( X1.8)	-4.3923
( X1.10)	2.5358	( X1.11)	-5.9283	( X1.20)	-	( X1.21)	-0.0000

VOLTAGE SOURCE CURRENTS  
NAME CURRENT

VDD	-7.015E-05
VSS	7.015E-05
VINP	0.000E+00
X1.005	0.000E+00

TOTAL POWER DISSIPATION 0.42E-01 WATTS

TITLE SPRIP CR

\*\*\*\*\* NO ANALYSIS \*\*\*\*\*

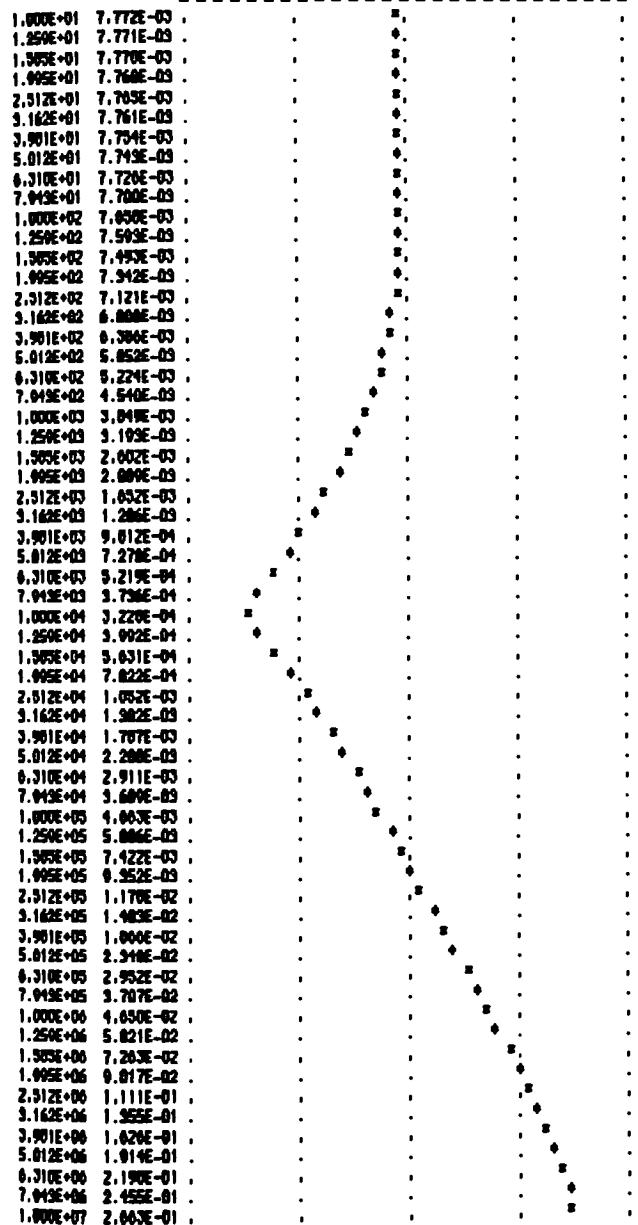
TEMPERATURE = 27.000 DEG C

LENSID:

+ UN(0)

FREQ UNH(0)

(x) ----- 1.000E-04 1.000E-03 1.000E-02 1.000E-01 1.000E+00



TITLE SPWTF.CN

SHEET AC ANALYSIS

TEMPERATURE = 27.000 DEG C

FREQ W(P)

(Hz)	-2.0000E+02	-1.0000E+02	0.0000E+00	1.0000E+02	2.0000E+02
1.000E+01	1.790E+02	.	.	.	.
1.250E+01	1.707E+02	.	.	.	.
1.500E+01	1.704E+02	.	.	.	.
1.750E+01	1.779E+02	.	.	.	.
2.500E+01	1.774E+02	.	.	.	.
3.162E+01	1.767E+02	.	.	.	.
3.901E+01	1.759E+02	.	.	.	.
5.012E+01	1.746E+02	.	.	.	.
6.310E+01	1.735E+02	.	.	.	.
7.943E+01	1.710E+02	.	.	.	.
1.000E+02	1.697E+02	.	.	.	.
1.250E+02	1.671E+02	.	.	.	.
1.500E+02	1.646E+02	.	.	.	.
1.750E+02	1.601E+02	.	.	.	.
2.500E+02	1.534E+02	.	.	.	.
3.162E+02	1.498E+02	.	.	.	.
3.901E+02	1.437E+02	.	.	.	.
5.012E+02	1.366E+02	.	.	.	.
6.310E+02	1.293E+02	.	.	.	.
7.943E+02	1.224E+02	.	.	.	.
1.000E+03	1.158E+02	.	.	.	.
1.250E+03	1.092E+02	.	.	.	.
1.500E+03	1.033E+02	.	.	.	.
1.750E+03	9.755E+01	.	.	.	.
2.500E+03	9.192E+01	.	.	.	.
3.162E+03	8.601E+01	.	.	.	.
3.901E+03	7.920E+01	.	.	.	.
5.012E+03	7.036E+01	.	.	.	.
6.310E+03	5.717E+01	.	.	.	.
7.943E+03	3.463E+01	.	.	.	.
1.000E+04	-7.172E-01	.	.	.	.
1.250E+04	-3.366E+01	.	.	.	.
1.500E+04	-5.313E+01	.	.	.	.
1.750E+04	-6.410E+01	.	.	.	.
2.500E+04	-7.107E+01	.	.	.	.
3.162E+04	-7.575E+01	.	.	.	.
3.901E+04	-7.911E+01	.	.	.	.
5.012E+04	-8.176E+01	.	.	.	.
6.310E+04	-8.370E+01	.	.	.	.
7.943E+04	-8.531E+01	.	.	.	.
1.000E+05	-8.644E+01	.	.	.	.
1.250E+05	-8.777E+01	.	.	.	.
1.500E+05	-8.870E+01	.	.	.	.
1.750E+05	-8.973E+01	.	.	.	.
2.500E+05	-9.065E+01	.	.	.	.
3.162E+05	-9.161E+01	.	.	.	.
3.901E+05	-9.265E+01	.	.	.	.
5.012E+05	-9.368E+01	.	.	.	.
6.310E+05	-9.521E+01	.	.	.	.
7.943E+05	-9.687E+01	.	.	.	.
1.000E+06	-9.800E+01	.	.	.	.
1.250E+06	-1.013E+02	.	.	.	.
1.500E+06	-1.044E+02	.	.	.	.
1.750E+06	-1.081E+02	.	.	.	.
2.500E+06	-1.126E+02	.	.	.	.
3.162E+06	-1.180E+02	.	.	.	.
3.901E+06	-1.243E+02	.	.	.	.
5.012E+06	-1.316E+02	.	.	.	.
6.310E+06	-1.397E+02	.	.	.	.
7.943E+06	-1.494E+02	.	.	.	.
1.000E+07	-1.575E+02	.	.	.	.

JOB CONCLUDED

TOTAL JOB TIME

15.60

TITLE CIRCUIT SPWTF

\*\*\*\*\* CIRCUIT DESCRIPTION

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***** CIRCUIT DESCRIPTION

* OPEN LOOP DIFFERENTIAL GAIN AND FREQUENCY RESPONSE
*
* TRANSISTORS ARE DRAIN GATE SOURCE SUBSTRATE
*
* BIASSET SPWTF 1 2 3 4 5
*
* DIFFERENTIAL AMP.
N1 6 20 7 NDEV L=10U N=15U
R2 5 4 7 7 NDEV L=10U N=15U
R3 6 6 1 1 PDEV L=10U N=20U
R4 5 6 1 1 PDEV L=10U N=20U
R5 7 8 2 2 NDEV L=10U N=30U
*
*
* OUTPUT STAGE
N6 1 5 9 1 PDEV L=10U N=15U
R7 9 8 2 2 NDEV L=10U N=30U
*
*
* VOLTAGE BIAS
R8 10 10 1 1 PDEV L=40U N=12U
R9 11 11 10 10 PDEV L=10U N=12U
R10 8 8 11 11 PDEV L=10U N=12U
N11 8 8 2 2 NDEV L=10U N=30U
*
*
CCWF 5 9 200PF
*
*
VBS 3 20 DC 0.00707044
*
.EBS
*
* POWER SUPPLIES
*
VDD 1 0 DC 6
VSS 2 0 DC -6
*
* INPUT SIGNALS
*
VINH 3 8 DC 0 AC 0
VINP 4 0 DC 0 AC 1
*
*
RI 1 2 3 4 5 SPWTF
*
.OPTIONS LINPTG=0000 ITLI=5000 PIOTOL=1E-15
.AC VINF -6E-3 0E-3 0.0005
.PLOT AC V(9) (-6,6)
.AC DEC 10 10 10NEA
.PLOT AC VIN(9)
.PLOT AC VP(9)
.PI000
*
*
.WIDTH OUT=80
*
* MODELS
*
.MODEL NDEV NMOS LEVEL=2 LD=0.4U TOX=500E-10 NSUB=1E+16 UT0=1.0
*NMN=1.3598 PHI=0.6 UD=600 UEXP=0.0 UCRT=1.0E6 UTRA=0.0
*DELTA=1.2405 WNMN=1E+5 XJ=0.87U LNMN=0.02 NF9=2E+11 NEFF=1.001E-2
*NF5=0.0 TPS=1.0 RSH=22 CSE0=350E-12 CSD0=200E-12 CSD0=350E-12 Cj=300E-0
*XJ=0.5 CJMN=500E-12 RJMN=0.9
*
*
.MODEL PDEV PMOS LEVEL=2 LD=0.5U TOX=500E-10 NSUB=1E+15 UT0=-1.0
*NMN=0.870023 PHI=0.6 UD=450 UEXP=0.0 UCRT=1.0E6 UTRA=0.0
*DELTA=1.35831 WNMN=1E+5 XJ=1.0U LNMN=0.02 NF5=1.5E+11 NEFF=1.002E-2
*NF9=0.0 TPS=1.0 RSH=95 CSE0=350E-12 CSD0=200E-12 CSD0=350E-12 Cj=150E-6
*XJ=0.5 CJMN=100E-12 RJMN=0.23
*
*.END

```

TITLE CH3S SPWTF

\*\*\*\*\* MOSFET MODEL PARAMETERS

	MDEV	PDEV
	MROS	PROS
LEVEL	2	2
TFS	-1	
LB	100.00000E-09	300.00000E-09
UTB	1	-1
CF	55.25030E-06	31.87029E-06
OMMA	1.2504	.879003
PHI	.6	.6
LAMBDA	.02	.02
RSH	22	75
CJ	500.00000E-06	150.00000E-06
CJSI	500.00000E-12	400.00000E-12
BLNK	.9	.25
CS00	350.00000E-12	350.00000E-12
CS00	350.00000E-12	350.00000E-12
CS00	200.00000E-12	200.00000E-12
RSUB	10.00000E+15	10.00000E+15
NBS	0	0
NFS	200.00000E+00	150.00000E+00
TOR	50.00000E-09	50.00000E-09
XJ	870.00000E-09	1.00000E-06
VB	800	750
NCIT	1.00000E+06	1.00000E+06
WKK	100.00000E+03	100.00000E+03
MEFF	.01001	.01002
DELTA	1.2405	1.53031

TITLE CMS SPWTF

DC TRANSFER CURVES

TEMPERATURE = 27.000 DEG C

V(1)	V(2)					
-8.000E-03	-5.874E+00	.	.	.	.	.
-7.500E-03	-5.862E+00	*	.	.	.	.
-7.000E-03	-5.849E+00	*	.	.	.	.
-6.500E-03	-5.835E+00	*	.	.	.	.
-6.000E-03	-5.819E+00	*	.	.	.	.
-5.500E-03	-5.801E+00	*	.	.	.	.
-5.000E-03	-5.780E+00	*	.	.	.	.
-4.500E-03	-5.754E+00	*	.	.	.	.
-4.000E-03	-5.720E+00	*	.	.	.	.
-3.500E-03	-5.683E+00	*	.	.	.	.
-3.000E-03	-5.927E+00	*	.	.	.	.
-2.500E-03	-4.132E+00	*	.	.	.	.
-2.000E-03	-3.312E+00	*	.	.	.	.
-1.500E-03	-2.482E+00	*	.	.	.	.
-1.000E-03	-1.649E+00	*	.	.	.	.
-5.000E-04	-8.204E-01	*	.	.	.	.
0.000E+00	5.723E-05	*	.	.	.	.
5.000E-04	8.096E-01	*	.	.	.	.
1.000E-03	1.667E+00	*	.	.	.	.
1.500E-03	2.388E+00	*	.	.	.	.
2.000E-03	3.151E+00	*	.	.	.	.
2.500E-03	3.895E+00	*	.	.	.	.
3.000E-03	4.614E+00	*	.	.	.	.
3.500E-03	5.184E+00	*	.	.	.	.
4.000E-03	5.274E+00	*	.	.	.	.
4.500E-03	5.324E+00	*	.	.	.	.
5.000E-03	5.385E+00	*	.	.	.	.
5.500E-03	5.394E+00	*	.	.	.	.
6.000E-03	5.423E+00	*	.	.	.	.
6.500E-03	5.446E+00	*	.	.	.	.
7.000E-03	5.466E+00	*	.	.	.	.
7.500E-03	5.484E+00	*	.	.	.	.
8.000E-03	5.500E+00	*	.	.	.	.

\*\*\*\*\* 11/07/90 \*\*\*\*\* PSpice 4.04 - July, 1990 \*\*\*\*\* 19:40:16 \*\*\*\*\*

TITLE CRDS SPWPF

\*\*\*\*\* SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

\*\*\*\*\*

NAME	VOLTAGE	NAME	VOLTAGE	NAME	VOLTAGE	NAME	VOLTAGE
( 1)	0.0000	( 2)	-0.0000	( 3)	0.0000	( 4)	0.0000
( 9)-32.59E-06 ( X1.5)	3.9063	( X1.6)	4.3146	( X1.7)	-1.6616		
( X1.8)	-4.3925	( X1.10)	2.5350	( X1.11)	-.9283	( X1.20)	-0.0000

VOLTAGE SOURCE CURRENTS

NAME CURRENT

VDD	-7.015E-05
VSS	7.015E-05
V1IN	0.000E+00
V1IP	0.000E+00
X1.405	0.000E+00

TOTAL POWER DISSIPATION 0.42E-04 WATTS

\*\*\*\*\* 11/07/98 \*\*\*\*\* Physics 4.04 - July, 1998 \*\*\*\*\* 10:48:16 \*\*\*\*\*

TITLE CROS SPNP

\*\*\* RC ANALYSIS

TEMPERATURE = 27.000 DEG C

LEGEND:

+: UN(0)

FREQ UN(0)

(z)	1.000E-01	1.000E+01	1.000E+03	1.000E+05	1.000E+07
1.000E+01	1.043E+03	.	.	.	.
1.250E+01	1.645E+03	.	.	.	.
1.500E+01	1.043E+03	.	.	.	.
1.750E+01	1.645E+03	.	.	.	.
2.000E+01	1.043E+03	.	.	.	.
2.500E+01	1.645E+03	.	.	.	.
3.162E+01	1.643E+03	.	.	.	.
3.901E+01	1.041E+03	.	.	.	.
5.012E+01	1.639E+03	.	.	.	.
6.310E+01	1.638E+03	.	.	.	.
7.943E+01	1.638E+03	.	.	.	.
1.000E+02	1.021E+03	.	.	.	.
1.250E+02	1.607E+03	.	.	.	.
1.500E+02	1.596E+03	.	.	.	.
1.750E+02	1.555E+03	.	.	.	.
2.000E+02	1.500E+03	.	.	.	.
2.500E+02	1.412E+03	.	.	.	.
3.162E+02	1.353E+03	.	.	.	.
3.901E+02	1.241E+03	.	.	.	.
5.012E+02	1.109E+03	.	.	.	.
6.310E+02	9.658E+02	.	.	.	.
7.943E+02	9.658E+02	.	.	.	.
1.000E+03	8.212E+02	.	.	.	.
1.250E+03	6.945E+02	.	.	.	.
1.500E+03	5.619E+02	.	.	.	.
1.750E+03	4.563E+02	.	.	.	.
2.000E+03	3.077E+02	.	.	.	.
2.500E+03	2.916E+02	.	.	.	.
3.162E+03	2.356E+02	.	.	.	.
3.901E+03	1.876E+02	.	.	.	.
5.012E+03	1.490E+02	.	.	.	.
6.310E+03	1.190E+02	.	.	.	.
7.943E+03	9.400E+01	.	.	.	.
1.000E+04	7.519E+01	.	.	.	.
1.250E+04	5.973E+01	.	.	.	.
1.500E+04	4.747E+01	.	.	.	.
1.750E+04	3.772E+01	.	.	.	.
2.000E+04	2.906E+01	.	.	.	.
2.500E+04	2.300E+01	.	.	.	.
3.162E+04	1.991E+01	.	.	.	.
3.901E+04	1.502E+01	.	.	.	.
5.012E+04	1.193E+01	.	.	.	.
6.310E+04	1.000E+01	.	.	.	.
7.943E+04	8.477E+00	.	.	.	.
1.000E+05	7.526E+00	.	.	.	.
1.250E+05	5.901E+00	.	.	.	.
1.500E+05	4.752E+00	.	.	.	.
1.750E+05	3.776E+00	.	.	.	.
2.000E+05	3.001E+00	.	.	.	.
2.500E+05	2.398E+00	.	.	.	.
3.162E+05	1.808E+00	.	.	.	.
3.901E+05	1.511E+00	.	.	.	.
5.012E+05	1.204E+00	.	.	.	.
6.310E+05	9.620E-01	.	.	.	.
7.943E+05	7.708E-01	.	.	.	.
1.000E+06	6.203E-01	.	.	.	.
1.250E+06	5.031E-01	.	.	.	.
1.500E+06	4.122E-01	.	.	.	.
1.750E+06	3.426E-01	.	.	.	.
2.000E+06	2.901E-01	.	.	.	.
2.500E+06	2.514E-01	.	.	.	.
3.162E+06	2.294E-01	.	.	.	.
3.901E+06	2.039E-01	.	.	.	.
5.012E+06	1.803E-01	.	.	.	.
6.310E+06	1.600E-01	.	.	.	.
7.943E+06	1.424E-01	.	.	.	.
1.000E+07	1.266E-01	.	.	.	.

\*\*\*\*\* 11/07/98 \*\*\*\*\* PSpice 4.04 - July, 1990 \*\*\*\*\* 19:48:46 \*\*\*\*\*

TITLE CRDS SPWTF

SIMU AC ANALYSIS

TEMPERATURE = 27.000 DEG C

FREQ WP(0)

(0)----- -2.000E+02 -1.500E+02 -1.000E+02 -5.000E+01 0.000E+00  
1.000E+01 -9.949E-01 . . . .  
1.250E+01 -1.252E+00 . . . .  
1.385E+01 -1.577E+00 . . . .  
1.495E+01 -1.944E+00 . . . .  
2.512E+01 -2.498E+00 . . . .  
3.162E+01 -3.143E+00 . . . .  
3.901E+01 -3.955E+00 . . . .  
5.012E+01 -4.974E+00 . . . .  
6.310E+01 -6.253E+00 . . . .  
7.043E+01 -7.054E+00 . . . .  
1.000E+02 -9.051E+00 . . . .  
1.250E+02 -1.233E+01 . . . .  
1.385E+02 -1.539E+01 . . . .  
1.495E+02 -1.911E+01 . . . .  
2.512E+02 -2.357E+01 . . . .  
3.162E+02 -3.077E+01 . . . .  
3.901E+02 -3.966E+01 . . . .  
5.012E+02 -4.104E+01 . . . .  
6.310E+02 -4.762E+01 . . . .  
7.043E+02 -5.104E+01 . . . .  
1.000E+03 -6.007E+01 . . . .  
1.250E+03 -6.513E+01 . . . .  
1.385E+03 -7.004E+01 . . . .  
1.495E+03 -7.302E+01 . . . .  
2.512E+03 -7.711E+01 . . . .  
3.162E+03 -7.970E+01 . . . .  
3.901E+03 -8.100E+01 . . . .  
5.012E+03 -8.314E+01 . . . .  
6.310E+03 -8.493E+01 . . . .  
7.043E+03 -8.502E+01 . . . .  
1.000E+04 -8.676E+01 . . . .  
1.250E+04 -8.746E+01 . . . .  
1.385E+04 -8.004E+01 . . . .  
1.495E+04 -8.050E+01 . . . .  
2.512E+04 -8.089E+01 . . . .  
3.162E+04 -8.021E+01 . . . .  
3.901E+04 -8.315E+01 . . . .  
5.012E+04 -8.074E+01 . . . .  
6.310E+04 -8.990E+01 . . . .  
7.043E+04 -8.021E+01 . . . .  
1.000E+05 -8.046E+01 . . . .  
1.250E+05 -8.073E+01 . . . .  
1.385E+05 -9.104E+01 . . . .  
1.495E+05 -9.114E+01 . . . .  
2.512E+05 -9.185E+01 . . . .  
3.162E+05 -9.239E+01 . . . .  
3.901E+05 -9.306E+01 . . . .  
5.012E+05 -9.399E+01 . . . .  
6.310E+05 -9.493E+01 . . . .  
7.043E+05 -9.623E+01 . . . .  
1.000E+06 -9.703E+01 . . . .  
1.250E+06 -9.909E+01 . . . .  
1.385E+06 -1.024E+02 . . . .  
1.495E+06 -1.056E+02 . . . .  
2.512E+06 -1.096E+02 . . . .  
3.162E+06 -1.144E+02 . . . .  
3.901E+06 -1.203E+02 . . . .  
5.012E+06 -1.273E+02 . . . .  
6.310E+06 -1.353E+02 . . . .  
7.043E+06 -1.441E+02 . . . .  
1.000E+07 -1.533E+02 . . . .

JOB CONCLUDED

TOTAL JOB TIME

16.64

\*\*\*\*\* 11/07/90 \*\*\*\*\* Pspice 4.04 - July, 1990 \*\*\*\*\* 20:17:52 \*\*\*\*\*

TITLE CMOS OPAMP UNCOMP

\*\*\*\*\* CIRCUIT DESCRIPTION

```
*****  
  
* UNCOMPENSATED OPEN LOOP DIFFERENTIAL GAIN AND FREQUENCY RESPONSE  
*  
* TRANSISTORS ARE BRATT GATE SOURCE SUBSTRATE  
*  
*  
.SUBCKT OPAMP 1 2 3 4 9  
*  
* DIFFERENTIAL AMP  
R1 6 20 7 7 NDEV L=10U H=15U  
R2 5 4 7 7 NDEV L=10U H=15U  
R3 6 6 1 1 PDEV L=10U H=20U  
M1 5 6 1 1 PDEV L=10U H=20U  
R5 7 8 2 2 NDEV L=10U H=30U  
*  
*  
* OUTPUT STAGE  
R6 1 3 9 1 PDEV L=10U H=15U  
R7 9 8 2 2 NDEV L=10U H=30U  
*  
*  
* VOLTAGE BIAS  
R8 10 10 1 1 PDEV L=40U H=12U  
R9 11 11 10 10 PDEV L=40U H=12U  
R10 8 8 11 11 PDEV L=40U H=12U  
R11 9 9 2 2 NDEV L=10U H=30U  
*  
*  
*  
W05 3 20 DC 0.00797044  
*  
.ENDS  
*  
* POWER SUPPLIES  
*  
VDD 1 8 DC 5  
VSS 2 9 DC -5  
*  
* INPUT SIGNALS  
*  
VINP 3 0 DC 0 AC 0  
VINN 4 0 DC 0 AC 1  
*  
X1 1 2 3 4 9 OPAMP  
*  
.OPTIONS LINPTF=6000 ITL1=5000 PIOTOL=1E-15  
.DC VINP -5E-3 0E-3 0.0005  
.PLOT DC V(9) (-6,0)  
.AC DEC 10 10 10MEG  
.PLOT AC VR(9)  
.PLOT AC VP(9)  
*  
*  
.WIDTH OUT=00  
*  
* MODELS  
*  
.MODEL NDEV NMOS LEVEL=2 LD=0.4U TOX=500E-10 NSUB=1E+16 VT0=1.0  
>GMN=1.3504 PH1=0.6 UD=800 UEXP=0.0 UCR1T=1.0E6 UTRH=0.0  
>DELTA=1.2403 UWRH=1E+3 XJ=0.07U LWRD=0.02 NF=2E+11 NEFF=1.001E-2  
>NS=0.0 TPF=-1.0 RSH=22 CSD0=350E-12 CSD0=200E-12 CSD0=350E-12 CJ=300E-6  
>RL=0.5 CJSN=500E-12 RJSN=0.3  
*  
*  
.MODEL PDEV PMOS LEVEL=2 LD=0.5U TOX=500E-10 NSUB=10.0E+15 VT0=-1.0  
>GMPN=0.079003 PH1=0.6 UD=450 UEXP=0.0 UCR1T=1.0E6 UTRH=0.0  
>DELTA=1.09291 UWRH=1E+5 XJ=1.0U LWRD=0.02 NF=1.5E+11 NEFF=1.002E-2  
>NS=0.0 TPF=1.0 RSH=95 CSD0=350E-12 CSD0=200E-12 CSD0=350E-12 CJ=150E-6  
>RL=0.5 CJSN=100E-12 RJSN=0.25  
*  
.END
```

\*\*\*\*\* 11/07/90 \*\*\*\*\* PSplus 1.01 - July, 1990 \*\*\*\*\* 20:17:52 \*\*\*\*\*

TITLE CDRS OPNP UNCOND

\*\*\*\*\* ROSET MODEL PARAMETERS

	NEU	PDEU
	MM25	PH25
LEVEL	2	2
TP0	-1	
LB	400.00000E-05	500.00000E-05
UT0	1	-1
KY	55.23030E-06	31.87629E-06
AMIN	1.2504	.870003
PH1	.6	.6
LAMBDA	.02	.02
RSH	22	95
CJ	300.00000E-06	150.00000E-06
CJEN	300.00000E-12	400.00000E-12
KLAM	.9	.25
CP00	350.00000E-12	350.00000E-12
CP00	350.00000E-12	350.00000E-12
CP00	200.00000E-12	200.00000E-12
NSUB	10.00000E+15	10.00000E+15
NFG	0	0
NFS	200.00000E+00	150.00000E+00
TRX	50.00000E-05	50.00000E-05
KL	870.00000E-09	1.00000E-06
UU	800	130
UCRIT	1.00000E+04	1.00000E+04
WMAX	100.00000E+03	100.00000E+03
HEFF	.01001	.01002
DELTA	1.2405	1.93631

\*\*\*\*\* 11/07/90 \*\*\*\*\* PSpice 4.04 - July, 1990 \*\*\*\*\* 20:17:52 \*\*\*\*\*

TITLE CMOS OPAMP UNCLIP

\*\*\*\*\* DC TRANSFER CURVES

TEMPERATURE = 27.000 DEG C

VINP	V(0)					
-6.000E-03	-5.874E+00	.	.	.	.	.
-7.500E-03	-5.862E+00	.	.	.	.	.
-1.000E-02	-5.849E+00	.	.	.	.	.
-6.000E-03	-5.835E+00	.	.	.	.	.
-6.000E-03	-5.819E+00	.	.	.	.	.
-5.500E-03	-5.801E+00	.	.	.	.	.
-5.000E-03	-5.780E+00	.	.	.	.	.
-4.500E-03	-5.754E+00	.	.	.	.	.
-4.000E-03	-5.720E+00	.	.	.	.	.
-3.500E-03	-5.683E+00	.	.	.	.	.
-3.000E-03	-5.927E+00	.	.	.	.	.
-2.500E-03	-4.132E+00	.	.	.	.	.
-2.000E-03	-3.312E+00	.	.	.	.	.
-1.500E-03	-2.482E+00	.	.	.	.	.
-1.000E-03	-1.649E+00	.	.	.	.	.
-5.000E-04	-8.204E-01	.	.	.	.	.
0.000E+00	-5.723E-05	.	.	.	.	.
5.000E-04	8.096E-01	.	.	.	.	.
1.000E-03	1.687E+00	.	.	.	.	.
1.500E-03	2.388E+00	.	.	.	.	.
2.000E-03	3.151E+00	.	.	.	.	.
2.500E-03	3.895E+00	.	.	.	.	.
3.000E-03	4.614E+00	.	.	.	.	.
3.500E-03	5.184E+00	.	.	.	.	.
4.000E-03	5.274E+00	.	.	.	.	.
4.500E-03	5.326E+00	.	.	.	.	.
5.000E-03	5.365E+00	.	.	.	.	.
5.500E-03	5.396E+00	.	.	.	.	.
6.000E-03	5.423E+00	.	.	.	.	.
6.500E-03	5.446E+00	.	.	.	.	.
7.000E-03	5.466E+00	.	.	.	.	.
7.500E-03	5.484E+00	.	.	.	.	.
8.000E-03	5.500E+00	.	.	.	.	.

\*\*\*\*\* 11/07/90 \*\*\*\*\* PSpice 4.01 - July, 1990 \*\*\*\*\* 20:17:52 \*\*\*\*\*

TITLE CH03 SPWIP UNCOMP

\*\*\*\*\* SHELL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

\*\*\*\*\*  
NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE  
( 1) 0.0000 ( 2) -0.0000 ( 3) 0.0000 ( 4) 0.0000  
( 9)-32.59E-06 ( X1.5) 3.9863 ( X1.6) 4.3146 ( X1.7) -1.6616  
( X1.8) -4.3923 ( X1.10) 2.5336 ( X1.11) -.9283 ( X1.20) -.0000

VOLTAGE SOURCE CURRENTS  
NODE CURRENT

UDD -7.015E-05  
USS 7.015E-05  
U1IN 0.000E+00  
U1NP 0.000E+00  
X1.N05 0.000E+00

TOTAL POWER DISSIPATION 0.42E-04 WATTS

\*\*\*\*\* 11/07/90 \*\*\*\*\* PSpice 4.04 - July, 1990 \*\*\*\*\* 20:17:52 \*\*\*\*\*

TITLE CRDS SPWTF UNCOMP

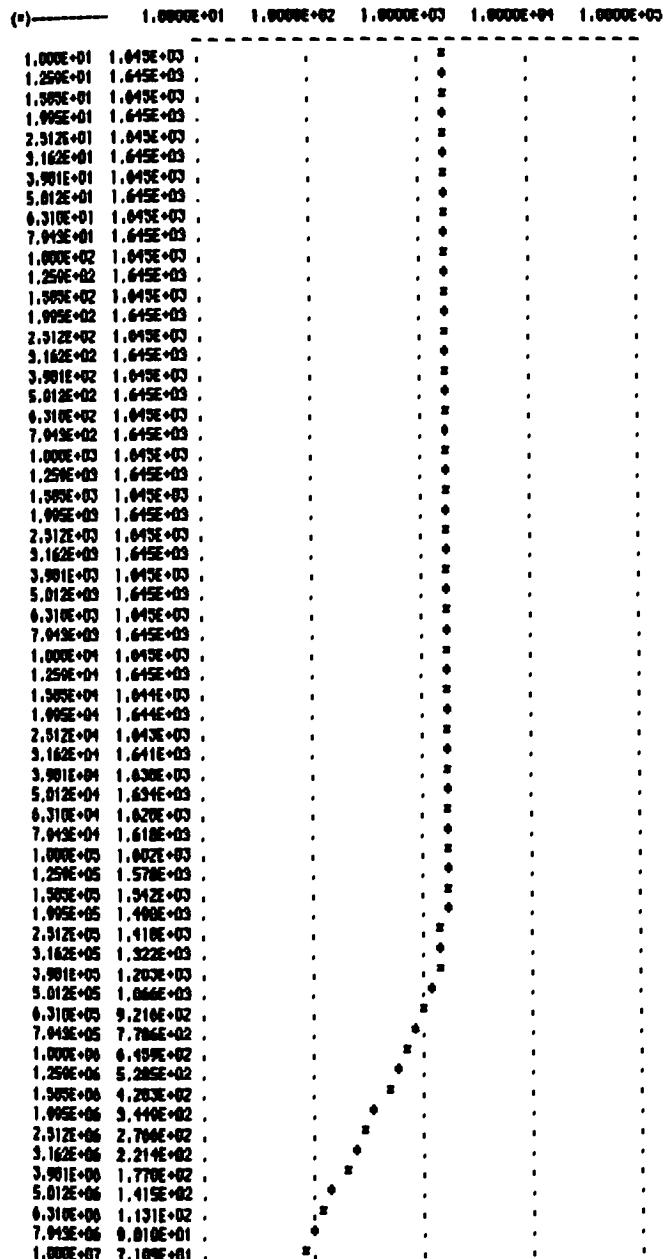
\*\*\*\*\* DC ANALYSIS \*\*\*\*\*

TEMPERATURE = 27.000 DEG C

LEGEND:

o: MM(t)

FREQ MM(t)



\*\*\*\*\* 11/07/90 \*\*\*\*\* PSPice 4.04 - July, 1990 \*\*\*\*\* 20:17:52 \*\*\*\*\*

TITLE CRSS SPWPF UNCOMP

\*\*\*\*\* DC ANALYSIS

TEMPERATURE = 27.000 DEG C

FREQ SP(0)

(Hz)	-1.000E+02	-1.000E+02	-9.000E+01	-7.1054E-15	5.0000E+01
1.000E+01	-1.304E-03	.	.	.	.
1.250E+01	-1.717E-03	.	.	.	.
1.333E+01	-2.162E-03	.	.	.	.
1.995E+01	-3.722E-03	.	.	.	.
2.512E+01	-3.420E-03	.	.	.	.
3.162E+01	-4.314E-03	.	.	.	.
3.991E+01	-5.431E-03	.	.	.	.
5.012E+01	-6.637E-03	.	.	.	.
6.310E+01	-8.607E-03	.	.	.	.
7.943E+01	-1.004E-02	.	.	.	.
1.000E+02	-1.304E-02	.	.	.	.
1.250E+02	-1.717E-02	.	.	.	.
1.333E+02	-2.162E-02	.	.	.	.
1.995E+02	-3.722E-02	.	.	.	.
2.512E+02	-3.420E-02	.	.	.	.
3.162E+02	-4.314E-02	.	.	.	.
3.991E+02	-5.431E-02	.	.	.	.
5.012E+02	-6.637E-02	.	.	.	.
6.310E+02	-8.607E-02	.	.	.	.
7.943E+02	-1.004E-01	.	.	.	.
1.000E+03	-1.304E-01	.	.	.	.
1.250E+03	-1.717E-01	.	.	.	.
1.333E+03	-2.162E-01	.	.	.	.
1.995E+03	-3.722E-01	.	.	.	.
2.512E+03	-3.420E-01	.	.	.	.
3.162E+03	-4.314E-01	.	.	.	.
3.991E+03	-5.431E-01	.	.	.	.
5.012E+03	-6.637E-01	.	.	.	.
6.310E+03	-8.607E-01	.	.	.	.
7.943E+03	-1.004E+00	.	.	.	.
1.000E+04	-1.304E+00	.	.	.	.
1.250E+04	-1.717E+00	.	.	.	.
1.333E+04	-2.162E+00	.	.	.	.
1.995E+04	-3.722E+00	.	.	.	.
2.512E+04	-3.420E+00	.	.	.	.
3.162E+04	-4.314E+00	.	.	.	.
3.991E+04	-5.431E+00	.	.	.	.
5.012E+04	-6.637E+00	.	.	.	.
6.310E+04	-8.607E+00	.	.	.	.
7.943E+04	-1.071E+01	.	.	.	.
1.000E+05	-1.340E+01	.	.	.	.
1.250E+05	-1.671E+01	.	.	.	.
1.333E+05	-2.071E+01	.	.	.	.
1.995E+05	-2.546E+01	.	.	.	.
2.512E+05	-3.102E+01	.	.	.	.
3.162E+05	-3.721E+01	.	.	.	.
3.991E+05	-4.385E+01	.	.	.	.
5.012E+05	-5.664E+01	.	.	.	.
6.310E+05	-5.724E+01	.	.	.	.
7.943E+05	-6.340E+01	.	.	.	.
1.000E+06	-6.990E+01	.	.	.	.
1.250E+06	-7.386E+01	.	.	.	.
1.333E+06	-7.822E+01	.	.	.	.
1.995E+06	-8.208E+01	.	.	.	.
2.512E+06	-8.561E+01	.	.	.	.
3.162E+06	-8.908E+01	.	.	.	.
3.991E+06	-9.242E+01	.	.	.	.
5.012E+06	-9.614E+01	.	.	.	.
6.310E+06	-1.003E+02	.	.	.	.
7.943E+06	-1.056E+02	.	.	.	.
1.000E+07	-1.120E+02	.	.	.	.

JOB CONCLUDED

TOTAL JOB TIME

16.20

TITLE OPAMP ARI

## \*\*\*\*\* CIRCUIT DESCRIPTION

```

* INPUT RESISTANCE
* TRANSISTORS ARE DRAIN GATE SOURCE SUBSTRATE
* .SUBCKT OPAMP 1 2 3 4 9
* DIFFERENTIAL AMP
N1 6 20 7 7 MDEV L=10U H=15U
N2 5 4 7 7 MDEV L=10U H=15U
N3 6 6 1 1 PDEV L=10U H=20U
N4 5 6 1 1 PDEV L=10U H=20U
N5 7 8 2 2 MDEV L=10U H=30U
* Comp 3 0 200PF
* OUTPUT STAGE
N6 1 5 9 1 PDEV L=10U H=15U
N7 9 8 2 2 MDEV L=10U H=30U
* VOLTAGE BIAS
N8 10 10 1 1 PDEV L=10U H=12U
N9 11 11 10 10 PDEV L=10U H=12U
N10 0 0 11 11 PDEV L=10U H=12U
N11 0 0 2 2 MDEV L=10U H=30U
* .VOS 3 20 DC 0.00797044
*.ENDS
* POWER SUPPLIES
VDD 1 0 DC 0
VSS 2 0 DC -6
* INPUT SIGNALS
VINN 3 0 DC 0 AC 0
VINP 4 0 DC 0 AC 1
* Nodes
Node1 3 5 DC 0
Node2 4 6 DC 0
X1 1 2 5 6 9 OPAMP
* .OPTIONS LINPT3=6000 ITL1=5000 PIOTOL=1E-15
*.AC VINF -5E-3 5E-3 0.0005
*.DC REC 10 10 1MEG
.PLOT AC IR(Vnode1) IR(vnode2) VR(3) VR(4)
*.probe
* .BOTH OUT=00
* MODELS
* .MODEL MDEV MNDS LEVEL=2 LD=0.4U TON=500E-10 NSUB=1E+10 VT0=-1.0
*.MNNP=1.5956 PHI=0.6 UD=800 UEXP=0.0 UCRT=1.0E6 HTM=0.0
*.DELTA=1.2405 VTRH=1E-5 XJ=0.07U LAMBDA=0.02 NF=2E+11 NEFF=1.001E-2
*.NS=0.0 TFB=-1.0 RSH=22 CSD0=350E-12 CSD0=200E-12 CSD0=350E-12 CJ=300E-6
*.IJ=0.3 CJSW=300E-12 RJSW=0.3
* .MODEL PDEV MNDS LEVEL=2 LD=0.5U TON=500E-10 NSUB=1E+15 VT0=-1.0
*.MNNP=0.679003 PHI=0.6 UD=150 UEXP=0.0 UCRT=1.0E6 UTRH=0.0
*.DELTA=1.03031 VND0=1E-5 XJ=1.0U LAMBDA=0.02 NF=1.5E+11 NEFF=1.002E-2
*.NS=0.0 TFB=-1.0 RSH=50 CSD0=350E-12 CSD0=200E-12 CSD0=350E-12 CJ=150E-6
*.IJ=0.5 CJSW=100E-12 RJSW=0.25
* .END

```

TITLE OF MPN RIN

\*\*\*\*\* MOSFET MODEL PARAMETERS

	NDEU	PDEU
	MDOS	PDOS
LEVEL	2	2
TP0	-1	
LD	400.00000E-09	500.00000E-09
VTO	1	-1
X <sub>F</sub>	35.230300E-06	31.076290E-06
ANBR	1.3506	.079003
PHI	.6	.6
LAMBDA	.02	.02
RSH	22	55
CJ	300.00000E-06	150.00000E-06
CJSW	300.00000E-12	400.00000E-12
CLSW	.3	.25
CSO	350.00000E-12	350.00000E-12
CSDD	350.00000E-12	250.00000E-12
CSDO	200.00000E-12	200.00000E-12
ISUB	10.00000E+15	10.00000E+15
NSC	0	0
MF3	200.00000E+09	150.00000E+09
TRH	30.00000E-09	30.00000E-09
TL	870.00000E-09	1.00000E-08
UD	800	450
MORIT	1.00000E+06	1.00000E+06
WWRK	100.00000E+03	100.00000E+03
NEFF	.01001	.01002
DELTA	1.2405	1.93631

\*\*\*\*\* 11/07/90 \*\*\*\*\* PSpice 4.04 - July, 1990 \*\*\*\*\* 20:13:11 \*\*\*\*\*

TITLE OPAMP.BIN

\*\*\*\*\* SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

---

NAME	VOLTAGE	NAME	VOLTAGE	NAME	VOLTAGE	NAME	VOLTAGE
( 1 )	0.0000	( 2 )	-0.0000	( 3 )	0.0000	( 4 )	0.0000
( 5 )	0.0000	( 6 )	0.0000	( 7 )	-32.99E-06	( X1.5 )	3.9003
( X1.6 )	4.3196	( X1.7 )	-1.6010	( X1.8 )	-4.3923	( X1.10 )	2.5338
( X1.11 )	-5.9263	( X1.20 )	-0.0000				

VOLTAGE SOURCE CURRENTS  
NAME CURRENT

VDD	-7.015E-05
VSS	7.015E-05
VINH	0.000E+00
VINL	0.000E+00
VDD001	0.000E+00
VDD002	0.000E+00
X1.VDS	0.000E+00

TOTAL POWER DISSIPATION 0.42E-04 WATTS

TITLE SPWV.RIN

\*\*\*\*\* AC ANALYSIS

TEMPERATURE = 27.000 DEG C

LEGEND:

- o: IR(Uminal)
- +: IR(Veooee2)
- : VR(3)
- \$: VR(4)

FREQ IR(Veooee1)

(*)-----	1.000E-12	1.000E-10	1.000E-08	1.000E-06	1.000E-04
(*)-----	1.000E-11	1.000E-09	1.000E-07	1.000E-05	1.000E-03
(*)-----	1.000E-20	1.000E-19	1.000E-18	1.000E-17	1.000E-16
(*)-----	1.000E+00	1.000E+01	1.000E+02	1.000E+03	1.000E+04
1.000E+01	1.173E-12	X	+	-	-
1.250E+01	1.477E-12	X	+	-	-
1.333E+01	1.660E-12	X	+	-	-
1.000E+01	2.344E-12	X	+	-	-
2.500E+01	2.954E-12	X	+	-	-
3.162E+01	3.725E-12	X	+	-	-
3.501E+01	4.702E-12	X	+	-	-
5.002E+01	5.944E-12	X	+	-	-
6.310E+01	7.331E-12	X	+	-	-
7.942E+01	9.576E-12	X	+	-	-
1.000E+02	1.224E-11	X	+	-	-
1.250E+02	1.576E-11	X	+	-	-
1.333E+02	2.049E-11	X	+	-	-
1.000E+02	2.605E-11	X	+	-	-
2.500E+02	3.553E-11	X	-	-	-
3.162E+02	4.846E-11	X	+	-	-
3.501E+02	6.562E-11	X	-	-	-
5.002E+02	8.945E-11	X	-	-	-
6.310E+02	1.200E-10	X	+	-	-
7.942E+02	1.614E-10	X	+	-	-
1.000E+03	2.120E-10	X	+	-	-
1.250E+03	2.772E-10	X	+	-	-
1.333E+03	3.574E-10	X	+	-	-
1.000E+03	4.573E-10	X	+	-	-
2.500E+03	5.819E-10	X	+	-	-
3.162E+03	7.377E-10	X	+	-	-
3.501E+03	9.320E-10	X	+	-	-
5.002E+03	1.179E-09	X	+	-	-
6.310E+03	1.495E-09	X	+	-	-
7.942E+03	1.872E-09	X	+	-	-
1.000E+04	2.350E-09	X	+	-	-
1.250E+04	2.971E-09	X	+	-	-
1.333E+04	3.741E-09	X	+	-	-
1.000E+04	4.710E-09	X	+	-	-
2.500E+04	5.930E-09	X	+	-	-
3.162E+04	7.467E-09	X	+	-	-
3.501E+04	9.491E-09	X	+	-	-
5.002E+04	1.183E-08	X	+	-	-
6.310E+04	1.499E-08	X	+	-	-
7.942E+04	1.876E-08	X	+	-	-
1.000E+05	2.361E-08	X	+	-	-
1.250E+05	2.973E-08	X	+	-	-
1.333E+05	3.743E-08	X	+	-	-
1.000E+05	4.712E-08	X	+	-	-
2.500E+05	5.932E-08	X	+	-	-
3.162E+05	7.467E-08	X	+	-	-
3.501E+05	9.491E-08	X	+	-	-
5.002E+05	1.183E-07	X	+	-	-
6.310E+05	1.499E-07	X	+	-	-
7.942E+05	1.876E-07	X	+	-	-
1.000E+06	2.361E-07	X	+	-	-
1.250E+06	2.972E-07	X	+	-	-
1.333E+06	3.741E-07	X	+	-	-
1.000E+06	4.710E-07	X	+	-	-
2.500E+06	5.932E-07	X	+	-	-
3.162E+06	7.457E-07	X	+	-	-
3.501E+06	9.360E-07	X	+	-	-
5.002E+06	1.179E-06	X	+	-	-
6.310E+06	1.482E-06	X	+	-	-
7.942E+06	1.861E-06	X	+	-	-
1.000E+07	2.333E-06	X	+	-	-

\*\*\*\*\* 11/07/90 \*\*\*\*\* Pspice 4.01 - July, 1990 \*\*\*\*\* 20:14:40 \*\*\*\*\*

TITLE OPMP.ROUT

\*\*\*\* CIRCUIT DESCRIPTION

```
*****  
*  
*          OUTPUT RESISTANCE MEASUREMENT  
*  
* TRANSISTORS ARE DRAIN GATE SOURCE SUBSTRATE  
*  
*  
* DIFFERENTIAL AMP  
R1 6 20 T T NDEV L=10U N=15U  
R2 5 4 7 7 NDEV L=10U N=15U  
R3 6 6 1 1 PDEV L=10U N=20U  
R4 5 6 1 1 PDEV L=10U N=20U  
R5 7 8 2 2 NDEV L=10U N=30U  
*  
Ccomp 5 0 200PF  
*  
* OUTPUT STAGE  
R6 1 5 9 1 PDEV L=10U N=15U  
R7 9 8 2 2 NDEV L=10U N=30U  
*  
*  
* VOLTAGE BIAS  
R9 10 10 1 1 PDEV L=40U N=12U  
R9 11 11 10 10 PDEV L=40U N=12U  
R10 6 6 11 11 PDEV L=40U N=12U  
R11 8 8 2 2 NDEV L=10U N=30U  
*  
* for output resistance  
*  
IOUT 0 10 AC 1E-6  
VUNIS1 19 0 AC 0  
*  
*  
VDD 1 0 DC 6  
VSS 2 0 DC -6  
VINP 4 0 DC 0  
VINN 3 0 DC 0  
VOS 3 20 DC 0.00797044  
*  
* NOTE: VINN ALSO CONTAINS OFFSET VOLTAGE VOS OF 0.00797044 VOLTS  
*  
*  
.OPTIONS LINPTS=6000 ITL1=5000 NOVDC PIVTOL=1E-15  
.AC DEC 10 10 10NEA  
*  
* OUTPUT RESISTANCE  
.PRINT AC 1(VUNIS1) U(9)  
.PROBE  
*  
.BIRTH OUT=0  
*  
* MODELS  
*  
.MODEL NDEV NMOS LEVEL=1 LD=0.4U TOX=500E-10 NSUB=1E+16 VT0=1.0  
>GMIN=1.3596 PHI=0.6 UD=600 UEXP=0.0 UCR1T=1.0E6 UTRR=0.0  
>DELTA=1.2405 UWR=1E+5 XJ=0.07U LAMBDA=0.02 NF=2E+11 NEFF=1.001E-2  
>NS=0.0 TP=-1.0 RSH=22 CSD=350E-12 CSD0=200E-12 CSD00=350E-12 CJ=300E-0  
>MJ=0.5 CJSW=500E-12 KJSW=0.3  
*  
*  
.MODEL PDEV PMOS LEVEL=1 LD=0.5U TOX=500E-10 NSUB=10.0E+15 VT0=-1.0  
>GMIN=0.079003 PHI=0.6 UD=450 UEXP=0.0 UCR1T=1.0E6 UTRR=0.0  
>DELTA=1.53831 UWR=1E+5 XJ=1.0U LAMBDA=0.02 NF=1.5E+11 NEFF=1.002E-2  
>NS=0.0 TP=1.0 RSH=95 CSD=350E-12 CSD0=350E-12 CSD00=200E-12 CJ=150E-6  
>MJ=0.5 CJSW=400E-12 KJSW=0.23  
*  
.END
```

\*\*\*\*\* 11/17/00 \*\*\*\*\* Pages: 4.04 - July, 1990 \*\*\*\*\* 20:19:40 \*\*\*\*\*

TITLE SWIMP ROUT

\*\*\*\*\* SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

\*\*\*\*\*

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
( 1)	0.0000	( 2)	-0.0000	( 3)	0.0000	( 4)	0.0000
( 5)	3.5724	( 6)	4.3219	( 7)	-1.5779	( 8)	-4.4197
( 9)	3.3523	( 10)	2.5266	( 11)	-0.9104	( 12)	0.0000
( 20)	-0.0000						

VOLTAGE SOURCE CURRENTS  
NAME CURRENT

W1E51	5.352E-12
VDD	-1.011E-04
VSS	1.011E-04
VIMP	0.000E+00
VINN	0.000E+00
VOS	0.000E+00

TOTAL POWER DISSIPATION 1.21E-03 WATTS

\*\*\*\*\* 11/07/90 \*\*\*\*\* Psplus 1.04 - July, 1990 \*\*\*\*\* 20:14:48 \*\*\*\*\*

TITLE SPK99.ROUT

2000 SC RIVLVS15

TEMPERATURE = 27.000 DEG C

FREQ I(MEAS1) U(0)

1.000E+01	1.000E-06	2.393E-02
1.250E+01	1.000E-06	2.393E-02
1.393E+01	1.000E-06	2.393E-02
1.493E+01	1.000E-06	2.393E-02
2.312E+01	1.000E-06	2.393E-02
3.162E+01	1.000E-06	2.393E-02
3.901E+01	1.000E-06	2.393E-02
5.012E+01	1.000E-06	2.393E-02
6.310E+01	1.000E-06	2.393E-02
7.043E+01	1.000E-06	2.393E-02
1.000E+02	1.000E-06	2.393E-02
1.250E+02	1.000E-06	2.393E-02
1.393E+02	1.000E-06	2.393E-02
1.493E+02	1.000E-06	2.393E-02
2.312E+02	1.000E-06	2.393E-02
3.162E+02	1.000E-06	2.393E-02
3.901E+02	1.000E-06	2.393E-02
5.012E+02	1.000E-06	2.393E-02
6.310E+02	1.000E-06	2.393E-02
7.043E+02	1.000E-06	2.392E-02
1.000E+03	1.000E-06	2.392E-02
1.250E+03	1.000E-06	2.392E-02
1.393E+03	1.000E-06	2.392E-02
1.493E+03	1.000E-06	2.392E-02
2.312E+03	1.000E-06	2.392E-02
3.162E+03	1.000E-06	2.392E-02
3.901E+03	1.000E-06	2.392E-02
5.012E+03	1.000E-06	2.392E-02
6.310E+03	1.000E-06	2.392E-02
7.043E+03	1.000E-06	2.392E-02
1.000E+04	1.000E-06	2.392E-02
1.250E+04	1.000E-06	2.392E-02
1.393E+04	1.000E-06	2.392E-02
1.493E+04	1.000E-06	2.392E-02
2.312E+04	1.000E-06	2.392E-02
3.162E+04	1.000E-06	2.392E-02
3.901E+04	1.000E-06	2.392E-02
5.012E+04	1.000E-06	2.392E-02
6.310E+04	1.000E-06	2.392E-02
7.043E+04	1.000E-06	2.392E-02
1.000E+05	1.000E-06	2.392E-02
1.250E+05	1.000E-06	2.392E-02
1.393E+05	1.000E-06	2.392E-02
1.493E+05	1.000E-06	2.392E-02
2.312E+05	1.000E-06	2.392E-02
3.162E+05	1.000E-06	2.392E-02
3.901E+05	1.000E-06	2.392E-02
5.012E+05	1.000E-06	2.392E-02
6.310E+05	1.000E-06	2.392E-02
7.043E+05	1.000E-06	2.392E-02
1.000E+06	1.000E-06	2.392E-02
1.250E+06	1.000E-06	2.392E-02
1.393E+06	1.000E-06	2.392E-02
1.493E+06	1.000E-06	2.392E-02
2.312E+06	1.000E-06	2.391E-02
3.162E+06	1.000E-06	2.390E-02
3.901E+06	1.000E-06	2.390E-02
5.012E+06	1.000E-06	2.387E-02
6.310E+06	1.000E-06	2.384E-02
7.043E+06	1.000E-06	2.379E-02
1.000E+07	1.000E-06	2.371E-02

JOB CONCLUDED

TOTAL JOB TIME

18.22

## **Appendix II**

## **Cross sections**

# RIT PWELL CMOS Process

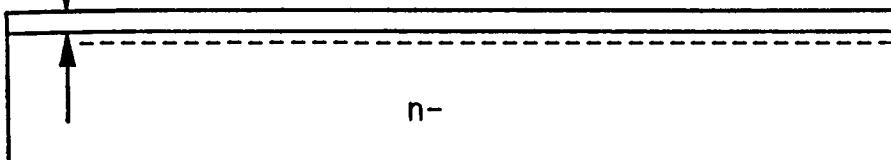
Edward Sayre

Prof. Robert Pearson

Phosphorous 145Kev  $1e12/cm^2$

1000Å

SiO<sub>2</sub>

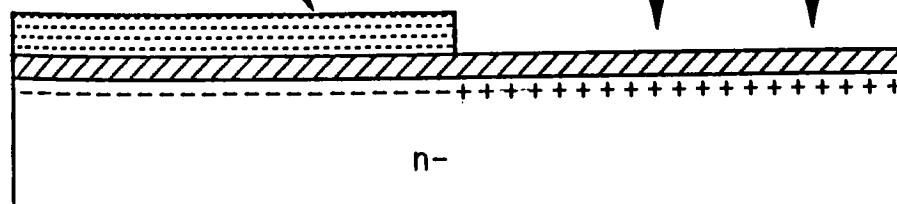


Starting Wafers

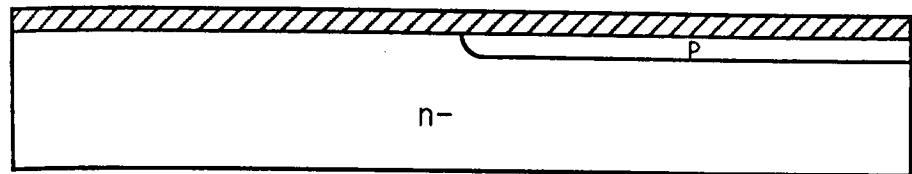
N-type  $\rho = 5-8 \Omega\text{-cm}$   
(N-) Punch Through  
ion implant

Photoresist  
 $\sim 13,000\text{\AA}$

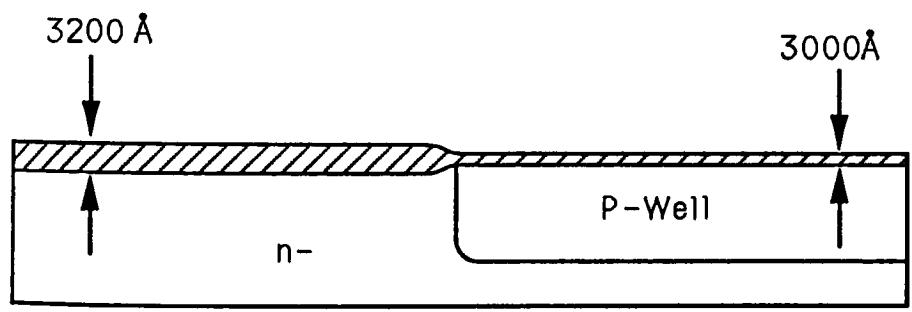
Boron (11) 80Kev  $3e12$



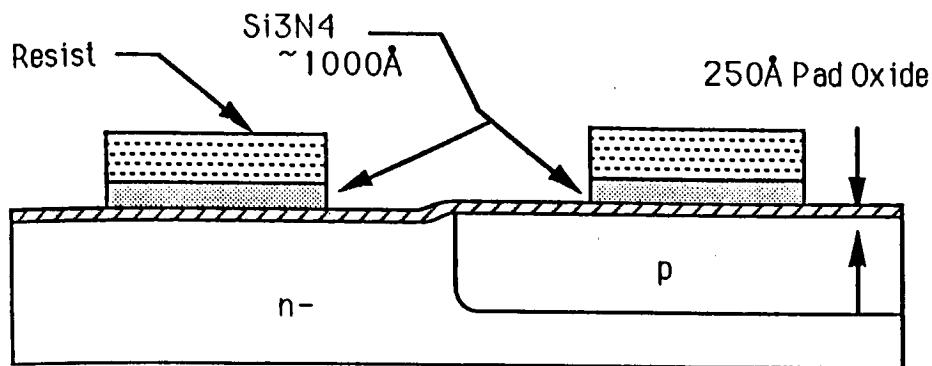
Mask level 1 (Clear Field)  
P-well Ion Implant



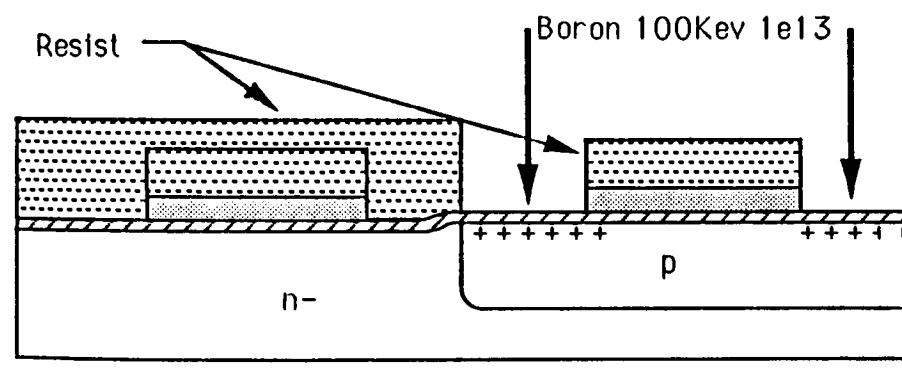
Resist strip and 30  
minute anneal at 1000°C.  
 $X_j = 1\mu\text{m}$



P-well drive-in  
and oxidation  
4 hrs dry O<sub>2</sub>  
5 hrs N<sub>2</sub> at 1150°C  
 $\rho_s = 14K \Omega/\text{cm}^2$   
 $X_j = 3.327 \mu\text{m}$

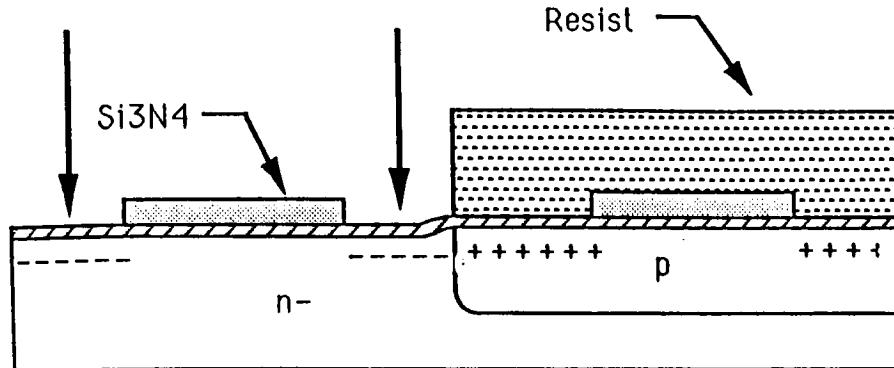


Oxide strip and regrowth of Pad oxide at 950°C for 35 min.  
LPCVD Nitride deposition at  $\approx 800^\circ\text{C}$   
Mask Level 2 (clear field)  
Active/thin oxide  
Si<sub>3</sub>N<sub>4</sub> etched dry in CF<sub>4</sub>

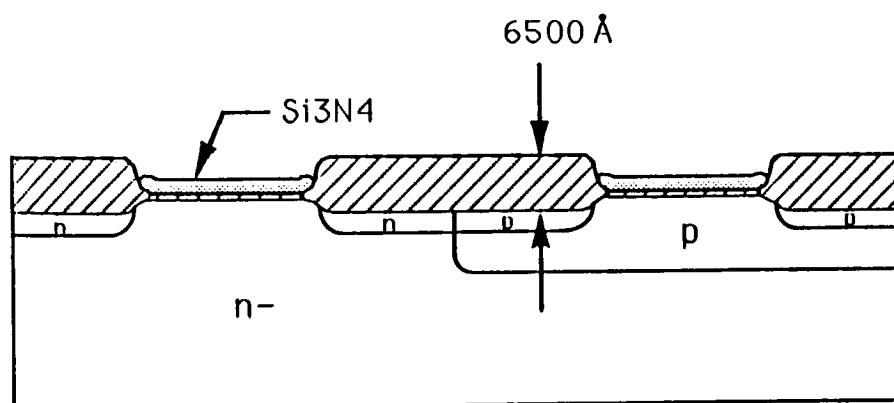


Mask Level 3 (mask level 1)  
Resist from photo level 2 not stripped before level 3 photo step. Field (P-) Ion implant. (2nd level resist was stripped during RIT processing)

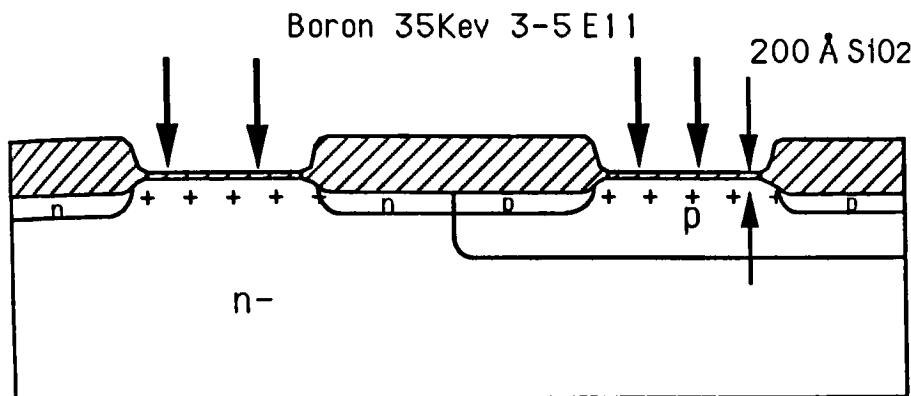
Phosphorous 40Kev 4e12



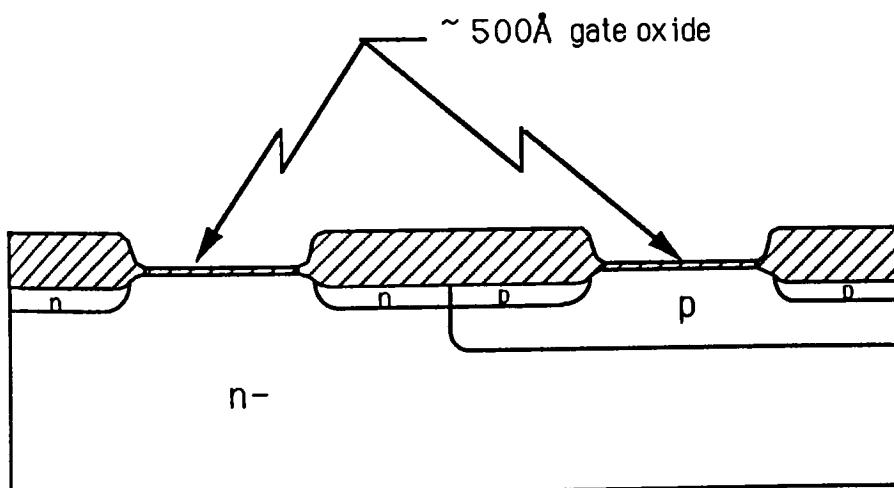
Mask Level 4 (mask level 1  
inverse, dark field).  
Field (N-) ion implant



LOCOS (Field) Oxidation/  
and field adjust drive-in  
5 min dry O<sub>2</sub>, 280 mln  
wel O<sub>2</sub>, 5 min dry O<sub>2</sub>, 20  
min anneal  
 $X_j = 3.775$ ,  $\rho = 5.5\Omega\text{-cm}$   
 $\rho_s = 14.73\text{K}\Omega/\text{in Pwell}$

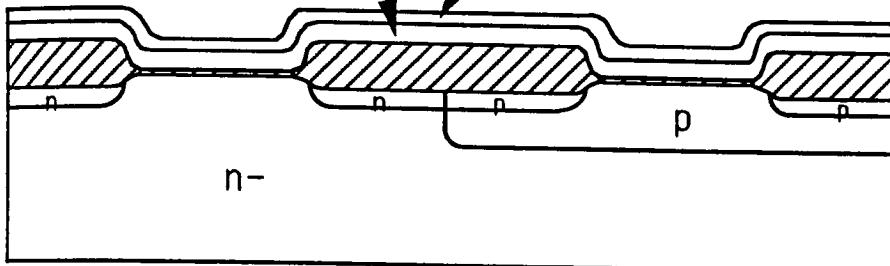


Nitride and pad oxide  
removal regrow 200Å SiO<sub>2</sub>  
Threshold voltage adjust  
Ion Implant  
thin oxide etch

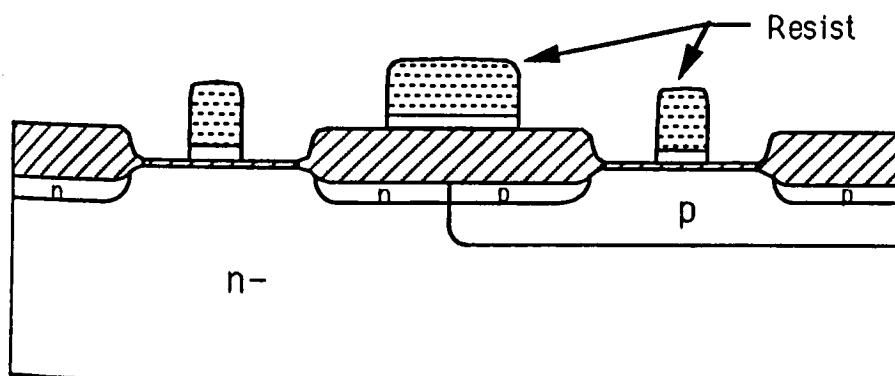


Gate oxidation/ drive in of  
threshold adjust implant  
1.5 hr at 950° C Dry O<sub>2</sub>

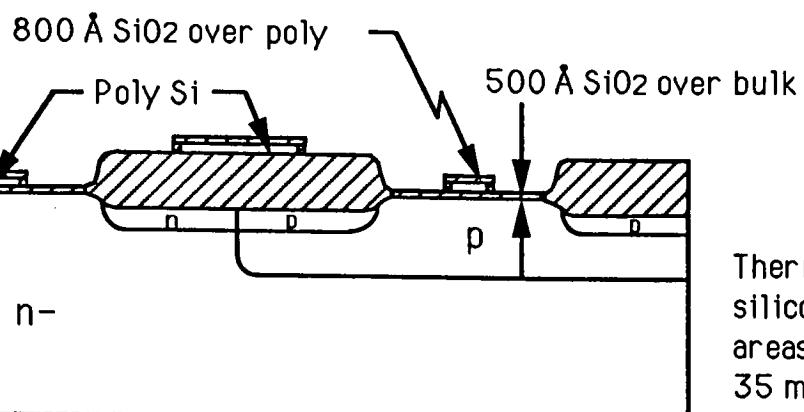
4500Å Polysilicon  
N type Spin on dopant  
 $t \approx 2000\text{\AA}$



Polysilicon Deposition by  
LPCVD at  $610^\circ\text{ C}$   
Doping of polysilicon with  
N-250 spin on dopant  
predep  $1000^\circ\text{ C}$  for 20 min  
 $\rho_s \approx 22 \Omega /$

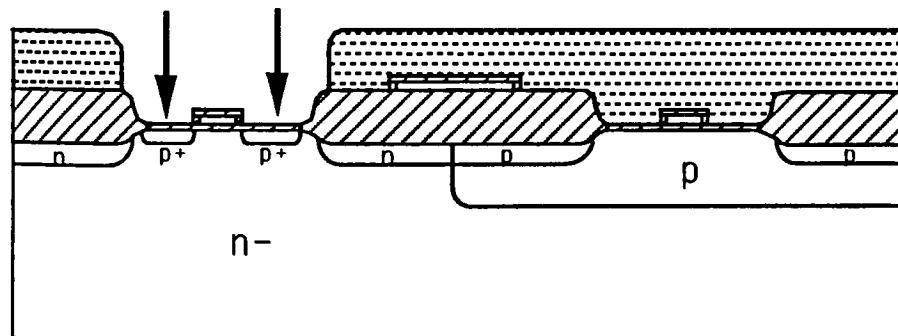


Mask level 5 (clear field)  
Poly Gate definition mask,  
Polysilicon dry etched

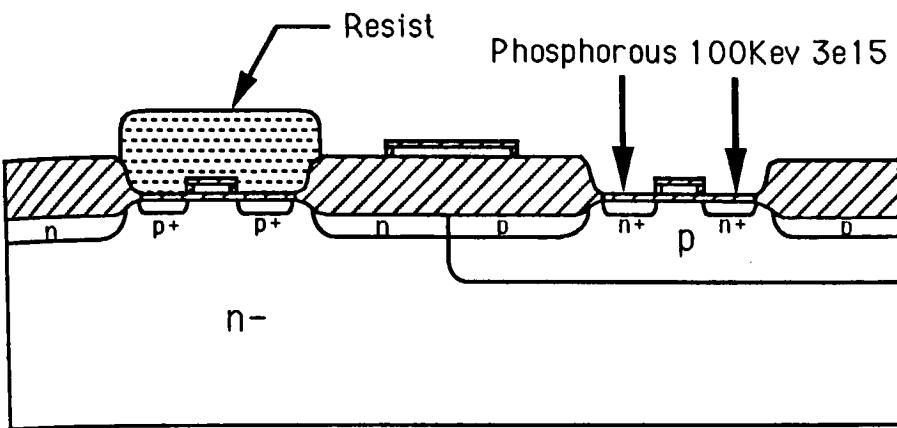


Thermal oxidation of poly-silicon and drain/source areas. 950°C in dry O<sub>2</sub> for 35 min

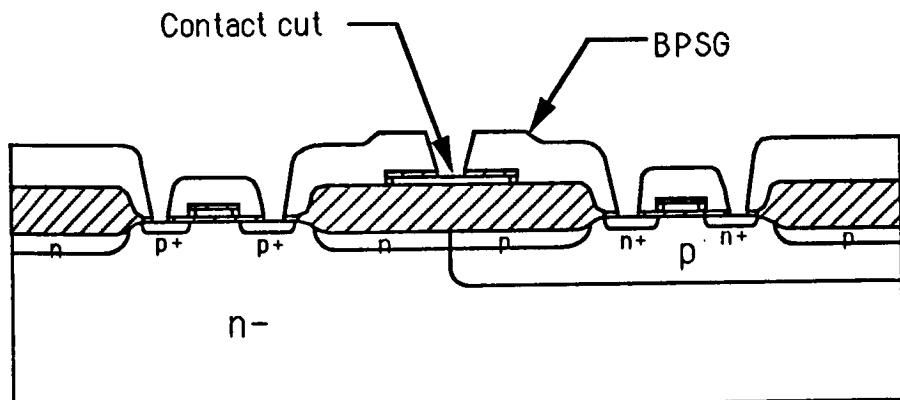
Boron 50Kev 2e15



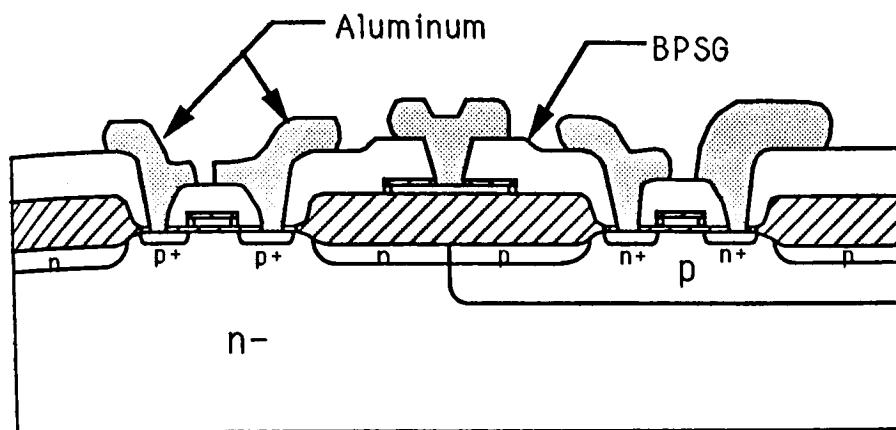
Mask level 6 (dark field) and P+ source/drain implant  
After drive in  
 $\rho_s \approx 46 \Omega /$   
 $X_j = 1.1 \mu\text{m}$



Mask level 7 (clear field)  
and N+ source/drain  
implant. After drive in  
 $\rho_s \approx 24 \Omega /$   
 $X_j = 0.87 \mu\text{m}$



Spin on Glass (BPSG),  $1000^\circ\text{C}$   
for 60 min densification  
Contact cut Mask level 8  
(clear field) contacts  
etched in BHF.



Metallization by evaporation  
of AlSi (3 pellets  $\approx$  3500Å)  
Mask level 9 (clear field)  
metal photo mask  
Al wet Etched

## Process Summary

PWELL Junction Depth	3.6 $\mu\text{m}$
PWELL Sheet Resistance	14K $\Omega/\square$
P+ D/S Junction Depth	1.1 $\mu\text{m}$
P+ D/S Sheet Resistance	45 $\Omega/\square$
N+ D/S Junction Depth	0.87 $\mu\text{m}$
N+ D/S Sheet Resistance	24 $\Omega/\square$
Polysilicon Thickness	4500 Å
Polysilicon Sheet resistance	22 $\Omega/\square$
Field Oxide thickness	6000 Å
Gate Oxide thickness	500 Å
Spin on Glass thickness	5000 Å

## **Appendix III**

### **Process steps**

## RIT CMOS PROCESS 1.0

7/18/90

<u>Processing Level</u>	<u>Task Numbers</u>
Mask Making . . . . .	A-0
PWELL . . . . .	7-15
PWELL Drive in . . . . .	16-21
Pad Oxide . . . . .	22-24
Nitride and Active Region . . . . .	25-31
Pwell Field Adjust Implant . . . . .	32-36
N Field Adjust Implant . . . . .	37-40
LOCOS . . . . .	41-47
Device Threshold Adjust . . . . .	48-53
Gate Oxide . . . . .	54-55
Polysilicon . . . . .	56-66
Oxidize Polysilicon . . . . .	67-68
P+ type Source/Drain . . . . .	69-74
N+ type Source/Drain . . . . .	75-78
Backside Etches . . . . .	80-82
Spin on Glass . . . . .	83-93
Metalization . . . . .	94-100

Mask Making - Assumptions; Mann file generated, Pattern generator set up properly, Size and split run,

<u>Process step</u>	<u>Process step Description</u>
A	Load Mask plate up and expose on PG
B	Unload mask plate and label (Clear Field Mask Process)
C	Develop for 3 minutes in 4:1 developer/DI
D	Stop for 30 seconds in ~200:1 DI/Stopper
E	Fix for 2 minutes in fixer
F	DI Rinse for 2 minutes
G	Blow plate dry
H	Inspection
( Reversal, Dark Field, Process)	
I	Develop for 10 minutes in 2:1 developer/DI
J	Bleach for 5 min in Bleach (1L H <sub>2</sub> O, 9.5mg K <sub>2</sub> Cr <sub>2</sub> O <sub>7</sub> , 0.2 ml H <sub>2</sub> SO <sub>4</sub> )
K	Clear for 5 min in clear mixture (1L H <sub>2</sub> O 90 gm NaSO)
L	DI rinse for 30 seconds
M	Blow plate dry
N	Expose with light source for 30 seconds
O	Standard clear field development process

<u>Masking levels</u>	<u>Type of mask</u>
1	Pwell (dark field, reversal process)
2	Active/Thin Oxide (clear field)
3	P- Field adjust (same as level 1)
4	N- Field adjust (Clear field, inverse of level 1)
5	Poly/Gate definition (clear Field)
6	P+ S/D (dark field, reversal process of level 7 )
7	N+ S/D ( Clear field)
8	Contact Cut (Dark Field, reversal process)
9	Metal 1 (Clear Field)

<u>Task #</u>	<u>Device Wafers</u>	<u>Control Wafers</u>	<u>Task Description</u>
1	all	all	Scribe
2	2,7,12	17,22	Four point probe
3	all	all	Standard RCA clean
4	all	all	Oxidation, 1000° C, 11.5min Wet O2 3.5 slpm; Target; tox=1000Å
5	2,7,12	all	Nanospec
6	all	all	Implant P+ (31amu) Dose=1e12, Energy=145Kev
7	all	none	Photoresist coat, trac line 3 Program 6
8	all	none	Expose Pwell mask dark field (level 1)
9	all	none	Standard develop wafer Trac
10	all	16-21	Pwell Implant B(11) Dose=3e12, Energy=80Kev
11	all	all	Anneal, temp=1000°C, Time=30 min, 4 slpm N2
12	none	21	Grove and Stain
13	even #'s	even #'s	Four point probe
14	all	16-21	Buffered HF etch of oxide Until wafers dewet (~2min)
15	all	None	Plasma ash (~15min)
16	all	all	Standard RCA Clean
17	all	all	Oxidation/drivein with TCA Clean. Temp=1150°C, 4 hrs 4 slpm Oxygen. 5 hrs 4 slpm Nitrogen Temp=1150°C Total time=9 hours Target; Xj=3.3um, tox=3000Å
18	even #'s	all	Measure Oxide thickness
19	all	all	Buffered HF strip of oxide
20	none	all	Four point probe
21	none	21	Grove and stain
22	all	16-21	RCA clean

<u>Task #</u>	<u>Device Wafers</u>	<u>Control Wafers</u>	<u>Task Description</u>
23	all	16-21	Oxide growth with TCA clean Temp=950°C, 35 min 4 slpm dry oxygen. Target; tox=200 Å
24	even*'s	16-21	Measure oxide thickness
25*	all	16-21	LPCVD Nitride deposition 14 min deposition Temp=(L)703°, (C)795°, (S)813°; 31% NH <sub>3</sub> , 30% SiH <sub>2</sub> C <sub>12</sub> , Recipe #2; Target; tox=1000Å
26	none	Dummies	Measure Nitride thickness from bare Si dummies
27	all	none	Photoresist coat, trac line 3 Program 7
28	all	none	Expose Active mask, clear Field (level 2)
29	all	none	Standard develop (line2 Prog2)
30	all	22,23	Dry etch nitride with 13 sccm CF <sub>4</sub> at 100 watts
31*	all	none	Standard O <sub>2</sub> plasma ash
32	1-4,6-14	none	Photoresist coat, trac Line 3 Program 7
33	1-4,6-14	none	Expose Pwell dark field same as level 1(level3)
34	1-4,6-15	none	Standard develop (line2 prog2)
35	1-4,6-14	all	Field adjust Ion Implant B(11), Dose=1E13, Energy=100Kev
36	all	none	Standard O <sub>2</sub> plasma ash
37	1-4,6-9,11-15	none	Photoresist coat, trac line 3 Program 6
38	1-4,6-9,11-15	none	Expose Pwell clear field, Same as mask level1 (level 4)
39	1-4,6-9,11-15	all	Field adjust Ion Implant P(31), Dose=5e12, Energy=40kev

<u>Task #</u>	<u>Device Wafers</u>	<u>Control Wafers</u>	<u>Task Description</u>
40	all	none	O2 plasma ash resist strip
41	all	all	Standard RCA clean
42	all	all	TCA Tube clean at 950° C 5 min Dry O2, 4 hrs 40 min Wet O2, 5 min Dry O2, 20 min N2 anneal Target; tox= 6500Å
43	all	all	1 min 10:1 HF dip and DI rinse
44	all	16-21,23-25	Nitride etch of fronts and Backs as previously etched
45	all	all	Etch pad oxide 10:1 HF, 2min
46	none	21	Grove and stain for Pwell Xj
47	none	18	Four point probe for sheet rho
48	all	all	Standard RCA clean
49	all	all	Oxidation for implant 950°C, for 30 min Dry O2; Target, tox=200Å
50	1,2,3		Threshold Adjust Ion Implant Dose=3e11, Energy=35kev
51	4,5,6,7,10,15	17	Threshold Adjust Ion Implant Dose=4e11, Energy=35kev
52	8,9,11	18	Threshold Adjust Ion Implant Dose=5e11, Energy=35kev
53	all	all	Strip of Implant oxide Buffered HF for 30 sec
54	all	all	Standard RCA clean
55	all	all	Gate Oxide,TCA tube clean 950°C, time=1.5hours, 3slpm Dry O2, Target; tox=500Å

<u>Task #</u>	<u>Device Wafers</u>	<u>Control Wafers</u>	<u>Task Description</u>
56	all	all	LPCVD Poly silicon deposition, Temp=611°C SiH4=45% Dep. time= 52min, Recipe #1,Target; t=4500Å
57*	all	all	Doping of poly layer N-250 dopant Spin 3000 rpm 30sec
58	all	all	Prebake at 200°C, 15 min
59	all	all	Predep 20 min @1000°C 2 slpm N2
60	all	all	Dopant Strip 10:1 HF, 3 min
61	all	all	Four point probe
62	all	none	Photoresist coat,trac line 3 Program 7
63	all	none	Expose with Gate oxide mask (level 5)
64	all	none	Standard develop line 2 program 2
65	all		Poly Si etch Dry using 10sccm-SF6,3.3-02 100 Watts
66	all	none	O2 plasma ash
67	all	all	RCA clean ; EXCEPT <b>10 Sec Max 10:1 HF dip</b>

<u>Task #</u>	<u>Device Wafers</u>	<u>Control Wafers</u>	<u>Task Description</u>
68	all	all	Reoxidation,TCA tube clean 950°C for 35 min Dry O2, Target (Si) tox=500Å, tox=800Å
69	all	none	Photoresist coat, trac line 3 program 7
70	all	none	Expose with Ptype S&D mask Dark field (level 7)
71	all	none	Standard develop
72	2,3,6,9-11,13,15	17-25	S&D Ion Implant B(11) Ptype Dose=2e15, Energy=50Kev
73	1,4,8,12	none	S&D Ion Implant BF2(48) Dose=2e15, Energy=50Kev
74	all	none	O2 Plasma Ash
75	all	none	Expose with Ntype S&D mask Clear field (level 6)
76	all	none	Standard develop line 2 program 2
77*	all	16,18-21,23-25	S&D Ion Implant P(31) Ntype, Dose=3e15, Energy=100Kev
78	all	none	O2 Plasma ash
79	all	all	Photoresist coat, trac line 3, Program 7
80	all	all	Etch backsides of wafers Buffered HF dip Poly silicon etch (wet) Buffered HF dip (until Dewets)
81	none	16,23	Grove and Stain
82	all	all	Standard RCA Clean
83	all	dummies	Spin On Glass, BPSG Emulsitone Solution#827 @3000rpm for 30sec
84	all	dummies	Prebake 200°C, 40 min
85	all	dummies	Postbake 1000°C, 60 min, N2
86	none	dummies	Step etch

<u>Task #</u>	<u>Device Wafers</u>	<u>Control Wafers</u>	<u>Task Description</u>
87	all	none	Photoresist coat, trac Line 3, Program 7
88	all	none	Expose Contact cut Mask Dark Field (level 8)
89	all	none	Standard develop line2 prog2
90	all	none	O2 Plasma Descum 50 watts for 2 min
91	all	none	Contact cut etch BHF
92	all	none	O2 Plasma Ash
93	all	none	Dehydration bake 600°C for 15min, N2
94	all	none	Aluminum evaporation 3 pellets, target t=3500Å
95	all	none	Sinter 450°C, 30 min 5 s1pm H2O2
96	all	none	Photoresist Coat, trac Line 3, Program 4
97	all	none	Expose Metal Mask clear field (level 9)
98	all	none	Standard Develop line 2 program 2
99	all	none	Aluminum etch at 40°C
100	all	none	O2 plasma ash

## **Appendix IV**

### **Simulations of closed loop circuits**

#### **TABLE 1**

**1. CIRCUIT DESCRIPTION**

TITLE INTEGRATOR

\*\*\*\*\* MOSFET MODEL PARAMETERS

	NDEU	PDEU
	NMOS	PMOS
LEVEL	2	2
TP0	-1	
LB	400.00000E-09	300.00000E-09
VTO	1	-1
KP	55.23000E-06	31.070290E-06
DMIN	1.3504	.879003
PHI	.6	.6
LARDA	.02	.02
RSH	.22	.95
CJ	500.00000E-06	150.00000E-06
CJSU	500.00000E-12	400.00000E-12
ILSH	.9	.25
CSSB	350.00000E-12	350.00000E-12
CSD0	350.00000E-12	350.00000E-12
CSD0	200.00000E-12	200.00000E-12
NSUB	10.00000E+15	10.00000E+15
NBS	0	0
NP3	200.00000E+09	150.00000E+09
TBX	50.00000E-09	50.00000E-09
XJ	870.00000E-09	1.00000E-06
UD	600	130
MCIT	1.00000E+06	1.00000E+06
WWR	100.00000E+03	100.00000E+03
WEFF	.01001	.01002
DELTA	1.2403	1.93631

## TITLE INTEGRATOR

BEGG DC TRANSFER CURVES

TEMPERATURE = 27.000 DEG C

U(111)	U(9)
(1)	-6.0000E+00
-8.0000E-03	5.3000E+00
-7.5000E-03	5.404E+00
-7.0000E-03	5.406E+00
-6.5000E-03	5.410E+00
-6.0000E-03	5.413E+00
-5.5000E-03	5.396E+00
-6.0000E-03	5.365E+00
-4.5000E-03	5.326E+00
-4.0000E-03	5.274E+00
-3.5000E-03	5.184E+00
-3.0000E-03	4.814E+00
-2.5000E-03	3.994E+00
-2.0000E-03	3.151E+00
-1.5000E-03	2.387E+00
-1.0000E-03	1.666E+00
-5.0000E-04	8.090E-01
0.0000E+00	5.057E-05
5.0000E-04	-8.205E-01
1.0000E-03	-1.049E+00
1.5000E-03	-2.408E+00
2.0000E-03	-3.311E+00
2.5000E-03	-4.131E+00
3.0000E-03	-4.926E+00
3.5000E-03	-5.652E+00
4.0000E-03	-5.720E+00
4.5000E-03	-5.764E+00
5.0000E-03	-5.778E+00
5.5000E-03	-5.801E+00
6.0000E-03	-5.819E+00
6.5000E-03	-5.835E+00
7.0000E-03	-5.849E+00
7.5000E-03	-5.862E+00
8.0000E-03	-5.874E+00

\*\*\*\*\* 11/07/90 \*\*\*\*\* FSplice 4.04 - July, 1990 \*\*\*\*\* 20:06:32 \*\*\*\*\*

TITLE INTEGRATOR

\*\*\*\*\* SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

---

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
( 1)	0.0000	( 2)	-0.0000	( 3)	0.0000	( 5)	0.0000
( 9)-1.677E-06 ( X1.5)	3.9963 ( X1.6)	4.3145 ( X1.7)	-1.5910				
( X1.8)	-4.3923 ( X1.10)	2.5550 ( X1.11)	-.9263 ( X1.20)				
							.0000

VOLTAGE SOURCE CURRENTS

NODE	CURRENT
000	-7.010E-05
005	7.816E-05
010	0.000E+00
X1.003	0.000E+00

TOTAL POWER DISSIPATION 0.42E-01 WATTS

## TITLE INTEGRATOR

\*\*\* IC ANALYSIS

TEMPERATURE = 27.000 DEG C

## LEGEND:

+: UN(0)

FREQ UN(0)

(s)	1.000E+02	1.000E+00	1.000E+02	1.000E+01	1.000E+00
1.000E+01	1.000E+02	.	.	.	.
1.250E+01	1.257E+02	.	.	.	.
1.500E+01	9.990E+01	.	.	.	.
1.750E+01	7.946E+01	.	.	.	.
2.512E+01	8.314E+01	.	.	.	.
3.162E+01	5.017E+01	.	.	.	.
3.501E+01	3.900E+01	.	.	.	.
5.012E+01	3.166E+01	.	.	.	.
6.310E+01	2.915E+01	.	.	.	.
7.412E+01	1.998E+01	.	.	.	.
1.000E+02	1.587E+01	.	.	.	.
1.250E+02	1.261E+01	.	.	.	.
1.500E+02	1.001E+01	.	.	.	.
1.750E+02	7.055E+00	.	.	.	.
2.512E+02	8.319E+00	.	.	.	.
3.162E+02	5.020E+00	.	.	.	.
3.501E+02	3.907E+00	.	.	.	.
5.012E+02	3.167E+00	.	.	.	.
6.310E+02	2.916E+00	.	.	.	.
7.412E+02	1.999E+00	.	.	.	.
1.000E+03	1.588E+00	.	.	.	.
1.250E+03	1.262E+00	.	.	.	.
1.500E+03	1.003E+00	.	.	.	.
1.750E+03	7.070E-01	.	.	.	.
2.512E+03	8.320E-01	.	.	.	.
3.162E+03	5.023E-01	.	.	.	.
3.501E+03	3.917E-01	.	.	.	.
5.012E+03	3.174E-01	.	.	.	.
6.310E+03	2.917E-01	.	.	.	.
7.412E+03	2.057E-01	.	.	.	.
1.000E+04	1.662E-01	.	.	.	.
1.250E+04	1.354E-01	.	.	.	.
1.500E+04	1.119E-01	.	.	.	.
1.750E+04	9.490E-02	.	.	.	.
2.512E+04	8.105E-02	.	.	.	.
3.162E+04	7.367E-02	.	.	.	.
3.501E+04	6.941E-02	.	.	.	.
5.012E+04	6.201E-02	.	.	.	.
6.310E+04	7.105E-02	.	.	.	.
7.412E+04	7.056E-02	.	.	.	.
1.000E+05	6.931E-02	.	.	.	.
1.250E+05	1.244E-01	.	.	.	.
1.500E+05	1.244E-01	.	.	.	.
1.750E+05	1.495E-01	.	.	.	.
2.512E+05	1.801E-01	.	.	.	.
3.162E+05	2.156E-01	.	.	.	.
3.501E+05	2.349E-01	.	.	.	.
5.012E+05	2.056E-01	.	.	.	.
6.310E+05	3.345E-01	.	.	.	.
7.412E+05	3.683E-01	.	.	.	.
1.000E+06	3.943E-01	.	.	.	.
1.250E+06	4.108E-01	.	.	.	.
1.500E+06	4.172E-01	.	.	.	.
1.750E+06	4.134E-01	.	.	.	.
2.512E+06	3.994E-01	.	.	.	.
3.162E+06	3.750E-01	.	.	.	.
3.501E+06	3.130E-01	.	.	.	.
5.012E+06	3.866E-01	.	.	.	.
6.310E+06	2.856E-01	.	.	.	.
7.412E+06	2.256E-01	.	.	.	.
1.000E+07	1.853E-01	.	.	.	.

TITLE INTEGRATOR

\*\*\*\*\* DC ANALYSIS

TEMPERATURE = 27.000 DEG C

FREQ WAVE(0)

(Hz)	-1.0000E+02	-5.0000E+01	0.0000E+00	5.0000E+01	1.0000E+02
1.000E+01	9.331E+01	.	.	.	.
1.250E+01	9.130E+01	.	.	.	.
1.385E+01	9.345E+01	.	.	.	.
1.995E+01	9.277E+01	.	.	.	.
2.512E+01	9.220E+01	.	.	.	.
3.162E+01	9.174E+01	.	.	.	.
3.991E+01	9.130E+01	.	.	.	.
5.012E+01	9.110E+01	.	.	.	.
6.310E+01	9.087E+01	.	.	.	.
7.943E+01	9.069E+01	.	.	.	.
1.000E+02	9.054E+01	.	.	.	.
1.250E+02	9.042E+01	.	.	.	.
1.585E+02	9.033E+01	.	.	.	.
1.995E+02	9.025E+01	.	.	.	.
2.512E+02	9.019E+01	.	.	.	.
3.162E+02	9.014E+01	.	.	.	.
3.991E+02	9.009E+01	.	.	.	.
5.012E+02	9.005E+01	.	.	.	.
6.310E+02	9.001E+01	.	.	.	.
7.943E+02	9.000E+01	.	.	.	.
1.000E+03	9.000E+01	.	.	.	.
1.250E+03	9.000E+01	.	.	.	.
1.585E+03	9.000E+01	.	.	.	.
1.995E+03	9.000E+01	.	.	.	.
2.512E+03	9.000E+01	.	.	.	.
3.162E+03	9.000E+01	.	.	.	.
3.991E+03	9.000E+01	.	.	.	.
5.012E+03	9.000E+01	.	.	.	.
6.310E+03	9.000E+01	.	.	.	.
7.943E+03	9.000E+01	.	.	.	.
1.000E+04	9.000E+01	.	.	.	.
1.250E+04	9.000E+01	.	.	.	.
1.385E+04	9.000E+01	.	.	.	.
1.995E+04	9.000E+01	.	.	.	.
2.512E+04	9.000E+01	.	.	.	.
3.162E+04	9.000E+01	.	.	.	.
3.991E+04	9.000E+01	.	.	.	.
5.012E+04	9.000E+01	.	.	.	.
6.310E+04	9.000E+01	.	.	.	.
7.943E+04	9.000E+01	.	.	.	.
1.000E+05	9.000E+01	.	.	.	.
1.250E+05	9.000E+01	.	.	.	.
1.385E+05	9.000E+01	.	.	.	.
1.995E+05	9.000E+01	.	.	.	.
2.512E+05	9.000E+01	.	.	.	.
3.162E+05	9.000E+01	.	.	.	.
3.991E+05	9.000E+01	.	.	.	.
5.012E+05	9.000E+01	.	.	.	.
6.310E+05	9.000E+01	.	.	.	.
7.943E+05	9.000E+01	.	.	.	.
1.000E+06	9.000E+01	.	.	.	.
1.250E+06	9.000E+01	.	.	.	.
1.385E+06	9.000E+01	.	.	.	.
1.995E+06	9.000E+01	.	.	.	.
2.512E+06	9.000E+01	.	.	.	.
3.162E+06	9.000E+01	.	.	.	.
3.991E+06	9.000E+01	.	.	.	.
5.012E+06	9.000E+01	.	.	.	.
6.310E+06	9.000E+01	.	.	.	.
7.943E+06	9.000E+01	.	.	.	.
1.000E+07	9.000E+01	.	.	.	.
1.250E+07	9.000E+01	.	.	.	.

JOB CONCLUDED

TOTAL JOB TIME

16.32

## TITLE DIFFERENTIATOR

## \*\*\*\*\* CIRCUIT DESCRIPTION \*\*\*\*\*

```

* CIRCUIT SPICE USED IN DIFFERENTIATOR
* TRANSISTORS ARE DRAIN GATE SOURCE SUBSTRATE
*
* SICKET SPICE 1 2 3 4 9
*
* DIFFERENTIAL AMP
B1 6 3 7 7 MDEV L=10U N=15U
R2 3 9 7 7 MDEV L=10U N=15U
R3 6 6 1 1 MDEV L=10U N=20U
M 5 6 1 1 MDEV L=10U N=20U
R5 7 8 2 2 MDEV L=10U N=30U
*
Ccomp 3 8 200PF
*
* OUTPUT STAGE
M6 1 5 9 1 MDEV L=10U N=15U
R7 9 8 2 2 MDEV L=10U N=30U
*
* VOLTAGE DIVS
R8 10 10 1 1 MDEV L=40U N=12U
R9 11 11 10 10 MDEV L=10U N=12U
R10 8 8 11 11 MDEV L=10U N=12U
R11 8 8 2 2 MDEV L=10U N=30U
*
*
*
VBS 20 4 DC 0.00797944
*
.EOP
*
* POWER SUPPLIES
*
VDD 1 0 DC 6
VSS 2 0 DC -6
*
* INPUT SIGNALS
*
VINH 3 0 DC 0 AC 1
VINLP 4 0 DC 0 AC 1
*
* Rail circuit
* Add bias Vin- Vin+ Vout
R1 1 2 5 6 9 SPWTF
*
C1 3 5 1PF
R1 0 5 1MEG
*
*
.OPTIONS L1WPTG=0.0001 ITL1=5000 PIOTOL=1E-15
.AC VINH -6E-3 DE-3 0.0005
.PLOT DC V(9) (-6,6)
.AC DEC 10 10 10MEG
.PLOT DC VIN(9)
.PLOT AC VP(0)
.PROBE
*
*
.MATH OUT=0
*
* MODELS
*
.MODEL MDEV MN02 LEVEL=2 LD=0.1U TON=500E-10 NSUB=1E+16 VT0=-1.0
+RSH=1.35E6 PHI=0.6 UD=0.0001 UEP=0.0 UCRT=1.0E6 UTRM=0.0
+DELTA=1.2105 VINH=1E+5 XJ=0.87U LAMBDA=0.02 NEF=2E+11 NEFF=1.001E-2
+NEP=0.0 TPF=1.0 RSH=22 CSD0=350E-12 CSD0=200E-12 CSD0=350E-12 CJ=300E-6
+XJ=0.5 CJS0=500E-12 KLSH=0.3
*
*
.MODEL PDEV PM02 LEVEL=2 LD=0.5U TON=500E-10 NSUB=1E+15 VT0=-1.0
+RSH=0.670003 PHI=0.6 UD=450 UEP=0.0 UCRT=1.0E6 UTRM=0.0
+DELTA=1.53E3 VINH=1E+5 XJ=1.0U LAMBDA=0.02 NEF=1.0E+11 NEFF=1.002E-2
+NEP=0.0 TPF=1.0 RSH=65 CSD0=550E-12 CSD0=200E-12 CSD0=350E-12 CJ=150E-6
+XJ=0.5 CJS0=400E-12 KLSH=0.25
*
*
.EOP

```

\*\*\*\*\* 11/07/90 \*\*\*\*\* PSpice 1.01 - July, 1990 \*\*\*\*\* 20:00:26 \*\*\*\*\*

TITLE DIFFERENTIATOR

\*\*\*\*\* MOSFET MODEL PARAMETERS

	MDEV	PDEV
	MROS	PROS
LEVEL	2	2
TP0	-1	
LB	400.00000E-09	300.00000E-09
UTB	1	-1
KF	33.290300E-06	31.076270E-06
BFRM	1.3506	.079003
PHI	.6	.6
LAMBDA	.02	.02
NSR	.22	.95
CJ	300.00000E-06	150.00000E-06
CJSR	300.00000E-12	400.00000E-12
CMW	.3	.25
CSD0	350.00000E-12	350.00000E-12
CSD0	350.00000E-12	350.00000E-12
CSD0	200.00000E-12	200.00000E-12
NEUB	10.00000E+15	10.00000E+15
NFG	0	0
NFS	200.00000E+09	150.00000E+09
TOR	50.00000E-09	50.00000E-09
BL	870.00000E-09	1.00000E-06
VO	500	450
MCNT	1.00000E+06	1.00000E+06
WMRM	100.00000E+03	100.00000E+03
MEFF	.01001	.01002
DELTR	1.2405	1.53531

## TITLE DIFFERENTIATOR

DC TRANSFER CURVES

TEMPERATURE = 27.000 DEG C

VIN	V(0)					
(V)	-6.000E+00	-3.000E+00	0.000E+00	3.000E+00	6.000E+00	
-8.000E-03	-1.490E-07	.	.	.	.	
-7.500E-03	-6.004E-08	.	.	.	.	
-7.000E-03	-6.004E-08	.	.	.	.	
-6.500E-03	-6.004E-08	.	.	.	.	
-6.000E-03	-6.004E-08	.	.	.	.	
-5.500E-03	-6.004E-08	.	.	.	.	
-5.000E-03	-6.004E-08	.	.	.	.	
-4.500E-03	-6.004E-08	.	.	.	.	
-4.000E-03	-6.004E-08	.	.	.	.	
-3.500E-03	-6.004E-08	.	.	.	.	
-3.000E-03	-6.004E-08	.	.	.	.	
-2.500E-03	-6.004E-08	.	.	.	.	
-2.000E-03	-6.004E-08	.	.	.	.	
-1.500E-03	-6.004E-08	.	.	.	.	
-1.000E-03	-6.004E-08	.	.	.	.	
-5.000E-04	-6.004E-08	.	.	.	.	
0.000E+00	-6.004E-08	.	.	.	.	
5.000E-04	-6.004E-08	.	.	.	.	
1.000E-03	-6.004E-08	.	.	.	.	
1.500E-03	-6.004E-08	.	.	.	.	
2.000E-03	-6.004E-08	.	.	.	.	
2.500E-03	-6.004E-08	.	.	.	.	
3.000E-03	-6.004E-08	.	.	.	.	
3.500E-03	-6.004E-08	.	.	.	.	
4.000E-03	-6.004E-08	.	.	.	.	
4.500E-03	-6.004E-08	.	.	.	.	
5.000E-03	-6.004E-08	.	.	.	.	
5.500E-03	-6.004E-08	.	.	.	.	
6.000E-03	-6.004E-08	.	.	.	.	
6.500E-03	-6.004E-08	.	.	.	.	
7.000E-03	-6.004E-08	.	.	.	.	
7.500E-03	-6.004E-08	.	.	.	.	
8.000E-03	-6.004E-08	.	.	.	.	

\*\*\*\*\* 11/07/90 \*\*\*\*\* PSpice 4.04 - July, 1990 \*\*\*\*\* 20:00:26 \*\*\*\*\*

TITLE DIFFERENTIATOR

\*\*\*\*\* SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
( 1 )	0.0000	( 2 )	-0.0000	( 3 )	0.0000	( 5 )	-149.0E-09
( 9 )	-149.0E-09	( X1.5 )	3.9863	( X1.6 )	4.3145	( X1.7 )	-1.5948
( X1.8 )	-4.3925	( X1.10 )	2.5358	( X1.11 )	-0.9263	( X1.20 )	.0000

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VDD	-7.016E-05
VSS	7.016E-05
U1INN	0.000E+00
X1.003	0.000E+00

TOTAL POWER DISSIPATION 0.42E-04 WATTS

## TITLE DIFFERENTIATOR

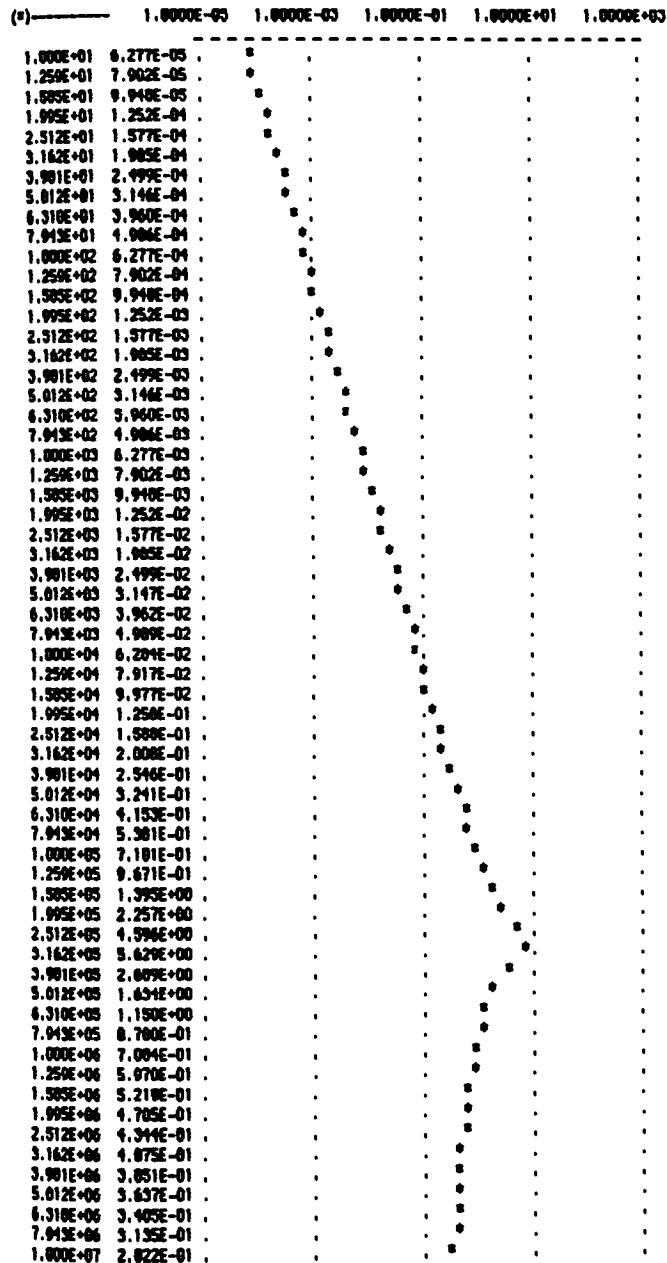
AC ANALYSIS

TEMPERATURE = 27.000 DEG C

## LEGEND:

o: UN(0)

FREQ V(0)



## TITLE DIFFERENTIATOR

\*\*\*\*\* TC ANALYSIS

TEMPERATURE = 27.000 DEG C

FREQ UP(0)

(Hz)	-2.0000E+02	-1.0000E+02	0.0000E+00	1.0000E+02	2.0000E+02
1.000E+01	-9.000E+01	.	*	.	.
1.250E+01	-8.000E+01	.	*	.	.
1.305E+01	-8.000E+01	.	*	.	.
1.395E+01	-8.000E+01	.	*	.	.
2.512E+01	-8.000E+01	.	*	.	.
3.162E+01	-8.000E+01	.	*	.	.
3.901E+01	-8.000E+01	.	*	.	.
5.012E+01	-8.001E+01	.	*	.	.
6.310E+01	-8.001E+01	.	*	.	.
7.945E+01	-8.001E+01	.	*	.	.
1.000E+02	-8.001E+01	.	*	.	.
1.250E+02	-8.001E+01	.	*	.	.
1.585E+02	-8.002E+01	.	*	.	.
1.995E+02	-8.002E+01	.	*	.	.
2.512E+02	-8.003E+01	.	*	.	.
3.162E+02	-8.003E+01	.	*	.	.
3.901E+02	-8.004E+01	.	*	.	.
5.012E+02	-8.005E+01	.	*	.	.
6.310E+02	-8.007E+01	.	*	.	.
7.945E+02	-8.008E+01	.	*	.	.
1.000E+03	-8.010E+01	.	*	.	.
1.250E+03	-8.013E+01	.	*	.	.
1.585E+03	-8.016E+01	.	*	.	.
1.995E+03	-8.021E+01	.	*	.	.
2.512E+03	-8.026E+01	.	*	.	.
3.162E+03	-8.033E+01	.	*	.	.
3.901E+03	-8.041E+01	.	*	.	.
5.012E+03	-8.052E+01	.	*	.	.
6.310E+03	-8.065E+01	.	*	.	.
7.945E+03	-8.082E+01	.	*	.	.
1.000E+04	-8.104E+01	.	*	.	.
1.250E+04	-8.131E+01	.	*	.	.
1.585E+04	-8.165E+01	.	*	.	.
1.995E+04	-8.207E+01	.	*	.	.
2.512E+04	-8.261E+01	.	*	.	.
3.162E+04	-8.330E+01	.	*	.	.
3.901E+04	-8.411E+01	.	*	.	.
5.012E+04	-8.520E+01	.	*	.	.
6.310E+04	-8.671E+01	.	*	.	.
7.945E+04	-8.850E+01	.	*	.	.
1.000E+05	-9.011E+01	.	*	.	.
1.250E+05	-9.146E+01	.	*	.	.
1.585E+05	-9.190E+01	.	*	.	.
1.995E+05	-9.190E+01	.	*	.	.
2.512E+05	-9.144E+01	.	*	.	.
3.162E+05	-9.133E+01	.	*	.	.
3.901E+05	-9.197E+01	.	*	.	.
5.012E+05	-9.064E+01	.	*	.	.
6.310E+05	-7.679E+01	.	*	.	.
7.945E+05	-6.189E+01	.	*	.	.
1.000E+06	-5.301E+01	.	*	.	.
1.250E+06	-4.360E+01	.	*	.	.
1.585E+06	-3.459E+01	.	*	.	.
1.995E+06	-2.527E+01	.	*	.	.
2.512E+06	-1.605E+01	.	*	.	.
3.162E+06	-6.964E+00	.	*	.	.
3.901E+06	-2.942E+00	.	*	.	.
5.012E+06	-1.108E+01	.	*	.	.
6.310E+06	-2.026E+01	.	*	.	.
7.945E+06	-2.958E+01	.	*	.	.
1.000E+07	-3.897E+01	.	*	.	.

JOB CONCLUDED

TOTAL JOB TIME

15.32

TITLE UNITY GAIN

## \*\*\*\*\* CIRCUIT DESCRIPTION

```

* UNITY GAIN AMPLIFIER WITH CROSS GAMP
* TRANSISTORS ARE BROWN GATE SOURCE SUBSTRATE

* .SUBCKT GAMP 1 2 3 4 9
*   * DIFFERENTIAL AMP
R1 6 3 7 7 NDEV L=10U H=15U
R2 5 20 7 7 NDEV L=10U H=15U
R3 6 6 1 1 PDEV L=10U H=20U
R4 5 6 1 1 PDEV L=10U H=20U
R5 7 8 2 2 NDEV L=10U H=30U
* .Coop 5 0 200PF
* .OUTPUT STAGE
M6 1 5 9 1 PDEV L=10U H=15U
M7 9 6 2 2 NDEV L=10U H=30U
*
* .VOLTAGE DIVS
M8 10 10 1 1 PDEV L=10U H=12U
M9 11 11 10 10 PDEV L=10U H=12U
D10 8 8 11 11 PDEV L=10U H=12U
M11 8 8 2 2 NDEV L=10U H=30U
*
*
*
MOS 20 4 DC 0.0079704
*
.ENDS
*
* POWER SUPPLIES
*
VDD 1 0 DC 6
VSS 2 0 DC -6
*
* INPUT SIGNALS
*
VINN 3 0 DC 0 AC 1
VINP 4 0 DC 0 AC 1
*
* Main circuit
* Add the Vin- Vin+ Gout
X1 1 2 3 0 9 GAMP
*
R1 9 3 1NEG
R2 3 5 1NEG
*
*
.OPTIONS LINPTP=6000 ITLI=5000 PINTOL=1E-13
.DC VINN -2E-3 0.0005
.PLOT DC V(9) (-0,0)
.AC DEC 10 10 100mA
.PLOT AC UN(9)
.PLOT AC UP(0)
.probe
*
*
.WIDTH OUT=80
*
* MODELS
*
.MODEL NDEV NMOS LEVEL=2 LB=0.4U TD=500E-10 NSUB=1E+16 UTO=1.0
+GMFP=1.3590 PHI=0.0 UD=600 UEXP=0.0 UCRT=1.0E6 UTRP=0.0
+DELTA=1.2465 UMAX=1E+5 NL=0.87U LNRDRA=0.02 MFS=2E+11 NEFF=1.001E-2
+NS=0.8 TPS=1.0 RSH=22 CGSD=350E-12 CGDO=200E-12 CGBO=350E-12 CJ=300E-6
+RL=0.5 CJSW=500E-12 RJSW=0.3
*
*
.MODEL PDEV PMOS LEVEL=2 LB=0.5U TD=500E-10 NSUD=10.0E+13 UTO=-1.0
+GMSP=0.870003 PHI=0.6 UD=450 UEXP=0.0 UCRT=1.0E6 UTRP=0.0
+DELTA=1.93631 UMAX=1E+5 NL=1.0U LNRDRA=0.02 MFS=1.5E+11 NEFF=1.002E-2
+NS=0.8 TPS=1.0 RSH=95 CGSD=350E-12 CGDO=200E-12 CGBO=200E-12 CJ=150E-6
+RL=0.3 CJSW=400E-12 RJSW=0.23
*
*
.END

```

TITLE UNITY BRIN

\*\*\*\*\* MOSFET MODEL PARAMETERS

	MDEV	PDEV
	MROS	PROS
LEVEL	2	2
TPO	-1	
LB	400.00000E-09	500.00000E-09
VBG	1	-1
KP	55.25000E-06	31.07029E-06
DMNA	1.2500	.070003
PHI	.0	.0
LAMBDA	.02	.02
RSH	22	95
CJ	300.00000E-06	150.00000E-06
CJSU	300.00000E-12	400.00000E-12
BLSH	.3	.25
CSS0	350.00000E-12	350.00000E-12
CSD0	350.00000E-12	350.00000E-12
CDO0	200.00000E-12	200.00000E-12
RSB0	10.00000E+15	10.00000E+15
RSS	0	0
RFS	200.00000E+09	150.00000E+09
TRH	50.00000E-09	50.00000E-09
WJ	870.00000E-09	1.00000E-06
WS	000	450
MCAT	1.00000E+06	1.00000E+06
MMR	100.00000E+03	100.00000E+03
MEFF	.01001	.01002
DELTA	1.2403	1.93631

\*\*\*\*\* 11/07/90 \*\*\*\*\* Psplot 4.04 - July, 1990 \*\*\*\*\* 20104147 \*\*\*\*\*

TITLE UNITY GRIN

\*\*\*\*\* DC TRANSFER CURVES

TEMPERATURE = 27.000 DEG C

I(V)	V(0)	-0.000E+00	-3.000E+00	0.000E+00	3.000E+00	6.000E+00
-8.000E-03	7.903E-03	.	.	.	.	.
-7.500E-03	7.194E-03	.	♦	.	.	.
-7.000E-03	6.955E-03	.	.	♦	.	.
-6.500E-03	6.146E-03	.	.	♦	.	.
-6.000E-03	5.957E-03	.	.	♦	.	.
-5.500E-03	5.140E-03	.	.	♦	.	.
-5.000E-03	4.959E-03	.	.	♦	.	.
-4.500E-03	4.490E-03	.	.	♦	.	.
-4.000E-03	3.991E-03	.	.	♦	.	.
-3.500E-03	3.493E-03	.	.	♦	.	.
-3.000E-03	2.994E-03	.	.	♦	.	.
-2.500E-03	2.495E-03	.	.	♦	.	.
-2.000E-03	1.996E-03	.	.	♦	.	.
-1.500E-03	1.497E-03	.	.	♦	.	.
-1.000E-03	9.977E-04	.	.	♦	.	.
-5.000E-04	4.987E-04	.	.	♦	.	.
0.000E+00	-2.179E-07	.	.	♦	.	.
5.000E-04	-4.991E-04	.	.	♦	.	.
1.000E-03	-9.981E-04	.	.	♦	.	.
1.500E-03	-1.497E-03	.	.	♦	.	.
2.000E-03	-1.996E-03	.	.	♦	.	.
2.500E-03	-2.495E-03	.	.	♦	.	.
3.000E-03	-2.994E-03	.	.	♦	.	.
3.500E-03	-3.493E-03	.	.	♦	.	.
4.000E-03	-3.992E-03	.	.	♦	.	.
4.500E-03	-4.491E-03	.	.	♦	.	.
5.000E-03	-4.980E-03	.	.	♦	.	.
5.500E-03	-5.169E-03	.	.	♦	.	.
6.000E-03	-5.908E-03	.	.	♦	.	.
6.500E-03	-6.497E-03	.	.	♦	.	.
7.000E-03	-6.906E-03	.	.	♦	.	.
7.500E-03	-7.405E-03	.	.	♦	.	.
8.000E-03	-7.904E-03	.	.	♦	.	.

\*\*\*\*\* 11/07/90 \*\*\*\*\* PSpice 4.04 - July, 1990 \*\*\*\*\* 20:04:47 \*\*\*\*\*

TITLE UNITY BIAS

\*\*\*\*\* SWELL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

---

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
( 1)	0.0000	( 2)	-0.0000	( 3)	0.0000	( 5)	-7.61E-09
( 9)	-175.2E-09	( X1.5)	3.5003	( X1.6)	4.3145	( X1.7)	-1.5940
( X1.8)	-4.3925	( X1.10)	2.5358	( X1.11)	-0.9203	( X1.20)	.0000

VOLTAGE SOURCE CURRENTS  
NAME CURRENT

U00	-7.010E-05
U09	7.016E-05
U10H	-0.701E-14
X1.005	0.000E+00

TOTAL POWER DISSIPATION 0.42E-01 WATTS

## TITLE UNITY GRIN

\*\*\*\*\* DC ANALYSIS

TEMPERATURE = 27.000 DEG C

## LEGEND:

o: UN(0)

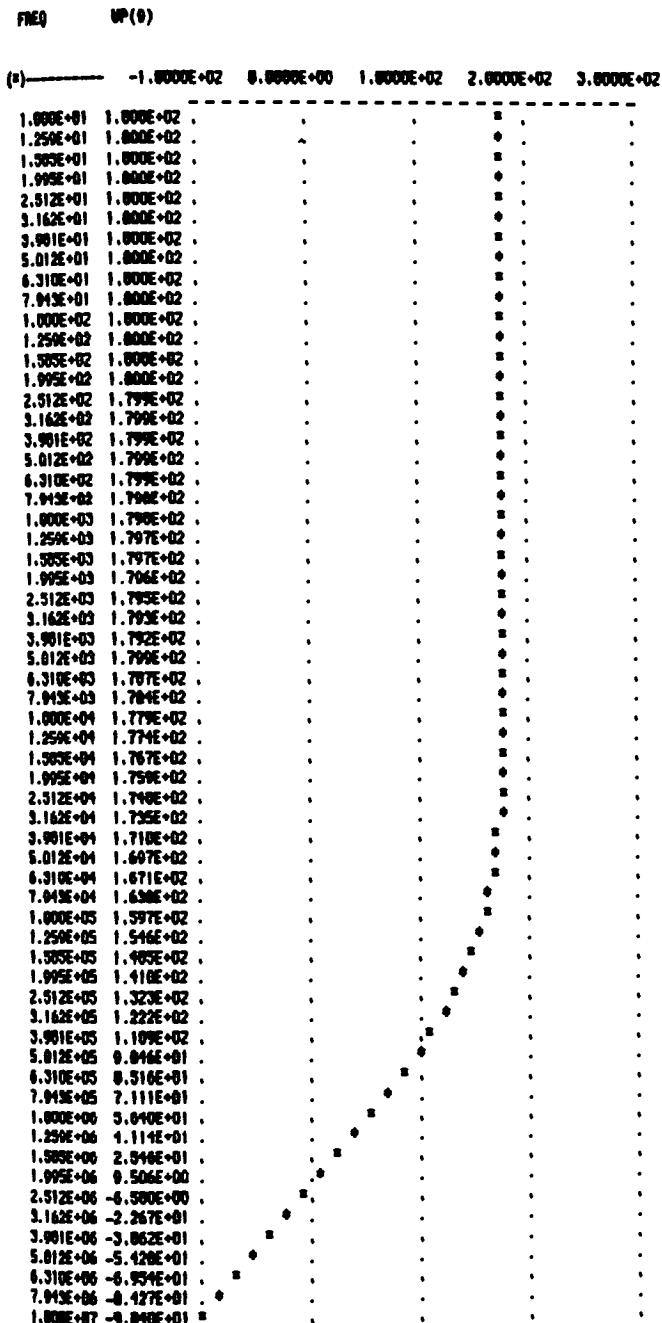
FREQ UN(0)

(a)-----	1.000E-02	1.000E-01	1.000E+00	1.000E+01	1.000E+02
1.000E+01	9.979E-01	.	.	.	.
1.250E+01	9.970E-01	.	♦	.	.
1.500E+01	9.979E-01	.	■	.	.
1.750E+01	9.970E-01	.	♦	.	.
2.000E+01	9.979E-01	.	■	.	.
2.312E+01	9.979E-01	.	♦	.	.
3.162E+01	9.970E-01	.	♦	.	.
3.991E+01	9.979E-01	.	■	.	.
5.012E+01	9.970E-01	.	♦	.	.
6.310E+01	9.979E-01	.	■	.	.
7.943E+01	9.970E-01	.	♦	.	.
1.000E+02	9.979E-01	.	■	.	.
1.250E+02	9.970E-01	.	♦	.	.
1.500E+02	9.979E-01	.	■	.	.
1.750E+02	9.970E-01	.	♦	.	.
2.312E+02	9.979E-01	.	■	.	.
3.162E+02	9.970E-01	.	♦	.	.
3.991E+02	9.979E-01	.	■	.	.
5.012E+02	9.970E-01	.	♦	.	.
6.310E+02	9.979E-01	.	■	.	.
7.943E+02	9.970E-01	.	♦	.	.
1.000E+03	9.979E-01	.	■	.	.
1.250E+03	9.970E-01	.	♦	.	.
1.500E+03	9.979E-01	.	■	.	.
1.750E+03	9.970E-01	.	♦	.	.
2.312E+03	9.979E-01	.	■	.	.
3.162E+03	9.970E-01	.	♦	.	.
3.991E+03	9.979E-01	.	■	.	.
5.012E+03	9.970E-01	.	♦	.	.
6.310E+03	9.979E-01	.	■	.	.
7.943E+03	9.970E-01	.	♦	.	.
1.000E+04	9.979E-01	.	■	.	.
1.250E+04	9.970E-01	.	♦	.	.
1.500E+04	9.979E-01	.	■	.	.
1.750E+04	9.970E-01	.	♦	.	.
2.312E+04	9.979E-01	.	■	.	.
3.162E+04	9.970E-01	.	♦	.	.
3.991E+04	9.979E-01	.	■	.	.
5.012E+04	9.970E-01	.	♦	.	.
6.310E+04	9.979E-01	.	■	.	.
7.943E+04	9.970E-01	.	♦	.	.
1.000E+05	9.979E-01	.	■	.	.
2.312E+05	9.344E-01	.	■	.	.
3.162E+05	7.970E-01	.	♦	.	.
3.991E+05	7.263E-01	.	■	.	.
5.012E+05	6.526E-01	.	♦	.	.
6.310E+05	5.757E-01	.	■	.	.
7.943E+05	5.035E-01	.	♦	.	.
1.000E+06	4.390E-01	.	■	.	.
1.250E+06	3.861E-01	.	♦	.	.
1.500E+06	3.414E-01	.	■	.	.
1.750E+06	3.036E-01	.	♦	.	.
2.312E+06	2.699E-01	.	■	.	.
3.162E+06	2.375E-01	.	♦	.	.
3.991E+06	2.053E-01	.	■	.	.
5.012E+06	1.720E-01	.	♦	.	.
6.310E+06	1.413E-01	.	■	.	.
7.943E+06	1.116E-01	.	♦	.	.
1.000E+07	8.381E-02	.	■	.	.

TITLE UNITY GRIN

---- RC ANALYSIS

TEMPERATURE = 27.000 DEG C



JOB CONCLUDED

TOTAL JOB TIME 15.53

TITLE AMPLIFIER WITH GAIN OF 100

## \*\*\*\*\* CIRCUIT DESCRIPTION

```

***** CIRCUIT DESCRIPTION

; AMPLIFIER WITH GAIN OF 100
; TRANSISTORS ARE DRAIN GATE SOURCE SUBSTRATE
;
; .NETLIST GPWIP 1 2 3 4 9
;
; DIFFERENTIAL AMP
M1 6 3 7 7 NDEU L=10U W=15U
M2 5 2 0 7 7 NDEU L=10U W=15U
M3 6 6 1 1 1 NDEU L=10U W=20U
M4 5 6 1 1 1 NDEU L=10U W=20U
M5 7 8 2 2 NDEU L=10U W=30U
;
C1 6 8 200PF
;
; OUTPUT STAGE
M6 1 5 9 1 NDEU L=10U W=15U
M7 9 8 2 2 NDEU L=10U W=30U
;
; VOLTAGE BIAS
M8 10 10 1 1 NDEU L=40U W=12U
M9 11 11 10 10 NDEU L=10U W=12U
M10 8 8 11 11 NDEU L=40U W=12U
M11 8 8 2 2 NDEU L=10U W=30U
;
;
;
;
V1 20 1 DC 0.00797044
;
.ENDS
;
; POWER SUPPLIES
;
VDD 1 9 DC 6
VSS 2 0 DC -6
;
; INPUT SIGNALS
;
VINN 3 0 DC 0 AC 1
;
; Main circuit
; Rdd Vdd Vin- Vin+ Vout
X1 1 2 5 0 0 OPAMP
;
R1 9 5 1.07E6
R2 3 5 1E4
;
;
;OPTIONS LINPT9=6000 ITL1=5000 PIUTBL=1E-15
;RC VINN =1E-3 0E-3 0.0005
;PLOT DC V(8)
;RC DEC 10 10 10REG
;PLOT AC V(8)
;PLOT AC UP(9)
;probe
;
;
;INPUT OUT=0
;
; MODELS
;
.MODEL NDEU NMOS LEVEL=2 LD=0.4U TH=3.0E-10 NSUB=1E+10 UT0=1.0
;NMUN=1.2506 PHI=0.6 UD=800 UEXP=0.0 UCRT=1.0E6 UTRA=0.0
;DELTA=1.2403 WMR=1E+5 XJ=0.07U LMRDUR=0.02 MFS=2E+11 NEFF=1.001E-2
;MBS=0.0 TPD=-1.0 RSH=22 CSD0=350E-12 CSD0=350E-12 CSD0=350E-12 CJ=500E-6
;XJ=0.5 CJSH=300E-12 RJSH=0.3
;
;
.MODEL PDEU PMOS LEVEL=2 LD=0.5U TH=5.0E-10 NSUB=10.0E+15 UT0=-1.0
;NMUN=0.679003 PHI=0.6 UD=150 UEXP=0.0 UCRT=1.0E6 UTRA=0.0
;DELTA=1.03631 WMR=1E+5 XJ=1.0U LMRDUR=0.02 MFS=1.5E+11 NEFF=1.002E-2
;MFS=0.0 TPD=1.0 RSH=95 CSD0=350E-12 CSD0=350E-12 CSD0=350E-12 CJ=150E-6
;XJ=0.5 CJSH=400E-12 RJSH=0.25
;
;
.END

```

TITLE GRIN OF 100

## \*\*\*\* MOSFET MODEL PARAMETERS

```
*****  
****  
MDEV  
MDOS  
POEV  
PROS  
LEVEL 2  
TP0 -1  
LD 400.00000E-09 300.00000E-09  
VTD 1 -1 -  
KP 35.230300E-06 31.876290E-06  
GMIN 1.3594 .879003  
PHI .6 .6  
LAMBDA .02 .02  
RSH 22 95  
CJ 300.00000E-06 150.00000E-06  
CJSU 300.00000E-12 400.00000E-12  
CLSU .9 .25  
CS0 350.00000E-12 350.00000E-12  
CD0 350.00000E-12 350.00000E-12  
CR0 200.00000E-12 200.00000E-12  
RSUB 10.00000E+15 10.00000E+15  
MSS 0 0  
MFS 200.00000E+09 150.00000E+09  
TOK 30.00000E-09 30.00000E-09  
XJ 870.00000E-09 1.00000E-06  
DD 000 450  
MCNT 1.00000E+06 1.00000E+06  
WWR 100.00000E+03 100.00000E+03  
NEFF .81001 .81002  
DELTA 1.2405 1.93631
```

\*\*\*\*\* 11/07/90 \*\*\*\*\* PSpice 1.04 - July, 1990 \*\*\*\*\* 20:02:24 \*\*\*\*\*

TITLE GRIN OF 100

\*\*\*\*\* SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

\*\*\*\*\*

MODE	VOLTAGE	MODE	VOLTAGE	MODE	VOLTAGE	MODE	VOLTAGE
( 1)	0.0000	( 2)	-6.0000	( 3)	0.0000	( 5)	-124.2E-03
( 9)-13.42E-06	( X1.5)	3.9063	( X1.6)	4.3145	( X1.7)	-1.5940	
( X1.8)	-4.3925	( X1.10)	2.3350	( X1.11)	-.9283	( X1.20)	.0000

VOLTAGE SOURCE CURRENTS

NAME CURRENT

VDD	-7.010E-05
VSS	7.010E-05
VTHM	-1.212E-11
X1.003	0.000E+00

TOTAL POWER DISSIPATION 0.42E-04 WATTS

TITLE GRIN OF 100

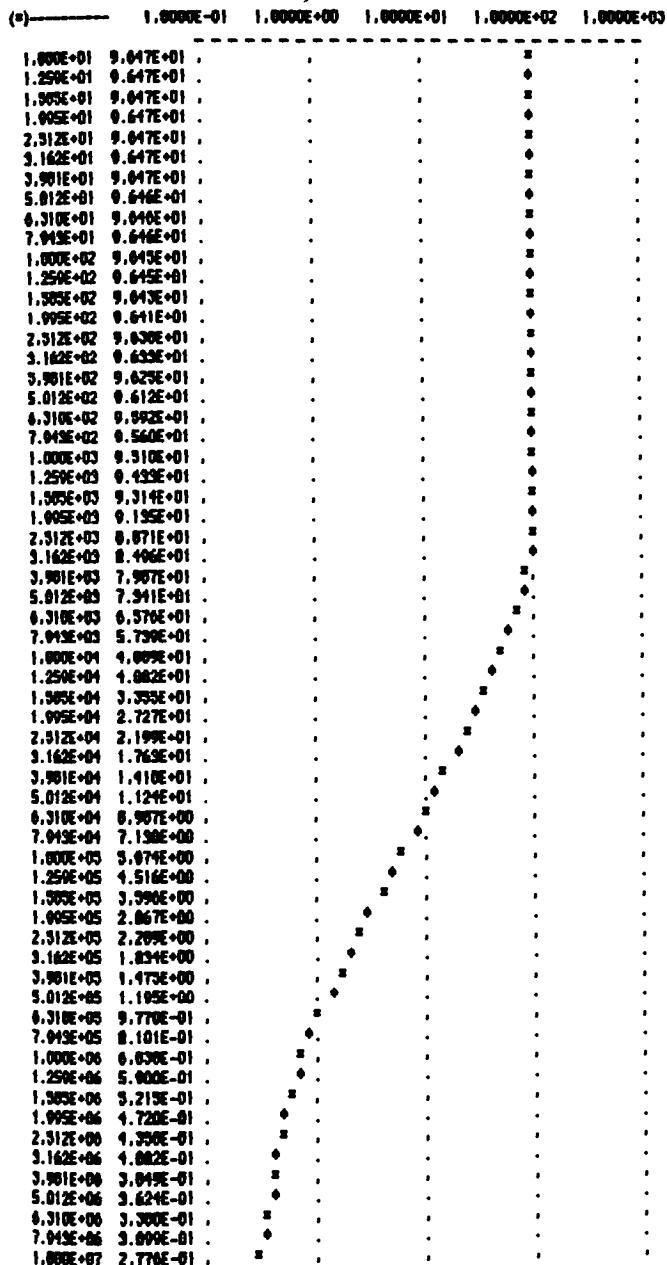
\*\*\*\*\* AC ANALYSIS

TEMPERATURE = 27.000 DEG C

## LEGEND:

♦: UN(0)

FREQ UN(0)



TITLE GRIN OF 100

---- AC ANALYSIS

TEMPERATURE = 27.000 DEG C

FREQ UP(0)

(Hz)	-1.000E+02	0.000E+00	1.000E+02	2.000E+02	3.000E+02
1.000E+01	1.799E+02	.	.	.	.
1.250E+01	1.799E+02	.	.	.	.
1.500E+01	1.799E+02	.	.	.	.
1.750E+01	1.799E+02	.	.	.	.
2.500E+01	1.799E+02	.	.	.	.
3.162E+01	1.797E+02	.	.	.	.
3.991E+01	1.795E+02	.	.	.	.
5.012E+01	1.795E+02	.	.	.	.
6.310E+01	1.794E+02	.	.	.	.
7.943E+01	1.792E+02	.	.	.	.
1.000E+02	1.790E+02	.	.	.	.
1.250E+02	1.788E+02	.	.	.	.
1.500E+02	1.786E+02	.	.	.	.
2.000E+02	1.784E+02	.	.	.	.
2.500E+02	1.782E+02	.	.	.	.
3.162E+02	1.780E+02	.	.	.	.
3.991E+02	1.778E+02	.	.	.	.
5.012E+02	1.776E+02	.	.	.	.
6.310E+02	1.774E+02	.	.	.	.
7.943E+02	1.772E+02	.	.	.	.
1.000E+03	1.770E+02	.	.	.	.
1.250E+03	1.679E+02	.	.	.	.
1.500E+03	1.644E+02	.	.	.	.
1.750E+03	1.612E+02	.	.	.	.
2.500E+03	1.587E+02	.	.	.	.
3.162E+03	1.561E+02	.	.	.	.
3.991E+03	1.537E+02	.	.	.	.
5.012E+03	1.502E+02	.	.	.	.
6.310E+03	1.477E+02	.	.	.	.
7.943E+03	1.261E+02	.	.	.	.
1.000E+04	1.200E+02	.	.	.	.
1.250E+04	1.145E+02	.	.	.	.
1.500E+04	1.094E+02	.	.	.	.
1.750E+04	1.055E+02	.	.	.	.
2.500E+04	1.020E+02	.	.	.	.
3.162E+04	9.900E+01	.	.	.	.
3.991E+04	9.659E+01	.	.	.	.
5.012E+04	9.441E+01	.	.	.	.
6.310E+04	9.246E+01	.	.	.	.
7.943E+04	9.063E+01	.	.	.	.
1.000E+05	8.893E+01	.	.	.	.
1.250E+05	8.646E+01	.	.	.	.
1.500E+05	8.415E+01	.	.	.	.
1.750E+05	8.200E+01	.	.	.	.
2.500E+05	8.002E+01	.	.	.	.
3.162E+05	7.820E+01	.	.	.	.
3.991E+05	7.313E+01	.	.	.	.
5.012E+05	6.862E+01	.	.	.	.
6.310E+05	6.325E+01	.	.	.	.
7.943E+05	5.895E+01	.	.	.	.
1.000E+06	4.973E+01	.	.	.	.
1.250E+06	4.170E+01	.	.	.	.
1.500E+06	3.307E+01	.	.	.	.
1.750E+06	2.407E+01	.	.	.	.
2.500E+06	1.491E+01	.	.	.	.
3.162E+06	5.607E+00	.	.	.	.
3.991E+06	-3.609E+00	.	.	.	.
5.012E+06	-1.306E+01	.	.	.	.
6.310E+06	-2.273E+01	.	.	.	.
7.943E+06	-3.264E+01	.	.	.	.
1.000E+07	-4.269E+01	.	.	.	.

JOB CONCLUDED

TOTAL JOB TIME

15.87

TITLE SINUSOID

## \*\*\*\*\* CIRCUIT DESCRIPTION

```

* OPEN LOOP DIFFERENTIAL GAIN AND FREQUENCY RESPONSE
* FOR A SINUSOIDAL INPUT WAVEFORM
*
* TRANSISTORS ARE BRATT BATE SOURCE SUBSTRATE
*
* .WAVE1 UPWIP 1 2 3 4 9
*
* DIFFERENTIAL AMP
M1 6 20 7 7 NDEV L=10U H=15U
I2 5 4 7 7 NDEV L=10U H=15U
M3 6 6 1 1 PDEV L=10U H=20U
M4 5 8 1 1 PDEV L=10U H=20U
M5 7 8 2 2 NDEV L=10U H=30U
*
* OUTPUT STAGE
M6 1 5 9 1 PDEV L=10U H=15U
M7 9 8 2 2 NDEV L=10U H=30U
*
* VOLTAGE BIAS
M8 10 10 1 1 PDEV L=40U H=12U
M9 11 11 10 10 PDEV L=40U H=12U
M10 8 8 11 11 PDEV L=40U H=12U
M11 8 8 2 2 NDEV L=10U H=30U
*
* CCOMP 3 8 200PF
*
VBS 3 20 DC 0.00797044
*
.EOB
*
* POWER SUPPLIES
*
VSS 1 8 DC 6
VSS 2 0 DC -6
*
* INPUT SIGNALS
*
VIN1 3 0 DC 0 AC 0
VIMP 4 0 SIN(0 0.001) 1K
*
* .WAVE1 UPWIP
*
.OPTIONS LINPTE=0000 ITL1=5000 PIVTEL=1E-15
*DC VINP -6E-3 6E-3 0.0005
*PLOT DC V(9) (-0,0)
*TRAN SDE=6 4E-3
*PLOT TRAN V(9) V(4)
*PROBE
*
* .WIOIN OUT=00
*
* MODELS
*
.MODEL NDEV NMOS LEVEL=2 LD=0.4U TH=500E-10 NSUB=1E+16 UT0=1.0
*NMNA=1.250E PHI=0.6 UD=800 DEHP=0.8 UCRI=1.0E6 UTRH=0.0
*DELTA=1.2405 NMRA=1E+5 XJ=0.07U LNDDA=0.02 MFS=2E+11 NEFF=1.001E-2
*MFS=0.0 TFS=-1.0 RSH=22 CSD0=350E-12 CSD0=350E-12 CJ=300E-6
*XJ=0.5 CJSN=300E-12 RJRN=0.3
*
.MODEL PDEV PMOS LEVEL=2 LD=0.5U TH=500E-10 NSUB=10.0E+15 UT0=-1.0
*NMNA=0.879803 PHI=0.6 UD=150 DEHP=0.8 UCRI=1.0E6 UTRH=0.0
*DELTA=1.03031 NMRA=1E+5 XJ=1.0U LNDDA=0.02 MFS=1.5E+11 NEFF=1.002E-2
*MFS=0.0 TFS=1.0 RSH=95 CSD0=350E-12 CSD0=350E-12 CJ=150E-6
*XJ=0.5 CJSN=100E-12 RJRN=0.25
*
.END

```

\*\*\*\*\* 11/07/90 \*\*\*\*\* Poploc 4.01 - July, 1990 \*\*\*\*\* 20:19:54 \*\*\*\*\*

TITLE SINUSOID

\*\*\*\*\* MOSFET MODEL PARAMETERS

	RDEV RDS	PDEV PDS
LEVEL	2	2
TP0	-1	
L0	400.00000E-09	500.00000E-09
UT0	1	-1
KF	33.23000E-06	31.07029E-06
AMPA	1.2504	.070003
PHI	.6	.6
LAMBDA	.02	.02
NRH	22	95
CJ	500.00000E-06	150.00000E-06
CJSU	500.00000E-12	400.00000E-12
ALSU	.3	.25
CSS0	350.00000E-12	350.00000E-12
CSB0	350.00000E-12	350.00000E-12
CS00	200.00000E-12	200.00000E-12
ISUB	10.00000E+15	10.00000E+15
NFS	0	0
NF2	200.00000E+09	150.00000E+09
T0K	50.00000E-09	50.00000E-09
XJ	870.00000E-09	1.00000E-06
UD	500	450
MCIT	1.00000E+06	1.00000E+06
VMX	100.00000E+03	100.00000E+03
NEFF	.01001	.01002
DELTA	1.2403	1.53031

\*\*\*\*\* 11/07/90 \*\*\*\*\* Poploc 4.01 - July, 1990 \*\*\*\*\* 20119154 \*\*\*\*\*

TITLE SINUSOID

\*\*\*\*\* INITIAL TRANSIENT SOLUTION TEMPERATURE = 27.000 DEG C

\*\*\*\*\*

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
( 1)	0.0000	( 2)	-0.0000	( 3)	0.0000	( 4)	0.0000
( 9)-32.59E-06 (X1.5)	3.9063 (X1.6)	4.3146 (X1.7)	-1.6010				
(X1.8)	-1.3923 (X1.10)	2.5350 (X1.11)	-.9283 (X1.20)				

VOLTAGE SOURCE CURRENTS  
NODE CURRENT

VDD	-7.015E-05
VSS	7.015E-05
V1IN	0.000E+00
V1NP	0.000E+00
X1.005	0.000E+00

TOTAL POWER DISSIPATION 0.42E-04 WATTS

TITLE SINUSOID

\*\*\*\*\* TRANSIENT ANALYSIS \*\*\*\*\*

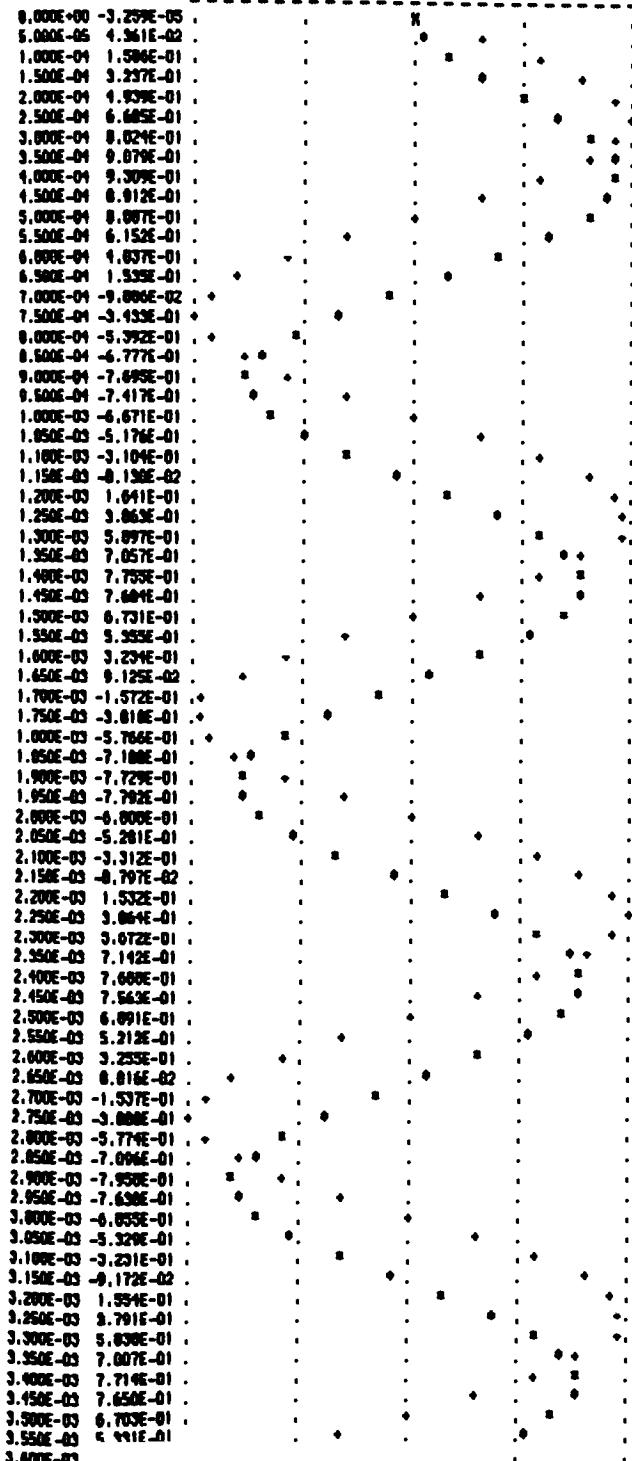
TEMPERATURE = 27.000 DEG C

## LEGEND:

0: U(0)

+1 U(1)

TIME	U(0)	U(1)	U(2)	U(3)	U(4)	U(5)
(0)-----	-1.0000E+00	-5.0000E-01	0.0000E+00	5.0000E-01	1.0000E+00	
(0)-----	-1.0000E-03	-5.0000E-04	0.0000E+00	5.0000E-04	1.0000E-03	



3.650E-03	8.950E-02	.	.	.	.	.
3.700E-03	-1.580E-01	.	.	*	.	.
3.750E-03	-3.820E-01	.	.	.	.	.
3.800E-03	-5.775E-01	.	.	.	.	.
3.850E-03	-7.194E-01	.	.	.	.	.
3.900E-03	-7.730E-01	.	.	.	.	.
3.950E-03	-7.821E-01	.	.	.	.	.
4.000E-03	-6.980E-01	.	.	.	.	.

JOB CONCLUDED

TOTAL JOB TIME 12.25

**Appendix V**  
**Fabricated NWELL CMOS Device Preliminary**  
**Results**

\*\*\*\*\* GRAPHICS PLOT \*\*\*\*\*

W# D4, R5, C15

VOUT  
( V )  
CURSOR (- .2360V , 2.3230V )  
MARKER (- .1890V , -5.5288V )

6.000

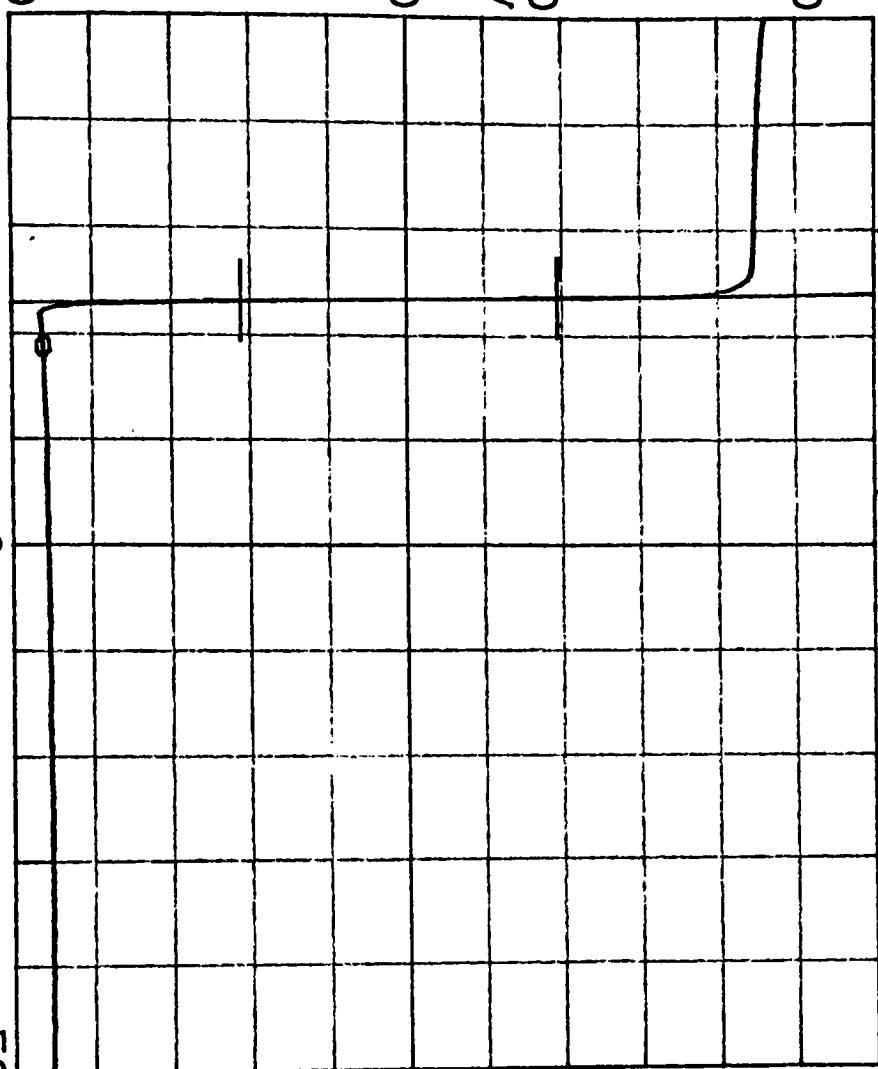
1.200  
/div

0

-6.000  
-500.0

VINV  
0  
100.0/div (mV)

500.0



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-1.22E+03	-822E-06	-234E-03	-285E+00
LINE2				

Variables:  
VINV -Ch4  
Linear sweep  
Start - .5000V  
Stop .5000V  
Step .0010V

Constants:  
VDD -Ch1 6.0000V  
VSS -Ch2 -6.0000V  
VNON -Ch3 .0000V

\*\*\*\*\* GRAPHICS PLOT \*\*\*\*\*  
W# D4, R7, LAST COL

卷之三

**GRAPHICS PLOT** -  
W# D4, R7, LAST col.

VOUT

Variable

( v) CURSOR (- .0650V - =1.6516V

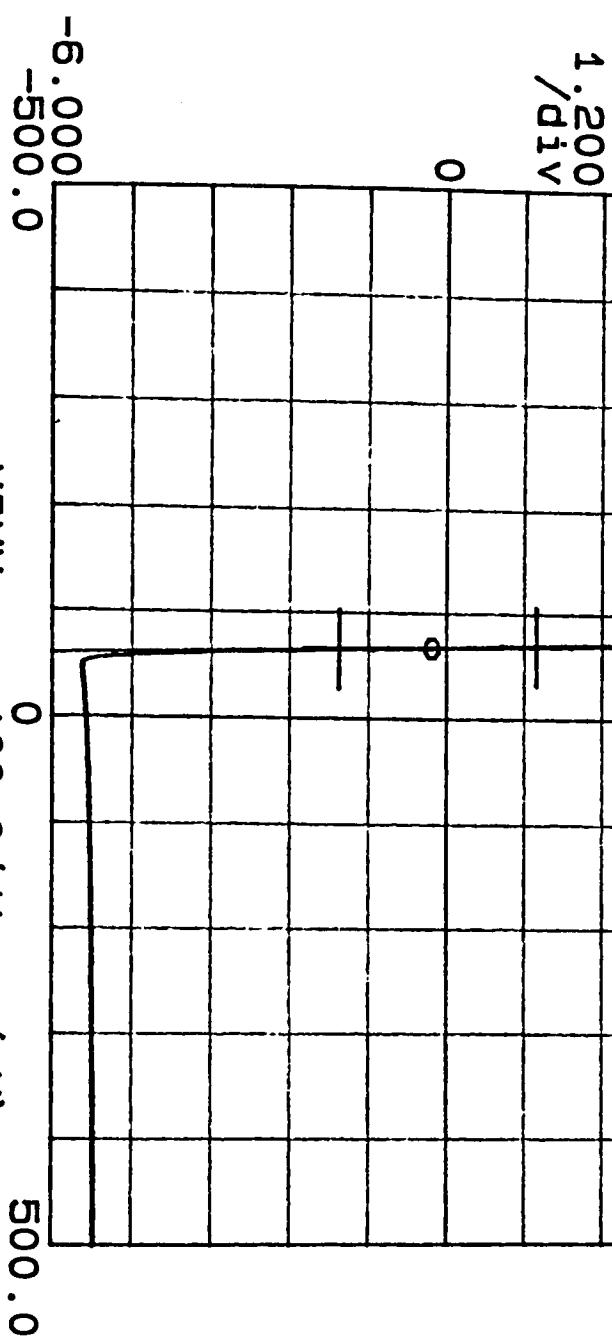
VINV -Ch4

```
( v) CURSOR (- .0650V -1.6516V
MARKER (- .0670V : = .2225V :
)
```

VINV -Ch4  
Linear sweep

6  
•  
000

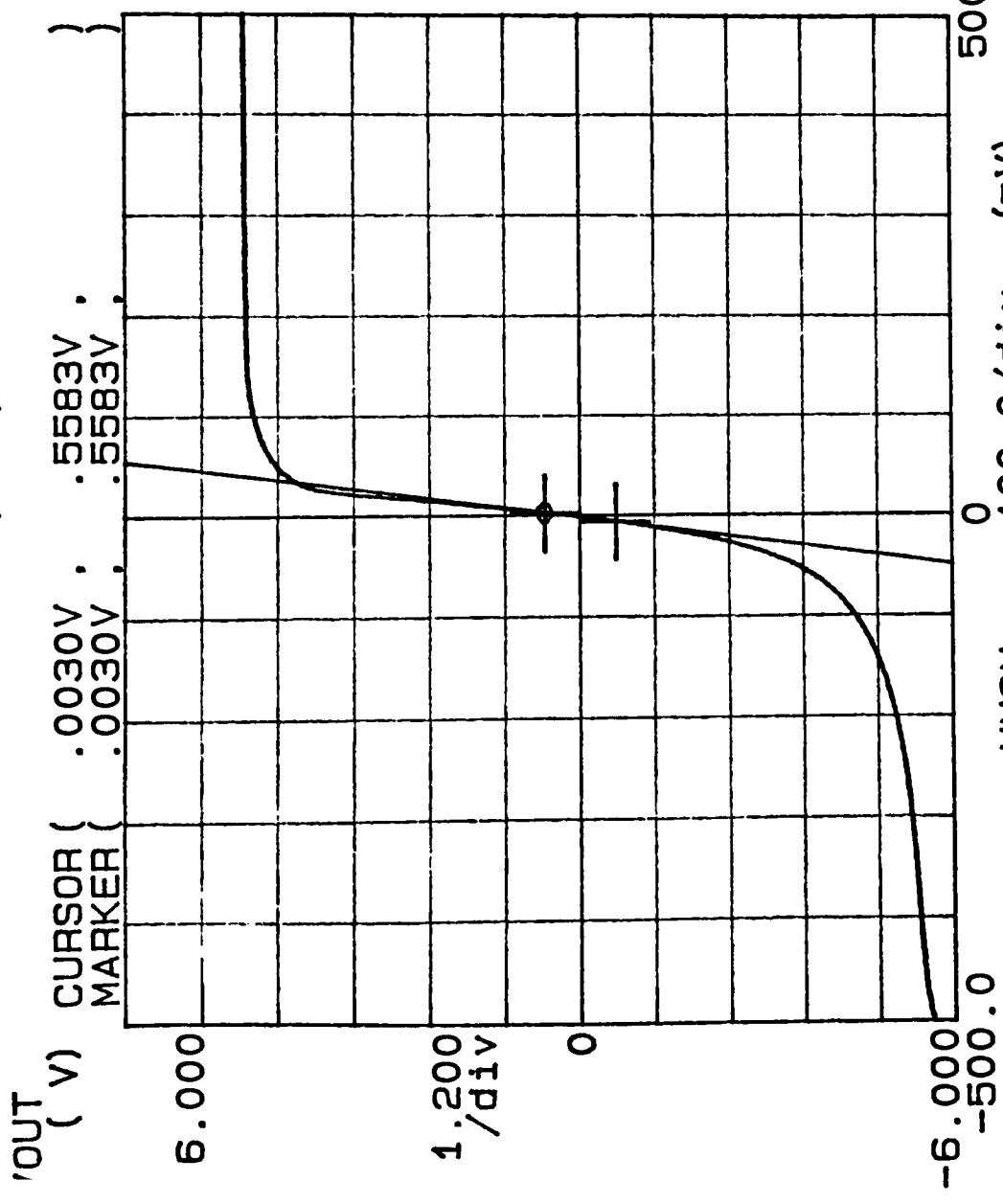
Stop  
Step  
.5000V  
.0010V



	GRAD	1/GRAD	XINTERCEPT	YINTERCEPT
LINE1	-759E+00	-1.32E-03	-67.2E-03	-51.0E+00
LINE2				

\*\*\*\*\* GRAPHICS PLOT \*\*\*\*\*

W# D4, R7, C5

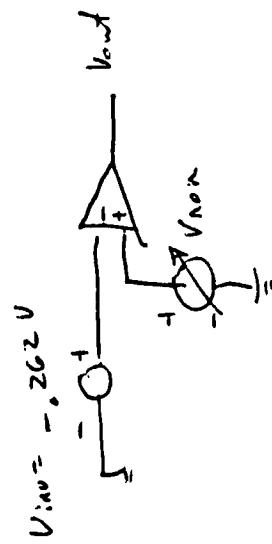


Variables:

$V_{NON}$	-Ch3
Linear sweep	
Start	-.5000V
Stop	.5000V
Step	.0010V

Constants:

VDD	-Ch1	8.0000V
VSS	-Ch2	-8.0000V
VINV	-Ch4	-.2620V



$$V_{INP} = -.262 \text{ V}$$

	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	127E+00	7.89E-03	-1.41E-03	178E-03
LINE2				

\*\*\*\*\* GRAPHICS PLOT \*\*\*\*\*

W# D4. R7. C5

VOUT  
( V )

CURSOR (- .2520V -1.0575V .  
MARKER (- .2520V .-1.0575V , )

6.000

1.200  
/div

0

-6.000  
-500.0

VINV

0

100.0/div (mV)

500.0

	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-122E+00	-8.17E-03	-261E-03	-31.9E+00
LINE2				

Variable1:  
VINN -Ch4  
Linear sweep  
Start - .5000V  
Stop .5000V  
Step .0010V

Constants:  
VDD -Ch1 6.0000V  
VSS -Ch2 -6.0000V  
VN0N -Ch3 .0000V



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