Development of Embedded Non-Volatile FRAMs for High Performance Smart Cards

Kang-Woon Lee, Byung-Gil Jeon, Byung-Jun Min, Seung-Gyu Oh, Han-Ju Lee, Woo-Taek Lim, Sung-Hee Cho, Hongsik Jeong, Chilhee Chung and Kinam Kim

Abstract—**Nonvolatile FRAMs with a design rule of 0.18 μm were developed for the high performance smart card. A 1Mb FRAM was embedded in place of an EEPROM and a 64Kb FRAM was embedded in place of a SRAM. It was confirmed that the FRAMs performed the roles of the EEPROM and SRAM successfully using the asynchronous write/read operation method and the one time programming (OTP) scheme. The cycle time of the FRAM was 10 MHz, which remarkably improved the write performance of the smart card in comparison with that of the conventional smart card with an EEPROM. Additionally, a simple and smart bit-line reference scheme for the future FRAM device having a 1T1C cell type was proposed.**

Index Terms—**FRAM, smart card, asynchronous operation, OTP, bit line reference scheme.**

I. INTRODUCTION

Recently, the demands for the potable electronic devices such as smart cards, cellular phones and PDAs have been increased due to their storage ability which is not limited by space and time. In particular, the smart card has a great potential for a huge market due to its widespread applications. The smart card consists of a CPU, a communication device and memories. The memories should have a small chip size, a high speed, low power consumption and non-volatility for the application to the smart card. However, the single memory to satisfy all the requirements could not be easily found. Therefore, several memories were used together in the conventional smart card. Typically, a mask ROM for storing the operating system, an EEPROM for storing the data and a SRAM for storing the temporary data are used. However, this system has inherent demerits of high cost, low performance, and complication in the controller system. Consequently, the unique memory is required for replacing those memories embedded in the conventional smart card.[1] In this work, the embedded non-volatile FRAMs for the high performance smart card system were developed using 1) the embedded FRAM core scheme, 2) the asynchronous operation method, 3) the one time programming (OTP) scheme and 4) the bit line reference scheme for the 1T1C FRAM. FRAMs replaced the EEPROM and the SRAM and supported all the functions of them successfully.

Manuscript received November 23, 2004; revised December 9, 2004.
ATD Team, Semiconductor R&D Center, Samsung Electronics Co., Ltd., San #16 Banwol-Ri, Taean-Eup, Hwasung-City, Gyeonggi-Do, 445-701, South Korea
E-mail : kw23.lee@samsung.com

II. DESIGN AND FEATURES OF THE FRAM

1. Core structure

Fig. 1 illustrates the core structure and the cell array of the FRAM device developed in this work. One cell is organized with two transistors and two capacitors (2T2C).

To reduce the plate line loading, the folded bit line structure was adopted.[2] The adjacent four bit lines are assigned to the main data lines and next adjacent four bit lines are assigned to the corresponding reference data

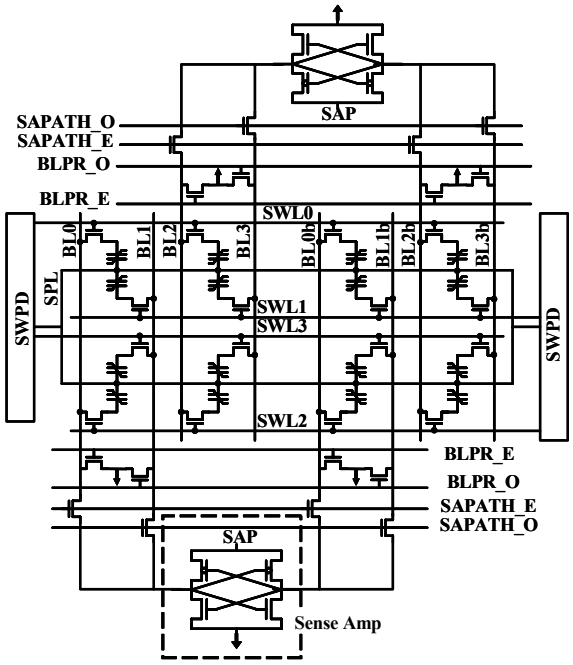


Fig. 1. The core structure and cell array of the FRAM.

lines. Consequently, the numbers of the operating memory cells in the folded bit line structure can be reduced as a half of that in the open bit line structure. Thus, the core area and the operating current can be reduced. The source node of the NMOS Tr in the sense amplifier is set at ground for the pre-sensing operation. If the voltage level of one bit line, which is developed by the charge sharing with the cell capacitors, reaches to the turn-on voltage of the NMOS Tr rapider than the other bit line level, the latter is discharged to ground by the NMOS Tr. Therefore, a large sensing margin can be obtained at the enabling point of the sense amplifier.

2. Asynchronous operation method

The FRAMs were designed to operate in the asynchronous method for replacing the EEPROM and SRAM. Asynchronous write/read waveforms of the FRAMs are plotted in Fig. 2. The device operation is activated by transiting the address transition detector (ATD) signal from high to low, and deactivated by transiting the next cycle ATD signal from low to high. In the write operation, the section plate (SPL) signal is disabled by transiting the external write enable (XWEB) signal from low to high for guaranteeing the data “0” set-up time (tDS). After the predetermined time for the writing “1”, the sense amplifier enable (SAP) signal and the sub-word-line (SWL) are disabled and then the pre-charge operation is performed. On the other hand, in the read operation, SPL is disabled after predetermined delay in which the charge-sharing and the sensing operation are performed. Subsequently, the next cycle ATD signal disables SAP and SWL, and enables pre-charge signals. This asynchronous read operation method enhances the read performance. If XWEB is enabled after SPL is disabled without changing of the address, second SPL is activated for the writing “0”. The asynchronous write/read technique designed in this work is applicable to the high performance smart card system.

3. One time programming scheme

The smart card system requires the specific cell region calleded as one time programming (OTP) to protect certain information. Only one time write operation is permitted in the OTP cell region. In this work, the OTP scheme was generated by reconfiguring the control scheme of the FRAM. Fig. 3-1 shows a simple block diagram of the OTP scheme. When the OTP cells are selected, the OTP controller controls a main sense amplifier (MSA, IO sense amplifier) and a write driver circuit. The OTP cell protection methodology is described in detail in Fig. 3-2. It has two steps. At the first step, the all OTP cells are written with data ”1” by enabling the test mode pin (TM_Pin) to disable the OTP controller. In this case, the writing operation in the OTP cells is performed in the same manner as that in the normal cells. In the second step, TM_Pin is disabled and the OTP controller can be enabled depending on the OTP_SEL signal. If the address selects the OTP region, the OTP controller is enabled by the OTP_SEL signal. In this case, even though XWEB is enabled, the OTP controller enables the MSA and compares the read out data to the previously written data (data “1”). If the read out data is “1”, the OTP controller enables the write driver for the write operation. However, if the read out data is “0”, the OTP controller does not enable the write driver because it means that the selected memory cell has been written with a data “0” previously. Therefore, the data which was already written in the OTP region can be protected.

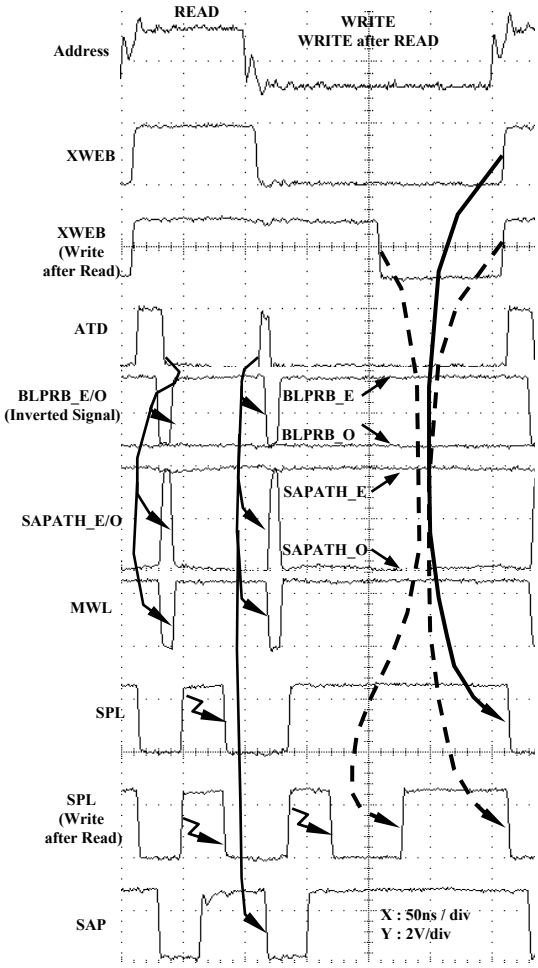


Fig. 2. Asynchronous write and read waveforms.

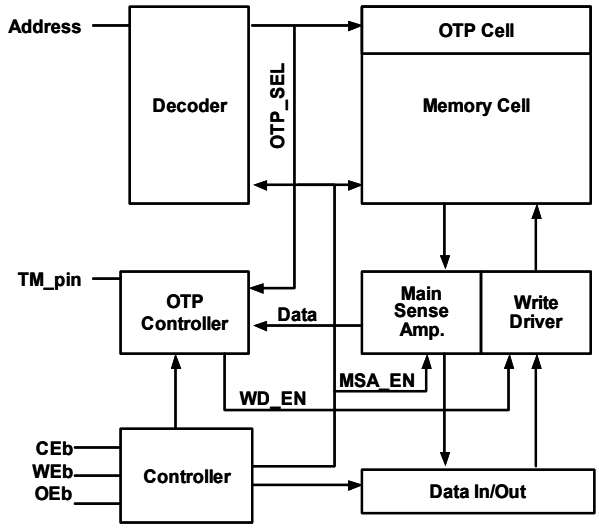


Fig. 3-1. A block diagram of the OTP scheme

4. Bit line reference scheme for the 1T1C FRAM

The additional vehicle FRAM with a 1T1C cell type was developed by modifying the 2T2C FRAM. A great deal

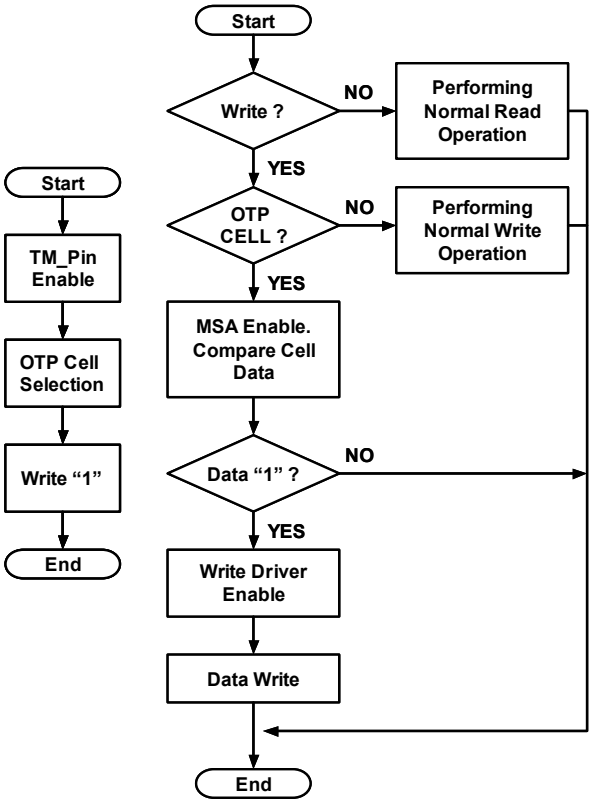


Fig. 3-2. A flow chart of the OTP scheme

of efforts have been devoted to develop more stable and effective bit line reference scheme because it determines the reliability of the 1T1C FRAM devices. However, the previous schemes have several demerits such as a large layout area, the limitation of placing the reference cell array, and the complexity of the control scheme. We propose new bit line reference scheme having the simple circuits and the stable reference voltage. Fig. 4-1 illustrates the bit-line reference scheme and the cell array for the 1T1C FRAM designed in this work. The bit-line reference level is generated by forcing the plate pulse to two reference ferroelectric capacitors storing data "0". The level of the plate pulse can be regulated to set the reference bit line level at the middle point between the bit line level of data "0" and that of data "1". The timing diagram is shown in Fig. 4-2. When the SWL0 is selected, the BLPR_E/BLPR_O signals are disabled, and the SAPATH_E/SAPATH_O signals are enabled. Simultaneously, the RSWL1 and RSWL3 signals are enabled to select two reference cells and then SPL and RSPL are enabled. Both SPL and RSPL signal are driven by the plate pulse driver (SPL_DRV) signal and, therefore, no additional circuits are required to

drive the reference plate line as shown in Fig. 4-3. After the charge sharing operation, the sense amplifier senses the difference between the main bit line level and the reference bit line level. During the restoring process to the main cells, the reference cells are written with data "0" by activating the BLPR_O and SAPATH_O signals. Therefore, no additional signals are needed for writing to the reference cells. Finally, all of the rest signals are disabled and the operation is finished. As described in Fig. 4-3, the height of the RSPL can be controlled by trimming the VG_Bias level to optimize the reference bit line level with the various ferroelectric properties of the reference cells. Furthermore, more stable bit line reference level can be obtained because the reference cell can be located in anywhere of the chip, resulting in minimizing the dependence of cell charge on the location of the ferroelectric capacitor.

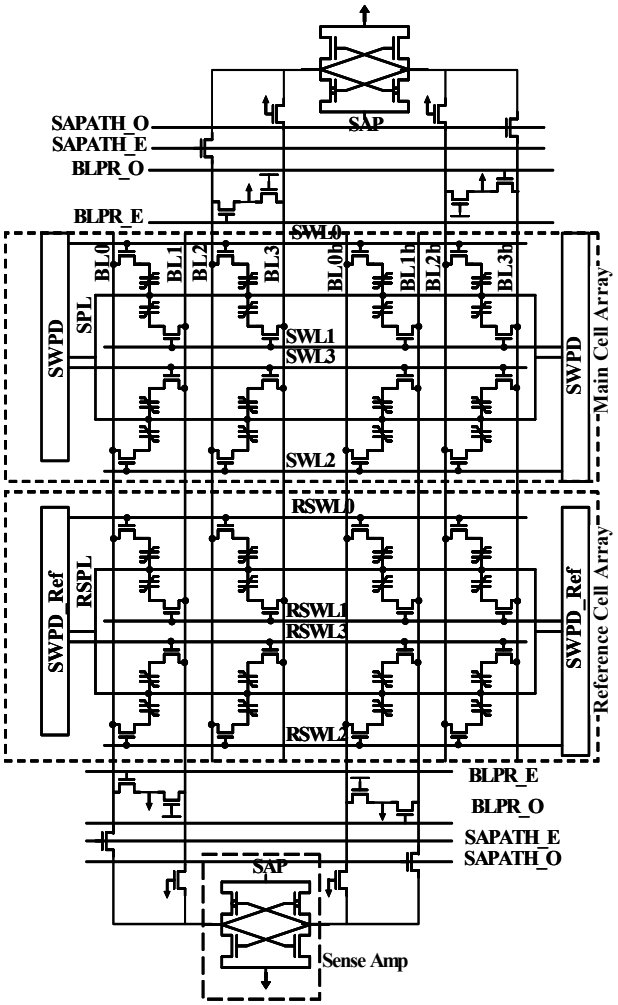


Fig. 4-1. The proposed bit line reference scheme for the 1T1C FRAM.

5. Device performance

The shmoo data of the embedded FRAM is plotted in Fig. 5. The write cycle time of the FRAM measured at an operating voltage of 1.6V and at room temperature was 100ns (10MHz), which was over 10000 times faster than that of the conventional EEPROM. Fig. 6 shows the bit line voltage population of 16Kb memory cells. The 1T1C 16Kb TEG with the fixed bit-line reference voltage generator scheme [3] was also fabricated to monitor the charge population of the ferroelectric cells. The sensing margin was 420mV at a core voltage of 2.5V. The key features and performance of the embedded FRAMs are summarized in Table 1 and the microphotograph of the smart card in which the FRAMs are embedded is shown in Fig. 7.

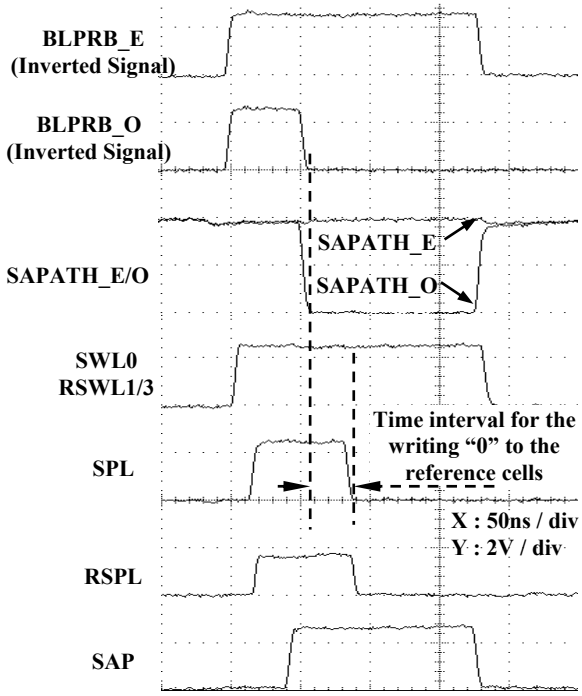


Fig. 4-2. Core timing waveforms of the 1T1C FRAM.

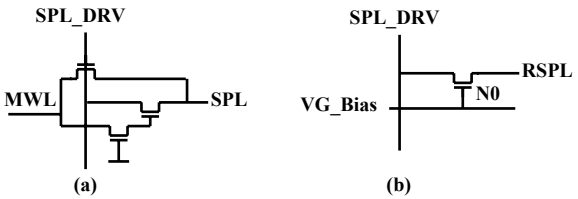


Fig. 4-3. Plate line drivers for (a) the main plate line and (b) the reference plate line

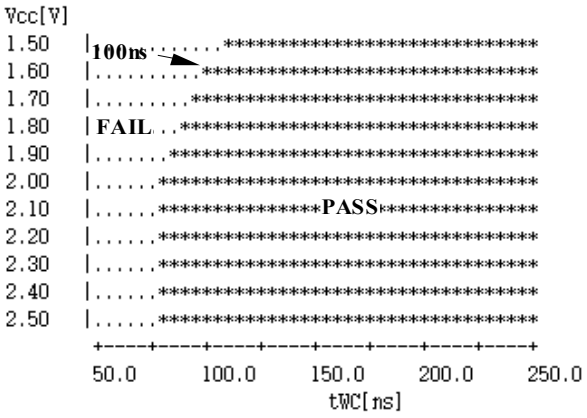


Fig. 5. The Shmoo data of the FRAM.

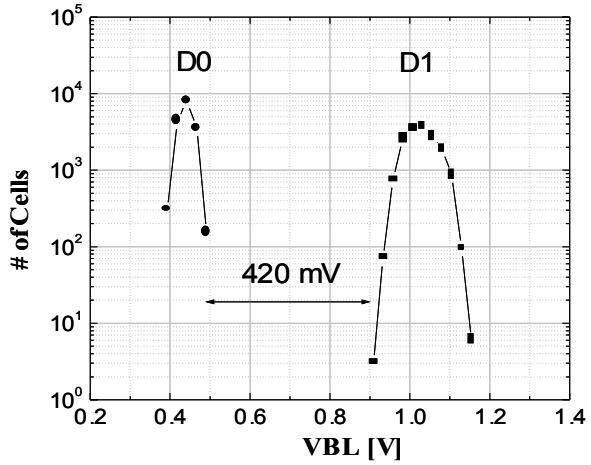


Fig. 6. Bit line population characteristics of the FRAM.

Table 1. The device features of the FRAM.

Data Memory Size (Replacing EEPROM)	128K Byte
Buffer Memory Size (Replacing SRAM)	8K Byte
Design Rule	0.18μm
Cell Type	2T2C
Cell Size	1.84μm x 1.30μm = 2.392μm^2
Data Memory Chip Size	3960μm x 2030μm = 8.04mm^2
Buffer Memory Chip Size	1140μm x 580μm = 0.66mm^2
Smart Card Chip Size	4350μm x 3540μm = 15.4mm^2
Supply Voltage	1.62V ~ 5.5V
Memory Frequency	Data memory : 10Mhz Buffer Memory : 13Mhz
Memory Current	1.0mA(@5Mhz)

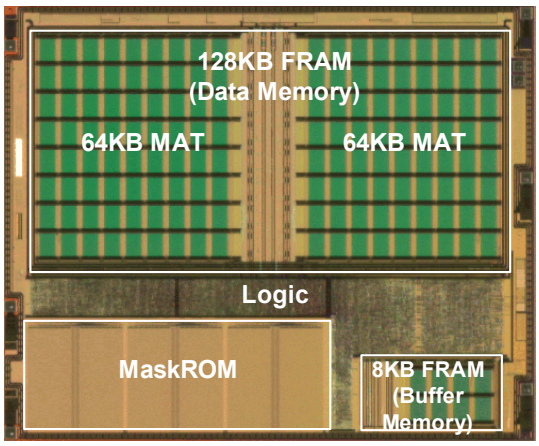


Fig. 7. A microphotograph of the smart card chip.

III. Conclusions

Embedded nonvolatile FRAMs for replacing EEPROM and SRAM in a smart card have been successfully developed using the asynchronous write/read method and the OTP scheme. The FRAMs show the write cycle of 10MHz, which can improve considerably the write performance of the smart card. The OTP controller produced by modifying the FRAM controller can protect the information in the OTP cells safely. The performance of the smart card in next generation will be absolutely improved using 1T1C FRAMs having our new bit line reference scheme.

References

[1] J. Yamada, et al., "A 128Kb FeRAM Macro for a Contact/Contactless Smart Card Microcontroller", ISSCC Digest of Technical Papers, pp. 270-271, 2000.

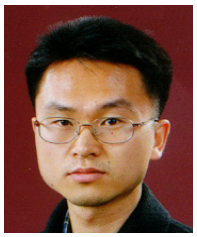
[2] M. K Choi et al., "A 0.25- m 3.0-V 1T1C 32-Mb Nonvolatile Ferroelectric RAM with Address Transition Detector and Current Forcing Latch Sense Amplifier Scheme", *J. Solid-State Circuits*, Vol. 37, pp. 1472-1478, November 2002.

[3] B. G Jeon, et al., "A 0.4 m 3.3 V 1T1C 4 Mb nonvolatile ferroelectric RAM with fixed bit-line reference voltage scheme and data protection circuit", ISSCC Digest of Technical Papers, pp. 272-273, 2000.

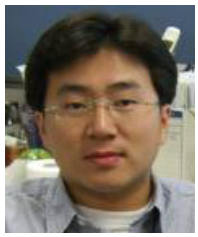
Kang-Woon Lee was born in Seoul, Korea in 1974. He received M.S. and Ph.D. degree in material science and engineering from KAIST (Korea Advanced Institute of Science and Technology) in 1999, 2003, respectively. In 2003, he joined Samsung Electronics Co., Ltd., as a FRAM device designer. His current major activity is focused on the design of low power and high performance embedded FRAMs.

Byung-Gil Jeon was born in Kyunsangbuk-Do, Korea, on October 27, 1966. He received the B.S. degree in electronic engineering from Konkuk National University, Korea, in 1992. He has been with the Memory Product & Technology Division at Samsung Electronics Co., Ltd., Kyunggi-Do, Korea, in December 1991. He has been involved in the design of 256-Kb and 1-Mb high speed BiCMOS SRAM's and developed Module Driver IC during 1992 - 1996. During 1995 - 2001, he had developed 64-Kb, 4-Mb, and 32-Mb FRAM. Since March 2002, he has been developing embedded FRAM. His current interests are the design and application of high-density and low-power FRAM's for embedded solution. He has received several patents related to ferroelectric memory technology.

Byung-Jun Min was born in Ulsan, Korea, on September 20, 1974. He received the B.S. degree and the M.S. degree in electrical engineering from Chungang University, Korea, in 1999 and 2001, respectively. He has been with the Memory Product & Technology Division at Samsung Electronics Co., Ltd., Kyunggi-Do, Korea, in 2001 where he works as assistant engineer for design and evaluation of high-density and low-power FRAM.



Seung-Gyu Oh was born in Cheju-Do, Korea, on October 23, 1970. He received the B.S. degree in electrical engineering from Chung-Ang University, Korea. He joined Samsung Electronics Co., Korea, where he was engaged in the CMOS logic IC design. Since 1996, he has been developing SRAM's and FRAM's. He is currently an assistant engineer for evaluation of FRAMs.



Han-Ju Lee was born in Seoul, Korea, on September 19, 1976. He received the B.S. amd M.S. degree in metallurgical engineering from Korea University, Korea, in 2001 and 2003, respectively. He has been with the Memory Product & Technology Division at Samsung Electronics Co., Ltd., Kyunggi-Do, Korea, in 2003 as an engineer for design and evaluation of high-density and low-power FRAM.

Woo-Taek Lim received the B.S and the M.S degrees in electronics engineering from the Yonsei University in 1991, 1993, respectively. In 1993, he joined Samsung Electronics, Co., Ltd, Korea, as a MCU(Micro Controler Unit) design engineer. From 1993 to 2000, he designed 8-bit MCU for Monitor applications. And since then has participated in the design of smartcard for an SIM (Subscriber Indetification Module) Card. His current research interests are Mobile LDI (LCD Driver IC) design for TFT-LCD.

Sung-Hee Cho was born in Kyung-ki, Korea, in 1964. He received the B.S degrees in electronics engineering from the Yonsei University in 1987, respectively. In 1987, he joined Samsung Electronics, Co., Ltd, Korea, as a memory circuit design engineer. From 1987 to 2000, he had participated in the design group of non-volatile memory for EEPROM, MASKROM and Flash memory. Since 2001, he has developed Smart Card IC which embeds memories such as EEPROM of Flash, ROM and SRAM.

Hongsik Jeong was born in Seoul, Korea, on May 27, 1962. He received the B.S., M.S. and Ph.D. degrees in department of physics from Yonsei University, Korea, in 1985, 1987 and 1992, respectively. In 1992, he studied the carrier dynamics of GaAs/AlGaAs quantum structure as a Post Doctor at Laser Spectroscopy Lab in KRISS, Taejon, Korea. In same year, he joined the Samsung Electronics Company, Ltd., Kyunggi-Do, Korea where he is involved in dry etching process for device fabrication such as 64Mb and 256Mb DRAM. Since 1997 he

has been engaged in the development of process integration. He participated in developing cutting edge technologies of 1Gb and 4Gb DRAM. Recently, he is in charge of developing new memories such as FRAM, MRAM and PRAM as a project leader.

Chilhee Chung was born in Seoul, Korea, on December 09, 1956. He received Ph.D. degree in Physics from Michigan State University in 1993. He received the B.S. degree in Physics in 1979 from Seoul National University. In 1981 he received M.S. degree in Physics from KAIST. In 1979, he joined Samsung Company and now is a project director of developing Smart Card IC which embeds memories such as EEPROM of Flash, ROM and SRAM.

Kinam Kim received Ph.D. degree in electrical engineering from University of California Los Angeles, CA. in 1994. He received the B.Sc. degree in electronic engineering in 1981 from Seoul National University, South Korea. In 1983 he received the master degree in electrical engineering from KAIST(Korea Advanced Institute of Science and Technology). In 1983 he joined Samsung Electronics Co., Ltd., where he has been involved in the development of DRAMs, ranging from 64Kb to 4Giga-bit densities. Currently he is a senior vice president responsible for the research and development of next generation memory technologies for DRAM, Non-volatile memory, SRAM, and emerging new memories such as FRAM, PRAM, and MRAM. He was a program director for 0.13 μm DRAM technology generation from its development at R&D center to transferring to manufacturing lines during period of 1999-2001. He was a technical director for 4Gb DRAM development for 1998~1999. He has been a project leader for the development of world first 1Gb DRAM using 0.18 μm CMOS technologies during 1994-1996. Dr. Kim received twice the grand prize of Samsung group for the successful developments of 1Mb DRAM and 1Gb DRAM in 1986 and 1996, respectively. His current major activity is focused on the development of technologies for low power and high performance multi-giga-bit density DRAMs and high density non-volatile memories. His research interests are memory device reliability, yield modeling on memory device, memory cell technology, and multi-level metallization for high performance of multi-giga bit memory devices. He published more than 280 technical papers on the field of memory technology. He holds 75 patents related to memory technology. He plays an active part in advancing future memory technology through participating panel discussions of prime conferences such as VLSI technology symposium, IEDM and ISSCC. He is a recipient of ISI's citation award for highly cited paper. Dr. Kim served as a committee member of international electron device meeting (IEDM), he is a member of editorial advisory board of Microelectronics reliability. He is an IEEE fellow and a Samsung fellow.