Integrated Deep Trench Capacitor in Si Interposer for CoWoS Heterogeneous Integration

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***Abstract*—**To accommodate the exceedingly demanding power integrity (PI) requirements for the advanced artificial intelligence (AI) and high performance computing (HPC) components, high-K (HK) based deep trench capacitors (DTC) have been integrated the first time in the silicon interposer with through silicon via (TSV) and fine-pitch interconnects for chip-on-wafer-on-substrate (CoWoS) integration. A specific capacitance density (C_s) of up to 340 nF/mm^2 is achieved over a large capacitor array, providing a total capacitance (C_t) of up to 68 μF per interposer die. The HK dielectric has intrinsic time-dependent dielectric breakdown (TDDB) lifetime of > 1,000 years at an operation voltage (V_{cc}) of 1.35V, and a normalized leakage current (I_{LK}) density < 1 fA/μm^2 under 1.35V at 105° C. No discernable process-induced damage or performance degradation (capacitance, I_{LK} & V_{bd} tailing) were observed. The high capacitance, low leakage, large area and reliability-proven Si-interposer integrated DTC, or iCap, provides superior PI performance and therefore greatly enhances the merit of using CoWoS for the next-generation heterogeneous wafer level system integration (WLSI).

I. Introduction

Technology scaling introduces exponentially rising average and transient current which demands more stable power delivery [1-2]. Decoupling capacitors are commonly used to reduce the impedance of a power distribution system in order to provide the required charges to the circuit more dynamically and to reduce the power supply noise. CoWoS with metal-insulator-metal (MIM) decoupling capacitors in the Si interposer has been demonstrated to have good PI handling capability [3-4]. However, as switching frequency and circuit power increase while operation voltage and noise margin decrease, a higher performance decoupling capacitors are required to mitigate voltage droop and noise ripple issues more effectively [5-9]. The performance of the capacitor is generally rated by its specific capacitance density (C_s) and total available capacitance per interposer (C_t). In this paper, HK DTC is integrated in the silicon interposer to form iCap to achieve an upgrade in both C_s and C_t by more than an order of magnitude compared with the planar MIM capacitors. The advantages of iCap create a significant benefit for minimized parasitics and enhanced power delivery and PI, making itself a very desirable feature in the very high power heterogeneous systems of HPC and AI in the CoWoS platform.

II. Fabrication

The iCap process is developed on 300 mm Si interposer wafers for CoWoS integration. The co-existence of DTC and TSV on a wafer, both require high aspect ratio silicon etch at dimensions nearly two orders of magnitude different from each other, calls for a decision for process sequence of the two distinct features. In the "DTC-first" approach, DTC forms on a nearly fresh silicon without having constraints from previous processes. However, the subsequent TSV processes must be well designed and controlled in order not to impact the prior-formed capacitor structures. In the "TSV-first" approach, on the other hand, the standard TSV process can be leveraged directly. However, care must be taken in the subsequent DTC process so that the potential TSV Cu protrusion issue may be prevented during DTC formation.

The schematic diagram of iCap in Fig. 1 depicts the cell array of iCap in the 100 μm thick Si interposer. The high-k dielectric layer is sandwiched between a top and a bottom electrode layers in the silicon trenches of aspect ratio >10 to form the DTC. The silicon interposer features such as TSV and metal layers are required to facilitate the high density routing demand among the active top dies attached to the interposer later on during CoWoS integration. Fig. 2 displays a cross-sectional SEM image of the iCap structure in the Si interposer.

The standard cell unit of iCap has an area of approximately 40 μm by 40 μm while multiple cells are allowed in one silicon interposer. A high specific capacitance density (C_s) of up to 340 nF/mm^2 is demonstrated for iCap based on a low cost and high yield process to achieve a total capacitance up to 68 nF per interposer die. The CoWoS, including CoW (chip-on-wafer) of various top dies of SoC (system-on-chip) and HBM (high bandwidth memory), and oS (on-substrate) assembly may be carried out to complete the heterogeneous integration on iCap interposer to achieve excellent PI in these high power, advanced HPC and AI systems.

III. Electrical Characterizations

A. HK Dielectrics

Fig. 3 shows iCap's normalized capacitance density versus voltage. The capacitance density is 300 nF/mm^2 at zero voltage for the HK-dielectric film. Note the capacitance density is defined over the equivalent plenary surface area over the iCap DTC structure. Fig. 4 displays two normalized I-V curves for this HK-dielectric film measured at 25°C and 105°C, respectively. It is clear that the measured leakage

current (I_{LK}) at +/-1.35V bias is still below 1 fA/μm^2 even at a higher testing temperature of 105°C.

B. Electrodes

The electrode structure of iCap is specially optimized in such a way to provide low contact resistivity to the via connecting to DTC to metal interconnect, supply charges through low sheet resistance to cover surfaces of DTC trenches, and prevent the accumulated semiconductor-process-induced static charges from damaging DTC HK dielectrics that may further impact the device performance and reliability. The resulting equivalent series resistance of a typical 1 μF iCap arrays is less than 2 mΩ. The DTC's accumulated process charge is typically negligible.

C. Si-Interposer Integration

Three key parameters of specific capacitance density, C_s, breakdown voltage, V_{bd}, and leakage current, I_{LK}, are measured on 12-inch CoWoS Si interposer wafers to ensure the uniformity and manufacturability of iCap technology. Fig. 5 demonstrates an average C_s of 300 nF/mm^2 with a tight distribution. Fig. 6 exhibits iCap's mean breakdown voltage (Vbd) of 6.13V. No premature Vbd failure occurs below 5.95V over an entire capacitor area of 200 mm^2.

Subsequently, Fig. 7 shows the cumulative distribution of measured leakage current (I_{LK}) at 25°C. The leakage current I_{LK} is 0.49pA in average for standard cell arrays with normalized leakage current density about 1 fA/μm^2. Overall the characteristics of iCap exhibits robust process and seamless integration with Si-interposer.

D. Reliability- TDDB

Fig. 8 displays the TDDB characterization for iCap HK dielectrics. The lifetimes (blue line) of the HK dielectric film are measured after accelerating conditions of 3.6V, 3.8V, 4.0V at 125°C. The lower red line represents the predicted TDDB lifetimes for 0.1% failure rate. From the result, the maximum operation voltage to sustain 10 years lifetime at 125°C is 2.1V for iCap with fixed area of 200 mm^2; moreover, at a little lower operation voltage of Vcc = 1.35V, the predicted lifetime can be drastically increased to > 1,000 years. The measurement result demonstrates iCap's excellent reliability characteristics.

IV. System Level Performance

To demonstrate system performance of the proposed iCap, a system level power delivery network is built as shown in Fig. 9 to demonstrate its capability on voltage droop reduction. An ARM core chip power model is applied, an equivalent S-parameter model of CoWoS associated with TSV is extracted by 3D EM tool of HFSS and built up in HSPICE, and a PCB equivalent circuit model is assumed. Fig. 10 shows the PDN impedance in frequency domain and voltage droop in time domain. Compared to CoWoS without iCap, CoWoS with iCap can have lower PDN impedance from 10 MHz to 2 GHz in frequency and about 100 mV voltage droop reduction. Table I compares the CoWoS technology with and without iCap and shows PDN impedance of CoWoS with iCap is only 0.05x of without iCap and voltage droop with iCap is only 0.45x of without iCap. This significantly voltage droop improvement supports AI or HPC cores on CoWoS with iCap operate at higher speed and lower system power consumption.

V. Conclusions

A low-cost, large-area, manufacturable HK DTC with high unit capacitance density (up to 340 nF/mm^2), low leakage current (I_{LK} < 1 fA/μm^2 at 105°C), and intrinsic TDDB lifetime of >1,000 years at 1.35V has been developed in silicon interposer. Electrical and reliability characterizations prove design and process flexibility while the fact that no detection of process-induced damage failure demonstrates a robust and manufacturable technology. In conclusion, iCap, the decoupling DTC technology integrated in CoWoS silicon interposer, has demonstrated an excellent PI solution for wafer-level heterogeneous integration for HPC/ AI applications.

Acknowledgment

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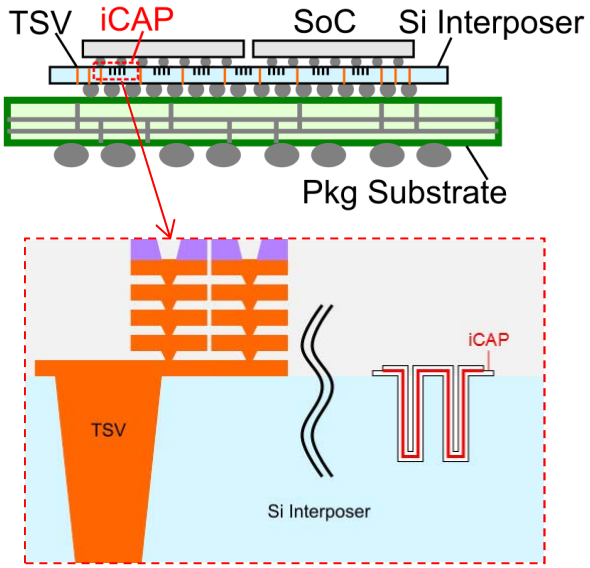

Fig. 1. The schematic diagram of iCap depicts the array of DTC in the 100 µm thick Si interposer. The silicon interposer contains TSV and metal routing layers to accommodate the high routing capacity demand.

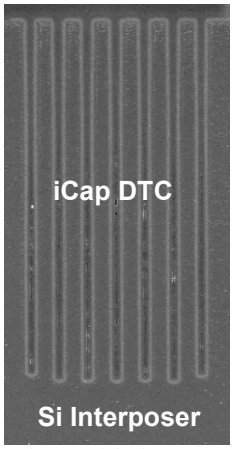

Fig. 2. Cross-sectional SEM image of the iCap structure in Si interposer.

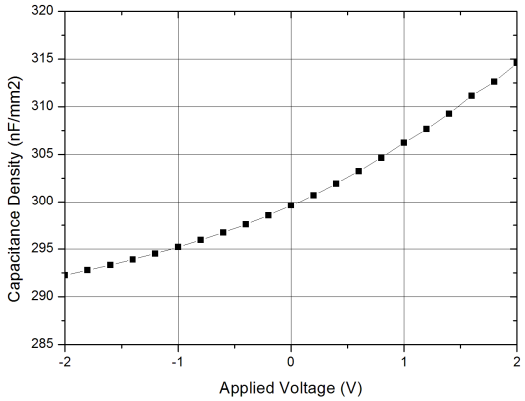

Fig. 3. iCap's capacitance area density versus applied bias voltage. The capacitance density is 300 nF/mm^2 at zero voltage.

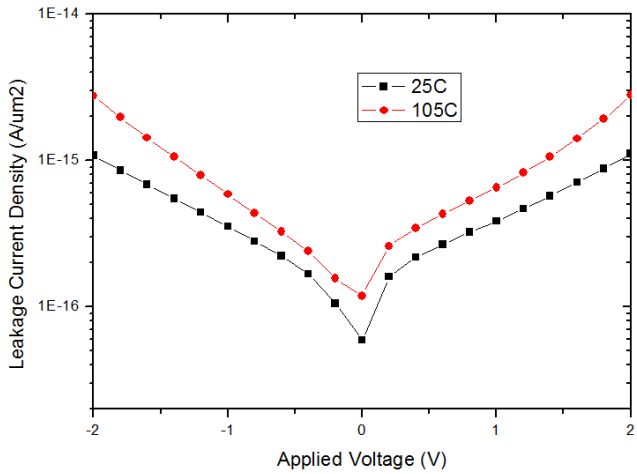

Fig. 4. Normalized I-V curves for this HK-dielectric film measured at 25 C and 105 C, respectively. The measured leakage current (I_{LK}) at +/-1 35V bias is still below 1 fA/µm^2 even at a higher testing temperature of 105 C

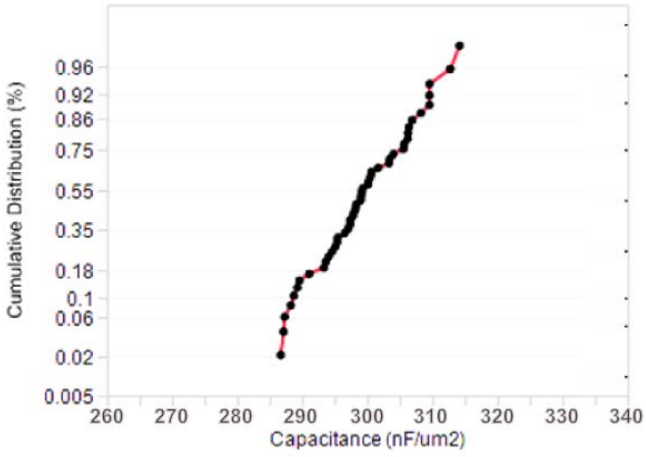

Fig. 5. Cumulative distribution for iCap's specific capacitance density for fully integrated DTC in CoWoS Si interposer. Average specific capacitance density C_s is 300 nF/mm^2 with narrow distribution.

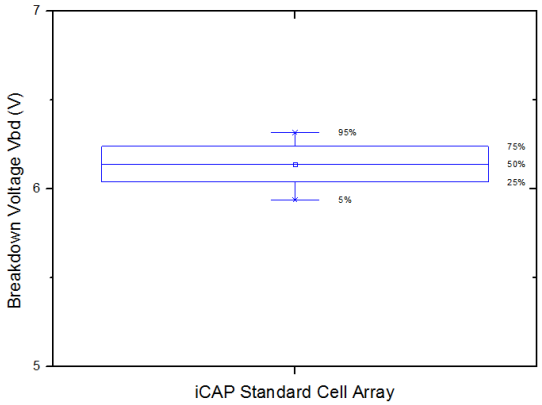

Fig. 6. Boxplot for iCap's breakdown voltage (Vbd) with mean value 6.13V. No premature Vbd failure occurs below 5.95V over an entire capacitor area of 200 mm^2.

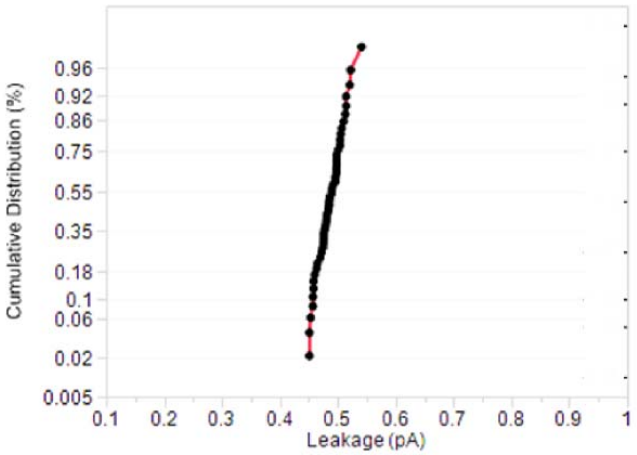

Fig. 7. Cumulative distribution for iCap's leakage current (I_{LK}) at 25 C with mean value of 0.49 pA. The normalized leakage current density is about 1 fA/μm^2.

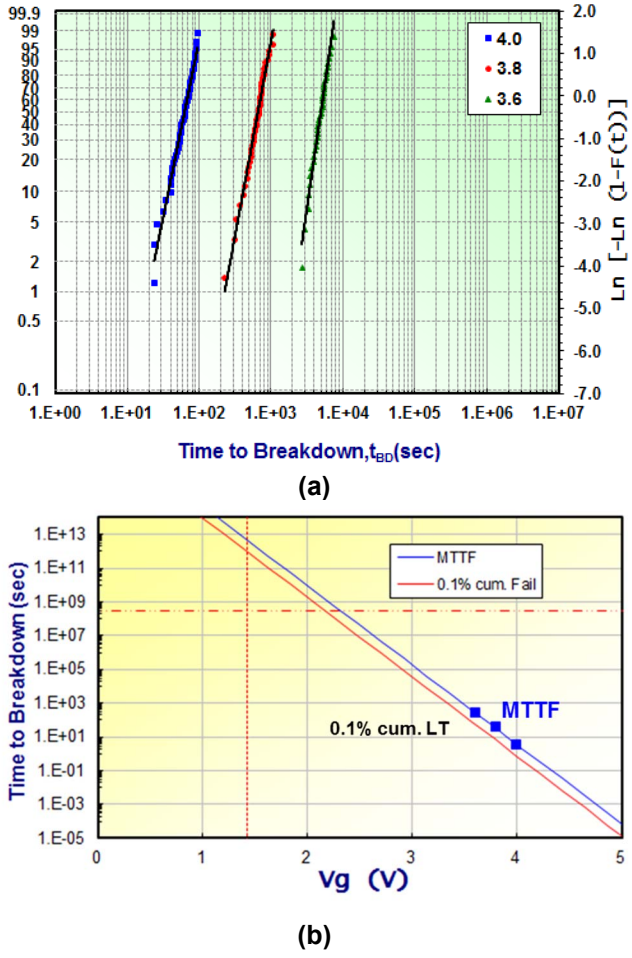

Fig. 8. TDDB analysis for iCap: (a) TDDB measurement for accelerating conditions of 3.6V, 3.8V, and 4.0V at 125 C. (b) The lifetimes (blue line) of the HK dielectric film are estimated from TDDB. The lower red line represents the predicted TDDB lifetimes for 0.1% failure rate. From the result, the maximum operation voltage to sustain 10 years lifetime at 125 C is 2.1V for iCap with a fixed area of 200 mm^2; moreover, at a little lower operation voltage of Vcc = 1.35V, the predicted lifetime can be drastically increased to > 1,000 years.

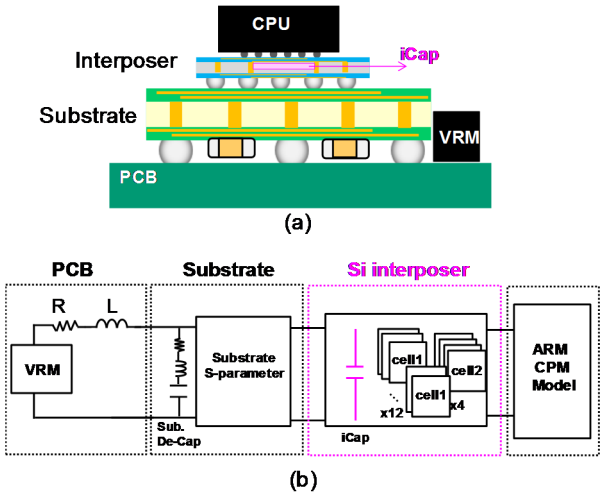

Fig. 9. A four-stage system level power delivery system.

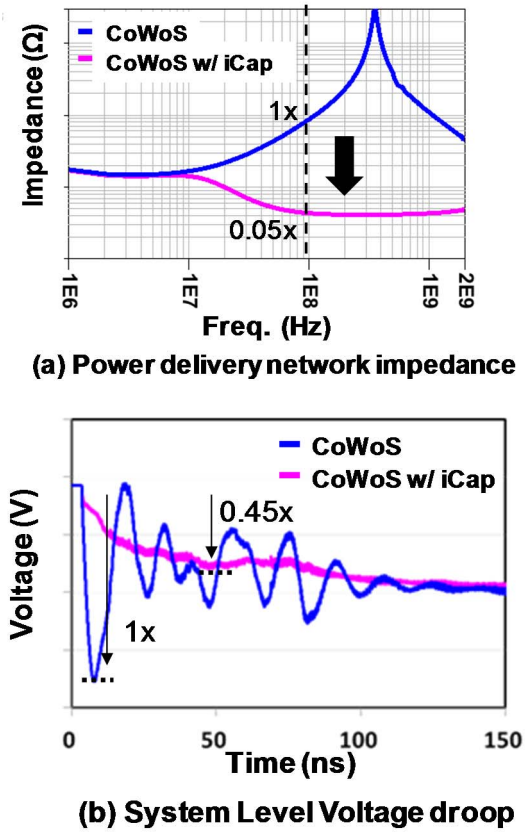

Fig. 10. (a) the PDN impedance in frequency domain and (b) voltage droop in time domain.

	CoWoS	CoWoS w/ iCap
PDN |Z| @100MHz	1x	0.05x
Voltage droop	1x	0.45x

Table I compares the CoWoS technology with and without iCap.