Single-chip universal digital satellite receiver with 480-MHz IF input

Article *in* IEEE Journal of Solid-State Circuits · December 1999

DOI: 10.1109/4.799874 · Source: IEEE Xplore

A Single-Chip Universal Digital Satellite Receiver with 480-MHz IF Input

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***Abstract*—This paper presents a complete single-chip universal digital satellite receiver supporting all current DBS system standards. The mixed-signal device accepts a modulated data stream at up to 90 Mbps and delivers a demodulated, error-corrected output data stream. The IC features an analog front end with 480-MHz intermediate-frequency downconversion and dual 8-bit analog-to-digital converters, an all-digital BPSK/QPSK/OQPSK variable-rate receiver supporting 1–45-MBaud operation with phase/frequency recovery, variable-rate digital filters, square-root Nyquist matched filters, acquisition and tracking loops, and a DVB/DSS/DigiCipher I/II-compliant concatenated Viterbi/Reed–Solomon forward error correction decoder with on-chip deinterleaver RAM. All required clocks are generated on chip from a single reference crystal. The chip contains 1.2 million transistors in a die area of 22 mm^2 and was implemented in a single-poly 0.35-μm CMOS process with four layers of metal.**

I. Introduction

A BLOCK diagram of a typical satellite TV system is shown in Fig. 1. The system contains an antenna that receives the K-band signal (11–12 GHz) transmitted by the satellite and a low noise block (LNB) that downconverts the signal for transmission over a coaxial cable to the set-top box. In Europe, the signal is downconverted by the LNB to 950–2150 MHz; in North America, the LNB downconverts the signal to 950–1450 MHz. An L-band tuner then selects the desired transponder channel. Fig. 2 shows a block diagram of a typical L-band satellite TV tuner. Most tuners in use today downconvert the signal to a 480-MHz intermediate-frequency (IF) and then use either a 36- or 55-MHz surface acoustic wave (SAW) filter to remove adjacent channels and out-of-band noise. An analog I/Q demodulator then produces a quadrature baseband (I/Q) output. Next, the digital data bitstream is recovered by a receiver, and error correction is performed to improve the bit error rate of the data. The data stream is then passed to a conditional access module that controls access to pay-per-view and premium channels. Last, an MPEG decoder recovers the digitized video data, and a video encoder produces an NTSC or phase alternation line (PAL) video output for a television.

Manuscript received May 12, 1999; revised June 15, 1999.

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Publisher Item Identifier S 0018-9200(99)08336-5.

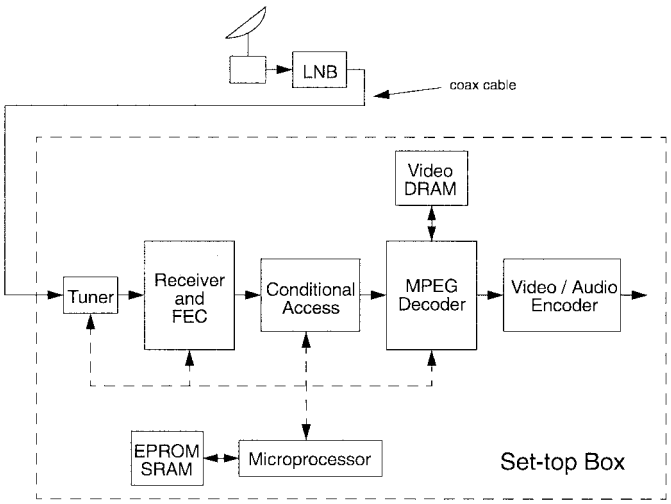


Fig. 1. Satellite TV system block diagram.

II. Chip Architecture

Fig. 3 shows a block diagram of the universal digital satellite receiver IC. The chip contains an analog front end, an all-digital receiver, and a concatenated Viterbi/Reed–Solomon (RS) forward error correction (FEC) decoder. The analog front end consists of a 480-MHz IF downconversion block, dual 8-bit analog-to-digital (A/D) converters that operate up to 128 MHz, and a low-jitter phase-locked loop (PLL) that generates all required clocks for the chip from a single external reference crystal.

The digital receiver supports variable symbol rates from 1 to 45 MBaud with BPSK, QPSK, or OQPSK modulation. The 8-bit A/D converter(s) operate with a free-running sample clock, and symbol timing is recovered digitally using multirate digital filters and a digital symbol timing recovery loop. The receiver also contains dual square-root Nyquist matched filters and digital carrier frequency recovery and phase-tracking loops with additional circuitry for automatic carrier acquisition that avoids all false lock points.

The error-correction block consists of a 64-state Viterbi decoder concatenated with a $t = 8$ RS decoder. The Viterbi decoder supports puncture modes for rate 5/11, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 6/7, and 7/8 operation with circuitry to automatically scan the data for the correct puncture mode. The decoder operates as a rate 1/2 based decoder for European

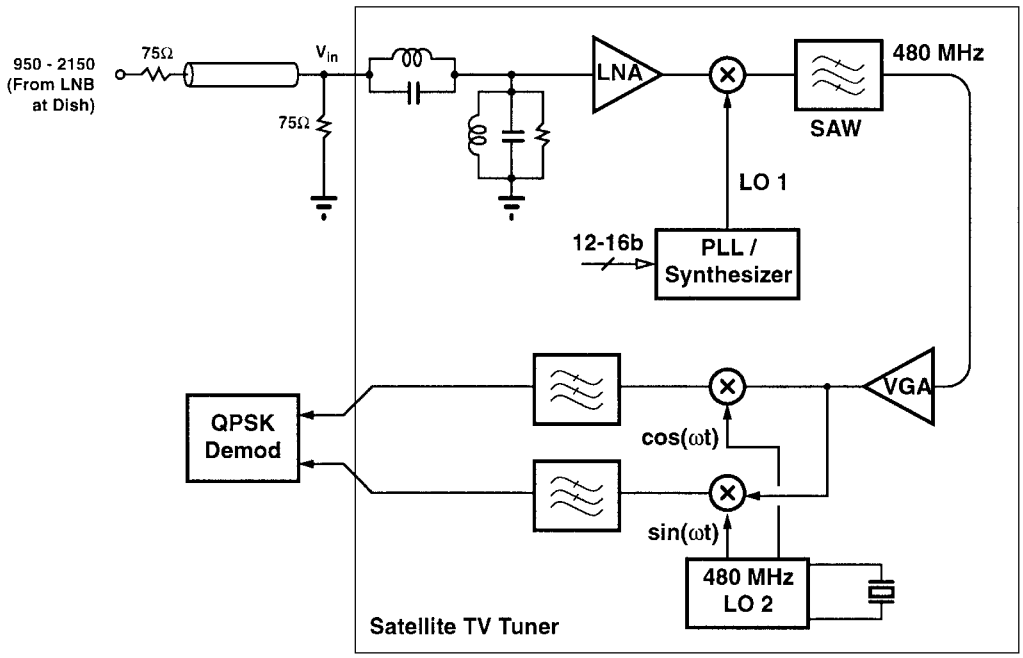


Fig. 2. Block diagram of a typical L-band satellite TV tuner.

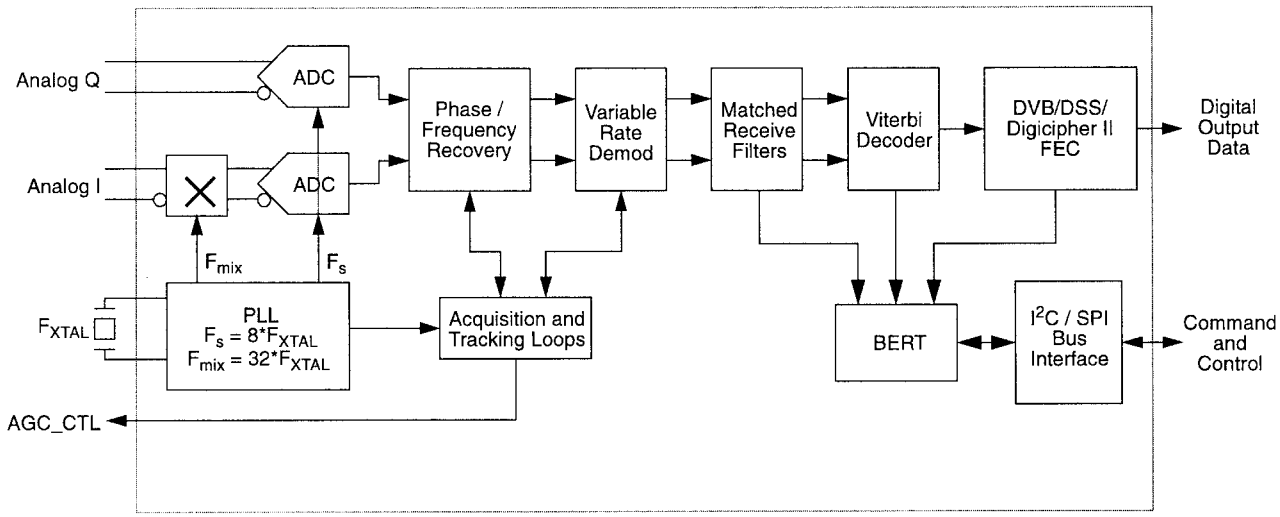


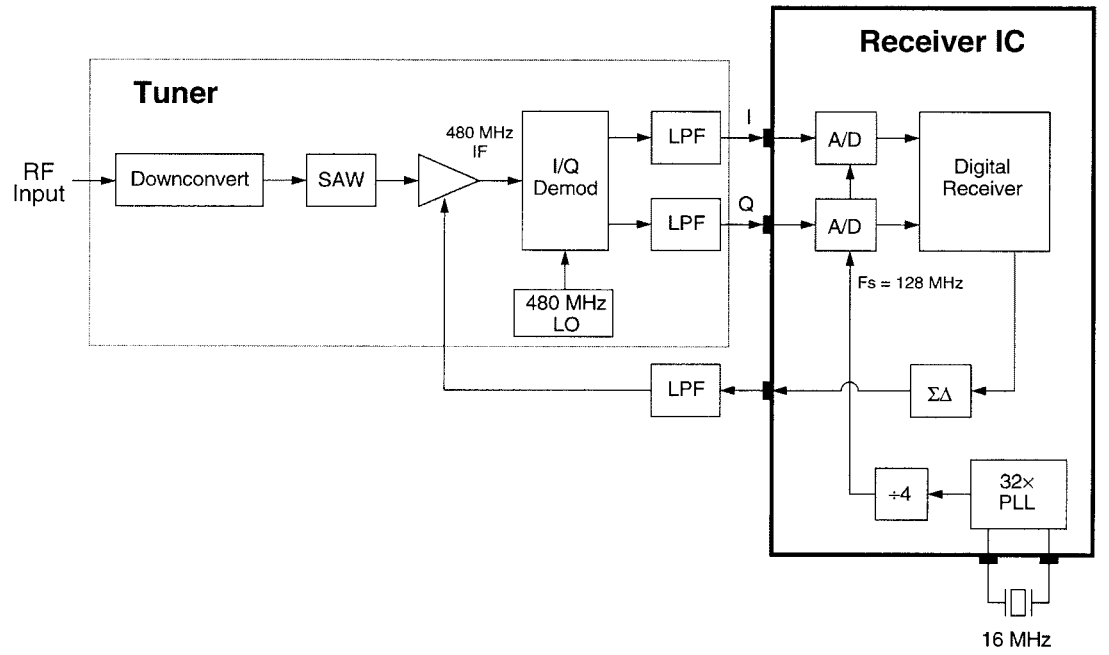
Fig. 3. Universal digital satellite receiver IC block diagram.

Digital Video Broadcast (DVB), or DirecTV Digital Satellite System (DSS), and as a rate 1/3 based decoder for Digicipher I/II operation. The RS decoder implements the DVB, DSS, and Digicipher I/II standards. It contains an on-chip deinterleaving RAM and can output either DSS or MPEG-2 formatted packets.

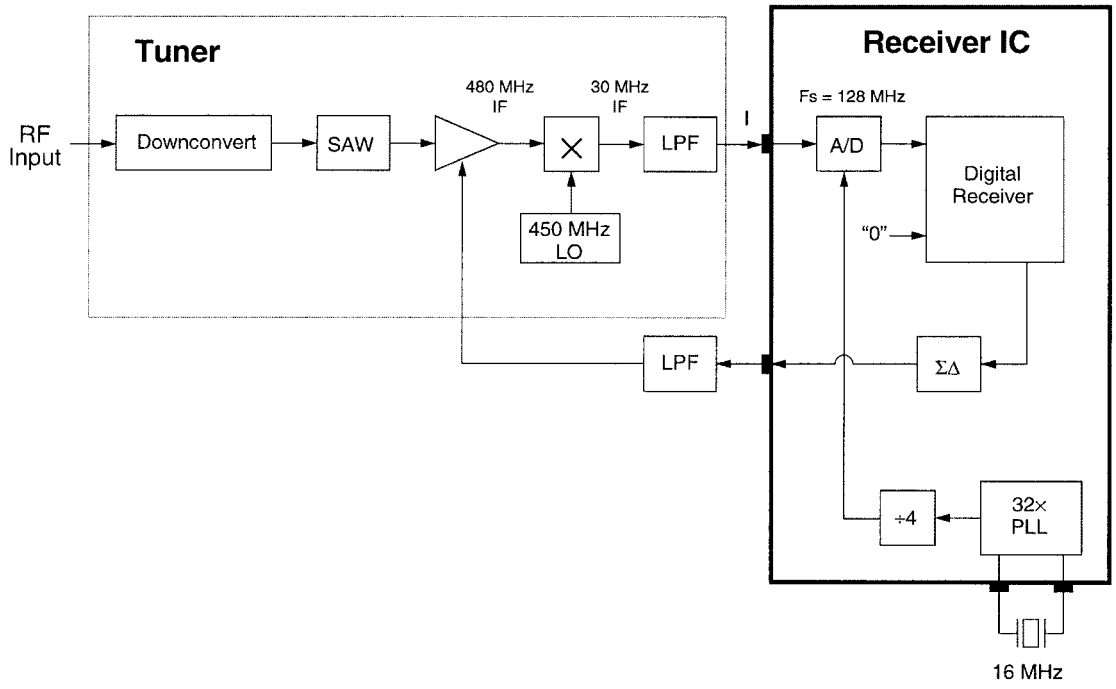
The chip architecture supports three tuner interface modes: baseband I/Q, low IF, and 480-MHz IF. For the baseband I/Q mode, the dual 8-bit A/D converters are used with a conventional tuner supplying quadrature baseband outputs, as shown in Fig. 4(a). Alternatively, the low-IF tuner interface mode allows the I/Q demodulator in the tuner to be replaced with a simple mixer that downconverts the signal to a low IF frequency within the bandwidth of the A/D converter, as shown in Fig. 4(b). A single A/D converter sampling at 128 MHz is used in this mode. For the lowest overall system cost, the I/Q demodulator in the tuner can be eliminated entirely and the chip can accept the 480-MHz IF signal directly, as shown in Fig. 4(c). In this mode of operation, the signal is downconverted on-chip to a 32-MHz IF using a 512-MHz mixer clock generated by the PLL and then directly sampled by a single 8-bit A/D converter operating at a 128-MHz sample rate. The I/Q demodulation is then performed digitally in the receiver.

III. Analog Front End

The integrated analog front end (AFE) accepts an analog input waveform in one of three formats: 480-MHz IF, low-frequency IF, or baseband I/Q. Fig. 5(a) shows a block diagram of the AFE, which switches the input signal according



(a)



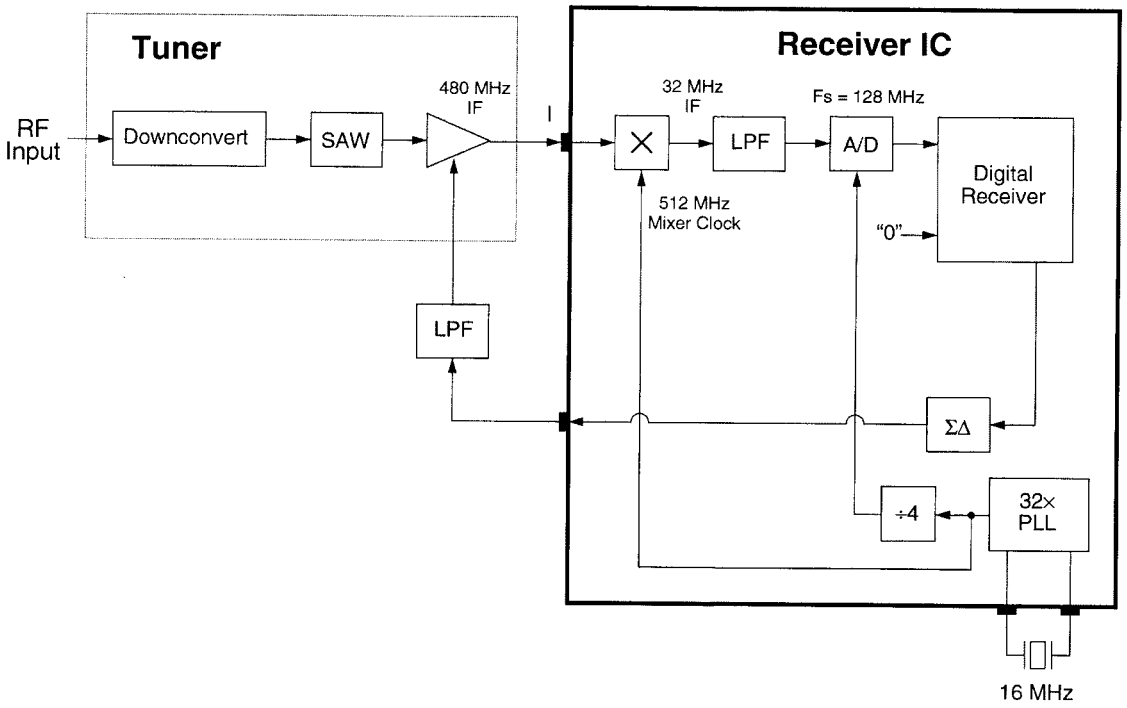
(b)

Fig. 4. Tuner interface modes: (a) baseband I/Q and (b) low IF.

to the desired mode of operation. The signal path for each of the three modes is indicated in the figure.

In the 480-MHz IF mode, the chip accepts a BPSK/QPSK/OQPSK input signal centered at 480 MHz. This signal is internally mixed to a lower IF frequency of 32 MHz using a 512-MHz on-chip PLL. It is then low-pass filtered and converted to a digital signal by an 8-bit A/D converter operating at a sampling rate of 128 MHz. A simplified schematic of the CMOS mixer and a block diagram of the PLL are shown in Fig. 5(b) and (c). The on-chip PLL is a four-stage differential ring oscillator operating at an internal frequency of 512 MHz. The 512-MHz clock is divided by 32 and phase-locked to a 16-MHz off-chip crystal reference.

In the low-frequency IF mode of operation, the chip accepts an IF input signal with a frequency spectrum within the A/D converter's Nyquist bandwidth. In this low-IF mode, the on-chip 480-MHz mixer is bypassed, and the signal is converted by the 8-bit A/D converter operating at a sampling rate of 128 MHz. Last, in the baseband I/Q mode, the chip accepts



(c)

Fig. 4. *(Continued.)* Tuner interface modes: (c) 480-MHz IF.

baseband I and Q input signals, which are sampled by dual 8-bit A/D converters operating at a maximum sampling rate of 128 MHz.

The ADC utilizes folding, interpolation, and averaging to achieve good integral- and differential-nonlinearity with relatively low complexity and power [1]. It differs from the ADC described in [1] in that it operates at a much higher sample rate (128 versus 50 Msample/s) with reduced resolution (8 versus 10 bits). Also the noise environment on the chip is quite different due to the integrated 45-MBaud digital receiver and FEC circuits. The ADC uses two cascaded stages of three times folding to reduce the number of comparators required from 256 to 32. Fig. 6(a) and (b) shows the measured integral nonlinearity (INL) and differential nonlinearity (DNL) for the 8-bit ADC. Fig. 7 shows the measured ADC output frequency spectrum for an input tone at 11 MHz. All measured data were taken with the chip in 480-MHz IF mode and with the digital receiver and FEC locked (i.e., all digital circuitry on the chip operating). The power dissipation of the ADC is approximately 160 mW from a 3.3-V supply. Since the 512-MHz mixer was designed to achieve 10-bit linearity, the performance of the analog front end is dominated by that of the ADC.

IV. Digital Receiver

The digital receiver is a BPSK/QPSK/OQPSK receiver capable of variable-rate operation from 1 to 45 MBaud. It consists of a frequency recovery loop, variable-rate digital filters controlled by a timing recovery loop, square-root Nyquist matched filters, a phase tracking loop, and circuitry to control loading the inputs to the Viterbi decoder. A block diagram of the receiver is shown in Fig. 8. The inputs to the frequency recovery loop and phase tracking loop can be taken from several different points in the system, allowing the loops to be operated independently or nested together under software control. This flexibility provides optimal performance of the receiver under varying operating conditions.

The automatic gain control (AGC) loop is a noncoherent loop designed to maintain a constant input power level into the A/D converters. The loop produces a 1-bit $\Delta\Sigma$-modulated output that is filtered off chip by a simple RC low-pass filter, providing a voltage control for the tuner's AGC amplifier. Input for the loop can be taken from either the I-channel or the Q-channel data, or an average of the two. A programmable loop threshold allows the input power level to be specified by the user.

The carrier frequency recovery and phase tracking loops are high-speed all-digital phase/frequency circuits capable of tracking out relatively large amounts of frequency offsets and phase noise such as those contributed by conventional tuners and LNB's. The loops are each filtered by an integral-plus-proportional filter. Programmable integrator and linear coefficients are provided to set the bandwidth of the loops, and a carrier sweep capability is included to reduce acquisition time and avoid all false lock points [2]. The output of the loop filter is used to control a complex derotator [3], providing extremely fine phase and frequency resolution. The phase/frequency recovery loops are capable of removing residual phase and frequency offsets in the signal of up to ± 16 MHz. An important parameter for satellite receivers is acquisition time. The automated frequency recovery loop in this receiver can acquire an input signal with ± 16-MHz offset in less than 50 ms.

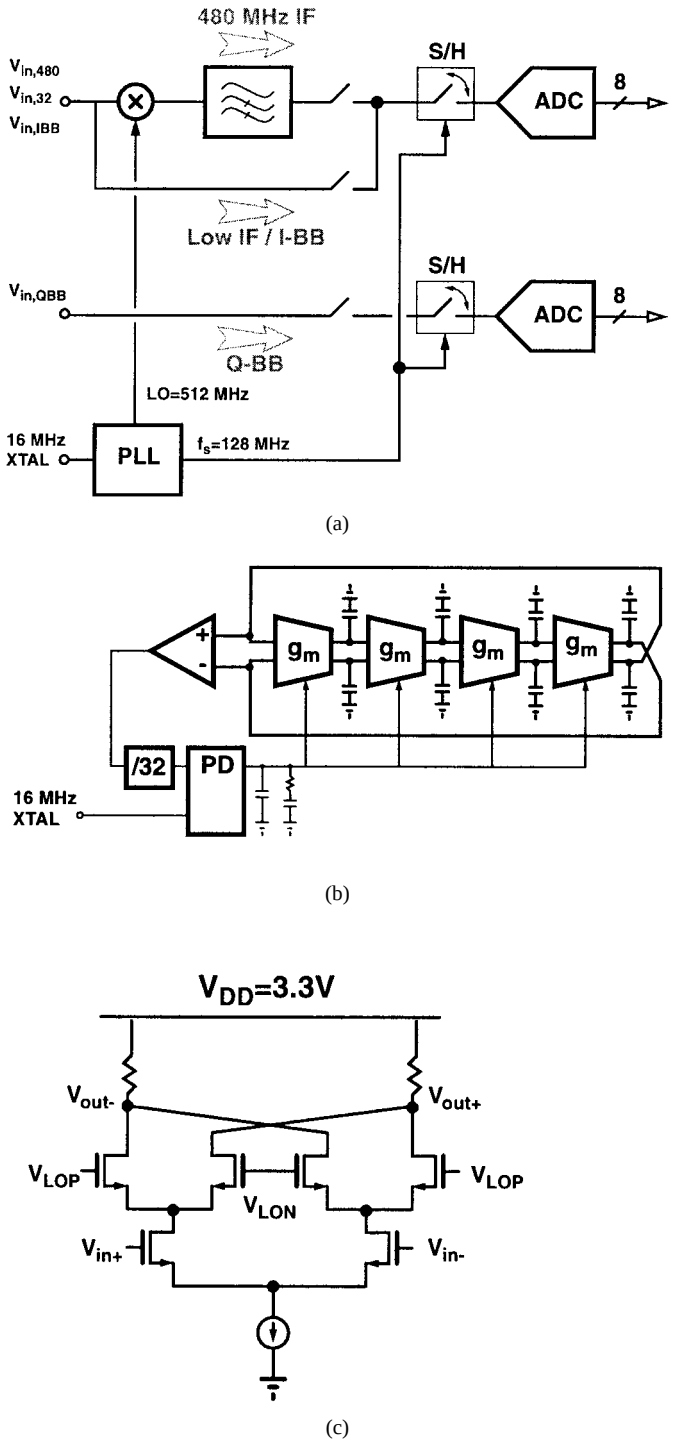


Fig. 5. (a) Analog front end block diagram, (b) PLL block diagram, and (c) CMOS mixer schematic.

The timing recovery loop consists of a timing error discriminant, a loop filter, and a digital timing recovery block, which controls the digital resampler. The timing error discriminant outputs a new value each symbol, which is filtered by a digital integral-plus-proportional low-pass filter. The output of the loop filter is applied to a numerically controlled oscillator, which allows the symbol rate to be varied from 1 to 45 MBaud. The variable-rate interpolation filters [4], which are under the control of the timing recovery loop, resample the input data at the correct frequency and phase to ensure that ideally sampled symbols are input to the matched filters. The matched filters consist of dual square-root Nyquist filters with a programmable 20% or 35% excess bandwidth factor. The output of the Nyquist filters is then scaled to optimally load the Viterbi decoder.

The receiver can also be configured to perform spectral analysis of the input signal with a resolution less than 50 kHz to aid in "blind" acquisition when the carrier frequency and/or symbol rate are not known.

Although the satellite-TV QPSK receiver architecture is similar to that of a quadrature amplitude modulation (QAM) receiver for cable-TV applications [5], there are some significant differences. The first major architectural difference is that the carrier recovery loop must be closed at the front end of the receiver to compensate for the large allowable frequency offset in the input signal (up to ± 5 MHz). This frequency offset is introduced in the LNB when the signal is downconverted from 11–12 GHz to 950–2150 MHz. This offset is very small as a percentage of the K-band carrier frequency; however, it is a rather large absolute offset that must be removed at the front of the receiver to ensure that the signal is within the passband of the matched filters. In the case of a cable system, the transmitted signal is typically on a carrier less than 1 GHz so the frequency offsets at the input of the receiver are much smaller. The second major architectural difference is that little or no equalization is required in the satellite-TV receiver. In a cable system, the channel contains many impairments that cause notches in the spectrum and intersymbol interference (ISI). An equalizer is typically required to remove these impairments. In the satellite-TV system, however, cable-type impairments are not typical because the signal is transmitted on a very high-frequency carrier (11–12 GHz) through a "line-of-sight" channel to the receiving antenna. The main impairment in the satellite-TV system is noise in the channel. Since the signal is transmitted from a satellite in orbit many miles from the receiver, it typically has a very low signal-to-noise ratio (SNR) at the input to the receiver (typically 5–10 dB). The cable channel, on the other hand, typically has a very high SNR ($\sim$30 dB). The low SNR of the satellite-TV system mandates the use of a lower order modulation format (QPSK) versus the higher order modulation formats used in the cable-TV systems (64/256/1024-QAM). Because of the lower order modulation format, the symbol rate must be increased to achieve comparable bit rates, thus requiring the use of more dedicated hardware (i.e., less hardware sharing in the architecture).

Fig. 9 shows the receiver constellation for a 1-MBaud input signal with no noise, clearly illustrating the wide dynamic range of the 8-bit A/D converters and the datapath in the receiver. The receiver performance including a conventional tuner is typically within 0.2 dB from theory at quasi-error-free operating conditions. Fig. 10 shows measured bit error rate (BER) performance of the receiver for 1-, 20-, and 45-MBaud input signals. All data were taken using the 480-MHz IF input mode with the A/D converter sampling at 128 MHz and include the degradation of a conventional 480-MHz L-band tuner. For all symbol rates, the overall

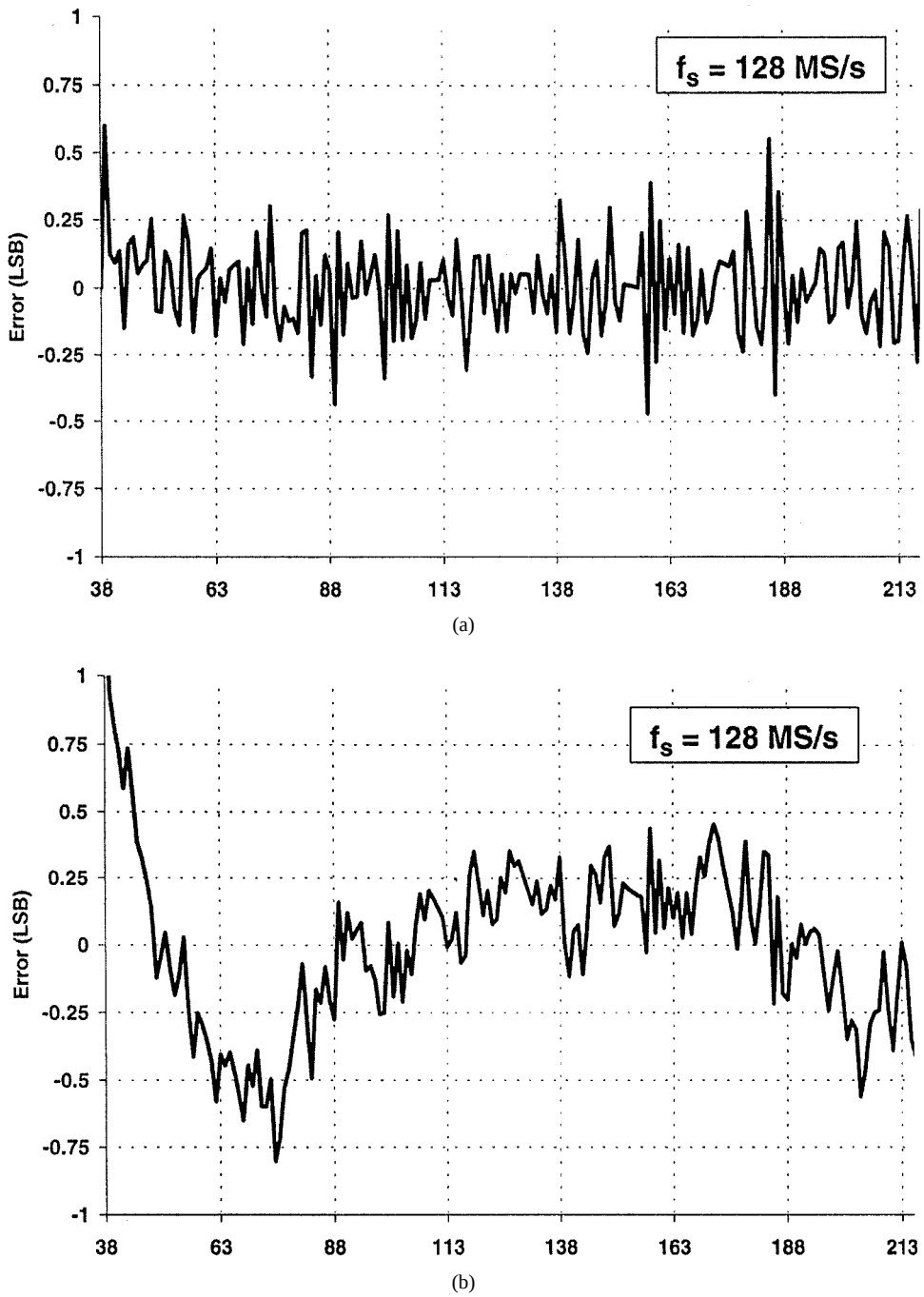


Fig. 6. Measured (a) ADC DNL and (b) ADC INL.

degradation (receiver + tuner) is well within the required DVB limit of 0.8 dB. The best performance occurs at 20 MBaud, approximately in the center of the 1–45-MBaud range. The performance degrades slightly at the two extremes of 1 and 45 MBaud. The degradation at 1 MBaud is primarily due to phase noise in the tuner and finite wordlength effects in the digital filters that recover the symbol timing from the highly oversampled input data (128-MHz sample rate versus 1-MBaud input signal) when adjacent channel interferers are present. The primary cause for the performance degradation at 45 MBaud is that the tuner's 55-MHz SAW filter cuts off some of the excess bandwidth of the input signal. (Note that a 45-MBaud signal shaped by a square-root Nyquist filter with a 0.35 alpha has a bandwidth of 60.75 MHz.) Additionally, the performance of the chip's analog front end degrades as the signal approaches the Nyquist frequency of the A/D converters.

Typical satellite systems operate in extremely noisy environments. Thus, receiver performance under low SNR conditions (i.e., high noise levels) is extremely important. Also, since the tuner's SAW filter bandwidth must be wide enough to pass a 45-MBaud signal, at lower symbol rates significant out-of-band energy is allowed to pass through to the receiver, and sufficient filtering must be performed in the variable-rate

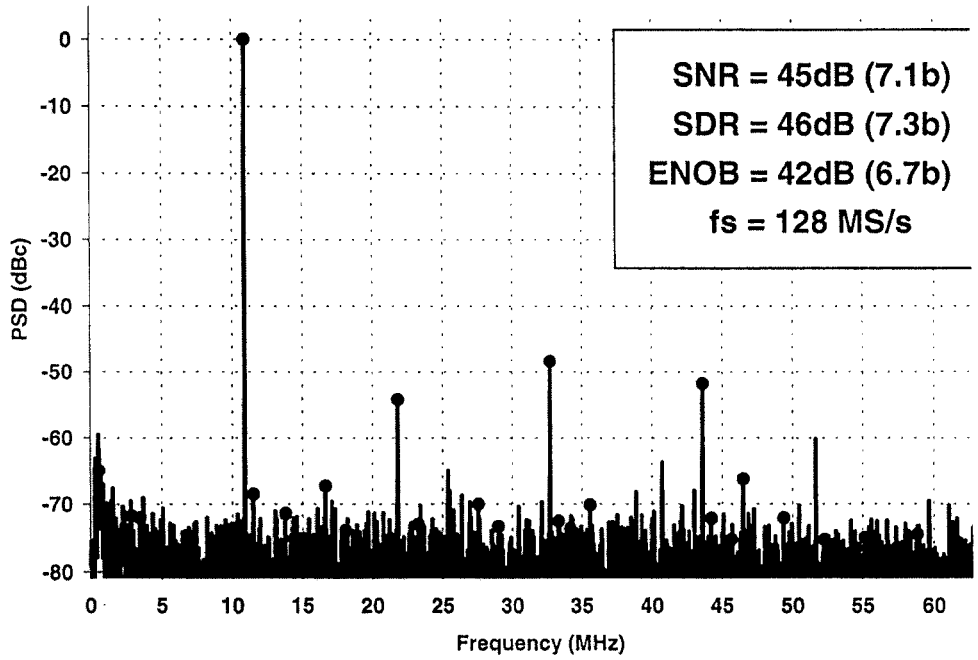


Fig. 7. Measured ADC frequency spectrum for 11-MHz input tone.

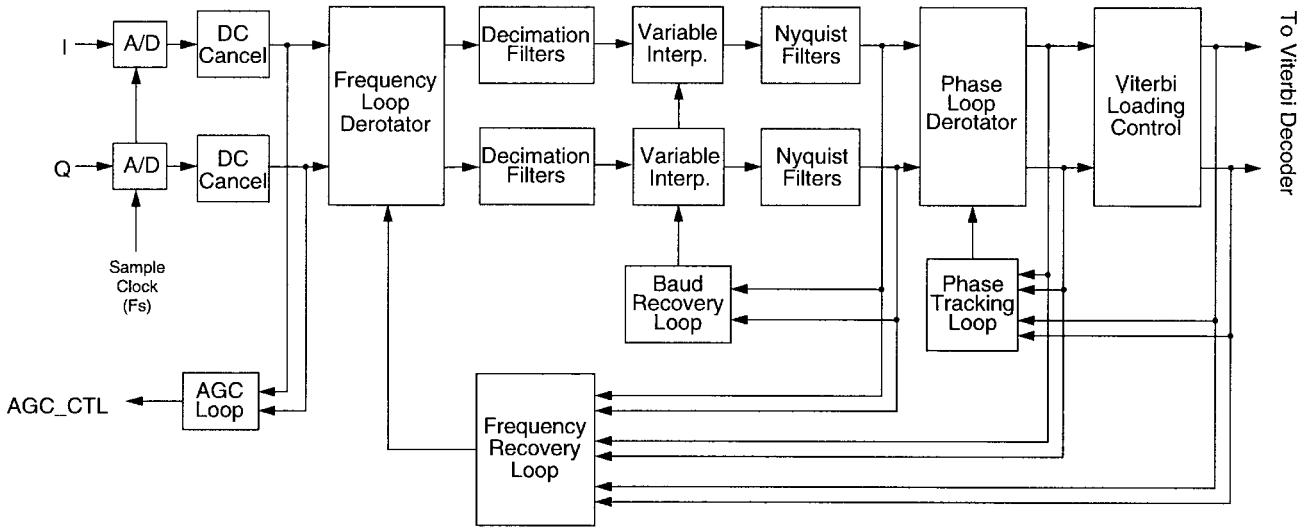


Fig. 8. BPSK/QPSK/OQPSK receiver.

receiver to remove the out-of-band energy. Fig. 11 shows a 4.42-MBaud signal in a 3-dB SNR (0-dB Eb/No) noise environment with two interfering signals within the bandwidth of the A/D converters, each +8 dB higher in power. Measured data show that the receiver's BER degradation due to the interferers is less than 0.1 dB. This is due to the 8-bit resolution of the A/D converters and the advanced multirate digital filtering in the datapath. Under high-noise operating conditions, QPSK receivers also suffer from a phenomenon known as cycle slips, where the receiver instantaneously "slips" phase lock by 90°, 180°, or 270°. The cycle slip cannot be detected by the receiver because it remains in lock, just with a different phase. Cycle slips occur when transmitted symbols repeatedly appear to the receiver as an adjacent symbol because of the additive noise in the channel. As the noise level in the channel increases, the cycle slip rate of the receiver also increases. The IC described in this paper uses two approaches to improve the cycle-slip performance of the receiver. The first is to use a low delay loop for carrier phase tracking (see Fig. 8), which allows for a much wider loop bandwidth and improved phase noise performance. The second improvement is the addition of a nondecision directed phase detector in the carrier tracking loop that has been optimized for low SNR operation [6]. Using these techniques, the receiver is capable of reliably acquiring an input signal at an SNR of 2.0 dB (Eb/No $= -1.0$ dB) with measured cycle-slip performance better than one slip every three hours using a conventional satellite tuner. Fig. 12 shows measured cycle-slip

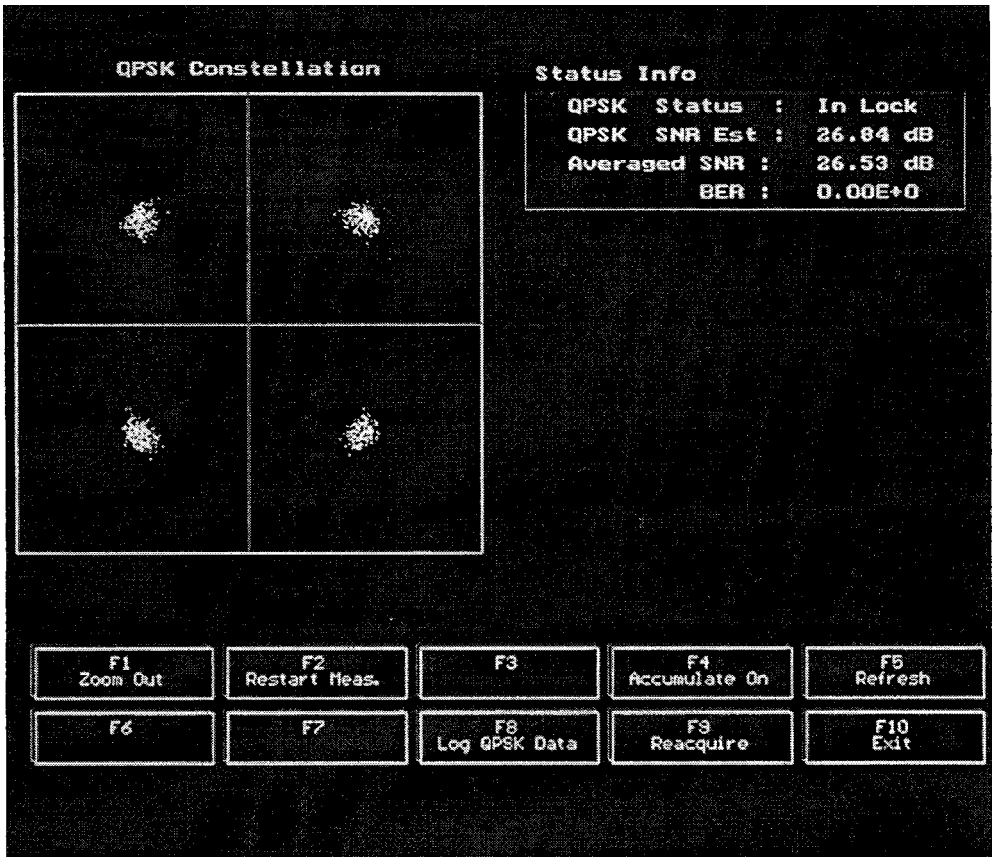


Fig. 9. Receiver constellation for a 1-MBaud input signal with no noise.

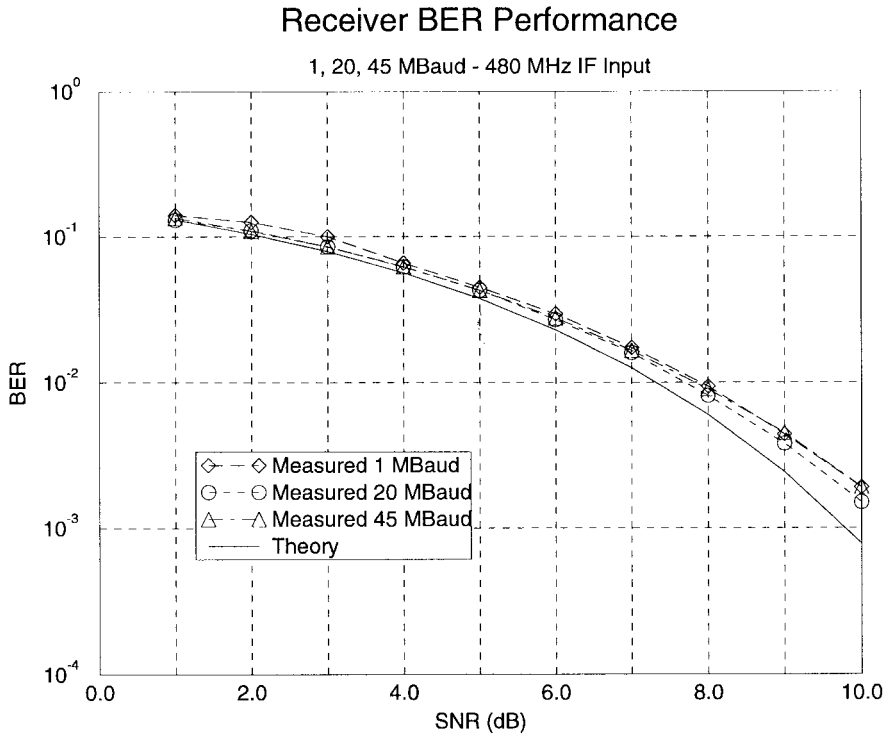
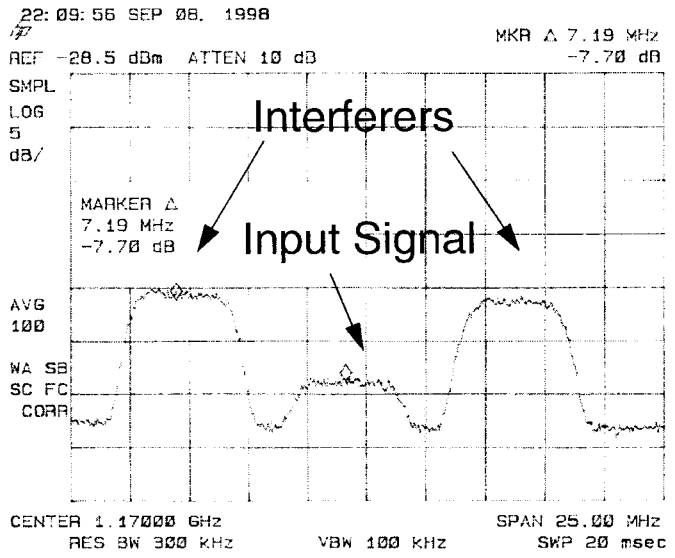
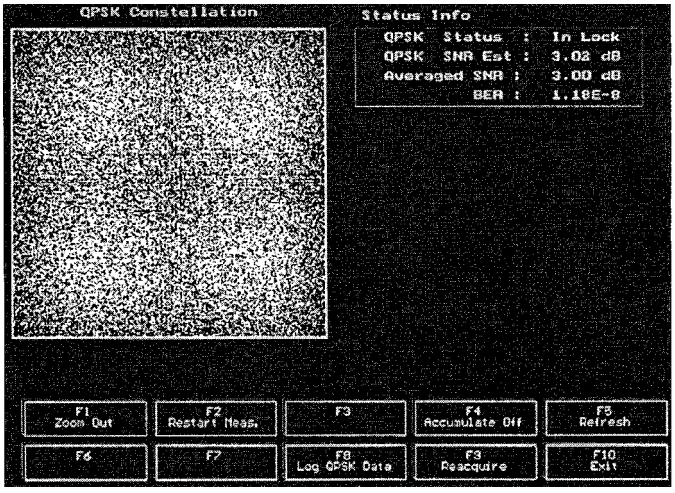


Fig. 10. Receiver BER performance for 1, 20, and 45 MBaud.



(a)



(b)

Fig. 11. Input spectrum and QPSK constellation plot for 4.42-MBaud input with +8-dB interferers in 3-dB SNR noise environment.

performance of the receiver versus SNR using the 480-MHz IF input mode with a conventional L-band tuner.

V. Forward Error Correction

Since satellite systems operate in extremely noisy environments, powerful error correction is required to achieve bit error rates appropriate for transmission of digitally compressed video signals. This IC contains an FEC decoder compatible with the European Digital Video Broadcast (DVB), DirecTV Digital Satellite System (DSS), and Primestar DigiCipher I/II forward error correction and framing scheme for satellite transmission. To achieve the level of error detection and correction required, a concatenated FEC code is used. This code is based on convolutional encoding for the inner code and RS encoding for the outer code. Protection against burst errors is achieved using byte interleaving. To support these functions, the decoder consists of five layers: Viterbi decoding, frame synchronization, convolutional deinterleaving, RS error correction, and derandomization.

The Viterbi decoder can decode two families of constraint length $K = 7$, 64-state punctured convolutional codes: the DVB/DSS rate 1/2 (171, 133) code and the DigiCipher I/II rate 1/3 (117, 135, 161) code. The Viterbi decoder consists of a depuncturing block, a dual-rate capable 64-state Viterbi core, and a node synchronization block, as shown in Fig. 13. The depuncturing block supports puncture rates 1/2, 2/3, 3/4, 5/6, 6/7, or 7/8 for the DVB/DSS rate 1/2 code, and puncture rates 5/11, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, or 7/8 for the DigiCipher I/II rate 1/3 code. The depuncture block accepts QPSK, BPSK, or offset QPSK (OQPSK) soft decisions from the receiver and inserts dummy cycles to restore the original rate 1/2 or 1/3 timing relationship before sending the data stream to the Viterbi core. The 64-state Viterbi core design employs a dual-rate capable add-compare-select block that can handle both codes with minimal chip area penalty. The node synchronization block corrects the receiver phase ambiguity and depuncturing timing ambiguity in the decoding process. In the case of a receiver cycle slip, the node synchronization logic will attempt to correct the cycle slip before triggering the resynchronization process. The node synchronization block also provides the capability to automatically scan for the correct puncture rate. The frame synchronization block will recover either MPEG-2 or DSS transport framed data streams as defined in the DVB, DSS, and DigiCipher I/II specifications.

In order to deal with burst errors in the channel, the coded data stream is interleaved so that the bursty channel is transformed into a channel having independent channels. The convolutional deinterleaver supports all of the standards by providing programmable interleaving depths of 1, 2, 3, 4, 6, 12, and 13 and programmable block sizes. The deinterleaving RAM is included on-chip.

The RS decoder supports $t = 8$, $(n, k) = (204, 188)$ or $(146, 130)$; or $t = 5$, (125 115) systematic Reed–Solomon codes. For DVB, DSS, or DigiCipher II applications, the RS code is a systematic code with 8-bit symbols, shortened from a block length of 255 symbols and correcting up to $t = 8$ symbols per block. The finite field GF (256) is constructed from the primitive polynomial $P(x) = x^8 + x^4 + x^3 + x^2 + 1$. The generator polynomial is $g(x) = (x + \alpha^0)(x + \alpha^1) \cdots (x + \alpha^{15})$. The data randomization block scrambles data with a pseudorandom number sequence for energy dispersal and to ensure a high data transition density for timing recovering purposes.

VI. Chip Performance

The IC has been extensively tested and is being deployed in DBS systems around the world. BER performance of the device has been measured to be well within all DVB, DSS, and DigiCipher I/II specifications. Fig. 14 shows BER performance for 1-, 20-, and 45-MBaud operation at three different Viterbi puncture rates using the 480-MHz IF input mode and a conventional L-band tuner. These performance data span the chip's operating range from 1 to 45 MBaud symbol

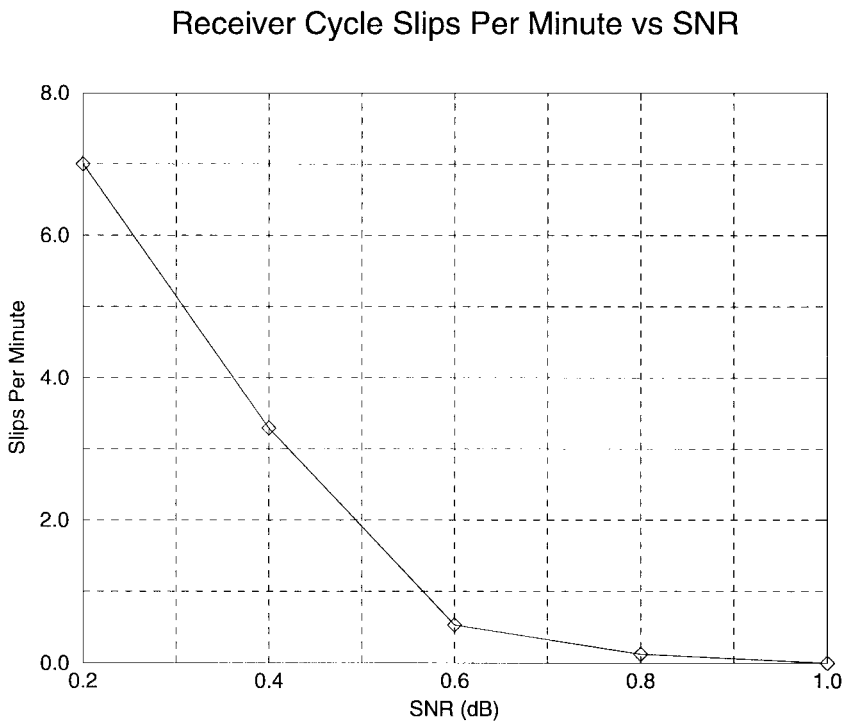


Fig. 12. Receiver cycle-slip performance.

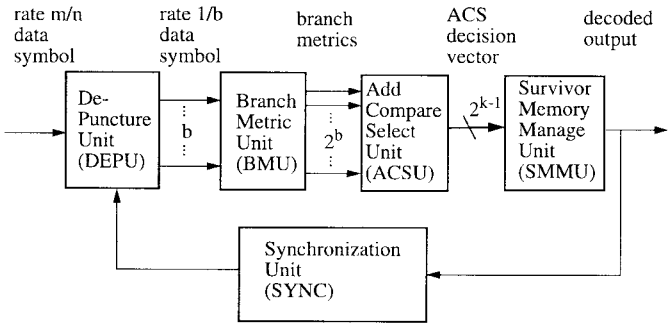


Fig. 13. Viterbi decoder block diagram.

TABLE I
IC SUMMARY

function	BPSK / QPSK / OQPSK satellite receiver and FEC
symbol rate	1 - 45 MBaud variable rate
FEC	DVB / DSS / DigiCipher I/II
sample rate	128 MHz
# of transistors	1.2 million
die area	22 mm^2 (including pads)
technology	0.35-μm single poly, quad metal
power dissipation	2.1W @ 45 MBaud, Fs=128 MHz
package	80-pin PQFP

rates and puncture rates from 1/2 to 7/8. Since the Viterbi and Reed–Solomon decoders are all-digital operations whose performance degradation is independent of the symbol rate, the chip's performance loss is dominated by the performance loss of the receiver. Thus the best performance for the overall chip occurs in the 20-MBaud example with some performance degradation at the two extremes of 1 and 45 MBaud, as was the case for the receiver performance by itself. For all cases, the chip's performance is within the required DVB limit of 0.8-dB loss, including the effects of the L-band 480-MHz tuner.

Fig. 15 shows the chip micrograph. The IC is packaged in an 80-pin PQFP package. Power dissipation is 2.1 W at worst case supply voltage of 3.465 V (3.3 V + 5%) with 128-MHz sample rate and 45-MBaud symbol rate under worst case temperature and process. The power dissipation breakdown is 0.7 W for the analog circuitry and 1.4 W for the digital circuitry.

Table I summarizes the details of the IC.

VII. CONCLUSION

Currently, most satellite tuners output analog I- and Q-waveforms at baseband. The 480-MHz IF mode for the IC

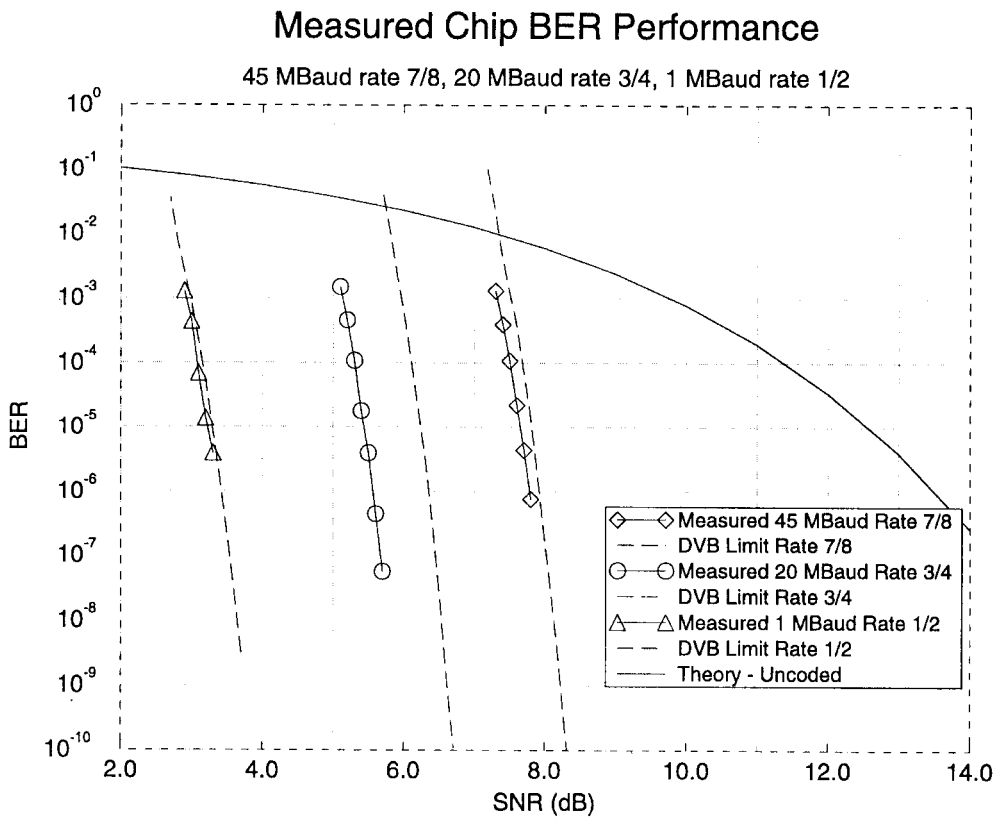


Fig. 14. Overall chip BER performance for 1-MBaud rate 1/2, 20-MBaud rate 3/4, and 45-MBaud rate 7/8 QPSK.

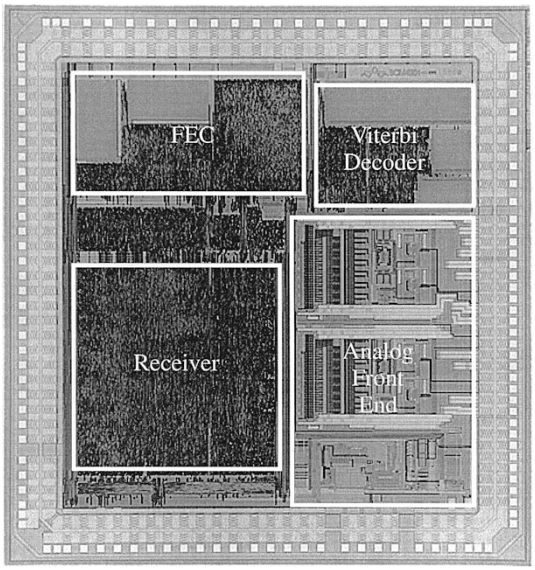


Fig. 15. Chip micrograph.

described above allows the I/Q demodulator in the tuner to be removed, significantly reducing the overall system cost. Similar solutions accepting 480-MHz IF input reported previously have been implemented as two or more chips, with the high-IF analog signal processing being realized in a bipolar IC and the digital signal processing in a CMOS IC [7]. All components of the AFE described above are implemented in a standard digital CMOS process, and all measured system performance data include the effects of digital switching noise on the 480-MHz analog front end.

ACKNOWLEDGMENT

The authors wish to thank J. Echtenkamp, K. Kindsfater, S. Tollefsrud, R. Hawley, A. Buchwald, M. Hatamian, V. Nguyen, D. Bogosh, I. Tsiperfal, F. Syed, and P. LaRocca for contributions to the development of this design.

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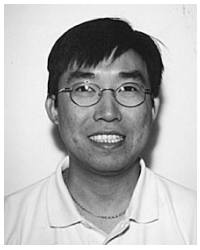

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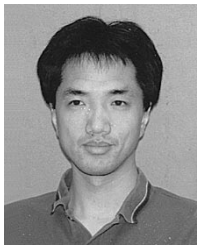

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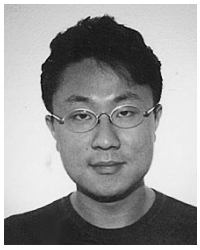

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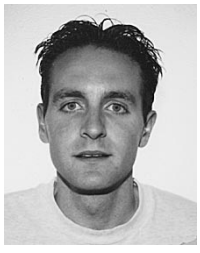

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Klaas Bult, photograph and biography not available at the time of publication.

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