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A Digitally Programmable Rail-to-Rail CMOS Operational Amplifier as Reusable Silicon IP

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Abstract

A digitally programmable rail-to-rail CMOS operational amplifier (Op Amp) is designed using standard 0.35 μm CMOS process. By using an efficient MOS capacitor is used to compensate the stability of the Op Amp. A compensation current switch is used to adjust the slew rate. Using the schemes, the Op Amp can obtain improved the stability, bandwidth, slew rate and settling time according to the output load.

Key Words: Op Amp, Rail-to-Rail, Programmable

1. Introduction

An Op Amp is a basic block in analog and mixed-signal processing circuits, such as A/D, D/A circuits, switched-capacitor circuits and filters. With the reduction of the supply voltage, the performance of CMOS analog building blocks is degraded. The operation of the input stage is specially limited by the supply voltage. Thus, circuit design techniques to regain operating range and maintain good performance must be developed.

For low-voltage Op Amp, a rail-to-rail operation is considered to keep a wide input/output signal range and good signal-to-noise ratio (SNR). The simple rail-to-rail input stage with an n-channel differential pair and a p-channel differential pair are connected in parallel shown in Figure 1 [1]. The total transconductance gm is halved at the ends of positive and negative input rails. To reduce signal distortion and maintain high performance, it is necessary to keep constant gm over the entire rails.

The current switch is used to compensate and maintain constant gm over entire rails [2–7]. However, the gm of the n-channel input and that of the p-channel pairs have to be matched to perform constant gm . A rail-to-rail

input stage without gm matching is applied in this work [8]. A class-AB output stage is used to improve power efficiency and faster response. A programmable MOS capacitor controlled by digital signals is applied to compensate the stability of the Op Amp according to the output load. A programmable current switch is applied to adjust the slew rate and settling time.

2. A Digitally Programmable Rail-to-Rail Op Amp

Figure 2 shows the block diagram of the proposed Op Amp. The architecture is composed of a bias circuit, a constant- gm rail-to-rail input stage, a current summing circuit, a class-AB output stage, and a programmable compensation scheme. The bias circuit provides the current sinks and the current sources. The input stage keeps constant total gm over entire input common-mode range and maintains less signal distortion. The current summing circuit is used to sum the input currents and convert current gain into voltage gain. The class-AB output stage with high driving capacity can obtain wide swing. The programmable schemes are composed of the programmable MOS capacitor and compensation current switch. The stability can be obtained according to the output

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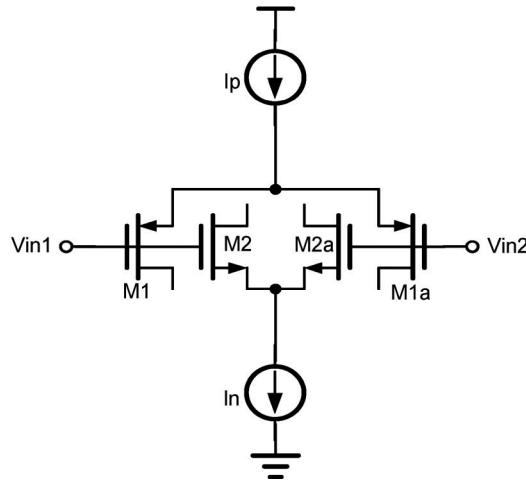


Figure 1. Simple rail-to rail input stage [1].

loads. The slew rate is controlled by compensation current switch to meet the output requirement.

Figure 3 shows the schematic diagram of a bias circuit. The output current depends on resistor R1. The device size of MC2 is four times that of MC4. The bias current is independent of the supply voltage variation.

Figure 4 shows the bias circuit of the constant-*gm* input stage. The constant transconductance can be obtained by the formula,

$$V_{SG5} + V_{GS6} = V_{SG4} + V_{GS3} \quad (1)$$

Assuming all transistors are operating in strong inversion, Eq. (1) can be written as,

$$\sqrt{\frac{I_c}{K_n}} + V_{T_6} + \sqrt{\frac{I_d}{K_p}} + V_{T_5} = \sqrt{\frac{I_n}{K_p}} + V_{T_4} + \sqrt{\frac{I_p}{K_n}} + V_{T_3} \quad (2)$$

Since the p-channel transistors Mb4 and Mb5 have a

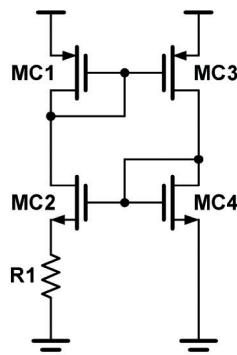


Figure 3. Schematic diagram of bias circuit.

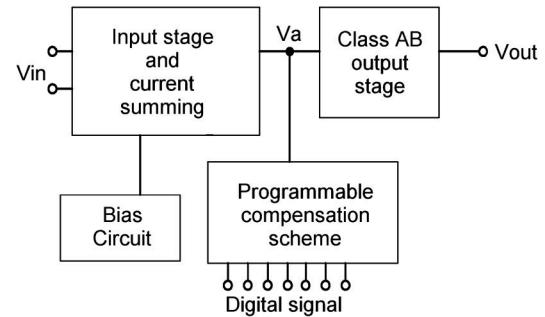


Figure 2. Block diagram of the programmable Op Amp.

common source terminal, the body effect of these transistors should be cancelled to the first order. That is, the device threshold voltage $V_{T_4} = V_{T_5}$. The n-channel transistors Mb3 and Mb6 also satisfy $V_{T_3} = V_{T_6}$. Therefore,

$$\sqrt{\frac{I_c}{K_n}} + \sqrt{\frac{I_d}{K_p}} = \sqrt{\frac{I_n}{K_p}} + \sqrt{\frac{I_p}{K_n}} \quad (3)$$

Multiplying both sides of Eq. (3) by $\sqrt{2KnKp}$, we get

$$\sqrt{2InKn} + \sqrt{2IpKp} = \text{Constant} \quad (4)$$

Figure 5 shows the complete Op Amp. The input stage is composed of a modified constant bias circuit (M3~M13), a rail-to-rail input stage (M1, M1a, M2, M2a), a current monitor (M3a, M3b), and a constant current circuit (Mb1~Mb9). The modified constant bias circuit can obtain constant *gm* as proved in Eqs. (1)–(4). Using the modified constant bias circuit, the transconductance

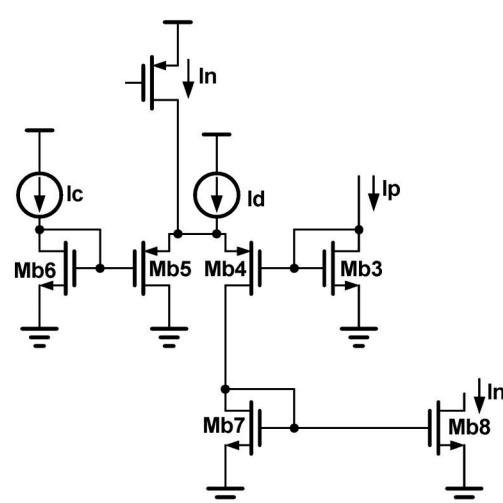


Figure 4. Bias circuit of the constant-gm input stage.

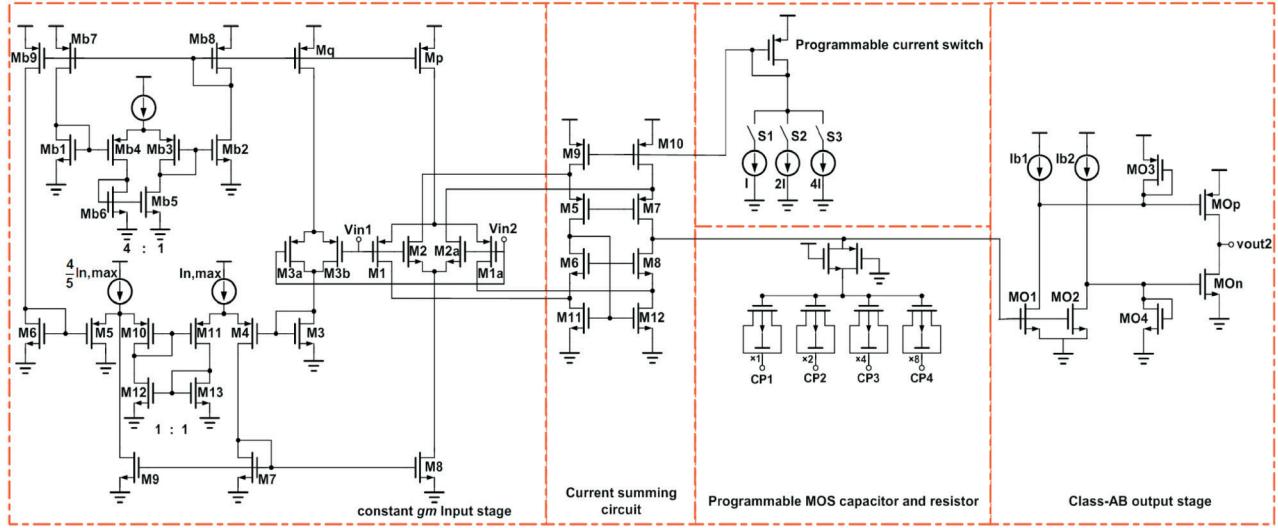


Figure 5. The complete Op Amp (without bias circuit).

still remains constant in weak inversion. The source terminals of M4 and M5 are separated. The voltages at these nodes maintain equal by matching the device M10, M11, M12 and M13. The drain currents in M10 and M11 are equal according to the current mirror M12 and M13. Therefore, their gate-to-source voltages are equal. A constant current source $I_{n,max}$ supplies currents to M4 and M11. The current through M4 and M8 are limited by $I_{n,max}$. It is independent on $VGS3$. The current monitor is to simulate the current which flows through p-channel input pair M1 and M1a. The constant current circuit can keep a constant total transconductance at full rails.

The current summing circuit is used to sum the p-channel and n-channel input current and to transfer the input stage total current to voltage. The cascode structure obtains high voltage gain due to its high output resistance. However, the bandwidth is degraded as the output load increases. The second stage is used to prevent the bandwidth degradation. The programmable current switch is the bias of the current summing circuit. We can use current switch to adjust the current through the current summing circuit. By changing the current through current summing circuit, the slew rate can be improved. The current can be programmed by the current switch.

Figures 6(a), (b) shows the implementation of MOS capacitors. Figure 6(c) plots the C-V curves. Using the inversion-mode MOS varactor, the digital signal can be applied to adjust precisely the capacitance value. PMOS devices in n-well are used to implement the capacitors.

The bulk terminal is connected to Vdd. The MOS capacitors share a common n-well. Four different sizes of MOS capacitors are connected in parallel to obtain 16 capacitance values shown in Figure 7. A CMOS trans-

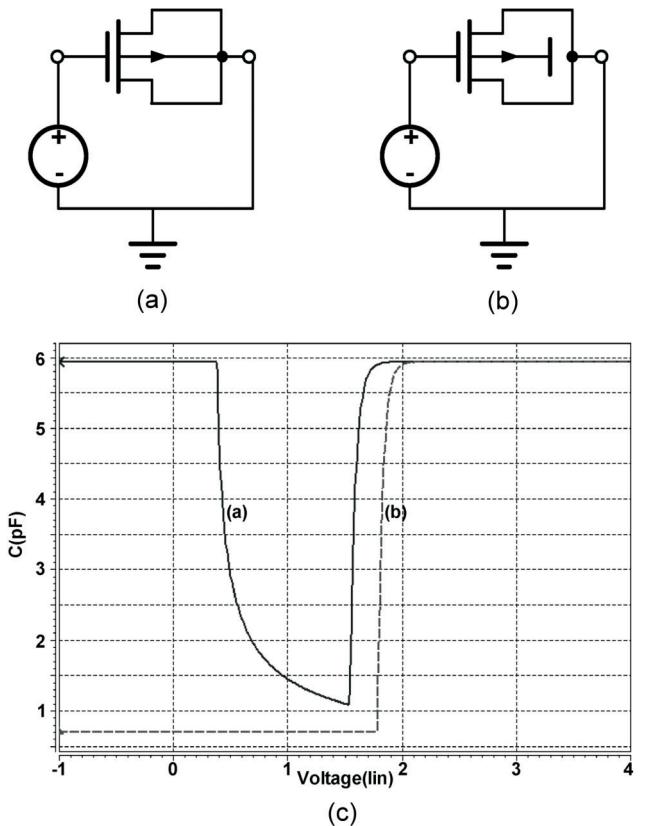


Figure 6. (a) MOS capacitance, (b) inversion-mode MOS varactor, (c) C-V curve.

mission gate plays the resistor. A zero is obtained using the compensation capacitor and resistor. The stability of the Op Amp can be improved by increasing the capacitance value. However, the bandwidth is sacrificed. Moreover, the slew rate is degraded.

A class-AB output stage shown in Figure 5 [9] provides a low output resistance and high power efficiency. Therefore, the bandwidth is not degraded at large output load. Using MO3 and MO4, the operation of MOp and MOn does not turn into weak inversion. MO1 and MO2 are quiescent current control devices which keep MOp and MOn in class-AB operation.

3. Simulation Result

This Op Amp is simulated using 0.35 um CMOS device parameters. The small-signal frequency response of the Op Amp with various output loads is shown in Figure 8. The stability is reduced as the output load increases.

The dimensions of four programmable MOS capacitor sizes are (66/20), (66/20) \times 2, (66/20) \times 4, (66/20) \times 8.

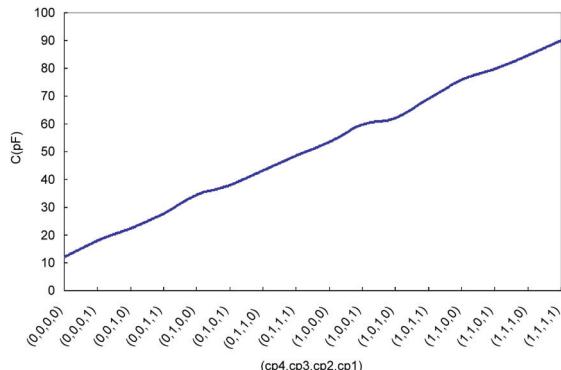


Figure 7. The value of compensation capacitor which is changed by CP1~CP4.

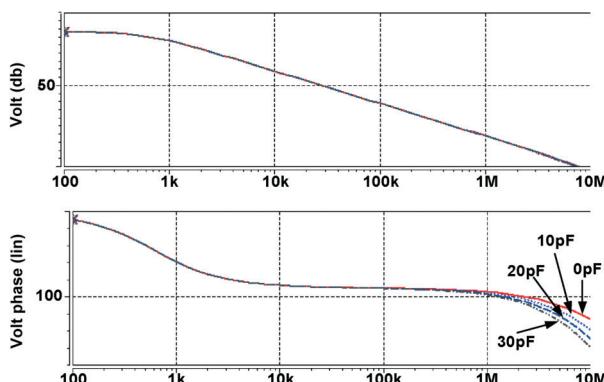


Figure 8. The frequency response at various output loads.

The stability can be adjusted by programming the value of the MOS capacitor to achieve the best performance according to the output requirement. Figure 9 shows the improvement of stability by controlling the (CP1, CP2, CP3, CP4). Figure 10 shows the allowable maximum load to achieve 45° phase margin.

The current through current summing circuit programmed by S1~S3 is shown in Table 1. Figure 11 shows the unit-gain operation at various programming current. The slew rate of the Op Amp is related to compensation capacitance C_c and the first stage bias current I_b . The slew rate is formula as,

$$\text{Slew Rate} = \frac{I_b}{C_c} \quad (5)$$

But we can improve the slew rate by adding the current flow the compensation capacitor C_c . The programmable

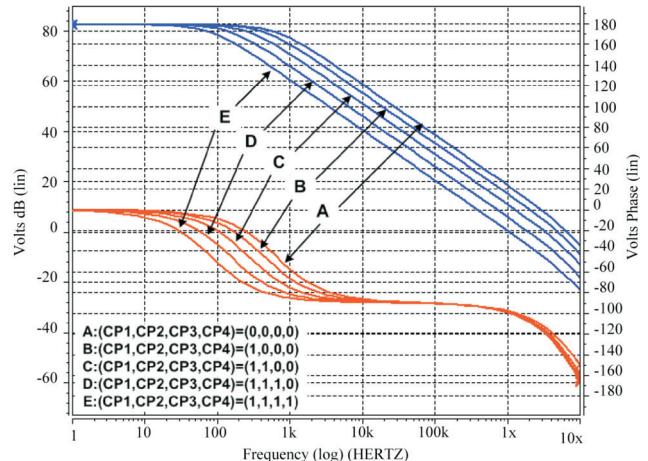


Figure 9. The stability of the Op Amp by controlling (CP1, CP2, CP3, CP4).

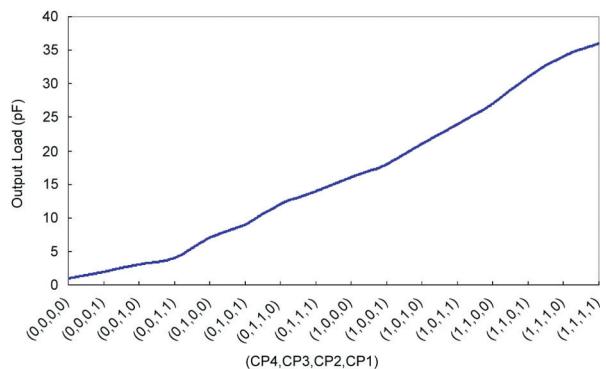


Figure 10. Allowable maximum load to achieve 45° phase margin.

current switch can adjust the current through the current summing circuit. The slew rate and the settling time are improved as the compensation capacitor increases.

The programmable compensation scheme can maintain stable operation as the output load increases. By programming the digital signals, the stability, slew rate, and the settling time as required can be obtained. Table 2 shows some results of the Op Amp. Figure 12 plots the Op Amp layout. The chip area is $270 \times 430 \mu\text{m}^2$.

4. Chip Measurement

The die photomicrograph of the Op Amp is shown in

Table 1. Programmable current

S1	S2	S3	Current (uA)
0	1	1	15
1	0	1	30
0	0	1	45
1	1	0	60
0	1	0	75
1	0	0	90
0	0	0	105

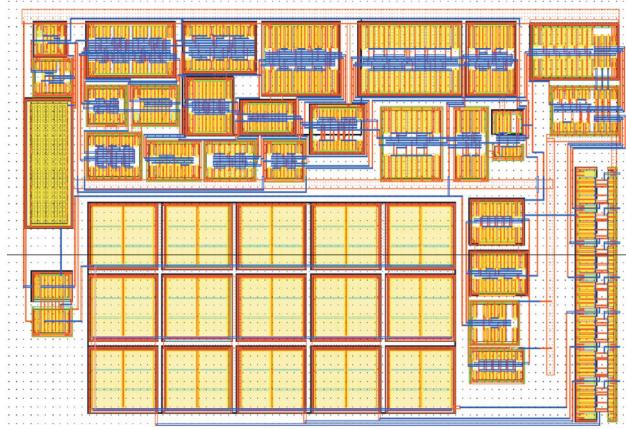


Figure 12. The test chip of the Op Amp.

Table 2. Some results of the Op Amp

PM > 45°, SR > 10 V/us						
Output	0pF	5pF	10pF	15pF	20pF	35pF
CP4~CP1	0000	0100	0110	1000	1010	1111
S1~S3	001	001	110	100	000	000
Bandwidth	23 M	7.5 M	4 M	520 k	470 k	230 k
Gain	85 dB	85 dB	80 dB	70 dB	67 dB	67 dB
Dynamic Range	53 dB	53 dB	58 dB	67 dB	70 dB	70 dB
Power dissipation	2.6 mW	2.6 mW	2.7 mW	2.9 mW	3.1 mW	3.1 mW

Figure 13. Figure 14 and Figure 15 plot the measured waveform of unity gain operation. As shown in Figure 14 and Figure 15, the slew rate and settling time can be improved by controlling (S1,S2,S3). Th3 stability of the Op Amp is not measured due to limitations of the test

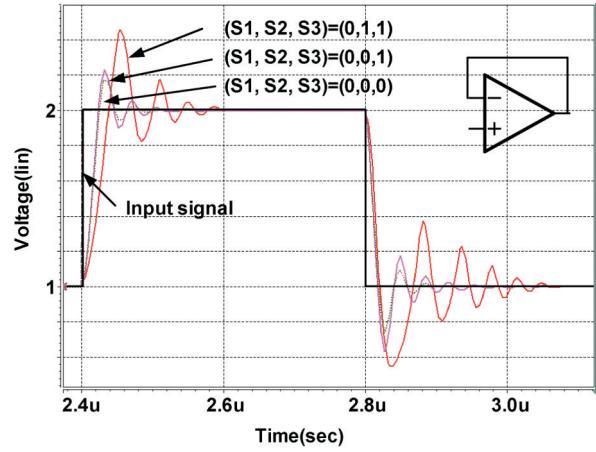


Figure 11. Unit-gain operation at various compensation current.

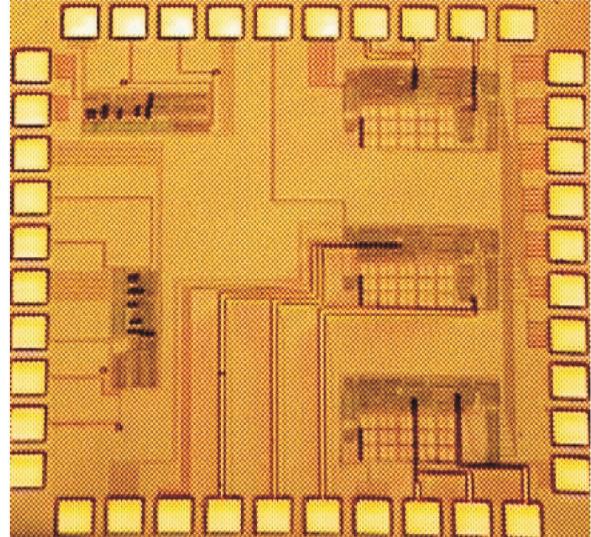


Figure 13. Die photomicrograph of the Op Amp.

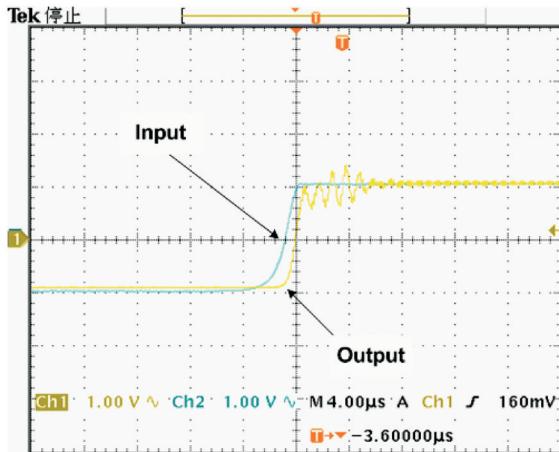


Figure 14. Unity gain operation at $(S_1, S_2, S_3) = (0, 1, 1)$.

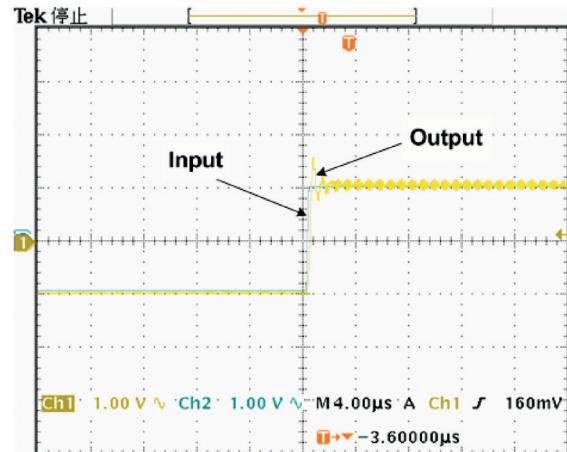


Figure 15. Unity gain operation at $(S_1, S_2, S_3) = (0, 0, 0)$.

Table 3. The comparison of simulation and measurement result

OP specification	Simulation (1)	Simulation (2)	Measurement
Power supply voltage	3.3 V	3.3 V	3.3 V
Offset Voltage	-	-	10 mV
Low frequency open loop gain	80 dB	80 dB	-
Unity-gain frequency	4 MHz	1.5 MHz	1.3 MHz
Common mode rejection ratio	120 dB	120 dB	-
Power supply rejection ratio	80 dB	80 dB	-
Phase Margin	70°	80°	-
Slew Rate	14 V/us	3.2 V/us	1.5 V/us
Input common mode Range	0.2~3 V	0.2~3 V	0.2~3 V
DC power dissipation	2.7 mW	2.7 mW	3 mW
Input voltage noise density	8u $\frac{V}{\sqrt{Hz}}$	8u $\frac{V}{\sqrt{Hz}}$	-
Total harmonic distortion	0.5%	0.5%	-
Settling time to 0.1%	0.4 us	2.3 us	4 us
Output load	10pF	40pF	-

environment. Table 3 is the comparison of simulation and measurement. Because of the load of pin and pad, the slew rate and settling time is degraded. But the programmable compensation scheme is still useful. It's still can improve the slew rate and settling time as shown in Figure 14 and Figure 15.

5. Summary

This work presents a digitally programmable rail-to-rail CMOS operational amplifier. Novel programmable schemes are proposed. The compensation capacitor is digitally controlled to achieve stable operation according the output load. A programmable current switch can

obtain required slew rate and settling time. The performance of the Op Amp can be optimized. This Op Amp is designed by standard 0.35 um CMOS process. A test chip is under fabrication. It will be measured to verify the performance of the Op Amp.

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