Laser Fine-Tuneable Deep-Submicrometer CMOS 14-bit DAC

David Marche, Yvon Savaria, and Yves Gagnon

***Abstract*—The ever-shrinking CMOS technology favors digital circuitry but imposes a challenge to the analog designer faced with limitations such as process gradients and random device variations. However, the trend to greater integration and systems-on-chips (SoCs), requires that digital and analog blocks be merged into single chips. High resolution digital–analog converters (DACs) are especially sensitive to the final matching of components and their nominal accuracy is typically enhanced with additional calibration circuitry or laser trimming. Additional calibration circuits increase cost significantly and mainstream laser trimming technique is applied on thin film resistive layers that are not available with most standard fabrication processes used for SoC. In this paper, we present a high-resolution DAC taking advantage of a new laser trimming technique which is compatible with standard CMOS processes, and that can be integrated in SoCs. While initial mismatch prevents reaching the targeted 14-bit resolution, the included tuning elements offer the necessary calibration to exceed the matching requirements and obtain the desired DAC linearity. The architecture of the DAC itself is a classic current-mode segmented resistor ladder: an inverted R2R ladder generating the binary weighted least significant bit currents is combined with unary current sources for the thermometer encoded most significant bits. The entire structure is precisely calibrated to obtain the final desired linearity. The effectiveness of the trimming technology and its application to high-accuracy DACs is demonstrated.**

***Index Terms*—Analog integrated circuits, calibration, CMOS, data converter, digital–analog conversion (DAC), laser trimming, linearity, R2R ladder.**

I. Introduction

UP UNTIL recently, the cost and performance of digital systems have been dominant forces driving the evolution of CMOS technology [1]. Speed, power consumption and area of digital circuitry are constantly and successfully enhanced by process dimension and supply scaling down. However, many cost effective systems are actually mixed signals application specific standard products (ASSPs) and systems-on-chips (SoCs) taking advantage of powerful digital signal processing (DSP) and relying to some extent on analog building blocks such as voltage reference, power-on-reset (POR), filters and data converters. In these ASSPs and SoCs, while digital designers are taking advantage of CMOS evolution, their analog peers are increasingly challenged to upgrade the performance level while migrating to newer submicrometer CMOS process generations [2].

Digital-to-analog converters (DACs) are one of the essential class of analog blocks facing high performance demand and DACs are so closely tied to digital circuitry that they are likely to be included in an ASSP or a SoC.

Among the many existing DAC architectures, the high-speed market segment is widely dominated by current-steering flash topologies.

- *Current source DACs* are unrivaled for very high-speed conversions up to the gigahertz range. With high ac performances they are a natural choice for communication applications (GSM, *x*DSL, HDTV).
- *Inverted R2R ladders* offer high precision in the Megahertz range. With high trimmed dc performances, they are favored for high absolute accuracy applications (sensors, instrumentation, digital waveform generation).

These DACs generate ratioed reference currents which are added to the output according to the digital input word. Speed is enhanced by steering any unused current source to a complementary output thus avoiding any shut-down and power-up delays in current sources.

Flash DACs resolution is mainly limited by the level of matching reached between all reference current sources and many different solutions have been explored to cancel mismatch errors caused by gradient and random variations: careful layout [3], [4] and other special techniques such as improved switching schemes [5] and dynamic element matching (DEM) [6] can reduce the mismatch effects to a certain extent. However, over 10–12 bits of resolution the matching requirement is such that some sort of calibration must be used to obtain the desired full accuracy.

Post processing calibration techniques such as heavily doped polysilicon resistors trimming [7], metal link cutting [8], Zener zapping [9], floating-gate devices [10], threshold voltage adjustment [11], and thin/thick film laser ablation [12], [13] can be used to enhance DAC differential and integral linearity (DNL and INL). This can also be achieved with dedicated digital or analog calibration circuitry working in background or at power-up [14]–[17]. All explored techniques come at additional costs of increased area, access point, or extra manufacturing layers in the case of film trimming.

In this paper a high-resolution R2R DAC calibrated with a novel laser trimming technique [18] is presented. The DAC is based on laser-diffused resistors which require no additional process steps, is fully compatible with standard CMOS processes and allows for accurate laser trimming of the circuit. Moreover, the DAC can equally be used in an ASSP, as a stand

Manuscript received October 12, 2007; revised January 1, 2008 and January 29, 2008. First published March 7, 2008; current version published September 17, 2008. This work was supported in part by LTRIM Technologies, Laval, QC, Canada. This paper was recommended by Associate Editor T. B. Tarim.

D. Marche and Y. Savaria are with the Department of Electrical Engineering, École Polytechnique de Montréal, Montréal, QC H3T 1J4, Canada (e-mail: david.marche@polymtl.ca).

Y. Gagnon was with LTRIM Technologies Laval, QC, H7V 4B4, Canada. He is now with Intégration Dolphin, Chomedy, QC H7T 1S8, Canada.

Digital Object Identifier 10.1109/TCSI.2008.920152

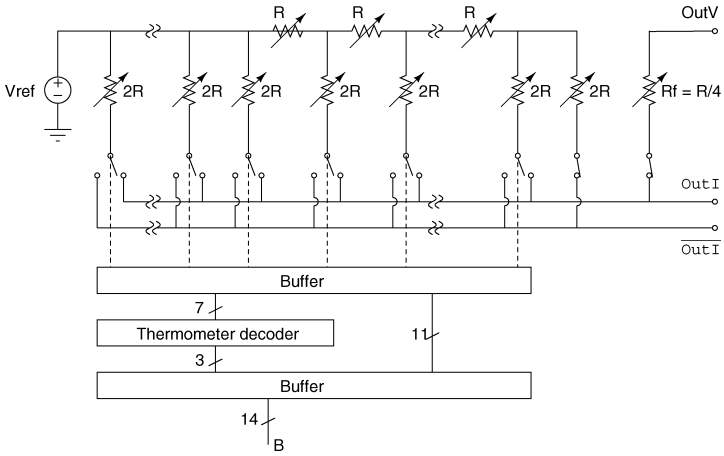

Fig. 1. DAC architecture.

alone chip, or as a precision analog intellectual property (IP) block for SoCs.

A description of the circuit architecture is given in Section II. An overview of matching challenges along with our laser-diffused resistor solution follows in Section III. Chip implementation is described in Section IV with the associated test and calibration procedures detailed in Section V. Finally, experimental results are shown and discussed in Sections VI and VII, respectively.

II. Architecture

Fig. 1 shows the current-mode DAC architecture. The core of the DAC is a current-mode resistor ladder structure generating a set of reference currents from a single voltage reference input. It is entirely based on resistance ratios and a single component value (R) favoring the essential matching needed for the DAC linearity performances. The ladder is segmented to produce 7 equal most significant bit (MSB) currents and 11 binary weighted least significant bit (LSB) currents.

The LSB section is a classic inverted R2R ladder [19], [20]. This current divider network is based on a minimal set of identical components, but requires a matching level closely related to the number of cascaded division stages. For the DNL to be less than 1 LSB, the resistor matching requirement for n stages is given by the following equation ([21]):

$$\frac{\Delta R}{R} = \frac{1}{2^{n-1}}. \tag{1}$$

The 3 MSBs are thermo-encoded over 7 bits. The corresponding 7 equal currents are generated with an unary weighted resistance network. This MSB network extends the DAC resolution, but does not change the matching requirement, which is only dictated by the number of binary encoded bits. Indeed, MSB matching must at least be equal to the LSB network matching, regardless of the number of thermo-encoded bits. It is well known that segmentation of DACs reduces matching requirements, achieves better linearity, ensures monotonicity and reduces glitch energy of MSBs major transitions. From a trimming point of view, thermo-encoding also allows independent calibration of all MSBs: changing a thermo-bit weight has no effect on the current division occurring in the rest of the resistor ladder. The drawback of this segmentation is the relatively important area dedicated to the MSBs and the additional thermo-encoder circuit.

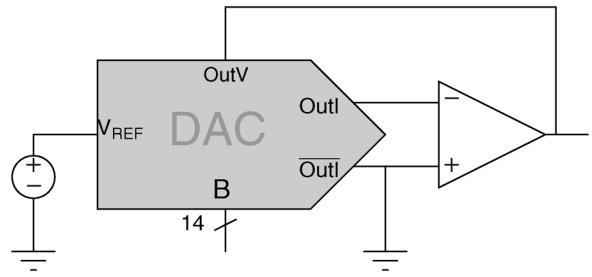

Fig. 2. Voltage output configuration.

Reference currents are steered to one output $(\mathrm{OUT}I)$ or the other $(\overline{\mathrm{OUT}I})$ by means of single-pole-double-throw (SPDT) switches controlled by bit values. Hence, reference currents flowing through the resistor network are only temporarily altered during switching. This current-steering property limits the transient voltage swing across the resistors, which in turns allows for increased operating speed. The output current I_{OUT} or voltage V_{OUT} is the analog converted value that corresponds to the digital input word $[B_0 B_1 \cdots B_{14}]$ and is given by the following expression:

$$I_{\mathrm{OUT}} = \frac{V_{\mathrm{REF}}}{R/4} \sum_{k=1}^{14} B_k * 2^{-k} \tag{2}$$

$$\begin{aligned} V_{\mathrm{OUT}} &= -V_{\mathrm{REF}} \frac{Rf}{R} \sum_{k=1}^{14} B_k * 2^{-k} \\ &= -V_{\mathrm{REF}} \sum_{k=1}^{14} B_k * 2^{-k}. \end{aligned} \tag{3}$$

Voltage output of (3) is obtained using the internal feedback resistor Rf and an external opamp as shown in Fig. 2. The feedback resistor is carefully matched with the others to optimally track the resistor ladder over a wide temperature range. This feedback resistor is the only resistor subject to voltage variation and associated non-linear effects (V_C). Equations (2) and (3) also show the multiplying property of the DAC. Hence, the

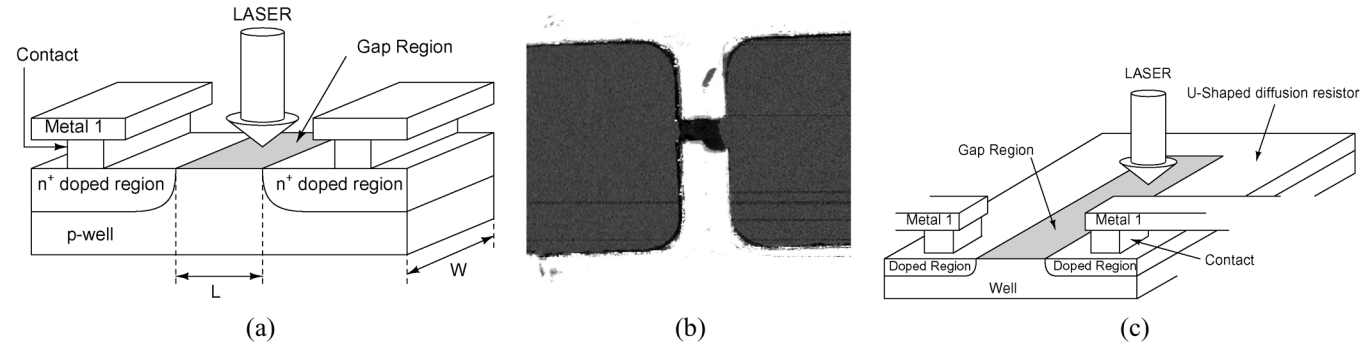

Fig. 3. Trimming technology: (a) cross section of the laser diffusible resistor, (b) scanning capacitance AFM image of a trimmed link, and (c) U-Shaped resistor.

DAC structure allows for digital gain adjustment (or digital attenuation) of the input reference voltage.

Current switches have effects on both the dynamic and static properties [22], [23]. R_{ON} of these switches are compensated in the resistor network as well as in the feedback loop as it impacts on the current division accuracy [24]. A typical compensation technique consisting of halving the switch's R_{ON} at every cascaded division stage was used. Also included in the DAC is an adapted buffer that synchronizes the operation of all SPDT switches. Nonoverlapping control signals [25], [26] are outputted from this buffer and drive the gates of the switches. This driving avoids complete off-mode, preventing current swing in the resistor network and also reducing feedthrough [27]. Although no outstanding dynamic performances optimization was intended, these simple precautions did reduce glitch energy, and improve settling time and dynamic ranges of the DAC. Note that the accuracies of the external voltage reference and optional op-amp must match the accuracy of the DAC itself to take advantage of its full performance.

III. Laser-Diffused Resistors

Resistance values are subject to variations inherent to all manufacturing processes and to several environmental conditions [3]. Process variations affect resistors according to process gradients, border effects and local random variations. Some of the phenomena causing these variations include fluctuation in film thickness, doping concentration and geometric accuracy. Packaging adds stress gradients affecting different parameters including resistivity. During circuit operation, temperature gradients, self-heating and aging inflict added variations in components values. To minimize the effects of these variations, robust designs rely on matched components instead of absolute values. Still, the level of mismatch remaining is unacceptable for some high-performance applications. Flash DAC is such an application strongly dependent on the level of matching reached between a large number of devices. Over 12-bit accuracy, the matching level required typically exceeds todays capabilities when designing with standard CMOS processes.

Post-processing cancellation of the mismatch effects is the most straightforward approach for pushing DAC's performances beyond their intrinsic limits. For this task, laser-trimming has already been widely used on thin and thick-film resistors found in data converter circuits. Unfortunately, this technique requires expensive extra processing steps. Furthermore, the required additional layer prevents the trimmable circuits from being used as analog IPs to be integrated in SoCs.

The DAC presented here stands apart from existing products, as it features standard CMOS resistors that are adjustable with a new laser-trimming technology [18]. This technology is compatible with most existing processes (CMOS, bipolar, SiGe). Resistors can be manufactured without any extra layer or process step and calibration can be done at the wafer level or after packaging when dies to be trimmed are first mounted in open-cavity packages. It finally allows for a single final fine tuning of resistors which may be part of larger SoCs.

The trimming technology, was first used on MOSFET without gates in conventional CMOS processes as illustrated in Fig. 3(a). Two highly doped regions separated by a gap are formed in a well, resulting in two p-n junctions facing each others. Before trimming the device is an open circuit. Focusing a laser beam on the gap region allows melting the silicon, causing dopant diffusion from the highly-doped regions into the gap. This new distribution of dopants creates an electrical link between the two highly-doped regions [Fig. 3(b)]. Tight control of process parameters allows very accurate tuning of the device's resistivity. This same technology can be extended to many different integrated structures to fit the targeted application [28], [29].

The value of a trimming solution is twofold: performance and cost. The results reported in the following sections are mainly related to the performance aspect enabled by the laser-diffused resistors, but it is worth positioning the technology from an economic perspective. The cost associated to trimming must take into account many factors such as laser equipment, clean room, probing time, trimming time, trimming area overhead to list only a few. Nowadays, high resolution trimming is mainly done on thin-film-based circuits, as it seems to be the best cost/performance option available for the precision market segment. Film layers are designed for improved resistor behaviour and feature low temperature and voltage coefficients (TC and VC). However, there is a large cost associated with the deposition of each additional layer in a clean environment. In contrast, laser-diffused resistors are designed within standard diffusion layers fitting the common design flow. Laser-diffused resistors will also scale with process, are typically smaller and easier to match than equivalent film resistors, and their trimming is a clean operation compared to the classic destructive laser film evaporation. Together these considerations make diffused-resistor a cost effective trimming solution.

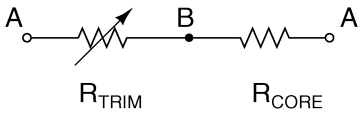

Fig. 4. R2R unit resistor: a polysilicon core ($R_{\rm CORE}$) in series with a trim structure ($R_{\rm TRIM}$).

Packaging is an important aspect to consider and is also closely tied with trimming costs. Trimming is usually done at the wafer level but can require expensive packaging techniques such as low-stress die attach, conformal coating and low-stress molding compound to limit subsequent packaging drifts. In this work, trimming was done after packaging the die samples in open cavity packages. This obviously leads to more complex handling at the trimming step, but it allows a standard packaging solution and fits our testing and trimming needs considering the limited number of prototype samples we had to process as part of this experimental work. An alternate solution consists of trimming dies attached to lead frames, before encapsulation. This compromise allows trimming away some package related stress and, if necessary, the fore mentioned low-stress encapsulation techniques can also be used after trimming. Further work is required to investigate all those possibilities.

IV. Trimming Solution

In our DAC, each resistor is composed of two parts (c.f. Fig. 4):

1) A polysilicon core ($R_{\rm CORE}$) implements 95% of the resistance. This core offers high resistivity combined with low second order distortion effects (voltage and temperature modulation). This is especially important for the feedback resistor which is subject to varying voltage according to the input code and where voltage modulation has direct impact on the DAC voltage output linearity.
2) A trim structure ($R_{\rm TRIM}$) is added in series to the core of each resistance. The trimming structure used is a U-Shaped resistor as shown in Fig. 3(c) where a serpentine segment of diffusion-resistor is laid out, leaving a stretched gap. Initial value of the structure is set by the U-shaped resistor dimensions. If necessary, trimming occurs in the gap region to create a diffused link and reach the desired resistivity. Fig. 5 shows a basic electrical model of a trimmed structure with its laser-diffused link (R_L). Laser focus, spot size, pulse duration and count, power, and positioning accuracy are the main challenges faced for obtaining stable and repeatable trimming results and specific resistance values. When all these parameters are well controlled, trimming is reduced to a simple two dimensional problem where the final trim structure resistance is a function of the link position along the gap and the resistance value of the link (R_L).

Note that keeping the diffusion portion of the composite resistors small ensures that the temperature and voltage tracking of all trimmed and untrimmed composite resistors will be mostly dictated by their polysilicon core. This is preferable because polysilicon resistors have lower TC and VC. For better initial matching, this same structure is used for all resistors, even though many resistors will never need trimming. Care is also taken to ensure that all diffusion resistor diodes are reverse-biased, limiting leakage current to the pico-Amp range. Since our LSB current is in the micro-Amp range, the DAC linearity is not significantly affected by resistor leakage.

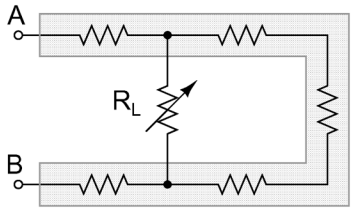

Fig. 5. The trim structure model: initial resistance is set by the U-shaped diffusion resistor and R_L models a laser diffused link presence. Note that the value and position of R_L with respect to the U-shape structure can both be controlled.

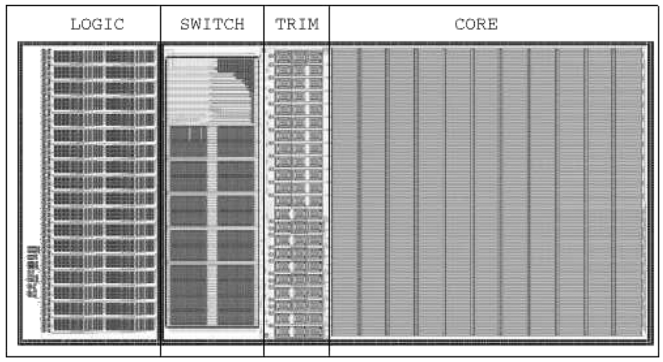

Fig. 6. Layout of the DAC core.

The U-Shaped resistor dimensions are set according to our calibration needs.

- Calibration accuracy is given by the targeted resistor matching level which we set to 0.1 LSB. Although 0.1 LSB of a 14-bit encoded value is 6 ppm, the segmentation used in our resistor ladder relaxes the matching requirement to 48 ppm [c.f. (1)].
- Calibration range is given by the forecasted worst case initial mismatch level. With sufficient layout efforts, one can usually expect a resistor relative mismatch level limited to 0.1%.

Based on these numbers, the final trim structures of our DAC had to allow trimming MSB resistors with at least 48-ppm accuracy over a range greater than 0.1%. In reality however, a security factor was used to ensure trimming capability was sufficient for worst case samples.

V. Implementation

The cell layout image shown in Fig. 6 was implemented as part of a test chip layout targeting the 0.25-μm TSMC CMOS process. Fig. 7 shows a picture of the final chip with the circuit blocks roughly delimited.

The total core area of this DAC is 0.47 mm^2 divided as follows.

- 23% for logic circuitry including thermo-decoder, registers and buffers. Note that accurate dc characteristics were targeted with this prototype and buffers were not individually sized according to their associated switch capacitive loads.

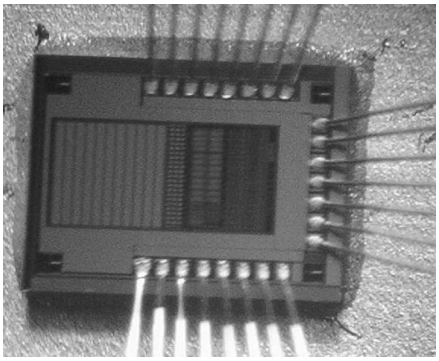

Fig. 7. Image of the DAC chip.

Better buffer sizing would not only enhance dynamic performance but also result in reduced logic area.

- 17% for SPDT switches. Complementary switches are closely matched together to offer the same on-resistance wherever they steer their branch current (OUTI or $\overline{\text{OUT}I}$).
- 60% for resistors. Unit resistance value is around 49 kΩ from which 5% (2.45 kΩ) is given by the trimmable structure initial state. The remaining 95% (46.55 kΩ) is made of large classic polysilicon strips carefully matched with common centroid techniques and edge dummies. As laid out, the trimmable part accounts for 12% of the total resistive area, while delivering only 5% of the total resistance. This area overhead is the cost associated with making this chip trimmable: 4.4% of the DAC area. In other words, the same DAC without trimming capability would be 4.4% smaller.

TABLE I
14-BIT TRIMMABLE DAC SUMMARY OF PERFORMANCES

Process	TSMC 0.25 μm CMOS
Active Area	0.47 mm^2
Supply Voltage	3.3 V
Resolution	14 bits
Initial INL	2 LSB
Initial DNL	0.5 LSB
Calibrated INL	0.7 LSB
Calibrated DNL	0.1 LSB
Settling time	1 μs
Static power diss.	1.7 mW @ $V_{REF} = 3.3V$

TABLE II
MAJOR CARRY TRANSITIONS TRIMMING RESULTS

Major carry #	Encoding type	Initial DNL (LSB)	Final DNL (LSB)
1	Binary	-0.04	-0.04
2	Binary	0.01	0.01
3	Binary	-0.03	-0.03
4	Binary	-0.01	-0.01
5	Binary	-0.02	-0.02
6	Binary	-0.03	-0.03
7	Binary	0.01	0.01
8	Binary	0.03	0.03
9	Binary	-0.05	-0.05
10	**Binary**	**-0.26**	**0.05**
11	**Binary**	**-0.19**	**0.01**
12	**Thermo**	**-0.92**	**-0.04**
13	**Thermo**	**-0.54**	**-0.02**
14	**Thermo**	**1.67**	**-0.03**
15	**Thermo**	**0.49**	**-0.06**
16	**Thermo**	**-0.66**	**-0.03**
17	**Thermo**	**0.20**	**-0.05**
18	**Thermo**	**-0.62**	**0.03**

VI. TEST AND CALIBRATION PROCEDURE

The proposed calibration procedure exploits the notion of *major carrier transitions*. The *major carrier transitions* x is usually defined as the 1-LSB digital input addition which results into the activation of bit x only while deactivating all its less significant bits. Note that the MSB major carrier transition (b011... 1 to b100... 0) occurring at midscale and generally known as the *major-carry transition* is usually documented in DAC product datasheets as it is typically responsible for the largest glitch in binary weighted converters. Major carrier testing is a popular selected-code test method in production frameworks as it allows rapid modeling of a DAC with its bit weight obtained from a reduced set of measurements [30], [31]. However, this method is only valid if superposition errors are low, since the analog output of all untested codes are extrapolated as a linear combination of bit weight values. Here, we have opted for the more accurate all-code testing method as time was less important than accuracy in the framework of this research.

In a perfect DAC, any two consecutive digital input codes always create 1-LSB progression at the output, which translates into a constant 0 DNL error over the entire input range. In reality however, bit weights are not perfectly balanced and DNL errors show up. In this case, major carrier transitions DNL errors give good measures of bit weight (im)balance with a reduced set of measurements. Note that thermo-encoded bits are special cases and we define their major carrier transitions as the transition resulting from a 1-LSB digital input addition which activates one additional thermo-bit while deactivating all binary-encoded bits. Trimming all major carrier transition to 1 $\pm$0.1 LSB was used to calibrate the DAC. Since trimming one DAC stage affects the weight of all more significant bit stages, calibration is done bottom-up, starting from the LSB and finishing with the MSB [20]. This simple straightforward trimming procedure can be summarized as follows:

1) First the offset $(I_{00...0})$ and the full-scale $(I_{11...1})$ outputs are measured. This gives the LSB value.
2) One bit at a time, starting from the LSB, major carrier transitions are measured and corrected if necessary: the current carried by the trimmed bit is adjusted to exactly 1 LSB more than all previous bits contributions added together.

Note that although the LSB value varies during the trimming process, this variation is generally so small that step 1 does not have to be repeated between each trim.

VII. EXPERIMENTAL RESULTS

The laid out DAC was fabricated as a prototype chip and several samples were tested and trimmed using the same calibration procedure. Measured initial accuracy of the DACs was always 12 bits, which shows a good untrimmed linearity. All chips were successfully calibrated to reach their 14-bit targeted resolution within $\pm$0.7-LSB INL and $\pm$0.2-LSB DNL. Chip data summary is given in Table I and typical results are detailed below for a typical sample.

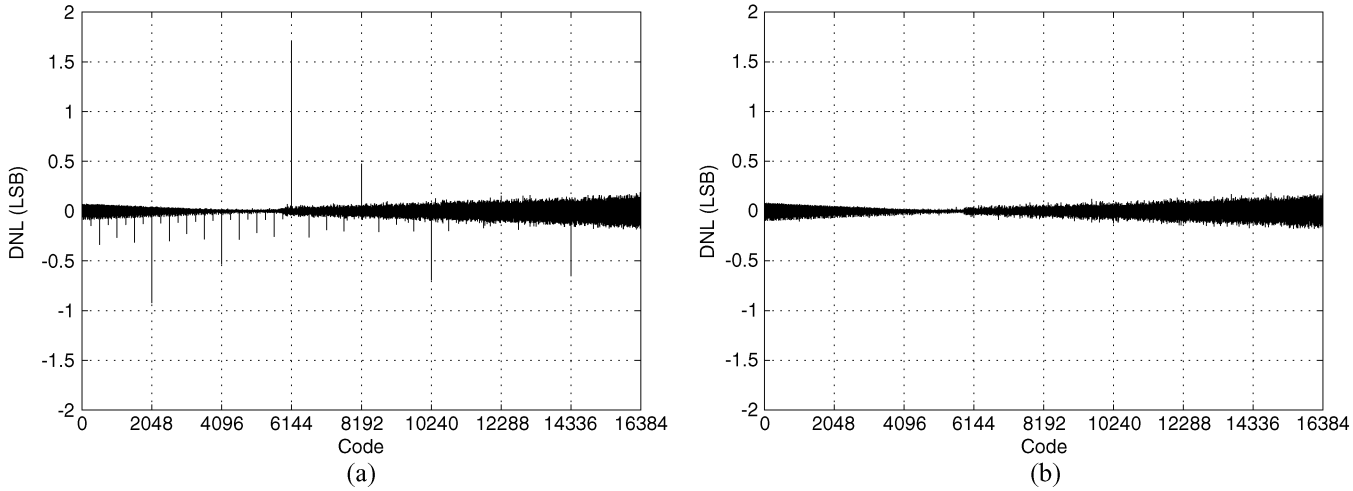

Fig. 8. DNL calibration results: (a) before trimming and (b) after trimming.

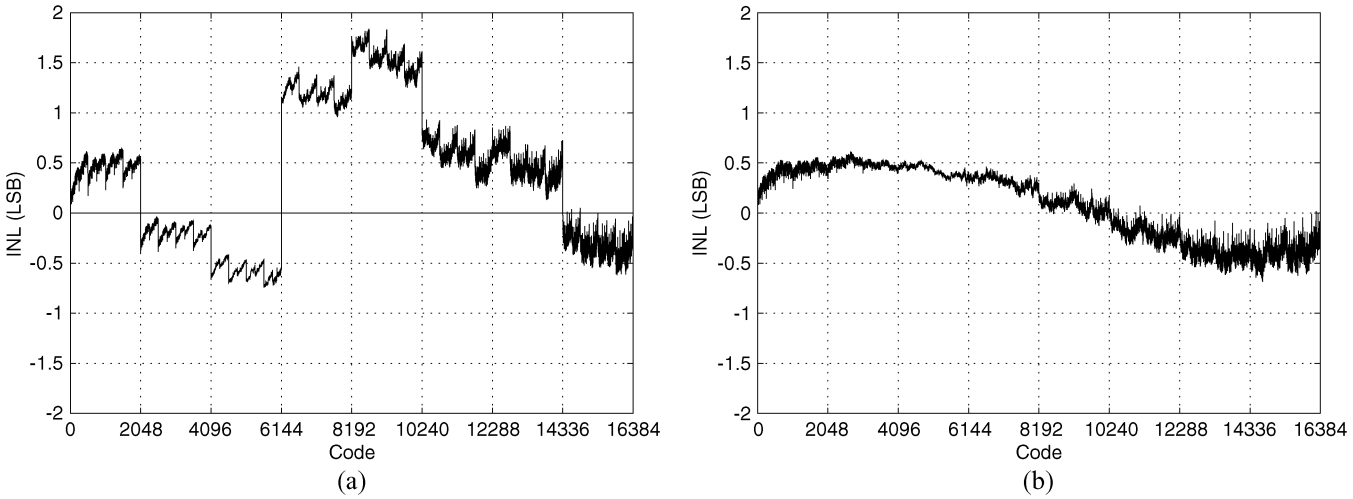

Fig. 9. INL calibration results: (a) before trimming and (b) after trimming.

Table II shows major carry transition DNL errors before and after calibration. All bits showing major carry transition error of more than 0.1 LSB were trimmed (Bit 10 to 18 in this case). Figs. 8 and 9 show the linearity enhancements obtained on the DAC. For this sample, INL has been reduced from 1.92 to 0.68 LSB, DNL has been reduced from 1.67 to 0.18 LSB.

Fig. 10 shows how trimming accuracy is affected by voltage or temperature variations. Results shown here were measured for a thermo-encoded bit which had to be trimmed for an initial 0.77-LSB DNL error. Thermo bit resistor trimming accuracy is a good measure of trimming robustness to VC and TC effects for several reasons:

- Thermo bit DNL errors are the most sensitive to any kind of mismatch.
- Thermo resistors are typically more trimmed than other bits, which brings their diffusion resistor portion smaller than any other bits. This resistor structure difference can cause VC and TC mismatch.
- When input voltage is modified, thermo resistors are the most affected by VC effects because they are directly connected to V_{REF}.

Fig. 10(a) plots DNL error measurements of the calibrated thermo-encoded bit for various reference voltage values. Calibration stays accurate over a wide input voltage range with typical measured DNL drifts in the order of the hundredth of LSB. Note that although designed in a 3.3 V process, 5 V input can be used since the switch devices are only subject to a fraction of this input voltage. This property is sometime used to fabricate high-voltage DAC using low voltage processes. Fig. 10(b) plots the same DNL error measured at various temperatures. Again, calibration tracks well over temperature with measured DNL drifts within 0.05 LSB/100 °C.

Although dynamic performance was not targeted by this work, it is still important to verify that our resistor design will not limit conversion speed. Sample measurements show that our DAC has a typical full-scale swing settling time of around 1 μs and thus reaches the performance of equivalent commercial R2R products such as AD5554 and LTC1591 ([32], [33]).

VIII. Discussion

Many calibration techniques have been used to enhance performances of analog circuits. Typical tradeoffs faced with these

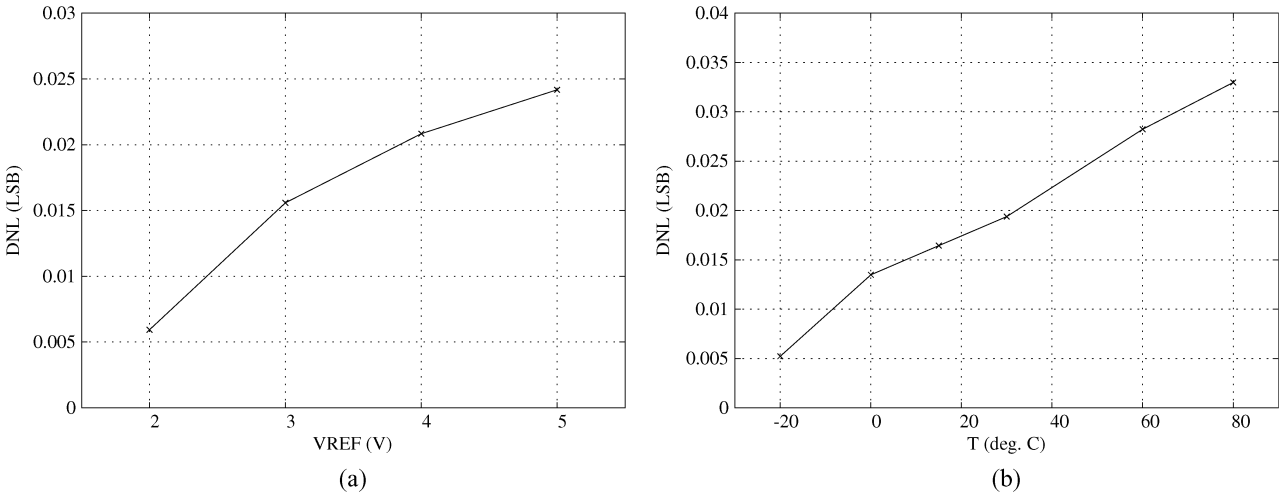

Fig. 10. Typical voltage and temperature variation effects on trimmed precision: a thermo bit DNL error is measured for different input reference voltage (a) and temperature (b) values. This DNL error was originally calibrated at 20 °C with $V_{\mathrm{REF}} = 3.3$ V.

techniques involve area, power consumption, complexity, fabrication steps and trimming operations. How much a particular solution fits the design, increases the performance and costs are the main concerns when integrating calibration structures into a chip.

Our first functional concern with adding diffused resistor trimming in our DAC was that the tuning structures could lead to a high initial mismatch. Although this can be taken into account when defining the calibration range needs, it would result into increased area and additional trimming operations. In our case, all tested chips showed 12-bit untrimmed linearity, which can only be reached if our trimmable resistor ladder has a mismatch level smaller than 0.05% (c.f. (1)). This good initial matching was obtained thanks to the composite structure of the resistor combined with the very small size of our trim structures: the resistor cores which account for most of the resistivity are laid out following standard strict matching rules, while the trim structures are placed close together in a very small area.

Once fabricated and functional, the main calibration issue is the final performance gain. In our case, it is obvious that the targeted accuracy is reached since all samples were trimmed to 14-bit level. However results were not completely satisfactory, because they did not show that the same design could be extended to higher resolution. Fig. 9(b) shows the remaining INL error after trimming. This figure shows the final distortion in the DAC transfer curve that is due to parasitic impedance of on-chip connections. S-shape INL and pinched DNL plots visible in Figs. (9b) and (8b) are typical output profiles of DACs subject to wire resistance distortion [31]. This was also confirmed by simulation when including parasitic elements extracted from the layout. Although acceptable at 14-bit accuracy level, these parasitics limit our final linearity performances with unexpected bit interaction ([37], [38]) and prevent getting the full accuracy reachable with the trimming technology. When going through the entire input code range (0 to 16384), each thermo-encoded bit switches only once and thus has a single associated DNL error which can be trimmed out. On the other hand, each binary

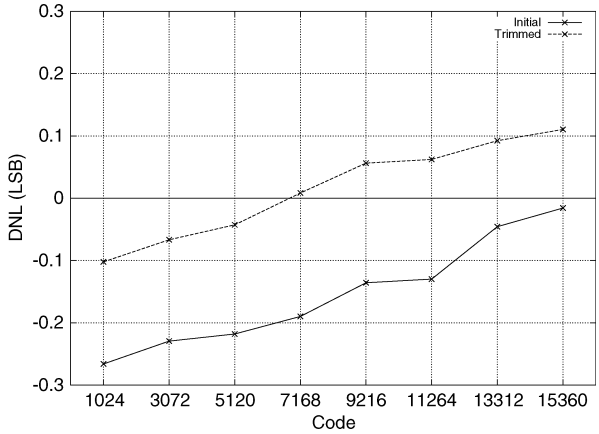

Fig. 11. Measured DNL for bit 10 at major transitions before and after trimming. For readability, the curves in the graph link the measured DNL errors at 8 selected major transitions.

encoded bit produces several transitions across the full input range. For an ideal DAC, all transitions produced by a specific bit are affected by the same DNL error, creating a typical repetitive DNL and INL pattern. In our case, this pattern is modulated by parasitic impedance of on-chip connections. Fig. 11 shows the initial DNL error values measured for the 8 transitions associated with the 10th bit along with the final trimmed values. Trimming cannot completely remove the DNL error for all transitions. However, calibration is used to shift the set of DNL errors so as to minimize the DNL excursions. If perfectly trimmed, the pinch point of our DAC DNL profile should be exactly at midscale. Hence, the trimmed DNL of Fig. 8(b) could be slightly further enhanced if all bit DNLs where shifted so as to be perfectly symmetric around the midscale point (code 8192). However, wire resistance would have to be reduced if this design was extended to higher resolutions.

Trimming, contrary to active calibration circuitry, cannot adapt to the conditions under which the chip is operated. For this reason, it is important that the trimming accuracy be stable

TABLE III
CALIBRATED 14-BIT DAC COMPARISON MATRIX

Chip	Type	INL / DNL (LSB)	Calibration Type	Process (μm^2)	Area (mm^2)	Calibration Area Overhead
Our chip	R2R ladder	0.7 / 0.2	Diffused resistor	0.25	0.47	4.4%
AD5554 [33]	R2R ladder	1 / 1	Thin-fi lm resistor	?	2.5	$> 30\%$
Cong [35]	Current sources	0.43 / 0.34	Caldac	0.13	0.1	$> 50\%$
Tiilikainen [36]	Current sources	0.5 / 0.5	Caldac	0.18	1	50%
Bugeja [37]	Current sources	0.35 / 0.25	Caldac	0.35	11.8	$> 20\%$
Hyde [10]	Current sources	0.35 / 0.25	Floating gate	0.25	0.44	14%

over temperature and voltage variation. This was verified (c.f. Fig. 10) and our trimmed DAC resistors shows good temperature and voltage tracking ensuring small linearity drifts when operating conditions change. Reliability tests on similar resistor structures have also demonstrated that aging does not affect significantly matching of trimmed resistors [29].

The final concern about our trimmable design is how it compares to other available solutions. Data on some commercial products and other published work reaching 14-bit resolution are listed in Table III. Since the table includes R2R and current source converters, the listed circuits obviously feature very different ac performances: current source based circuits run at higher speed and outperform resistor ladders in terms of signal to noise ratios. However, all listed circuits have been designed with a common goal of reaching higher dc performances with the addition of calibration structures. Although it is difficult to establish fair means for comparing all these different circuits, our design shows similar linearity performance with drastically lower calibration area overhead. To our knowledge, it is also the smallest reported monolithic flash DAC featuring 14-bit accuracy.[1]

IX. CONCLUSION

A high-resolution DAC calibrated with a novel laser trimming technique has been presented. The DAC includes laser-diffused resistors to allow post-processing trimming of the dc performances: DNL down to ± 0.18 LSB and INL down to ± 0.7 LSB. The final accuracy is very robust to temperature as well as input reference voltage variations. Trimming would allow reaching even higher accuracy, but our design is limited by the impedance of on-chip parasitic connections. Calibration structures are accountable for 4.4% of the total chip core area (excluding pins). This area overhead is very small compared to other available calibration solutions. Furthermore, the trimming is implemented in a standard CMOS process without any additional layer. Considering the offered accuracy, the low area cost and the process compatibility, our laser-diffused trimmed DAC is a very attractive solution for either IC or IP circuits.

[1]Some reported designs have a smaller size (e.g., [10], [34]), but their accuracy is maintained with periodic or background calibration using significant additional off-chip circuitry.

ACKNOWLEDGMENT

The authors would like to thank M. Ducharme, A. Lacourse and H. St-Jean for the shared expertise in analog design, trimming and test fields. This work exploits several patents assigned to LTRIM Technologies Inc. [40], [41].

REFERENCES

[1] D. D. Buss, "Technology in the internet age," in *Proc. Int. Solid-State Circuits Conf.*, 2002, pp. 18–21.
[2] A. J. Annema, "Analog circuit in ultra-deep-submicron cmos," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 132–143, Jan. 2005.
[3] A. Hasting, *The Art of Analog Layout*. Upper Saddle River, NJ: Prentice-Hall, 2000.
[4] L. Yu and R. Geiger, "Resistors layout for enhancing yield of r-2r dacs," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2002, vol. 5, pp. 97–100.
[5] D.-H. Lee, Y.-H. Lin, and T.-H. Kuo, "Nyquist-rate current-steering digital-to-analog converters with random multiple data-weighted averaging technique and q^n rotated walk switching scheme," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 11, pp. 1264–1268, Nov. 2006.
[6] P. Stubberud and J. W. Bruce, "An analysis of dynamic element matching flash digital-to-analog converters," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 2, pp. 205–213, Feb. 2001.
[7] K. Kato, T. Ono, and Y. Amemiya, "A monolithic 14-bit d/a converter fabricated with a new trimming technique (dot)," *IEEE J. Solid-State Circuits*, vol. SC-19, no. 5, pp. 734–740, Oct. 1984.
[8] J. J. Price, "A passive laser-trimming technique to improve the linearity of a 10-bit D/A converter," *IEEE J. Solid-State Circuits*, vol. SC-11, no. 6, pp. 789–794, Dec. 1976.
[9] D. T. Comer, "A monolithic 12-bit DAC," *IEEE Trans. Circuits Syst.*, vol. CAS-25, no. 7, pp. 504–509, Jul. 1978.
[10] J. Hyde, T. Humes, C. Diorio, M. Thomas, and M. Figueroa, "A floating-gate trimmed, 14-bit, 250 Ms/s digital-to-analog converter in standard0.25- μm CMOS," in *Proc. IEEE Symp. VLSI Circuits*, Honolulu, HI, 2002, vol. 1, pp. 328–331.
[11] A. Biman and D. G. Nairn, "Trimming of current mode DACs by adjusting Vt," in *Proc. IEEE Int. Symp. Circuits Syst.*, Ma 1996, vol. 1, pp. 33–36.
[12] J. R. Naylor, "A complete high-speed voltage output 16-bit monolithic DAC," *IEEE J. Solid-State Circuits*, vol. SC-18, no. 6, pp. 729–735, Dec. 1983.

[13] T. Tobita and H. Takasago, "New trimming technology of a thick film resistor by pulse voltage method," *IEEE Trans. Comput., Hybrids, Manufact. Technol.*, vol. 14, no. 3, pp. 613–617, Sep. 1991.
[14] U.-K. Moon, G. C. Temes, and J. Steensgaard, "Digital techniques for improving the accuracy of data converters," *IEEE Commun. Mag.*, pp. 136–143, Oct. 1999.
[15] J. Pirkkalaniemi, M. Kosunen, M. Waltari, and K. Halonen, "A digital calibration for a 16-bit, 400-Mhz current-steering DAC," in *Proc. IEEE Int. Symp. Circuits Syst.*, Vancouver, Canada, May 2004, vol. 1, pp. 297–299.
[16] I. Galton, "Digital cancelation of D/A converter noise in pipelined A/D converters," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 47, pp. 185–196, Nov. 2000.
[17] K. Parthasarathy, T. Kuyel, Z. Yu, D. Chen, and R. Geiger, "A 16-bit resistor string DAC with full-calibration at final test," in *Proc. IEEE Int. Test Conf.*, 2005, pp. 1–10.
[18] M. Meunier, Y. Gagnon, Y. Savaria, A. Lacourse, and M. Cadotte, "A novel laser trimming technique for microelectronics," *Appl. Surface Sci.*, vol. 186, pp. 52–56, 2002.
[19] L. Wang, Y. Fukatsu, and K. Watanabe, "A CMOS R2R ladder digital-to-analog converter and its characterization," *IEEE Trans. Instrum. Meas.*, vol. 2, no. 5, pp. 1026–1031, May 2001.
[20] M. P. Kennedy, "On the robustness of R2R ladder DACs," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 47, no. 2, pp. 109–116, Feb. 2000.
[21] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*. New York: McGraw-Hill, 1999.
[22] M. Clara, A. Wiesbauer, and W. Klatzer, "Nonlinear distortion in current-steering D/A-converters due to assymetrical switching errors," in *Proc. IEEE Int. Symp. Circuits Syst.*, Vancouver, Canada, May 2004, vol. 1, pp. 285–288.
[23] T. Chen and G. G. E. Gielen, "The analysis and improvement of a current-steering DAC dynamic SFDR-I: The cell-dependent delay differences," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 1, pp. 3–15, Jan. 2006.
[24] D. Marche, Y. Savaria, and Y. Gagnon, "A novel switch compensation technique for inverted R2R ladder DACs," in *Proc. Int. Symp. Circuits Syst.*, May 2005, pp. 386–392.
[25] Y. S. Park, H. C. Hyun, and S. Y. Kwang, "A 3.3 V–110 MHz 10-bit CMOS current-mode DAC," in *IEEE Asia-Pacific Conf. ASIC*, Aug. 2002, vol. 1, pp. 173–176.
[26] B. Hyuen-Hee, Y. Jin-Sik, L. Myung-Jin, S. Eun-Seok, and L. Seung-Hoon, "A 3 V 12b 100 MS/s CMOS D/A converter for high-speed system applications," in *Proc. Int. Symp. Circuits Syst.*, May 2003, vol. 1, pp. 869–872.
[27] X. Weize and E. Friedman, "Clock feedthrough in CMOS analog transmission gate switches," in *Proc. IEEE Int. ASIC/SOC Conf.*, Sep. 2002, pp. 181–185.
[28] S. Rioux, A. Lacourse, Y. Savaria, and M. Meunier, "Design methods for CMOS low-current finely tunable voltage references covering a wide output range," in *Proc. Int. Symp. Circuits Syst.*, May 2005, pp. 4257–4260.
[29] LTRIM Technologies Inc.. Laval, QC, Canada, (Feb. 2007) [Online]. Available: http://www.ltrim.com
[30] M. Burns and G. W. Roberts, *An Introduction to Mixed-Signal IC Test and Measurment*. New York: Oxford University Press, 2000.
[31] L. Wang, Y. Fukatsu, and K. Watanabe, "Characterization of CMOS R2R ladder digital-to-analog converters," *IEEE Trans. Instrum. Meas.*, vol. 50, pp. 1781–1786, Dec. 2001.
[32] AD5554 Precision QUAD 14-Bit D/A Converter Analog Devices. Dallas, TX [Online]. Available: http://www.analog.com
[33] Ltc1591—14-Bit Parallel Low Glitch Multiplying DAC With 4-Quadrant Resistors [Online]. Available: http://www.linear.com Linear Technology Corp.. Milpitas, CA
[34] Y. Cong and T. L. Geiger, "A 1.5–V 14-Bit 100-MS/s Self-calibrated DAC," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2051–2059, Dec. 2003.
[35] M. P. Tiilikainen, "A 14–bit 1.8-V 20-mW 1- mm^2 CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1144–1147, Jul. 2001.
[36] A. R. Bugeja and B.-S. Song, "A self-trimming 14-b 100-MS/s CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 1841–1852, Jul. 2000.
[37] J. R. Naylor, "Testing digital/analog and analog/digital converters," in *Proc. IEEE Int. Symp. Circuits Syst.*, Jul. 1978, vol. 25, pp. 526–538.
[38] P. Prazak and T. Wang, "Superposition: The hidden DAC linearity error," *Electron. Test*, pp. 70–79, Jul. 1982.
[39] Y. Gagnon, M. Meunier, and Y. Savaria, "Method and Apparatus for Iteratively, Selectively Tuning the Impedance of Integrated Semiconductor Devices Using a Focussed Heating Source," U.S. Patent # 09/332,059, Dec. 11, 2001.
[40] A. Lacourse, H. Langlois, Y. Gagnon, and Y. Savaria, "Method for Modifying the Impedance of Semiconductor Devices Using a Focused Heating Source," U.S. Patent # 10/631,825, Mar. 25, 2005.
[41] A. Lacourse, H. Langlois, H. St-Jean, Y. Gagnon, Y. Savaria, and M. Meunier, "A Tunable Semiconductor Component Provided With a Current Barrier," U.S. Patent # 11/431,610, May 11, 2006.

David Marche received the B.Ing. and M.Sc.A degrees in electrical engineering from École Polytechnique de Montréal, Montréal, Canada, in 1993 and 1996, respectively. He is currently working toward the Ph.D. degree on the design of analog and mixed signal integrated circuits at the École Polytechnique de Montréal and teaching at the École de Technologies Supérieure de Montréal.

As a Software Engineer and Analog Designer with OPMAXX, Portland, OR, and later with LTRIM Technologies, Laval, QC, Canada, he has participated in the development of several analog and mixed signal circuit optimisation and test tools. H

Yvon Savaria (S'77–M' 86–SM'97–F'08) received the B.Ing. and M.Sc.A. degrees in electrical engineering from École Polytechnique de Montréal, Montréal, Canada, in 1980 and 1982, respectively, and the Ph.D. degree in electrical engineering in from McGill University, in 1985.

Since 1985, he has been with École Polytechnique de Montréal, where he is currently Professor and Director of the Microelectronics And Microsystems Research Group (www.grm.polymtl.ca). He has carried work in several areas related to microelectronic circuits and microsystems such as testing, verification, validation, clocking methods, defect and fault tolerance, high speed interconnects and circuit design techniques, CAD methods, reconfigurable computing and applications of microelectronics to telecommunications, image processing, video processing, radar signal processing, and digital signal processing acceleration. He holds six patents, has published 71 journal papers and 300 conference papers, and he was the thesis advisor of 115 graduate students who completed their studies.

Dr. Savaria was the Program Co-Chairman of the 1992 edition and the chairman of the 1993 edition of the IEEE Workshop on Defect and Fault Tolerance in VLSI Systems. He was program co-chairman of ASAP2006 and the general co-chair of ASAP2007. He has been working as a consultant or was sponsored for carrying research by CNRC, Design Workshop, DREO, Genesis, Gennum, Hyperchip, LTRIM, Miranda, MiroTech, Nortel, PMC-Sierra, Technocap, and Tundra. He is a member of the Regrouppement Stratégique en Microélectronique du Québec (RESMIQ), of the Ordre des Ingénieurs du Québec (OIQ), and is the vice-chairman of the board of CMC Microsystems. He was awarded in 2001 a Canada Research Chair (www.chairs.qc.ca) on design and architectures of advanced microelectronic systems. He also received in 2006 a Synergy Award of the Natural Sciences and Engineering Research Council of Canada.

Yves Gagnon received the B.Ing. degree from École Polytechnique de Montréal, Montréal, Canada, in 1989.

He was CTO and Founder of LTRIM Technologies, where he managed laser trimming technology and mixed-signal chip development. He is currently working as Executive Director of Intégration Dolphin Inc., the Montréal subsidiary of Dolphin Integration SA France, where he manages power management IP development.