CMOS090_LP

Design Rule Manual

90 nm Low Power Bulk CMOS Process

Revision 1.0

JSC Mikron

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TITLE: CMOS090_LP DESIGN RULES MANUAL FOR TRANSFER

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1. PURPOSE

To provide all the rules and reference information regarding the design and layout of integrated circuits using the CMOS090_LP bulk CMOS technology and its specific options.

2. SCOPE

This specification is intended for use by all internal and external product groups as a common design rule manual for CMOS090_LP. All requirements stated in this document must be followed as applicable for the covered rules and process.

3. REFERENCE DOCUMENTS

- N/A

4. DEFINITIONS

4.1 STANDARD DEFINITIONS

For definitions for layout design rules elaboration see §7.3.1 and §7.3.2. For definitions for reliability design rule elaboration see §7.5.2.1, §7.5.2.2, and §7.6.2.1.

4.2 ADDITIONAL DEFINITIONS

- Chip size: defined with respect to the most external layer of the seal ring. See also §7.2.4.
- Die size: the pitch of the scribe street (distance between the median lines of two adjacent scribing streets).

5. GENERAL

- N/A

6. SAFETY REQUIREMENTS

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- transmission
- disposal
- safekeeping and storage

MUST all follow the rules defined in the companies standard operation procedures.

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7. PROCEDURE

7.1 GENERAL CMOS090_LP TECHNOLOGY

7.1.1 STANDARD PROCESS

CMOS090_LP: Targeted as Low Power to serve battery operated and wireless applications. It is a Dual Gate Oxide dual Vt process that gives access to standard Vt transistors (SVT), high Vt transistors (HVT), high density SRAM as well as thick oxide IO transistors (2.5V). It uses Copper metallization with 7 metal levels (5 thin + 2 thick) and low-K dielectrics.

7.1.2 TECHNOLOGY OPTIONS

The following add-on options are available:

- CMOS090_LP-A (Analog): CMOS090_LP + HIPO resistor option.
- CMOS090_LP-R (RF): CMOS090_LP + MIM Capacitor + Inductor option.
- CMOS090_LP-B (Flip-Chip Bump): CMOS090_LP + Flip-Chip Bump packaging option.

7.1.3 KEY TECHNOLOGY FEATURES

Power supply:

- This process is designed for 1.2V +/- 10% applications with 2.5V capable IO's. See also §7.6.3.1 for more details on the power supply.

Front-End main features:

- Shallow trench isolation, isolated P-Well (DNW) twin-tub, single poly CMOS process using a type (100) P-substrate in a <110> orientation.
- 21A gate oxide, cobalt silicide on junctions and polysilicon gates and lines, and resistors on active and inter-connect N+ or P+ poly.
- Dual Vt 1.2V transistors
- IOs using 5.0 nm gate oxide for 2.5V.

Back-End main features:

- Back-End with 7 metal levels.
- Damascene Copper for metal 1 to last metal.
- Thick metal layer for power, clock, busses and major interconnect signal distribution, as well as for Inductors in Analog/RF applications.
- Tight pitch levels for routing on thin copper for the other metal levels underneath.
- Low K (<3.0) inter-metal dielectrics for thin metal layers

7.1.4 PROCESS FLOW

7.1.4.1 Key features

- SHALLOW TRENCH ISOLATION (STI): used for active isolation to reduce active pitch (OD pitch).
- RETROGRADE TWIN WELLS allow getting a low well sheet resistance and enhancement of latch-up behavior compared to conventionally diffused wells, and a very good control of short parasitic field transistors.
- TRIPLE WELL (Deep N-WELL) allows isolating PWELL from the substrate.
- DUAL Gate Oxide for IO compatibility.
- N+/P+ POLY GATE. This technology allows symmetrical design of N-Channel and P-Channel devices.
- Self-aligned SILICIDED DRAIN, SOURCE AND GATE: silicide is necessary to short N+ and P+ gates; furthermore, it drastically reduces gate and S/D series resistance. Self-aligned Silicide on Source/Drain allows butting straps with only one minimum contact.
- POLY AND ACTIVE RESISTORS: Silicide protection is used to prevent silicide formation over active areas, for ESD protection. This process is also used to fabricate poly resistors.
- CHEMICAL MECHANICAL POLISHING for enhanced planarization (on STI, Contacts, Metals and vias).
- Dual Damascene COPPER interconnects.

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7.1.4.2 Simplified process flow

The below table summarizes the key process steps for the standard process including process options indicated in *italic*.

PROCESS STEP	PATTERN STEP - MASK
1. Active Areas (CAD layer OD) • Oxide, Nitride stack deposition (hard mask) • Active areas PATTERN and trench etching • Trench oxidation and oxide filling • Chemical Mechanical Planarization (CMP) • Hard mask removal • Sacrificial oxidation	1. ACTIVE
2. Deep NWELL - (CAD layer DNW) • NISO PATTERN • Deep N-Well implant	2. NISO
3. NWELL & NWELLGO2 (derived from CAD layer NW and OD2) • NWELL PATTERN • Retrograde NWELL + anti punch through implants • PMOS standard Vt implant • ADHVTP PATTERN (CAD layers VTH_P) • PMOS High Vt implant • NWELLGO2 PATTERN and implant • PMOSGO2 Vt Implant	3. NWELL 4. ADHVTP *5. NWELLGO2*
4. PWELL & PWELLGO2 (derived from CAD layer NW and OD2) • PWELL PATTERN • Retrograde PWELL + anti punch through implants • NMOS standard Vt implant • ADHVTN PATTERN (CAD layers VTH_N) • NMOS High Vt implant • PWELLGO2 PATTERN and implant • NMOSGO2 Vt Implant	6. PWELL 7. ADHVTN *8. PWELLGO2*
5. VT of NMOS SRAM transistors (derived from CAD layer SRM and NW) • VTNCELL PATTERN • SRAM NMOS Vt implant	9. VTNCELL
6. Thick gate oxide (CAD layers OD25) • Strip sacrificial oxide • Gate oxidation for GO2 • GO2 PATTERN and oxide etch	*10. GO2*
7. GATE Poly (CAD layer PO) • Gate oxidation GO1 • Poly deposition • Poly predoping PATTERN and implant • Poly PATTERN • Poly reoxidation	11. NPLUS 12. POLY
8. LDD • NLDDGO2 PATTERN and implant • PLDDGO2 PATTERN and implant • NLDD PATTERN (all core transistors) and implant • PLDD PATTERN (all core transistors) and implant	*13. NLDDGO2* *14. PLDDGO2* 15. NLDD 16. PLDD
9. Spacers • Sidewall (oxide + nitride) deposition • Sidewall (nitride + oxide) etch	

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PROCESS STEP	PATTERN STEP - MASK
10. Source/Drains (CAD layers NP, PP) • NPLUS PATTERN (including GO2) • N+ S/D implant • PPLUS PATTERN • P+ S/D implant • PPLUSGO2 PATTERN and implantS/D Rapid Thermal Annealing	17. NPLUS 18. PPLUS *19. PPLUSGO2*
11. High resistance Poly resistor - Optional (CAD layer HRI) • *PRESIST PATTERN* • *HIPO implant*	*20. PRESIST*
12. Silicide protection (CAD layer RPO) • TEOS + nitride deposition • SIPROT PATTERN	21. SIPROT
13. Silicide formation • Cobalt deposition • Cobalt silicide formation • Cobalt removal	
14. Inter level dielectric • Nitride deposition • Oxide deposition • CMP planarization	
15. Contact (CAD layer CO) • Contact PATTERN • Contact vertical etch • Tungsten plugs deposition and CMP	22. CONTACT
16. Metal 1 (CAD layer M1) • Nitride deposition • Low K Dielectric deposition • Metal PATTERN (single damascene) • Dielectric etch • Barrier + Copper deposition & anneal • Cu CMP (+ Barrier)	23. METAL1
17. Via1 + Metal 2 (CAD layers VIA1, M2) • Etch stop deposition • Low K Dielectric deposition • Hard mask deposition • Metal 2 PATTERN and hard mask etch • VIA1 PATTERN • Via etch • Via resist plug formation • Trench etch (metal pattern defined by hard mask) • Barrier + Copper deposition • Cu CMP (+ Barrier)	24. METAL2 25. VIA1
18. Via 2 + Metal 3 (CAD layers VIA2, M3) • Idem 17	26. METAL3 27. VIA2
19. Via 3 + Metal 4 (CAD layers VIA3, M4) • Idem 17	28. METAL4 29. VIA3
20. Via 4 + Metal 5 (CAD layers VIA4, M5) • Idem 17	30. METAL5 31. VIA4

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PROCESS STEP	PATTERN STEP - MASK
21. TOP-1 large via and thick metalEtch stop deposition • *Dielectric deposition* • *VIATOP_1 PATTERN* • *Via etch* • *METALTOP_1 PATTERN* • *Metal etch* • *Barrier + Copper deposition* • *Cu CMP (+ Barrier)*	32. VIATOP_1 33. METALTOP_1
22. TOP large via and thick metal • Idem 21	34. VIATOP 35. METALTOP
23. MIM Capacitor: • *Nitride + Oxide deposition* • *Aluminum mim bottom plate deposition* • *Dielectric deposition* • *Aluminum mim top plate deposition* • *MKTOPMIM PATTERN and etch (top plate)* • *Nitride deposition* • *BOTMIM PATTERN and etch (bottom plate and nitride)*	*36. MKTOPMIM* *37. BOTMIM*
24. Encapsulation + Pads + Nitride Passivation (CAD layers CB, AP, NITRIDE) • Encapsulation deposition + anneal • PADOPEN PATTERN (define opening for pad in encapsulation) • Al cap deposition • ALUCAP PATTERN (includes CAD layer AP) • Passivation deposition • Nitride PATTERN (passivation opening)	38. PADOPEN 39. ALUCAP 40. NITRIDE

7.1.4.3 Mask Count and Patterning Steps

For details about mask usage for the different process features see §7.2.5.

Standard Process	Std. mask count	Std. pattern steps
Dual Vt, Dual Gate Oxide, 7 Metal Layers	36	37

Option	Process Option	Mask count	Pattern steps
	MIM	+ 2	+ 2
	Single Vt (no HVT transistors)	- 2	- 2
	Single Gate Oxide (no 2.5V IO)	- 6	- 6
-A-	HIPO	+ 1	+ 1

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7.1.5 BASIC DEVICES AVAILABLE FOR CIRCUIT DESIGN AND MAIN FEATURES

Devices other than specified in this section are not authorized for design. Depending on the level of support we define the following categories of devices:

Device Category Definitions	Fully Supported	Specific Application	Process Option	Naturally Available
Part of common platform	YES	YES	YES	YES
Characterization + Spice Modeling	General	Application specific	General	NO
Spice alignment	Full alignment	Full alignment	Full alignment	Target only
Available in Design Kit	YES	YES	YES	NO

Thin Oxide MOSFETs						
Device	**Name in DK**	**Fully Supported**	**Specific Applic.**	**Process Option**	**Natural**	**Comment**
LP Thin Oxide MOSFETs						
LP NMOS 21A 1.2V, SVT	nsvt	x				1.4V overdrive see §7.6.3
LP PMOS 21A 1.2V, SVT	psvt	x				1.4V overdrive see §7.6.3
LP NMOS 21A 1.2V, HVT	nhvt	x				1.4V overdrive see §7.6.3
LP PMOS 21A 1.2V, HVT	phvt	x				1.4V overdrive see §7.6.3
LP NMOS 21A 1.2V, SVT unsilicided	nsvtrpo		x			1.4V overdrive see §7.6.3; IO application; model same as silicided device + series resistance
LP PMOS 21A 1.2V, SVT unsilicided	psvtrpo		x			1.4V overdrive see §7.6.3; IO application; model same as silicided device + series resistance
LP NMOS 21A 1.2V, HVT unsilicided	nhvtrpo		x			1.4V overdrive see §7.6.3; IO application; model same as silicided device + series resistance
LP PMOS 21A 1.2V, HVT unsilicided	phvtrpo		x			1.4V overdrive see §7.6.3; IO application; model same as silicided device + series resistance
LP SRAM Bitcell MOSFETs						
MOSFET (cell sizes)						Models for LP SRAM transistors are the same for all cell sizes
LP NMOS 1.2V, HVT + cell (1.15)	nhvtpgsp, nhvtpgdp, nhvtpdsp, nhvtpddp		x			1.4V overdrive see §7.6.3
LP PMOS 1.2V, HVT (1.15)	phvtpusp, phvtpudp		x			1.4V overdrive see §7.6.3

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Thick Oxide MOSFETs						
Device	**Name in DK**	**Fully Supported**	**Specific Applic.**	**Process Option**	**Natural**	**Comment**
2.5V MOSFETs						
OD25 NMOS 50A 2.5V, SVT	nsvt25	x				Overdrive see §7.6.3.
OD25 PMOS 50A 2.5V, SVT	psvt25	x				Overdrive see §7.6.3.
OD25 NMOS 50A 2.5V, SVT unsilicided	nsvt25rpo		x			Overdrive see §7.6.3; IO application; model same as silicided device + series resistance
OD25 PMOS 50A 2.5V, SVT unsilicided	psvt25rpo		x			Overdrive see §7.6.3; IO application; model same as silicided device + series resistance
OD25 NMOS-no-LDD 50A	nsvt25rponoldd		x			IO application: ESD clamp

DIODES						
Device	**Name in DK**	**Fully Supported**	**Specific Applic.**	**Process Option**	**Natural**	**Comment**
LP - Thin Oxide Wells						
N+ / PWELL: LP SVT	dnsvt	x				
P+ / NWELL: LP SVT	dpsvt	x				
N+ / PWELL: LP HVT	dnhvt	x				
P+ / NWELL: LP HVT	dphvt	x				
NWELL / Psubstr.	dnwps	x				Diode NWELL/PWELL is lateral part of NWELL/ Psubstr.
PWELL / Deep NWELL	ddnwpw	x				
Deep NWELL / Psubstr.	ddnwps	x				
2.5V - Thick Oxide Wells						
N+ / PWELL: 50A SVT	dnsvt25	x				
P+ / NWELL: 50A SVT	dpsvt25	x				
N+ / PWELL 50A gated diode	dgnsvt25		x			IO application: gated diode
P+ / NWELL 50A gated diode	dgpsvt25		x			IO application: gated diode

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BIPOLARS						
Device	**Name in DK**	**Fully Supported**	**Specific Applic.**	**Process Option**	**Natural**	**Comment**
LP - Thin Oxide Wells						
N+ / PWell / Deep NWELL	npniso4, npniso25		x			Bandgap reference; fixed geometry emitter 2x2 um^2 or 5x5 um^2
P+ / NWell / Psubstr.	pnps4, pnps25		x			Bandgap reference; fixed geometry emitter 2x2 um^2 or 5x5 um^2
PWELL / Deep NWELL / Psubstr.					x	

RESISTORS						
Device	**Name in DK**	**Fully Supported**	**Specific Applic.**	**Process Option**	**Natural**	**Comment**
General						
N+ Poly silicided	rnpo	x				
P+ OD non-silicided	rpodrpo	x				
N+ OD non-silicided	rnodrpo	x				
P+ Poly non-silicided	rpporpo	x				
N+ Poly non-silicided	rnporpo	x				
NWELL in OD, no DNW	rnwod				x	
P+ Poly silicided					x	
N+ OD silicided					x	
P+ OD silicided					x	
NWELL under STI, no DNW					x	
PWELL under STI, with DNW					x	
DNW					x	
High-Resistance P+ Poly (HIPO)	rhiporpo			x		
Metal Resistors	rm1, rm2, rm3, rm4, rm5, rm6, rm7	x				
AP resistor	rap	x				
Interconnection N+ Poly line	rnpoi				x	Limited support model
Interconnection P+ Poly line	rppoi				x	Limited support model

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CAPACITORS						
Device	**Name in DK**	**Fully Supported**	**Specific Applic.**	**Process Option**	**Natural**	**Comment**
LP - Thin Oxide						
N+ Poly / 21A Gox / NWELL	cponw	x				
P+ Poly / 21A Gox / PWELL	cpopw	x				
2.5V - Thick Oxide						
N+ Poly / 50A Gox / NWELL	cpo25nw	x				
P+ Poly / 50A Gox / PWELL	cpo25pw	x				
Backend Capacitors						
Metal fringe capacitor M1-M5	cfrm1m5	x				Fixed finger geometry P-cell
Metal plate capacitors	cmsbe, cm1m2, cm2m3, cm3m4, cm4m5, cm5m6, cm6m7	x				
MIM Capacitor	cmimmk			x		High linearity capacitor

RF Devices						
Device	**Name in DK**	**Fully Supported**	**Specific Applic.**	**Process Option**	**Natural**	**Comment**
NMOS Standard Vt LP (1V2)	nsvtrf	x				
PMOS Standard Vt LP (1V2)	psvtrf	x				
NMOS GO2 2V5	nsvt25rf	x				
PMOS GO2 2V5	psvt25rf	x				
Symmetrical Inductor	ind_sym_nw	x				
Differential inductor	ind_dif_nw	x				
Varactor NMOS GO2 2V5	var_sg_nmos25	x				
Varactor PMOS GO2 2V5	var_sg_pmos25	x				

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7.2 MASK GENERATION

7.2.1 MASK TYPE

- Deep UV

7.2.2 CAD LAYER DEFINITION

The following tables lists the layer numbers as they must be used in the GDS database sent to the fab. Unless otherwise indicated, all drawn layers use GDS datatype 0.

CAD Levels		
Name	**Number**	**Description**
OD	6	Defines Active Area
DNW	1	Drawn to obtain PWELL or PWELLGO2 isolated from the substrate: isolated (PWELL or PWELLGO2) is obtained with (PWELL or PWELLGO2) + DNW implant surrounded by a NWELL guard ring.
NW	3	Defines NWELL
VTH_N	67	Drawn to fix the threshold voltage of high Vt NMOS transistors
VTH_P	68	Drawn to fix the threshold voltage of high Vt PMOS transistors
SRM	50	A SRM layer should cover the SRAM cell array in order to generate the VTNCELL mask. The SRM edge should be aligned to the boundary of cell array that may include storage, strapping, and dummy edge cells. (see §7.3.8.6 for related design rules)
OD25	41	Defines 2.5 V capable IO's MOS transistors with thick gate oxide (alias OD_25)
PO	17	Defines Poly-Silicon
NP	26	Defines N-type Source/Drain implant
PP	25	Defines P-type Source/Drain implant
HRI	70	Defines HIPO resistor implant
RPO	29	Defines Silicide Protection
CO	30	Defines connection between Poly/Active and Metal1
M1	31	Defines 1st metal level for interconnect
VIA1	51	Defines connection between Metal1 and Metal2
M2	32	Defines 2nd metal level for interconnect
VIA2	52	Defines connection between Metal2 and Metal3
M3	33	Defines 3rd metal level for interconnect
VIA3	53	Defines connection between Metal3 and Metal4
M4	34	Defines 4th metal level for interconnect
VIA4	54	Defines connection between Metal4 and Metal5
M5	35	Defines 5th metal level for interconnect
VIA5	55	Defines connection between Metal5 and Metal6
M6	36	Defines 6th metal level for interconnect
VIA6	56	Defines connection between Metal6 and Metal7
M7	37	Defines 7th metal level for interconnect
CB	43	Defines Copper Bondpad (wirebond pad connecting to top metal)
CB;via	43;33	Defines connection between Mtop and Alucap (not required for standard pads)
AP	42	Defines aluminum cap (not required for standard pads)
NITRIDE	231	Defines Nitride passivation opening on top of aluminum cap (not required for standard pads)
NITRIDE;bump	231;35	Defines Nitride passivation opening on top of aluminum cap for flip-chip

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CAD Levels (continued)		
Name	**Number**	**Description**
MKTOPMIM	77	Defines top plate for MIM capacitor above top metal level
BOTMIM	88	Defines bottom plate for MIM capacitor above top metal level
MKR;bjtdmy	110	Marker layer to cover the vertical bipolar transistors (NPN and PNP) (alias MKR;BJT, BJTDMY)
MKR;rhdmy	117	Layer to cover active and poly resistors to block LDD implant (alias RH)
MKR;inddmy	144	Marker layer covering the complete inductor (alias INDDMY)
MKR;logo	158	Marker layer to cover logos and product labels (alias LOGO)
MKR;sealring	162	Marker layer to cover seal ring for DRC (alias SEALRING)
MKR;sramdmy	186;0	Marker layer for 3rd party SRAM
MKR;7M2T	218;73	Marker layer to identify metallization 7M2T
MKR;GATED	218;111	Marker layer to identify gated diodes
MKR;wb	218;119	Marker layer to identify wirebond region
MKR;tp	218;121	Marker layer to identify test point region
PW;blk	222;20	Defines area that receives neither NWELL nor PWELL implants (special applications only).
N1V;blk	225;20	Defines area that does not receive NLDD nor NLDDGO2 implants (special applications only)
N2V;blk	227;20	Defines area that does not receive NLDDGO2 implant (obsolete, use N1V;blk instead)

Dummy Pattern CAD Levels		Dummy_O Pattern CAD Levels	
Name	**Number;datatype**	**Name**	**Number;datatype**
OD;dummy	6;1		
PO;dummy	17;1		
M1;dummy	31;1	M1;dummy_O	31;7
M2;dummy	32;1	M2;dummy_O	32;7
M3;dummy	33;1	M3;dummy_O	33;7
M4;dummy	34;1	M4;dummy_O	34;7
M5;dummy	35;1	M5;dummy_O	35;7
M6;dummy	36;1		
M7;dummy	37;1		
AP;dummy	42;1		
BOTMIM;dummy	88;1		
MKTOPMIM;dummy	77;1		

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Table of key devices with associated CAD Layers

Transistors						
CAD level Name	NMOS			PMOS		
	SVT	HVT	SVT25	SVT	HVT	SVT25
OD	x	x	x	x	x	x
PO	x	x	x	x	x	x
NW				x	x	x
VTH_N		x				
VTH_P					x	
NP	x	x	x			
PP				x	x	x
OD25			x			x

Resistors									
CAD Level Name	Unsilicided					Silicided			
	N+ PO	P+ PO	N+ OD	P+ OD	HIPO	N+ PO	P+ PO	N+ OD	P+ OD
OD			x	x				x	x
PO	x	x				x	x		
NW	x	x		x	x	x	x		x
NP	x		x			x		x	
PP		x		x	x		x		x
RPO	x	x	x	x	x				
RH	x	x	x	x		x	x	x	x
HRI					x				

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7.2.3 MASK TABLE

The masks are generated with logical operations done on CAD layers. These logical operations (N/A) are performed during the data preparation for mask processing. Below, “Associated CAD Name” refers to the level in the Common Technology Kit on which the corresponding inactive mask patterns are placed.

Mask Levels			
Mask Level Name	**Mask Number [a]**	**Field**	**Associated CAD Name**
ACTIVE	2	Clear	OD
NISO	24	Dark	DNW
NWELL	1	Dark	NW
ADHVTP	83	Dark	VTH_P
NWELLGO2	84	Dark	NW2V
PWELL	8	Clear	PW
ADHVTN	82	Dark	VTH_N
PWELLGO2	85	Dark	PW2V
VTNCELL	94	Dark	VTNCELL
GO2	6	Clear	OD25
POLY	13	Clear	PO
NLDDGO2	76	Dark	N2V
PLDDGO2	77	Dark	P2V
NLDD	14	Dark	N1V
PLDD	15	Dark	P1V
NPLUS	16	Dark	NP
PPLUS	17	Dark	PP
PPLUSGO2	26	Dark	PP2V
PRESIST	42	Dark	HRI
SIPROT	18	Clear	RPO
CONTACT	19	Dark	CO
METAL1	23	Dark	M1
VIA1	25	Dark	VIA1
METAL2	27	Dark	M2
VIA2	32	Dark	VIA2
METAL3	34	Dark	M3
VIA3	35	Dark	VIA3
METAL4	36	Dark	M4
VIA4	52	Dark	VIA4
METAL5	53	Dark	M5
VIATOP_1	130	Dark	VIA5
METALTOP_1	131	Dark	M6
VIATOP	132	Dark	VIA6
METALTOP	133	Dark	M7
PADOPEN	40	Dark	CB
ALUCAP	41	Clear	AP
NITRIDE	31	Dark	

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Mask Levels (Continued)			
Mask Level Name	**Mask Number [a]**	**Field**	**Associated CAD Name**
BOTMIM	96	Clear	BOTMIM
MKTOPMIM	81	Clear	MKTOPMIM

a.Mask number is NOT the same as GDS stream number.

7.2.4 CHIP DIMENSIONS CONSTRAINTS

Maximum size is Fab dependent.

Length and width of the die (X and Y axis) must be a multiple of 2 microns including the seal ring (see §7.4.6).

7.2.5 PROCESS FEATURE MATRIX

	Process Feature	Opt	Devices	CAD Layers	Masks
Standard Process	Minimum Process		nsvt, psvt, nsvtrpo, psvtrpo, dnsvt, dpsvt, dnwps, pnps4, pnps25, rnpo, rnpoi, rppoi, rpo-drpo, rnodrpo, rpporpo, rnporpo, rm1, rm2, rm3, rm4, rm5, rm6, rm7, rap, cponw, cpopw, cfrm1m5, cmsbe, cm1m2, cm2m3, cm3m4, cm4m5, cm5m6, cm6m7	OD, NW, PO, NP, PP, RPO, RH, CO, M1, VIA1, M2, VIA2, M3, VIA3, M4, VIA4, M5, VIA5, M6, VIA6, M7, CB, AP, NITRIDE, MKR;7M2T	ACTIVE, NWELL, PWELL, POLY, NLDD, PLDD, NPLUS, PPLUS, SIPROT, CONTACT, METAL1, VIA1, METAL2, VIA2, METAL3, VIA3, METAL4, VIA4, METAL5, VIATOP_1, MTOP_1, VIATOP, METALTOP, PADOPEN, ALU-CAP, NITRIDE
	Deep NWELL		ddnwpw, ddnwps, npniso4, npniso25	DNW	NISO
	High Vt		nhvt, phvt, nhvtrpo, phvtrpo, dnhvt, dphvt	VTH_N, VTH_P	ADHVTP, ADHVTN
	2.5V I/O		nsvt25, psvt25, nsvt25rpo, psvt25rpo, dnsvt25, dpsvt25, cpo25nw, cpo25pw	OD25	GO2, NWELLGO2, PWELLGO2, NLDDGO2, PLDDGO2, PPLUSGO2
	+ no-ldd		nsvt25rponoldd	N1V;blk	
	+ gated-diodes		dgnsvt25, dgpsvt25	MKR;GATED	
	High Density SRAM		nhvtpgsp, nhvtpgdp, nhvtpdsp, nhvtpddp, phvtpusp, phvtpudp	SRM	VTNCELL
Process Options	HIPO	-A-	rhiporpo	HRI	PRESIST
	MIM	-R-	cmimmk	MKTOPMIM, BOTMIM	MKTOPMIM, BOTMIM
	Flip-Chip	-B-		NITRIDE;bump	-

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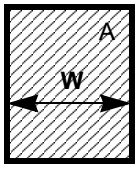
7.3 LAYOUT DESIGN RULES

7.3.1 DESIGN RULE LABEL AND GEOMETRY TERMINOLOGY

Note: Boolean (logical) operations realized on layers are indicated in the rule descriptions by brackets, as {A or B}

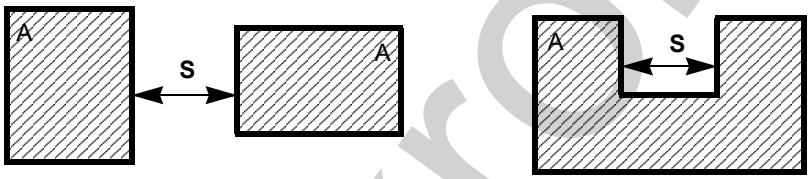
WIDTH: Width of a single layer A

Rule label: layer.**W**.n



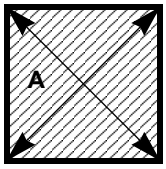
SPACE: Space between external boundaries of the same layer.

Rule label: layer.**S**.n



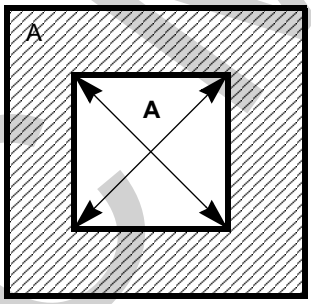
AREA: Geometrical area of a polygon.

Rule label: layer.**A**.n



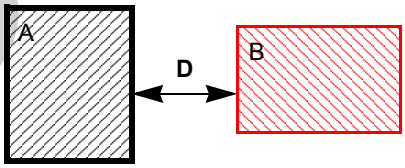
ENCLOSED AREA: Geometrical area of hole in a polygon.

Rule label: layer.**A**.n



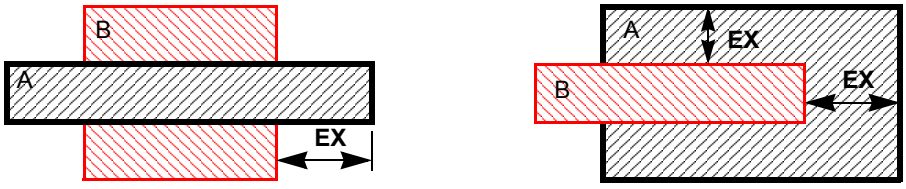
A DISTANCE TO B: Distance between boundaries of two polygons of different layers (A and B)

Rule label: layer.**D**.n



A EXTENSION ON B: Distance between internal boundary of A and external boundary of B.

Rule label: layer.**EX**.n



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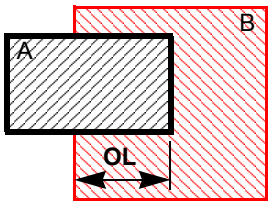
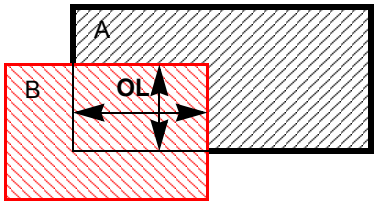
A OVERLAP OF B: Distance between internal boundary of A and internal boundary of B.

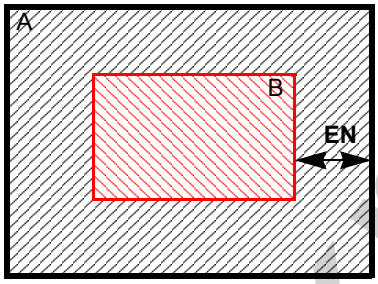
Rule label: layer.**OL**.n





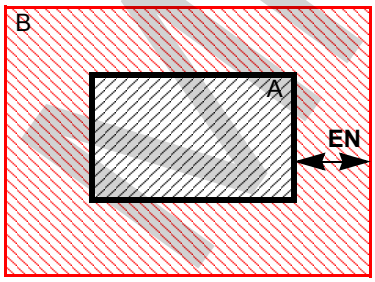
A ENCLOSURE OF B: Distance between the internal boundary of A and the external boundary of B, where B is completely included in A.

Rule label: layer.**EN**.n



A ENCLOSURE BY B: Distance between the internal boundary of B and the external boundary of A, where A is completely included in B. (A Enclosure by B = B Enclosure of A)

Rule label: layer.**EN**.n



PASS/FAIL ILLUSTRATION: For pass/fail design rules, cases that pass a design rule are marked “O” (OK), cases that fail a design rule are marked “X” (cross out).

Rule label: layer.**R**.n

Illustrated case **passes** the design rule

Illustrated case **fails** the design rule

INTERSECT : A intersects B, if the boolean operation A .and. B does return an area > 0.

INTERACT : A interacts with B, if they have one or more points in common (i.e. if they intersect, or if they touch at one or more points or touch along an edge)

UNREMOVABLE WIDTH OR SPACE : Width or space that remains after a upsizing / downsizing / upsizing operation for a given geometry

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7.3.2 DERIVED GEOMETRIES

OD2: OD25
Thick oxides devices

FIELD: **.not.** OD
Anything that is not OD

PW: **.not.** (NW **.or.** PW;blk)
Anything that is not NW and where PW is not blocked.

NW1V: NW **.not.** OD2
NW of core device

NW2V: NW **.and.** OD2
NW of I/O device

RW: DNW **.not.** NW
An isolated PW

GATE: OD **.and.** PO
PO over OD

N-CHANNEL: GATE **.not.** NW
GATE over PW

P-CHANNEL: GATE **.and.** NW
GATE over NW

P+ OD: OD **.and.** PP **.not.** PO
Heavily doped P type OD that does not include transistor channels

N+ OD: OD **.and.** NP **.not.** PO
Heavily doped N type OD that does not include transistor channels

NW STRAP: (N+ OD) **.and.** NW
N+ OD in NW; ohmic connection to NW

PW STRAP: (P+ OD) **.and.** PW
P+ OD in PW; ohmic connection to PW

N+ SD: (N+ OD) **.and.** PW
N+ OD in PW (N+ Source/Drain, N+/PW junction)

P+ SD: (P+ OD) **.and.** NW
P+ OD in NW (P+ Source/Drain, P+/NW junction)

SOURCE/DRAIN: P+ SD **.or.** N+ SD
Heavily doped OD enclosed by a well of the opposite doping type

BUTTED STRAP: (N+ SD **.touching.** PW STRAP) **.or.** (P+ SD **.touching.** NW STRAP)
Silicided OD shared by Source/Drain and well strap. SD and well strap are connected by silicide, i.e. both are at the same potential

VARACTOR: (OD **.and.** NW **.and.** PO **.and.** NP) **.or.** (OD **.and.** PW **.and.** PO **.and.** PP)
GATE consisting of a PO over OD of the same doping polarity. Structures with opposite PO and OD doping polarity are extracted as transistor gate capacitance.

MOS transistor: *Structure consisting of a Source and a Drain region of the same type separated by a GATE*

Thin oxide MOS: MOS **.not.** OD2

Thick oxide MOS: MOS **.and.** OD2

ENDCAP: *The PO extension of a transistor gate in the width direction (onto the field) required to ensure that the gate has full control of the channel*

BarfromLDD: (RH .or. HRI .or. MKR;BJT .or. N1V;blk .or. N2V;blk)
Structures that must be blocked from all LDD implants

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7.3.3 GENERIC LAYER REFERENCES

CMOS090 offers the 7M2T metallization: where xMyT refers to a process with a total of x metal layers out of which y are thick.

An actual design is always designed in real metal levels M1, M2, M3, ..., but for description purposes in this document we use generic layer references for

- thin and thick metals (Mx and Mn, respectively) and small and large vias (VIAx and VIAn, respectively).
- top-most metal and via layers (Mtop, etc.).

Depending on the metallization choice the rules and process characteristics apply according to the following tables:

M1, VIAx (small via), Mx (thin metal), VIAn (large via), Mn (thick metal)													
	M1	**VIA1**	**M2**	**VIA2**	**M3**	**VIA3**	**M4**	**VIA4**	**M5**	**VIA5**	**M6**	**VIA6**	**M7**
7M2T	M1	VIAx	Mx	VIAx	Mx	VIAx	Mx	VIAx	Mx	VIAn	Mn	VIAn	Mn

Mtop (top-most metal), VIAtop (topmost via), etc.					
	M5	**VIA5**	**M6**	**VIA6**	**M7**
7M2T	M5	VIAtop-1	Mtop-1	VIAtop	Mtop

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7.3.4 GENERAL DESIGN RULES

7.3.4.1 Assumptions for Rule Elaboration

Assumptions for Design Rule Elaboration	
	All rules are MINIMUM dimensions except if something else is specified.
	All dimensions are defined in MICRONS and areas in SQUARE MICRONS, unless otherwise specified.

7.3.4.2 General Data Requirements

General Data Design Rules	
GEN.1	Standard layout design grid is 0.005 micron for all the levels. Off-grid design data is not allowed.
GEN.2	Only vertical or horizontal geometries are allowed. Any angle different from 0 or 90° is forbidden except where 45° or other angles are explicitly allowed. Non-acute shapes with 45° angles are allowed for: - OD, PO, M1, Mx, Mn, CB, AP, NITRIDE - CB;via (unless when covered by NITRIDE;bump) - PW;block under INDDMY - features in approved bitcells - features in the corners of the sealring (must be marked with MKR;sealring) Non-acute shapes with any angle are allowed for: - CB;via when covered by NITRIDE;bump - special features metal on datatype 31 for logo artwork (must be marked with MKR;logo).
GEN.4	Minimum width and minimum space rules must be followed for any layer;datatype that results in a physical feature [a]. Specifically, shapes with acute angles do not fulfill these requirements and are forbidden in any layer;datatype that results in a physical feature.

a.Except for DNW, CB, BOTMIM and MKTOPMIM in the corner-L .

7.3.4.3 Process Identification Marker Requirements

The product designs must contain markers to identify the standard process and the metallization choice. This is required for the CAD2MASK (N/A) and reticle enhancement operations.

Process Identification Marker Design Rules	
ID.BEOL.1	Any final product design must be covered by the metallization ID marker MKR;7M2T Any Metal in the design must be covered with this marker with a >0 enclosure. The marker shall cover the whole data extent (typically it is drawn line on line with the exterior boundary of the MKR;sealring that faces the scribe line).

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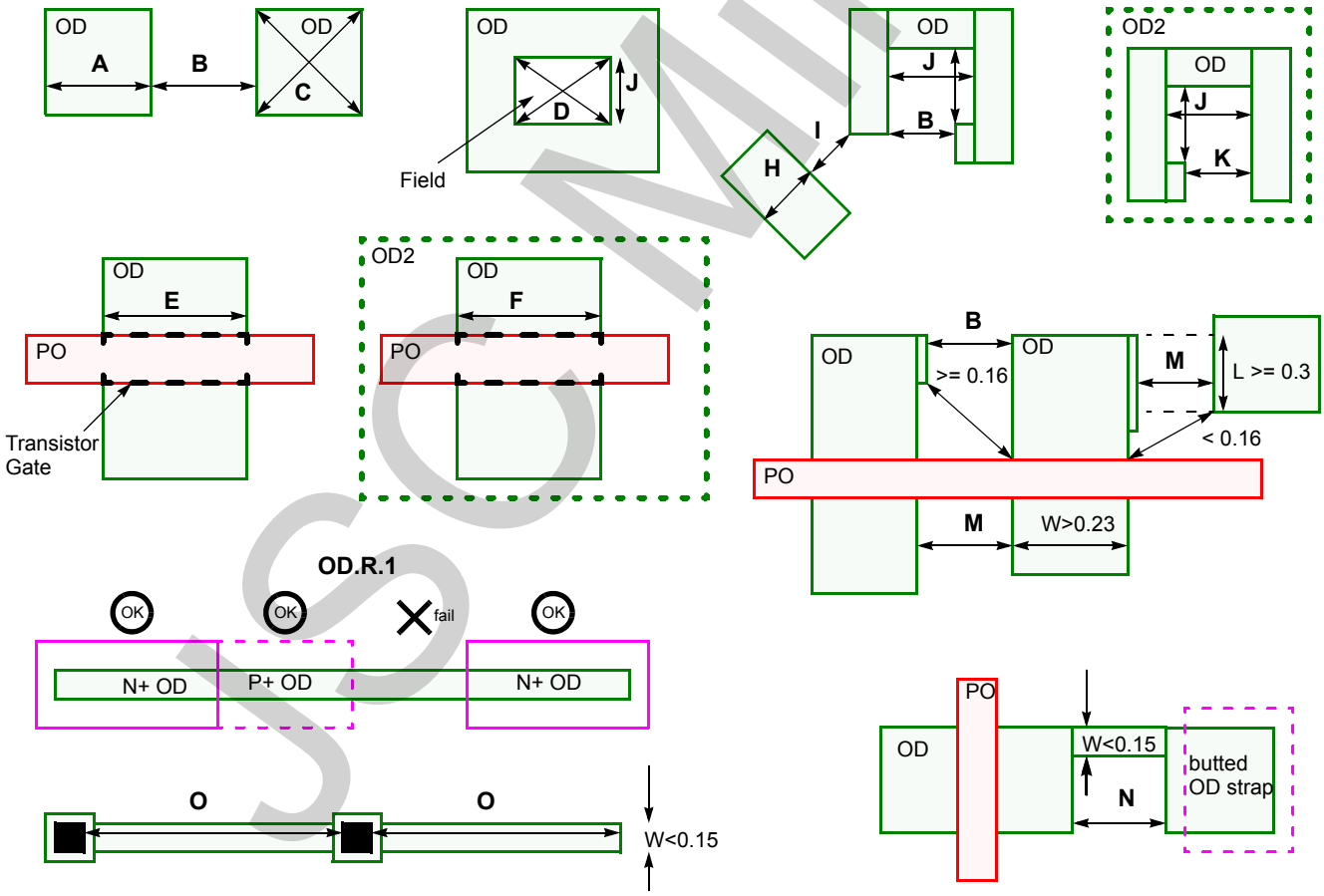
7.3.5 FRONT-END PROCESS DESIGN RULES

7.3.5.1 Gate Oxide and Diffusion (OD)

OD Design Rules			
OD.W.1	Width	A	0.110
OD.S.1	Space	B	0.140
OD.A.1	Area	C	0.060
OD.A.2	Enclosed area	D	0.085
OD.W.2	Width of transistor	E	0.120
OD.W.2.1	Width of 2.5 V transistors	F	0.400
OD.W.3	Width of 45° OD lines	H	0.180
OD.S.2	Space of 45° OD lines	I	0.180
OD.S.3	Space between 2 OD segments of U-shaped OD or OD enclosed area (notch)	J	0.200
OD.S.4	Space (within OD2)	K	0.180
OD.S.5	Space between two OD with a parallel length >= 0.3um (L) if at least one of the corresponding OD regions has width > 0.23 µm (W) and at least one of the OD is crossed by PO. Rule only applies for distances < 0.16um from the gate edge where the PO crosses the OD edge.	M	0.160
OD.L.1	Maximum length of OD connected to butted OD (strap) when width of this OD is < 0.15um	N	0.500
OD.L.2	Maximum OD length between 2 CO as well as between 1 CO and the OD line end when the OD width is < 0.15µm	O	25.00
OD.R.1	OD must be fully covered by the {combination of NP + PP} (except N-Well resistor) [a]		

a.N-Well resistor is not a fully supported device. OD;dummy is not required to follow that rule, i.e. it can be undoped.



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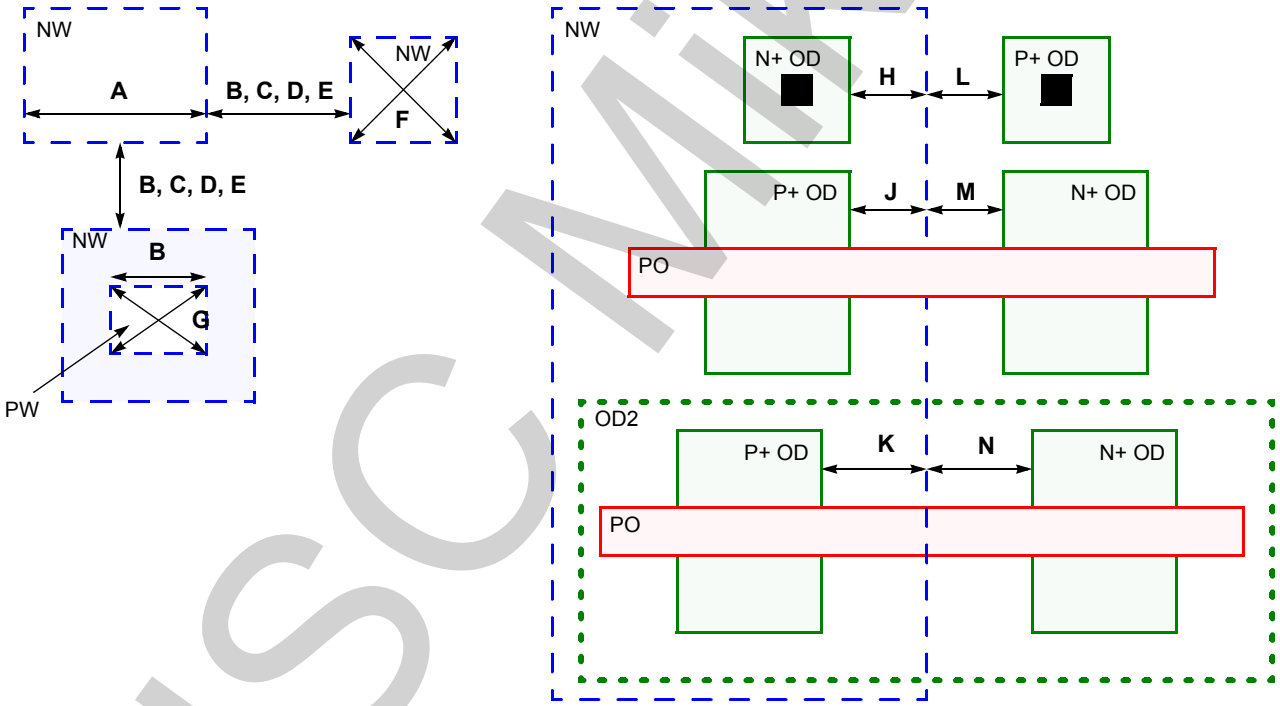
7.3.5.2 NWELL (NW)

a) N-Well

NW Design Rules (N-Well)			
NW.W.1	Width	A	0.620
NW.S.1	Space	B	0.620
NW.S.2	Space of two NW1V at different potential [a]	C	1.000
NW.S.3	NW1V Space to NW2V (align if less) [a]	D	1.200
NW.S.4	Space of two NW2V at different potential [a]	E	1.200
NW.A.1	Area	F	1.550
NW.A.2	Enclosed area	G	1.550
NW.EN.1	Enclosure of NWELL strap [b]	H	0.170
NW.EN.2	Enclosure of P+ OD [c]	J	0.220
NW.EN.3	Enclosure of P+ OD in OD2	K	0.310
NW.D.1	Distance to PWELL strap	L	0.170
NW.D.2	Distance to N+ OD [c]	M	0.220
NW.D.3	Distance to N+ OD in OD2	N	0.310

a.DRC implementation is “on different net”
b.NW strap across NW/PW boundary not allowed
c.Combined N+ OD to P+ OD distance across well boundary is 0.44um



b) P-Well

P-Well (PW) is not a drawn layer, it is derived from {NW or PW;blk}. Areas marked with PW;blk (P-Well block) will receive neither N-Well nor P-Well implants. For further details on PW;blk layer see §7.3.8.12.

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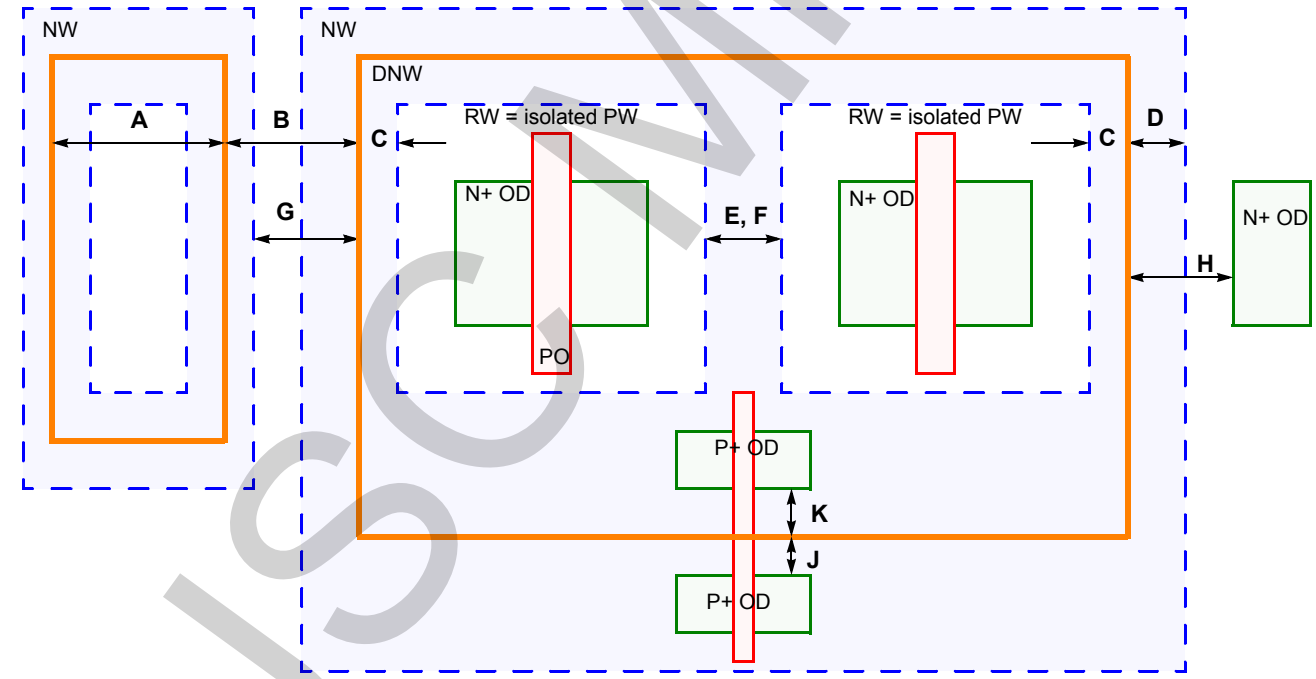
7.3.5.3 Deep NWELL (DNW)

The purpose of this layer is to get PW isolated from substrate: DNW (vertical isolation) must be used with a NW guard ring (lateral isolation).

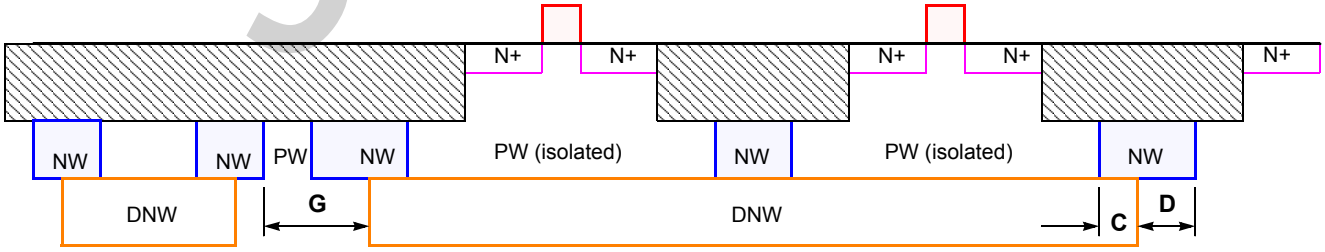
The DNW should also be drawn under NW for better latch-up immunity.

DNW Design Rules (Deep NWELL)			
DNW.W.1	Width	A	3.000
DNW.S.1	Space	B	4.800
DNW.OL.1	Overlap of NW [a]	C	0.400
DNW.EN.1	Enclosure by NW	D	1.500
DNW.S.2	RW Space (Width of NW between two RW) if one RW is at different potential <= 1.2V [b]	E	1.000
DNW.S.3	RW Space (Width of NW between two RW) if one RW is at different potential > 1.2V [c]	F	1.200
DNW.D.1	Distance to NW on different net	G	3.300
DNW.D.2	Distance to N+ SD	H	1.820
DNW.D.3	Distance to PFET Gate (P-Channel) [d]	J	1.000
DNW.EN.2	Enclosure of PFET Gate (P-Channel) [d]	K	0.500
DNW.R.1	DNW edge must be fully enclosed by NW		
DNW.R.2	NWs shorted by the DNW level must be at the same potential		
DNW.R.3	DNW must not intersect OD of PNP (MKR;BJT)		

a.NW strap across DNW is allowed
b.DRC implementation is RW space to RW on different net
c.DRC implementation is RW space to {RW interacting with P+ OD/OD2} on different net
d.P-Channel must be either completely inside DNW or completely outside DNW.



Cross Section:



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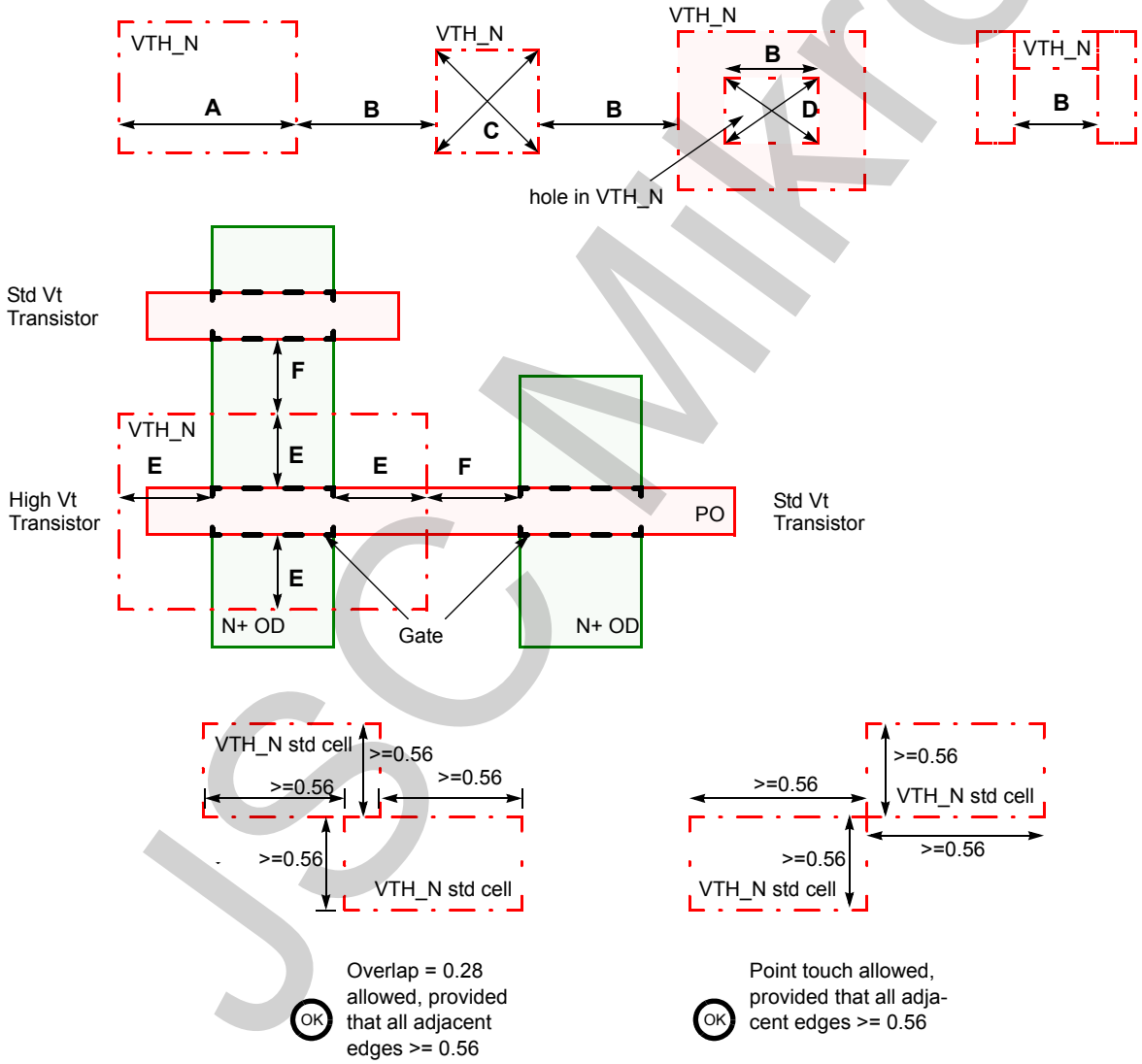
7.3.5.4 High Vt NMOS (VTH_N)

The purpose of the VTH_N layer is to allow the additional P-type implant necessary for HVT NMOS transistors.

VTH_N Design Rules (HVT NMOS)			
VTH_N.W.1	Width (with exception of touching standard cell library cells) [a]	A	0.400
VTH_N.S.1	Space (with exception of touching standard cell library cells) [a]	B	0.240
VTH_N.A.1	Area	C	0.400
VTH_N.A.2	Enclosed area	D	0.400
VTH_N.EN.1	Enclosure of Gate	E	0.220
VTH_N.D.1	Distance to Gate not using VTH_N	F	0.220
VTH_N.R.1	VTH_N must not intersect P-Channel (transistor and varactor), P+ SD, OD2		

a.Point touch of corners of std library cells and 1 track overlap of std library cells are allowed as these are recognized and specially treated by OPC. A minimum length of 0.56 is required at the edges adjacent to the point touch or the single track overlap.



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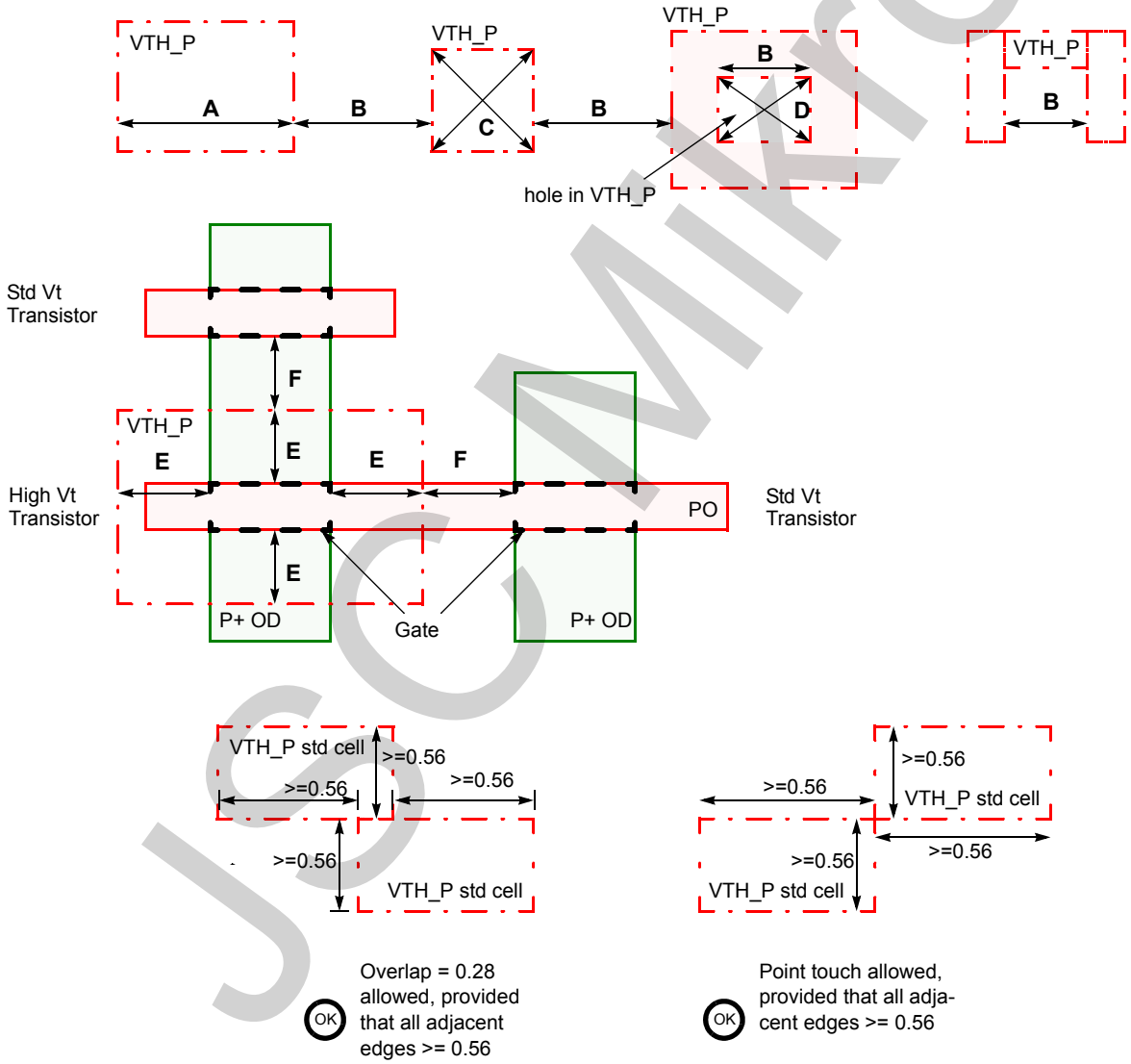
7.3.5.5 High Vt PMOS (VTH_P)

The purpose of the VTH_P layer is to allow the additional N-type implant necessary for HVT PMOS transistors.

VTH_P Design Rules (HVT PMOS)			
VTH_P.W.1	Width (with exception of touching standard cell library cells) [a]	A	0.400
VTH_P.S.1	Space (with exception of touching standard cell library cells) [a]	B	0.240
VTH_P.A.1	Area	C	0.400
VTH_P.A.2	Enclosed area	D	0.400
VTH_P.EN.1	Enclosure of Gate	E	0.220
VTH_P.D.1	Distance to Gate not using VTH_P	F	0.220
VTH_P.R.1	VTH_P must not intersect N-Channel (transistor and varactor), N+ SD, OD2		

a.Point touch of corners of std library cells and 1 track overlap of std library cells are allowed as these are recognized and specially treated by OPC. A minimum length of 0.56 is required at the edges adjacent to the point touch or the single track overlap.



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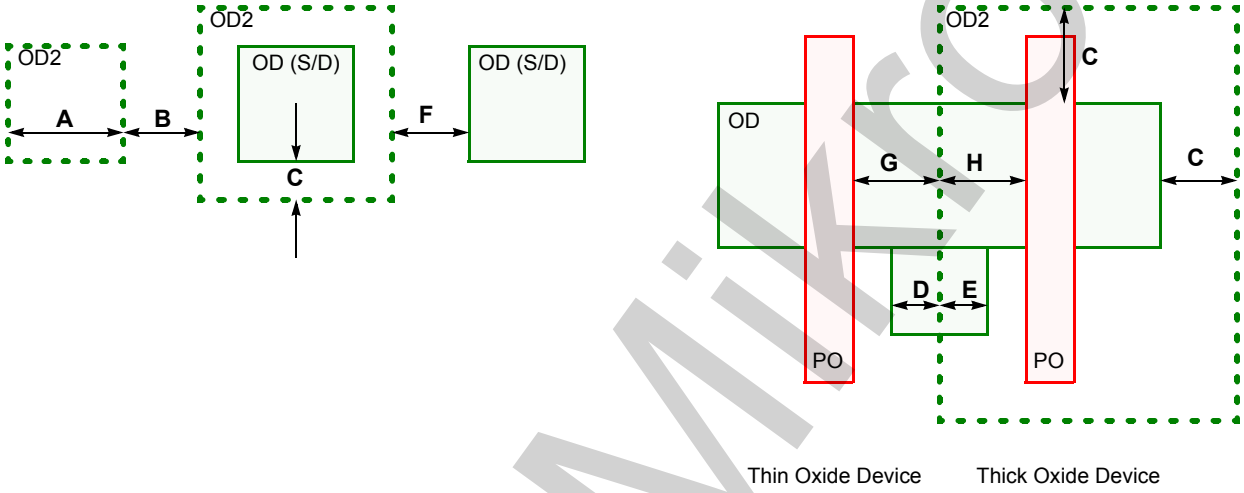
7.3.5.6 Thick Oxide Device (OD25)

The purpose of this layer is to get thick gate oxide transistors.

- The OD25 layer is used for 2.5V / 5nm gate oxide transistors.

Note that OD2 refers to thick oxide device, i.e. OD2 = OD25

OD2 Design Rules (Thick Oxide Device - OD25)			
OD2.W.1	Width	A	0.620
OD2.S.1	Space. Merge if less	B	0.620
OD2.EX.1	Extension on {Source/Drain or Gate} (well straps excluded)	C	0.270
OD2.EX.2	P+ SD Extension on OD2	D	0.130
OD2.OL.1	Overlap of P+ SD	E	0.130
OD2.D.1	Distance to Source/Drain OD (well straps excluded)	F	0.270
OD2.D.2	Distance to Gate of thin oxide MOS	G	0.340
OD2.EN.1	Enclosure of Gate of 2.5V MOS in S/D direction	H	0.340



OD2 rules for NWELL, NWELLGO2, PWELL and PWELLGO2 logical operation

The NWELL, PWELL, NWELLGO2, and PWELLGO2 masks are generated from drawn layers NW and OD2 by logical operations (N/A) as default. CAD2MASK also will remove features from the well masks that would be non-manufacturable. The following rules (OD2.B.1, OD2.B.2, OD2.B.3, OD2.B.4) are defined to avoid small patterns or gaps that would not be removable by CAD2MASK operations. For sensitive circuits where the wells shall not be altered, shall follow the corresponding recommended rules on the next page instead.

This smoothing is performed by a up-size/down-size/up-size scaling. The value of each up-sizing is equal to half the rule value minus a grid step, while the corresponding down-size value is therefore equal to the rule value minus two grid steps. Thus the smoothing ensures that patterns smaller than the rule value can be removed in the mask.

OD2 Design Rules - Continued (Rules related to logical operations)			
OD2.B.1	Unremovable Width or Space of {OD2 .and. NW} (NWELLGO2 mask)		0.550
OD2.B.2	Unremovable Width or Space of {OD2 .not. (NW .or. PW;blk)} (PWELLGO2 mask)		0.550
OD2.B.3	Unremovable Width or Space of {NW .not. OD2} (NWELL mask)		0.550
OD2.B.4	Unremovable Width or Space of {(.not. OD2) .not. (NW .or. PW;blk)} (PWELL mask)		0.550

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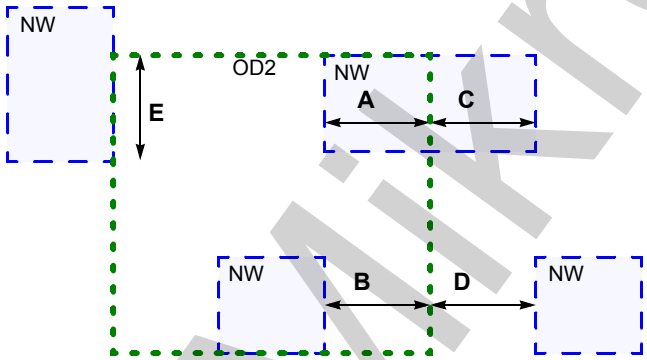
Recommended OD2 rules for NWELL, NWELLGO2, PWELL and PWELLGO2 logical operation

The NWELL, PWELL, NWELLGO2, and PWELLGO2 masks are generated from drawn layers NW and OD2. The recommended design rules R-OD2.B.1, R-OD2.B.2, R-OD2.B.3, R-OD2.B.4, R-OD2.B.5) will completely avoid small patterns or gaps during logical operation (N/A), and therefore not gaps will need to be filled and no slivers will need to be removed - i.e. the wells will be generated exactly as drawn.

The design rules R-OD2.B.1, R-OD2.B.2, R-OD2.B.3, R-OD2.B.4, and R-OD2.B.5 shall be followed for tape-outs to foundries. Designs that follow design rules R-OD2.B.1, R-OD2.B.2, R-OD2.B.3, R-OD2.B.4, and R-OD2.B.5 are automatically clean to rules OD2.B.1, OD2.B.2, OD2.B.3, OD2.B.4 as well.

Recommended OD2 Design Rules - Continued (Rules related to logical operations)			
R-OD2.B.1	OD2 Overlap of NW (align if less) (NWELLGO2 mask)	A	0.620
R-OD2.B.2	OD2 Extension on {NW or PW;blk} (align if less) (PWELLGO2 mask)	B	0.620
R-OD2.B.3	NW Extension on OD2 (align if less) (NWELL mask)	C	0.620
R-OD2.B.4	OD2 Distance to {NW or PW;blk} (align if less) (PWELL mask)	D	0.620
R-OD2.B.5	Width of {OD2 or NW or PW;blk} (PWELL mask)	E	0.620



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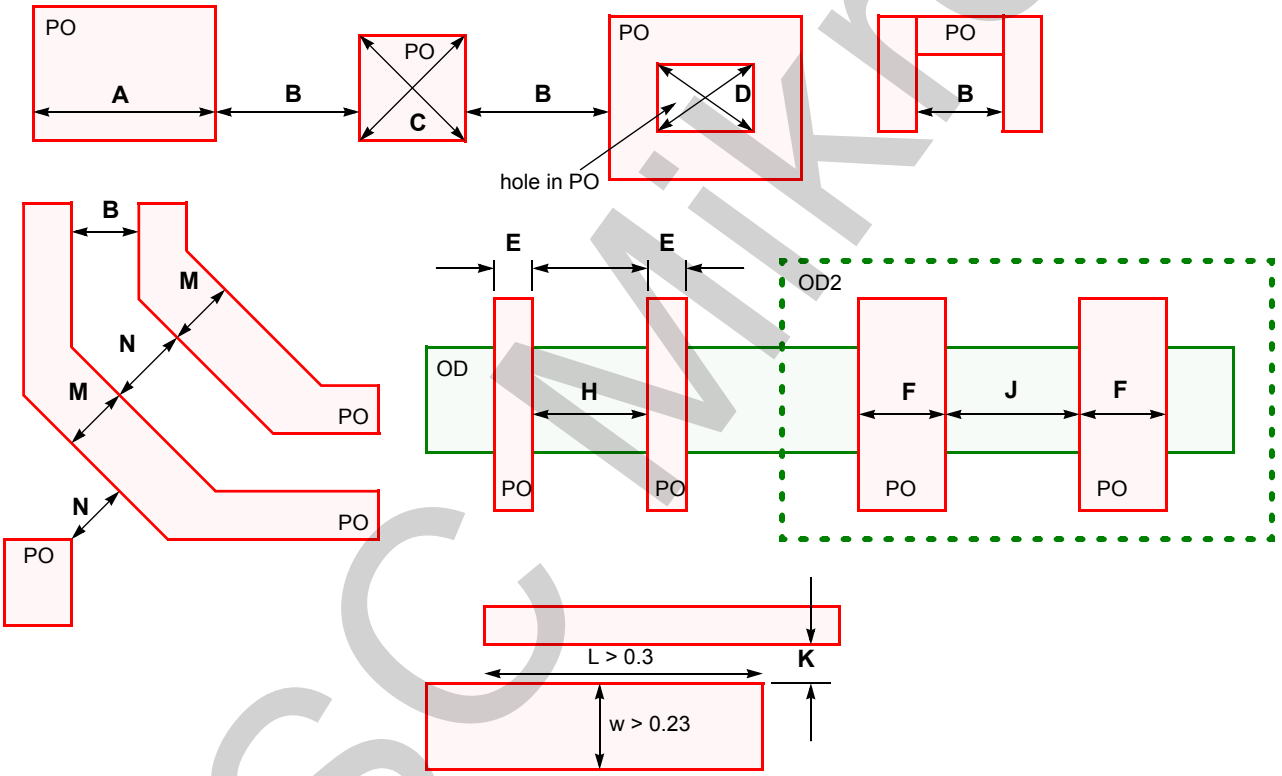
7.3.5.7 Poly (PO)

Note that intrinsic (un-implanted) PO lines are not allowed. PO lines must be implanted with NP or PP (PO.R.5).

PO Design Rules (POLY)			
PO.W.1	Width	A	0.100
PO.S.1	Space on field oxide	B	0.140
PO.A.1	Area	C	0.060
PO.A.2	Enclosed area	D	0.110
PO.W.2	Transistor length for thin oxide NMOS and PMOS	E	0.100
PO.W.4	Transistor length for 2.5V NMOS and PMOS	F	0.280
PO.S.2	PO space on OD for thin oxide NMOS and PMOS	H	0.150
PO.S.3	PO space on OD for 2.5V NMOS and PMOS	J	0.250
PO.S.4	Space if at least one PO width is > 0.23 µm (W) and if the parallel PO run length (between both PO) is > 0.3 µm (L)	K	0.180
PO.W.6	Width of 45° PO lines on field oxide	M	0.190
PO.S.5	Space of 45° PO lines on field oxide	N	0.190



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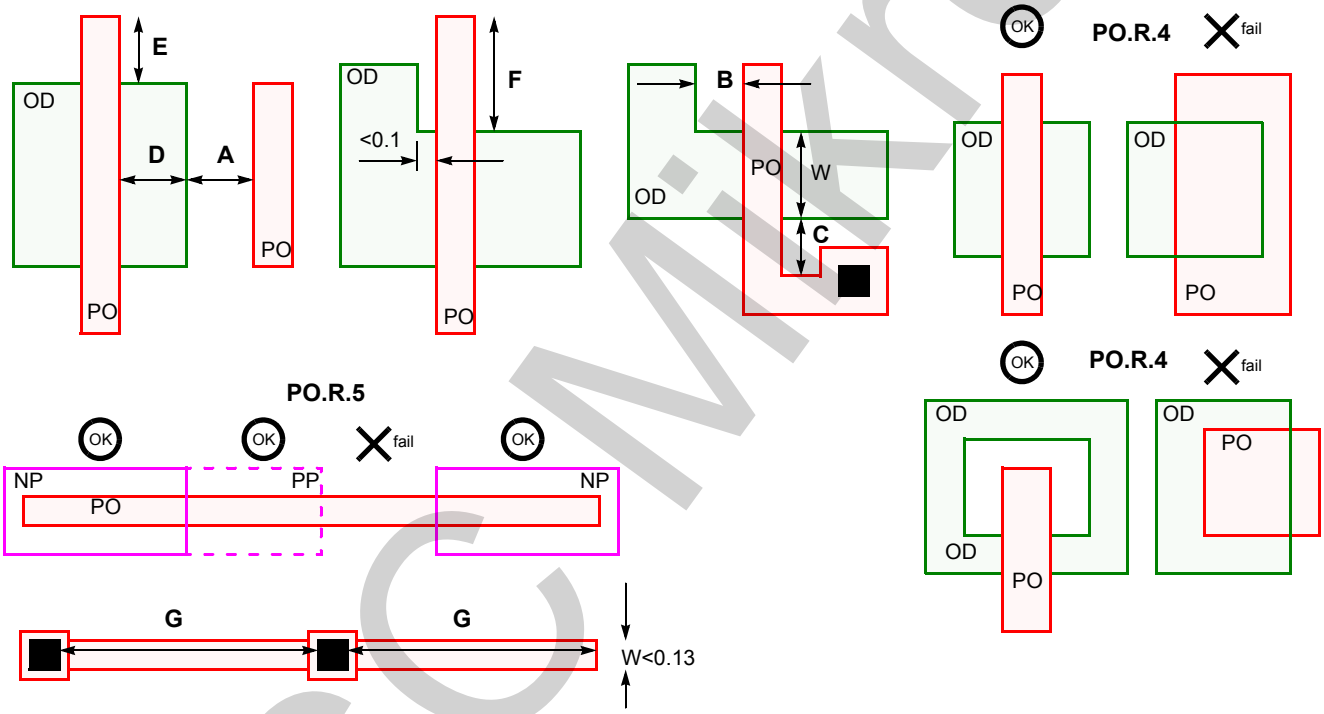
PO Design Rules (Bulk) - Continued			
PO.D.1	Distance of a PO on field to an OD	A	0.050
PO.D.2	Distance to OD corner when PO and OD are in the same MOS transistor, if W<0.2 µm	B	0.100
PO.D.3	Distance between PO corner on field and Gate when PO and Gate are in the same MOS transistor, and W<0.2 µm	C	0.100
PO.EX.1	OD Extension on PO (width of source and drain)	D	0.150
PO.EX.2	PO Gate extension on OD (endcap)	E	0.160
PO.EX.3	PO Gate extension on OD (endcap) when L-shaped OD to PO distance is < 0.1	F	0.180
PO.L.1	Maximum PO length between 2 CO as well as between 1 CO and the PO line end when the PO width <0.13 µm	G	25.00
PO.R.3	Gate must be a rectangle orthogonal to grid (except varactors). For varactor: no 90° corner of OD under PO		
PO.R.4	PO intersecting OD must completely straddle OD (except varactors)		
PO.R.5	PO must be fully covered by the combination NP + PP (except for HIPO resistor) [a]		

a.PO;dummy is not required to follow that rule, i.e. PO;dummy can be undoped.



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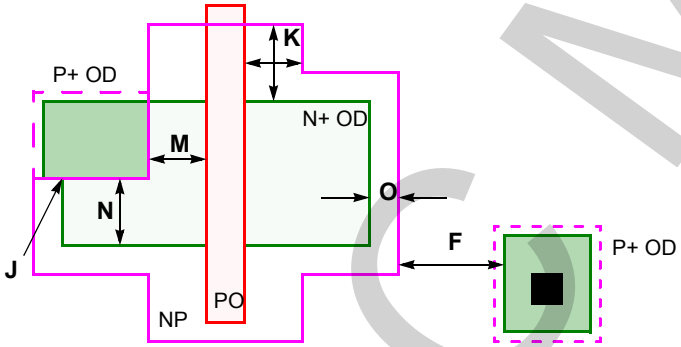
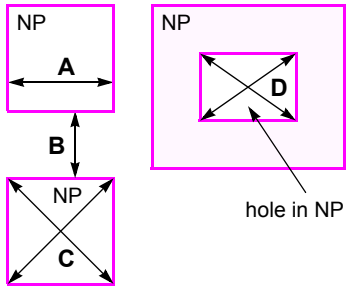
7.3.5.8 NPLUS (NP)

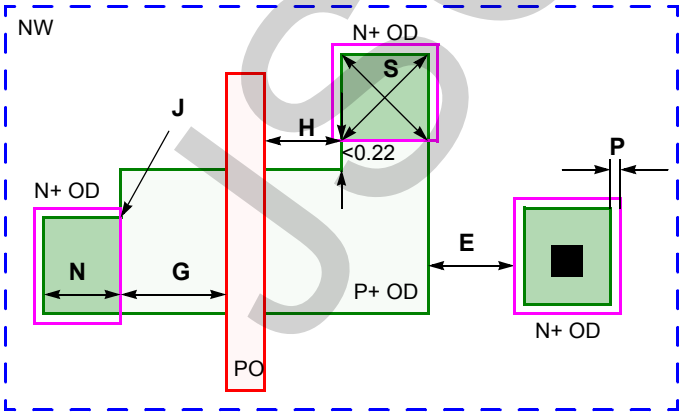
a) NPLUS

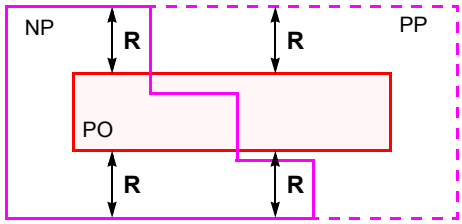
NP Design Rules (NPLUS)			
NP.W.1	Width	A	0.240
NP.S.1	Space	B	0.240
NP.A.1	Area	C	0.122
NP.A.2	Enclosed area	D	0.122
NP.D.1	Distance to a P+ OD (not along PO) other than PW strap	E	0.130
NP.D.2	Distance (in PW) to a non butted PW strap	F	0.020
NP.D.3	Distance (including NW strap) to P+ Gate on OD	G	0.320
NP.D.4	Distance from a butted N+ OD to the related PO edge if butting P+ OD is extending < 0.22 in NW	H	0.320
NP.D.5	Distance to OD for an NP edge forming a butted N+ OD/P+ OD (allowed for up to 0.13um distance from butted N+ OD/P+ OD)	J	0.000
NP.EN.1	Enclosure of Gate (square corner) (except varactors)	K	0.220
NP.EN.2	Enclosure of Gate on OD	M	0.320
NP.OL.1	Overlap of N+ OD	N	0.130
NP.EX.1	Extension on OD (other than NW strap)	O	0.130
NP.EX.2	Extension on OD (NW strap)	P	0.020
NP.EX.3	{Combination of NP + PP} Extension on PO [a]	R	0.200
NP.A.3	Area of N+ OD butted to a P+OD	S	0.040
NP.R.1	Intersection with PP is not allowed [b]		

a.Rule is identical to PP.EX.3. The HIPO resistoris the only device where the combined NP + PP does not fully enclose PO - see PO.R.5.
b.Butted NP and PP is allowed. Rule is identical to PP.R.1









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b) NPLUS rules for NLDD and NLDDGO2 logical operation

The NLDD and NLDDGO2 masks are generated from drawn layers by logical operations as default (N/A). During the mask operations, it is required to even the small patterns or gaps that might result after the Boolean operations. This smoothing is performed by a up-size/down-size/up-size scaling. The value of each up-sizing is equal to half the rule value minus a grid step, while the corresponding down-size value is therefore equal to the rule value minus two grid steps. Thus the smoothing ensures that patterns smaller than the rule value can be removed in the mask.

NLDD and NLDDGO2 masks bar from the corresponding LDD implants the regions covered with the following markers:

- BarfromLDD: (RH .or. HRI .or. MKR;BJT .or. N1V;blk .or. N2V;blk) Structures that must be blocked from all LDD implants

NP Design Rules - Continued (Rules related to logical operations)			
NP.B.1	Unremovable Width or Space of {NP .not. NW .and. OD2 .not. BarfromLDD} (NLDDGO2 mask)		0.240
NP.B.2	Unremovable Width or Space of {NP .not. NW .not. OD2 .not. BarfromLDD} (NLDD mask)		0.240

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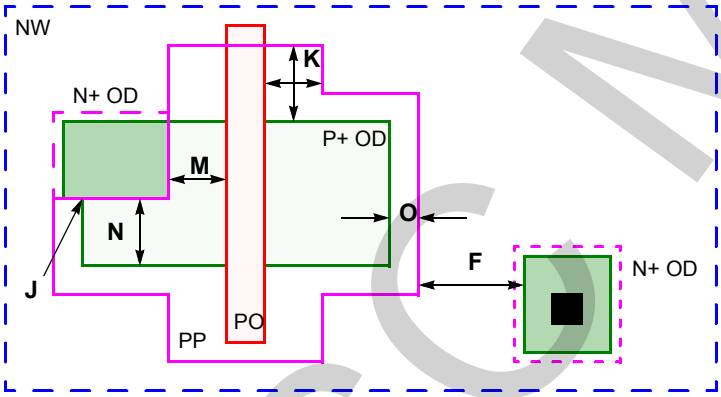
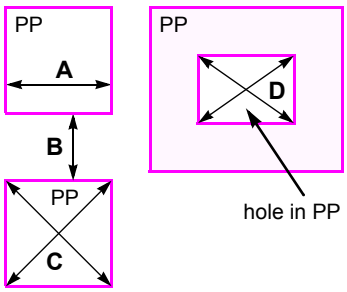
7.3.5.9 PPLUS (PP)

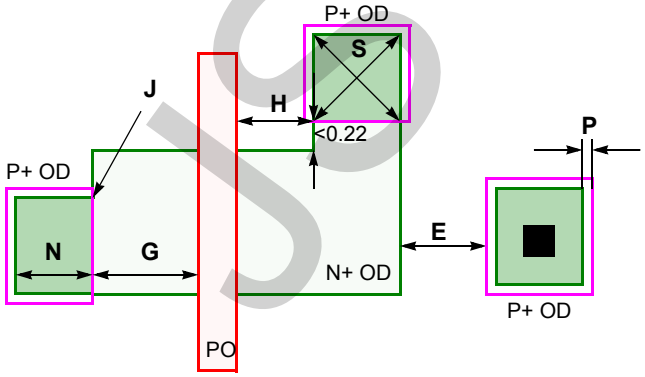
a) PPLUS

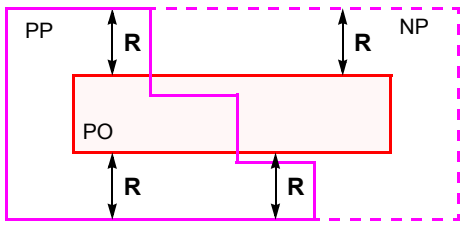
PP Design Rules (PPLUS)			
PP.W.1	Width	A	0.240
PP.S.1	Space	B	0.240
PP.A.1	Area	C	0.122
PP.A.2	Enclosed area	D	0.122
PP.D.1	Distance to N+ OD (not along PO) other than NW strap	E	0.130
PP.D.2	Distance (in NW) to non butted NW strap	F	0.020
PP.D.3	Distance (including PW strap) to N+ Gate on OD	G	0.320
PP.D.4	Distance from a butted P+ OD to the related PO edge if butting N+ OD is extending < 0.22 in PW	H	0.320
PP.D.5	Distance to OD for an PP edge forming a butted N+ OD/P+ OD (allowed for up to 0.13um distance from butted N+ OD/P+ OD)	J	0.000
PP.EN.1	Enclosure of Gate (square corner) (except varactors)	K	0.220
PP.EN.2	Enclosure of Gate on OD	M	0.320
PP.OL.1	Overlap of P+ OD	N	0.130
PP.EX.1	Extension on OD (other than PW strap)	O	0.130
PP.EX.2	Extension on OD (PW strap)	P	0.020
PP.EX.3	{Combination of NP + PP} Enclosure of PO [a]	R	0.200
PP.A.3	Area of P+ OD butted to an N+ OD	S	0.040
PP.R.1	Intersection with NP is not allowed [b]		

a.Rule is identical to NP.EX.3. The HIPO resistoris the only device where the combined NP + PP does not fully enclose PO - see PO.R.5.
b.Butted NP and PP is allowed. Rule is identical to NP.R.1









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b) PPLUS rules for PLDD/PLDDGO2/PPLUS/PPLUSGO2 logical operation

The PLDD, PLDDGO2, PPLUS and PPLUSGO2 masks are generated from drawn layers by logical operations as default (N/A). During the mask operations, it is required to even the small patterns or gaps that might result after the Boolean operations. This smoothing is performed by a up-size/down-size/up-size scaling. The value of each up-sizing is equal to half the rule value minus a grid step, while the corresponding down-size value is therefore equal to the rule value minus two grid steps. Thus the smoothing ensures that patterns smaller than the rule value can be removed in the mask.

PLDD and PLDDGO2 masks bar from the corresponding LDD implants the regions covered with the following markers:

- BarfromLDD: (RH .or. HRI .or. MKR;BJT .or. N1V;blk .or. N2V;blk) Structures that must be blocked from all LDD implants

PPLUS and PPLUSGO2 are generated from the PP and OD2 layers and should be also verified for unremovable dimensions.

PP Design Rules - Continued (Rules related to logical operations)			
PP.B.1	Unremovable Width or Space of {PP .and. NW .and. OD2 .not. BarfromLDD} (PLDDGO2 mask)		0.240
PP.B.2	Unremovable Width or Space of {PP .and. NW .not. OD2 .not. BarfromLDD} (PLDD mask)		0.240
PP.B.4	Unremovable Width or Space of {PP .and. OD2} (PPLUSGO2)		0.240
PP.B.5	Unremovable Width or Space of {PP .not. OD2} (PPLUS)		0.240

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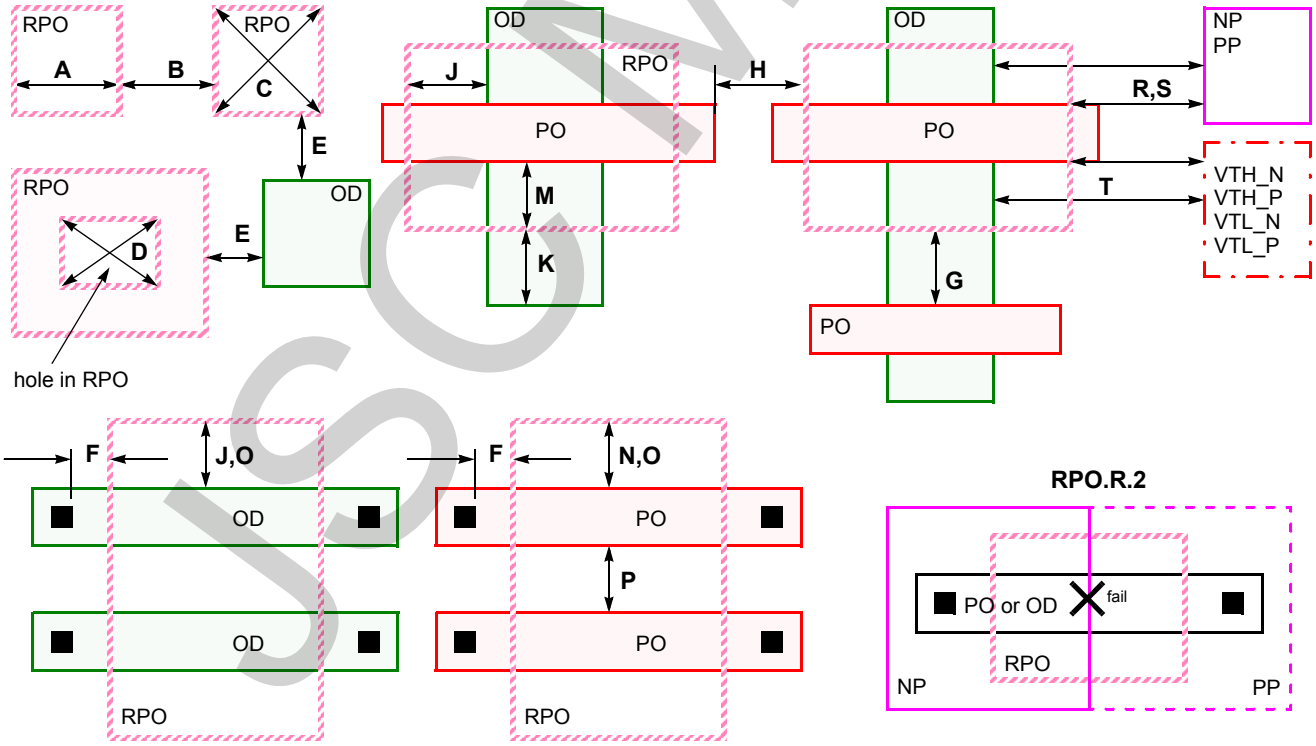
7.3.5.10Resist Protection Oxide (RPO)

Inside the feature of this layer, there is no silicidation of the silicon (substrate - mono silicon - or any deposited amorphous or poly crystalline silicon). Outside the feature, all sources, drains and poly are silicided. Due to the doping of the PO by the source/drain implants, the designer must avoid forming N+/P+ diodes in the unsilicided PO or OD features (design rule RPO.R.2).

RPO Design Rules (Resist Protection Oxide)			
RPO.W.1	Width	A	0.430
RPO.S.1	Space	B	0.430
RPO.A.1	Area	C	1.000
RPO.A.2	Enclosed area	D	1.000
RPO.D.1	Distance to OD on field	E	0.220
RPO.D.2	Distance to CO (on OD or on PO. RPO overlap with CO not allowed)	F	0.220
RPO.D.3	Distance to PO Gate, on OD	G	0.380
RPO.D.4	Distance to PO on field	H	0.300
RPO.EX.1	Extension on related OD for unsilicided OD (S/D or OD resistor)	J	0.220
RPO.EX.2	OD extension on RPO	K	0.220
RPO.EX.3	Extension on PO, on OD	M	0.300
RPO.EX.4	Extension on PO on field (RPO must overlap PO on both sides)	N	0.220
RPO.EX.5	Extension on unsilicided OD or PO (if RPO width > 10.0um)	O	0.300
RPO.S.2	PO space to PO within RPO	P	0.250
RPO.D.5	{Unsilicided PO or OD} Distance to NP	R	0.200
RPO.D.6	{Unsilicided PO or OD} Distance to PP	S	0.200
RPO.D.7	{Unsilicided PO or OD} Distance to VTH_N, VTH_P (overlap not allowed except for unsilicided transistors)	T	0.220
RPO.R.2	Unsilicided PO or OD can only be either NP or PP (butted NP/PP not allowed within RPO)		
RPO.R.3	Partially unsilicided Gate are not allowed		



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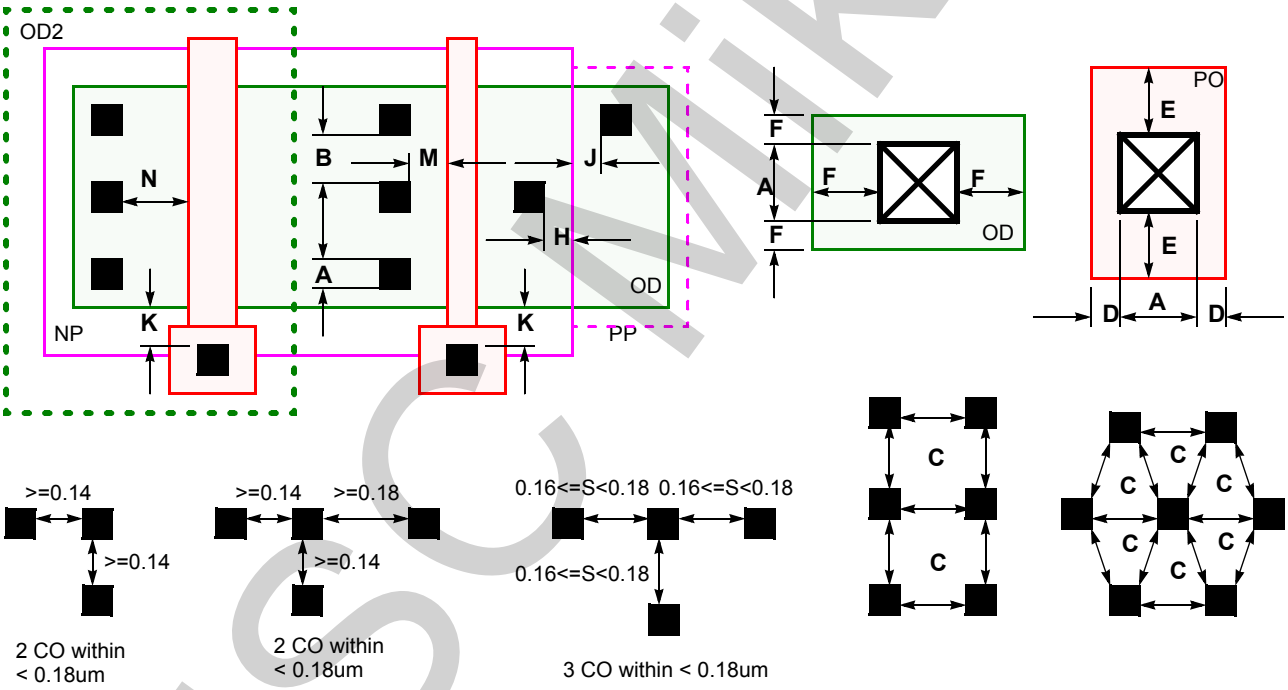
7.3.6 BACK-END PROCESS DESIGN RULES

7.3.6.1 Contact (CO)

CO Design Rules (Contact)			
CO.W.1	Width (width = length, min = max)	A	0.120
CO.S.1	Space	B	0.140
CO.S.2	Space to CO in an array (CO with 3 or more CO within < 0.18 um distance)	C	0.160
CO.EN.1	Enclosure by PO	D	0.020
CO.EX.1	PO Extension on CO on at least 2 opposite sides	E	0.050
CO.EN.2	Enclosure by OD	F	0.040
CO.D.1	Distance to butted P+ OD	H	0.060
CO.D.2	Distance to butted N+ OD	J	0.060
CO.D.3	Distance of {CO on PO} to OD	K	0.100
CO.D.4	Distance of {CO on OD} to Gate (CO on Gate is not allowed)	M	0.070
CO.D.5	Distance of {CO on OD} to Gate on OD2	N	0.110
CO.R.2	CO on NP/PP boundary on OD not allowed		
CO.R.3	CO inside RPO not allowed.		
CO.R.4	45° rotated CO not allowed		
CO.R.5	Non-square CO (bar-shape) not allowed except for seal ring		
CO.R.6	CO must be fully covered by M1 and by {PO or OD}		



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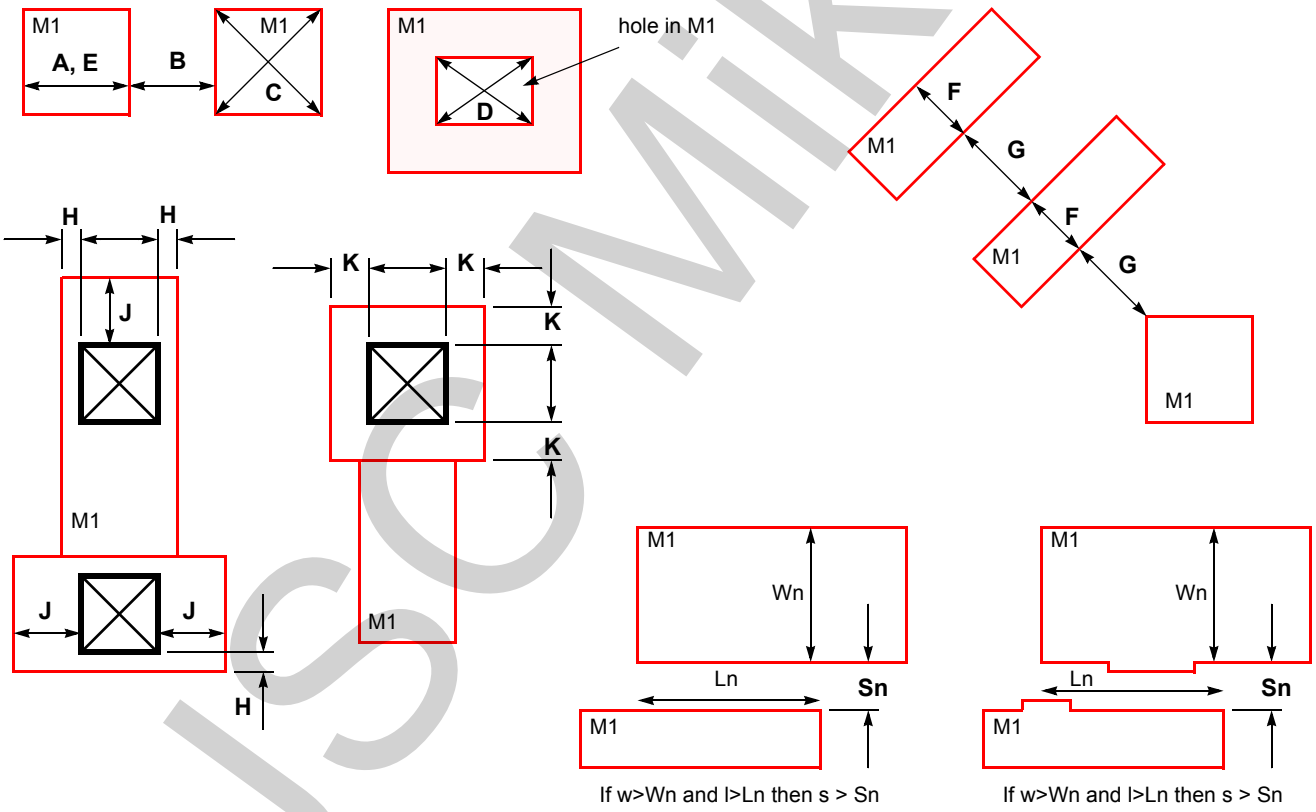
7.3.6.2 Metal 1 (M1)

M1 Design Rules (Metal 1)			
M1.W.1	Width	A	0.120
M1.S.1	Space	B	0.120
M1.A.1	Area	C	0.058
M1.A.2	Enclosed area	D	0.200
M1.W.2	Maximum width	E	12.00
M1.W.3	Width for 45° metal lines	F	0.190
M1.S.2	Space for 45° metal lines	G	0.190
M1.R.1	Line extension on CO is defined by either M1.EN.1 + M1.EX.1, or M1.EN.2		
M1.EN.1	Enclosure of CO	H	0.000
M1.EX.1	Extension on CO on at least 2 opposite sides, unless M1.EN.2 is fulfilled	J	0.050
M1.EN.2	Enclosure of CO, unless M1.EX.1 is fulfilled	K	0.025
M1.S.3.1	Space if at least one metal line width is > 0.3 um (W1) and if the parallel metal run length (between both metals) > 0.52 um (L1)	S1	0.170
M1.S.3.2	Space if at least one metal line width is > 1.50 um (W2) and if the parallel metal run length (between both metals) > 1.50 um (L2)	S2	0.500
M1.S.3.4	Space if at least one metal line width is > 4.50 um (W4) and if the parallel metal run length (between both metals) > 4.50 um (L4)	S4	1.500



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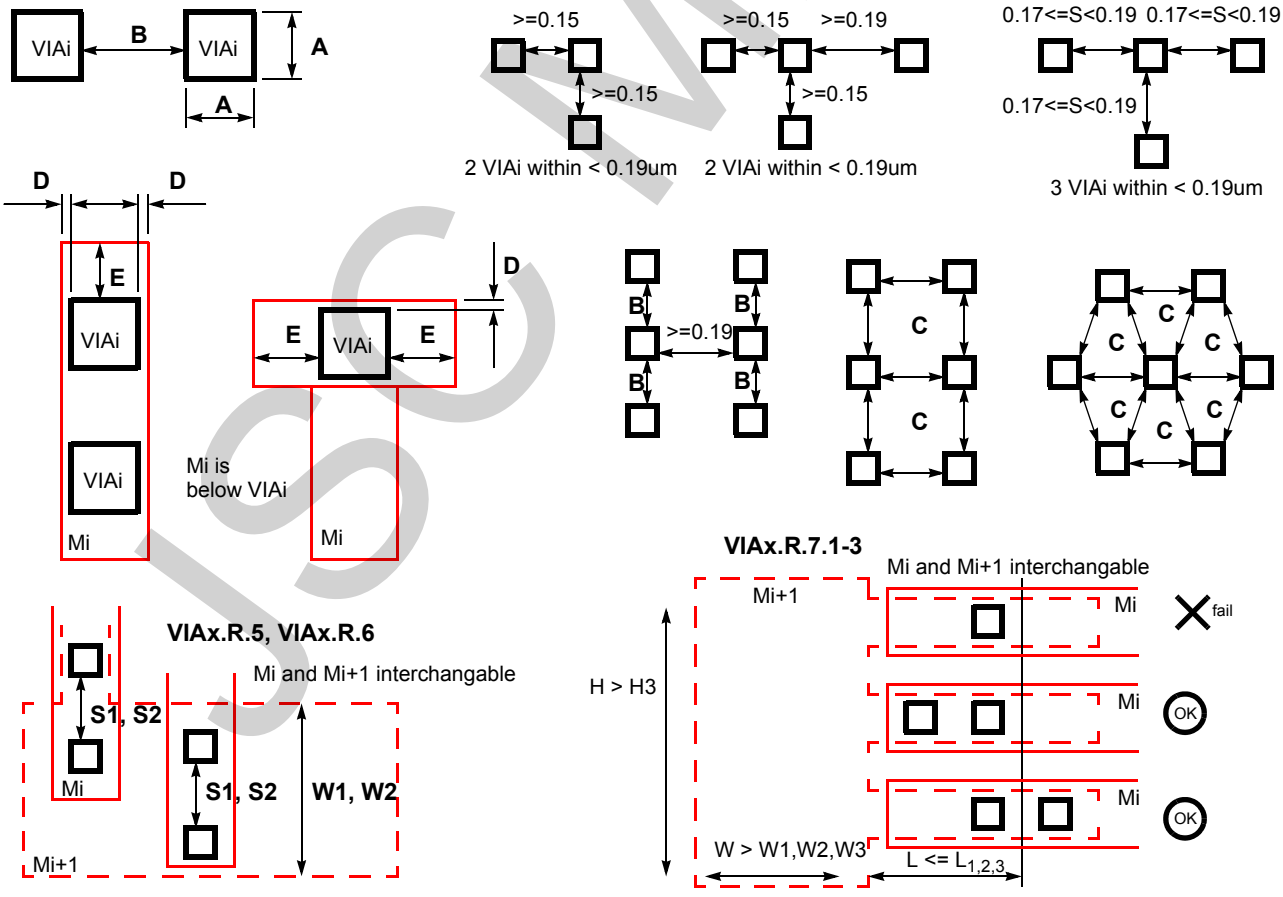
7.3.6.3 VIAx

For a specification of VIAi levels (i = 1, 2, 3, 4) to which the VIAx rules do apply see §7.3.3.

VIAx Design Rules			
VIAx.W.1	Width (width = length, min = max)	A	0.130
VIAx.S.1	Space	B	0.150
VIAx.S.2	VIAi Space to VIAi in an array (VIAi with 3 or more VIAi within < 0.19 um distance)	C	0.170
VIAx.EN.1	Enclosure of VIAi by Mi [a]	D	0.005
VIAx.EX.1	Mi Extension on VIAi on at least 2 opposite sides [a]	E	0.050
VIAx.R.1	45° rotated VIAi not allowed		
VIAx.R.2	Non-square VIAi (bar-shape) is not allowed except for seal ring		
VIAx.R.3	VIAi must be fully covered by metal below (Mi) and above (Mi+1)		
VIAx.R.4	VIAi can be partially or fully stacked. Maximum consecutive stacked VIAi is 4, unless there are 2 or more vias at each VIAi level on the same metal Mi/Mi+1 intersection.		
VIAx.R.5	At least 2 VIAi at space <= 0.29 um (S1), or at least 4 VIAi with space <= 0.57 um (S1') are required to connect Mi and Mi+1 when one of these 2 metals has width 0.42 um (W1) < w <= 0.98 um (W2)		
VIAx.R.6	At least 4 VIAi at space <= 0.29 um (S2), or at least 9 VIAi with space <= 0.77 um (S2') are required to connect Mi and Mi+1 when one of these 2 metals has width > 0.98 um (W2)		
VIAx.R.7.1	At least 2 VIAi within the same Mi/Mi+1 intersection must be used for a connection that has a VIAi <= 1 um (L1) away from a metal plate with height > 0.7 um (H1) and width > 0.7 um (W1)		
VIAx.R.7.2	At least 2 VIAi within the same Mi/Mi+1 intersection must be used for a connection that has a VIAi <= 2 um (L2) away from a metal plate with height > 2 um (H2) and width > 2 um (W2)		
VIAx.R.7.3	At least 2 VIAi within the same Mi/Mi+1 intersection must be used for a connection that has a VIAi <= 5 um (L3) away from a metal plate with height > 10 um (H3) and width > 3 um (W3)		

a.Note that this also applies to M1-VIA1



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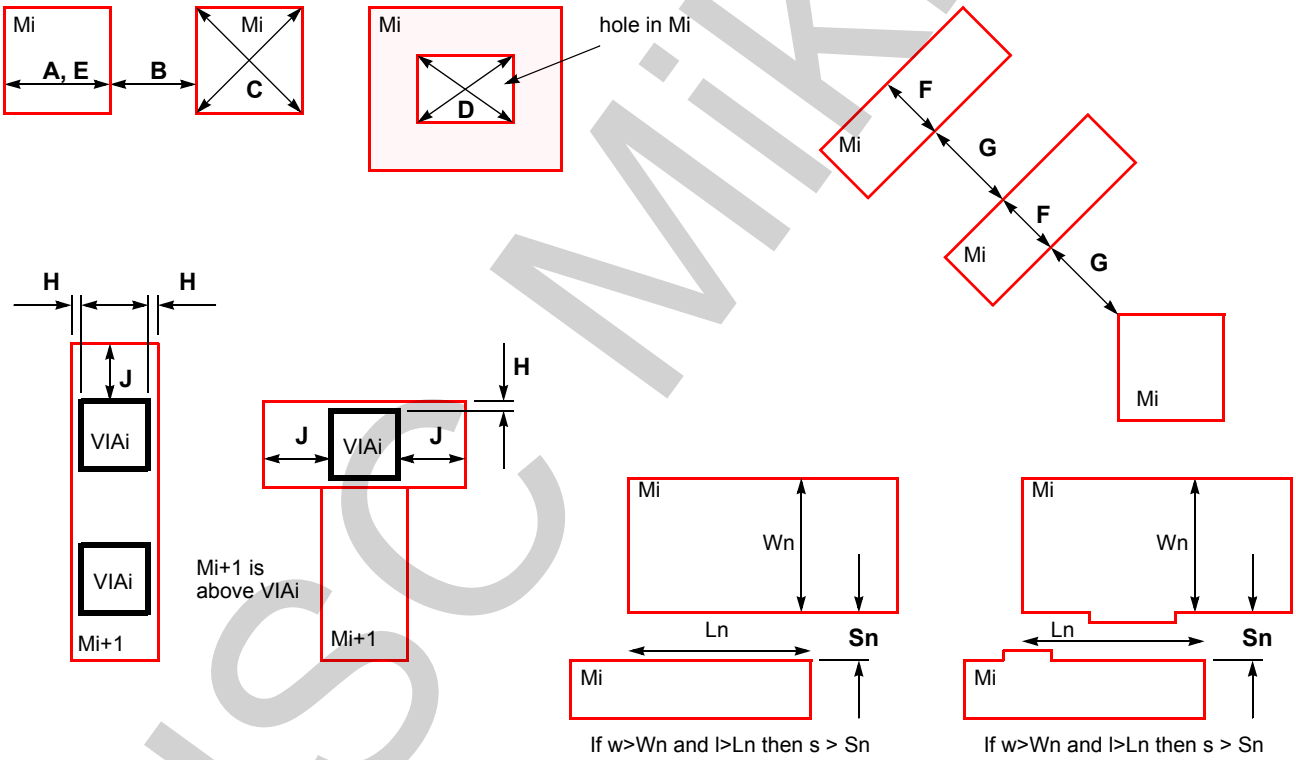
7.3.6.4 Thin Metal (Mx)

For a specification of Mi levels (i = 2, 3, 4, 5) to which the Mx rules do apply see §7.3.3.

Mx Design Rules (Thin Metal)			
Mx.W.1	Width	A	0.140
Mx.S.1	Space	B	0.140
Mx.A.1	Area	C	0.070
Mx.A.2	Enclosed area	D	0.200
Mx.W.2	Maximum Width	E	12.00
Mx.W.3	Width for 45° metal lines	F	0.190
Mx.S.2	Space for 45° metal lines	G	0.190
Mx.EN.1	Enclosure of VIAi-1 by Mi	H	0.005
Mx.EX.1	Extension on VIAi-1 by Mi on at least 2 opposite sides	J	0.050
Mx.S.3.1	Space if at least one metal line width is > 0.21 um (W1) and if the parallel metal run length (between both metals) > 0.52 um (L1)	S1	0.190
Mx.S.3.2	Space if at least one metal line width is > 1.50 um (W2) and if the parallel metal run length (between both metals) > 1.50 um (L2)	S2	0.500
Mx.S.3.4	Space if at least one metal line width is > 4.50 um (W4) and if the parallel metal run length (between both metals) > 4.50 um (L4)	S4	1.500



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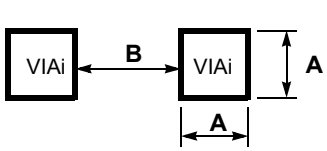
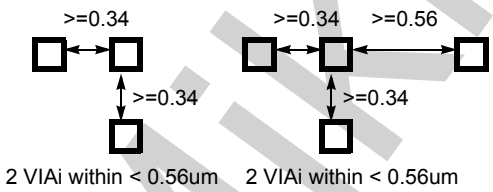
7.3.6.5 Large VIA (VIAn)

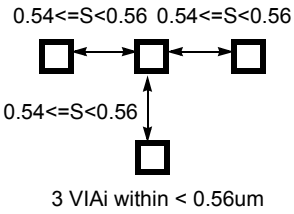
For a specification to which VIAi (i = 5 or 6) levels the VIAn rules do apply see §7.3.3.

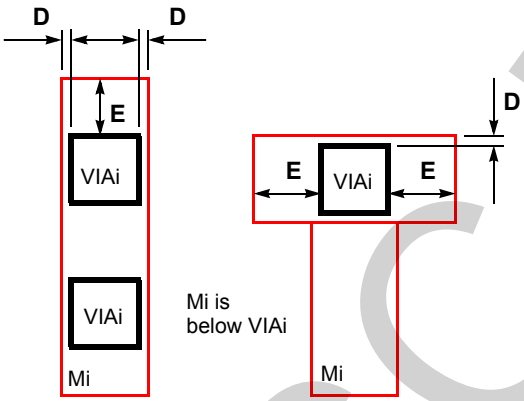
VIAn Design Rules (Large VIA)			
VIAn.W.1	Width (width = length, min = max)	A	0.360
VIAn.S.1	Space [a]	B	0.340
VIAn.S.2	Space to VIAi in an array (VIAi with 3 or more VIAi within < 0.56 um distance)	C	0.540
VIAn.EN.1	Enclosure of VIAi by Mi (Metal under VIAi) [b]	D	0.030
VIAn.EX.1	Mi (Metal under VIAi) Extension on VIAi on at least 2 opposite sides [b]	E	0.080
VIAn.R.1	45° rotated VIAi not allowed		
VIAn.R.2	Non-square VIAi (bar-shape) is not allowed except for seal ring		
VIAn.R.3	VIAi must be fully covered by metal below (Mi) and above (Mi+1)		
VIAn.R.4	At least 2 VIAi with space <= 1.7 um (S1) are required to connect Mi and Mi+1 when one of these 2 metals has width > 1.8 um (W1)		
VIAn.R.5	At least 2 VIAi within the same Mi/Mi+1 intersection must be used for a connection that has a VIAi <= 5 um (L2) away from a metal plate with height > 10 um (H2) and width > 3 um (W2)		

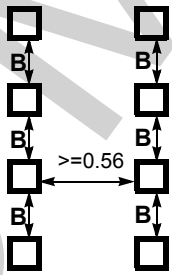
a.VIAn can be partially or fully stacked
b.Metal under VIAi is either Mx for thin metal under VIAi, or Mn for thick metal under VIAi.

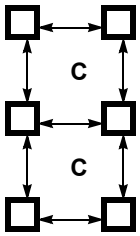


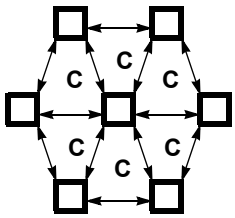


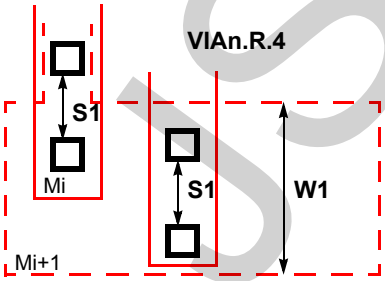


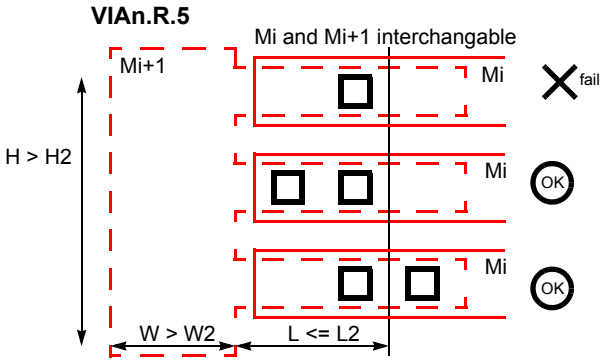












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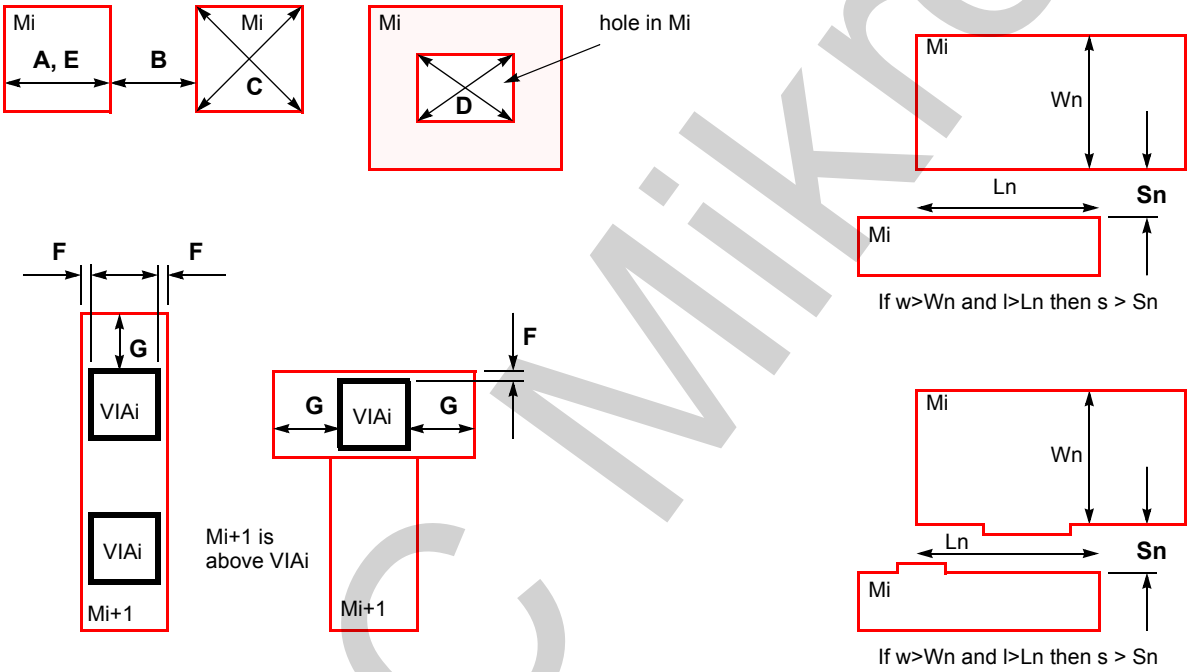
7.3.6.6 Thick Metal (Mn)

For a specification to which metal levels Mi (i = 6 or 7) the Mn rules do apply see §7.3.3.

Mn Design Rules (Thick metal: Metal n)			
Mn.W.1	Width	A	0.420
Mn.S.1	Space	B	0.420
Mn.A.1	Area	C	0.565
Mn.A.2	Enclosed area	D	0.565
Mn.W.2	Maximum width (Exclusion: Mtop under CB, CB;via)	E	12.00
Mn.EN.1	Enclosure of VIAi-1 by Mi	F	0.030
Mn.EX.1	Extension on VIAi-1 by Mi on at least 2 opposite sides	G	0.080
Mn.S.3.1	Space if at least one metal line width is > 1.50 um (W1) and if the parallel metal run length (between both metals) > 1.50 um (L1)	S1	0.500
Mn.S.3.3	Space if at least one metal line width is > 4.50 um (W3) and if the parallel metal run length (between both metals) > 4.50 um (L3)	S3	1.500



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7.3.7 FAR-BACK-END PROCESS DESIGN RULES

For standard applications such as simple wirebond pads, the usual approach is to use the CAD layer CB. This layer is used to derive the different required mask levels as follows:

- CB → PADOPEN (mask for opening in the glass encapsulation to provide access to the top metal)
- CB [upsized] → ALUCAP (mask for defining aluminum cap)
- CB → NITRIDE (mask for opening in nitride passivation)

For other applications (MIM, inductor, test-points, flip-chip, etc.), and to give maximum design flexibility for complex wirebond pads, CAD levels CB;via, AP, NITRIDE, and NITRIDE;bump are used to derive mask levels as follows:

- CB;via → PADOPEN (opening in the glass encapsulation to provide access to the top metal)
- AP → ALUCAP (aluminum cap)
- NITRIDE → NITRIDE (opening in the final passivation)
- NITRIDE;bump → NITRIDE (opening in the final passivation)

In CAD2MASK (N/A) the following operations are applied (simplified):

- PADOPEN = CB or CB;via
- ALUCAP = AP or CB [upsized]
- NITRIDE = CB or NITRIDE or NITRIDE;bump

In addition to the physical layers, a marker layer shall identify the purpose of the structure, for both LVS identification and for specific DRC. The following table describes which layers are required for each type of structure.

Layer use for the various structures

CAD Layers / Structures	Physical Layers							Marker Layers			
	Mtop	**CB**	**CB ,via**[a]	**AP**	**NITRIDE**	**NITRIDE;bump** (Bump Area)	**BOTMIM**[b]	**MKR;wb** (WireBond Area)	**MKR;tp**	**MKR;sealring**	**MKR;inddmy** (Inductor)
Bondpads (using CB)	x	x									
Bondpads (drawing each layer)	(x)		(x)	x	x			x			
Flip-chip pads	(x)		(x)	x		x					
Seal Ring	x	x								x	
Inductor	x		x	x							x
MIM Capacitor			x	x			x				
Alucap routing			x	x							

a.It is used as an opening in the encapsulation layer (first passivation)
b.Process Option MIM. The CAD layers BOTMIM and MKTOPMIM and corresponding masks are required.

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7.3.7.1 Copper Bondpad Opening (CB), Connecting Via from Mtop to AP (CB;via)

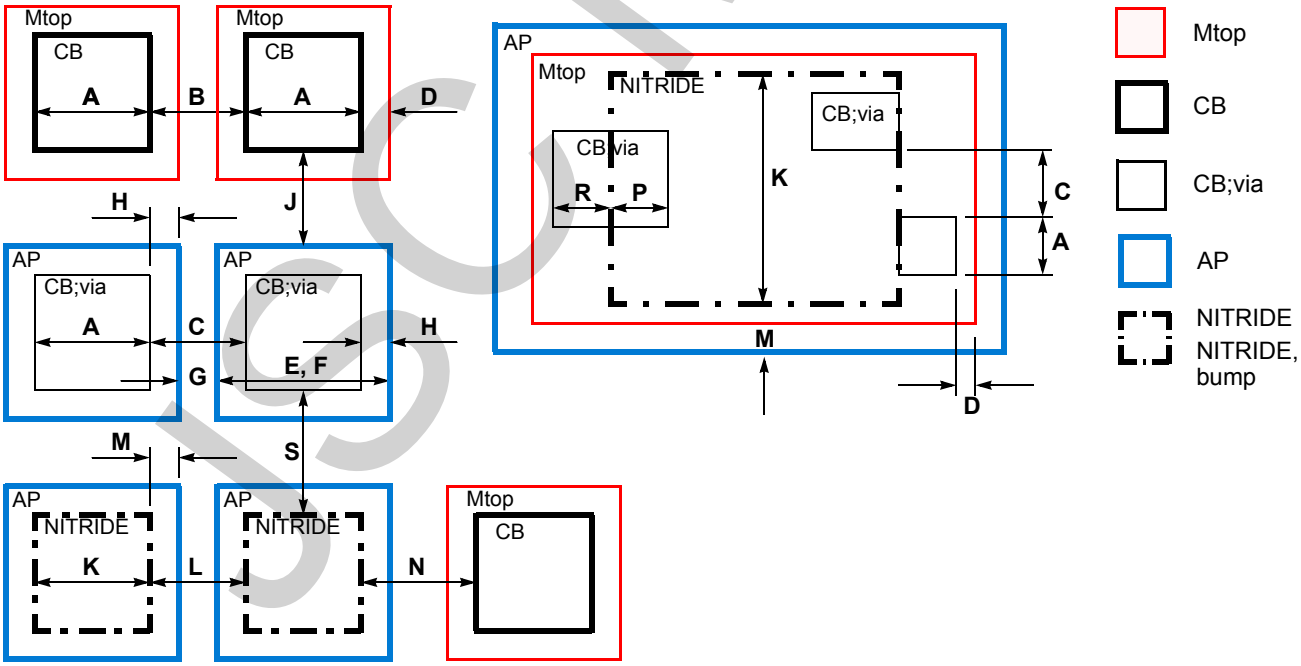
CB and CB;via Design Rules			
CB.W.1	{CB or CB;via} Width (except CB;via in MIM)	A	3.000
CB.S.1	CB Space	B	6.000
CB.S.2	CB;via Space (except CB;via in MIM)	C	2.000
CB.EN.1	{CB or CB;via} Enclosure by Mtop (Mtop must cover {CB or CB;via} except CB under MKR;sealring)	D	0.700
CB.R.1	CB must not interact with CB;via		

7.3.7.2 Aluminum Cap (AP)

AP Design Rules			
AP.W.1	AP Width (except in MIM)	E	3.000
AP.W.2	Maximum AP width (excluding AP under NITRIDE or INDDMY or NITRIDE;bump)	F	35.000
AP.S.1	AP Space	G	2.000
AP.EN.1	AP Enclosure of CB;via (AP must cover CB;via)	H	0.700
AP.D.1	AP Distance to CB (AP must not interact with CB)	J	4.000

7.3.7.3 Nitride Passivation (NITRIDE)

NITRIDE and NITRIDE;bump Design Rules			
NIT.W.1	{NITRIDE or NITRIDE;bump} Width	K	2.000
NIT.S.1	{NITRIDE or NITRIDE;bump} Space	L	2.000
NIT.EN.1	{NITRIDE or NITRIDE;bump} Enclosure by AP (must be fully covered by AP)	M	1.000
NIT.D.1	{NITRIDE or NITRIDE;bump} Distance to CB (must not interact with CB)	N	4.000
NIT.OL.1	CB;via Overlap of NITRIDE (align if less)	P	2.000
NIT.EX.1	CB;via Extension on NITRIDE (align if less)	R	2.000
NIT.R.2	NITRIDE must be fully covered by a marker layer {MKR;wb or MKR;tp}		



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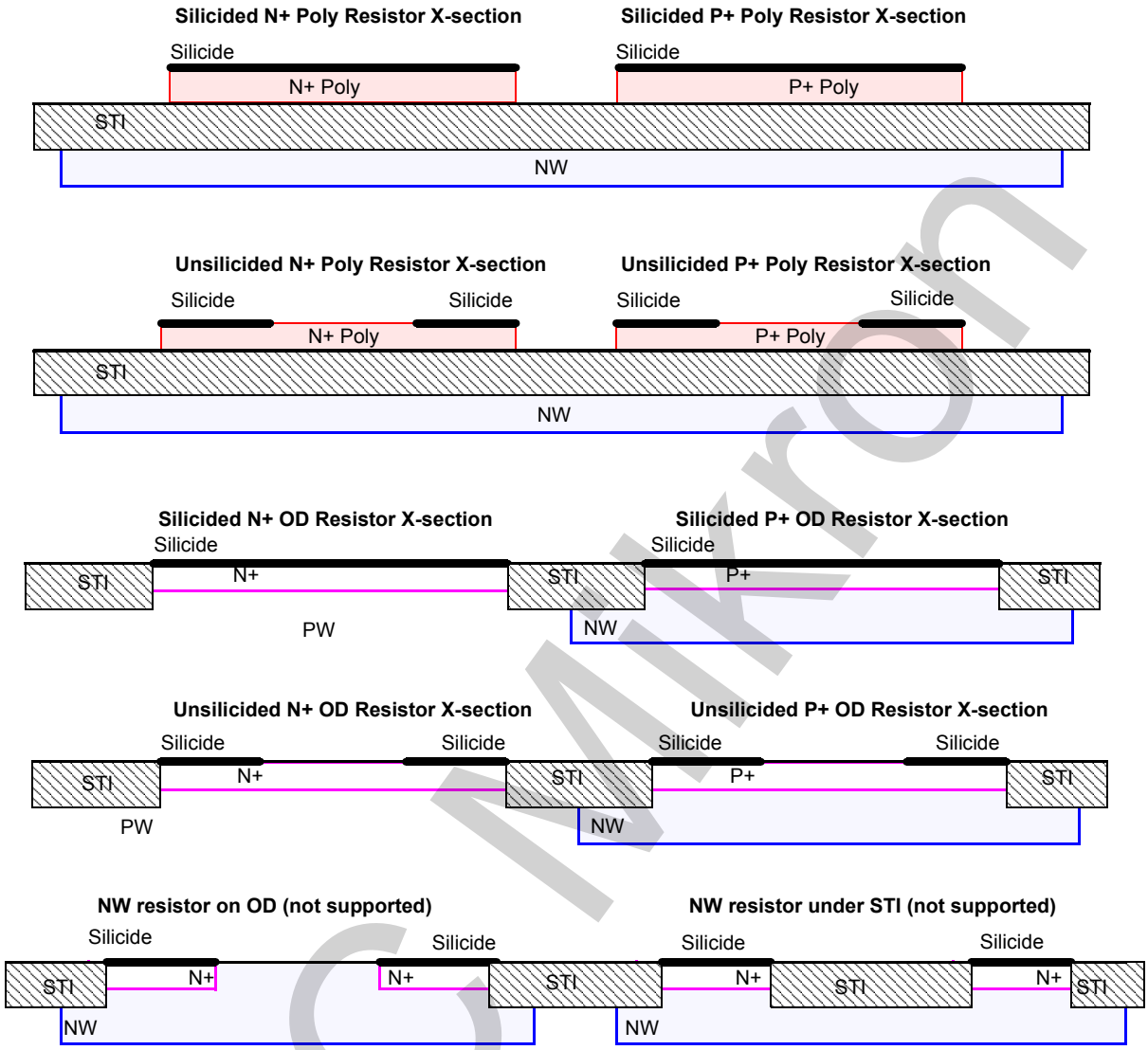
7.3.8 DEVICE SPECIFIC DESIGN RULES

7.3.8.1 Resistors (POLY and OD, N+ and P+, Unsilicided and Silicided)



These devices do not require any additional mask levels. They all require the CAD layer RH which is used in CAD2MASK (N/A) to protect them from all LDD implants. Routing poly layout retargeting is blocked from poly resistors (ADCS # 7771145 CMOS090 LAYOUT RETARGETING DURING RET)

They can be built in the following flavors (exclusively one per row):

- either Poly or OD, according to the layer in which they are fabricated
- either N+ or P+, as to the doping type
- either unsilicided or silicided, relying in the presence or not of the silicidation protection layer RPO

As for the dimensions, the drawn width is defined by the PO/OD width. The drawn length is defined as:

- the distance between the CO for silicided resistors
- the length of the resulting shape of the intersection of the RPO layer and the PO/OD for unsilicided resistors
- for spice accuracy:
  - — do not dog-bone the resistor at the transition from head to body
  - — put OD/PO resistor among dense pattern
- for maximum current density see §7.7.3

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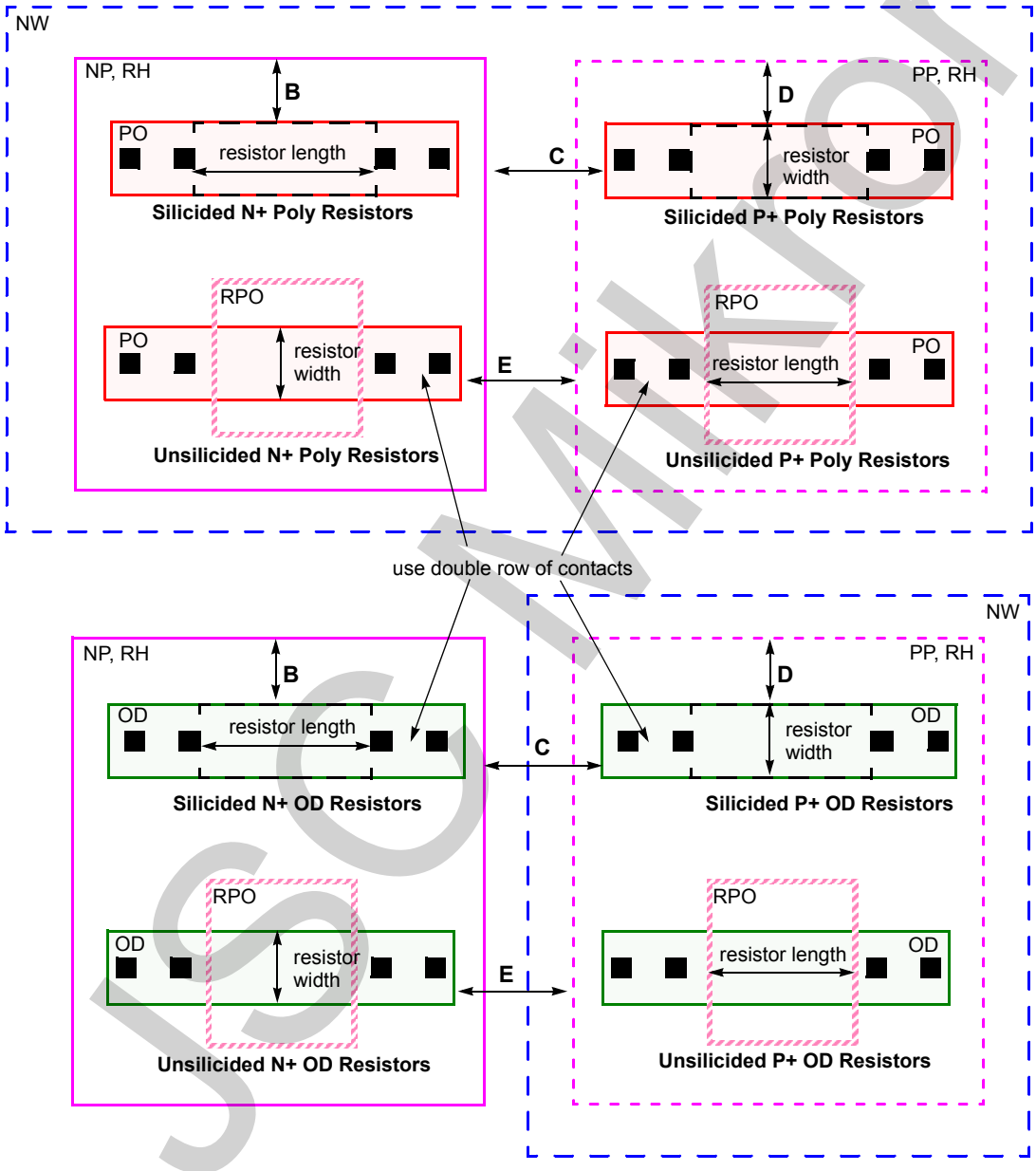
Poly/OD Resistor Design Rules			
RES.W.1	PO or OD width of a PO/OD resistor (minimum resistor width) [a]	A	0.240
RES.EN.1	NP Enclosure of PO/OD of an N+ resistor (N+ resistor must be completely covered by NP)	B	0.200
RES.D.1	NP Distance to PO/OD of a P+ resistor (P+ resistor must not interact with NP)	C	0.200
RES.EN.2	PP Enclosure of PO/OD of a P+ resistor (P+ resistor must be completely covered by PP)	D	0.200
RES.D.2	PP Distance to PO/OD of an N+ resistor (N+ resistor must not interact with PP)	E	0.200
RES.R.1	N+ or P+ poly resistor is not allowed on OD (PO of poly resistor must not intersect OD)		

a.It is recommended to use at least 0.060 PO Enclosure of CO.



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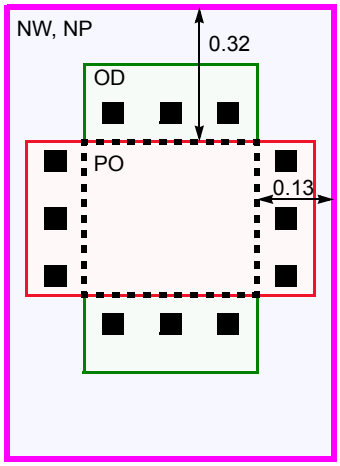
7.3.8.2 MOS Varactors

MOS varactors are gate capacitors where the doping type of PO has the same polarity as the well doping in the underlying OD. MOS varactors follow the general design rules (§7.3.5, §7.3.6) but are excluded from the following design rules: PO.R.3, PO.R.4.

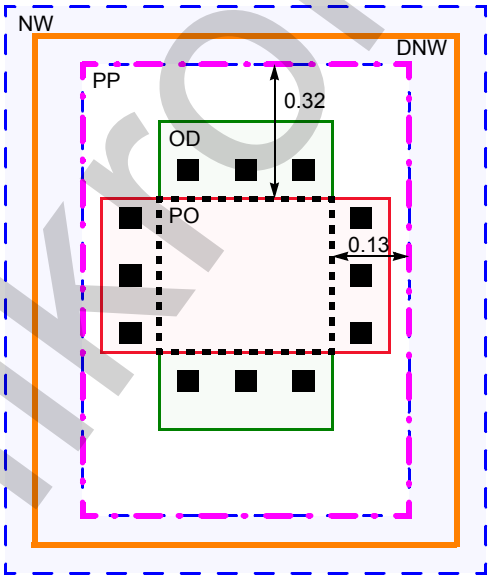
MOS Varactor Design Rule			
MVAR.R.1	No 90° corner of OD under PO		
MVAR.R.5	NP/PP must fully cover {((Gate of Varactor) sizing 0.19) and OD) sizing 0.13}[a]	A	

a.In practice, this rule can be seen as an enclosure of the Gate at 0.19um and an extension in the direction of the OD at 0.32um.

Example: N+PO / NW OD Capacitor



Example P+PO / PW OD Capacitor in DNW



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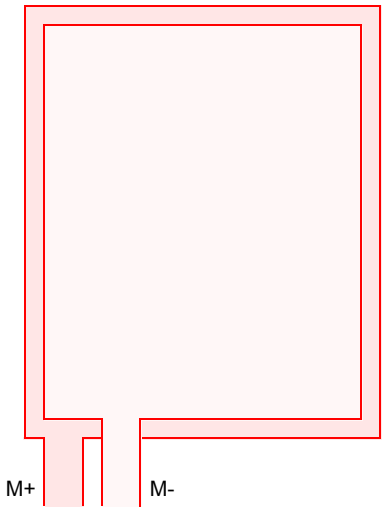
7.3.8.3 Metal Plate Capacitors

The metal plate capacitors (cmsbe, cm1m2, etc.) are based on the vertical coupling capacitance between stacked metal plates separated by the inter-level dielectric. These devices do not require any additional mask levels. Metal plate capacitors follow the general design rules (§7.3.6) and are not excluded from any of these design rules.

The stacked metal plate capacitor (cmsbe) is made out of a configurable number of metal levels and is designed such that when used in a repeated scheme it will still follow the metal density design rules. For electrical targets see §7.8.2.1.

Example layout : metal plate capacitor



Example X-section: Stacked metal plate capacitor

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7.3.8.4 Fringe Capacitor Design Rules (FMOM)

The fringe capacitor (CFR, also known as FMOM capacitor) is based on the lateral coupling capacitance between parallel metal lines separated by the intra-level dielectric. The device does not require any additional mask levels. The cfrm1m5 capacitor is using 5 metal levels: M1 to M5.

The cfrm1m5 capacitor is made at each metal level from two interdigitated combs. The combs are stacked and aligned from M1 to M5. A bus connects the fingers for both combs at each level, and the levels are connected at the bus using VIA1 to VIA4. The capacitor is placed in an NWell with N+ OD and PO stripes and is covered by M6 stripes.

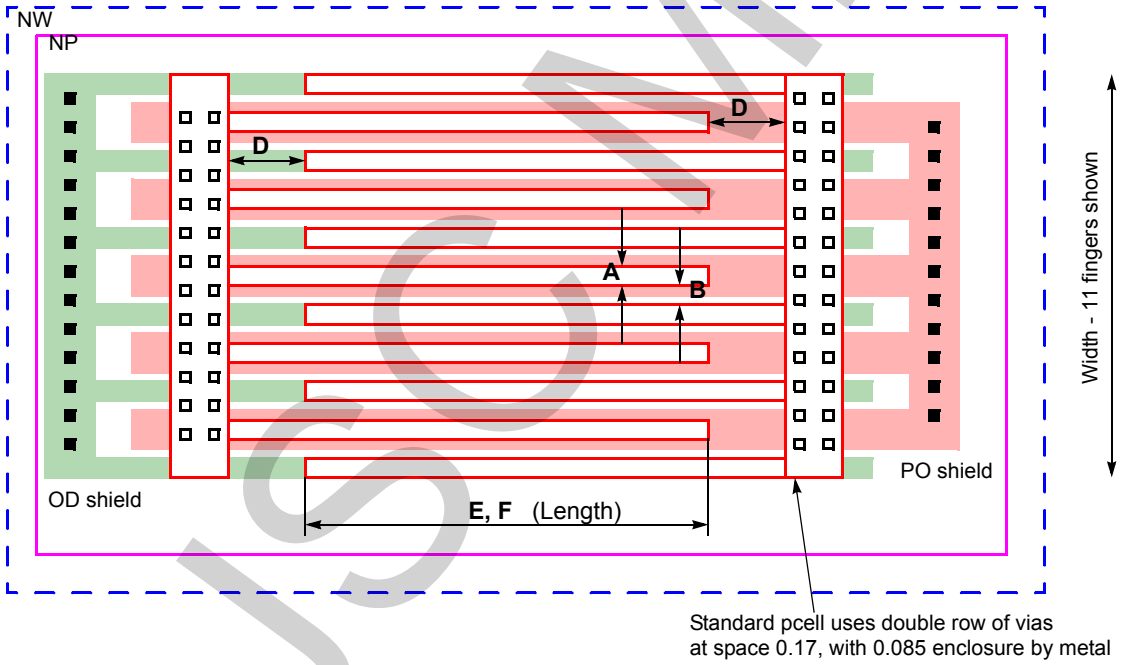
For electrical targets see (§7.8.2.1). It is recommended to use an uneven number of fingers. It is strongly advised to follow the recommended aspect ratio (Length/Width) = 2

The maximum finger length and maximum number of fingers must be chosen such that capacitance does not go beyond the authorized capacitance range. A P-cell is available in the design kit and shall be used.

a) M1-M5 comb P-cell design

Typical Fringe Capacitor Construction Values (FMOM, Rules for M1-M5 combs)			
FMOM.W.1	Metal Width of capacitor finger (min = max)	A	0.180
FMOM.S.1	Metal Space between capacitor finger (min = max)	B	0.180
FMOM.S.2	Metal Space between metal bus and metal finger	D	1.000
FMOM.L.1	Minimum finger length	E	10.00
FMOM.L.2	Maximum finger length [a]	F	200.0
FMOM.R.1	Minimum finger number		11

a.The rule OD.L.2 (maximum length of OD) is excepted for the OD shield in the fringe capacitor



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b) PO, OD and M6 design

The capacitor is placed in an NWell with N+ OD and N+ PO stripes and is covered by M6 stripes. These stripes enable to meet density rules with known impact on parasitic capacitance that are included in the device model.

- The N+ PO shield is made of PO stripes on field oxide, placed in parallel direction underneath the fingers of comb #1. The stripes are connected on the side by a parallel PO and M1 bus.
- The N+ OD shield is made of OD stripes, placed between the PO stripes, i.e. in parallel direction underneath the fingers of comb #2. The OD stripes are connected on the side by a parallel N+ OD and M1 bus.
- The M6 stripes are perpendicular to the comb fingers and use minimum Mn design rules.

Typical Fringe Capacitor Construction Values (FMOM, Rules for PO, OD and M6)			
FMOM.W.11	PO Width of poly stripes (min = max)	A	0.340
FMOM.W.12	OD Width of N+ OD stripes (min = max)	B	0.180
FMOM.S.12	M1-M6 shield bus Space to FMOM Metal	D	0.540
FMOM.D.11	PO Distance to OD for shield stripes	E	0.100

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7.3.8.5 Bipolar Transistor Design Rules

Bipolar transistors (N+ / PWell / Deep NWell and P+ / NWell / P-substrate) are only allowed in two predefined sizes: emitter size 2x2um^2 and emitter size 5x5um^2. The entire device needs to be covered with an MKR;BJT layer which is used to blocks LDD and halo implants from the device.
The only versions of these two devices that are supported, are those distributed within the common design kit.

Bipolar Transistor Design Rules			
BIP.R.2	OD (Emitter) of bipolar transistor must be covered by MKR;BJTDMY		

Supported devices:

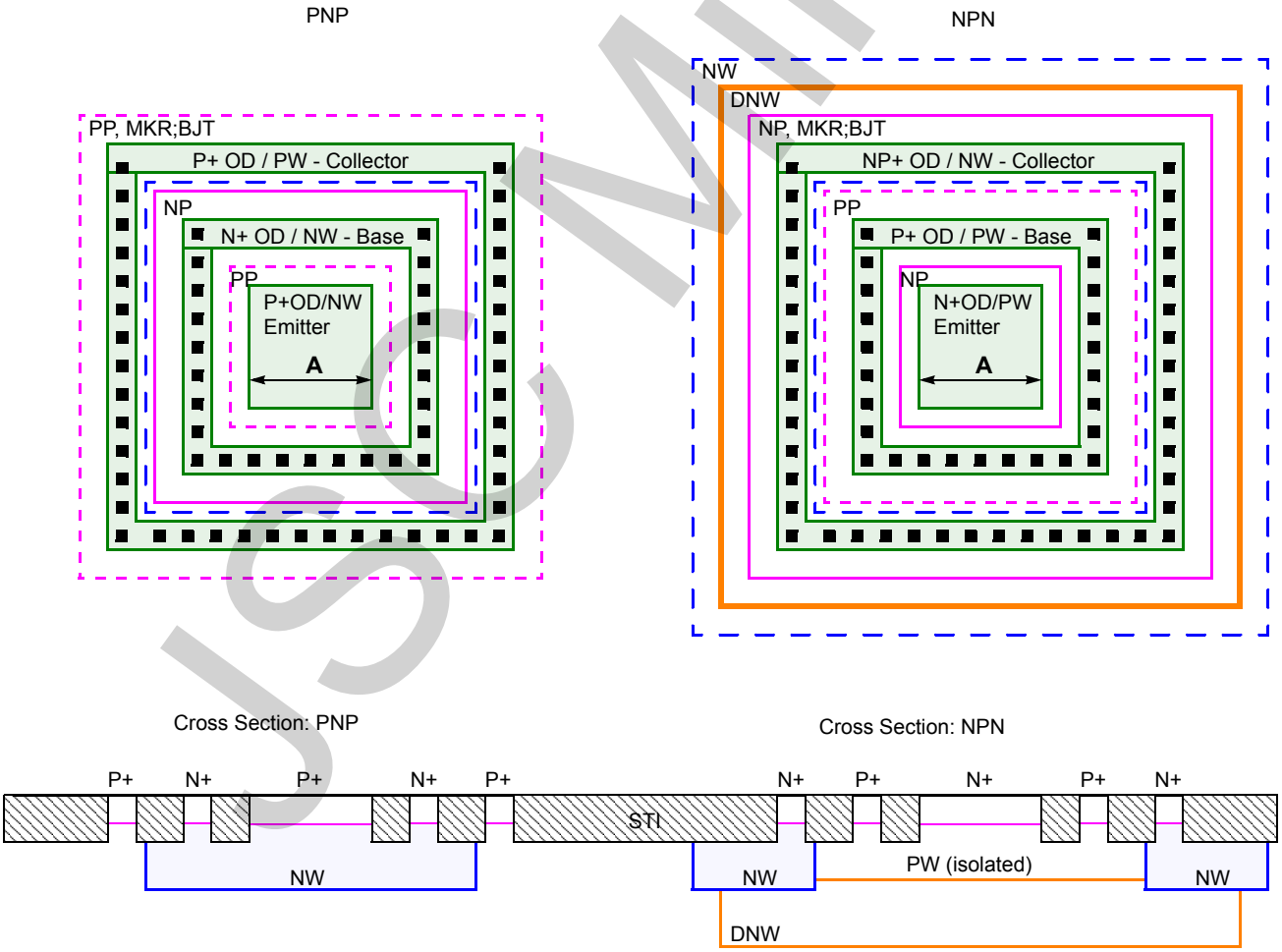
Only 4 bipolar transistors (for band gap reference) are supported in the common design kit:

- NPN and PNP with emitter size 2x2um^2
- NPN and PNP with emitter size 5x5um^2

For the supported bipolars MKR;BJT is drawn in the following manner:

- line-on-line with outermost NP edge for NPN (collector ring)
- line-on-line with outermost PP edge for PNP (collector ring)
- MKR;BJT of the PNP is not intersecting DNW
- MKR;BJT of the NPN is fully covered by DNW
- MKR;BJT does not intersect OD2.

Layout/X-section of the supported devices:



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7.3.8.6 High Density Memories

7.3.8.6.1 Bicell Reference Library

The table below list the authorized High Density bitcells in CMOS090. They are provided through Bitcell Reference Libraries (BRL), for which precise usage conditions exists (see BRL usage policy below).

CMOS090 BITCELL OFFER				
Size		Type	Type	Reference Library Name
1.150um²		SRAM Single-Port	HD	memcellhd_c090
2.300um²		SRAM Dual-Port	HD	memcellhd_c090
1.980um²	SPSmall	SRAM Single-Port	STD	memcellhd_c090
0.190um²	ROM Via (ROMV)	ROM	STD	memcellhd_c090

Bitcell Reference Libraries (BRL) usage policy rules includes:

- DRC filters are only allowed in cells from BRL.
- The only cells authorized for the construction of the complete memory array (including all boundary cells and strap cells) are those from the BRL.
- Only a limited list of leaf cells is allowed for usage, this list is in the /doc directory of the BRL: “brl_name”_authorized_cells
- It is forbidden to add, modify, copy or flatten any cell from a BRL, including waiver cells (DRC filters).
- No changes are allowed on any cell from any BRL, even by DRC correct additions of some shape in existing layer, even if it is drawn at a different hierarchy level. Exceptions to this rule is: For SRAM: on M2X and M3X layers for which DRC correct addition of shapes is allowed (removal of any shape is forbidden, complete or partial) at a higher hierarchy level.
- All metal layers that are not used in the instantiated cells from the BRL can be freely drawn on top of these cells.

.All HD SRAM cells that are not compliant with the general design rules (§7.3.4) are drawn in layers with the special “hd” purpose that is mapped to datatype 30 for the respective drawing layer. The design rules used for these HD SRAM cells are specific to these particular layouts and are not allowed for other cells.

A SRM layer covers these cells, as well as the entire memory array including straps and dummy cells. The VTN-CELL implant mask is built from the logical operation {SRM .not. NW}. Thus the SRM layer needs to comply to the following rules:

SRM Design Rules			
SRM.W.1	Width (if error shape intersects OD)		0.280
SRM.S.1	Space (if error shape intersects OD)		0.280
SRM.EN.1	Enclosure of OD of MOS		0.070
SRM.EN.2	Enclosure of Gate		0.220
SRM.D.1	Distance to OD of MOS not using SRM		0.070
SRM.D.2	Distance to Gate not using SRM		0.170
SRM.EX.1	SRM Extension on NW (if error shape intersects OD. Align if less)		0.280

Marker MKR;sramdmy may be used in 3rd party SRAM that do not use the memory cell reference library.

SRAM Marker Restrictions			
MSRM.R.1	MKR;sramdmy must intersect {Gate within SRM} (cannot use marker on non-SRAM circuit)		

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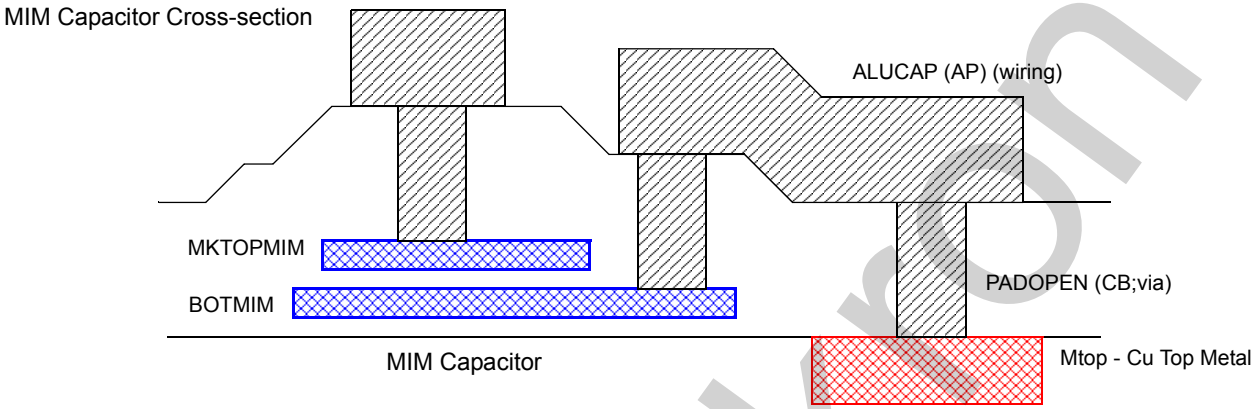
7.3.8.7 MIM Capacitor

The MIM capacitor is a metal-dielectric-metal capacitor placed between top-metal and Alucap. The main features of this device are: thin-aluminium electrodes with a low plate resistance, a very low parasitic capacitance to the substrate, and high linearity. The MIM capacitor is especially suited for analog and RF applications.

The device requires two additional mask levels: MKTOPMIM to define the top plate and BOTMIM to define the bottom plate of the MIM capacitor. All the connections to the capacitor are made in ALUCAP metal (AP CAD layer) through the PADOPEN “vias” (CB;via CAD layer). No vias are possible underneath the BOTMIM level.



7.3.8.7.1 Design Rules for MIM

MIM Capacitor Design Rules			
BOTMIM Rules			
CBM.W.1	BOTMIM Width	A	4.500
CBM.S.1	BOTMIM Space	B	2.500
CBM.EN.1	BOTMIM Enclosure of CB;via	C	0.300
CBM.D.1	BOTMIM Distance to CB;via	D	2.000
CBM.D.2	BOTMIM Distance to Mtop on a different net (not allowed to interact)	E	2.000
CBM.W.2	Maximum Mtop width (including Mtop;dummy) under BOTMIM		0.900
MKTOPMIM Rules			
CTM.W.1	MKTOPMIM Width	F	3.500
CTM.S.1	MKTOPMIM Space	G	3.500
CTM.A.1	Maximum MKTOPMIM Area		20000.
CTM.DEN.1	Minimum MKTOPMIM density within a window that is 500um larger than the MIM capacitor (MKTOPMIM)		10%
CTM.DEN.2	Minimum Mtop density under {BOTMIM upsize 25.00} [a]		10%
CTM.DEN.3	Minimum Mtop density in the region defined by {(BOTMIM upsize 25.00) .not. BOTMIM}		20%
CTM.EN.1	MKTOPMIM Enclosure by BOTMIM	J	0.500
CTM.EN.2	MKTOPMIM Enclosure of CB;via	K	0.500
CTM.D.1	MKTOPMIM Distance to CB;via	L	0.700
CTM.D.2	MKTOPMIM Distance to AP on different net (AP must not intersect MKTOPMIM on different net)		0.600
CTM.R.1	MKTOPMIM must be completely covered by BOTMIM		

a.Area under BOTMIM is excluded from regular minimum density rule Mn.R.1 and is allowed to have lower density as defined by CTM.DEN.2. The region immediately surrounding the MIM must fulfill the minimum density rule to provide a density transition zone (CTM.DEN.3).

CB;via Rules for MIM			
C-CBV.W.1	CB;via Width (CB;via that connect AP to BOTMIM or MKTOPMIM, and for any CB;via on an AP shape that also has CB;via connecting to BOTMIM or MKTOPMIM) (width=length, min=max)	M	1.000
C-CBV.S.1	CB;via Space (CB;via that connect AP to BOTMIM or MKTOPMIM, and for any CB;via on an AP shape that also has CB;via connecting to BOTMIM or MKTOPMIM)	N	1.000

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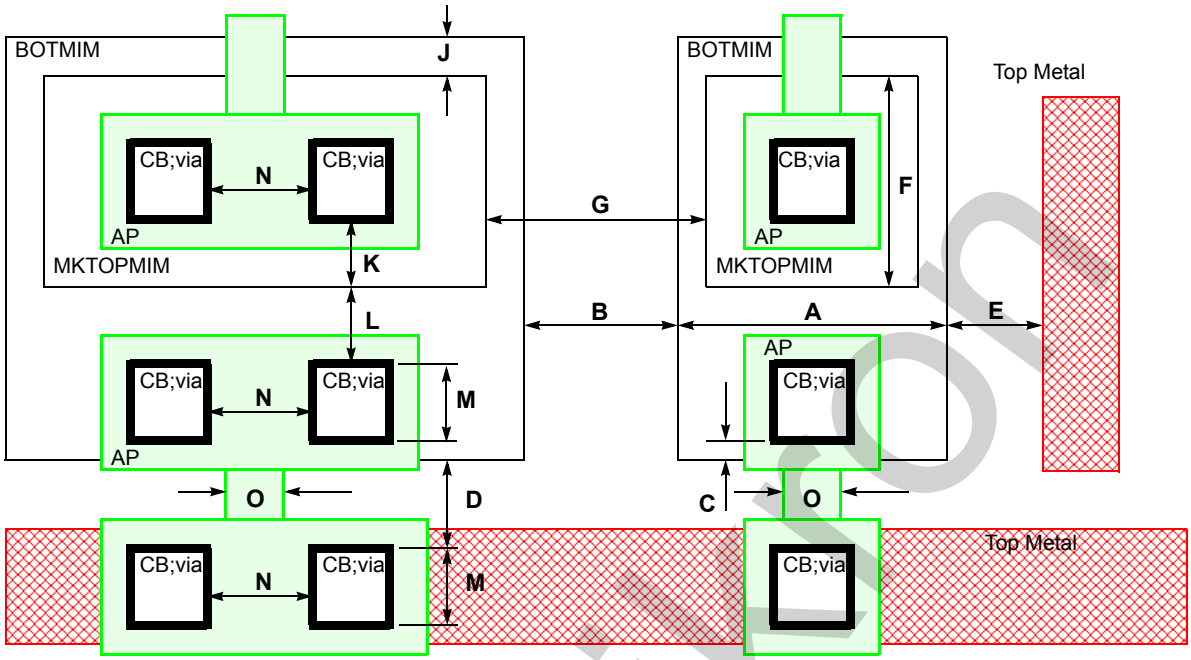
AP Rules for MIM			
C-AP.W.1	AP Width (any AP shape that has CB;via connecting it to BOTMIM or MKTOPMIM)	O	1.000



7.3.8.7.2 Antenna Design Rules for MIM Capacitors

The most important contributions to charging of the MIM capacitor are the PADOPEN (CB;via) etch followed by the ALUCAP (AP) etch. Charging effects can therefore be limited by:

- limiting the number of vias on the MIM plates
- limiting the length of the ALUCAP lines connected to the MIM plates
- keeping the ALUCAP length to each MIM plate identical
- having an identical number of PADOPEN vias to the Top- and Bottom MIM plates
- the use of small capacitors

These rules are based on the model of a dielectric with a “weak point.” The probability of getting a weak point increases with the capacitor area. As the MIM capacitors increase in size the effects of charging must be minimized by proper design. It is recommended to use several capacitors in parallel rather than one large capacitor. The following table summarizes the mandatory (CMIM.ANT.2, 3, 5, 6, 8, 9) and robust or recommended (CMIM.ANT.4, 7, 10) design rules.

Antenna Design Rules for MIM Capacitor			
CMIM.ANT.2	For any BOTMIM plate, the number of CB;via connected to the common BOTMIM plate must be the sum of the number of CB;via connected to MKTOPMIM plate.		
CMIM.ANT.3	The two plates must be simultaneously either floating (it must be the case at BOTMIM and MKTOPMIM levels) or non floating (it is the general case at AP level) [a]		
CMIM.ANT.5a	Maximum number of CB;via connected to each MIM capacitor plate if area < 200 um2		4
CMIM.ANT.5b	Maximum number of CB;via connected to each MIM capacitor plate if 200 um2 <= area < 500 um2		10
CMIM.ANT.6	Maximum number of CB;via connected to each MIM capacitor plate if area >= 500 um2		30
CMIM.ANT.8	Maximum drawn ratio of AP sidewall area to the MIM capacitor area connected directly to it [b].		5000
CMIM.ANT.9	Maximum AP Antenna ratio [c]		400

a.Any node connected to a N+OD or P+OD (transistor terminal, diode or well tie) directly through metal or through poly resistors is NOT floating.
b.AP considered thickness is 1.0um
c.The antenna ratio is defined as the ratio of the AP area to the MIM capacitor area, determined as the MKTOPMIM area, calculated following the gate-oxide-protection methodology, as referred in §7.5.2.2.

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Antenna Guidelines for MIM Capacitor			
CMIM.ANT.4	It is recommended to protect capacitor against antenna effect by connecting simultaneously the two capacitors plate to a diode at AP level.		
CMIM.ANT.7	If AP connected to the plates of the capacitor is not connected to a diode, the length of the two AP connections shell be minimized and if possible identical		
CMIM.ANT.10	The AP connection to each MIM plate must be, if possible, identical		

7.3.8.7.3 MIM Pattern Density Dummy Fill Procedure

In order to fulfill the minimum density requirement CTM.DEN.1, dummy shapes (BOTMIM;dummy, MKTOP-MIM;dummy) need to be inserted according to the following guidelines.

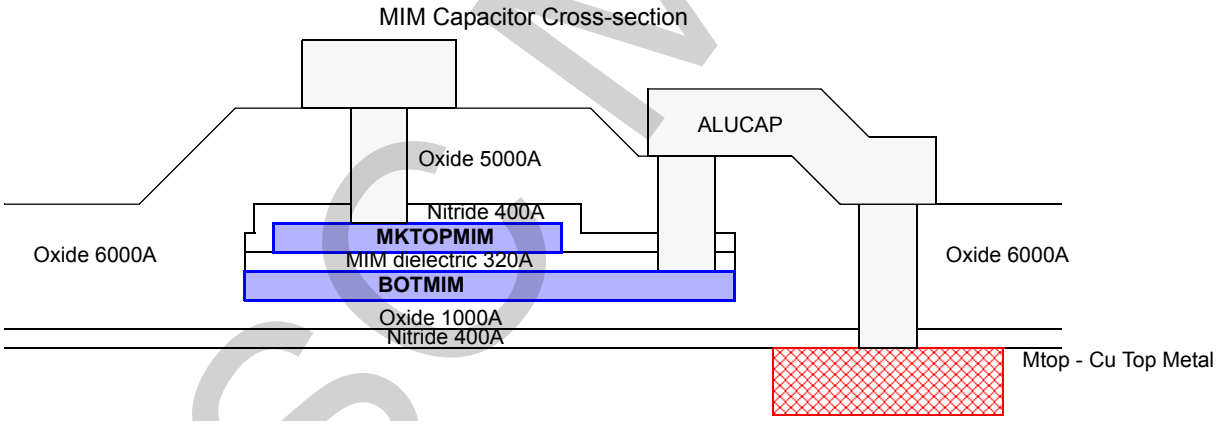
BOTMIM and TOPMIM Dummy Fill Guidelines			
DCBM.R.1	BOTMIM;dummy must completely cover MKTOPMIM;dummy [a]		
DCBM.R.2	BOTMIM;dummy must not intersect Mtop (drawn metal) [b]		
DCBM.W.1	BOTMIM;dummy Width		4.500
DCBM.S.1	BOTMIM;dummy Space		2.500

a.MKTOPMIM;dummy shall be equal to {BOTMIM;dummy undersized by 0.5um/side}.
b.Mtop;dummy under BOTMIM is allowed.

Impact of MIM layers on other dummy generation routines and density rules (§7.5.7.3):

- All dummies but Mtop shall be generated under BOTMIM (see §7.5.7.3)
- Mtop;dummy shall not be generated under edges of the capacitor (see §7.5.7.3)
- Areas under BOTMIM are excluded from Mtop minimum density rule, but are not excluded from density checks on other levels.

7.3.8.7.4 MIM Process and Electrical Parameters



CONDUCTORS AND DIELECTRICS				
Layers (for MIM)		Thick (A)	Var (A)	k
Modified Encapsulation (§7.7.1)	Oxide	5000	500	4.2
Above MIM top plate (conformal)	Nitride	400	40	8.1
MIM top plate	Metal	1900	190	-
Between MIM top and bottom plates	Nitride	320	32	7.25
MIM bottom plate	Metal	1900	190	-
Below MIM bottom plate	Oxide	1000	100	4.2

SHEET RESISTANCES				
Layer (from bottom to top)	MIN	TYP	MAX	
MIM bottom plate	230	300	370	mOhm/sq
MIM top plate	160	230	300	mOhm/sq

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SHEET RESISTANCES				
Layer (from bottom to top)	**MIN**	**TYP**	**MAX**	
ALUCAP		see §7.7.3		mOhm/sq

CONTACT RESISTANCES				
Contact type	**MIN**	**TYP**	**MAX**	**UNIT**
CB;via 1umx1um		see §7.7.4		Ohm

MIM ELECTRICAL PARAMETERS				
Parameter	**MIN**	**TYP**	**MAX**	**UNIT**
Capacitance	1.7	2.0	2.3	fF/um2
Matching		1.0		%.sqrt(fF)
Voltage coeff (CV1)		-30		ppm/V
Leakage Current			<10	nA/cm2
Breakdown Voltage	>10			V

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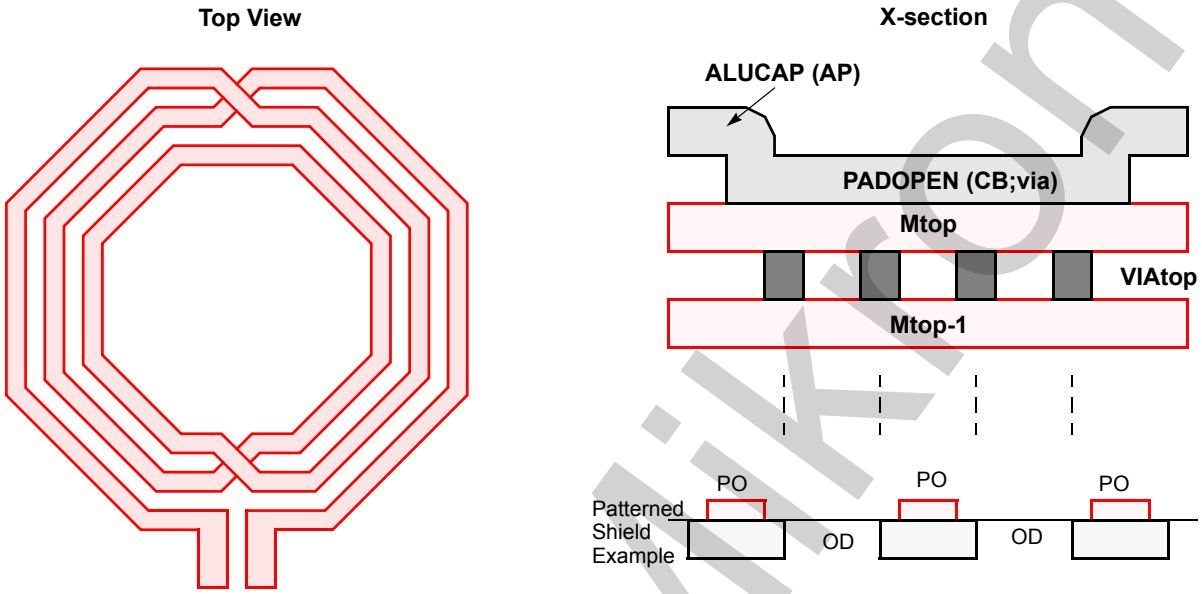
7.3.8.8 Inductors

Inductors are realized by stacking the at last two (or more) copper metal levels available in the core CMOS090 process. The Alucap level (design level AP) is used to further reduce the coil resistance. A trench at PADOPEN (CB;via design level) connects the Alucap to the top-metal copper levels. The inductor coil is covered with an MKR;inddmy marker layer for: DRC and LVS verification and to avoid dummy generation on OD, PO, M1, Mx, Mn and AP.

Inductor layouts shall always include at least: Mtop+Mtop-1, the use of additional AP or Mtop-2 metal levels to reduce the series resistance is allowed.



7.3.8.8.1 Design Rules for Inductors

Inductor Design Rules			
I-Mn.W.1	Minimum Metal Width (applicable to all Mn, Mx drawing levels within MKR;inddmy: coil, connectors and center tab, but not to the dummies, and not to M1)	A	1.500
I-Mn.S.1	Minimum Metal Space (applicable to all Mn, Mx drawing levels within MKR;inddmy: coil, connectors and center tab, but not to the dummies, and not to M1 and M2)	B	1.500
I-AP.W.1	Maximum AP width within INDDMY		60.000

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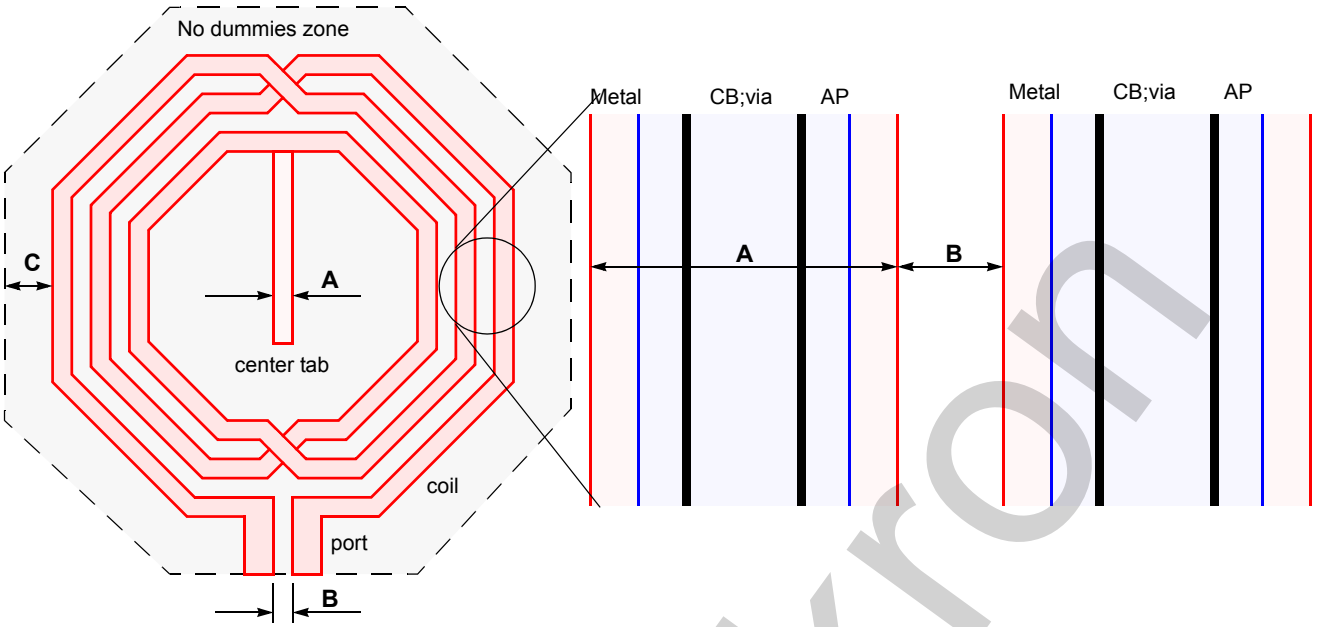

Marker and Dummy Requirements for Inductor

MKR;inddmy must be present to identify the inductor structure. The MKR;inddmy is used as follows:

- it covers the complete inductor structure including a mandatory density transition ring.
- it blocks the automated dummy generation
- it excludes the all metal levels (Mn, Mx, M1) from the lower limit local density checks (M1.R.2, Mx.R.1, Mn.R.1) if the check box interacts with MKR;inddmy.

As automated dummy generation and density checks are excluded from a region defined by MKR;inddmy, it is critical that the inductor design contains its own dummies:

- A density transition ring is necessary to reduce the impact of the low metal density in the inductor on surrounding circuitry
- The zone interior to the coils shall be filled with dummies
- Avoid having large empty areas between the coil and the density transition ring. In particular, the dummies from the density transition ring should be placed not further than 20 µm from the coil (distance A).
- Use an homogeneous density (target 25%) inside the density transition ring. It is highly recommended to use the 3µm x 3µm dummies at 3µm space

If no ground shield is used, the following features can be used to generate an OD;dummy pattern with minimum impact on parasitics: OD;dummy under the inductor coil can be covered with RPO to block silicidation.

Inductor Surrounding Area Design Rules (Density Transition Ring)			
I-DUM.D.1	Minimum Metal;dummy Distance to Metal [a]	C	13.000
I-DUM.DEN.1	Density-Transition Ring minimum density (the ring must contain dummies, and also may contain metal to connect the inductors). The density transition ring is defined as the 18um (W) wide ring inside coincident with MKR;inddmy.		20%
I-DUM.DEN.2	Minimum Metal Density within MKR;inddmy		5%

a.DRC verifies this distance within the same metal level only. Designs shall not place dummies on under the coil of the inductor.

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7.3.8.9 POLY/GO2/WELL Capacitances

7.3.8.9.1 N+POLY/NWELLGO2 Capacitor

This capacitor is a MOS capacitance varactor, realized with N+GO2 active area and N+ Poly in a NWELLGO2 (NWELL .AND. GO2). This device is using GO2 oxide. This device requires no additional mask.

7.3.8.9.2 P+POLY/PWELLGO2 Capacitor

This capacitor is a natural MOS capacitance, realized with P+GO2 active area and P+ Poly in a PWELLGO2 (GO2 .NOT. NWELL). This device is using GO2 oxide. This device requires no additional mask.

7.3.8.9.3 Antenna Rules

The probability of getting a weak point in the gate oxide is increasing as the gate oxide area is increasing. As the capacitors are using large areas, the effects of charging must be minimized by a proper design. In order to minimize the charging at contact etch, the number of contacts on the POLY plate area must be minimized; the rules given hereafter are acceptable for the capacitor access resistance.

S : Capacitor Area

BECA_m : Back-End Cumulative Area connected to the capacitor

BECA_via : Vias Cumulative Area connected to the capacitor

The unit used for areas is µm²

Antenna Design Rules		
CGO2.A.1	Maximum POLY area per capacitor	1000
CGO2.ANT.1	If BECA_m > 35000 µm², Diode Area >	(BECA_m-35000)/500
CGO2.ANT.2	If BECA_via > 900 µm², Diode Area >	(BECA_via-900)/200

7.3.8.9.4 Specific recommended rules for decoupling capacitors.

With the improved speed of the products and the increasing number of gates able to switch at the same time, the need for decoupling capacitors is increasing. These capacitors are usually made with gate oxide; this extra oxide area is increasing the risk of yield loss and reliability. So the following rules must be applied (note: these rules are not checked in the DRC):

Recommended Antenna Design Rules	
R-CGO2.ANT.1	The POLY plate should be connected to a diode at Metal 1 : See CGO2.ANT.1 and CGO2.ANT.2
R-CGO2.ANT.2	If a diode cannot be connected to the POLY, the length and area of the METAL connections should be minimized; the number of VIAS should be minimized as well.
R-CGO2.ANT.3	Maximum Number of Contacts per capacitor =4*sqrt(S)
R-CGO2.ANT.4	If S<12 µm², Maximum Number of contacts per capacitor = 12

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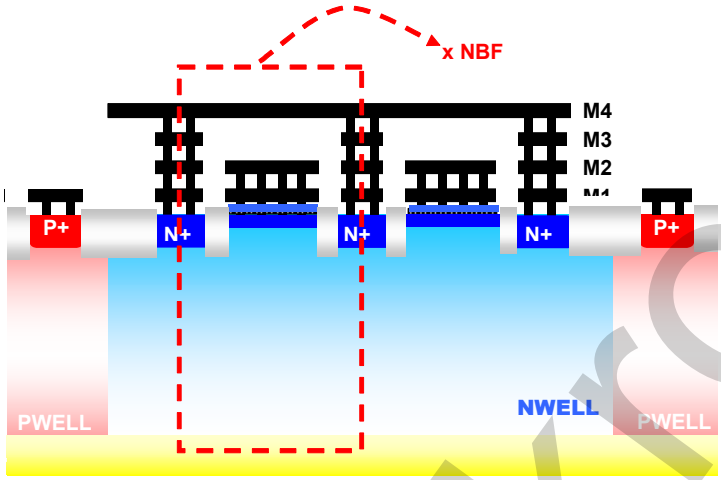
7.3.8.10Varactors

The varactors are non-linear devices that provides a voltage dependent capacitance.

7.3.8.10.1N+POLY/NWELL MOS Varactor

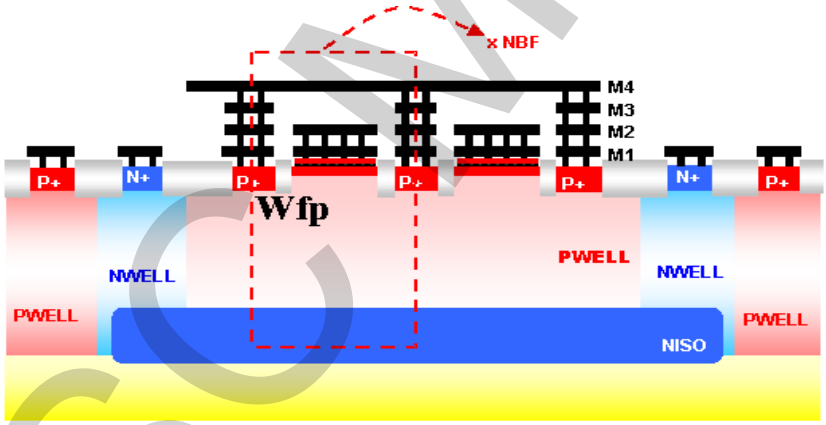
The N+poly/Nwell varactors are composed of N+poly fingers inserted between 2 N+ implants on NWELL. The next figure presents the structure of this varactor.



Cross-Section of N+poly/NWELL MOS Varactor

7.3.8.10.2P+POLY/PWELL MOS Varactor

The P+poly/Pwell MOS varactors are composed of P+poly fingers inserted between 2 P+ implants on PWELL. The next figure presents the structure of this varactor.



Cross-Section of P+poly/PWELL MOS Varactor

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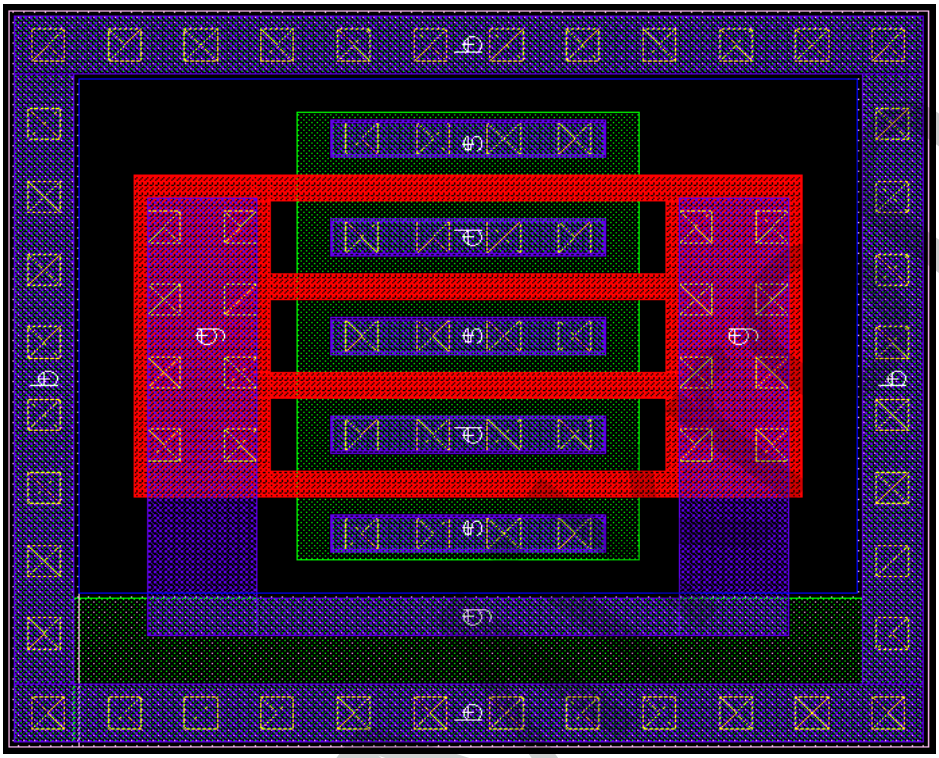
7.3.8.11RF MOS

For optimum fit to the SPICE model, transistors should be drawn as close as possible to the devices used for SPICE extraction.



Top view of an RF transistor used for modeling

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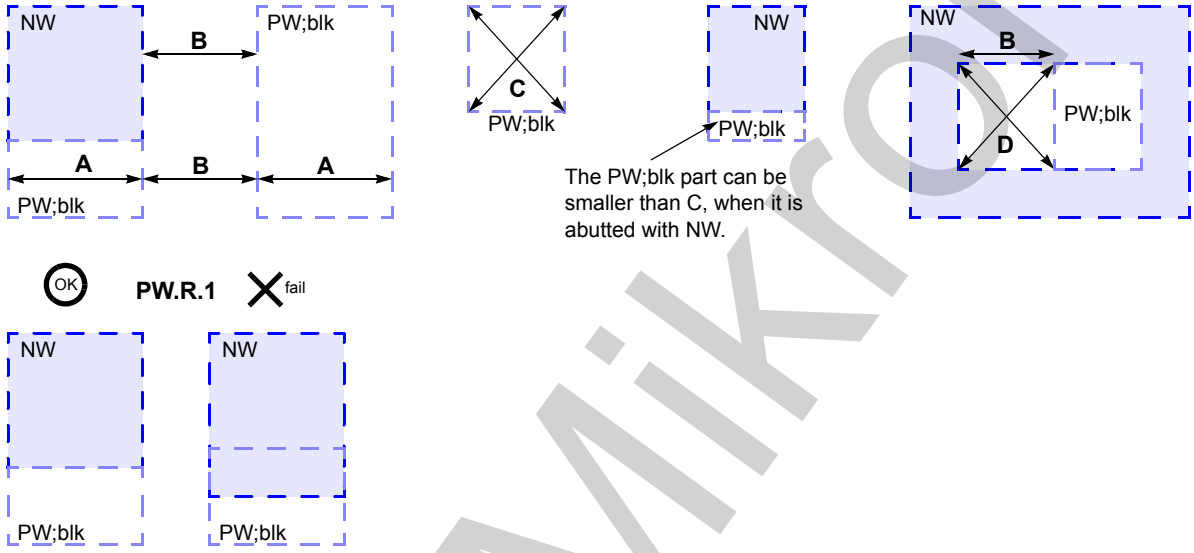
7.3.8.12P-Well Block Design Rules

P-Well (PW) is not a drawn layer, it is derived from {NW or PW;blk}. Areas marked with PW;blk (P-Well block) will receive neither N-Well nor P-Well implants, i.e. expose the undoped substrate. The use of PW;blk shall be avoided except where its use is explicitly stated in this document.

PW;blk Design Rules (P-Well block)			
PWB.W.1	{NW or PW;blk} Width	A	0.620
PWB.S.1	PW;blk Space to {NW or PW;blk}	B	0.620
PWB.A.1	PW;blk Area, except when abutted with NW	C	1.550
PWB.A.2	{NW or PW;blk} Enclosed Area	D	1.550
PWB.R.1	PW;blk must not intersect NW, except under INDDMY		



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7.3.8.13NO-NLDD Transistors

No-LDD transistors are supported in limited configuration for specific applications:

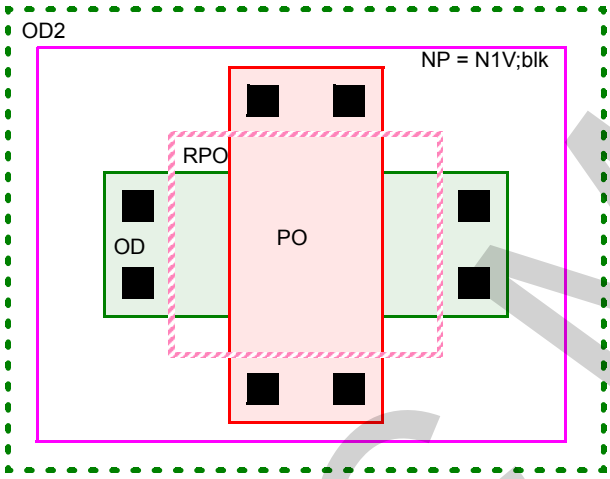
- NMOS transistors for ESD applications (nsvt25rponoldd).

Special CAD Levels (for reference only)		
Name	**Number**	**Description**
N1V;blk	225;20	Defines area that does not receive NLDD nor NLDDGO2 implants (special applications only)
N2V;blk	227;20	Defines area that does not receive NLDDGO2 implant (obsolete, use N1V;blk instead)

7.3.8.13.1NLDD Block Design Rules

Areas marked with N1V;blk will receive neither NLDD nor NLDDGO2 implants. The no-ldd devices can now be drawn using N1V;blk, even for OD2 devices; this is enabled by a change in CAD2MASK (N/A). The use of N1V;blk shall be avoided except where its use is explicitly stated in this document.
There are no device specific design rules for the no-ldd transistors. The design of the N1V;blk layer is limited by the NP and PP boolean rules (NP.B.1, NP.B.2, PP.B.1, PP.B.2). It is recommended to draw N1V;blk line-on-line with the NP or PP it is covering.

Example no-LDD-NMOS unsilicided



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7.3.8.14Gated Diodes

Gated diodes are supported in limited configuration for specific applications:

- Diode for ESD applications (dgnsvt25, dgpsvt25).

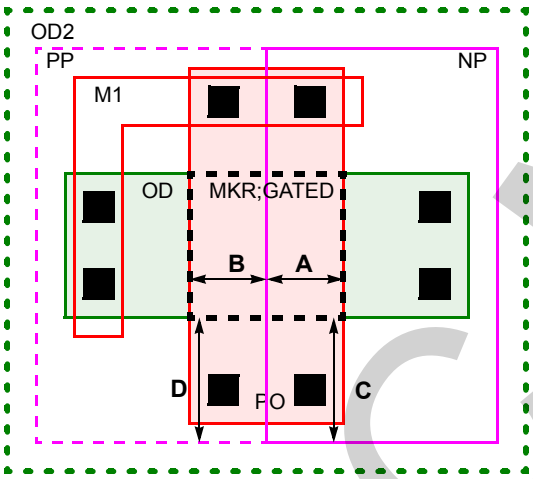
Special CAD Levels (for reference only)		
Name	**Number**	**Description**
MKR;GATED	218;111	Marker layer for gated diodes.

7.3.8.14.1Gated Diode Design Rules

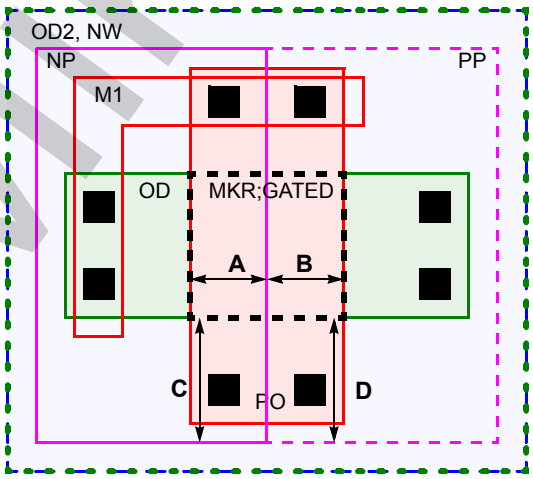
Gated diodes are constructed with a PO protecting a lateral NP/PW or PP/NW junction from silicidation. The PO (gate) is typically connected to the well-tie end of the diode. Gated diodes are excepted from the following design rules: NP.EN.1 (replaced by GD.EX.1), PP.EN.1 (replaced by GD.EX.2), PO.W.5.

Gated Diode Design Rules			
GD.OL.1	NP Overlap of Gate of gated diode	A	0.150
GD.OL.2	PP Overlap of Gate of gated diode	B	0.150
GD.EX.1	NP Extension on Gate	C	0.220
GD.EX.2	PP Extension on Gate	D	0.220
GD.R.1	MKR;GATED must be drawn line-on-line with Gate of gated diode		
GD.R.2	Gated diode not allowed outside OD2 (MKR;GATED outside OD2 not allowed)		

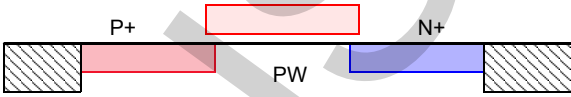
Example N+/P-Well Gated Diode



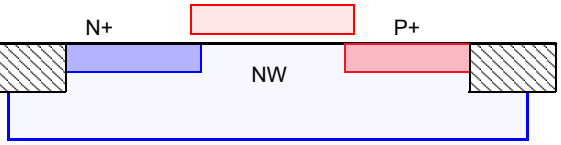
Example P+/N-Well Gated Diode



Cross Section: N+/P-Well



Cross Section: P+/N-Well



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7.3.8.15High Resistance Poly Resistor (HIPO RESISTOR)

The HIPO resistor is an unsilicided poly resistor designed for reaching high resistance values useful in analog applications. This device requires one additional mask PRESIST derived from CAD layer HRI (High Resistance Implant).

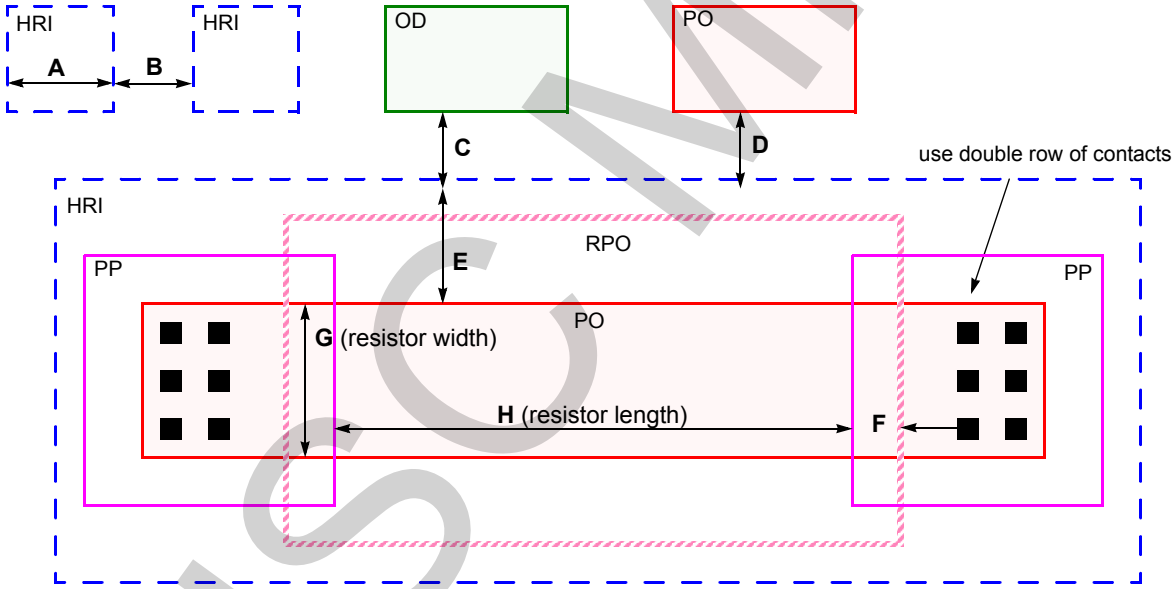
- the drawn width is defined by the poly width.
- the drawn length is defined by the spacing between P+ implants.
- for maximum current density, please see §7.7.3

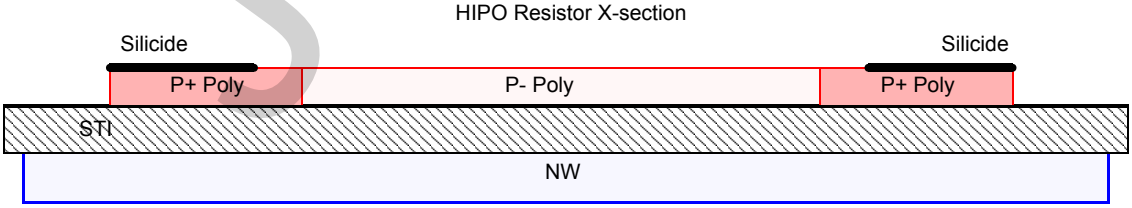
Derived geometries:

HIPO RESISTOR: PO **.and.** RPO **.and.** HRI **.not.** PP **.not.** NP **.not.** RH
Unsilicided poly area doped P- type between two heavily doped P+ type poly regions at the opposite ends of the resistor defining heads of HIPO resistor.

HIPO DUMMY RESISTOR: *HIPO resistor whose heads are not contacted. These dummy resistors are drawn next to HIPO resistors to improve matching performance.*

HRI Design Rules (High Resistance Implant)			
HRI.W.1	Width	A	0.720
HRI.S.1	Space	B	0.310
HRI.D.1	Distance to OD (HRI must not interact with OD)	C	0.260
HRI.D.2	Distance to PO	D	0.260
HRI.EN.1	Enclosure of PO	E	0.260
HRI.OL.1	Overlap of PP (min = max)	F	0.300
HRI.W.2	PO width within HRI (minimum resistor width)	G	1.000
HRI.L.1	Resistor length (defined by PP space to PP)	H	3.000





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7.4 PACKAGING INTERFACE DESIGN RULES

7.4.1 ELECTRICAL WAFER SORT (EWS) AND ASSEMBLY CONSTRAINTS

The detailed rules depend on the target final manufacturing organization used for the product. Design rules of the target assembly organization have to be followed.

7.4.2 ASSEMBLY RULE SPECIFICATION

Packaging technology should be taken into account at the very first steps of any design project. Special care must be taken regarding power dissipation, functional testability, and assembly. The detailed rules depend on the target final manufacturing (assembly) organization used for the product.

In the subsequent sections we describe the minimum requirements to enable Wirebond (§7.4.3) and Flip-Chip (§7.4.4) packaging technology. The rules in these sections are the most aggressive of several options. This is not meant to suggest the use of the most aggressive option available. For guidance on the most appropriate option to use for a given design, contact Packaging Engineering.

7.4.3 WIREBOND PAD INTERFACE RULES

7.4.3.1 Generalities

Large metal plates are not compatible with the general design rules. The mechanical properties of the low-K material in the cmos090 backend require a careful design of the structure under the wirebond pad to provide mechanical integrity. Specific design rules are required thus to verify the wirebond pad area.

Definitions:

- For general layer references Mtop, etc., used in the rule descriptions, please refer to §7.3.3.
- Bonding Area = {MKR;wb or {CB outside MKR;sealring}}
- Downsized Bonding Area = {MKR;wb or {CB outside MKR;sealring}} [downsized 3um/side]

Construction of pads:

- Simple wirebond-pad construction uses only the CAD layer CB following design rules in §7.3.7.1 and §7.4.3.2. All necessary masks are generated from CB:
  - CB [unsized] → PADOPEN
  - CB [upsized] → ALUCAP
  - CB [unsized] → NITRIDE
  - CB defines the area where wirebond will be performed
- Complex wirebond-pads where the masks could not be generated from the CB alone, must not use the CAD layer CB, but instead must use CAD drawing layers CB;via, AP, NITRIDE, and CAD marker layer MKR;wb (following design rules in §7.3.7.1-§7.3.7.3, and §7.4.3.2):
  - CB;via [unsized] → PADOPEN
  - AP [unsized] → ALUCAP
  - NITRIDE [unsized] → NITRIDE
  - for complex pads (not using CB) it is **mandatory** to use the marker layer **MKR;wb** in all areas where wirebond will be performed.

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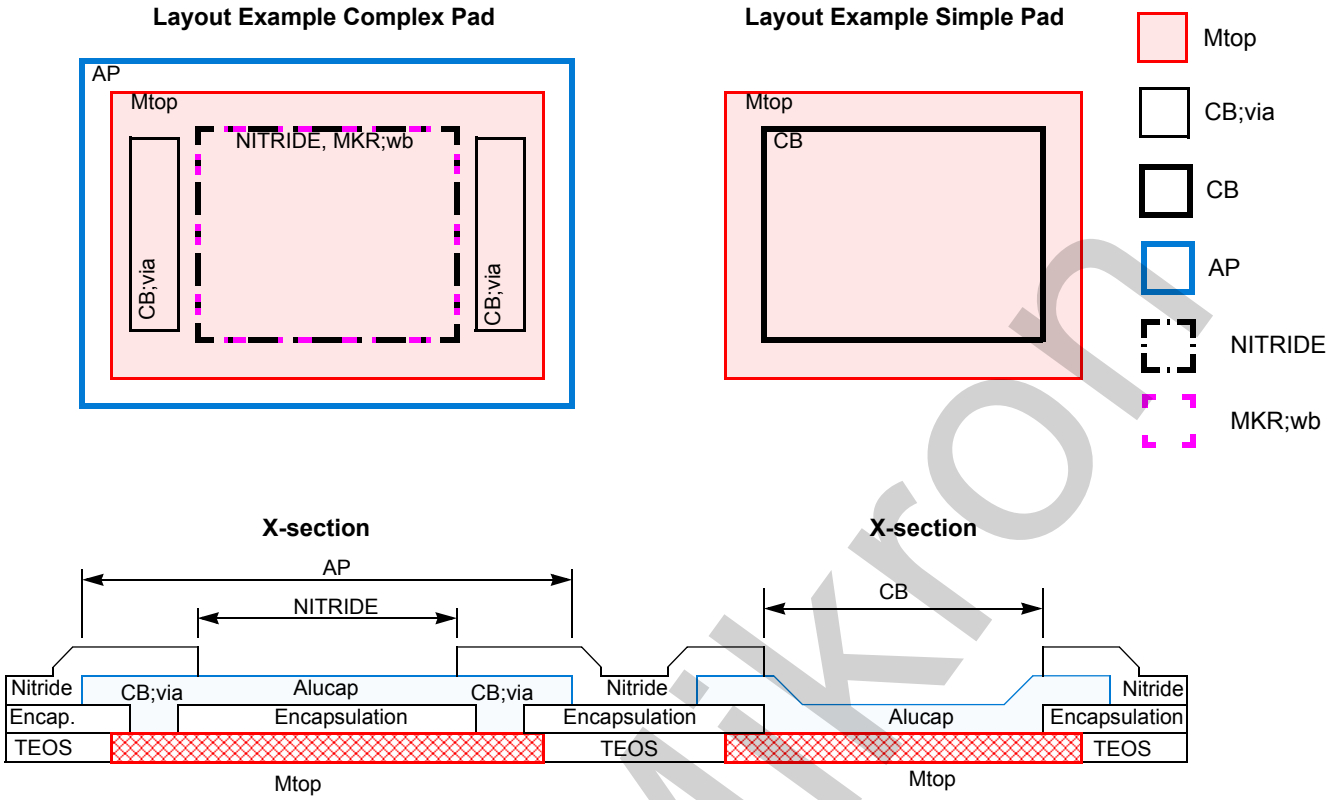

7.4.3.2 Wirebond Pad Layout Rules

For construction wirebond pads, follow all generic rules for CB (§7.3.7.1), CB;via (§7.3.7.1), AP (§7.3.7.2), and NITRIDE (§7.3.7.3). In addition the pad construction must follow the design rules of the target assembly organization to ensure bondability. The following design rules are necessary (but not guaranteed sufficient) conditions to ensure mechanical integrity during bonding. For a definition of bonding area see §7.4.3.1.

Bond Pad Design Rules			
WB.W.1	Bonding Area Width		30.000
WB.D.1	Mtop Distance to unrelated CB or CB;via (to limit distance for pads and distance between pad and wiring metal) [a]	A	3.000
WB.S.2	M4, M5, ..., Mtop Space (within downsized bonding area)	B	1.000
WB.R.2	NITRIDE may extend on maximal one edge of MKR;wb		
WB.DEN.1	M1, M2, M3 minimum density over local 20um x 20um areas stepped in 5um increments (if check window is within downsized bonding area)		20%
WB.DEN.1.1	M4, M5, ..., Mtop minimum density over local 20um x 20um areas stepped in 5um increments (if check window is within downsized bonding area)		30%
WB.DEN.2	M1, M2, M3, ..., Mtop-1 maximum density over local 20um x 20um areas stepped in 5um increments (if check window is within downsized bonding area)		80%
WB.DEN.3	Maximum density of the layer combination {Mtop-1 .or. ... .or. M4} over local 20um x 20um areas stepped in 5um increments (if check window is within downsized bonding area)		85%

a.Assembly design rules will require larger space depending on the bond-pad pitch option.

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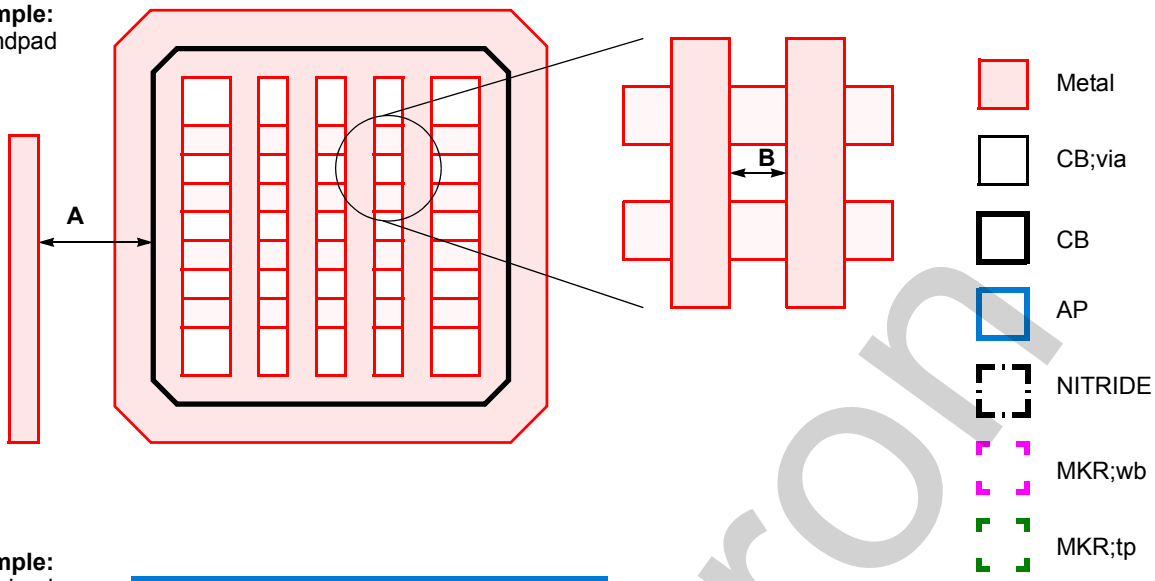
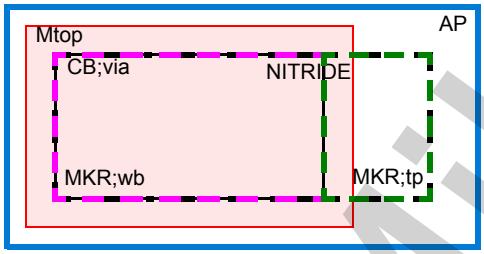
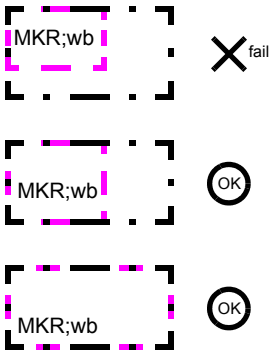
Layout example:
standard bondpad



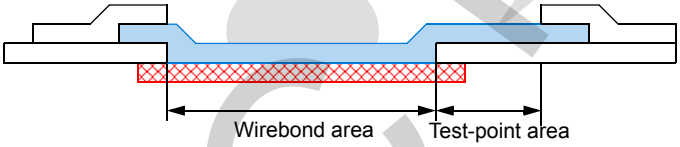
Layout example:
complex bondpad



WB.R.2



X-section example:
complex bondpad



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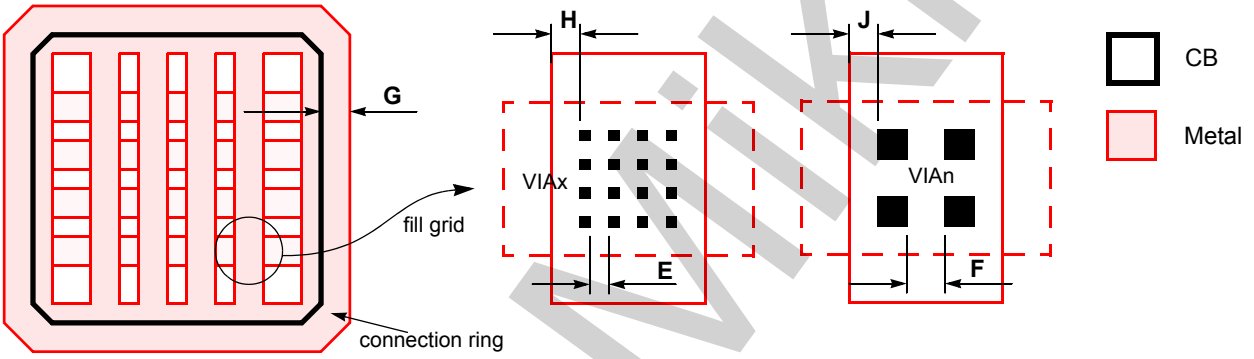
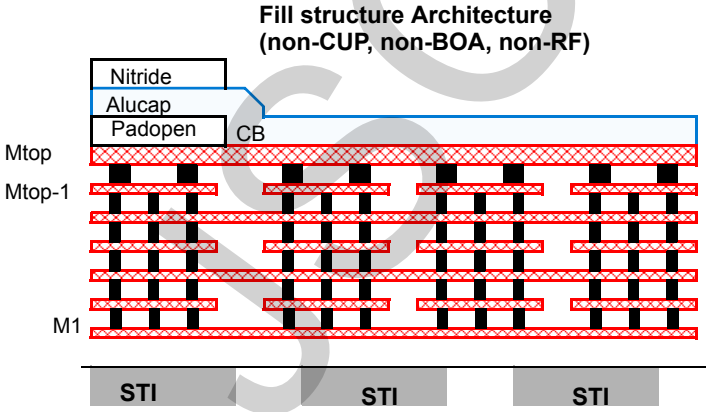
a) Standard wirebond pad structure

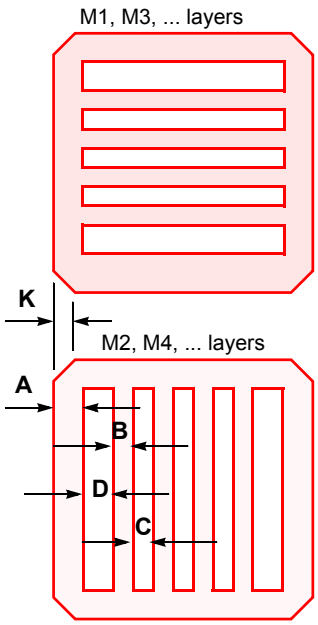
The below table and illustration show the construction values (not DRC verified) that are used for the standard pads. The design rules verified on these pads are the WB rules from the previous page.

Standard Pad Construction Rules			
S-WB.W.1	M1, Mx, Mn (up to Mtop-1) Width for connection ring (except: minimum 3.0 at 45deg corners)	A	5.000
S-WB.W.2	M1, Mx, Mn Width in grid (min = max)	B	1.500
S-WB.S.2	M1, Mx, Mn Space (use min = max inside grid)	C	1.000
S-WB.S.3	Maximum M1, Mx, Mn Space of grids to metal connection ring	D	3.500
S-WB.S.4	VIAx Space in grid	E	0.220
S-WB.S.5	VIAn Space in grid (is same as array space VIAn.S.2)	F	0.540
S-WB.EN.2	M1, Mx, Mn Enclosure of CB for connection ring	G	2.000
S-WB.EN.3	Metal (above and below) Enclosure of VIAx	H	0.160
S-WB.EN.4	Metal (above and below) Enclosure of VIAn	J	0.120
S-WB.L.1	Metals must have 45deg beveled corners. Minimum M1, Mx, Mn Corner Length	K	2.000
S-WB.R.3	Standard pad consists of solid Mtop, and a fill pattern below. The fill pattern must consist of all metals (M1 to Mtop-1) and vias (VIA1 to VIAtop) levels. It must not contain any CO.		
S-WB.R.4	Number of VIAx in each metal intersection inside bonding area		16
S-WB.R.5	Number of VIAn in each metal intersection inside bonding area		4



Mtop is solid. Other metals are slotted





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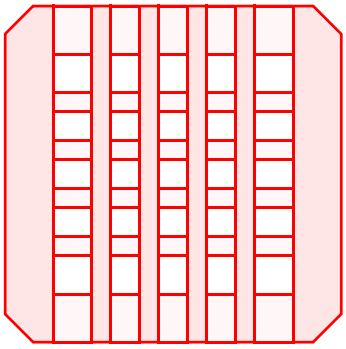
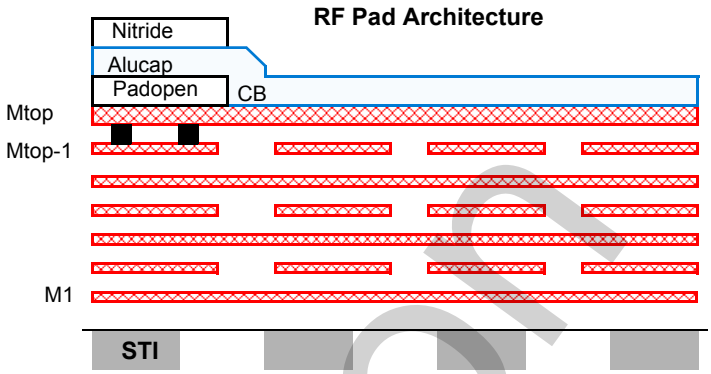
b) Wirebond RF pads

For RF applications the pad architecture is typically modified to minimize parasitic capacitance while maintaining mechanical stability during bonding. RF pads must fulfill the regular WB design rules.

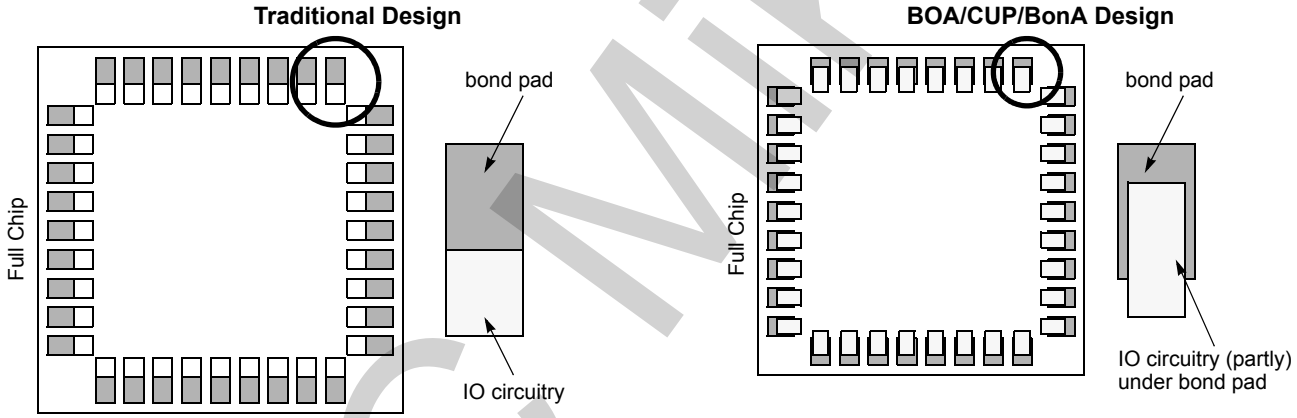
Example RF pad layout



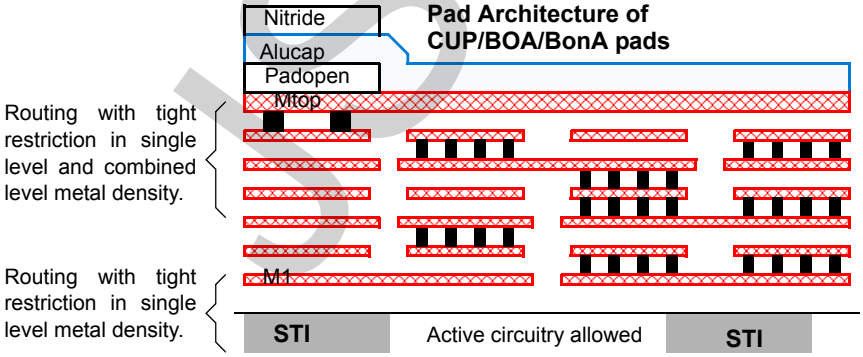


c) BOA/CUP/BonA wirebond pads

The WB design rules allow active circuitry under the wirebond pads. These complex pads enable a significantly more compact IO design (“Bond Over Active” or “Circuitry Under Pad” or “Bond on Active” - BOA/CUP/BonA)



New BOA/CUP/BonA pad designs based on the WB rules need to be reviewed by the process technology and assembly teams early in the design cycle and are required to be approved by the process technology team. IP-tag verification shall be enforced for BOA/CUP/BonA designs.



Recommendations for design of BOA/CUP/BonA IOs:

- M1, …, Mtop-1 density shall be distributed as uniformly as possible so as to minimize the density differences between adjacent check boxes.
- VIA1, …, VIAtop shall be distributed as uniformly as possible within MKR;wb and at as high via density as possible to help support each low-k dielectric layer.
- M1, …, Mtop-1 individual tiles placed under the bonding area shall be minimized. Instead, metals with enclosed slots are strongly recommended.
- Parallel metal lines on the same net shall be “bridged” to form metal buses with enclosed slots.

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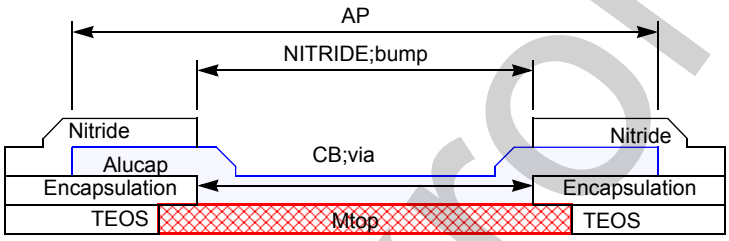
7.4.4 FLIP-CHIP INTERFACE RULES

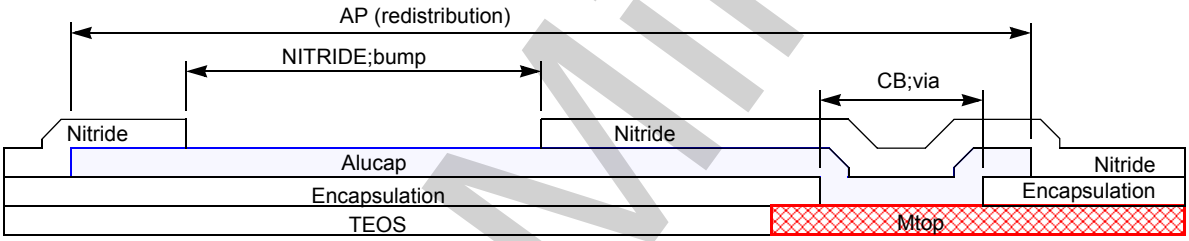
7.4.4.1 Generalities

- For general layer references (Mtop, VIAtop, etc.) used in the rule descriptions, please refer to §7.3.3.
- The Flip-Chip pads are the AP (ALUCAP) shapes that are exposed by the NITRIDE;bump opening.
- Routing redistribution can be achieved in Mtop or in AP (§7.4.5)
- The CAD levels for defining the flip-chip interface are used as follows:
  - — CB;via provides access to Mtop - PADOPEN (Mask Level 40)
  - — AP defines the Aluminum cap pad - ALUCAP (Mask Level 41)
  - — NITRIDE;bump defines opening in nitride passivation for the bumps - NITRIDE (Mask Level 33)

Example X-section (no AP redistribution)



Example X-section (AP redistribution)



7.4.4.2 Process Steps and Masks Added for Flip-chip Interface

Interface to Flip-Chip packaging does not require any additional processing or masks.

7.4.4.3 Cad Layer Definition for Flip-chip Interface

The flip-chip interface requires an additional CAD level (NITRIDE;bump) that identifies the location of the bump balls and is used to generate the necessary opening in the standard NITIRDE mask. NITRIDE;bump also shall be used to derive assembly masks by appropriate sizings as required by assembly organizations, for instance UBM (under bump metal) or PI (polyimide).

Special CAD Levels (for reference only)			
Name	**Number**	**Description**	**Option**
NITRIDE;bump	231;35	Opening in NITRIDE for flip-chip bump balls	Flip-Chip

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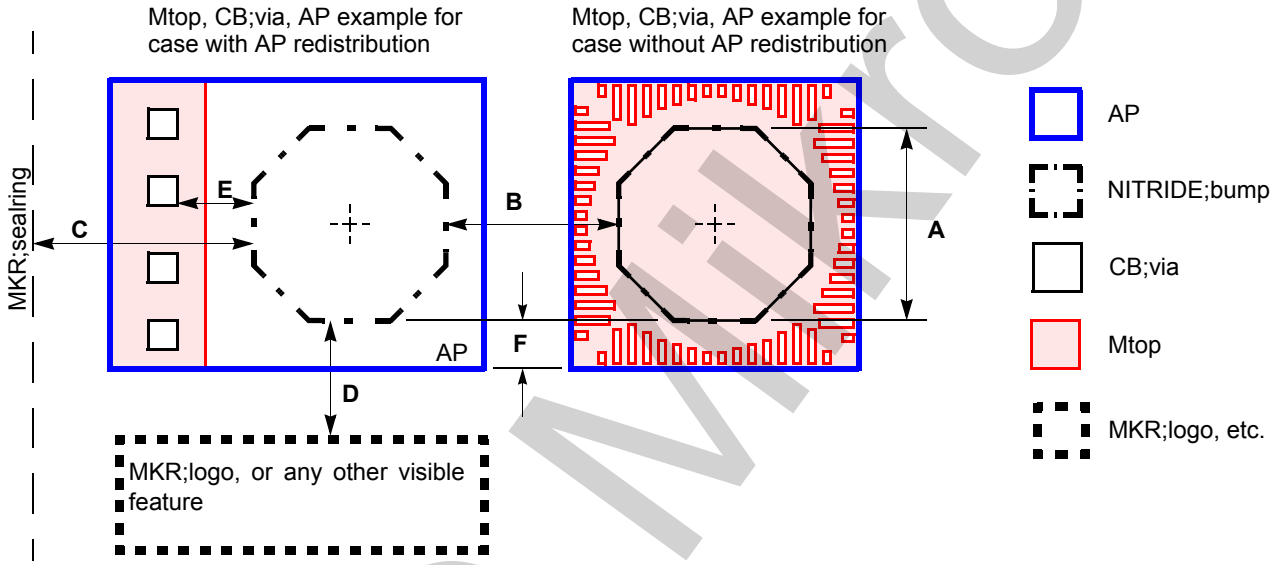
7.4.4.4 Flip-Chip Interface Design Rules

For construction of the flip-chip interface, follow all generic rules for CB (§7.3.7.1), CB;via (§7.3.7.1), AP (§7.3.7.2), and NITRIDE (§7.3.7.3). In addition the pad construction must follow the design rules of the target assembly organization. Below we illustrate some of the typical limitations found in flip-chip assembly documents.

Flip-Chip Pad Construction Values			
FC.W.1	NITRIDE;bump Width (size of passivation opening)	A	40.000
FC.S.1	NITRIDE;bump Space has to be chosen such that pitch is not smaller than 150um	B	110.00
FC.D.1	NITRIDE;bump Distance to MKR;sealring (chip edge)	C	90.000
FC.D.2	NITRIDE;bump Distance to Visible Feature {MKR;logo}	D	90.000
FC.D.5	NITRIDE;bump Distance to unrelated CB;via [a]	E	12.000
FC.EN.2	NITRIDE;bump Enclosure by AP	F	12.000

a.see also NIT.D.2.



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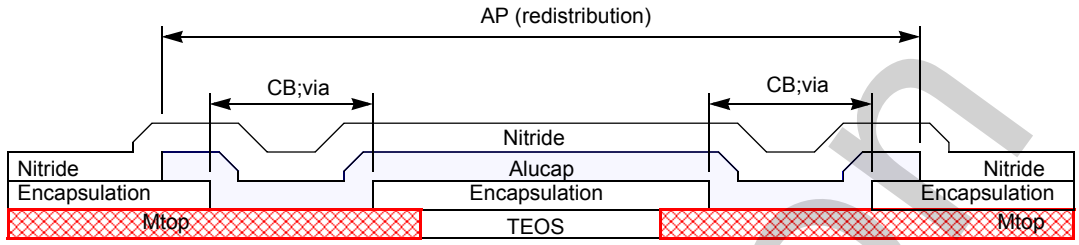
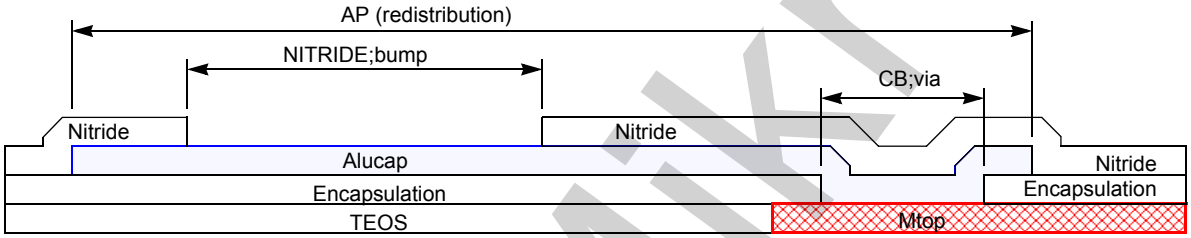
7.4.5 REDISTRIBUTION IN ALUCAP (RDL)

Redistribution can be established in the AlCu metal level (mask level ALUCAP, CAD level AP). The interconnect to the top copper metal level (Mtop) is established using the encapsulation opening (mask level PADOPEN, CAD level CB;via). For electromigration performance of AP and CB;via see §7.6.2.

Cross-section example: AP routing



Cross-section example: AP redistribution for flip-chip



7.4.5.1 Process Steps and Masks added for redistribution in Alucap

Redistribution in AP does not require any additional processing or masks.

7.4.5.2 CAD Layer definition for redistribution in Alucap

Redistribution in AP does not require any additional CAD levels.

7.4.5.3 Design Rules for redistribution in Alucap

AP redistribution follows the regular layout rules of CB;via (§7.3.7.1) and AP (§7.3.7.2). Actual layout will be driven by the electromigration restrictions (§7.6.2).

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7.4.6 DIE SEAL RING

The purpose of the seal ring is to give information for achieving a moisture resistant die, without the possibility that cracks generated in the scribe lane during the saw can propagate into the die.

For DRC purposes, the die seal ring is recognized as the area under MKR;sealring. Note: The automated dummy generation routine will not generate any dummies under MKR;sealring.

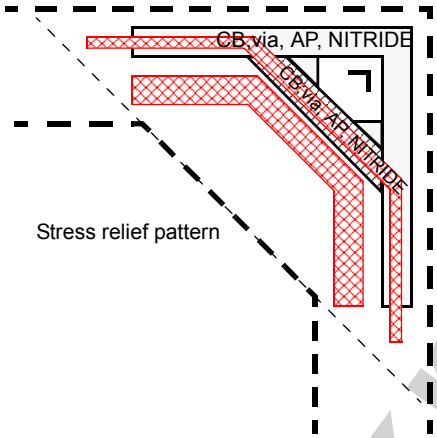

Fig. 1 : Robust Seal Ring Top View
Corner Detail

Robust Sealring Construction Rules			
RSR.R.2	The die seal ring must be a continuous ring around the entire chip consisting of 2 rings on all metals with 3 rings of CO and all vias (2 on inner, 1 on the outer metal). The outer metal ring is covered by CB;via, AP and NITRIDE. The die seal ring must be covered with MKR;seal-ring.		
RSR.D.1	Distance of die seal ring Metal to any NW, DNW, unrelated PO, NP or any dummy (these shapes not allowed under MKR;sealring). Metal Space within MKR;sealring. Space of Metal inside MKR;sealring to other metal.	A	3.000
RSR.D.2	CB;via Distance to metal of inner metal ring, except at corners	B	2.000
RSR.S.1	VIAn Space in die seal ring (space between continuous VIAn rings in inner metal ring)	C	1.120
RSR.S.2	VIAx Space in die seal ring (space between continuous VIAx rings in inner metal ring)	D	1.270
RSR.S.3	CO Space in die seal ring (space between continuous CO rings in inner metal ring)	E	1.280
RSR.S.4	Metal Space in die seal ring (space between inner and outer metal ring)	F	3.000
RSR.W.4	VIAn Width in seal ring (min=max width of continuous VIAn rings)	G	0.280
RSR.W.5	VIAx Width in seal ring (min=max width of continuous VIAx rings)	H	0.130
RSR.W.6	CO Width in seal ring (min=max width of continuous CO rings)	J	0.120
RSR.W.7	CB;via and NITRIDE Width in die seal ring (min=max width of continuous CB;via and NITRIDE rings, except at corners)	K	3.000
RSR.EN.1	Metal Enclosure of VIAn (continuous ring)	L	0.360
RSR.EN.2	Metal Enclosure of VIAx (continuous ring)	M	0.435
RSR.EN.3	M1 Enclosure of CO (continuous ring)	N	0.440
RSR.EN.4	MKR;sealring Enclosure of CB;via	O	1.000
RSR.L.1	Die seal ring corner exclusion length (only sealring, corner-L and stress relief pattern are allowed inside the zone defined by MKR;sealring)	P	70.00
RSR.L.2	Die seal ring metal corner length (corner-L placed in triangle outside the sealring metal)	R	30.00
RSR.D.3	CB;via Distance to metal of inner metal ring at corners	S	1.000
RSR.R.3	NITRIDE is drawn line-on-line with CB;via		
RSR.W.8	AP Width in die seal ring (min=max width of continuous AP rings, except at corners)	T	5.000
RSR.EN.5	AP enclosure of CB;via	U	1.000

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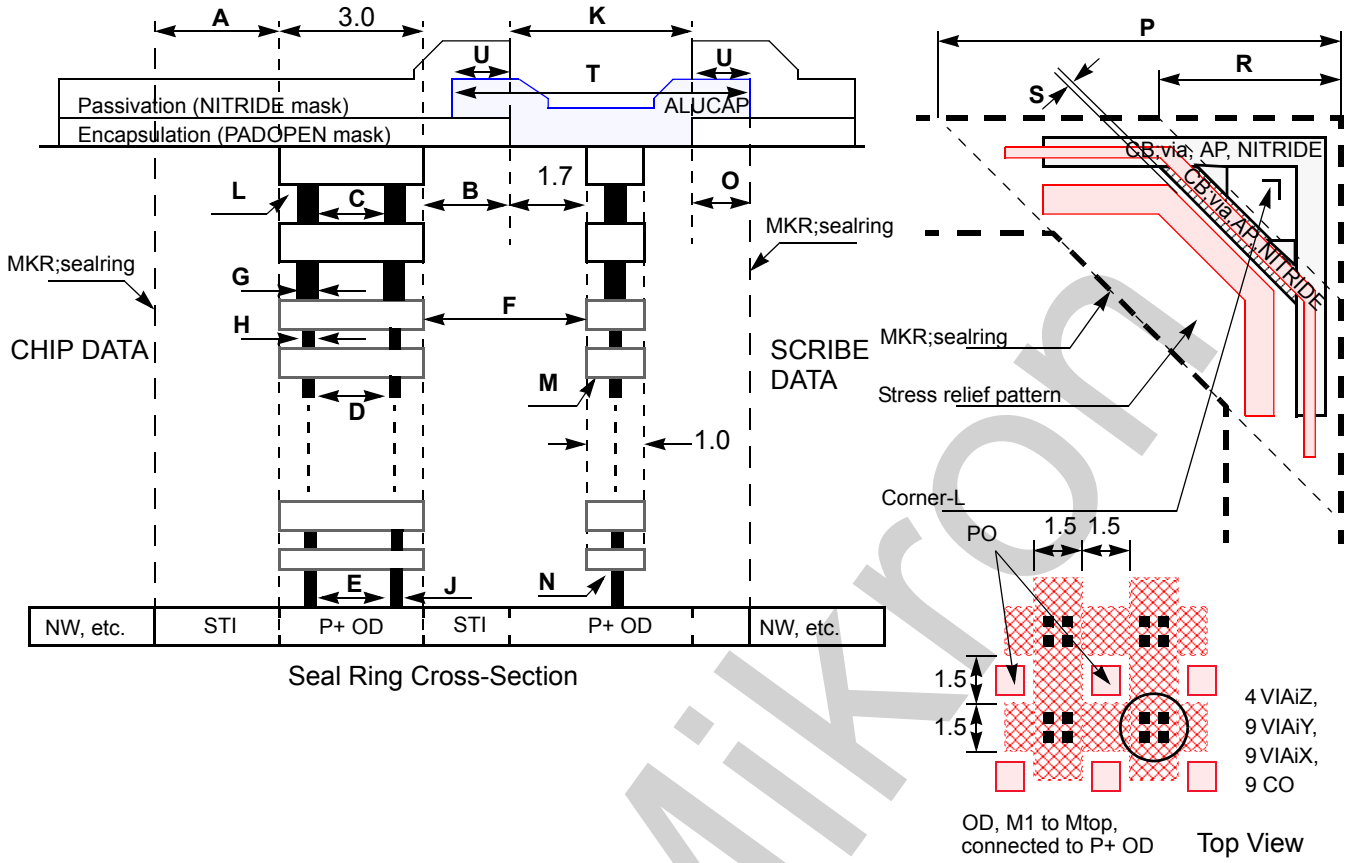
A
3.0
K
U
T
U
Passivation (NITRIDE mask)
Encapsulation (PADOPEN mask)
ALUCAP
L
C
B
1.7
O
MKR;sealring
MKR;sealring
G
F
H
CHIP DATA
SCRIBE DATA
M
D
1.0
E
J
N
NW, etc.
STI
P+ OD
STI
P+ OD
NW, etc.
Seal Ring Cross-Section
P
R
S
CB;via, AP, NITRIDE
CB;via, AP, NITRIDE
MKR;sealring
Stress relief pattern
Corner-L
PO
1.5 1.5
1.5
1.5
4 VIAiZ,
9 VIAiY,
9 VIAiX,
9 CO
OD, M1 to Mtop,
connected to P+ OD
Top View

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7.4.7 INACTIVE PATTERNS INSIDE THE DIE

7.4.7.1 Generalities

In the Common Technology Kit, CAD software is used to generate automatically seal ring and the masks patterns inside the die.

- Inactive patterns include:
  - Logos, Copyrights, Reticle numbers, etc (identified by MKR;logo)
  - Corner-L patterns for mask making (included in standard sealring - covered by MKR;sealring)
- Inactive patterns are drawn in CAD purpose noProcessing (GDS datatype 31)

7.4.7.2 Design Rules for Layout finishing Inactive Patterns

7.4.7.2.1 Line-Name

Must be written only on one metal layer (10 characters max, including revision number) in the corner of the IOs and shall be covered by the MKR;logo layer. For semi-custom products, the line name for base wafers can be written on Active, and on one metal layer for the customization.

	Line-name Digit height	15
	Line-name Digit width	10
	Line-name Digit space	3
	Minimum Line-name distance to Active devices (see design rule LOGO.EN.1)	3

7.4.7.2.2 Logo, Copyright and Year Requirements

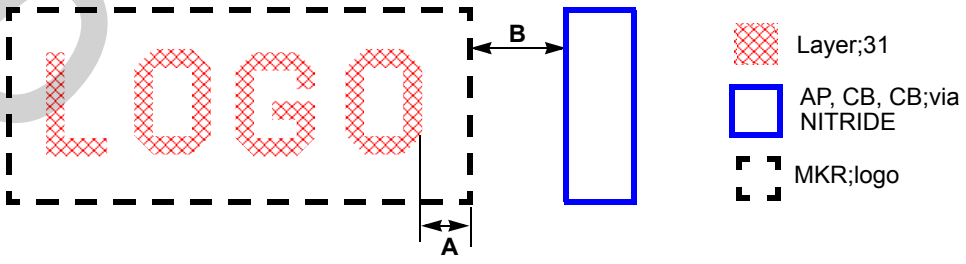
Special customization “art” drawings using large lines or curves of metal must be avoided, as it can be detected as defects by automatic inspection tools, thus creating false defect counts. Logo, Copyright and Year shall be drawn in Mtop, shall be placed in the corners of the IOs and shall be covered by the MKR;logo layer.

- shapes must comply with generic design rules (§7.3.4), in particular with the minimum width/space requirements of the layers they are drawn in (§7.3.6.6).
- shapes drawn in datatype 31 covered with the MKR;logo marker can have any angle (even non 45°), but no acute shapes. Note that only Metals, Poly and OD shapes produce visible features.

MKR;logo marker layer and dummy generation:

- Dummy generation in the Mtop, AP and MIM levels will be blocked within MKR;logo
- If dummy generation should be blocked on any other level, use the corresponding tileNot layer and datatype (§7.5.7.3).

Logo Design Rules			
LOGO.EN.1	MKR;logo Enclosure of OD, PO and metal shapes on datatype 31 (MKR;logo layer must cover the logo area)	A	3.000
LOGO.D.1	MKR;logo Distance to CB, CB;via, AP, NITRIDE (MKR;logo must not interact with these shapes)	B	2.000



7.4.7.2.3 Visual Aid Characters

In some cases, designers might want to place shapes that can be easily identified in specific layers. Locating an area of interest could be significantly easier when using those shapes as references.

Note that only Metals, Poly and OD shapes produce visible features. Drawing them in other layers (such as implants) are not of practical use.

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When required, those “visual aid” shapes must comply to the generic design rules (§7.3.4), in particular

- with the minimum width/space requirements of the layers they are drawn in (§7.3.6.6). It is a good practice to use dimensions that are several times the minimum feature size
- with the 45° angle requirements for the layer they are drawn in
- with the corresponding density rules

If dummy generation should be blocked on any level above the shape, especially to make it visible from the top, use the corresponding tileNot layers and datatypes (§7.5.7.3).

7.4.7.2.4 Reticles Numbers

Reticle numbers with revision letters shall be written at the corresponding layer for all reticles (including not drawn layers) excepted for NITRIDE for which the reticle number is not allowed. They shall be placed in the corners of the IOs, and adhere to the following rules.

A POLY plate must be drawn under the CONTACT letters: PO enclosure of CO	1
An ELEC2 pad must be drawn over the ELEC1 letters: ELEC2 enclosure of ELEC1	1
A M1 pad must cover the contact letters: M1 enclosure of CO	1
A Mi (i from 1 to top-1) pad must be drawn under the VIAi letters: Mi enclosure of VIAi	1
A Mi+1 pad must cover the Viai letters: Mi+1 enclosure of VIAi	1
A Last Metal pad (Mtop) must be drawn under the PADOPEN letter: Mtop enclosure of PADOPEN	1
A BOTMIM must be drawn under MKTOPMIM: BOTMIM enclosure of MKTOPMIM	1
ALUCAP pad must cover the PADOPEN letters: AP enclosure of CB	1
Minimum Layers numbers distance to Active devices	3
Minimum digits height	5
Minimum digits width	1
Minimum digits space	1
Minimum space between numbers	3

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7.4.7.2.5 Mask Set Name

Must not be written inside the die.

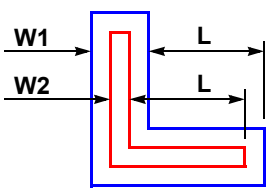
7.4.7.2.6 Corner L

Four Corner L defining a rectangle shall be drawn in the four corners of the die (minimum requirement is three) for all layers except passivation layers (NITRIDE). See sections §7.2.3 and §7.3.8.7 for correspondence between mask name and CAD level for this inactive mask pattern. These structures are designed to measure overlay of masks.

The Corner L features are included in the standard sealring, i.e. they are always covered with MKR;sealring. The MKR;sealring also ensures that no dummies are generated within 3um of any Corner-L structure. Corners must be drawn superimposed and with the following dimensions (enclosures must be the same on all sides; rules are the same in X and Y directions).

Corner L Design Rules			
CORL.L.1	Corner L length. (min = max) [a]	L	6.500
CORL.W.1	Corner L width (min = max) for: OD, DNW, NW, NW2V, PW, PW2V, VTH_N, VTH_P, VTNCELL, OD25, PO, N1V, P1V, N2V, P2V, VTL_N, VTL_P, NP, PP, PP2V, RPO, M1, ..., Mtop, CB, AP, HRI, BOTMIM, MKTOPMIM	W1	1.500
CORL.W.2	Corner L width (min = max) for: CO, VIA1, ..., VIAtop	W2	0.500

a.That means extent of the corner Ls is 7um x 7um, or 8um x 8um, respectively.



CO, VIA1, ..., VIAtop

OD, DNW, NW, NW2V, PW, PW2V, VTH_N, VTH_P, VTNCELL, OD25, PO, N1V, P1V, N2V, P2V, VTL_N, VTL_P, NP, PP, PP2V, RPO, M1, ..., Mtop, CB, AP, HRI, BOTMIM, MKTOPMIM

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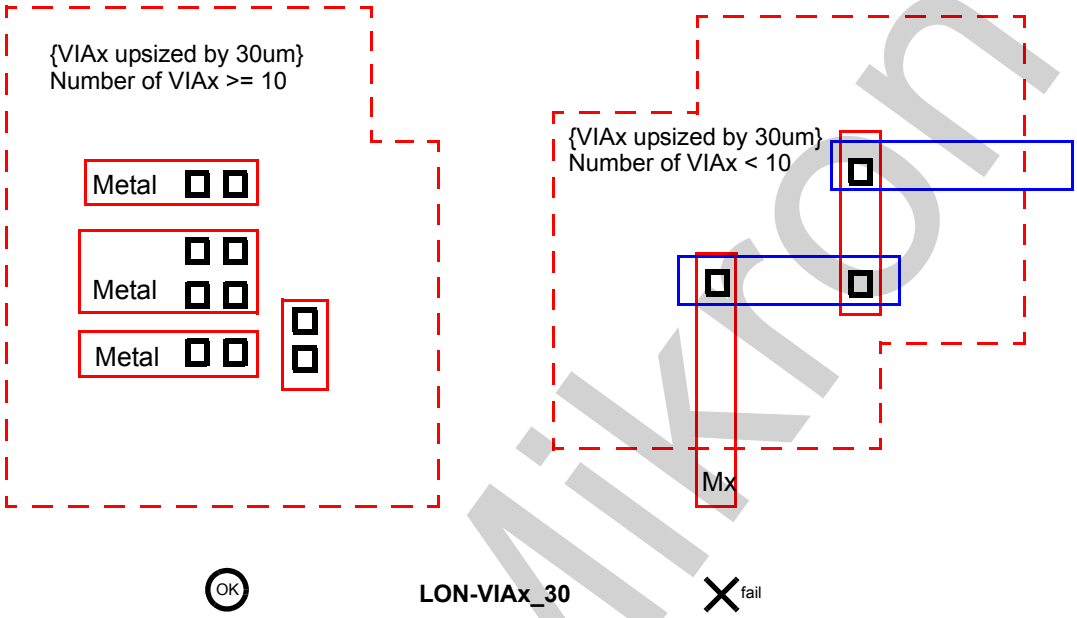
7.5 ROBUST DESIGN RULES

7.5.1 LONELY VIA RULE

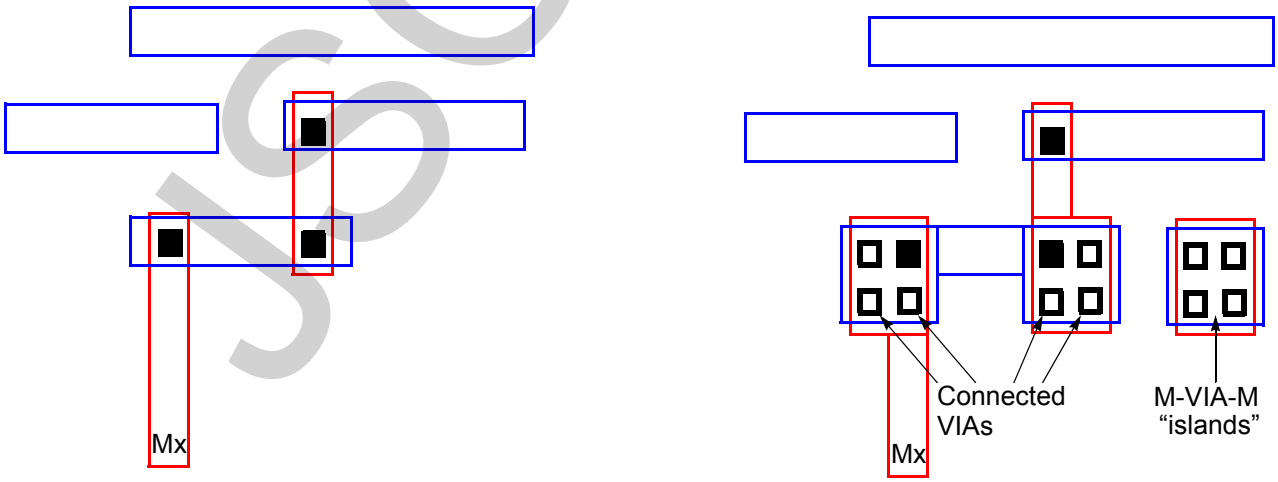
It has been found that VIAs located in a very isolated environment can show a systematic failure (VIA opening). Critical VIAs can be located with the following rule:

Lonely VIAx (only applies for VIAx)			
LON-VIAx_30	Minimum number of VIAx inside {VIAx upsized by 30um}		10



Regions with critical VIAs can be corrected by:

- increasing the number of connected VIAs in the near vicinity of the lonely VIAs. This might require enlarging the metal lines below and/or above.
- placing “islands” of metal-VIA-metal, in case connected VIAs cannot be placed due to space limitations as for instance in case of neighbouring metal lines.



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7.5.2 PROCESS-INDUCED DAMAGE ANTENNA RULES

During poly, inter-layer dielectric, contact, via and metal processing, damage is induced in the gate oxide. Damage during poly etch is driven by the poly perimeter, however, an additional design rule is defined in terms of poly area to limit damage during ILD0 deposition. For damascene metal processing, the damage accumulated in the gate oxide is approximated as a function of the gate oxide area and the area of connected contacts, vias and metal lines.

7.5.2.1 General definitions

subnet is a net connecting conducting layers up to the respective processing level. Examples: (A) a subnet relevant for VIA2 only has the connectivity built through OD, PO, CO, M1, VIA1, M2, and VIA2, but does not use any levels above VIA2 for the connectivity. (B) a subnet relevant for M3 only has the connectivity built through OD, PO, CO, M1, VIA1, M2, VIA2, and M3, but does not use any levels above M3 for the connectivity.

unprotected net a subnet that is not connected to any effective N+ OD or P+ OD. An effective N+ OD or P+ OD has to at least fulfill the minimum OD area rule OD.A.1. See §7.5.2.3 for applicable design rules.

protected net a subnet that is connected to an effective N+ OD or P+ OD (for instance a diode, or any source/drain of a transistor or a well tie). See §7.5.2.4 for applicable design rules.

7.5.2.2 Antenna ratio definitions

The different PO or metal layer wires can act as “antennas” for collection of charges. Note, that at Last Metal, every gate is connected to the output of the previous stage, except for the inputs; for the inputs, the gate is connected to the diodes of the ESD clamp. So the last metal layer can always be assumed to be protected, i.e. connected to a N+ OD or P+ OD.

Definitions of the antenna ratios:

AR_poly_area: Poly antenna ratio for a PO node

$$AR_{poly\_area} = \frac{A_{poly}}{A_{gate}}$$

A_gate is the Gate area connected to this node.
A_poly is the PO top area connected to this node.

AR_poly_sidewall: Poly antenna ratio for a PO node

$$AR_{poly\_sidewall} = \frac{Asw_{poly}}{A_{gate}}$$

A_gate is the Gate area connected to this node.
Asw_poly is the PO side-wall area connected to this node. The sidewall area is the perimeter x thickness of the poly.

AR_cont: Contact antenna ratio for a CO node

$$AR_{cont} = \frac{A_{cont}}{A_{connected\_gates}}$$

A_cont is the contact area connected to this node (CO subnet).
A_connected_gates is the sum of all gate areas directly connected to this contact node (i.e. gates in this CO sub-net).

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PAR_via: Partial via antenna ratio for a via node

$$PAR_{via} = \frac{A_{via}}{A_{connected\_gates}}$$

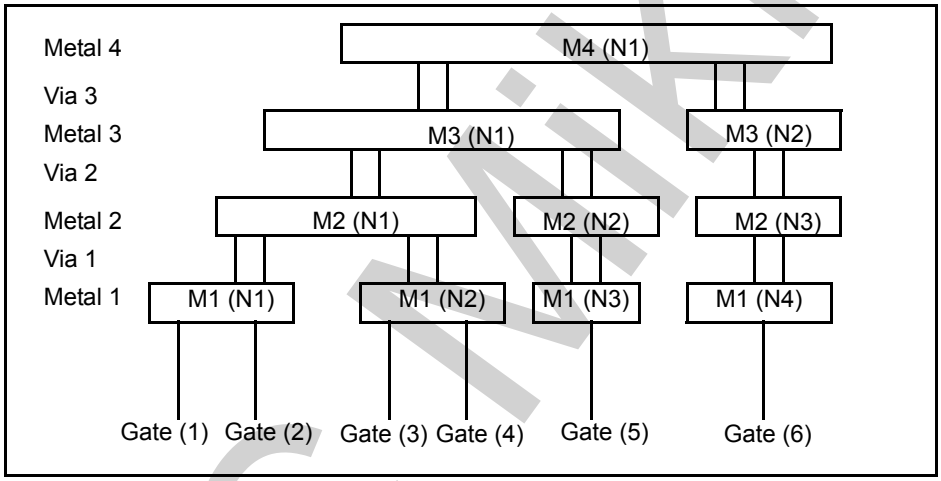
A_via is the via area connected to this node (VIA subnet).
A_connected_gates is the sum of all gate areas directly connected to this via node (i.e. gates in this VIA sub-net).

PAR_m: Partial Antenna Ratio for a metal node:

$$PAR_m\{Mi\,(Nj)\} = \frac{A_{metal}\{Mi(Nj)\}}{A_{connected\_gates}}$$

A_metal{Mi(Nj)} is the area of Metal-i at Node-j
A_connected_gates is the sum of all gate area connected to node-j below Metal-i (Metal-i subnet).

Example for Partial Antenna Ratio:



At the Metal 1 and IMD1 process, a Metal1 line can induce charges to directly connected poly gates:

$$PAR_m\{M1(N1)\} = \frac{\text{Area of Metal 1, Node 1}}{\text{Area Gate (1) + Area Gate (2)}}$$

At the Via 1 process, a Via 1 can induce charges to directly connected poly gates:

$$PAR_{via}\{V1(N1)\} = \frac{\text{Area of Via 1, Node 1}}{\text{Area Gate (1) + Area Gate (2)}}$$

At the Metal2 and IMD2 process, the Metal1 lines do not collect charges, as they are not in direct contact with the plasma; a Metal2 line can induce charging only to the poly gates connected through Metal 1:

$$PAR_m\{M2(N1)\} = \frac{\text{Area of Metal 2, Node 1}}{\text{Area Gate (1) + Area Gate(2) + Area Gate (3) + Area Gate (4)}}$$

At the Via 2 process, a Via 2 can induce charges to directly connected poly gates:

$$PAR_{via}\{V2(N1)\} = \frac{\text{Area of Via 2, Node 1}}{\text{Area Gate (1) + Area Gate(2) + Area Gate (3) + Area Gate (4)}}$$

In a similar way, at higher metal levels a metal line or via can induce charging only to the poly gates in the same subnet.

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BECAR_m: Back End Cumulated Antenna Ratio for metal is defined for each PO node:
BECAR_m = Sum of PAR_m of all the nodes connected on top of this PO node.

In the previous example:
BECAR_m {M3, gate(1)} = PAR_m{M1(N1)} + PAR_m{M2(N1)} + PAR_m{M3(N1)}
BECAR_m {M4, gate(1)} = PAR_m{M1(N1)} + PAR_m{M2(N1)} + PAR_m{M3(N1)} + PAR_m{M4(N1)}

BECAR_via: Back End Cumulated Antenna Ratio for via is defined for each PO node:
BECAR_via = Sum of PAR_via of all the nodes connected on top of this PO node.

In the previous example:
BECAR_via {V2, gate(1)} = PAR_via{V1(N1)} + PAR_via{V2(N1)}
BECAR_via {V3, gate(1)} = PAR_via{V1(N1)} + PAR_via{V2(N1)} + PAR_via{V3(N1)}

7.5.2.3 Antenna design rules for unprotected gates (subnet without diode protection)

To prevent MOS devices from charging damage, the transistor antenna ratio has to be compliant with the maximum antenna ratio rules described in the below table for all the layers.

The following table gives the maximum antenna design rules for each level. A thin oxide device, or a GO2 device, without protection is design rule compliant if all the design rules fulfill the condition form the “Thin Ox,” or “OD2” column, respectively.

Maximum Antenna Ratio Design Rules - Unprotected Nets		**Thin Ox**	**OD2**
PO.ANT.1	Maximum drawn ratio of PO area to the active PO gate area connected directly to it (AR_poly_area)	250	250
PO.ANT.2	Maximum drawn ratio of PO Sidewall area to the active PO gate area connected directly to it (AR_poly_sidewall) [a]	500	500
CO.ANT.1	Maximum drawn ratio of poly CO area to the active PO gate area connected directly to it (AR_cont)	10	10
VIA.ANT.1	Maximum drawn per-layer ratio of via area to the active PO gate area connected directly to it (PAR_via)	20	20
M.ANT.2	Maximum Cumulative Metal (M1, Mx, Mn) Antenna Ratio for any PO node (BECAR_m)	5000	1000

a.Gate poly thickness is 0.15um for both thin oxide and OD2 devices.

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7.5.2.4 Antenna design rules for protected gates (subnet with protection)

For protected gates, one must use a sufficiently large N+OD or P+OD protection area. The N+OD or P+OD area required to protect the gate depends on the metal and via area connected to the gate.

All N+OD and P+OD areas that do fulfill the minimum OD area rule OD.A.1 and are connected to the metal or via do contribute to the protection area. I.e. any source or drain diffusion of a MOS transistor (with an area fulfilling OD.A.1) or any NWell or PWell tie are considered part of the protection area.

Antenna Design Rules for Protected Gates (Thin Oxide and OD2) [a]	
VIA.ANT.3	For any protected gate the cumulative via area connected to that gate must not exceed: Maximum Cumulative Antenna Ratio for via = 900 + 210 * protection area / um2 (evaluated for all sub-nets at processing of VIA1, VIA2, ..., VIAtop)
M.ANT.5	For any protected gate the cumulative metal area connected to that gate must not exceed: Maximum Cumulative Antenna Ratio for metal = 43000 + 456 * protection area / um2 (evaluated for all sub-nets at processing of M1, M2, ,,,, Mtop-1), Maximum Cumulative Antenna Ratio for metal = 50000 + 8000 * protection area / um2 (evaluated for sub-nets at processing of Mtop)

a.If a large diode is used, it is recommended to have one big diffusion area with multiple CO. Avoid covering the entire diode area with metal.

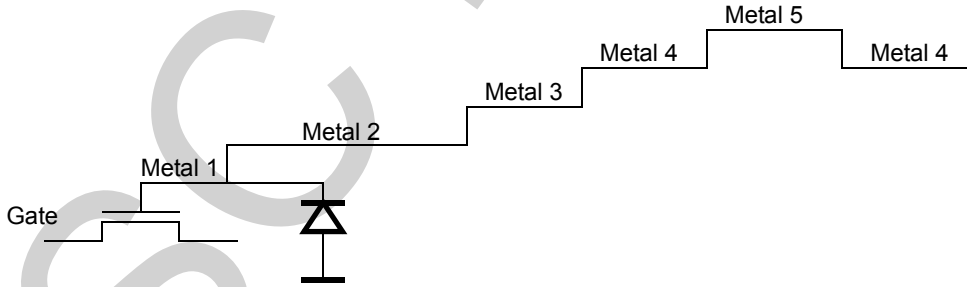
7.5.2.5 Guidelines to decrease the antenna ratio

In all cases where it is possible in term of silicon area availability, diode connection of metal lines to active area is recommended. These diodes derive the charges created during following process steps directly to the substrate, preventing the transistor from any subsequent damage. For highest efficiency such diode protection has to be introduced at M1 level if possible. The earlier (in terms of process steps) the diode is created, the more efficient is the protection.

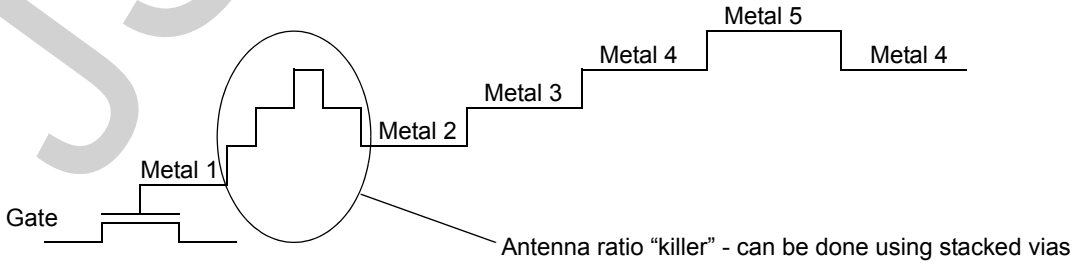
Any error detected at the DRC must be corrected using one of the following solutions:

- Connect directly the node to the output of the driver with a lower metal level and reduce the metal area
- Connect the node to a diode.
- Connect the gate to the highest metal level as close to the gate as possible.
- This last Metal can then be routed with other Metal lines. Stacked vias on contacts allow doing this connection in a small area.

Diode Protection



Metal bridging Protection



IMPORTANT: In cases where matching of transistors is of first importance, strong care has to be taken when designing the connection to the paired devices. In order to avoid mismatch between antenna ratio, metal lines are to be as much symmetrical as possible. For same reason, the connection lengths have to be minimized.

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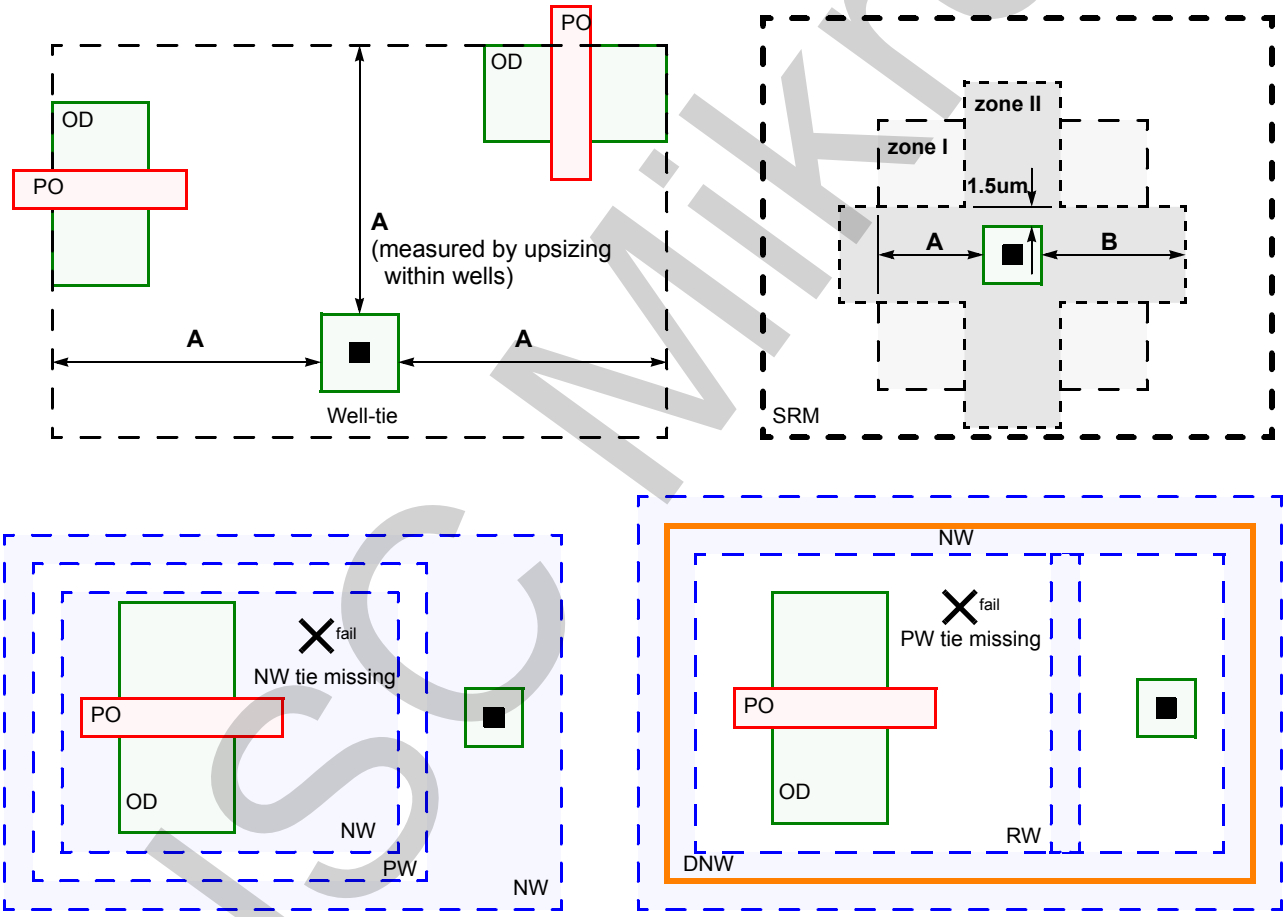
7.5.3 LATCH-UP PROTECTION

Standard recommendations used in the company apply to CMOS090. It is important to note that as minimum dimensions are decreasing, resistance of minimum straps is increasing; so rails should be preferred to minimum size straps.

7.5.3.1 Latch-Up Protection Design Rules for Internal Circuit Devices (DRC checked)

Latch-Up Protection Design Rules (DRC checked) [a]			
LUP.D.1	Maximum distance from any point inside Source/Drain OD area to the nearest OD of a well tie within the same NW or PW (see LUP.D.2 for special treatment of SRAM)	A	30.000
LUP.D.2	Maximum distance from any point inside Source/Drain OD area to the nearest OD of a well tie within the same NW or PW in SRAM region (marked with layer SRM). The distance is defined by the larger of the zones I, II: (I) OD of well tie sized by A inside the well (=LUP.D.1), (II) OD of well tie upsized by 1.5um in one direction and value B in the other direction.	B	40.000

a.Internal circuits: LUP.D.1 is not sufficient for IO buffers and ESD devices which should be protected following the latch-up guidelines described in §7.5.3.2. DRC implementation inaccuracies are acceptable up to a distance of 42um for non-orthogonal or non-straight distance measurements.



Designs shall always be laid out such that DNW can be added/removed later on without generating new design rule violations. Therefore missing PW and NW ties will be flagged independent of the existence of DNW.

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7.5.3.2 Latch-Up Protection Guidelines for I/O Devices

Latch-Up Protection Guidelines			
LUP.GL.1	IO buffers and ESD devices MUST be surrounded by double guard rings.		
LUP.GL.2	Devices formed in a PW or an isolated PW (with DNW) which have any hot OD area connecting to IO pads MUST be enclosed by a continuous P+ OD/PW guard (well tie) ring and a continuous N+ OD (with or without DNW)/NW guard (well isolator) ring. P+ OD/PW guard ring MUST be tied to VSS or VSS_IO and N+ OD/NW guard ring MUST be tied to VDD or VDD_IO. Multiple devices formed in a PW or isolated PW (with DNW) with or without hot OD area may be placed in a single P+ OD/PW guard ring.		
LUP.GL.3	Devices formed in an NW (with or without DNW) which have any hot OD area connecting to IO pads MUST be enclosed by a continuous N+ OD/NW with DNW guard (well tie) ring and a continuous P+ OD/PW guard (well isolator) ring. N+ OD/NW guard ring (with or without DNW) MUST be tied to VDD or VDD_IO. P+ OD/PW guard ring MUST be tied to VSS or VSS_IO. Multiple devices formed in an NW (with or without DNW) with or without hot OD area may be placed in a single N+ OD/NW (with or without DNW) guard ring.		
LUP.GL.4	P+ OD/PW and N+ OD/NW (with or without DNW) guard rings (well ties and isolators) can be merged together (P+ OD with P+ OD or N+ OD with N+ OD) only when both the adjacent wells and ring types match. No devices can be placed inside the well isolator guard ring itself. Devices are only intended to be placed inside the well that is enclosed by the guard ring.		
LUP.GL.5	Drawing DNW under PW greatly improves latch-up immunity if DNW is shared only with the surrounding guard (well isolator) NW ring.		
LUP.GL.6	Drawing DNW under NW slightly improves latch-up immunity if DNW is not shared with the adjacent PW.		
LUP.GL.7	Drawing DNW under both adjacent NW and PW which have any hot OD area connecting to IO pads is not allowed. If no hot OD area is present in either NW or PW, sharing of DNW for NW and PW is allowed provided latch-up rule LUP.D.1 described in §7.5.3.1 is followed.		
LUP.GL.8	The OD width for all continuous P+ OD/PW or N+ OD/NW guard rings (with or without DNW) MUST allow for a continuous single row of contacts.	A	0.200
LUP.GL.9	All the guard rings and pickups shall be connected to VDD, VDD_IO, VSS or VSS_IO with very low series resistance. CO and VIAs should be used as many as possible. All guard rings MUST be strapped with M1/CO. Occasional breaks in the metal strapping are allowed but the number of breaks should be minimized. The length of unstrapped OD should not exceed B = 3 * A (OD guard ring width). Breaks in the guard ring active (OD) are NOT allowed and each M1 strap must be connected directly to VDD, VDD_IO, VSS or VSS_IO.	B	0.600

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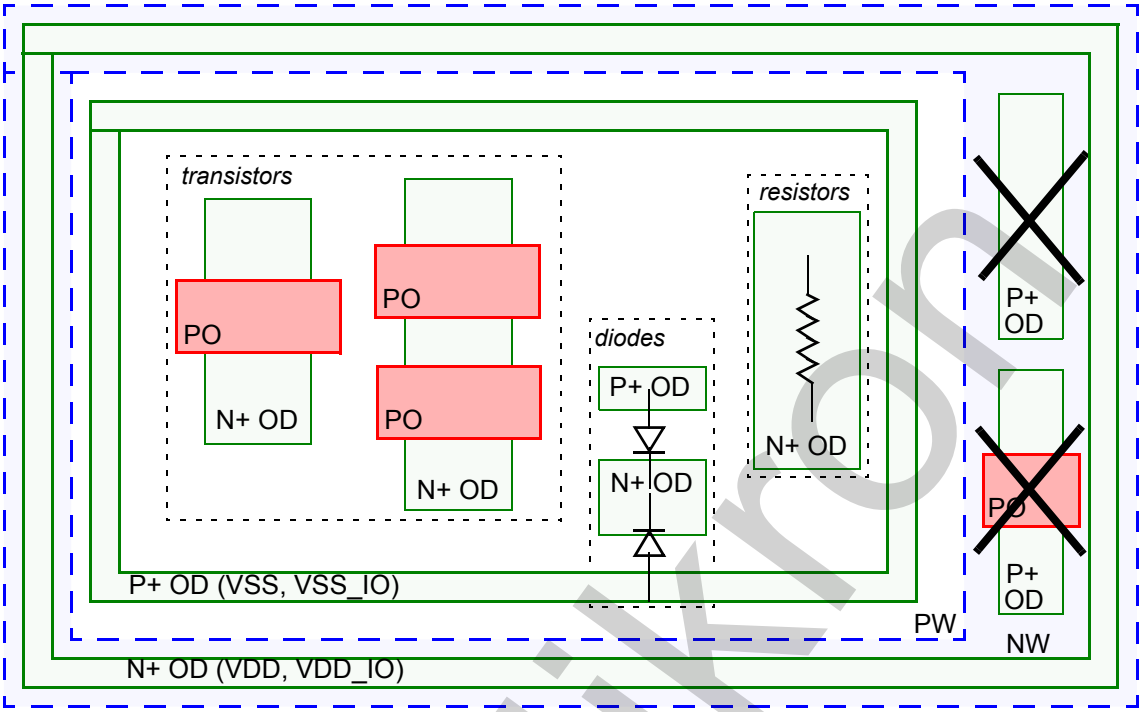
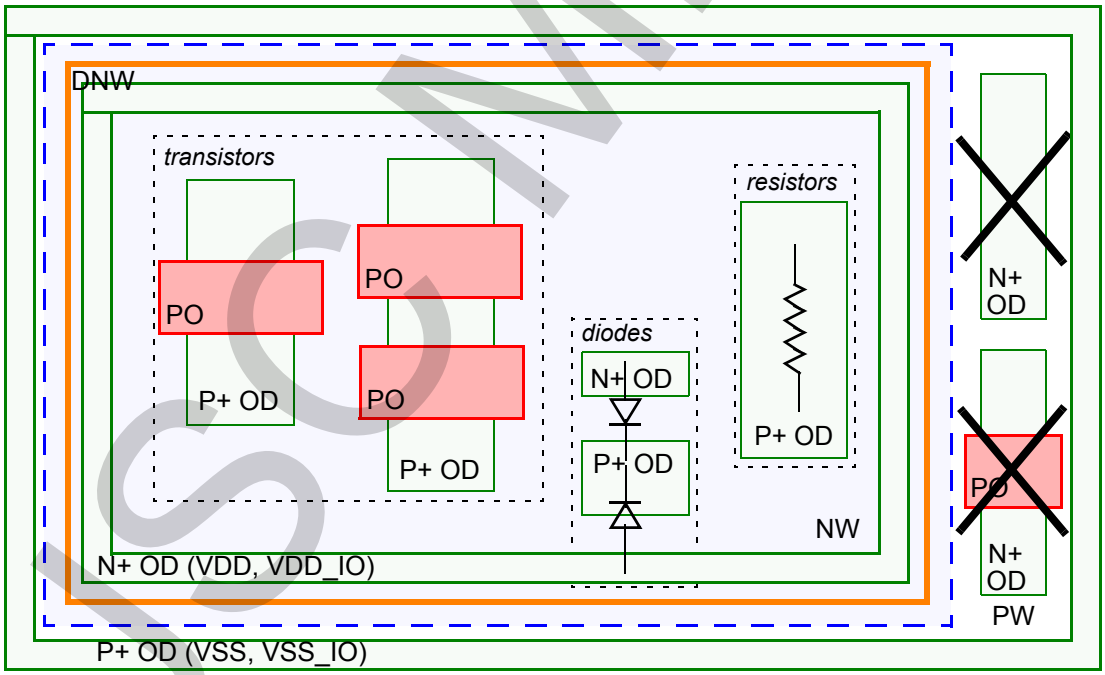
LUP.GL.1, LUP.GL.2, LUP.GL.4





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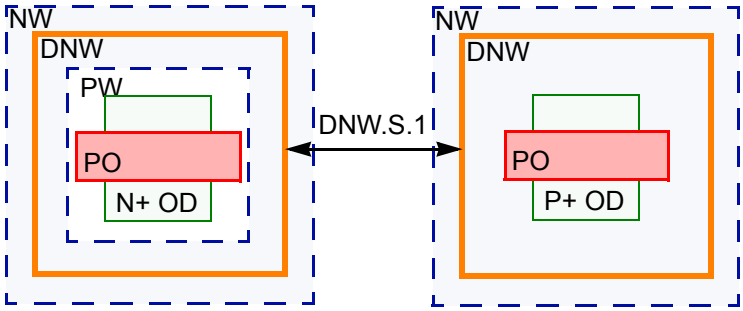
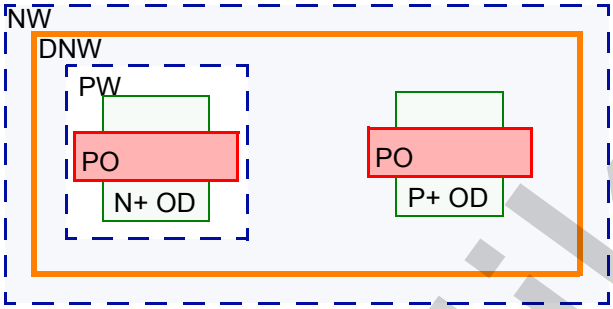
LUP.GL.5, LUP.GL.6, LUP.GL.7

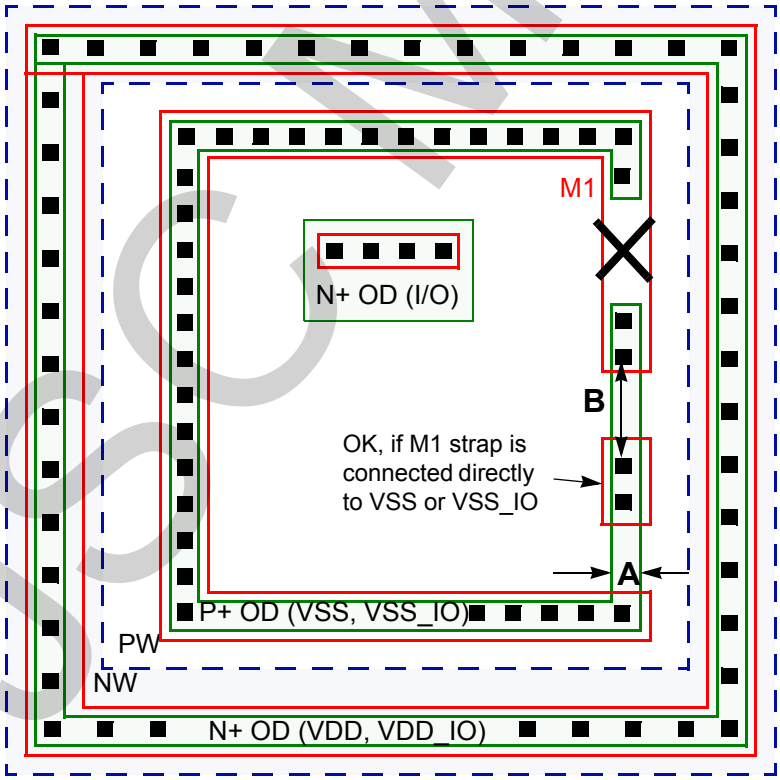


+ Best latch-up protection
- Layout penalty (DNW.S.1)



+ Layout compactness
- Worse latch-up protection (not suitable if hot OD area connected to I/O pads is present)

LUP.GL.8, LUP.GL.9



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7.5.4 ESD PROTECTION

- General information: CO to PO space in output buffers is increased to avoid metal melting in the CO during an ESD events. This also reduces current crowding. Some major design related parameters are critical for ESD performance:
- *Unsilicided active area:* In CMOS090, silicided ODs make current crowding more critical, so ESD performance is increased by preventing silicide formation. That is done with the RPO mask. The rule RPO.EX.3 is process related; it does not guarantee ESD performance. A larger value, in particular on the drain side of the transistor, is necessary to achieve the ESD performance required for each product.
- *Gate length of the transistor:* It has been observed in previous process that the optimum ESD performance occurs for the minimum channel length, due to the better activation offered by the parasitic NPN transistor. This is the reason why we advice to use the minimum gate length for ESD protection devices in IO's.
- *Width of the transistor:* Due to current density considerations, it is advised to use large transistors.
- *LDD suppression:* N-MOS transistor has been proved to be efficient as a clamping device without LDD implant. See §7.3.8.13.1 for design rules to block LDD implants
- *A complete IO solution:* has been characterized on silicon realized during the process development, for more information see the documents provided with the IO library.

7.5.5 ADDITIONAL GUIDELINES FOR GATE OXIDE PROTECTION

Analog Applications

The gates of core thin oxide and OD2 thick oxide transistors in mismatch sensitive configurations shall be tied to an active region by M1 to prevent any Vt shift caused by process induced damage.

Antenna Diodes in Multiple Voltage Designs

Any p-type antenna diode MUST be included in the schematics. The use of p-type antenna diodes as floating gate ties is strongly discouraged for designs with multiple power supplies. Some organizations will not approve any designs with p-type antenna diodes in their libraries for reuse.

Direct Connection of Gates to Power Supply

Direct connections of gates of low-voltage transistors to power supply nodes shall be avoided to reduce the risk of gate oxide damage and increase of gate leakage current.

7.5.6 SHEAR STRESS DESIGN RULES

General rule: Designing of the product must be in agreement with the shear stress design rules of the target final manufacturing (assembly) organization. Shear stress rules need to be followed in order to minimize reliability problems related to the mechanical and thermal stresses seen by dielectric layers during plastic packaging. The most important rules to be applied on large metal lines in IO (PAD plus ESD protection circuitry) design and corner of the circuits are:

- Run metal at a global 45° angles in the corner of the die.
  Reason: distributes force along a line instead of a point.
- Slot all wide metal lines in the IO circuit.
  Reason: slots acts as stress relief points on the metal.
- No active circuitry in the corner of the die.
  Reason: this is the area with the highest stress.

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7.5.7 FILLING PROCEDURE FOR DENSITY RULES (DUMMY GENERATION)

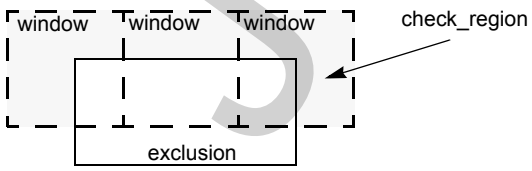
7.5.7.1 Density Rules Summary

In order to meet the extremely tight requirements in terms of process control for STI etch and polish, channel length definition as well as Inter-Level Dielectric (ILD) planarization, density requirements have to be strictly followed.

Density Design Rules			
OD.D.1	Max space without OD or OD;dummy		40.000
OD.R.2	Minimum OD + OD;dummy density across full chip		25%
OD.R.2.1	Maximum OD + OD;dummy density across full chip		75%
OD.R.3	Minimum OD + OD;dummy density over local 150um x 150um areas stepped in 75um increments		20%
OD.R.3.1	Maximum OD + OD;dummy density over local 150um x 150um areas stepped in 75um increments. Rule applies if window contains any active OD (Source/Drain) that is not covered with OD2.		80%
OD.R.3.2	Maximum OD + OD;dummy density over local 150um x 150um areas stepped in 75um increments within OD2. Rule applies if all active OD (Source/Drain) within the window is covered with OD2.		90%
PO.R.1	Min PO density across full chip after dummies insertion		14%
PO.R.2	Max PO density across full chip after dummies insertion		50%
M1.R.2	M1 density over local 100 um x 100 um areas stepped in 50um increments [a]. Dummy patterns (M1;dummy and M1;dummy_O) are required to keep density > 15%. Exclusions from minimum density check: M1 under MKR;inddmy.		15%
M1.R.2.1	Maximum M1 density over local 100 um x 100 um areas stepped in 50um increments.		70%
M1.R.4	M1 widths and spaces have to be chosen such that Maximum M1 density over local 20 um x 20 um areas stepped in 10 um increments cannot exceed this value		90%
Mx.R.1	Metal density over local 100 um x 100 um areas stepped in 50um increments. Dummy patterns (Mi;dummy and Mi;dummy_O) are required to keep density > 15%. Exclusions from minimum density check: Mx under MKR;inddmy.		15%
Mx.R.1.1	Maximum Metal density over local 100 um x 100 um areas stepped in 50um increments.		70%
Mx.R.4	Mi widths and spaces have to be chosen such that Maximum Mi density over local 20 um x 20 um areas stepped in 10 um increments cannot exceed this value		90%
Mn.R.1	Metal density over local 100 um x 100 um areas stepped in 50 um increments. Dummy patterns (Mi;dummy) are required to keep density > 20%. Exclusions from minimum density check: Mtop under BOTMIM, Mn under MKR;inddmy.		20%
Mn.R.1.1	Maximum Metal density over local 100 um x 100 um areas stepped in 50um increments. Exclusions from maximum density check: Mtop under CB, CB;via.		80%
Mn.R.4	Mi widths and spaces have to be chosen such that Maximum Mi density over local 20 um x 20 um areas stepped in 10 um increments cannot exceed this value (Exclusions: Mtop under CB, CB;via)		90%
AP.R.2	Minimum AP density after dummy insertion across full chip [b]		10%
AP.R.2.1	Maximum AP density across full chip [b]		60%

a.The window size for the automated tiling routine is 50um x 50um stepped by 25um.
b.Density calculation does take into account the shapes generated from CB.

Handling of exclusion zones:



The density calculation is performed in
check_region = {window minus exclusion}.
The rule is applied only for
check_region with width > 1/4 window size.

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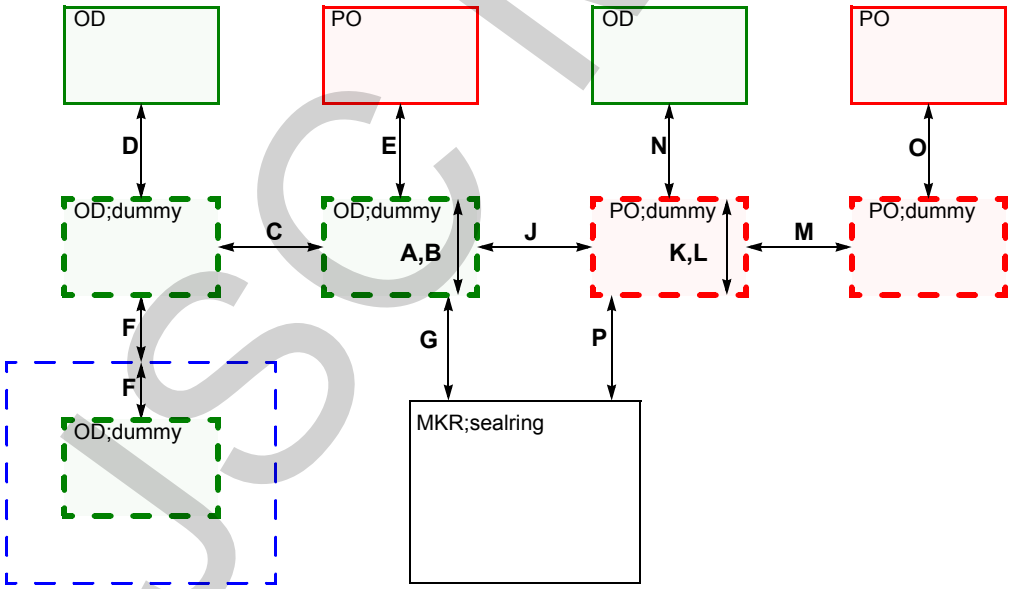
7.5.7.2 Fill Pattern (Dummy) Design Rules

a) General guidelines

- Dummy fill pattern should be well dispersed if possible to maximize process uniformity at etching and chemical mechanical planarization
- Unless otherwise specified in rules below a minimum recommended Dummy fill pattern distance to real design shapes or letters on the same level is 1.5um.
- Dummy shapes should be drawn as solid blocks (lines or squares). They need to be dense enough to raise the metal density to the above min values.
- Designers are responsible for excluding dummy shapes from regions bordering structures that could be sensitive for functionality or performances reasons.
- The above recommended metal fill design rules are not checked in the DRC. It only checks the density rules.

b) OD and PO

OD;dummy/PO;dummy Design Rules			
DOD.W.1	Minimum OD;dummy Width	A	0.500
DOD.W.2	Maximum OD;dummy Width	B	5.000
DOD.S.1	Minimum OD;dummy Space	C	0.400
DOD.D.1	OD;dummy Distance to OD (not allowed to interact with OD)	D	0.600
DOD.D.2	OD;dummy Distance to PO (not allowed to interact with PO)	E	0.600
DOD.D.3	OD;dummy Distance to NW/PW boundary (OD;dummy must not cross the NW/PW boundary)	F	0.600
DOD.D.5	OD;dummy Distance to MKR;sealring (OD;dummy not allowed in sealring)	G	0.000
DOD.D.7	OD;dummy Distance to PO;dummy (not allowed to interact with each other)	J	0.300
DPO.W.1	Minimum PO;dummy Width	K	0.400
DPO.W.2	Maximum PO;dummy Width	L	5.000
DPO.S.1	Minimum PO;dummy Space	M	0.300
DPO.D.1	PO;dummy Distance to OD (not allowed to interact with OD)	N	0.200
DPO.D.2	PO;dummy Distance to PO (not allowed to interact with PO)	O	0.500
DPO.D.5	PO;dummy Distance to MKR;sealring (PO;dummy not allowed in sealring)	P	0.000



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c) Metals (M1, Mx, and Mn)

Two different types of dummies can be used to meet the density requirements on metals. Regular metal shapes are drawn using the datatype 0, while dummies are drawn in both datatype 1 and datatype 7. Both dummies are used during the Optical Proximity Correction (OPC) of regular metal shapes. Rectangles drawn in datatype 1 are left as is, while rectangles drawn in datatype 7 are modified by the OPC algorithm. Thus, dummies that receive OPC can be placed close to metal lines. The table below summarizes the differences.

	M1 Mx Mn	**M1;dummy Mx;dummy Mn;dummy**	**M1;dummy_O Mx;dummy_O**
	Datatype 0	**Datatype 1**	**Datatype 7**
Referred by OPC	Yes	Yes	Yes
Modified by OPC	Yes	No	Yes
LVS recognition	Yes	No	No

M1;dummy Design Rules			
DM1.W.1	Minimum M1;dummy Width		0.320
DM1.W.3	Maximum M1;dummy Width		3.000
DM1.S.1	Minimum M1;dummy Space		0.400
DM1.A.1	Minimum M1;dummy Area		0.320
DM1.D.1	Minimum M1;dummy Distance to M1 (exclusion zone). Any dummy structure that exceeds length of 4.5, must use an exclusion zone >= 1.5. M1;dummy is not allowed to interact with the corresponding metal drawing layer M1		0.600
DM1.D.4	Minimum M1;dummy Distance to MKR;sealring (dummies not allowed in sealring)		0.000
DM1.R.2	M1;dummy must be rectangles or squares orthogonal to grid		

Mx;dummy Design Rules			
DMx.W.1	Minimum Mx;dummy Width		0.320
DMx.W.3	Maximum Mx;dummy Width		3.000
DMx.S.1	Minimum Mx;dummy Space		0.400
DMx.A.1	Minimum Mx;dummy Area		0.320
DMx.D.1	Minimum Mx;dummy Distance to Mx (exclusion zone). Any dummy structure that exceeds length of 4.5, must use an exclusion zone >= 1.5. Mx;dummy is not allowed to interact with the corresponding metal drawing layer Mx		0.600
DMx.D.4	Minimum Mx;dummy Distance to MKR;sealring (dummies not allowed in sealring)		0.000
DMx.R.2	Mx;dummy must be rectangles or squares orthogonal to grid		

Mn;dummy Design Rules			
DMn.W.2	Minimum Mn;dummy Width		0.600
DMn.W.3	Maximum Mn;dummy Width		3.000
DMn.S.2	Minimum Mn;dummy Space		0.800
DMn.A.2	Minimum Mn;dummy Area		0.600
DMn.D.2	Minimum Mn;dummy Distance to Mn (exclusion zone). Mn;dummy is not allowed to interact with the corresponding metal drawing layer Mn		0.600
DMn.D.4	Minimum Mn;dummy Distance to MKR;sealring (dummies not allowed in sealring)		0.000
DMn.R.2	Mn;dummy must be rectangles or squares orthogonal to grid		

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The Metal;dummy_O shapes must comply to their corresponding drawing metal spacing rules.

Metal;dummy_O Design Rules			
DOM1.A.1	Minimum M1;dummy_O Area		0.070
DOMx.A.1	Minimum Mx;dummy_O Area		0.070
DOM1.R.1	M1;dummy_O are not allowed to interact with M1 or M1;dummy shapes		
DOMx.R.1	Mx;dummy_O are not allowed to interact with Mx or Mx;dummy shapes		
DOM1.R.2	M1;dummy_O must be rectangle or square orthogonal to grid, with a maximum allowed length of 6.0 um and maximum width of 0.21 um		
DOMx.R.2	Mx;dummy_O must be rectangle or square orthogonal to grid, with a maximum allowed length of 6.0 um and maximum width of 0.21 um		

d) AP (ALUCAP)

AP;dummy Design Rules			
DAP.W.1	AP;dummy Width		2.500
DAP.S.1	AP;dummy Space		2.000
DAP.D.1	AP;dummy Distance to AP. Dummies are not allowed to interact with these shapes.		5.000
DAP.D.2	AP;dummy Distance to CB, CB;via, NITRIDE, NITRIDE;bump. Dummies are not allowed to interact with these shapes.		5.000
DAP.D.3	AP;dummy Distance to MKR;inddmy, BOTMIM, and MKR;logo. Dummies are not allowed to interact with these shapes.		5.000
DAP.D.4	AP;dummy Distance to MKR;sealring (dummies not allowed in sealring)		0.000

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7.5.7.3 Procedure for automatic generation of the dummy patterns:

A procedure for the automatic generation of dummy patterns is available in the CMOS090 Design Kit.
This procedure:

- Is aligned to the design rules described in this document for dummy patterns (OD, PO, METALs).
- Includes a feature to allow selective generation of dummy patterns for the METAL layers, so that designers using such a procedure can master the eventual impact of dummy patterns on their design.
- generates dummy patterns (for each related layer) on GDS2 Datatype 1 (refer to §7.2.2).

For more information, refer to the documentation available inside the CMOS090 Design Kit.

Blocking Automatic Dummy Generation

Automatic dummy generation is blocked from areas that are covered with the respective tile block layer:

Tile Block CAD Levels	
Name	**Number;datatype**
OD;tileNot	150;20
PO;tileNot	150;21
M1;tileNot	150;1
M2;tileNot	150;2
M3;tileNot	150;3
M4;tileNot	150;4
M5;tileNot	150;5
M6;tileNot	150;6
M7;tileNot	150;7
AP;tileNot	150;22
BOTMIM;tileNot	150;23

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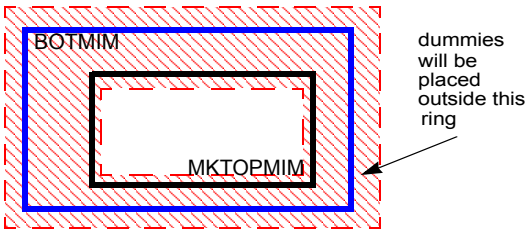
Exclusion zone values for the dummy generation procedure

Existing shapes \ Generated dummy shapes	OD;dummy *first / second* **min**	PO;dummy *default* **min**	M1;dummy *first / second* **min**	M1; dummy_O	Mx;dummy *first / second* **min**	Mx; dummy_O	Mtop;dummy *default* **min**		AP;dummy	BOTMIM; dummy
OD	*1.5 / 0.6* **0.6**	*1.5* **0.2**								
OD;dummy	0.4	0.3								
OD;tileNot	0.0									
PO	*1.5 / 0.6* **0.6**	*1.5* **0.5**								
PO;dummy	0.3	0.3								
PO;tileNot		0.0								
NW boundary	0.6									
M1			*1.5 / 0.6* **0.4**	0.14						
M1;dummy			0.4	0.6						
M1;dummy_O			0.6	0.14						
M1;tileNot			0.0	0.0						
Mx					*1.5 / 0.6* **0.4**	0.14				
Mx;dummy					0.4	0.6				
Mx;dummy_O					0.6	0.14				
Mx;tileNot					0.0	0.0				
Mtop							*1.5* **0.6**	0.42		5.0
Mtop;dummy							0.8	0.6		
Mtop;tileNot							0.0	0.0		
AP									5.0	
AP;dummy									2.0	
AP;tileNot									0.0	
CB					0.0 [b]	0.0 [b]	0.0	0.0	5.0	0.0
MKR;inddmy	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	5.0	0.0
MKR;logo [a]							0.0	0.0	5.0	5.0
MKR;sealring	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
MKR;wb					0.0 [b]	0.0 [b]	0.0	0.0	0.0	0.0
MKR;tp									0.0	0.0
BOTMIM									5.0	2.5
BOT-MIM;dummy										2.5
BOTMIM;tileNot										0.0
donut BOTMIM MKTOPMIM [c]							3.5 0.5 [c]	3.5 0.5 [c]		

a.MKR;logo blocks the dummy generation for Mtop, AP and BOTMIM. Refer to §7.4.7.2 for information on MKR;logo

b.only M4 and above. M1, M2, M3 are generated.

c.The exclusion zone is calculated as the {(BOTMIM upsized by 3.5 um) .not. (MKTOPMIM upsized by -0.5 um)}.



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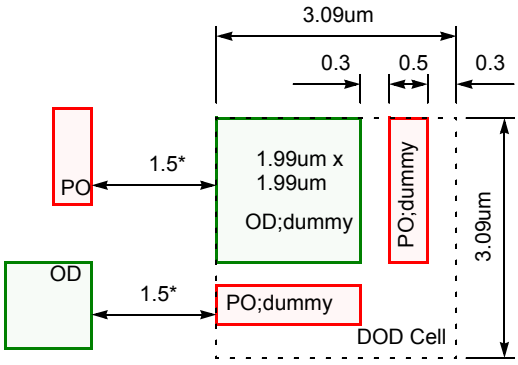
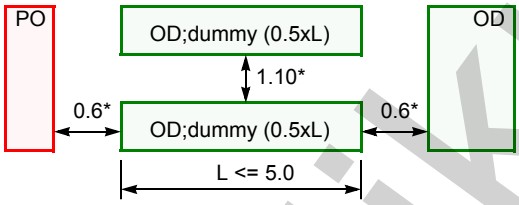
DUMMY OD and PO generation

The standard OD and PO dummy generation procedure includes the following steps. Values marked with an asterisk (*) are default values and are user customizable.

1. Insert OD;dummy/PO;dummy following the below DOD Cell configuration:



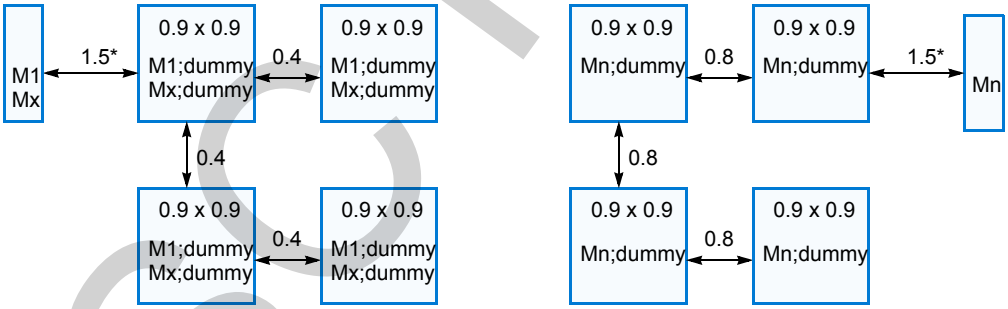
2. Insert OD;dummy rectangles in horizontal and vertical direction:



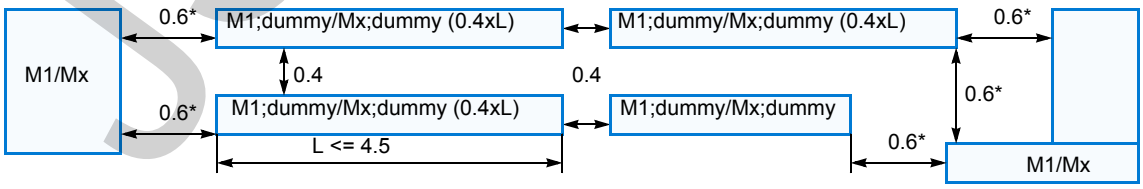
DUMMY METALs generation

The standard metal dummy generation procedure includes the following steps. Values marked with an asterisk (*) are default values and are user customizable.

1. For M1, Mx, and Mn insert square dummies in low density (<20%*) regions (100um x 100um):



2. For M1, Mx insert rectangular dummy stripes in horizontal and vertical direction in low density (<20%*) regions (100um x 100um):



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7.6 RELIABILITY DESIGN RULES

7.6.1 RELIABILITY DESIGN RULE INTRODUCTION

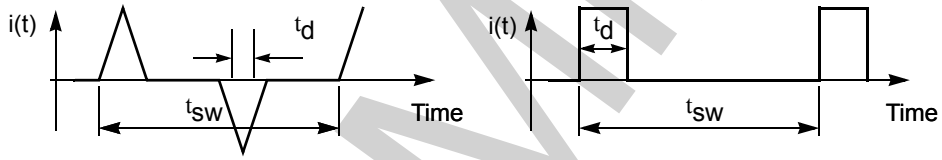
The transistor and interconnect reliability rules presented in the following sections include several assumptions about device application requirements, including expected use time, junction temperature, and acceptable cumulative percent failure at the end of product life. In particular, target applications are assumed to specify a cumulative failure in the range of 0.01% to 0.1% (or 100ppm to 1000ppm) after 100,000 device-power-on hours at junction temperatures of 105, 110 and 125°C. Adjustments for other junction temperatures, power-on hours (POH), cumulative percent failure, and device failure criteria are given, where available, for each of the mechanisms covered: electromigration, time-dependent gate oxide breakdown, and transistor degradation due to hot-carrier injection or negative bias temperature instability. When applications are more stringent, the adjustment factors must be applied. When applications are less stringent, adjustment factors should be used only when it is absolutely certain that the devices will never be used at more stringent conditions.

Except in the case of HCI, products designed to the higher junction temperature specifications for each failure mechanism will exhibit equivalent or better reliability in lower temperature applications; for HCI, products designed to the lowest junction temperature specifications will exhibit better reliability under higher temperature operation. To ensure IP portability, it is recommended that requirements should be determined in consultation with the appropriate Product Reliability and Quality Engineering organization.

7.6.2 ELECTROMIGRATION DESIGN RULES

7.6.2.1 Terminology and Symbol Definitions

- **Operating Switching Time (t_{sw}):** Minimum time between successive current switching operations.



- **Current Operating Frequency (f_{sw}):** $1/t_{sw}$
- **Puls Duration (td):** Duration of current flow (based on average current during non-zero current flow).
- **Duty Ratio (r):** $r = \frac{t_d}{t_{sw}} = \frac{|i|_{dc}}{i_{peak}}$
- **Switching Factor (s):** Fraction of operating cycles over the life of the product during which a given circuit switches.
- **Average DC Current (i_{dc}):** $i_{dc} = \frac{s}{t_{sw}} \int_0^{t_{sw}} i(t)dt$, $|i|_{dc} = \frac{s}{t_{sw}} \int_0^{t_{sw}} |i(t)|dt$

  Note that for pure AC current, i_{dc} is zero.

- **RMS Current (i_{rms}):** $i_{rms} = \sqrt{\frac{s}{t_{sw}} \int_0^{t_{sw}} i^2(t)dt}$
- **Peak current (i_{peak}):** $i_{peak} = \max(|i(t)|)$

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7.6.2.2 EM Fail Types and Corresponding Current Limits

Rules are given to protect against two types of current-induced fails: standard EM and local heating enhanced EM:

- For standard EM the rules define
  - a maximum DC current Idc: $\mathbf{i_{dc} < I_{dc}}$
- For local-heating enhanced EM the rules define
  - a maximum RMS current Irms: $\mathbf{i_{rms} < I_{rms}}$
  - and in addition, a maximum peak current Ipeak: $\mathbf{i_{peak} < I_{peak\_eff}}$

For any current signal i(t) all three conditions ($\mathbf{i_{dc} < I_{dc}}$, $\mathbf{i_{rms} < I_{rms}}$, and $\mathbf{i_{peak} < I_{peak\_eff}}$) have to be fulfilled.

Ipeak_eff is the current at which metal line will have excessive Joule heating and will possibly start melting. Design should stay away from Ipeak_eff as far as possible. The limit Ipeak_eff can be calculated by the following formula:

$$I_{peak\_eff} = \frac{I_{peak\_DC}}{\sqrt{r}}$$

where Ipeak_DC is approximated by a multiple of Imax, and the multiplication factor is shown in §7.6.2.4. The Ipeak rule is applied to the periodical AC or pulsed DC signals. For single event high current pulse or signals cannot be specified by duty ratio, please follow the ESD rules.

The Ipeak_DC approximation is applicable to signals with pulse duration (td) less than 1μs. No temperature adjustment factor for the Irms and Ipeak is given.

7.6.2.3 EM Current Limit Translation into Line Capacitance

For the typical CMOS situation where circuits are used to charge and discharge capacitances, the following formula may be used to translate EM line current limits into load capacitance limits.

For periodic signals, the capacitive load is limited by either the Idc or the Irms current:

- if the signal is asymmetrical bi-directional (with a DC current component), the maximum capacitive load is approximated by

$$C_{max} = \frac{I_{dc}}{V \cdot f}$$

- if the signal is symmetrical bi-directional (with no net DC current component), the maximum capacitive load is approximated by

$$C_{max} = \sqrt{\frac{r}{2}} \cdot \frac{I_{rms}}{V \cdot f}$$

where

I_{dc}, I_{rms}	current limits in mA
V	voltage in volts
f	frequency in MHz
C_{max}	capacitance in nF
r	duty factor, as defined in §7.6.2.1

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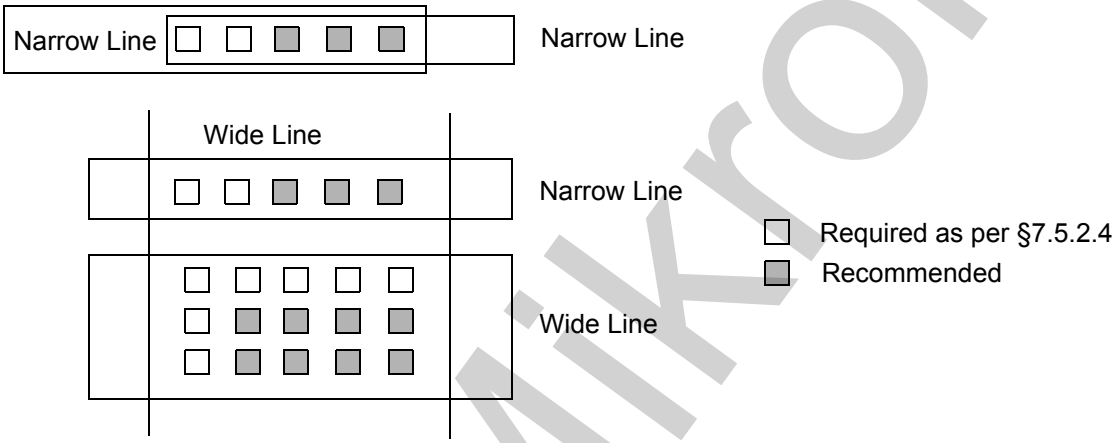
7.6.2.4 General Metal Line Rules at 105, 110 and 125C/100K POH

The tables in this section provide the maximum allowed Idc, Irms and Ipeak for each of the metal wiring levels for the CMOS090 High Density backend option at junction temperatures of 105, 110 and 125°C. In the tables, W represents the width of the metal line. The Irms rules limit the local temperature rise due to Joule heat to 5°C above the junction temperature.

In the case of narrow stripes where only a single via or contact fits along the width, the general rules can be applied by using two or more contacts or vias along the line length consistent with the limits provided in §7.6.2.5. The general rules can be applied for cases of wide lines, provided the maximum number of contacts or vias allowed along the width are used. For a wide line crossing over a wide line, the general rule can be applied by using the maximum number of contacts or vias to create an L-shaped array (see example). Additional redundant vias are recommended for use, where possible.



EM Line Current Limits (High Density Backend) (Tj <= 105C)			
Metal Level	**Idc (mA)**	**Irms (mA)**	**Ipeak_DC (mA)**
M1 (M1)	3.036 * (W - 0.02)	sqrt [93.83 * (W-0.02) * ((W-0.02) + 0.484)]	16.45 * Idc
M2 (Mx)	4.026 * (W - 0.02)	sqrt [30.08 * (W-0.02) * ((W-0.02) + 0.654)]	8.07 * Idc
M3 (Mx)	4.026 * (W - 0.02)	sqrt [15.77 * (W-0.02) * ((W-0.02) + 1.248)]	8.07 * Idc
M4 (Mx)	4.026 * (W - 0.02)	sqrt [10.68 * (W-0.02) * ((W-0.02) + 1.842)]	8.07 * Idc
M5 (Mx)	4.026 * (W - 0.02)	sqrt [8.08 * (W-0.02) * ((W-0.02) + 2.436)]	8.07 * Idc
M6 (Mn)	11.616 * (W - 0.02)	sqrt [13.10 * (W-0.02) * ((W-0.02) + 4.159)]	5.42 * Idc
M7 (Mn)	11.616 * (W - 0.02)	sqrt [11.68 * (W-0.02) * ((W-0.02) + 4.664)]	5.42 * Idc
AP	3.55 * (W - 0.10)	sqrt[7.42 * (W-0.10) * ((W-0.10) + 5.160)]	

EM Line Current Limits (High Density Backend) (Tj = 110C)			
Metal Level	**Idc (mA)**	**Irms (mA)**	**Ipeak_DC (mA)**
M1 (M1)	2.116 * (W - 0.02)	sqrt [92.55 * (W-0.02) * ((W-0.02) + 0.484)]	23.58 * Idc
M2 (Mx)	2.806 * (W - 0.02)	sqrt [29.68 * (W-0.02) * ((W-0.02) + 0.654)]	11.57 * Idc
M3 (Mx)	2.806 * (W - 0.02)	sqrt [15.55 * (W-0.02) * ((W-0.02) + 1.248)]	11.57 * Idc
M4 (Mx)	2.806 * (W - 0.02)	sqrt [10.54 * (W-0.02) * ((W-0.02) + 1.842)]	11.57 * Idc
M5 (Mx)	2.806 * (W - 0.02)	sqrt [7.97 * (W-0.02) * ((W-0.02) + 2.436)]	11.57 * Idc
M6 (Mn)	8.096 * (W - 0.02)	sqrt [12.92 * (W-0.02) * ((W-0.02) + 4.159)]	7.78 * Idc
M7 (Mn)	8.096 * (W - 0.02)	sqrt [11.53 * (W-0.02) * ((W-0.02) + 4.664)]	7.78 * Idc
AP	3.55 * (W - 0.10)	sqrt[7.32 * (W-0.10) * ((W-0.10) + 5.160)]	

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EM Line Current Limits (High Density Backend) (Tj = 125C)			
Metal Level	**Idc (mA)**	**Irms (mA)**	**Ipeak_DC (mA)**
M1 (M1)	0.759 * (W - 0.02)	sqrt [88.93 * (W-0.02) * ((W-0.02) + 0.484)]	65.79 * Idc
M2 (Mx)	1.007 * (W - 0.02)	sqrt [28.51 * (W-0.02) * ((W-0.02) + 0.654)]	32.23 * Idc
M3 (Mx)	1.007 * (W - 0.02)	sqrt [14.94 * (W-0.02) * ((W-0.02) + 1.248)]	32.23 * Idc
M4 (Mx)	1.007 * (W - 0.02)	sqrt [10.13* (W-0.02) * ((W-0.02) + 1.842)]	32.23 * Idc
M5 (Mx)	1.007 * (W - 0.02)	sqrt [7.66 * (W-0.02) * ((W-0.02) + 2.436)]	32.23 * Idc
M6 (Mn)	2.904 * (W - 0.02)	sqrt [12.42 * (W-0.02) * ((W-0.02) + 4.159)]	21.69 * Idc
M7 (Mn)	2.904 * (W - 0.02)	sqrt [11.07 * (W-0.02) * ((W-0.02) + 4.664)]	21.69 * Idc
AP	2.60 * (W - 0.10)	sqrt[7.03 * (W-0.10) * ((W-0.10) + 5.160)]	

EM Line Current Limits at minimum Line Width (High Density Backend) (Tj <= 105C)				
Metal Level	**Min Design Width (um)**	**Idc (mA) min. W**	**Irms (mA) min. W**	**Ipeak (mA) min. W**
M1 (M1)	0.12	0.304	2.34	5.0
M2 (Mx)	0.14	0.483	1.67	3.9
M3 (Mx)	0.14	0.483	1.61	3.9
M4 (Mx)	0.14	0.483	1.59	3.9
M5 (Mx)	0.14	0.483	1.57	3.9
M6 (Mn)	0.42	4.646	4.89	25.2
M7 (Mn)	0.42	4.646	4.86	25.2
AP	3.00	10.3	13.4	

EM Line Current Limits at minimum Line Width (High Density Backend) (Tj = 110C)				
Metal Level	**Min Design Width (um)**	**Idc (mA) min. W**	**Irms (mA) min. W**	**Ipeak (mA) min. W**
M1 (M1)	0.12	0.212	2.32	5.0
M2 (Mx)	0.14	0.337	1.66	3.9
M3 (Mx)	0.14	0.337	1.60	3.9
M4 (Mx)	0.14	0.337	1.58	3.9
M5 (Mx)	0.14	0.337	1.56	3.9
M6 (Mn)	0.42	3.238	4.85	25.2
M7 (Mn)	0.42	3.238	4.83	25.2
AP	3.00	10.3	13.4	

EM Line Current Limits at minimum Line Width (High Density Backend) (Tj = 125C)				
Metal Level	**Min Design Width (um)**	**Idc (mA) min. W**	**Irms (mA) min. W**	**Ipeak (mA) min. W**
M1 (M1)	0.12	0.076	2.28	5.0
M2 (Mx)	0.14	0.121	1.63	3.9
M3 (Mx)	0.14	0.121	1.57	3.9
M4 (Mx)	0.14	0.121	1.54	3.9
M5 (Mx)	0.14	0.121	1.53	3.9
M6 (Mn)	0.42	1.162	4.76	25.2
M7 (Mn)	0.42	1.162	4.74	25.2
AP	3.00	7.55	13.1	

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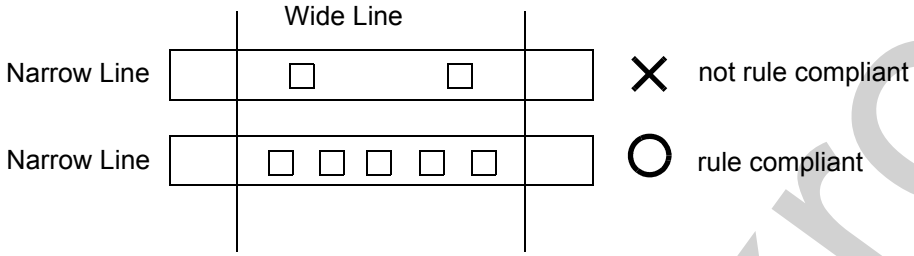
7.6.2.5 Contact and Via Rules

The maximum current (Idc) allowed through all contact and via interfaces is described below. The number of contacts and vias placed across a line (perpendicular to direction of current flow) must be maximized (increased as soon as the line width permits, per layout rule restrictions). For use of multiple vias, the allowable current values equal the allowable current per via times the number of vias (please see the discussion in §7.6.2.4). In all cases, the total current must not exceed the interconnecting metal line current limit given in §7.6.2.4. For determining the necessary number of vias (considering Idc, Irms and Ipeak) please proceed as follow: (1) from the Idc, Ipeak and Irms currents in the connected line determine the necessary line width w_line; (2) for that line width w_line calculate the maximum allowed Idc_line from the EM Line Current Limits tables; (3) calculate the number of contacts or vias required to carry Idc_line: number_of_vias = Idc_line / Idc_via.



Multiple vias or arrays of vias must be used to increase reliability by providing redundancy in the case of blocked or resistive vias.

EM Current Limits for Contacts and Vias (High Density Backend)			
Contact/Via	**Idc (mA) per CO/VIA T <= 105C**	**Idc (mA) per CO/VIA T = 110C**	**Idc (mA) per CO/VIA T = 125C**
CO	0.423	0.294	0.105
VIAx	0.483	0.337	0.121
VIAn	4.646	3.238	1.162
CB;via (1umx1um)	3.30	3.30	2.36
CB;via (>3um)	7.00	7.00	5.00

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7.6.3 TRANSISTOR RELIABILITY DESIGN RULES

7.6.3.1 Overview of Power Supply

The nominal and overdrive conditions for every type of transistor are summarized in the table below. The reliability data (Oxide lifetime, HCI and NBTI) are fulfilled for the listed biasing conditions. Note that the most critical data for the LP overdrive is the HCI NMOS performance.

	Nominal and Over-drive operation	Nominal channel length	Typical Ion (uA/um) @ Vdd nom	Fast Ion (uA/um) @ Vdd nom
LP (21A)	1.2 V +10% nominal	0.10um	NMOS: 411 PMOS:191	NMOS: 501 PMOS:235
	1.4 V +5% overdrive	0.10um		
OD25 (50A)	2.5 V +10% nominal	0.28 um	NMOS: 580 PMOS: 290	NMOS: 653 PMOS: 347
	3.0 V +10% overdrive	0.30 um		
	3.3 V +10% overdrive	0.50 um		

7.6.3.2 Hot Carrier Injection Degradation (HCI)

7.6.3.2.1 General - About the HCI Degradation Mechanism

A degradation in FET device characteristics occurs as a result of exposure to high drain to source bias, over time. Hot electron effects will limit the voltages that may be used with CMOS90 devices, and are most severe at shorter channel lengths. Detailed models to calculate device degradation during circuit operation and to simulate the impact on circuit operation are available, but as a general rule the degradation of device characteristics can be approximated using

$$\mathrm{ttf} = A \cdot \left(\frac{\Delta}{10\%}\right)^{1/n} \cdot L^{m} \cdot \exp\left(B \cdot \left[\frac{1}{Vd} - \frac{1}{Vd0}\right]\right)$$

where Δ represents the percentage degradation of an electrical parameter (e.g. 10% Idsat, 10% Gm), L is the drawn channel length, Vds is the drain to source bias, and Vd0 is typically VDD+10% (VDD is the nominal supply voltage, for overdrive conditions the tolerance may be less than 10%). A, B, n and m are constants determined empirically. When L is measured in drawn microns, Vd and Vd0 in volts, ttf is given in years. The values of the constants (A, B, n, m) are listed in the below tables for each device type.

In order to avoid HCI-induced drift in transistor characteristics and hence loss of proper circuit functionality (including but not limited to degradation in timing and/or input/output transfer characteristics), the total time that each device is operated under worst-case bias conditions over the anticipated life of the product must not exceed the lifetime given in the below tables. For certification purposes, nominal channel length devices are tested to ensure that their lifetime for a 10% change in forward Idsat is at least 0.2 years under a static Vds bias of Vd0 at a junction temperature of 25°C.

For a given Lpoly, Vbs and temperature, worst case HCI stress occurs under the following device bias conditions:

- 50A devices:
  NMOS: 0.7Vds >= Vgs >= 0.3Vds, Vds >= Vdd/2
  PMOS : Vds >= Vgs >= Vt, Vds >= Vdd/2
- 21A devices:
  NMOS: Vds >= Vgs >= Vt, Vds >= Vdd/2
  PMOS : Vds >= Vgs >= Vt, Vds >= Vdd/2

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7.6.3.2.2 Hot Carrier Injection Lifetime

The parameters to determine HCI lifetime of a typical transistor (Idsat typ) for various degradation criteria (Idsat, Idlin, and Gm) are provided in the below tables. Adjustment factors for forward vs. reverse operation are given. In addition adjustment factors are given depending on the transistor drive current for fast transistor (Idsat bcs), and slow transistor (Idsat wcs).

The forward Idsat, Idlin and gm_lin lifetimes presented in the below tables apply when unidirectional current flow is anticipated through a device. The reverse lifetimes apply when bidirectional current flow is anticipated through a device. In those instances where bidirectional current flow is anticipated, the A value given in the below tables should be divided by the Fwd/Rev ratio to determine the worst-case lifetime.

HCI Degradation Parameters (T=25C)										
Device	**Parameter**	**Vd0 [V]**	**L [um]**	**n**	**A [yrs]**	**B [V]**	**m**	**Fwd / Rev**	**Typ / Fast**	**Slow / Typ**
LP NMOS (21A)	Fwd Idsat 1.2V	1.32	0.10	0.48	3.5e11	55.8	9.1	2.6	11.8	12.4
	Fwd Idlin	1.32	0.10	0.39	3.6e11	57.3	9.2			
	Fwd Gmlin	1.32	0.10	0.47	5.6e11	55.6	10.5			
	Fwd Vtlin	1.32	0.10	0.47	3.5e11	56.0	9.2			
	Fwd Idsat 1.4V	1.47	0.10	0.48	9.5e9	55.8	9.1	2.6	11.8	12.4
OD25 NMOS (50A)	Fwd Idsat 2.5V	2.75	0.28	0.5	2.52e5	83.4	8.3	1.2	3.18	3.19
	Fwd Idlin	2.75	0.28	0.22	2.65e4	91.7	9.2			
	Fwd Gmlin	2.75	0.28	0.38	4.71e2	82.9	7.5			
	Fwd Vtlin	2.75	0.28	0.55	1.6e6	70.8	7.5			
	Fwd Idsat 3.0V	3.3	0.30	0.5	2.84e3	84.4	8.2	1.2	3	3
	Fwd Idsat 3.3V	3.6	0.50	0.5	3.08e2	94.1	8.2	1.2	3	3

HCI Degradation Parameters (T=125C)										
Device	**Parameter**	**Vd0 [V]**	**L [um]**	**n**	**A [yrs]**	**B [V]**	**m**	**Fwd / Rev**	**Typ / Fast**	**Slow / Typ**
LP PMOS (21A)	Fwd Idsat 1.2V	1.32	0.10	0.21	1.3e7	54.6	5	3.5	2.8	2.8
	Fwd Idlin	1.32	0.10	0.20	4.9e9	56.2	6.8			
	Fwd Gmlin	1.32	0.10	0.24	7.7e9	57.0	7.2			
	Fwd Vtlin	1.32	0.10	0.24	3.3e7	50.7	6.3			
	Fwd Idsat 1.4V	1.47	0.10	0.17	7.2e5	57.1	5	3.5	2.8	2.8
OD25 PMOS (50A)	Fwd Idsat 2.5V	2.75	0.28	0.25	2.3e4	101.3	6.7	1.6	3	3
	Fwd Idlin	2.75	0.28	0.25	2.1e5	97.2	7.6			
	Fwd Gmlin	2.75	0.28	0.21	2.84e5	95	8.7			
	Fwd Vtlin	2.75	0.28	0.29	6.75e2	86.6	7.1			
	Fwd Idsat 3.0V	3.3	0.30	0.2	1.47e3	100	6.7	1.6	3	3
	Fwd Idsat 3.3V	3.6	0.50	0.2	2.03e2	100	6.7	1.6	3	3

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7.6.3.2.3 HCI Guidelines for Analog Applications

In order to guarantee 10 year device DC drift-time for a 10% change in parameters typically considered important in sensitive analog applications, it is mandatory to increase the drawn channel length for both NMOS and PMOS transistors to take into account the degradation induced by hot-carrier injection under worst-case bias conditions. The corresponding guidelines are given in below tables.

Analog Channel Ldrawn Recommendations					
Device	**Parameter**	**L [um] @ 2.75V**	**L [um] @ 3.00V**	**L [um] @ 3.30V**	**L [um] @ 3.60V**
OD25 NMOS (50A)	IdLin	0.43	0.57	0.76	0.96
	GmLin	0.61	0.85	1.15	1.52
	VtLin	0.52	0.69	0.92	1.16
OD25 PMOS (50A)	IdLin	0.30	0.45	0.66	0.92
	GmLin	0.35	0.49	0.68	0.90
	VtLin	0.73	1.01	1.40	1.83

Analog Channel Length Recommendations					
Device	**Parameter**	**L [um] @ 1.20V**	**L [um] @ 1.32V**	**L [um] @ 1.50V**	**L [um] @ 1.65V**
LP NMOS (21A)	IdLin	0.10	0.10	0.14	0.20
	GmLin	0.10	0.10	0.17	0.25
	VtLin	0.10	0.10	0.14	0.19
LP PMOS (21A)	IdLin	0.10	0.10	0.12	0.19
	GmLin	0.10	0.10	0.12	0.20
	VtLin	0.10	0.10	0.20	0.32

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7.6.3.3 Negative Bias Temperature Instability (NBTI)

This section aims at providing to circuit designers information and design guidance to deal with Negative Bias Temperature Instability in 90nm CMOS technologies.

7.6.3.3.1 General - About the NBTI Degradation Mechanism

Negative Bias Temperature Instability (NBTI) is a vertical field induced mechanism that causes degradation at the $Si\text{-}SiO_2$ interface and its vicinity due to an applied negative gate bias at high temperature. Though a lot of work has been carried out, a common understanding of the phenomenon has not yet been reached in the literature. The degradation proceeds with time following a power law,

$$\text{Degradation} \propto t^n \qquad (1)$$

and the time exponent, n, is typically lies in the range of 0.15-0.25 that points to a diffusion-limited mechanism. The degradation depends exponentially on Vgs - increased Vgs presenting higher degradations and is activated by temperature.

Degradation features

NBTI degradation takes place in the absence of any current flow in the channel, that is, under dc conditions. For example, if a digital IO cell doesn't switch for some days, e.g., in standby mode, then parts of the circuit are actually undergoing degradation. When it starts to function again, it may have a reduced current drive, higher propagation delay, changed switching threshold, or a combination of these. Even when it is operating (switching), the NBT stress is sum of all the time for which the PMOS's Vgs is at -VDD (10 years of switching at 50% duty cycle = 5 years of NBT stress).

The degradation occurs uniformly along the entire channel area. The interface states and trapped charges, created during NBT stress, contribute to a net positive charge at the interface for the PMOS increasing the absolute value of threshold voltage. The mobility is also affected due to the interaction of the carriers with the interface states. Consequently, the current flowing through the channel is affected. As a first approximation, it may be seen that the

$$\frac{\Delta Ion}{Ion} \propto \frac{2\Delta Vth}{(Vgs - Vth)} \quad \text{and} \quad \frac{\Delta Ion}{Ion} \propto \frac{\Delta \mu}{\mu} \qquad (2)$$

Device length dependence

It is normally observed that degradation of Ion is higher for longer devices. This is probably due to short-channel effect screening the interface defects for small channel lengths. This implies that even analog circuits where longer lengths are routinely used are not immune to NBTI, but are immune due to lower operating voltages in general.

Voltage dependence

In addition to the stress voltage dependence, Eqn (2) implies that there is an operating voltage dependence. That is to say, a given damage could impact the current from the device differently based on the operating point. The increase in degradation of saturation currents at lower supply voltage could be a concern in instances where the device operates at a low Vgs, but has Vdd applied during power down. The closer it is to Vth, the higher the influence.

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Temperature dependence

The NBTI phenomenon has a temperature dependence characterized by activation energy of about 0.1eV (which could be a range 0.05-0.15eV depending on the device and the temperature region of operation). This means that there would be a gain by reducing the temperature, but this would not be very large.

Three additional points relevant to the circuit degradation are under investigation:

- frequency dependence of the degradation, that is, to see if there would be a difference in degradation if the circuit operates at 1KHz or 100 MHz.
- examine the property of this degradation to relax upon removal of stress.
- understand the long term behavior of the stress under dc-conditions.

7.6.3.3.2 Idsat and Vth shift due to NBTI stress

Idsat and Vth shift expected for 5 year DC operation under NBTI stress at max VDD and 125°C:

Idsat and Vth shifts for PMOS devices			
	Voltage	**Idsat**	**Vth**
LP PMOS (21A)	1.2V +10%	6.2 %	34 mV
	1.4V +5%	6.2 %	43 mV
OD25 PMOS (50A)	2.5V +10%	6.3 %	71 mV
	3.0V +10%	7.9 %	112 mV
	3.3V +10%	9.1 %	144 mV

7.6.3.3.3 Considerations on NBTI dependence on transistors

Note that:

- Threshold voltage shifts more for thicker oxides than for the thinner oxides
  - Analog circuits are built with thick oxides and these circuits typically show more sensitivity to Vth shift, e.g., in the form of offset voltage, etc.
- Due to the lower VDD, the impact of threshold voltage shift on the Ion of core transistors is higher (Eqn (2))
  - As the digital core is built from these devices, these circuits would typically be sensitive to Ion change, e.g, in the form of critical path delays, propagation time, etc.
  - At the same time, the extrapolated lifetime is much greater than 10 years, and this would enable reliable operation of the circuits.

7.6.3.3.4 Influence of NBTI effect on circuits

General influence

Circuit performance parameters that could be potentially impacted by NBTI:

- Propagation delay - increase
- Rise time will be longer for the stage that is under NBTI
- Duty cycle from an inverter - the ratio of high level to low level would decrease since the rise time would be slower and fall time would be slightly faster.
- Setup and hold time for latch/flip-flop
- Switching threshold - will change
- Increase of offset voltage for a differential input if the voltages are very asymmetrical.

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Digital operation

Note that the all PMOS devices in a CMOS digital circuit are subjected to the NBTI stress during the normal switching operation. The NBTI corresponds to the portion of the signal period where the input to the PMOS is at '0' level.

- Impact of power-down
  A standard power down condition would stop all transitions in the circuit, but the supply would still be present. In this condition, the stages having PMOS gate at '0' would have a DC NBTI condition. The ring circuit has an enable signal to study the ring under locked mode conditions (which would emulate power down condition).
- Switching Threshold
  As NBTI degraded PMOS, the switching threshold of the circuit as a whole would vary. For example, this would be felt as the change in input threshold of input IO buffers. In signal paths which are very sensitive to such switching threshold shifts, one way to reduce the drift would be to use inputs with pull-ups, which ensures that there is no NBTI during inactive periods of the IOs. This shift would depend on the Vth shift of the transistor and hence this is expected to be more pronounced for IO (OD25) circuits.
- Consumption
  Since the PMOS becomes slower, the overall consumption reduces with time.
- Leakage currents
  The leakage current would have two opposing aspects. One is that as there are more available energy states within the band gap of the silicon in a degraded PMOS, there would be an increased leakage (as carriers can be exchanged between these states and gate). At the same time, the increased threshold voltage lowers the number of carriers in the silicon, for a given gate voltage and this would reduce the leakage.

Summary for digital circuits: NBTI would not pose a concern to typical digital designs. However, sensitive designs, for example, those working with no margin on critical path, clocks with strict duty cycle constraints or signals with switching threshold constraints have to be careful not to be influenced by a small NBTI degradation.

Analog operation

NBTI in analog circuits is extremely design specific and depends very much on the biasing used and the various modes of operation which see different stresses and can affect other modes of operation. **Analyzing NBTI in analog circuits primarily involves detecting the specific PMOS' that are exposed to NBTI condition in one or more modes of operation and cause sensitivity in the same or another mode of operation.**

Incidentally, certain classes of the analog designs - mainly the linear analog circuits - are automatically “NBTI-free” because:

- Typical operating Vgs is lower than VDD
- During power-down circuits such as PMOS current mirrors tend have their gate nodes pulled up to VDD, resulting in no NBTI. For example, the different PMOS current sources derived from a mirror would all have their gate pulled up to VDD when switched off. All the same, having an additional pull up would be prudent
- Feedback can also help in better immunity against degradation.

The classes of circuits most susceptible to NBTI would be those working with large signals such as comparators, output stages as well as those circuits that are very sensitive to changes to process, voltage, temperature conditions in general, such as start up circuitry.

In the case of matched PMOS devices, a serious offset would result if one of the PMOS is biased with its gate at '0' and the other with its gate at 'VDD'. Circuit robustness depends on what is the design margin taken into account for offset voltage and also what are the other contributions - various random and systematic offsets - that could occur.

- Power down condition
  The power down condition has to be carefully considered in case of analog operation to ensure that there is no critical PMOS undergoing degradation and there are no floating inputs feeding critical transistors such as inputs to differential pairs. The transistors which buffer power-down signal may not be critical with respect to the degradation, since neither their functionality is affected, nor their speed important (but this has to ensured to be so, e.g., if the power-down transistor is a part of start-up circuitry, then a current reduction could affect the functionality).

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Summary for analog operation:

- NBTI degradation in analog circuits would affect those PMOS transistors that have high Vgs (or Vgd) applied.
- Such transistors have to be examined for, taking care to include different modes of operation.
  - This can be typically found by performing dc-analysis for different modes of operation
- Once identified, the sensitivity of the circuit performance to such PMOS transistor has to be checked.
  - For example, one simple way of checking the sensitivity would be to first perform a simulation at fast-fast corner, and replace the PMOS in question by a typical or slow model (but keep in mind that this would be pessimistic).
- If there is a sensitivity, design workarounds would need to be found
  - For example, by making the circuit more tolerant to changes, or design using NMOS instead of PMOS, or even by reviewing the specifications.
- Additionally, it is to be recognized with operating with low Vgs voltages in one particular mode could turn into a disadvantage if another mode of operation, for example, the standby condition, causes an NBTI stress of VDD on the same transistors. As explained before (Eqn 2), this is so as the NBTI degradation results in increase of Vth. Lower the operating Vgs is, the higher the impact of this Vth change would be.

7.6.3.3.5 NBTI guidelines

In this section, the NBTI degradation is quantified as a tentative equation, in order to allow the designer to estimate the shift in Vth or Ion of the transistor undergoing degradation under a specified operating condition. This would help provide a first order estimate of the impact of NBTI on the performance of the circuit. Note that the saturation effects are not taken into account in these equations.

How to use the equations

- Identify the PMOS to be studied
- Running a dc spice analysis, determine the |Vgs| applied on the PMOS
- Estimate the duration of applied stress. For example,
  - if the device is stressed for 10% of the time, then 10 years correspond to 1 year of stress time
  - if the clock has 50% duty cycle, the stress time is half the total time of applied clock
  - for sleep mode/dc operation, the stress time is the total time of sleep mode.
- Determine the temperature of operation
- The current and threshold voltage degradation can be evaluated after keying in the parameters
- Conversely, if the limit of acceptance can be gauged for a device not to affect the circuit performance, such as 5% Ion or 20mV Vth shift, then this value can be used to determine the maximum Vgs in the circuit. This Vgs can then be used as a circuit guideline.

Guidelines to improve immunity against NBTI	
Mode of Operation	**The degradation can be avoided by**
DC Mode and small signal mode	1. Complying with max Vgs and Vgd derived from the equations 2. Reducing asymmetry between stresses of matched devices 3. Using NMOS instead of PMOS
Large signal (CMOS level) switching	1. Complying with max Vgs and Vgd
Power-down conditions	1. Having critical PMOS in non-conducting mode (e.g., this would mean a '1' at the input of an inverter), so that Vgs or Vgd is not negative. 2. Complying with max Vgs and Vgd 3. Reducing asymmetry between stresses of matched devices 4. Ensuring that the devices operating at low vgs conditions are not exposed to VDD during power down. 5. Shutting down the block completely during power-down.

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NBTI equations and parameters

The degradation of forward Idsat and Vt is modeled as

$$ttf = t_1 \cdot e^{-B_1 \cdot V} \cdot e^{E_1/(k_b T)} \cdot \Delta Vt^{1/n_1} \qquad \text{Vt degradation [mV]}$$

$$ttf = t_2 \cdot e^{-B_2 \cdot V} \cdot e^{E_2/(k_b T)} \cdot L^{-m} \cdot \Delta\%Idsat^{1/n_2} \qquad \text{Forward Idsat degradation [\%]}$$

where:

ttf	time to failure (years)
t_1, B_1, E_1, n_1	experimentally determined constant for Vt degradation
t_2, B_2, E_2, m, n_2	experimentally determined constant for Idsat degradation
V	absolute value of gate voltage (V)
k_b	Boltzmann constant k_b = 8.617E-5 eV/K
T	junction temperature (K)
L	gate length (um)
ΔVt, Δ%Idsat	normalized failure criterion (% Idsat or mV Vt degratation)

NBTI Model Parameters - Vt Degradation						
Transistor Type	**L [um]**	**t1 [yrs]**	**B1 [1/V]**	**E1 [eV]**	**-**	**n1**
LP PMOS (21A)	0.10	2.38e-09	9.42	0.487		0.205
OD25 PMOS (50A)	0.28	4.28e-12	4.13	0.497		0.201

NBTI Model Parameters - Idsat Degradation						
Transistor Type	**L [um]**	**t2 [yrs]**	**B2 [1/V]**	**E2 [eV]**	**m**	**n2**
LP PMOS (21A)	0.10	1.01e-09	10.72	0.555	3.889	0.180
OD25 PMOS (50A)	0.28	1.35e-06	4.13	0.497	0.497	0.201

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7.6.3.4 Gate Oxide Reliability

Dielectric Vmax

To protect against time dependent dielectric breakdown (TDDB), the catastrophic destruction of gate oxides induced by a combination of current, voltage and temperature, maximum voltage guidelines (Vmax values) are given below for the CMOS90 technology. These guidelines ensure a reliability performance of 1 FIT for reference conditions (cumulative failure of 0.01% per 100,000 power on device hours or 11.4 years for a gate oxide area of 10^6 um^2 for core and IO oxides) as a function of transistor type, oxide thickness, junction temperature (Tj). Deviations from these guidelines could result in a potentially unreliable integrated circuit. Since the reliability of NMOS and PMOS gate oxide differs from one product to another, separate values are provided for each of these device types; the maximum voltage experienced by each type must be determined on a product-by-product basis and compared to the provided guidelines.

To determine the maximum DC voltages that can be sustained by the circuitry while meeting any given reliability goal, the total on-silicon gate oxide area Aox for all NMOS or PMOS devices, the product lifetime, and the failure rate must be used in the equation below (log - logarithm to base10):

$$V_{max}(A_{ox}, T_j, L, F) = V_0(A_{ref}, T_j, L_{ref}, F_{ref}) - m \times \log\left(\frac{A_{ox}}{A_{ref}}\right) - n \times \log\left(\frac{L}{L_{ref}}\right) + p \times \log\left(\frac{F}{F_{ref}}\right)$$

In the preceding equation:

- V_0 is the reference V_{max} voltage for this technology
- A_{ref} is the on-silicon reference area ($10^6 um^2$)
- T_j is the junction temperature
- L_{ref} is the reference product lifetime (11.4 years = 100,000 hours)
- F_{ref} is the reference failures per 10,000 (1),

and A_{ox}, L, and F are the new oxide area, product lifetime, and failure rate, respectively, that are to be used to compute a new V_{max} value. The parameters m, n, and p are empirical constants which generally vary for each technology and transistor type. The V_{max} that is calculated with this formula should exceed anticipated worst-case biases (including power supply variations and overshoot/undershoot) to ensure reliable operation.

FET Maximum DC Gate Oxide Voltage [a]										
Transistor Type	**EOT [A]**	**Max Gate Voltage (V0(Tj)[V])** at var. junction temp. for reference conditions: Area (Aref = $10^6 um^2$) Product Lifetime (Lref = 11.4 years) Failure Rate [failures in 10,000] (Fref = 1)						**Adjustment Coefficients** for **Area (m)** **Product Lifetime (n)** **Failure Rate (p)**		
		45C	**65C**	**85C**	**105C**	**125C**	**150C**	**m [V]**	**n [V]**	**p [V]**
LP NMOS (21A)	21.0	1.90	1.87	1.84	1.81	1.79	1.77	0.051	0.068	0.051
LP PMOS (21A)	21.0	2.10	2.08	2.04	2.00	1.97	1.93	0.045	0.064	0.045
OD25 NMOS (50A)	50	3.93	3.79	3.66	3.55	3.44	3.30	0.124	0.376	0.124
OD25 PMOS (50A)	50	4.60	4.41	4.24	4.09	3.95	3.79	0.174	0.376	0.174

a.Parameters in this table are related to just one dominating failure mode (oxide dielectric breakdown).

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7.6.3.5 Lifetime for 25-150 C operating conditions

Front-End transistor reliability (TDDB, HCI and NBTI) has been expressed at worst-case temperature for each failure mode. The lifetime at any operating temperature within the 25-150 C range can be extracted by the following Arrhenius law:

$$\text{Lifetime}(T) = \text{Lifetime}(T_{ref}) \cdot \exp\left(E_a \cdot \left(\frac{1}{kT} - \frac{1}{kT_{ref}}\right)\right)$$

with Lifetime (T) being the TDDB, HCI or NBTI lifetime at a given temperature T,
Ea being the activation energy in eV,
Lifetime (Tref) being the lifetime extracted at the reference temperature Tref

The table below summarizes the activation energy for the different reliability mechanisms.

TDDB Activation Energies (Oxide reliability)		
Transistor Type	**EOT [A]**	**Activation Energy [eV]**
LP NMOS (21A)	21.0	0.50
LP PMOS (21A)	21.0	0.81
OD25 NMOS (50A)	50	0.42
OD25 PMOS (50A)	50	0.45

HCI Activation Energies (Transistor reliability)		
Transistor Type	**EOT [A]**	**Activation Energy [eV]**
LP NMOS (21A)	21.0	0.00
LP PMOS (21A)	21.0	0.46
OD25 NMOS (50A)	50	-0.30
OD25 PMOS (50A)	50	0.46

NBTI Activation Energies (Transistor reliability)		
Transistor Type	**EOT [A]**	**Activation Energy [eV]**
LP PMOS (21A)	21.0	0.49
OD25 PMOS (50A)	50	0.50

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7.7 PROCESS PARAMETERS

7.7.1 CONDUCTORS AND DIELECTRICS

CONDUCTORS					DIELECTRICS				
Name	**Thick (A)**	**Th Var (A)**	**W Var (nm)**	**∆CD (nm)**	**Name**		**Thick (A)**	**Th Var (A)**	**k**
					NITRIDE Passivation conformal on ALUCAP	Nitride	6000	600	8.1
ALUCAP conformal on encapsulation	12000	2400	100	0		Oxide	5000	500	4.2
					PADOPEN Encapsulation	Oxide	6000	600	4.2
						Nitride	400	40	8.1
Metal 7 (Mn)	9000 inc. 500 overetch	1400 inc. 50 overetch	42	30	Intrametal dielectric M7	Oxide	7900	1290	4.2
						Nitride	600	60	8.1
Via 6 (VIAn)	6500	650			Intermetal dielectric M7 - M6	Oxide	6400	640	4.2
						Barrier	600	60	5.0
Metal 6 (Mn)	9000 inc. 500 overetch	1400 inc. 50 overetch	42	30	Intrametal dielectric M6	Oxide	7900	1290	4.2
						Nitride	600	60	8.1
Via 5 (VIAn)	6500	650			Intermetal dielectric M6 - M5	Oxide	6400	640	4.2
						Barrier	600	60	4.9
All Mx layers are the same as M2									
All VIAx layers are the same as VIA1									
Metal 2 (Mx)	3300	510	14	25	Intrametal dielectric M2	Low-k	3300	510	2.9
Via 1 (VIAx)	2900	290			Intermetal dielectric M2 - M1	Low-k	2400	240	2.9
						Barrier	500	50	4.9
Metal 1 (M1)	2400 inc. 300 overetch	440 inc. 50 overetch	12	10	Intrametal dielectric M1	Low-k	1800	360	2.9
						Barrier	300	30	4.9
Contact (CO)					PMD oxide and nitride thickness on OD	Oxide	4900 [a]	490 [a]	4.2
Poly (PO)	1500	150	§7.7.2			Nitride	300	30	7.0
					Spacer width/heights	Nitride	§7.7.2		7.0
					Gate oxide	Oxide	§7.1.5		3.9
					STI step height	Oxide	200	200	4.0
					STI depth [b]	Oxide	3500	350	4.0

a.The PMD thickness and variation from top of nitride over PO to bottom of M1 is approximated as 2900 +/-290 and is derived from: PMD oxide on OD - PO thickness - STI_step_height - M1 overetch.
b.STI oxide surface is 200A +/- 200A above OD (active) surface, i.e. for the trench depth measured from top of active to bottom of STI of 3500A +/- 350A, the STI oxide thickness is 3700A +/- 550A.

Standard 3 sigma variation for physical parameters:

- for metal resistance calculation use the sheet resistances from §7.7.3.
- for capacitance calculations use thickness and width variations:
  Thickness: see column Th Var in table above
  Widths: see column W Var in table above

Width for capacitance modeling:

- isolated narrow lines are retargeted (upsized) to achieve manufacturability as described in document ADCS # 7771145 CMOS090 LAYOUT RETARGETING DURING RET. Poly lines have an additional systematic width bias (§7.7.2)
- cross-section of metal lines is approximated by a trapezoid
  Metal bottom CD: designed/retargeted width
  Metal top CD: bottom CD + ∆CD (from table above)

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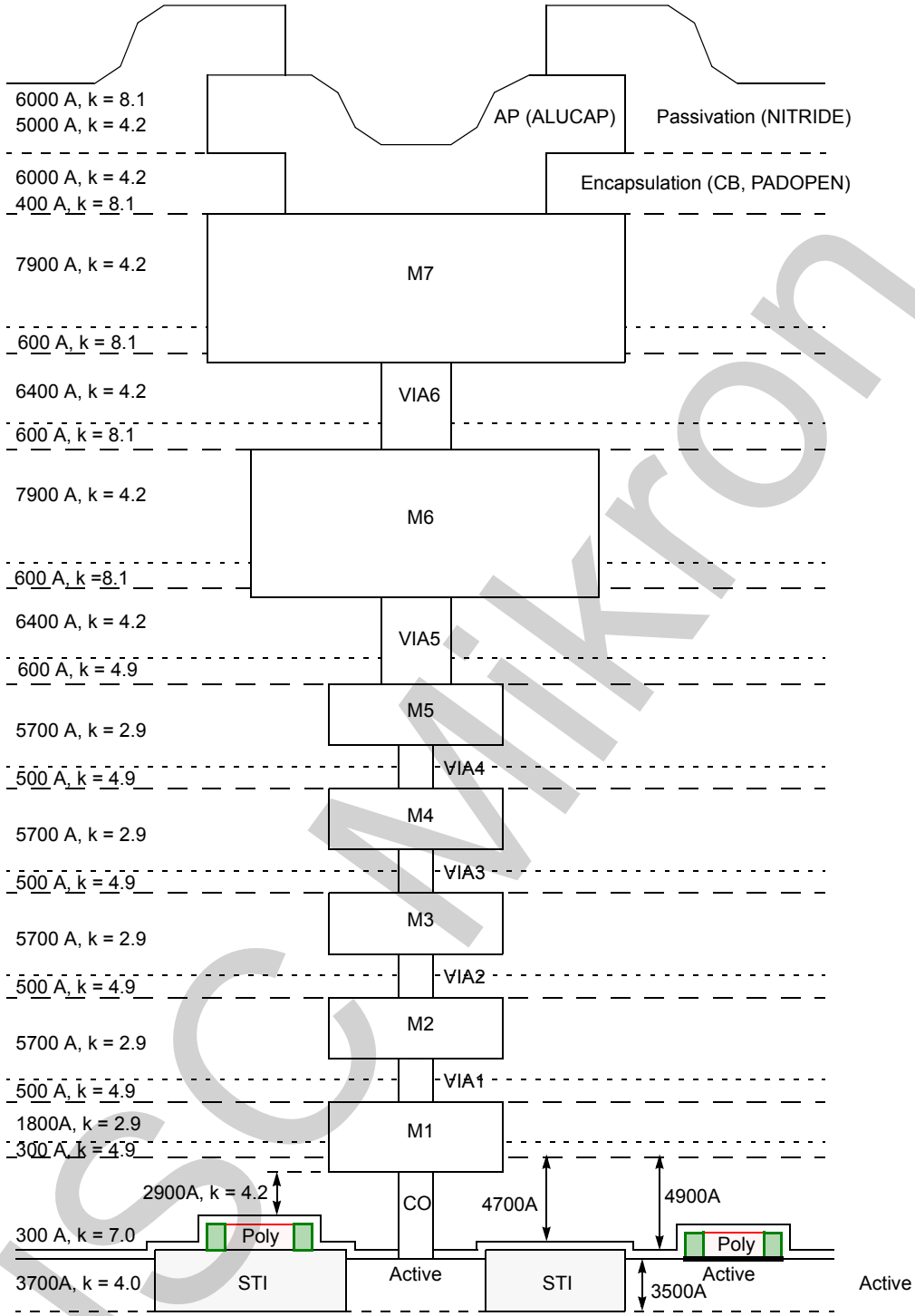
6000 A, k = 8.1
5000 A, k = 4.2
AP (ALUCAP)
Passivation (NITRIDE)
6000 A, k = 4.2
400 A, k = 8.1
Encapsulation (CB, PADOPEN)
7900 A, k = 4.2
M7
600 A, k = 8.1
6400 A, k = 4.2
VIA6
600 A, k = 8.1
7900 A, k = 4.2
M6
600 A, k =8.1
6400 A, k = 4.2
VIA5
600 A, k = 4.9
M5
5700 A, k = 2.9
500 A, k = 4.9
VIA4
M4
5700 A, k = 2.9
500 A, k = 4.9
VIA3
M3
5700 A, k = 2.9
500 A, k = 4.9
VIA2
M2
5700 A, k = 2.9
500 A, k = 4.9
VIA1
1800A, k = 2.9
300 A, k = 4.9
M1
2900A, k = 4.2
CO
4700A
4900A
300 A, k = 7.0
Poly
Poly
3700A, k = 4.0
STI
Active
STI
Active
3500A
Active

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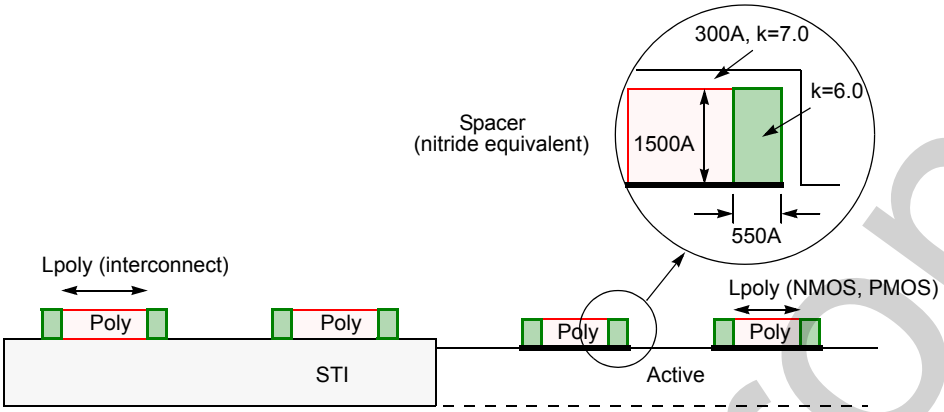
7.7.2 TRANSISTOR PHYSICAL DIMENSIONS

For extraction of parasitic resistances and capacitances associated with each transistor the following dimensions have to be applied for the poly and the spacer along the edge of the poly.



TRANSISTOR PHYSICAL DIMENSIONS			
Parameter	**min design [um]**	**on-silicon [um]**	**Variation [um]**
LP NMOS and PMOS Lpoly (SVT, HVT)	0.10	0.085	0.0105
OD25 2.5V IO NMOS and PMOS Lpoly	0.28	0.265	0.012
LP Interconnect Lpoly	0.10	0.085	0.0105
Equivalent Spacer Width at dielectric constant k=6.0	-	0.055	0.010

7.7.3 SHEET RESISTANCES

SHEET RESISTANCES - FRONT END (25 °C)						
Layer	**MIN [Ohm/sq]**	**TYP [Ohm/sq]**	**MAX [Ohm/sq]**	**TCR [%/K]**	**Imax [mA/um] [a]**	**Matching [%.um]**
Standard Process						
NWELL or NWELLGO2 under OD	280	350	420			
NWELL under Field Oxide	440	550	660			
NWELL+NISO under Field Oxide	220	275	330			
NISO under PWELL under Field Oxide	480	600	720			
PWELL or PWELLGO2 isolated by NISO under Field oxide	600	1000	1400			
Silicided N+ Source/Drain	6	9	15			
Silicided P+ Source/Drain	6	9	15	0.27		
Silicided N+ Poly on field oxide	6	10	16	0.265	1.16	1.02
Silicided P+ Poly on field oxide	6	10	16	0.27	1.16	
Unsilicided P+ Source/Drain	120	150	180	0.141		L<20um:1.93 else:0.57
Unsilicided N+ Source/Drain	70	100	130	0.127		L<20um:5.50 else:1.30
Unsilicided P+ poly	380	440	500	-0.0171	0.195	1.54
Unsilicided N+ poly	80	110	140	0.0136	0.230	4.20
Process Options						
HIPO resistor	800	1000	1200	-0.0633	0.130	1.45

a. Imax is the maximum current allowed prior to a temperature increase of 5C due to Joule self-heating.

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SHEET RESISTANCES - BACK END (25 °C) [a]					
Layer (from bottom to top)	**MIN**	**TYP**	**MAX**		**TCR [%/K]**
M1 (w <= 0.30um)	80	110	140	mOhm/sq	0.27
M1 (w > 0.30um)	65	95	125	mOhm/sq	0.37
Mx (w <= 0.30um)	52	72	92	mOhm/sq	0.30
Mx (w > 0.30um)	52	72	92	mOhm/sq	0.37
Mn	16	22	28	mOhm/sq	0.37
Alucap	18	24	30	mOhm/sq	

a.the variation on sheet resistance includes all process variations at room temperature (width, space, density, and thickness). Resistances are based on bottom CD to be at target drawn dimension.

7.7.4 CONTACT RESISTANCES

CONTACT and VIA RESISTANCES				
Contact type	**MIN**	**TYP**	**MAX**	**UNIT**
CO “Kelvin” structures [a]	10	17	35	Ohm
CO N+ Active	10	18	35	Ohm
CO P+ Active	10	18	35	Ohm
CO Polycide N+	10	17	35	Ohm
CO Polycide P+	10	17	35	Ohm
VIAx	1.0	2.2	4.0	Ohm
VIAn	0.5	0.7	1.5	Ohm
CB;via 1um x 1um	0.1	0.2	0.5	Ohm
CB;via 3um x 3um	0.05	0.1	0.25	Ohm

a.for process monitoring only, “Kelvin Structure” resistance values are not to be used for design.

7.7.5 PARASITIC EXTRACTION - SPECIAL CONSIDERATIONS

7.7.5.1 Process corners

For parasitic extraction, process corners are defined as follows:

PARASITIC EXTRACTION - CORNER DEFINITIONS							
Corner	**Metal th [a]**	**Metal w [a]**	**VIA th [a]**	**k1/k2 [b]**	**VIA res [c]**	**Metal res [c]**	**Temp [c]**
TYP	typ	typ	typ	typ/typ	typ	typ	typ (25C)
RC min	min	min	max	min/min	min	min	typ (25C)
RC max	max	max	min	max/max	max	max	typ (25C)
C min	min	min	max	min/min	min	max	min (-40C)
C max	max	max	min	max/max	max	min	max (105C)
X-talk	max	max	max	max/min	min	min	min (-40C)
Delay	min	min	min	min/max	max	max	max (105C)

a.for capacitance calculation
b.k1 = intra-layer dielectric, k2 = inter-layer dielectric. Currently typ=min=max for all dielectric constants.
c.for resistance calculation

7.7.5.2 Sizing / retargetting of isolated features

Isolated narrow lines are retargeted (upsized) to achieve manufacturability as described in document ADCS # 7771145 CMOS090 LAYOUT RETARGETING DURING RET.

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7.8 DEVICE PARAMETERS

7.8.1 MOS TRANSISTORS

7.8.1.1 General properties for Low Power (LP) 1.2V, Gox 21A, transistors

Ldrawn = 0.10 µm, Wdrawn = 1µm, SA=SB = 0.63µm, Tox = 21A
Min, typ and max are given at 25 °C

Device		Vt typ [a] [V]	Ion typ [µA/µm]	Ioff typ [nA/µm]	Ioff max [nA/µm]	Iginv max [nA/µm]	Avt [mV.µm]
SVT	NMOS	0.37	535	0.3	< 2	< 0.02	<= 6.1
	PMOS	0.39	220	0.3	< 2	< 0.0075	<= 5.2
HVT	NMOS	0.46	400	0.01	< 0.05	< 0.02	<= 6.0
	PMOS	0.51	155	0.01	< 0.05	< 0.0075	<= 3.9

a.linear Vt at Id = 40 nA/µm, Vds = 25 mV

7.8.1.2 General properties for 2.5 Volts IO transistors

Ldrawn = 0.28 µm, Wdrawn = 10µm, SA=SB = 0.82µm, Tox = 50A
Min, typ and max are given at 25 °C

Device		Vt typ [a] [V]	Ion typ [µA/µm]	Ioff typ [nA/µm]	Ioff max [nA/µm]	Avt [mV.µm]	
OD25	NMOS	0.495	575	0.03	< 0.18	8.0 (L<=0.38)	5.0 (L>0.38)
	PMOS	0.459	280	0.06	< 0.3	4.9	4.9

a.linear Vt at Id = 100 nA/µm, Vds =100 mV

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7.8.2 PASSIVE DEVICES

7.8.2.1 Capacitors

Capacitors						
Capacitor Type	**DK name**	**C min** [fF/um2]	**C typ** [fF/um2]	**C max** [fF/um2]	**CV1** [ppm/V]	**matching** [%.sqrt(fF)]
Fringe Capacitor (FMOM) [a]	cfrm1m5	1.00	1.20	1.4	<1	0.75
Metal Plate Capacitor (M1 to M5 stacked)	cm1m2 - cm4m5	0.085	0.10	0.115	<1	0.75
MIM Capacitor	cmimmk	see §7.3.8.7.4				

a.allowed total capacitance: 100fF < Ctot < 10 pF

7.8.2.2 Resistors

PO and OD Resistors							
Resistor Type	**DK name**	**Rs min**	**Rs typ**	**Rs max**	**TCR**	**Imax**	**matching**
N+ Poly silicided	rnpo	see §7.7.3					
N+ OD non-silicided	rnodrpo						
P+ OD non-silicided	rpodrpo						
N+ Poly non-silicided	rnporpo						
P+ Poly non-silicided	rpporpo						
High-Resistance P+ Poly	rhiporpo						
Interconnection N+ Poly line	rnpoi						
Interconnection P+ Poly line	rppoi						
AP resistor	rap						

7.8.3 JUNCTIONS

7.8.3.1 Junctions capacitances and leakages

Refer to the CMOS090 SPICE MODEL PARAMETERS.

7.8.3.2 Junctions breakdown voltage

N+/PWELL junction voltage : - 10 V
P+/NWELL junction voltage : + 10 V.

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7.8.4 MAXIMUM POWER SUPPLY

The 21A thin oxide MOS devices are targeted for nominal power supply voltages of 1.2V.Accounting for a 10% tolerance, the process/devices is qualified for a **max power supply of 1.32V.**

The 50A thick oxide MOS devices (2.5V IO) are targeted for nominal power supply voltages of 1.8V. Accounting for a 10% tolerance, the process/devices is qualified for a **max power supply of 2.75V.**

	Maximum Supported Voltage Operation
LP (21A)	1.2 V +10%
OD25 (50A)	2.5 V +10%

The process has been qualified for these operation conditions. Any deviation from those normal operation conditions may impact product reliability, therefore it has to be validated by the **Risk Assessment Review Board (RARB)**, even if the device is fulfilling the different reliability criteria from the reliability models provided in section §7.5.3.1. A fully documented mission profile must be provided for that purpose.

7.9 CAD TOOLS

7.9.1 SPICE MODELS

Spice models are included in design kit.

7.9.2 DESIGN KIT

The Design Kit is provided by the CCDS organization.

8. QUALITY REQUIREMENTS

Violation of any rule in this document for any reason must be verified in the design/layout review with the process team prior to first tape release.

9. ENVIRONMENTAL / ECOLOGICAL REQUIREMENTS

Environmental procedures and environment instructions for Crolles site are applicable.

They conformed with the defined policy: limitation of energy and material consumptions including chemicals, necessary separation and recycling of waste.

Specific provisions are set up and validated in agreement with the environment management.

(It is recommended to view the document on the screen rather than print it to limit consumption.)

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APPENDIX A: REVISION HISTORY

	Comments/Changes
Revision 1.0 (Rev A)	
Rev1.0_Draft1 10 May 2010	First CMOS090 design rules manual for transfer

END OF DOCUMENT

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