Available online at www.sciencedirect.com

SciVerse ScienceDirect

Procedia Environmental Sciences 10 (2011) 1052 – 1058

Procedia Environmental Sciences

2011 3rd International Conference on Environmental Science and Information Application Technology (ESIAT 2011)

Design and Simulation of a CMOS Current Source Cell

Kaiyu Wang[a]a*, Zhenan Tang, Hualong Li, Yun Zhao, Xi Song, Jiandong Su,

[a]*Dalian University of Technology,Gaoxinyuanqu Linggong Road 2, Dalian 116024, PR China*

Abstract

This paper presents a voltage threshold-based self-bias and can be used for integrated CMOS current source structure. When the power supply voltage change from $3V$ to $6.5V$, the current source can output 20 current constant currently and enable control terminal also be added that can effectively control the circuit open or closed. After pre - simulation achieve the desired effect we designed and verified the layout, then extracted the parasitic parameters and used it with the HSPICE software finish the layout simulation. The circuit can be good for the other sub-circuit modules to provide a stable DC bias, so that they can work in a suitable quiescent point.

*Keywords:*CMOS; current source; layout; layout simulation

1 The designed current source circuit and device parameters

1.1 The design principle of this current source

Desired reference current or voltage, are all with the power supply and temperature independent. In many applications of analog integrated circuits, are required to have a module that can provide a steady current and voltage[1].

If turn the voltage on the source device into the current, and try to use the current to provide the initial current through the device, then we can get all kinds of purposes, independent of voltage or current. The technology is called reference, also known as the bootstrap benchmark[2]. Figure 1.1 shows an instance of the use of MOS to achieve this technology[3].

M3 and M4 make the current I1 and I2 equal. I1 flow through M1 generates a voltage Vgs1, and I2 flow through R generated I2R. Because these two voltages are linked, so when the circuit is stable, a balance point will be determined. Figure 1.2 illustrates the method for determining the equilibrium point. In

* Kaiyu Wang. Tel.: +0086-411-84706003-3388;
E-mail address: wkaiyu@dlut.edu.cn.

1878-0296
doi:10.1016/j.proenv.2011.09.168

the curve, I1 and I2 are seen as a function of V. The intersection of these curves is defined as the equilibrium point, with Q to represent. Describe the equilibrium equation is:

$$I_2 R = v_{T1} + \left(\frac{2 I_1 L_1}{K_N^{'} W_1} \right)^{1/2} \tag{1.1}$$

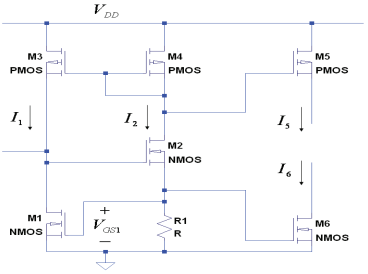

Figure 1.1 Independence and the supply voltage current source design

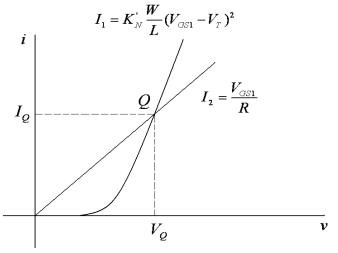

Figure 1.2 determine the balance

Because I_1=I_2=I_Q, we can solve for (λ ignored):

$$I_Q = I_2 = \frac{V_{T1}}{R} + \frac{1}{\beta_1 R^2} + \frac{1}{R} \sqrt{\frac{2 V_{T1}}{\beta_1 R} + \frac{1}{\beta_1^2 R^2}} \tag{1.2}$$

First of all, I_1 and I_2 don't change with the V_{dd}, so the sensitivity of I_Q to V_{dd} approaches to zero. Then through M_5 or M_6 copies M_4 and M_1, we can get the mirror of reference current.

Unfortunately, there are two intersection points in the curve in Figure 1.2: One at Q, and the other one at the origin. This means that the circuit may be stable at any one of the two equilibrium points. In order to avoid the circuit chooses the wrong balance point, we must design a start circuit. Start circuit as shown in Figure 1.3.

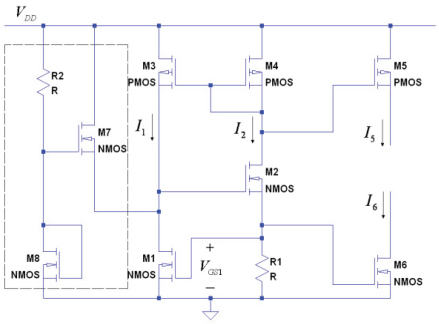

Figure 1.3 the start circuit of current source

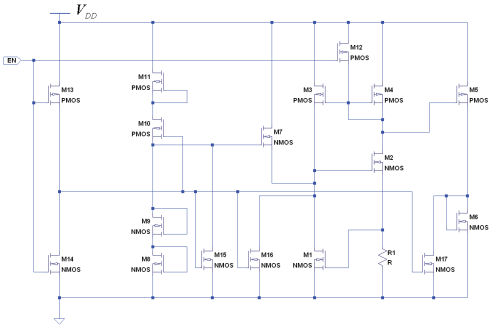

Figure 1.4 the optimized start-up circuit

Figure within the dashed box is the start circuit. If the circuit has chosen the wrong balance point, $I_1$and I_2 are all equal to 0. However, M_7 will provide start-up current for M_1, making the circuit moved to the balance point Q that we want. Along with the circuit's operation point close to the Q, the voltage of M_7's source electrode increases, so the current of M_7 decreases. The most left of the circuit is a MOSFET that connected as an active resistor and a resistor in the form of partial voltage, which provides the gate of M_7 with bias voltage. In analog design of CMOS integrated circuits, we should try to avoid the emergence of resistor, because a poly resistor's area is very large in layout. Sometimes a passive resistor can also be replaced by an active resistor[4].

The optimized circuit is presented in Figure 1.4. In the figure,M_8、M_9、M_{10}、M_{11} four MOSFET are connected in the form of diode separately, and used as active resistor to connect in series to separate voltage, then provide the gate of M_7 with bias voltage and let the launch MOS M_7 empty the launch current into M_1[5], so the circuit transfers from the undesired balance point to the desired balance point Q. On the basis of the start circuit, this paper designed an enable-control circuit, through an enable terminal EN to control the circuit work or not.

1.2 The design parameters of the current source circuit

This design is based on CSMC 0.5um 6S05DPTM process, and using TT (typical typical) process corners for circuit simulation. By looking up h05mixddst02v231.lib model library files, we can get the following parameters (TT process corner model) that may be used for manual calculation in Table 1.1.

Table1.1 parameters

Device type	Minimum channel length(*m*)	Minimum channel width(*m*)	Model class	Thickness of Gate Oxide(*m*)	Threshold voltage(*V*)	Mobility coefficient
NMOS	0.5E-6	0.5E-6	49	1.28E-8+toxn	0.7016+vth0n	4.04257E-2
PMOS	0.55E-6	0.6E-6	49	1.24E-8+toxp	-0.9508+vth0p	0.02195

This design set bias current at 20 *uA*. According to the simulation model, M_1's threshold is about 0.8 *V*, to ensure the M_1 working in saturated zone, need about 200 *mV*, overdrive voltage. So the voltage between M_1's gate and source is about 1*V*.

R_1's resistance is $\mathrm{R1}=\frac{U}{I}\approx\frac{1V}{20\mathrm{m}A}=50K\Omega$,

When calculate the wide long ratio of M1, according to figure 1.2 ,

$$I_1=K_N^{'}\frac{W_1}{L_1}\left(V_{GS1}-V_T\right)^2,\ \frac{W_1}{L_1}=\frac{I_1}{K_N^{'}\left(V_{GS1}-V_T\right)^2}=5$$

We select gate's length L=2 *um*, so W = 10 *um*. The next selection: $\frac{W_{N1}}{L_{N1}}=\frac{10}{2}$, $\frac{W_{P0}}{L_{P0}}=\frac{W_{P1}}{L_{P1}}=\frac{10}{2}$

Other MOS tube as long as realizing the function of digital circuit, so we can choose their wide long ratio uniformly $\frac{W}{L}=\frac{2}{1}$, all of the devices' parameters are as the table 1.2 follows:

Table 1.2 devices' parameters list

Device Number	Device type	Channel length L（*um*）	Channel width W（*um*）	Device Number	Device type	Channel length L（*um*）	Channel width W（*um*）
M1	NMOS	10	2	M10	PMOS	2	10
M2	NMOS	10	2	M11	PMOS	2	10
M3	PMOS	10	2	M12	PMOS	2	1
M4	PMOS	10	2	M13	PMOS	2	1
M5	PMOS	10	2	M14	NMOS	2	1
M6	NMOS	10	2	M15	NMOS	2	1
M7	NMOS	2	1	M16	NMOS	2	1
M8	NMOS	2	1	M17	NMOS	2	1
M9	NMOS	2	1	R1	Resister	$50K\Omega$	

2 The spice simulation of current source circuit

This paper focuses on the current source's output current value, stability, temperature coefficient and enable pin's control function EN four parameters to simulate, the simulation tool is HSPICE software.

2.1 Current source output current simulation

In this design, during simulation, the debugging of resistance continuously until set it at 54.5*K* , the current source output current reached 20 *uA* that we stated .therefore, we modify resistance value to 54.5*K*. Simulation waveform is shown in Figure 2.1.

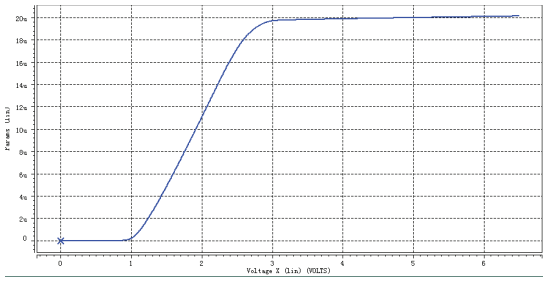

Figure 2.1 the current source output current simulation wavform

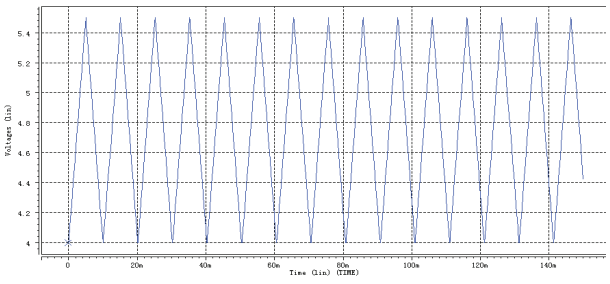

Figure 2.2 voltage source fluctuation simulation waveform

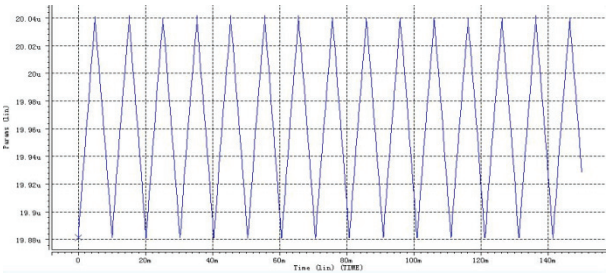

Figure 2.3 the current source output value stability simulation waveform

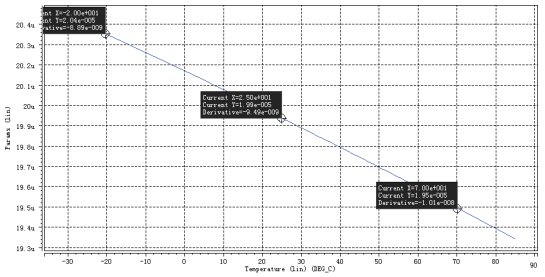

Figure 2.4 the simulation waveform and calculation of voltage source temperature coefficient

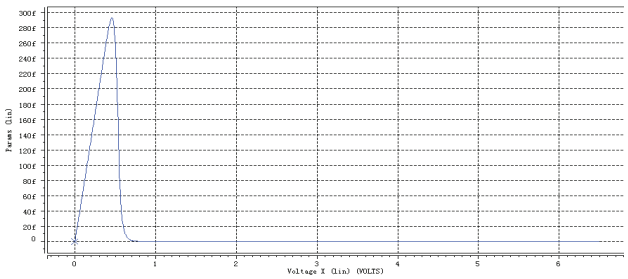

Figure 2.5 current source enable pin EN's simulation waveform

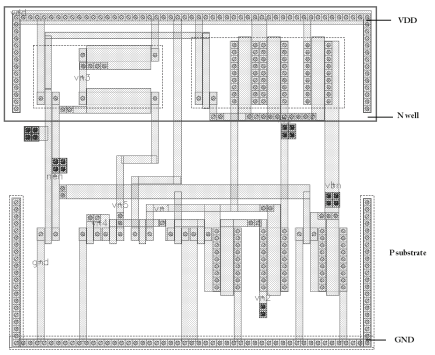

Figure 3.1 the layout design of current

We can see from the graph, this circuit realized our pre-set functions: When the power supply voltage, current source than 3 *V* can output constant current basic stability, current value in the 20 *uA* .

2.2 Current source stability simulation

In order to simulate the influence of power supply fluctuation on current source output current value, we can use triangle wave to simulate power fluctuation .We set the power supply voltage value at 4.75 *V*, and the amplitude of fluctuation interference is 0.75 *V*, waveform is in Figure 2.2.

From the current source waveform in Figure 2.3 we can see, when the power supply voltage fluctuation range from 4 *V* to 5.5 *V*, amplitude of fluctation is 15.79%, the current source output current value fluctuate range for19.88 *uA* ~ 20.04 *uA* , fluctuant range is very small, the change is only 0.16 *uA* , fluctuant amplitude is only 0.4%.

2.3 Current source temperature coefficient simulation

Take dc scanning on temperature, scanning range is 30 ℃ ~ 85 ℃, step length is 1 ℃, simulation waveform as shown in Figure 2.4:

According to the graph of the coordinates, we can compute the draw:

$$\text{Current source temperature coefficient} = \frac{20.4\mu A - 19.5\mu A}{(70°C + 20°C) \times 9.9\mu A} = 5.03 \times 10^{-4} = 503ppm$$

2.4 Current source enable pin EN's function simulation

The current source has enable pin EN that can control the whole circuit work or not. When EN connects with the power, circuit regular work; When EN connects with low potential, the entire circuit shutoff. The waveform that when circuit normal working we have seen several in the above simulated waveform, next let's see when EN connects with low potential, circuit's work situation.

We set circuit connection is as follows: EN grounding, input voltage V_{dd} scans from 0 to 6.5 *V*, the circuit waveform is shown in Figure 2.5. From the simulation waveform, we can see: when V_{dd} scans from 0 to 6.5 *V*, the entire circuit only output a small current at the *fA* level, 1f = 10^{-15} , the output current is very small, namely the whole circuit is in closed state, EN control terminals effective control the whole circuit.

3 Current source layout design and validation

This paper adopts CSMC 0.5μm CMOS DPTM process rules for the current source circuit layout design and validation[6-7], the layout is shown in Figure 3.1.

4 Current source layout simulations

Using the parasitic parameters extracted from the layout of current source to take layout simulation, mainly includes the output current value[8] , the current source stability and temperature coefficient three basic parameters, comparing with the layout simulation results, each simulation waveform contrast is from Figure 4.1 to Figure 4.2.

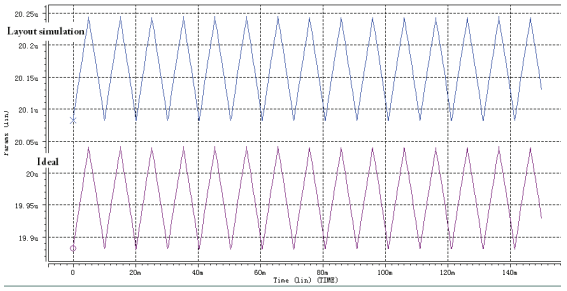

Figure 4.1 current value waveform
comparison between former simulation and layout simulation

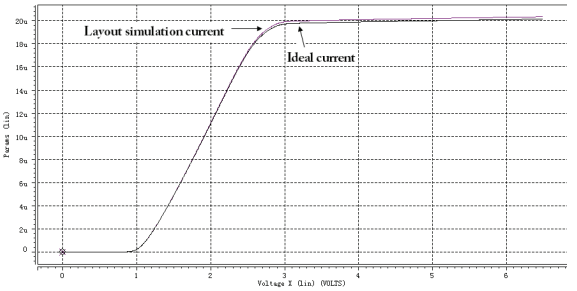

Figure 4.2 current source stability waveform
comparison between former simulation and layout simulation

5 Current source layout simulation data analysis

5.1 Current source output current layout simulation data analysis

It can be seen from the figure 4.1, among pre-simulation and layout simulation data, the current source output current no apparent change, two curves is almost coincident, both two current value can stabilize at 20 *uA*, therefore the parasitic parameters of layout influences current source's output current value very little.

5.2 Current source layout simulation data analysis of stability

It can be seen from figure 4.2,when power supply voltage fluctuates from 4 *V* to 5.5 *V* and the fluctuation range is 15.79%,the current source output current value fluctuates from 20.08 *uA* to 20.24 *uA* ,the change is 0.16 *uA*,and the fluctuation range is 0.4% .And in the pre-simulation data shown in figure 2.2, the current source output current value fluctuates from 20.08 *uA* to 20.24 *uA* ,the change is 0.16 *uA*,and the fluctuation range also is 0.4% . Therefore, we can conclude that the effect of layout parasitic parameters on the stability of the current source is very small.

5.3 Current source layout simulation data analysis of temperature coefficient

According to layout simulation data, we can calculate the simulation temperature coefficient of current source:

$$\text{Current source temperature coefficient} = \frac{22.4\,\mu A - 17.7\mu A}{(70°C + 20°C) \times 20.1\mu A} = 2.60 \times 10^{-3} = 2598ppm$$

While in 2.4 section, we have calculated the pre-simulation temperature coefficient of current source is 503*ppm*. From the two data contrast, we can see that the current source temperature coefficient changes largely in layout simulation. Therefore, we can draw the conclusion that the parasitic parameters of layout have a big effect on current source temperature drift.

Conclusion:

According to the pre-simulation waveform of current source designed by this paper, when the power supply voltage change from 0 to 6.5 *V* and the power voltage bigger than 3 *V*,the current source can output 20 *uA* current constantly; when power supply voltage fluctuates from 4 *V* to 5.5 *V* and the fluctuation range is 15.79%, the current source output current value fluctuates from20.8 *uA* to20.24 *uA* , the fluctuation range is only 0.4% ; the pre-simulation temperature coefficient of current source is 503 *ppm*; the enable pin can effectively control the circuit open or closed. After extract the parasitic parameters of layout take layout simulation, and do a detailed comparison between pre-simulation data and layout simulation data, the results showed that besides the temperature coefficient change a lot, the three other indicators of layout simulation are basically same with pre-simulation data, the parasitic parameters of layout influence the function of circuit little, and the layout this paper designed is perfect. If you want to reduce the temperature coefficient of current source simulation, need to adjust the layout, optimize the layout distribution and cuts down the resistance and capacitance that mismatched and parasitic.

This paper adopts the standard CMOS technology, therefore, the design of current source unit can be used as a module appeared in a complete chip design to provide static dc bias for other circuit module, and make them work in the appropriate dc operating point to ensure the whole chip can work normally.

References

[1] Ying Liu. Analog Electronics Technique [M].Beijing: Beijing Jiaotong University Press,2008.

[2] Jianhui Wu.Analysis and Design of CMOS Analog Integrated Circuits [M].Beijing:Publishing House of Electronics Industry,2004.

[3] Phillip E Allen, Douglas R Holberg. CMOS Analog Circuit Design, 2nd Edition. Oxford:Oxford University Press, 2002.

[4] Alan Hastings .The Art of Analog Layout Second Edition. Prentice Hall Press,2005.

[5] Razavi B.Design of Analog CMOS Integrated Circuits[M]Boston,MA:McGraw-Hill Press,2001.

[6] Qi Ma,Xiaohua Luo,Xiaolang Yan. An Overview of CMOS Cell Layout Generation Algorithms[J]. Microelectronics , 2001,31(3):204-205

[7] Wei Tang,Zhenghui Lin,Yinan Zhu,etc. A New Method for Layout Verification of Integrated Circuits [J].Microelectronics, 2003, 33(2):113-117.

[8] Jun Xiao,Zhenghui Lin. New Hierarchical Approach for Layout-Circuit Extraction[J]. Journal of Shanghai Jiaotong University, 1999, 33(5):197-199.