Design Considerations For Common-Mode Feedback Circuits In Fully-Differential Operational Transconductance Amplifiers with Tuning

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ABSTRACT: Power consumption, chip area, feedback loop gain, parasitic capacitance and nonlinearity of three popular common-mode feedback (CMF) circuits used in operational amplifiers are analyzed and compared in this paper. One of them is chosen as a candidate for CMF in fully-differential operational transconductance amplifiers (OTAs). Three improved versions of this circuit are proposed that can be used in an OTA without leading to DC offset caused by the always unavoidable tuning. Simulation results show that the improved circuits reduce the DC offset from 0.6 V to nearly zero for the whole tuning range.

I. Introduction

In recent years, continuous-time fully-balanced OTA-C filters have been developed with fully differential OTAs. Because of the balanced nature of these circuits, power supply rejection is improved, output dynamic range is increased by a factor 2 and harmonic distortion is reduced by cancellation of all even-order harmonics [1]. A problem with fully balanced circuits is that no feedback loop exists for the common-mode (CM) voltage; CM output, therefore, is undefined and the transistors in the output stage may drift out of their linear range. To avoid this problem, an additional feedback loop, called common-mode feedback (CMF) circuit, should be employed [2].

The CMF circuits may increase both power consumption and chip area. Also, because they form additional loads for the differential-mode (DM) signal, the frequency response of the OTA will be degenerated. To reduce these effects of CMF circuits, the simplest circuitry with small-size transistors should be used. Another potential problem is caused by the nonlinearity of a CMF circuit. After CMF is added to an amplifier, its output voltage is constrained by the currents in the CMF circuit. Due to the nonlinearity of the I-V characteristic of MOSFETs, the output voltages may become assymmetric [1]. So, choosing a CMF circuit with minimum nonlinearity distortion is also an important consideration for the design. Furthermore, when a CMF circuit is used in an OTA, a further serious problem may appear: usually, both CMF and tuning, which is unavoidable in an OTA for post-fabrication adjustment [3], implement their functions by changing DC bias currents. This may result in a large DC offset or unnecessary tuning, and may even cause the filtering system to be unstable. Consequently, to make the operations of CMF and tuning independent of each other is a very important aspect for fully differential OTA design.

In this paper, first three popular CMF circuits used in operational amplifiers (op-amps) will be analyzed and compared in terms of power consumption, chip area, parasitic capacitance and nonlinearity, and one of them will be chosen as a candidate for an OTA. Then, improved versions of this circuit will be proposed so that the interdependence between tuning and CMF is minimum.

II. General Considerations For CMF Circuits

In a fully differential amplifier, CMF senses the CM output voltage $V_{o,CM}$ but, ideally, not the DM output voltage $V_{o,DM}$. The output signal of the CMF circuit is fed back to the amplifier to adjust the DC current in the output stage so that $V_{o,CM}$ can be maintained at a preset DC level, normally at zero.

The three most common CMF circuits are shown in Fig. 1, among which Circuit 1 is a typical differential pair. Because the output voltage V_s is taken from the common sources of transistors M_1 and M_2, V_s ideally does not change with $V_{o,DM}$ of the amplifier, but only with $V_{o,CM}$. In Circuit 2, where the voltage V_{cm} is the preset DC output level, changes of the currents I_{d1} and I_{d4} caused by $V_{o,DM}$ are balanced by corresponding changes of the currents I_{d2} and I_{d3}. For $V_{o,CM}$, this balance is broken, and the voltage V_s changes until a new balance is reached [4]. In Circuit 3, transistors M_4 and M_5 are part of the output stage of the amplifier, and transistor M_6 is part of the bias circuit. Transistors M_1 and M_2 operate in the triode region, and M_3 is used to set a reference voltage V_{cm}. It can be seen that, in Circuit 3, the sum $I_{d1}+I_{d2}$ is constant with changing $V_{o,DM}$, but varies with $V_{o,CM}$.

Understanding the basic principle of CMF circuits, a comparison can be made. For power consumption, it can be seen from Fig. 1 that Circuit 1 consumes little power because the current $2I_{dd}$ can be very small. Circuit 2 consumes more power than Circuit 1 since two differential pairs are used. For Circuit 3, the additional power consumption is almost zero, because M_1 and M_2 are inserted to the output stage of the amplifier and M_3 is inserted to the bias circuitry.

As to chip real estate, Circuit 1 occupies a very small area, because it consists of only three small-size transistors. Circuit 2 contains eight transistors, so that, compared to Circuit 1, the area increases nearly three times. The chip area for Circuit 3 is large, because large currents flow through the output stage and bias circuit and the transistor sizes for M_1, M_2, and M_3 must be large.

In Circuits 1 and 2, as mentioned above, the transistor sizes of input transistors M_1 and M_2, and M_1 and M_4, respectively, can be very small, so that the additional parasitic capacitive load caused by the CMF circuits is very small. But in Circuit 3, large transistor sizes of M_1 and M_2 are used, so that the additional parasitics are large also.

The CMF loop gain is required to be as large as possible because it determines the sensitivity of the circuit to the CM signal. For Circuit 1, the output signal V_s of the CMF circuit is used to control the gate of the transistors which act as the current sources in the output stage of the amplifier (see Fig. 2) and which must operate in saturation. Therefore, the current I_s in the output stage changes with V_s according to the square-law characteristics of a MOSFET. This situation is the same for Circuit 2, because the output of Circuit 2 is also connected to the gate of current source transistors [4]. Because transistors M_1 and M_2 in Circuit 3 operate in the triode region, the change of I_s caused by the change of CM output voltage is less than that for Circuit 1 and its loop gain is smaller.

Next, distortion of the output voltage caused by the nonlinearity of the CMF circuit will be analyzed. Suppose that the preset DC voltages at the output nodes are zero. Then, for Circuit 1, when $V_{o+}=V_{o-}=0$

$$I_{d1}=I_{d2}=I_{dd}=k(-V_{s0}-V_T)^2 \qquad (1)$$

where k is the transconductance parameter, V_{s0} is the DC value of V_s and V_T is the threshold voltage.

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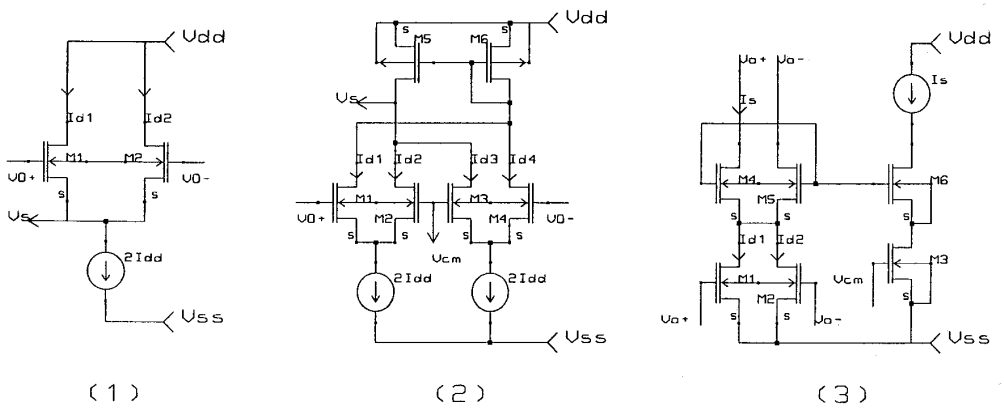


(1) (2) (3)

Fig. 1. The three most common CMF circuits used in op-amps.

Suppose that for a "pure" DM output voltage ($V_{o+} = -V_{o-} \neq 0$) V_s has a small change ΔV_s; then V_{gs1} and V_{gs2} are

$$V_{gs1} = V_{o+} - (V_{s0} + \Delta V_s) \quad \text{and} \quad V_{gs2} = -V_{o+} - (V_{s0} + \Delta V_s) \tag{2}$$

According to (2), I_{d1} and I_{d2} become

$$I_{d1} = k[(V_{o+} - \Delta V_s)^2 + (-V_{s0} - V_T)^2 + 2(V_{o+} - \Delta V_s)(-V_{s0} - V_T)] \tag{3a}$$

and

$$I_{d2} = k[(-V_{o+} - \Delta V_s)^2 + (-V_{s0} - V_T)^2 + 2(-V_{o+} - \Delta V_s)(-V_{s0} - V_T)] \tag{3b}$$

Considering that $I_{d1} + I_{d2} = 2I_{dd}$ from (1), ΔV_s is solved from (3)

$$\Delta V_s = (|V_{s0}| - V_T) - \sqrt{(|V_{s0}| - V_T)^2 - (V_{o+})^2} \tag{4}$$

It is seen from (4) that, for Circuit 1, $\Delta V_s = 0$ when $V_{o+} = 0$. But, when a "pure" DM output voltage $V_{o+} = -V_{o-} \neq 0$ is present, $\Delta V_s \neq 0$. When this change of V_s is fed back to the amplifier to vary the output voltage, the latter becomes assymmetric: An easy way to consider the nonlinear distortion for a DM signal is to determine a relationship between V_{o+} and V_{o-} when $\Delta V_s = 0$. Then, the ratio of the obtained V_{o+} and V_{o-} will be a measure of the distortion.

If $V_{o+} \neq 0$ and $V_{o-} \neq 0$, and $V_s = V_{s0}$ is considered constant, V_{gs1} and V_{gs2} are

$$V_{gs1} = V_{o+} - V_{s0} \quad \text{and} \quad V_{gs2} = V_{o-} - V_{s0} \tag{5}$$

to yield

$$I_{d1} = kV_{o+}^2 + 2kV_{o+}(-V_{s0} - V_T) + k(-V_{s0} - V_T)^2 \tag{6a}$$

and

$$I_{d2} = kV_{o-}^2 + 2kV_{o-}(-V_{s0} - V_T) + k(-V_{s0} - V_T)^2 \tag{6b}$$

From (6) with (1), it can be shown that

$$\frac{V_{o+}}{-V_{o-}} = \frac{1 - \dfrac{-V_{o-}}{2(-V_{s0} - V_T)}}{1 + \dfrac{V_{o+}}{2(-V_{s0} - V_T)}} \tag{7}$$

Thus, $V_{o+} \neq -V_{o-}$ which means that the CMF circuit forces the output voltages to become assymmetric, with the assymmetry being dependent on the ratio $r = |V_{o+} / [2(-V_{s0} - V_T)]|$. If $r \ll 1$, $V_{o+} \simeq -V_{o-}$, a situation achievable by choosing a large V_{s0}. It can also be seen from (4) that $\Delta V_s \simeq 0$ if $r \ll 1$.

Applying the same analysis to Circuit 2 shows that $V_{o+} = -V_{o-}$, i.e., there is no distortion. For Circuit 3, distortion appears also. It was pointed out in [1] that SPICE simulation results indicate that Circuit 2 has the best linearity and Circuit 3 has the worst.

The above analysis is summarized in Table 1, from which it can be seen that the most important problem of Circuit 2 is the large chip area. Because an OTA-C filter may require many OTAs, the OTA circuit should be designed to be as simple as possible. For Circuit 3, the main drawback is the large parasitics which may degrade the high-frequency response. The only disadvantage of Circuit 1 is potential nonlinearity which, fortunately, is less critical in OTA-C filters, because (i) the output voltage swing of OTAs in an OTA-C filter is generally not large and (ii) $|V_{s0}|$ can be designed large by using a large-size transistor for the current source $2I_{dd}$ and small-size transistors for M_1 and M_2 in Circuit 1. Circuit 1 is, therefore, recognized as the best candidate for CMF circuitry in OTAs and will be modified so that it can be used in OTAs.

Table 1. Summary of the comparison of three typical CMF circuits.

	Add'l Power Consumption	Chip Area	Linearity	Sensitivity to CM signal	Parasitic Capacitance
Fig. 1	Small	Small	Poor*	Large	Small
Fig. 2	Large	Large	Good	Large	Small
Fig. 3	Zero	Large	Poor**	Small	Large

* If $|V_{s0}|$ is chosen to be very large and output swing is small, the linearity is acceptable.

** See the reference [1].

III. Improved CMF Circuits For OTA

A typical simple fully-differential OTA with the above-chosen CMF circuit is shown in Fig. 2, its DC output voltage V_{o+} can be expressed as

$$V_{o+} = \left(\frac{2L}{kW_1} I_1\right)^{1/2} + \left(\frac{2L}{kW_4} I_s\right)^{1/2} + V_{T1} + V_{T4} - V_{ss} \tag{8}$$

where W_i and L are the width and length of the transistors M_i.

In (8), V_{o+} is a monotonic function of bias current I_s, so that V_{o+} is no longer constant because, in contrast to op-amps, in an OTA I_s must be changed for post-fabrication tuning. This leads to DC offset during tuning. In order to avoid or minimize this problem, the CMF circuit in Fig. 2 must be modified.

Equation (8) points to three possibilities to improve the CMF circuit in Fig. 2. *First,* V_{o+} is a monotonic function of I_s because I_1 remains constant when tuning. If I_1 can be made to change as a function of I_s, but in direction opposite to the second term, the changes of the second term may be canceled and V_{o+} may become near constant. *Second,* because during tuning, g_m changes with the DC currents in the *input* transistors, it is not required to change the currents, say I_s, in the *output* stage. Thus, if a new tuning method can be designed to change g_m without changing I_s, the second term of (8) and V_{o+} becomes constant. *Third,* if an additional adjustable bypass current from the output node to ground is introduced, I_s will not be controlled by V_s (see Fig. 1). Then, I_s is removed from (8)

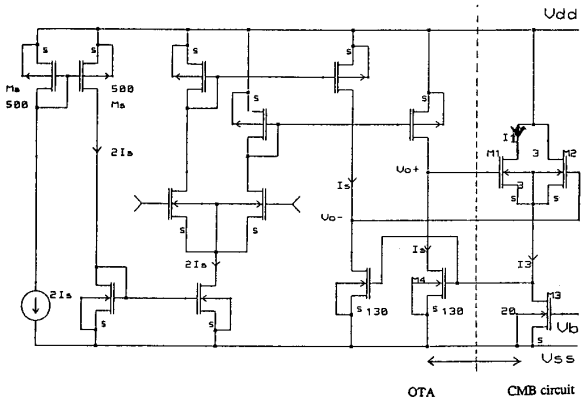


Fig. 2. Circuit diagram for a simple fully differential OTA with a typical common-mode feedback circuit.

and V_{o+} becomes constant. Based on these considerations, three improved circuits are proposed in Fig. 3.

Fig. 3a shows the improved CMF circuit for the first choice mentioned above; it adds only one transistor, M5, to the CMF circuit in Fig. 2. Because the gates of M5 and Ms are connected, the current I_5 changes proportionally to $2I_s$, and I_1 becomes

$$I_1 = \frac{(I_3 - I_5)}{2} = \frac{I_3}{2} - \frac{I_s W_5}{W_s} \tag{9}$$

In (9), I_1 is a decreasing function of I_s as required, which results in (8) becoming

$$V_{o+} = [\frac{L}{kW_1}(I_3 - \frac{2W_5 I_s}{W_s})]^{1/2} + (\frac{2L}{kW_4} I_s)^{1/2} + V_{T1} + V_{T4} + V_{ss} \tag{10}$$

It is apparent from (10) that, for a proper choice of W_5 or, equivalently, W_3, i.e. I_3, the increase of the second term may be balanced by the decrease of the first term when I_s increases. Due to the square-root in both the first and the second terms, a complete cancellation is impossible, but, analysis shows that one optimum solution exists: Setting the derivative of V_{o+} in (10) with respect to I_s to zero shows that V_{o+} has only one extreme value at

$$I_{s,m} = \frac{W_1 W_s^2 I_3}{2W_4 W_5^2 + 2W_1 W_5 W_s} \tag{11}$$

This means that V_{o+} is either a convex or a concave function of I_s. Further, in (10) V_{o+} is monotonic in I_3. For a function with these two properties, the range of variation is minimum if $V_{o+}(I_{s,min}) = V_{o+}(I_{s,max})$. From this condition, the optimum I_3 can be solved to be

$$I_3 = [\frac{W_5}{W_s}(\frac{W_4}{2W_1})^{1/2}(\sqrt{I_{s,max}} + \sqrt{I_{s,min}}) + (\frac{W_1}{2W_4})^{1/2}(\sqrt{I_{s,max}} - \sqrt{I_{s,min}})]^2 + \frac{2W_5 I_{s,min}}{W_s} \tag{12}$$

After I_3 is obtained, it is easy to calculate the required width W_3 for a constant gate voltage V_b.

This circuit and the circuit in Fig. 2 were simulated by SPICE to verify the above conclusion. The transistor widths [μm] are shown in Fig. 2 and Fig. 3a and the transistor lengths are 10 μm. Note that, in Fig. 2, W_1 = 3 μm and W_3 = 20 μm, which shows $W_3 \neq 2W_1$. The reason for this choice is to obtain large V_{gs1} and V_{gs2} to decrease nonlinear distortion as discussed in the last section. Also, W_3 = 28 μm is chosen according to I_3 = 53.9 μA which is calculated by using (12) with $I_{s,min}$ = 100 μA and $I_{s,max}$ = 250 μA. With these choices, the simulation results in Fig. 4 show that, V_{o+} changes from -30 mV to 600 mV (curve <1>) with I_s changing for the CMF circuit in Fig. 2, but changes only from -30 mV to only 50 mV (curve <2>) for the circuit in Fig. 3a. DC offset is reduced by nearly a factor 10, which is generally acceptable in the design of fully-differential OTAs.

The maximum value of V_{o+} at $I_{s,m}$ in Curve <2> cannot be reduced. It can be seen that, after $I_{s,m}$ is substituted in (10), V_{o+} is only function of W_i because I_3 has been set for the condition $V_{o+}(I_{s,min}) = V_{o+}(I_{s,max})$. Then, if W_i is changed, not only Curve <2> changes but also Curve <1>. This means the maximum values of V_{o+} in both curves change proportionally, resulting in the ratio of the two $V_{o+,max}$ remaining almost constant.

Observe from curve <2> in Fig. 4 that $V_{o+}(I_{s,min}) \approx V_{o+}(I_{s,max})$. This means the current I_3 as calculated by (12) is close to I_3 required in the simulations. Note, though, that (12) should be modified by including the channel-length modulation parameter λ if small-length transistors are used.

The other considerations discussed in the last section are still satisfied for the improved circuit in Fig. 3a; neither power consumption nor chip area increase significantly because I_5 in Fig. 3a can be chosen as small as I_1. Also, because the output signal does not flow through M_5, the output parasitics of OTA and linearity are not changed.

For the second choice, the corresponding proposed circuit is shown in Fig. 3b where the actual CMF circuit has not changed; there are only two bypass transistors M_6 and M_7 placed in parallel to the input transistors M_{d1} and M_{d2}. Now, as V_a changes, the current I_6 changes, which, in turn, results in

$$I_{d1} = I_s - I_6 \tag{13}$$

Since the transconductance g_m is proportional to I_{d1}, not I_s, then, g_m can be tuned without changing I_s, which results by (8) in constant V_{o+}. Because this is obviously true, a proof by SPICE simulation is not necessary.

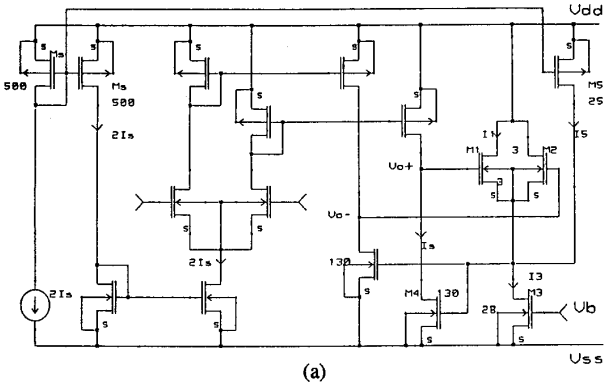
The advantage of this choice is that tuning and the CMF loop are totally independent of each other, so that no DC offset is generated. The disadvantage of the circuit is that the sizes of transistors M6 and M7, usually, should be chosen to be compatible to that of Md1 to maintain a large tuning range; thus power consumption and chip area will increase. Also, the additional transistors increase parasitic capacitances at the nodes A and B in Fig. 3b, which results in a reduction of bandwidth.

For the last choice mentioned above, the CMF circuit in Fig. 3c, compared to the CMF circuit in Fig. 2, contains two more transistors M_8 and M_9 which are connected in parallel to transistors M_4 and M_{10} in Fig. 3c. The output voltage V_s of the CMF circuit is now used to control the gates of M_8 and M_9, instead of M_4 and M_{10}. Then, the output voltage is stabilized not by changing the bias current I_s, but by adjusting the current I_9, which results in V_{o+} in (8) becoming

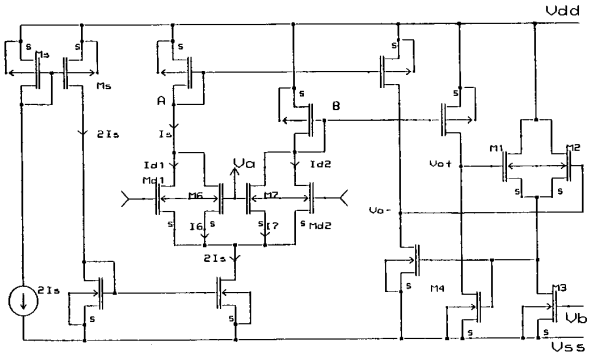
$$V_{o+} = (\frac{2L}{kW_1} I_1)^{1/2} + (\frac{2L}{kW_9} I_9)^{1/2} + V_{T1} + V_{T9} - V_{ss} \tag{14}$$

so that V_{o+} is independent of I_s. It should be pointed out, however, that I_9 is not totally independent of I_s, because $I_s + I_9 = I_{11}$. Obviously, this dependence is determined by proper choice of the ratio of W_4/W_9: if it is very large, I_9 is almost independent of I_s, the CMF loop is nearly independent of I_s and only a very small DC offset is generated.

If small transistors are used for M_8 and M_9, all considerations discussed in the last section are satisfied except the reduced feedback loop gain. This implies that this circuit cannot used in OTAs with large CM output swing. But, as a tradeoff, large transistors used will result in increased power consumption, large chip area, big parasitics, and DC offset. Fortunately, in the filtering application, the CM output swing is generally not large [5] and this is particularly true for filters operating under low power supplies such as ±2.5 V. So, the circuit in Fig. 3c can be used with a small W_8 and W_9.



(a)



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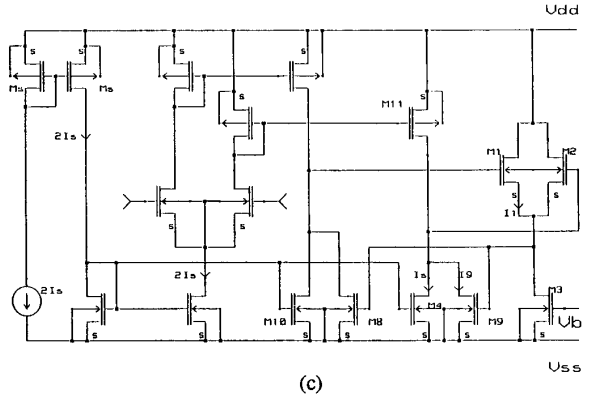

(c)

Fig. 3. Circuit diagrams for the improved CMF circuits suitable for OTAs with tuning; (a) the DC offset is diminished by changing I_1, and (2) the DC offset is avoided by making tuning independent of I_s. (3) DC offset is reudced by making CMF independent of I_s or tuning.

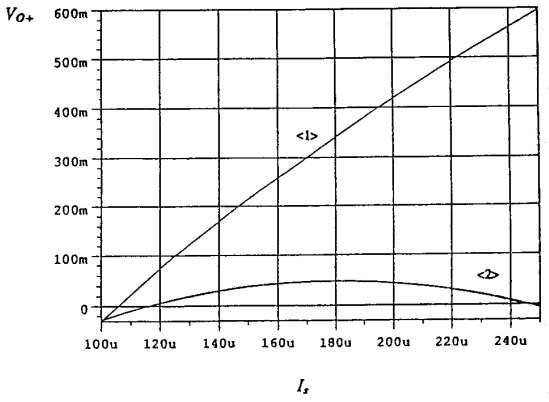

Fig. 4. SPICE simulation results for common-mode output voltage, V_{o+}, of the OTA with the CMF circuits <1> in Fig. 2 and <2> in Fig. 3a.

IV. Conclusions

Design considerations for CMF circuits have been discussed, and three improvements suitable for OTAs have been proposed. The simulation results of Circuit 1 show that DC offset caused by tuning has been effectively reduced. The other two circuits have also been used in the OTAs design; one in a GaAs OTA and another in a CMOS OTA with low-power supplies. They worked well. Due to the space limits, the results are not shown in this paper.

V. Acknowledgements

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