CMOS090 technology
21A POLYWELL CAPS models
DK_MIKRON

SPICE Models Benchmarks

June 2010

TR&D / STD / T2D /

Modeling / CM2A

General information on 21A POLYWELL CAPS models

Supply voltage (Vdd) is 1.2 V.

Validity domain is defined as follows:

Vgs, Vds and Vbs vary from 0 V to 1.32 V (i.e. Vdd + 10%).

Conditions of simulation

Simulations were done with Bench v3.6.3sram using Eldo simulator v6.7_1.2.

If not explicitly mentioned elsewhere, temperature is set to 25 ° C and Vbs to 0 V.

Output parameters definition

In what follows, M, W and L (all default to 1) designate the number of devices in parallel (i.e. multiplication factor), the total drawn gate width and the drawn gate length, respectively.

- **Cgg_inv:** Total gate capacitance at Vgs = 1.2 V, Vds = 0 V, f = 100k Hz.
- **Cgd_0V:** Gate-to-Drain capacitance at Vgs = 0 V, Vds = 0 V, f = 100k Hz.

CPONW

Electrical characteristics per geometry

cponw carea=1600 cperi=80

	CPOLYN_CMIN	CPOLYN_TYP	CPOLYN_CMAX
Cgg_inv [pF]	18.752	19.578	20.408
Cgd_0V [pF]	10.614	13.871	16.333

cponw carea=40 cperi=2

	CPOLYN_CMIN	CPOLYN_TYP	CPOLYN_CMAX
Cgg_inv [fF]	466.29	494.41	522.97
Cgd_0V [fF]	258.22	345.47	414.7

CPOPW

Electrical characteristics per geometry

cpopw carea=1600 cperi=80

	CPOLYN_CMIN	CPOLYN_TYP	CPOLYN_CMAX
Cgg_inv [pF]	19.606	20.418	21.283
Cgd_0V [pF]	10.205	12.876	15.465

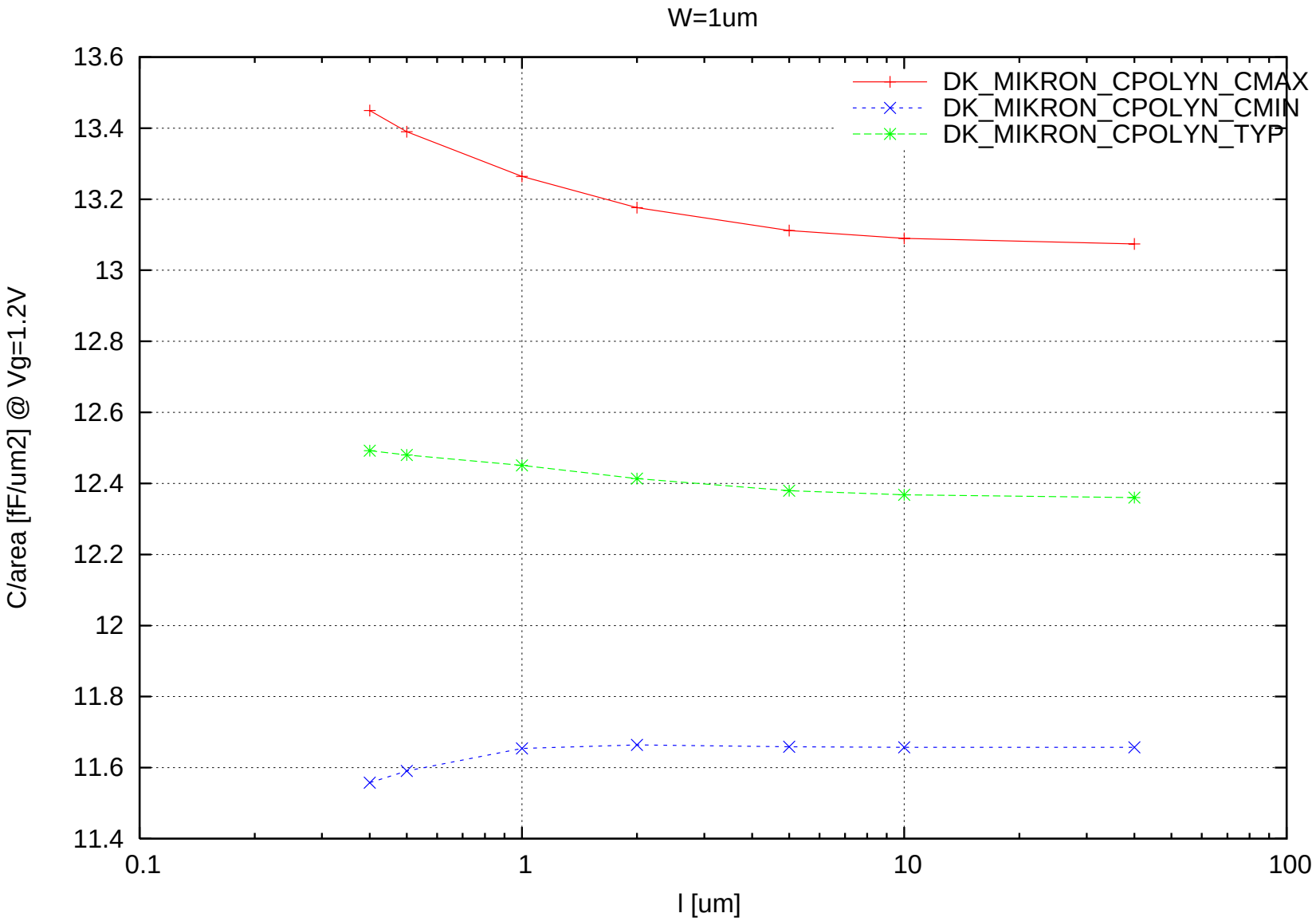
cpopw carea=40 cperi=2

	CPOLYN_CMIN	CPOLYN_TYP	CPOLYN_CMAX
Cgg_inv [fF]	502.33	530.4	560.51
Cgd_0V [fF]	276.47	347.1	416.92

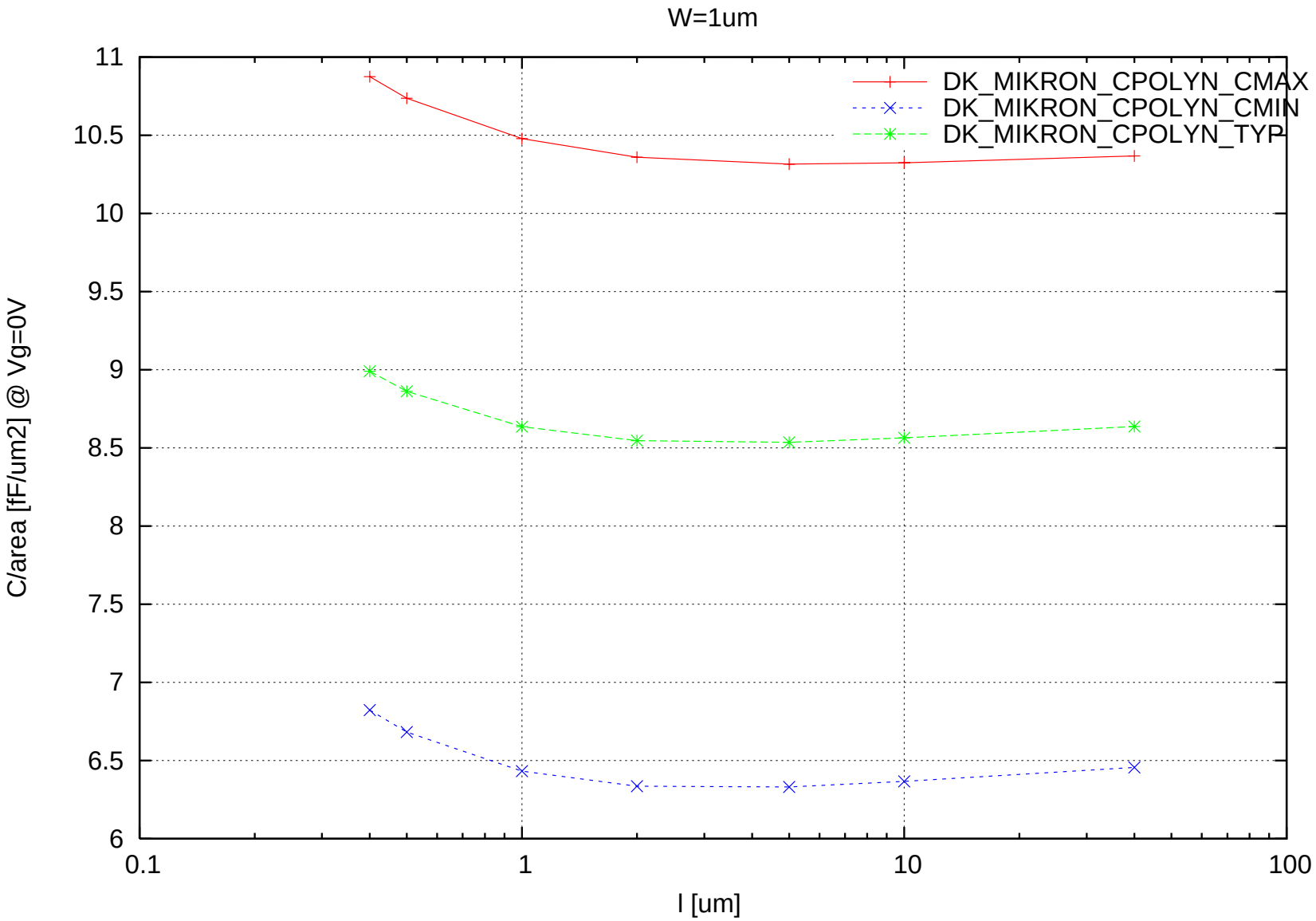
CPONW

Electrical characteristics scaling

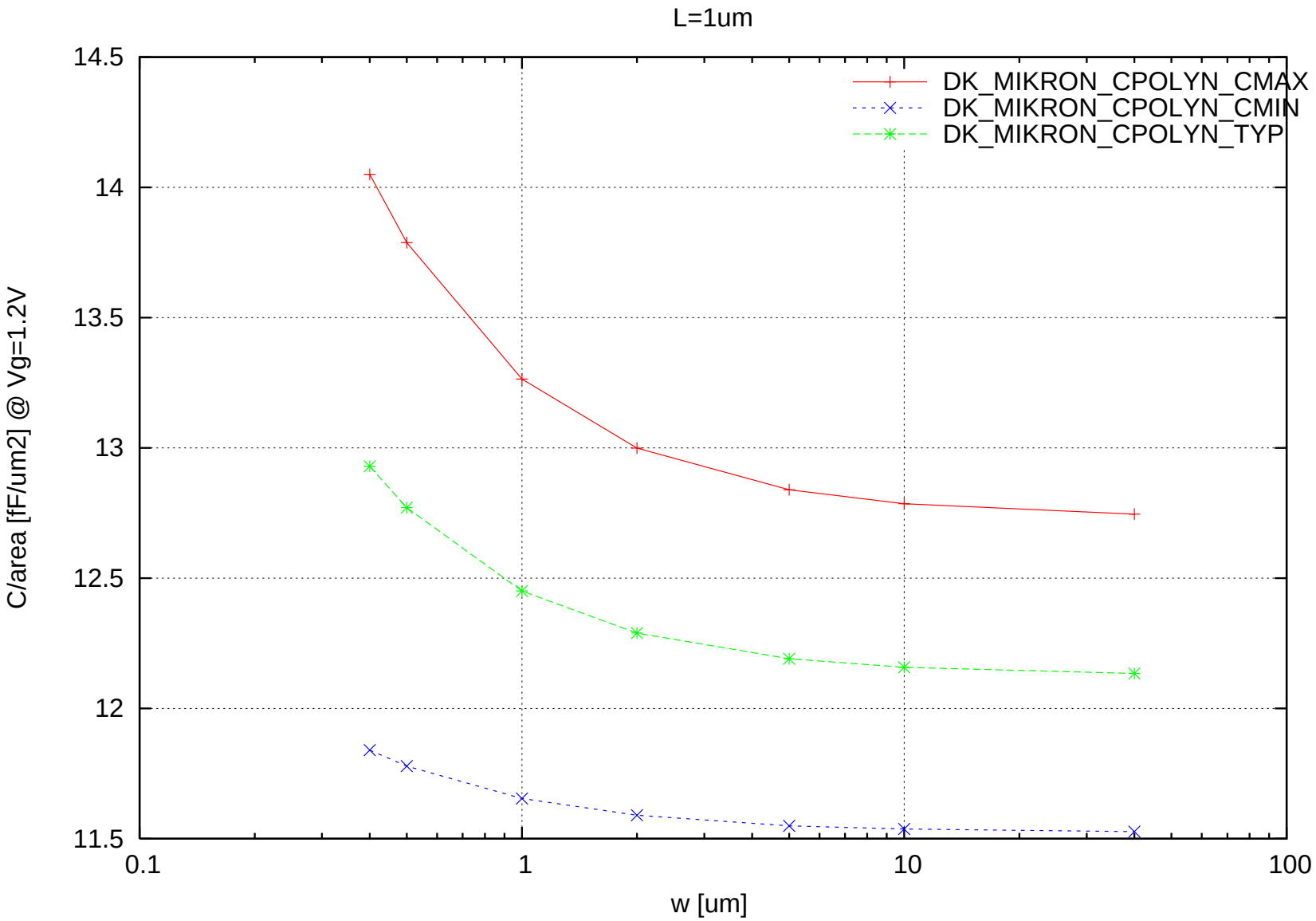
cponw C/area [fF/um2] @ Vg=1.2V vs. l [um] , W=1um



cponw C/area [fF/um2] @ Vg=0V vs. l [um] , W=1um



cponw C/area [fF/um2] @ Vg=1.2V vs. w [um] , L=1um



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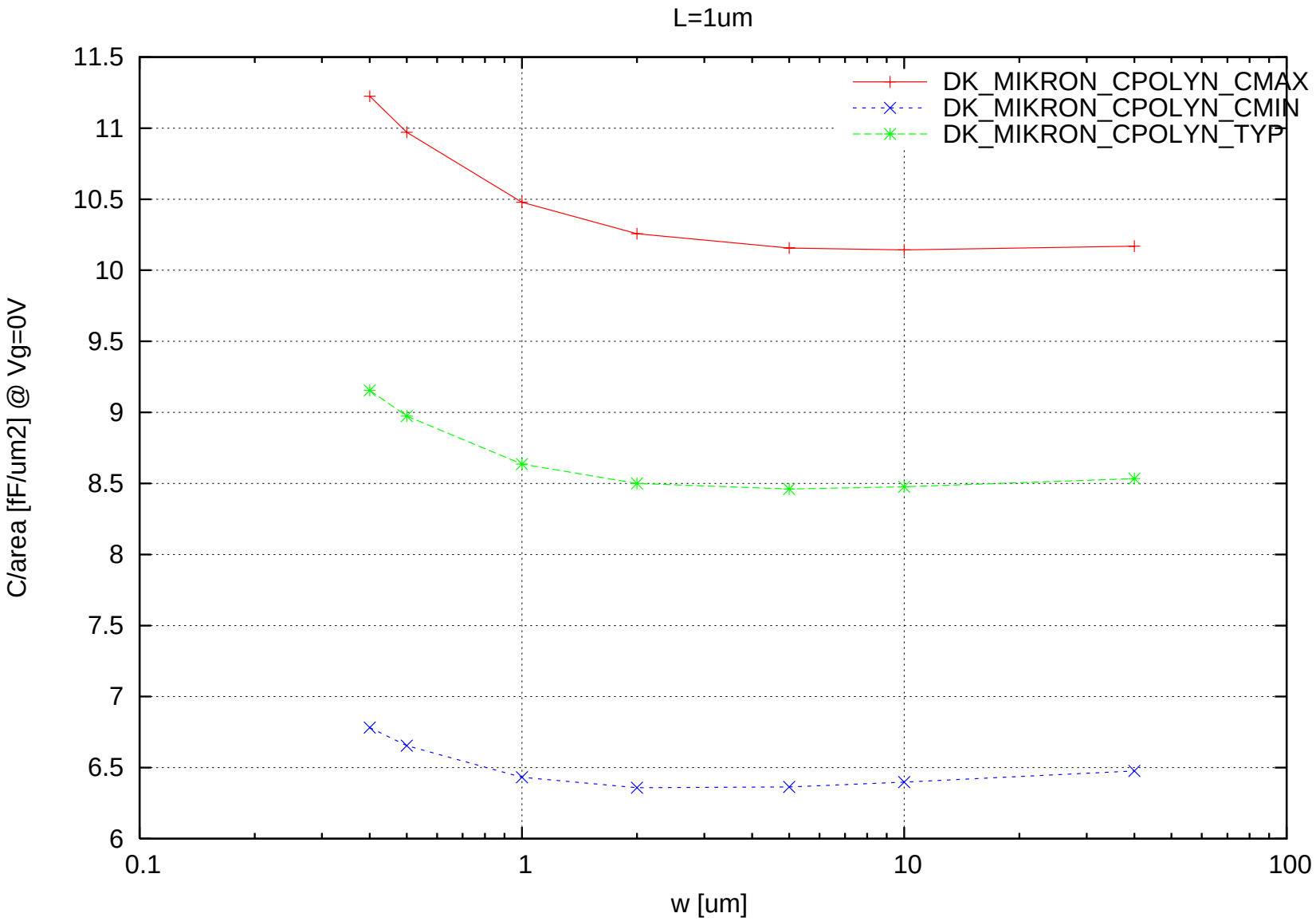

CPOPW

Electrical characteristics scaling

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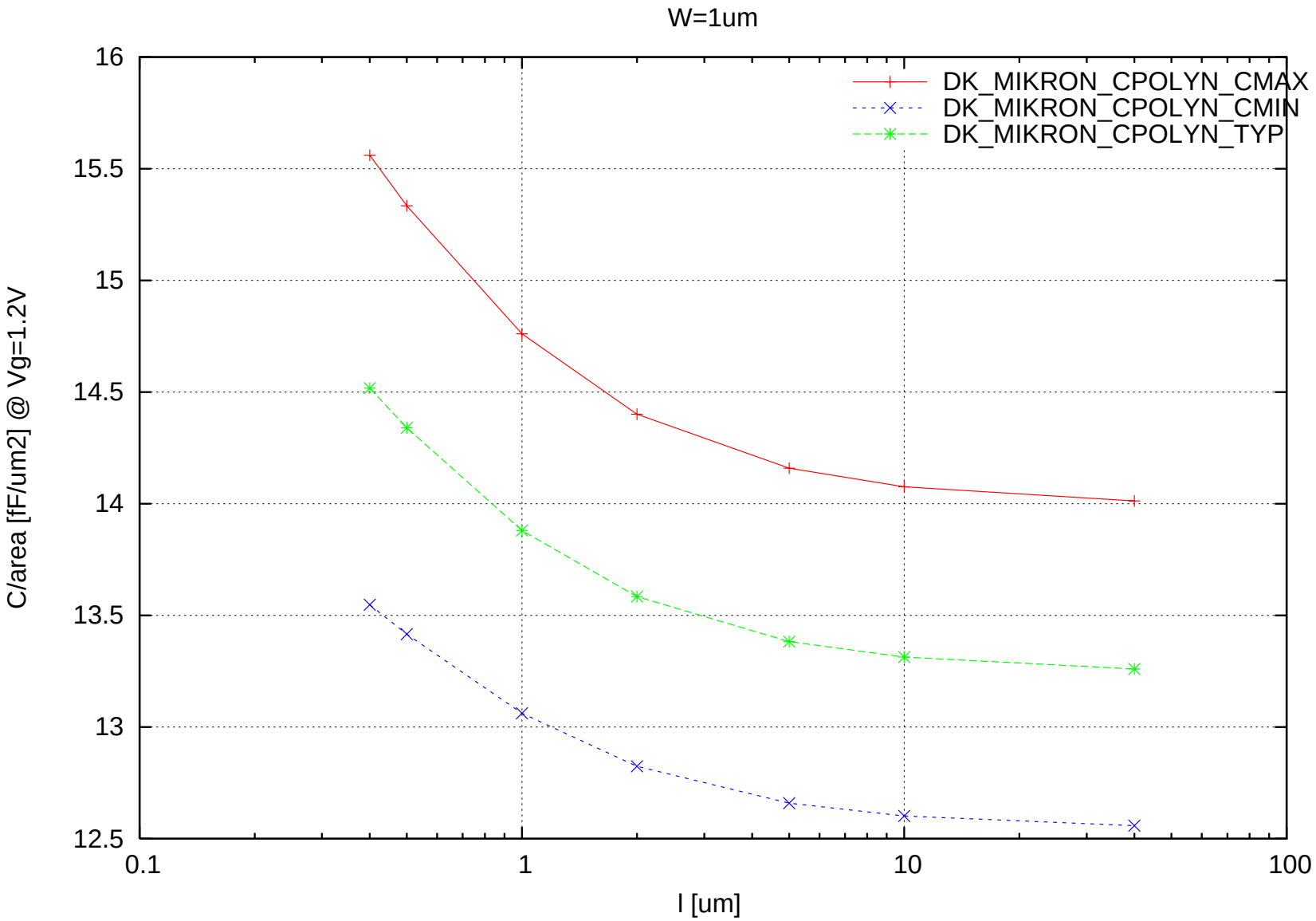

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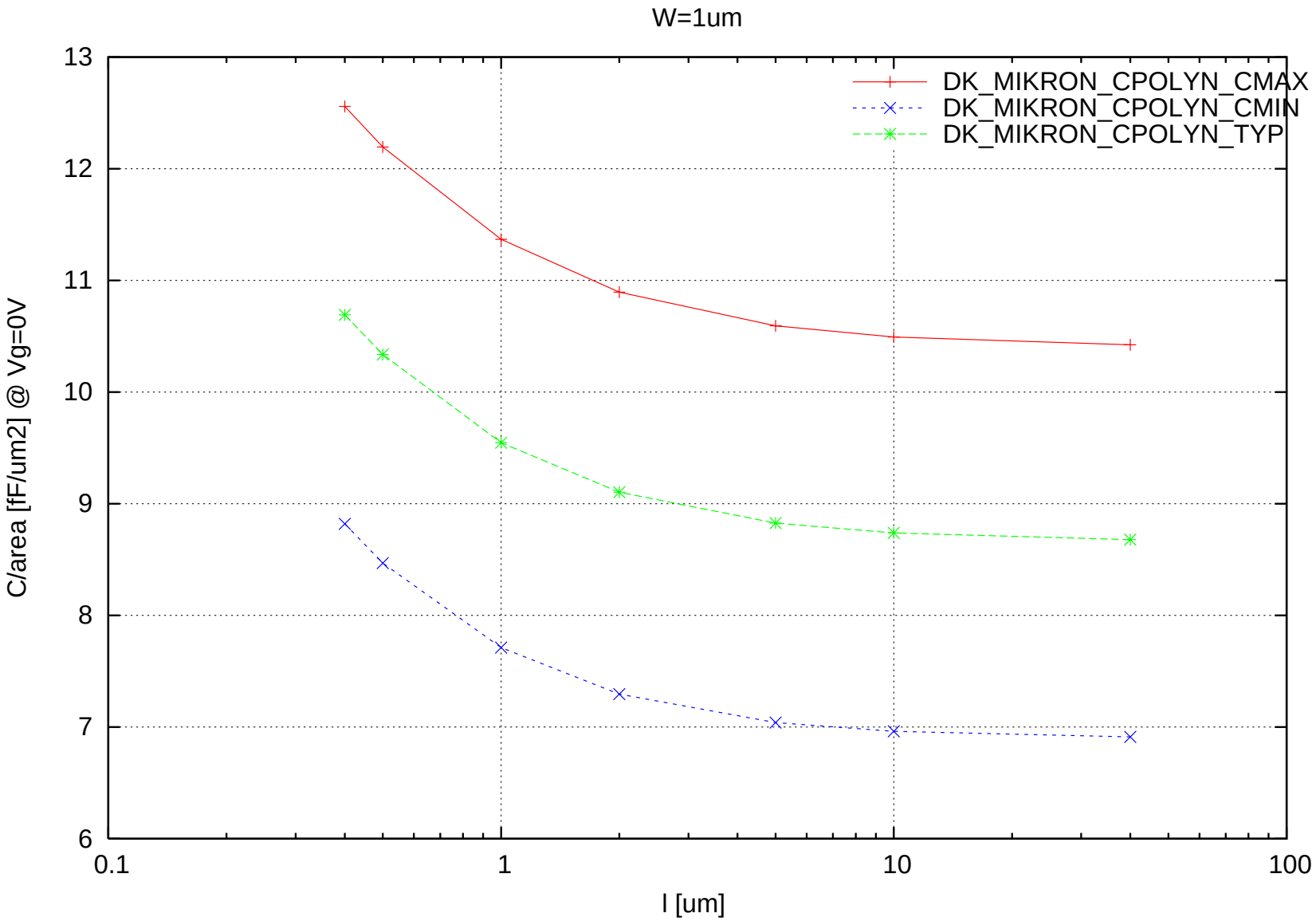

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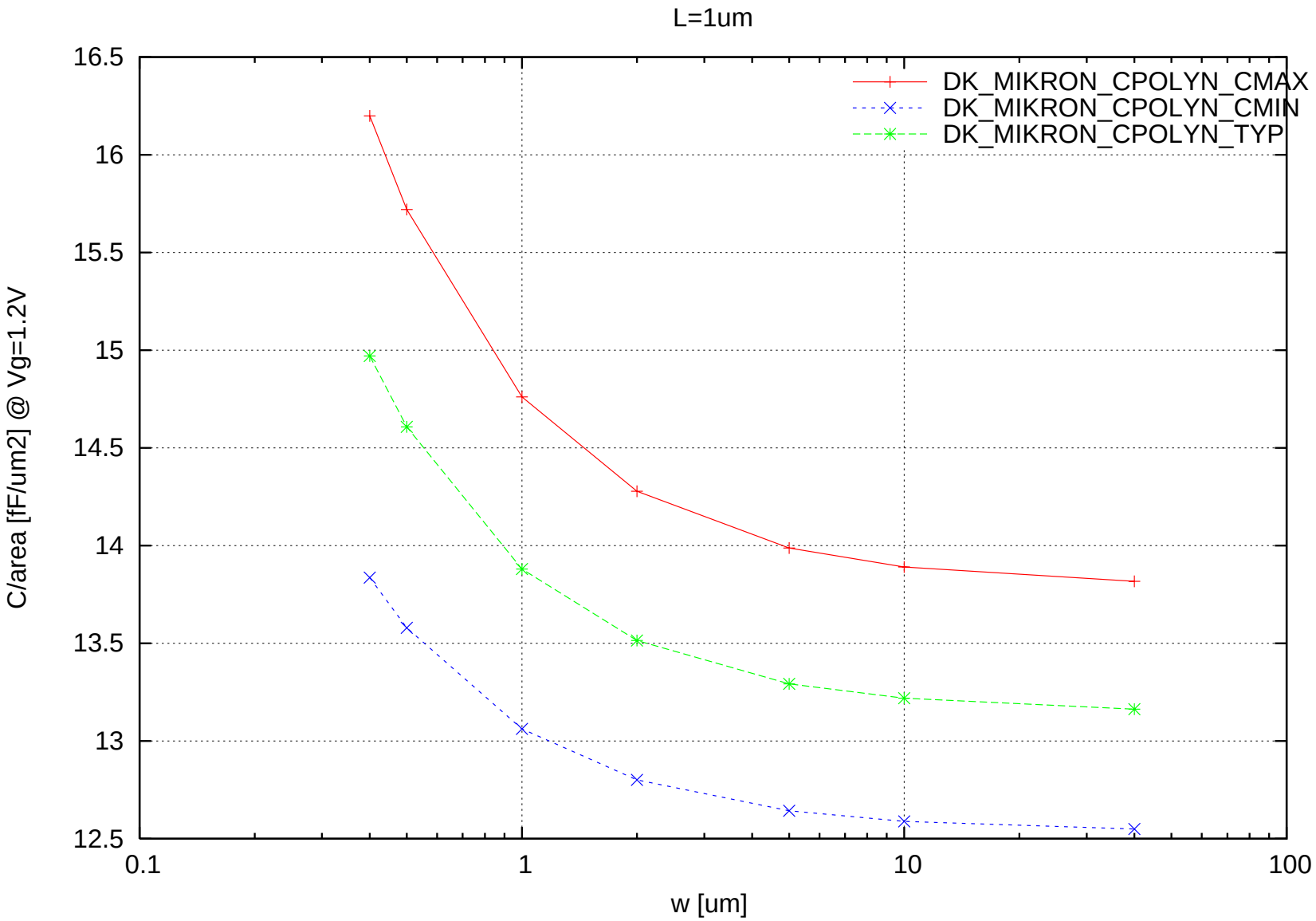
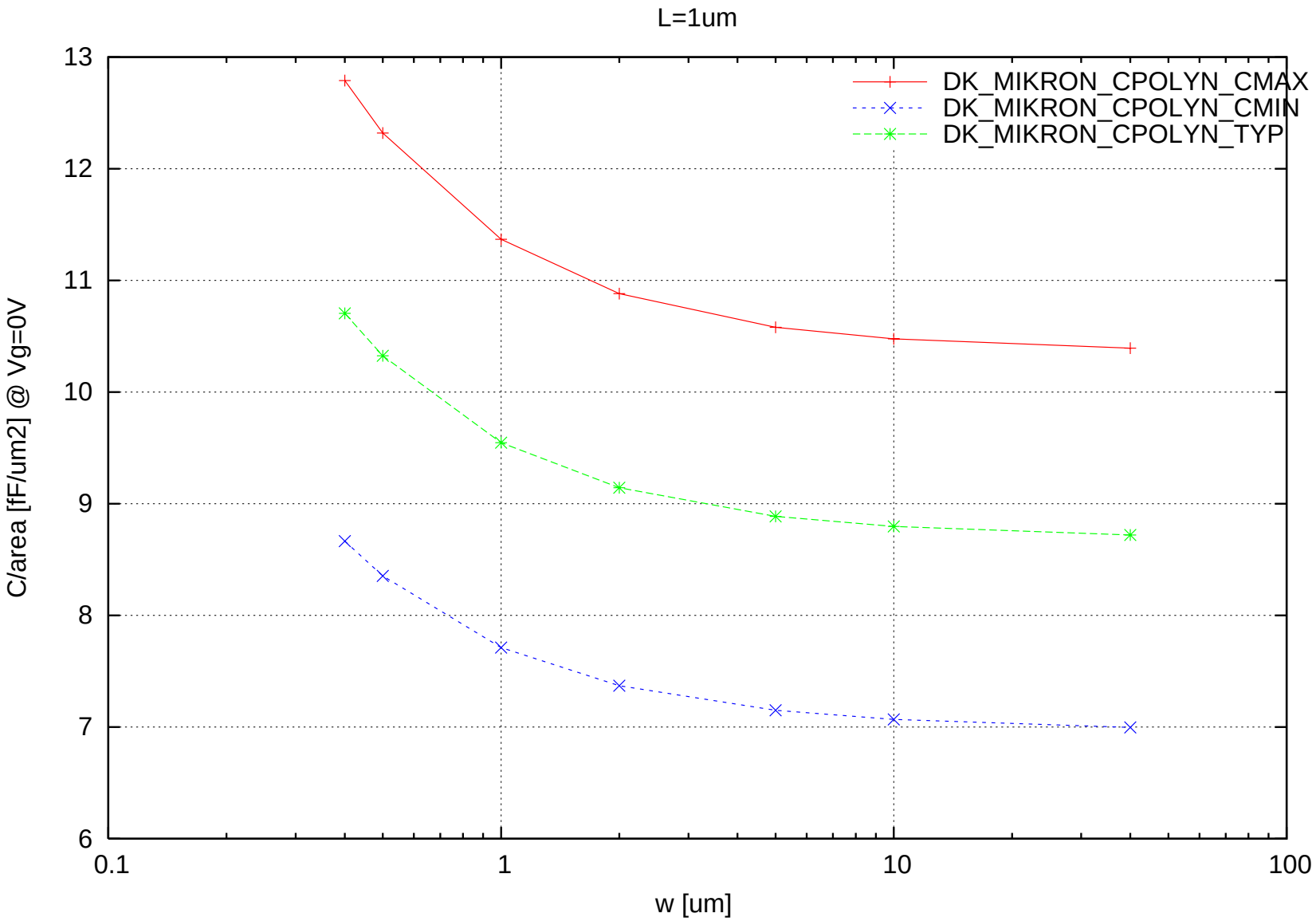
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