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Design of a CMOS Comparator for Low Power and High Speed

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Abstract

This paper reports comparator design for low power & high speed. The present Design is specially design for high resolution Sigma Delta Analog to Digital Converters (SDADCs). Design is based on two stage CMOS OP-AMP technique. Simulation results have been obtained by 0.5 micron technology, considering ±2.5 supply voltage & 2.5 V Input range. Design has been carried out in Tanner tool using HP 0.5 micron technology. Simulation results are verified using S-Edit and W-Edit. We have achieved the propagation delay (speed) of 3.6 nano sec. with low power consumption about 0.31 mW. Finally, compare the proposed results with earlier work done [5], [10] and get improvement in presented results.

Keywords: Sigma-Delta, Comparator, S-Edit, W-Edit, CMOS OPAMP, low power consumption.

Introduction

Comparator is an important device widely used in Analog to Digital Converter (ADC). Among the many architectures of ADC, Sigma delta, designs are used in a large class of applications ranging from low frequency [1] and audio [2] to down converted intermediate frequency and digital video [3]. Their property to Trade speed for accuracy makes them more attractive in the context of present CMOS technology evolution [4]. Low power and high speed ADCs are the main building blocks in the front-end of a radio-frequency receiver in most of the modern telecommunication systems [5]. The ever-growing application of portable devices makes the power consumption a very critical constraint for circuit designers. Comparators are used in

ADCs, data transmission, switching power regulators, and many other applications. The comparator design plays an important role in high speed ADCs.

Power consumption & speed is key metrics in comparator design [6]. For all high-speed ADCs, regardless of the architecture, one of the critical performance limiting building blocks is the comparator, which in large measure determines the overall performance of data converters, including the maximum sampling rate, bit resolution, and total power consumption[7]. In a SDADCs, internal comparators are main building blocks for amplify small voltages into logic levels and the results are stored in the latch which will be used for conversion. This comparator gives high speed & low power consumption for using in SDADCs design. Comparators can be divided into open-loop and regenerative comparators. The open loop comparators are basically op-amps without compensation. Regenerative comparators use positive feedback. Similar to sense amplifier or flip-flops, to accomplish the comparison of the magnitude between two signals. A third type of comparator emerges that is a combination of the open-loop and regenerative comparators. This combination results in comparators that are extremely fast [8]. This Design proposed the high speed & low power consumption comparators referred as an open loop comparators.

Comparator Design

A comparator acts as the quantizer in the ADCs. Since the comparator is of 1-bit it has only two levels either a '1' or a '0'. A '1' implies that V_{DD} = + 2.5V and a '0' implies that V_{SS} = - 2.5V. If the input of the comparator is greater than the reference voltage (V_{ref}) it has to give an output of '1' and if the comparator input is less than reference voltage then the output of the comparator should be '0'. A simple comparator performs the required function efficiently. Given a reference level, a comparator gives an output of V_{DD} when the signal is greater than the reference level and an output of V_{SS} when signal is less than reference level. In this design the V_{ref} = 0V. The operational amplifier can be used as a comparator. In this comparator design we have used the two stage CMOS OPAMP design technique for achieving high speed & low power consumption. Eliminated the compensation capacitor which will be used for designing a high gain two stage CMOS OPAMP topology and reduced the power consumption & increase speed in the presented design. Compensation capacitor is used in two stage CMOS OPAMP for providing stability in the design, compromise with stability to obtain the high performance as low power consumption with high speed. Present CMOS comparator design is shown in Fig.1. This comparator consists by using current mirrors, current sinks, active load & constant current source. Transistor W/L ratios are as selected which gives accurate & optimum results. Parasitic effects which influences in the comparators performance is minimized in this design. This help to get the desired output for a high speed & low power consumption. Present Design has used ± 2.5 Volts power supply for simulation & designing. The comparator circuit as shown in Fig.1 has been simulated using TSPICE with HP 0.5 technology.

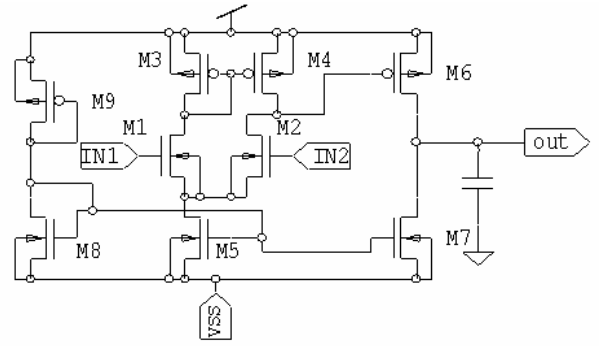

Figure 1: Proposed design of a CMOS comparator.

Simulation Results & Discussion

The simulation is done using Tanner EDA tool with HP 0.5 technology. We apply sinusoidal wave of 2.5 V amplitude with 5 kHz frequency on IN1 terminal and other terminal is grounded. Comparators perform the comparison for these inputs and we have obtained the response as square wave output and is presented in Fig.2. Generally comparators work as a one bit ADCs so the output response of comparator is used to evaluate the binary values for an analog output. All the simulated responses are reported for a period of 0.0002 sec to 0.001sec. Average power consumption for this period (0.0002sec to 0.001sec) has been observed from net list output file and the output result is shown in Fig.4 and power consumption is about 0.31 mW. The output results for power consumption are shown in Fig.3. Power consumption is the most important factor for designing a high performance comparator which will be used in SDADCs design. Speed of the reported design is obtained by apply the square wave of 2.5 V amplitude to IN terminal of the comparator. Obtained results are presented in Fig.4. The speed of the proposed design is measured by observing the difference between 50% rise of input & output waveform as shown. The speed of this design is 3.6 nano sec. Slew rate is 11.85 V/μs as shown in Fig. 5. We have compared present design results with earlier reported work and get improvement in the reported design and are shown in Table 1.

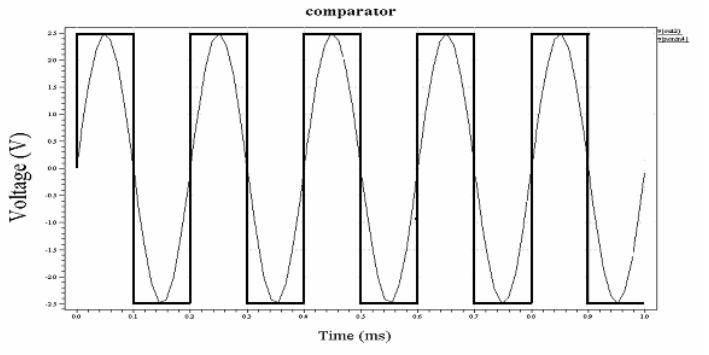

Figure 2: Output of Comparator for sinusoidal wave of 5 KHZ frequency.

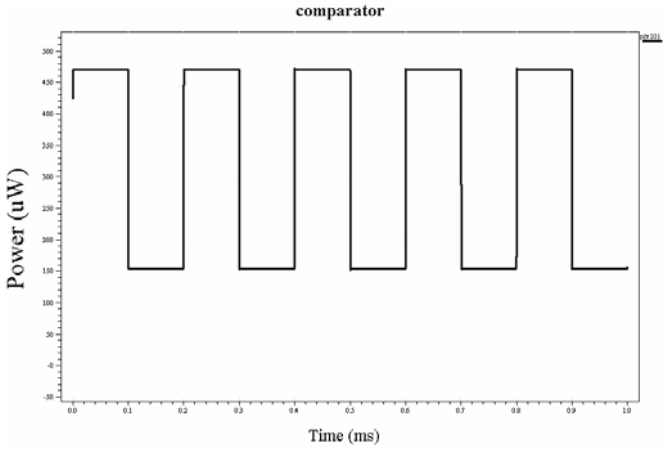

Figure 3: Present design results for power consumption.

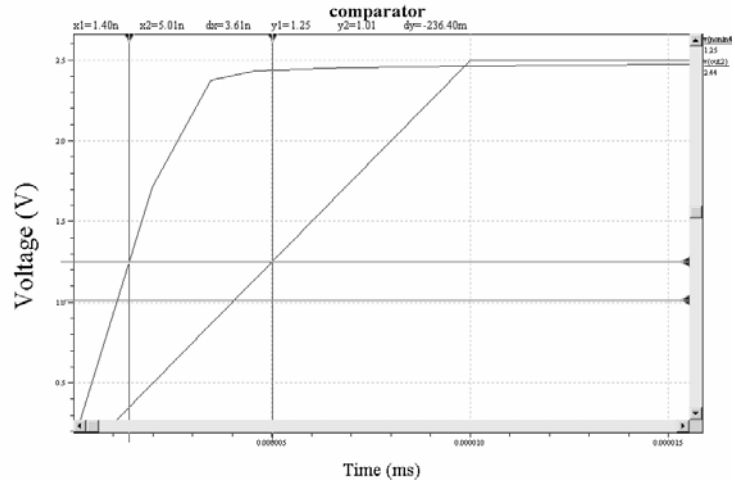

Figure 4: Present design results for speed.

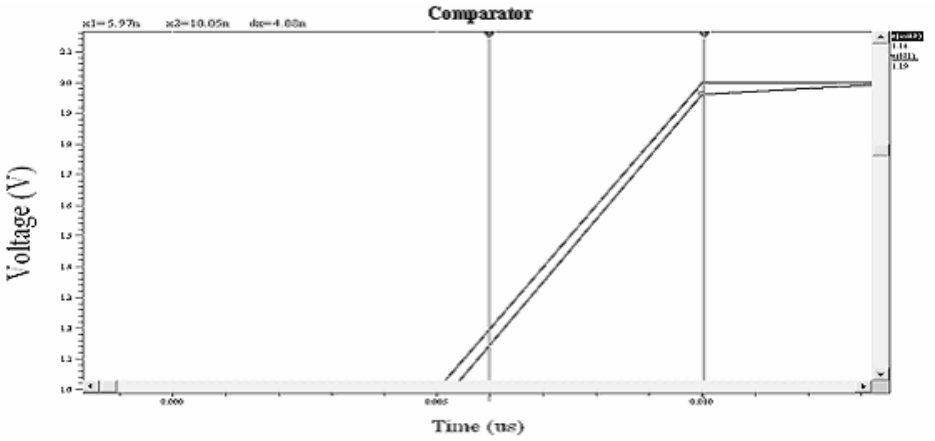

Figure 5: Results for slew rate of Comparator.

Table 1: Comparison of the design parameters of present comparator design with the earlier designs.

Performance parameters	Earlier work by [5]	Earlier work by [10]	Present work
Power supply	5 V	5 V	2.5 V
Speed	-	17.3 nsec	3.6 nsec
Power consumptions	1.8 mW	0.8 mW	0.31 mW
Input range	2 V	2-3 V	2.5 V

Conclusions

This paper has presented the CMOS comparator design and its simulation results of high speed, low power consumption. Design has used the two stage CMOS OPAMP design technique generally it referred as an open loop comparators where we eliminate the compensation to achieved better performance. This comparator is designed for used in high resolution sigma delta ADCs. Simulation results is obtained by cosidering ± 2.5 V power supply. Here we achieved the high speed of 3.6 nano sec and power consumption of 0.31 mW as compare to earlier reported work [5,10], comparison shown in Table 1.

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References

[1] Y. Perelman, R. Ginosar, 2001, “A low light level sensor for medical diagnostic applications”, IEEE, JSSC, Vol.36, No.10, Oct. 2001.

[2] L. Coban, P. E. Allen, “A 1.5 V, 1.0 mV Audio $\Delta\sum$ modulator with 98 db dynamic range”, Digest of technical papers, ISSCC 1999.

[3] L. Breems, E. J. Vander Swam and J. H. Huijsi, 2000, “A 1.8 mW CMOS $\sum\Delta$ modulator with integrated Mixer for A/D conversion of IF signals”, IEEE Journal of solid state circuits, Vol.35, April 2000.

[4] K.Vleugels, S. Rabii and B. A. Wooky, 2001, “ A 2.5 V Broad band multi bit $\sum\Delta$ modulator with 95 db dynamic range”, Digest of Technical Papers, Feb.2001.

[5] B. Razavi and B. A. Wooley, “ Design Techniques for High-speed, High-Resolution Comparators”, IEEE Journal of solid state circuits, Vol. 27, No. 12, Dec. 1992.

[6] Sunghyun Park and Michael P. Flynn, 2006,“A Regenerative Comparator Structure With Integrated Inductors”, IEEE Transactions on circuits and systems-I: Regular papers, Vol. 53, No. 8, Aug. 2006.

[7] X. Li, W. L. Kuo, Y. Lu, R. Krithivasan, T. Chen, J. D. Cressler, and A. J. Joseph, 2005, “ A 7-bit, 18 GHz SiGe HBT Comparator for Medium Resolution A/D Conversion”, IEEE 2005.

[8] P. E. Allen and D. R. Holberg, 2002, “CMOS Analog Circuit Design”, 2nd Edition, Oxford. University Press, 2002.

[9] D. F. Hoeschele, 1994, “ Analog-to-Digital and Digital-to-Analog Conversion Techniques”, John Wiley & Sons, 1994.

[10] M. B. Guermaz, L. Bouzerara, 2006,“High Speed Low Power CMOS Comparator for Pipeline ADCs”, Proc. 25th Int. Conf. On Microelectronics (MIEL-2006), Belgarde, Serbia Montenegro, 14-17 May. 2006.

[11] N. H. E. Weste and K. E. Ihraghian, 1993 “Principle of CMOS VLSI Design”, 2nd Ed., Reading: Addison-Wesley. 1993.

[12] B. Razavi, 1995, “Principles of Data Conversion System Design”, IEEE Press, 1995.