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A Constant-g_m Rail-to-Rail Op Amp Input Stage Using Dynamic Current Scaling Technique

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***Abstract*— In this paper, we introduce an innovative constant-transconductance (g_m) CMOS input stage. Rather than handling the tail currents of the input differential pairs, the proposed circuit scales the output signal currents of the input differential pairs dynamically for a constant g_m while keeping tail currents of the input transistors unchanged. The operation of the new circuit does not rely on quadratic characteristic of the input MOS devices, and is independent of the operation regions of the input transistors. The new constant-g_m scheme, which has potentials for high-frequency applications, can be employed universally to both short and long channel transistors, and is suitable for new generations of deep submicrometer CMOS technologies. The technique is demonstrated through the design of a rail-to-rail CMOS Op Amp with 3 V of supply voltage in 0.35 μm CMOS technology. Simulations show that, when the input common-mode voltage swings from rail to rail, the Op Amp's input stage g_m varies around $\pm 1.5\%$ and $\pm 2.9\%$, respectively, for input transistors in the strong and weak inversion regions.**

I. Introduction

In recent years, there has been significant interest in analog integrated circuits operating with low supply voltages. Op Amp, one of the most widely used building blocks, is not an exception. The input common-mode voltage ($V_{i,cm}$) of an Op Amp should be kept as wide as possible in many applications to keep a high signal-to-noise ratio with a low supply voltage [1], [2], [3], [4]. The conventional scheme to achieve a rail-to-rail input common-mode voltage range is through utilizing a complementary input stage with both p-channel and n-channel differential pairs in parallel, as shown in Fig. 1(a). However, the transconductance (g_m) of this input stage when both differential pairs are in full operation (Region II in Fig. 1(b)) is twice of that when only one pair is in active (Region I or III in Fig. 1(b)). The large variation of the input stage transconductance prevents optimal frequency compensation, and introduces large variation in unity-gain bandwidth and severe signal distortion [1], [2], [3], [4].

A number of schemes have been proposed in the literature to obtain a rail-to-rail constant g_m. One general approach is through controlling the DC tail currents of the differential input pairs, including square root circuit [1], [2], [3] and 1:3 current mirror circuit [1], [5], [6]. However, these schemes may not be applied to CMOS input stage operating in the weak inversion region. In [7] and [8], back-up pairs were used to keep a constant g_m. Although the schemes work well in weak inversion, the systematic g_m variation in strong inversion is as large as 20%. Another technique employs maximum/minimum current selection circuits to maintain constant g_m such as those circuits in [9], [10]. They all have low g_m variations and can operate well in all operation regions of input MOS devices, but the large-signal settling behavior of these schemes is not optimal. More recent works include [11], [12], which all achieve within $\pm 5\%$ variations in g_m. The first scheme [11] uses two identical n-channel input differential pairs, two identical source followers as DC level shifters, and employs a feedforward canceling stage which cancels the g_m contribution of one input pair at mid-supply common-mode input. The second scheme [12] maintains a constant g_m by using DC level

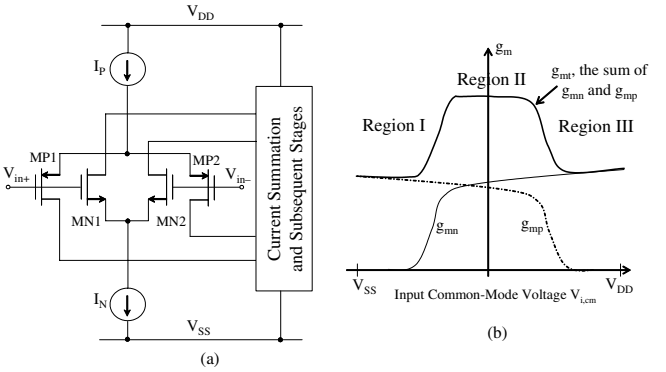

Fig. 1. Traditional complementary rail-to-rail CMOS amplifier input stage, (a) basic circuit configuration, (b) g_m vs. with input common-mode voltage.

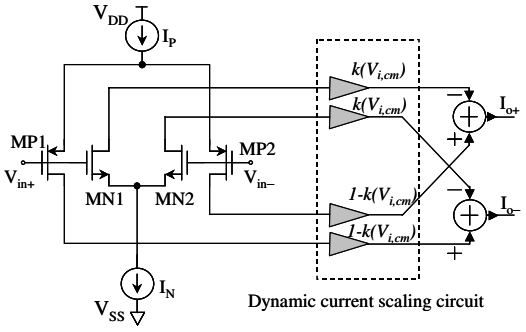

Fig. 2. Basic structure of the proposed rail-to-rail constant-g_m input stage.

shifters combined with two static feedback loops, but the g_m variation is sensitive to V_T and supply voltage changes. In this contribution, we propose a new dynamic current scaling technique that can ensure very low input stage g_m variation independent of the operation regions of the input devices.

II. Proposed Constant-g_m Rail-to-Rail Input Stage

The basic structure of the proposed constant-g_m input stage is illustrated in Fig. 2. Transistors MN1 and MN2 form an n-channel input differential pair, and MP1 and MP2 form a p-channel input differential pair. Both pairs are biased with a nominal tail current level of I_{tail}. The output currents of differential pair (MN1, MN2) are applied to two identical current scaling circuits to scale the currents by a factor of $k(V_{i,cm})$ varying from 0 to 1 with $V_{i,cm}$. Similarly, another two identical current scaling circuits are connected to the output nodes of (MP1, MP2) to scale the output currents of the p-channel input pair by a factor of $1 - k(V_{i,cm})$. The output currents I_{O+} and I_{O-} in Fig. 2 are combined together in a current summation stage [5] that is not shown for the sake of brevity.

A. Basic Operating Principles

The basic principle to compensate for g_m variation is to use dynamic current scaling technique to scale output currents of the complementary differential pairs according to the input common-mode voltage, $V_{i,cm}$, and hence the name of the technique.

According to Fig. 2, the output current of MN1, $i_{O,MN1}$, is given by

$$i_{O,MN1} = -\left(g_{mn}\frac{v_{id}}{2} + \frac{I_N}{2}\right) \tag{1}$$

where g_{mn} is the transconductance of the n-channel differential pair, v_{id} is the differential input signal voltage, and I_N is the tail current of the n-channel pair. Note that I_N, and hence g_{mn}, becomes zero, when $V_{i,cm}$ approaches the negative power supply rail V_{SS}. The leading negative sign at the right side of (1) comes from the fact that we assume the reference direction of the current is flowing out to the load.

Similarly, the output current of MN2, $i_{O,MN2}$, is given by

$$i_{O,MN2} = -\left(-g_{mn}\frac{v_{id}}{2} + \frac{I_N}{2}\right). \tag{2}$$

The output currents of MP1 and MP2 are

$$i_{O,MP1} = -g_{mp}\frac{v_{id}}{2} + \frac{I_P}{2} \tag{3}$$

and

$$i_{O,MP2} = g_{mp}\frac{v_{id}}{2} + \frac{I_P}{2} \tag{4}$$

respectively, where I_P is the tail current of the p-channel pair. Note that I_P and g_{mp} become zero, when $V_{i,cm}$ approaches the positive power supply rail V_{DD}.

According to Fig. 2, the combined output currents I_{O+} and I_{O-} can be written as,

$$\begin{aligned} I_{O+} &= -i_{O,MN1} + i_{O,MP1} \\ &= k(V_{i,cm})\frac{g_{mn}v_{id} + I_N}{2} \\ &\quad (1-k(V_{i,cm}))\frac{g_{mp}v_{id} + I_P}{2} \end{aligned} \tag{5}$$

$$\begin{aligned} I_{O-} &= -i_{O,MN2} + i_{O,MP2} \\ &= k(V_{i,cm})\frac{-g_{mn}v_{id} + I_N}{2} \\ &\quad +(1-k(V_{i,cm}))\frac{-g_{mp}v_{id} + I_P}{2}. \end{aligned} \tag{6}$$

Thus, the total g_m of the input stage in Fig. 2 is given by

$$g_{mt} = \frac{I_{O+} - I_{O-}}{v_{id}} = k(V_{i,cm})g_{mn} + (1-k(V_{i,cm}))g_{mp}. \tag{7}$$

When $V_{i,cm}$ approaches the positive (or negative) supply rail, only the n-channel (p-channel) pair is active, thus $k(V_{i,cm})$ becomes 1 (or 0) and $1-k(V_{i,cm})$ becomes 0 (or 1). Thus the total transconductance g_{mt} of the input stage is g_{mn} (g_{mp}), the transconductance of the n-channel (p-channel) pair. When $V_{i,cm}$ is at the mid-supply range, both n-channel and p-channel pairs are operating, hence $k(V_{i,cm})$ and $1-k(V_{i,cm})$ are around 0.5. The n-channel and p-channel pairs each contribute around half of the g_{mt}. Therefore, by varying the value of $k(V_{i,cm})$, g_{mt} is maintained nearly constant over the entire $V_{i,cm}$ range.

B. Circuit Implementation

Fig. 3 illustrates circuit implementation of the rail-to-rail input stage with the proposed dynamic current scaling technique described in Fig. 2.

The output currents of the p-channel differential pair (MP1, MP2) are scaled by two n-channel differential pairs (MN11, MN12) and (MN13, MN14), which function as the n-channel dynamic current scaling circuit. Each of the differential pairs (MN11, MN12) and (MN13, MN14) is biased by a tail current of I_{BN}. The circuit operation can be explained as follows: (i) When $V_{i,cm}$ is close to V_{SS}, V_a is much higher than V_b. MN12 and MN13 cut off. All output currents of the p-channel input pair (MP1, MP2) are steered to the next stage, current summation circuit. Scaling factor $1-k(V_{i,cm})$ in Fig. 2 is 1. (ii) When $V_{i,cm}$ is at mid-supply voltage, $V_a \approx V_b$, around half of the output current of differential pair (MP1, MP2) passes through. Scaling factor $1-k(V_{i,cm})$ becomes around 0.5. (iii) When $V_{i,cm}$ approaches V_{DD}, V_a is much lower than V_b, all of the output currents of the input differential pair (MP1, MP2) are steered to MP15 and MP16 and discarded. Thus differential pair (MP1, MP2) will not contribute to any signal gain. Scaling factor $1-k(V_{i,cm})$ is 0. Note that MP15 and MP16 form a cascode structure to bias the drain terminal voltage of (MN12, MN13) at a similar level to those of MN11 and MN14. The n-channel differential pair (MN1, MN2) and p-channel dynamic current scaling circuit work in a similar way but a complementary fashion.

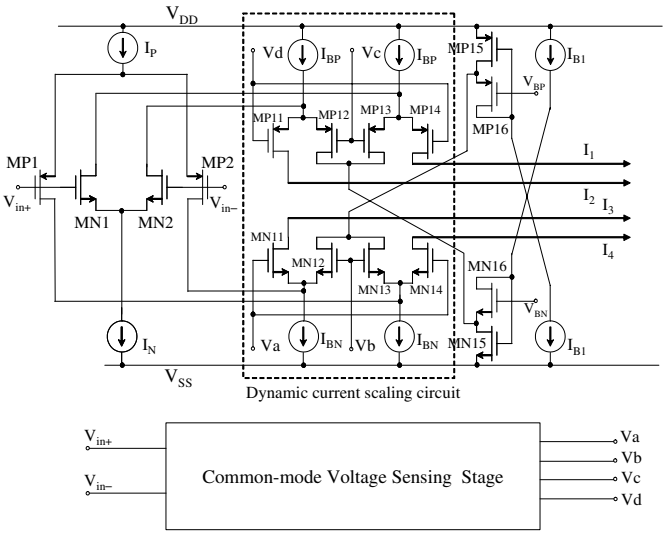

Fig. 3. Circuit implementation of the proposed rail-to-rail constant-g_m input stage.

The common-mode voltage sensing circuit illustrated in Fig. 4 generates V_a, V_b, V_c, and V_d in Fig. 3. The common-mode input voltage $V_{i,cm}$ of differential pair (MP21, MP22) is compared with the mid-supply voltage $V_{CM,REF}$. (MN24, MN26) and (MN25, MN27) form two current mirrors. For low $V_{i,cm}$ levels, most of the drain current of MP26, I_{tail}, flows through differential pair (MP21, MP22), current mirror (MN24, MN26), and diode-connected transistor MP24. Thus V_a is much higher than V_b, and V_c is much lower than V_d. While for high $V_{i,cm}$ levels, most of I_{tail} flows through current mirror (MN25, MN27) and diode-connected transistor MP25, causing V_b to be much higher than V_a, and V_d to be much lower than V_c. Fig. 5 illustrates how V_a to V_d change with the $V_{i,cm}$. In order to leave enough voltage headrooms for I_{BN} and I_{BP}, extra attentions should be paid when sizing the trasistors (MN24, MN25) and (MP24, MP25).

III. Simulation Results

Based on the proposed constant-g_m input stage, a rail-to-rail input/output CMOS Op Amp has been designed in a standard 0.35 μm CMOS technology. The Op Amp consists of a rail-to-rail input stage (Fig. 3), a current summation stage (Fig. 6) and a rail-to-rail class AB output stage (Fig. 6) [13]. To enhance the DC gain of the

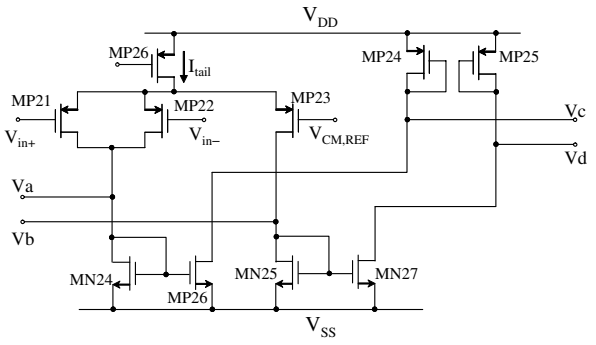

Fig. 4. Circuit implementation of the common-mode voltage sensing stage in Fig. 3.

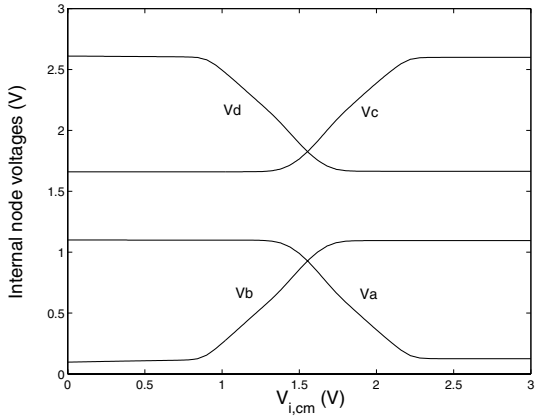

Fig. 5. Node voltages V_a to V_d vs. $V_{i,cm}$ in the proposed rail-to-rail input stage.

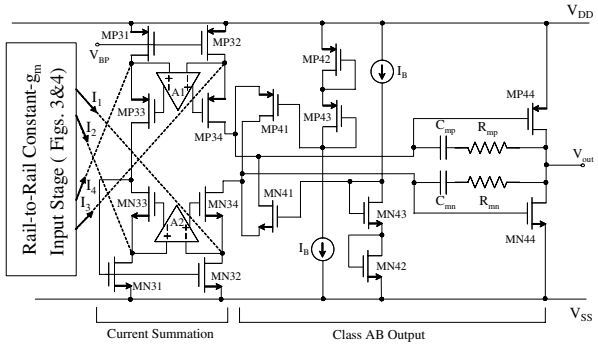

Fig. 6. Current summation and class AB output stages.

Op Amp, two gain-boosting amplifiers A1 and A2 have been added. In addition, the Miller compensation capacitors C_{mn} and C_{mp} are tunable to accommodate different load conditions. The Op Amp is currently being fabricated through MOSIS, and we only present post-layout simulation results here.

Fig. 7(a) shows the simulated results of the total input stage transconductance g_{mt}, along with the individual g_m contributions of each input differential pair (i.e., $g_{mn,c}$=$k(V_{i,cm})g_{mn}$ and $g_{mp,c}$=$(1-k(V_{i,cm}))g_{mp}$), versus $V_{i,cm}$ for I_{tail}=240 μA and V_{DD}=3 V. The g_{mt} variation is $\pm 1.5\%$ as simulated. For input transistors operating in the weak inversion region (I_{tail}=15 μA), the simulated g_m variation is $\pm 2.9\%$ as shown in Fig. 7(b). The proposed circuit works very well for both the strong and weak inversion operation regions of the input transistors. We note that, even though the above results

TABLE I

OP AMP CHARACTERISTICS (POST-LAYOUT SIMULATION) WITH A 3-V SUPPLY VOLTAGE AND DIFFERENT LOADS.

Load	1 MΩ ‖ 15 pF	50 Ω ‖ 33 pF
DC gain (dB)	165	135
GBW (MHz)	47.8	31.7
Phase Margin (deg.)	66.5	72.5
Average Slew rate (V/μs)	42	30
CMRR (dB) (DC)	$\geq$ 100	$\geq$ 100
Vout swing (V)	rail-to-rail	0.36$\sim$2.59
Power consumption (mW)	9.8	9.8

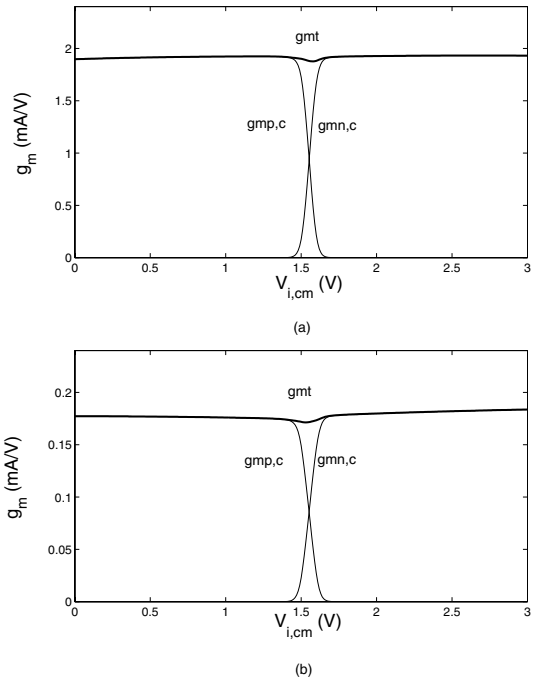

Fig. 7. Simulated g_m vs. $V_{i,cm}$ of the input stage (Fig. 3), (a) in strong inversion region, (b) in weak inversion region.

are obtained using 3-V supply voltage, this rail-to-rail input stage can still operate with supply voltage as low as 2.5V. Fig. 8 shows variations of $g_{mn,c}$, $g_{mp,c}$, and g_{mt} under different supply voltages. The small g_{mt} variation is mainly contributed by the limited output resistance of tail current sources. It is also interesting to mention that the total slew rate of the Op Amp's input stage is constant over the entire $V_{i,cm}$ range as the total limit current of this input stage (i.e., $I_{tot} = \sum_{i=1}^{4} |I_i|$ in Fig. 3) keeps nearly constant, as depicted in Fig. 9.

Fig. 10 shows the frequency responses of the entire amplifier for different $V_{i,cm}$ values. The amplifier has a DC gain (A_{vo}), gain-bandwidth product (GBW), and phase margin (PM) better than 130 dB, 30 MHz and 60°, respectively. The GBW and PM of this Op Amp remain almost independent of $V_{i,cm}$. Finally, Fig. 11 shows the transient response to a 3-V_{pp} 100-KHz rectangular pulse of the amplifier in unity-gain noninverting configuration. The simulated characteristics of the Op Amp under different loads at $V_{i,cm}$ = 1.5 V are summarized in Table I.

This proposed constant-g_m technique has several advantages. First, the structure of the dynamic current scaling is simple and easy to implement. Hence the resulting two-stage Op Amp is compact which makes it very desirable for VLSI cell libraries. Second, it does not depend on the operation regions of the input CMOS transistors. Third, the high-frequency and large-signal settling behaviors of the resulting

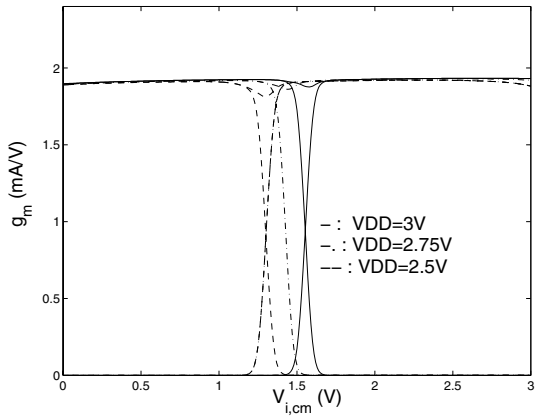

Fig. 8. Simulated g_m vs. $V_{i,cm}$ of the input stage (Fig. 3) under different supply voltages.

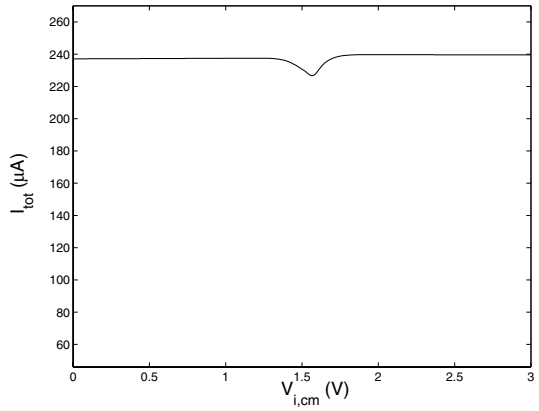

Fig. 9. Simulated I_{tot} vs. $V_{i,cm}$ of the input stage (Fig. 3).

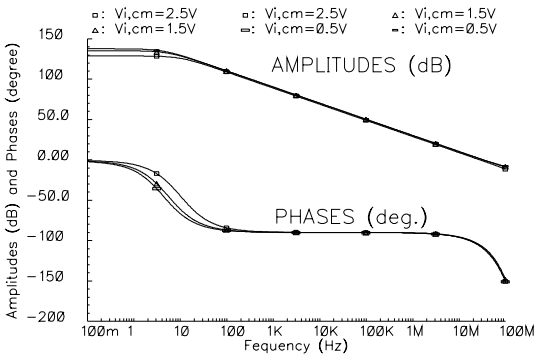

Fig. 10. Frequency responses of the Op Amp (load: 50 $\Omega||33$ pF).

Op Amp are very good.

IV. Conclusion

A novel dynamic current scaling technique for constant-g_m CMOS input stage is introduced in this paper. The new technique can be implemented in any CMOS technologies, and has the potential to be employed in bipolar technology as well. Therefore it considerably simplifies the design of rail-to-rail input Op Amps. The new scheme has been verified through the design of a two-stage Op Amp in 0.35 μm CMOS technology with input transistors in both weak and strong inversions. The circuit achieves nearly constant-g_m (within

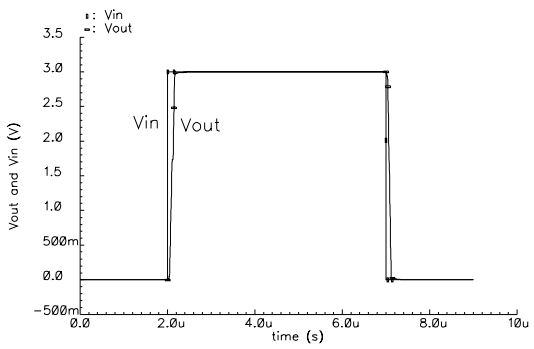

Fig. 11. Transient response of the Op Amp to a 3-V_{pp} 100-KHz rectangular pulse in unity-gain noninverting configuration (load: 1 M$\Omega||$ 15 pF).

$\pm 3\%$) behavior over the full input common-mode voltage range, for both strong and weak operation regions of the input transistors. The authors acknowledge the valuable comments and suggestions of the anonymous reviewers.

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