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Charge Injection and Clock Feedthrough

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CHARGE INJECTION AND CLOCK FEEDTHROUGH

A Thesis

Presented to

The Faculty of the Department of Electrical Engineering

San Jose State University

In Partial Fulfillment

of the Requirements of the Degree

Master of Science

by

Jonathan Yu

May 2010

The Designated Thesis Committee Approves the Thesis Titled

CHARGE INJECTION AND CLOCK FEEDTHROUGH

by

Jonathan Yu

APPROVED FOR THE DEPARTMENT OF ELECTRICAL ENGINEERING

SAN JOSE STATE UNIVERSITY

May 2010

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ABSTRACT

CHARGE INJECTION AND CLOCK FEEDTHROUGH

by Jonathan Yu

Turning off a transistor introduces an error voltage in switched-capacitor circuits. Circuits such as analog-to-digital converters (ADC), digital-to-analog converters (DAC), and CMOS image sensor pixels are limited in performance due to the effects known as charge injection and clock feedthrough. Charge injection occurs in a switched-capacitor circuit when the transistor turns off and disperses channel charge into the source and drain. The source, which is the sampling capacitor, experiences an error in the sampled voltage due to the incoming channel charge. Simultaneously, the coupling due to gate-source overlap capacitance also contributes to the total error voltage, which is known as clock feedthrough. In order to fully understand this behavior, charge injection and clock feedthrough are modeled, simulated, and measured. A basic charge injection/clock feedthrough model is first introduced to identify key components and explain fundamental behavior. This model is expanded upon by using Technology Computer Aided Design (TCAD) simulations, which can more accurately model the distribution of channel charge. TCAD simulations can also easily predict how charge injection and clock feedthrough are affected by various parameters, such as transistor operation, size, and geometry. Test structures are fabricated in a 0.18 µm CMOS process to measure and verify charge injection and clock feedthrough. It is shown that the model and simulations agree within 10%. The measurements are 40% higher than the model, but exhibit good trend agreement with the model and simulations.

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I would like to thank God and many people for providing me inspiration, emotional support, and technical guidance that has led me to the completion of this thesis. I am very fortunate to be surrounded by great people in my academic, professional, and personal life.

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Finally, I would like to thank the love of my life, Yvette, for her support and patience. She has always provided love, encouragement, and happiness.

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1   Introduction

Since its introduction in the early 1960s [1], the metal-oxide-semiconductor field-effect transistor (MOSFET) has become the most widely used semiconductor device in advanced integrated circuits. The transistor is utilized in a variety of circuits, including mixed-signal applications. It is commonly used as a switch in switched-capacitor circuits, which form analog-to-digital converters (ADC), digital-to-analog converters (DAC), and CMOS image sensor pixels. There are, however, inherent non-ideal effects when a transistor is used as a switch in switched-capacitor circuits. These effects often limit the performance of the circuits and they are commonly referred to as charge injection and clock feedthrough.

1.1   Charge Injection and Clock Feedthrough

Charge injection and clock feedthrough are illustrated by using the switched-capacitor circuit shown in Figure 1.1. This circuit uses an NMOS transistor to function as the switch. In the schematic, the NMOS drain is connected to an ideal, low impedance voltage source, while the source is connected to a sampling capacitor. The gate voltage changes from high to low, transitioning the switch from closed to open state.
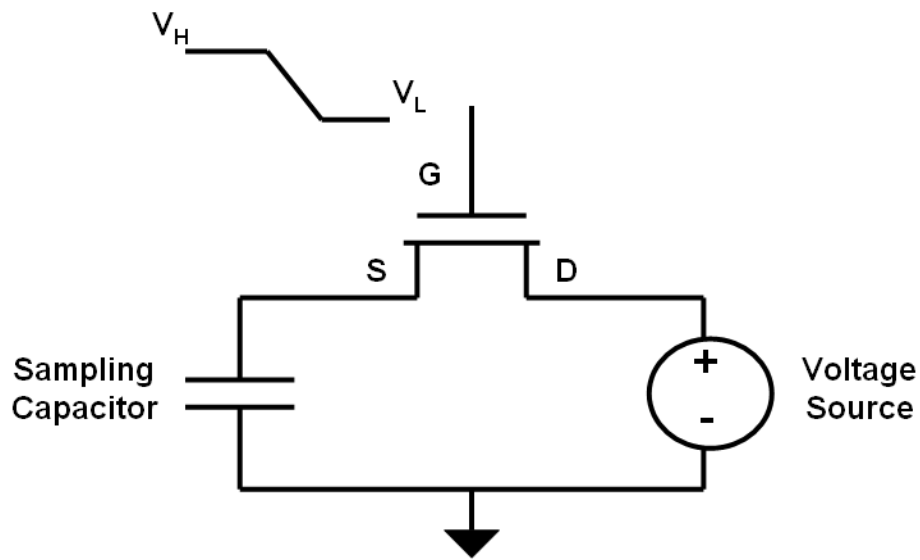
Figure 1.1 Charge injection and clock feedthrough occur in a switched-capacitor circuit when the gate turns off

When the switch is closed, the voltage on the voltage source is sampled on the capacitor. This occurs when the gate of the NMOS transistor is high and the transistor is on. When the switch opens, the voltage on the capacitor should ideally remain unchanged so that it could be processed. However, non-ideal effects from the NMOS switch create an error in the sampled voltage. These effects are known as charge injection and clock feedthrough and they affect the performance of a variety of circuits, including CMOS image sensor pixels and ADCs.

1.2   Effect of Charge Injection/Clock Feedthrough in Various Circuits

Figure 1.2 shows a schematic of a three-transistor (3T) pixel in a CMOS active pixel image sensor. The pixel consists of a photodiode and three transistors: reset, source follower, and row select.
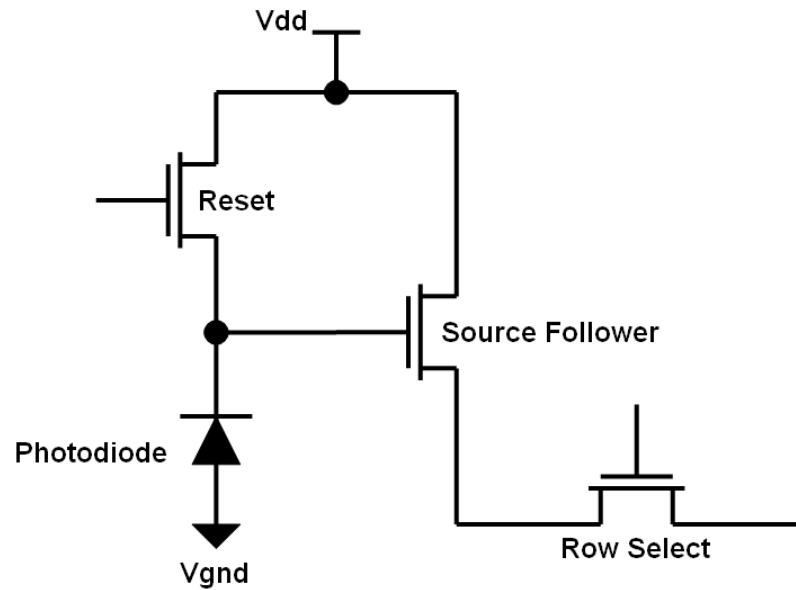
Figure 1.2 Schematic of a 3T CMOS active pixel sensor

An n^+/p-well junction forms the photodiode [2] and its capacitance is used to convert the collected photo charge into voltage. The reset transistor allows the photodiode to be reset and the source follower and row select transistors form the pixel's read out circuitry.

In order to read the charge in a pixel, the photodiode is first reset to Vdd by turning on the reset transistor. This initializes the photodiode and prepares it for integration. Next, the reset transistor turns off to allow for photo charge integration by the photodiode. During integration, the photodiode voltage decreases as photons are converted to electrons. At the end of the integration period, the final photodiode voltage is sampled. The reset transistor is turned on and off to sample the reset voltage. The pixel value is calculated by taking the voltage difference between reset and after photo charge integration. This pixel value is directly related to dynamic range, which is an

important image sensor performance specification. The higher the pixel value, the

greater the dynamic range. The effect of charge injection/clock feedthrough however,

limits dynamic range. Ideally, the photodiode should be reset to Vdd to allow for

maximum voltage swing from the photo charge integration. This is never achieved

because turning off the reset transistor induces charge injection/clock feedthrough and

introduces an offset voltage. This offset results in a sampled voltage less than Vdd and

limits the dynamic range.

Another circuit that is affected by charge injection and clock feedthrough is the

sample-and-hold circuit. This circuit is important to many applications, such as data

converters and switched-capacitor filters. The purpose of the sample-and-hold circuit,

shown in Figure 1.3, is to sample an input and hold the value for a period until it is ready

to be processed.
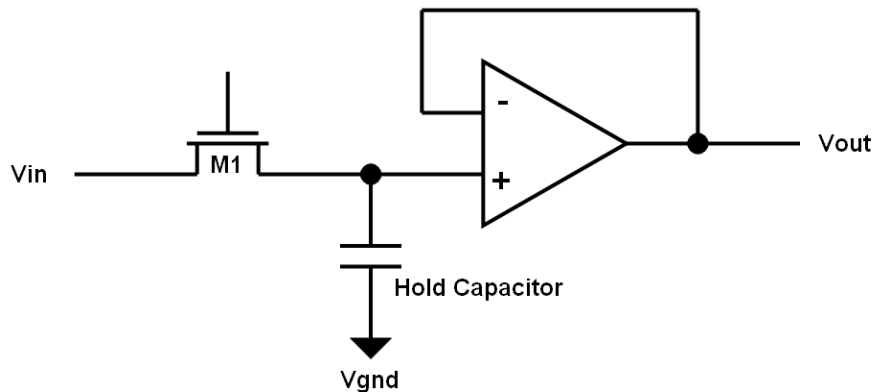
Figure 1.3 Schematic of a sample and hold circuit

This basic sample-and-hold circuit consists of a transistor, hold capacitor, and an op-amp

with unity gain [3]. A pulse is applied to the transistor to allow the hold capacitor to

sample the input voltage. However, similar to the reset transistor in the 3T pixel, when the transistor M1 turns off, charge injection and clock feedthrough create an error in the sampled voltage; this limits the accuracy of the sample-and-hold circuit.

1.3   Previous Research

Charge injection and clock feedthrough have been studied in many different ways. The phenomenon was identified in early publications of switched-capacitor circuits [4] and compensation techniques [5] were used to reduce the effects of charge injection and clock feedthrough. Analytical expressions [6-10] were developed to analyze the switching-off behavior the of MOSFET switch. These expressions were based on lumped-element models and verified using circuit simulators and test structure measurements. Advancements were made to the model when the transistor is in weak inversion [11], and the accuracy was verified experimentally and by using two-dimensional mixed-mode device simulations.

In the previous work, once an analytic model was developed, Computer Aided Design (CAD) tools were relied upon due to the complex nature of charge injection and clock feedthrough. Unfortunately, the majority of the tools were circuit simulators that used compact models for the MOSFET. Problems related to charge non-conservation [12] could cause inaccurate simulation results for switched-capacitor circuits. Therefore, mixed-mode device simulation is the CAD tool better suited to verify an analytic model. Present day computer hardware allows for extensive mixed-mode device simulations in not only the two-dimensional, but the three-dimensional space as well.

1.4 Thesis Objective

The objective of this thesis is to fully understand charge injection and clock feedthrough by developing a model and verifying it through simulations and test structure measurements. A basic charge injection/clock feedthrough model is developed to identify the mechanisms that contribute to this phenomenon. This model is expanded upon by using TCAD simulations to explore how charge injection and clock feedthrough are affected by various parameters, such as transistor operation, size, and geometry. Test structures are designed and fabricated in a 0.18 µm CMOS process to measure and verify charge injection and clock feedthrough.

1.5 Overview of Thesis

This thesis focuses on the study of charge injection and clock feedthrough by using models, simulations, and measurements. Chapter 2 introduces the theory of charge injection and clock feedthrough. A basic model is presented to identify key components and explain fundamental behavior. Chapter 3 discusses the use of TCAD simulations to further examine charge injection and clock feedthrough. The primary focus of this chapter is to explain the methodology for the 2D simulations. The discussion of simulation flow includes detailing process simulation, device simulation, and electrical parameter extraction. Chapter 4 describes the methodology for setting up the 3D simulations. The main difference between 2D and 3D simulation methodology is how the device is generated in process simulation. Chapter 5 discusses the charge injection and clock feedthrough simulation results. By accumulating the 2D and 3D simulation results, this chapter examines the effect that transistor operation, size, and geometry have

on charge injection/clock feedthrough. Test structure measurements are presented in

Chapter 6. This chapter includes a discussion of the test structure designed to measure

charge injection/clock feedthrough, measurement setup, and measured results. Chapter 7

concludes this thesis by summarizing the research results and recommending the

direction for future work.

2 Background

This chapter details the mechanisms that contribute to charge injection and clock feedthrough. A first order model is developed to identify key components and fundamental behavior. While the equations in the model pertain to the NMOS transistor, the physics can also be applied to the PMOS transistor by using the corresponding equations. The model is quasi-steady state and should hold as long as the dielectric relaxation time is much shorter than all timescales.

Figure 2.1 is a cross sectional view of the NMOS transistor modeled. As discussed in section 1.1, this transistor is utilized in a switched-capacitor circuit by connecting the drain to a low impedance voltage source and the source to a sampling capacitor.
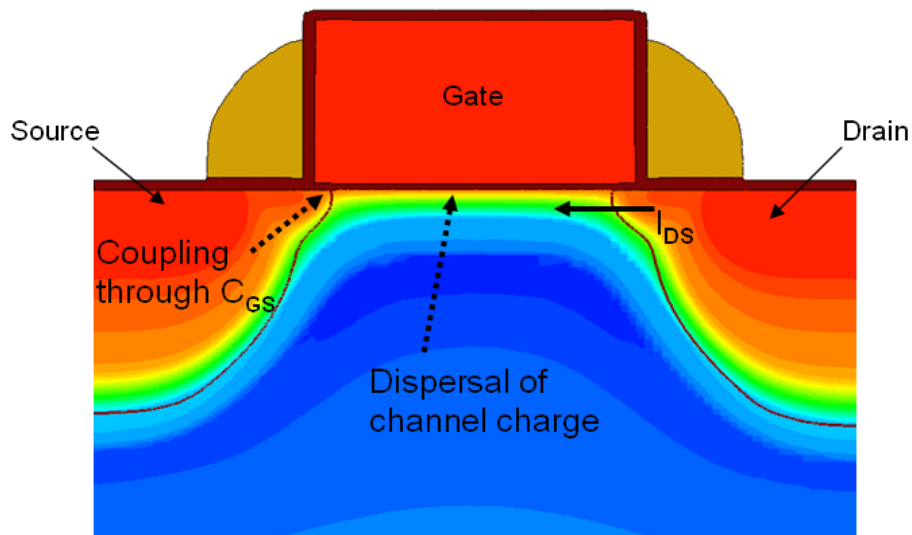
Figure 2.1 Cross sectional view of an NMOS transistor showing channel charge contour. Components that are important when the transistor is turning off are identified.

The figure illustrates the important components when the transistor is turning off. In this first order model, the components are dispersal of channel charge, coupling through overlap capacitance, and source-drain conduction.

2.1 Dispersal of Channel Charge

When the transistor turns off, charge injection occurs and channel charge is dispersed into the source and drain. The charge in the channel, Q_{ch} is a function of gate voltage [13], which can be modeled as

$$Q_{ch} = C_{ox}(V_{GD} - V_t)$$ (2.1)

where,

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$ (2.2)

C_{ox} : Oxide capacitance per unit area (F/cm^2)

ε_{ox} : Permittivity of oxide (F/cm)

t_{ox} : Oxide thickness (cm)

V_{GD} : Gate-drain voltage (V)

V_t : Threshold voltage with back-bias (V)

As the transistor turns off, it is approximated that half of the channel charge enters the drain, while the other half enters the source. Since the drain is connected to an ideal voltage source, the drain voltage remains unchanged. However, channel charge entering the source introduces an error voltage, which can be represented as

$$dV_{Qch} = \frac{Q_{ch}}{2C_S} \tag{2.3}$$

C_S : Total source capacitance (F)

In this model, it is assumed that the charge pumping phenomenon [14] due to the trapping of channel charge by interface states is insignificant.

2.2   Coupling through Overlap Capacitance

When the transistor turns off, clock feedthrough also occurs and contributes to the total error voltage. When the gate swings from high to low voltage, the source voltage is affected due to the coupling through gate-source overlap capacitance. The error voltage introduced due to gate-source coupling can be approximated as a voltage divider.

$$dV_{Col} = dV_G \frac{C_{GS}}{C_{GS} + C_S} \tag{2.4}$$

where,

$$C_{GS} = C_{OL} \cdot W \tag{2.5}$$

C_{GS} : Gate-source overlap capacitance (F)

W : NMOS transistor width (μm)

C_{OL} : Gate-diffusion overlap capacitance (F/μm)

dV_G :   Change in gate voltage (V)

2.3   Source-Drain Conduction

The combined effects of charge injection and clock feedthrough lower the source voltage and create a potential difference between source and drain. This induces a

current that flows between the source and drain, I_{DS}. The current flow allows the

capacitor (connected to the source) to recharge toward the drain voltage. Therefore,

some of the source voltage that is lost due to charge injection and clock feedthrough is

recovered. The drain current I_{DS} is represented as

$$I_{DS} = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L}[2(V_{GS} - V_t)V_{DS} - V_{DS}^2]$$
(2.6)

μ_n: Electron mobility (cm^2/V·s)

L: NMOS transistor length (µm)

V_{GS} : Gate-source voltage (V)

V_{DS} : Drain-source voltage (V)

The recovery of source voltage due to source-drain conduction is approximated as

$$dV_{IDS} = \frac{I_{DS} \cdot dt}{C_S}$$
(2.7)

dt : Change in time (s)

The combined effect of charge injection, clock feedthrough, and source-drain conduction

is discussed in the following section.

2.4 Model Implementation

This section models the combined effect of charge injection, clock feedthrough,

and source-drain conduction when the transistor turns off. By using some assumptions in

the model, plots are generated based on the equations from the previous sections. For

convenience, Vdrain, Vsource, and Vgate will represent drain, source, and gate voltages, respectively.

2.4.1 Model Assumptions

Various assumptions are made to implement this first order model. Table (2.1) summarizes the parameter values used to calculate charge injection, clock feedthrough and source-drain conduction.

Table 2.1 Parameter values used to model the transistor in a 0.18 μm technology node turning off.

Parameter	Symbol	Value	Unit
NMOS transistor width	W	1.0	μm
NMOS transistor length	L	1.0	μm
Total source capacitance	C_S	2.0×10^{-15}	F
Gate-diffusion overlap capacitance	C_{OL}	1.5×10^{-16}	F/μm
Threshold voltage with back-bias	V_t	0.8	V
Drain Voltage	V_D	1.0	V
Electron mobility	μ_n	600	cm^2/V·s
Oxide thickness	t_{ox}	6.0×10^{-7}	cm
Permittivity of oxide	ε_{ox}	3.51×10^{-13}	F/cm

In addition to the parameter values, the waveform shown in Figure 2.2 is applied to the gate to turn off the transistor. The plot illustrates Vgate as a function of time.
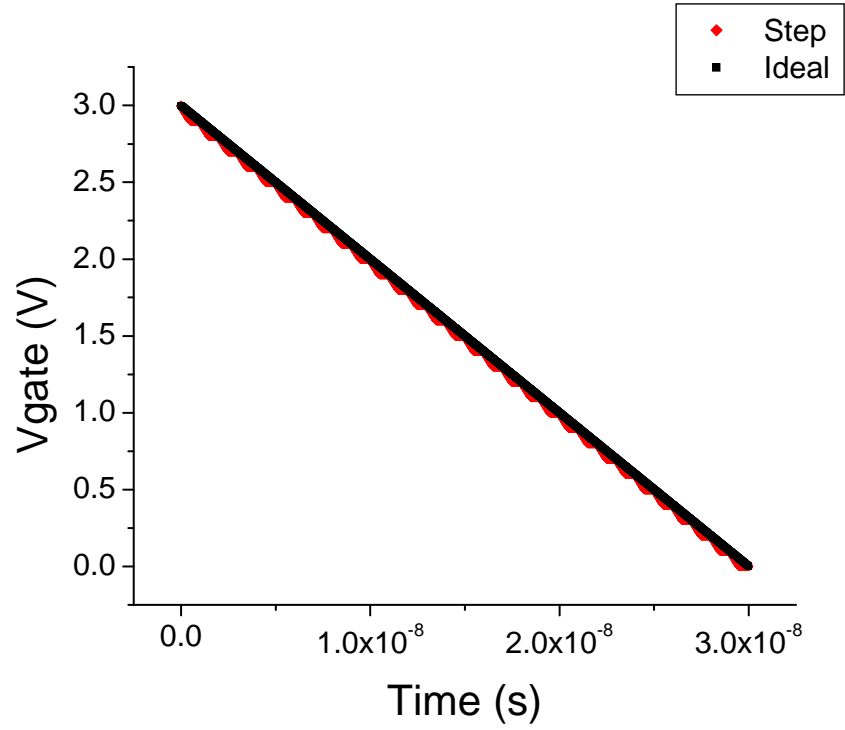
Figure 2.2 Waveform characteristic of the gate voltage used in the model

As shown in Figure 2.2, the Vgate decreases from 3 to 0 V with a fall time of 30 ns and

dt time step of 2 ps. In this model, two types of waveforms are used to turn off the

transistor, an ideal gate ramp and a step approximation. The step waveform is created to

approximate an ideal ramp and help emphasize the voltage recovery due to source-drain

conduction. A closer look at the two waveform types is shown in Figure 2.3.
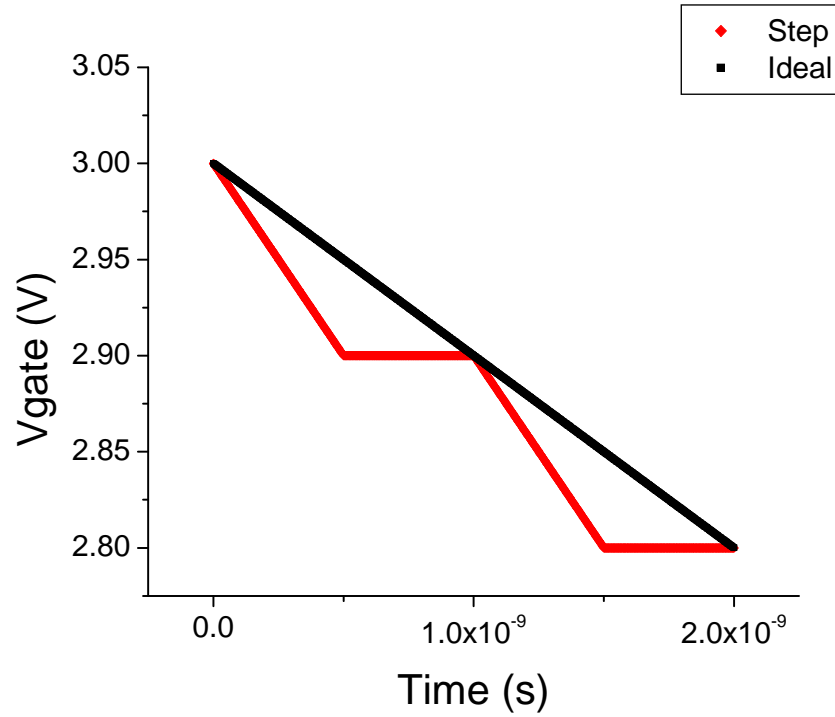
Figure 2.3 A closer look at the two gate waveforms

By using the parameter values and the gate waveform, charge injection, clock feedthrough, and source-drain conduction can be modeled. Charge injection and clock feedthrough are first examined individually and later combined.

2.4.2   Charge Injection

As discussed earlier, charge injection is coupled with source-drain conduction because the dispersal of channel charge introduces a potential difference between source and drain. Using equations (2.3) and (2.7), the error voltage due to charge injection can be written as

$$dV_{CI} = dV_{Qch} - dV_{IDS} \qquad (2.8)$$

or

$$dV_{CI} = \frac{Q_{ch} - 2I_{DS} \cdot dt}{2C_S} \qquad (2.9)$$

By applying the model assumptions to this equation, the behavior of source voltage can

be examined. Figure 2.4 plots Vsource as a function of time for an ideal gate ramp and a

step approximation.
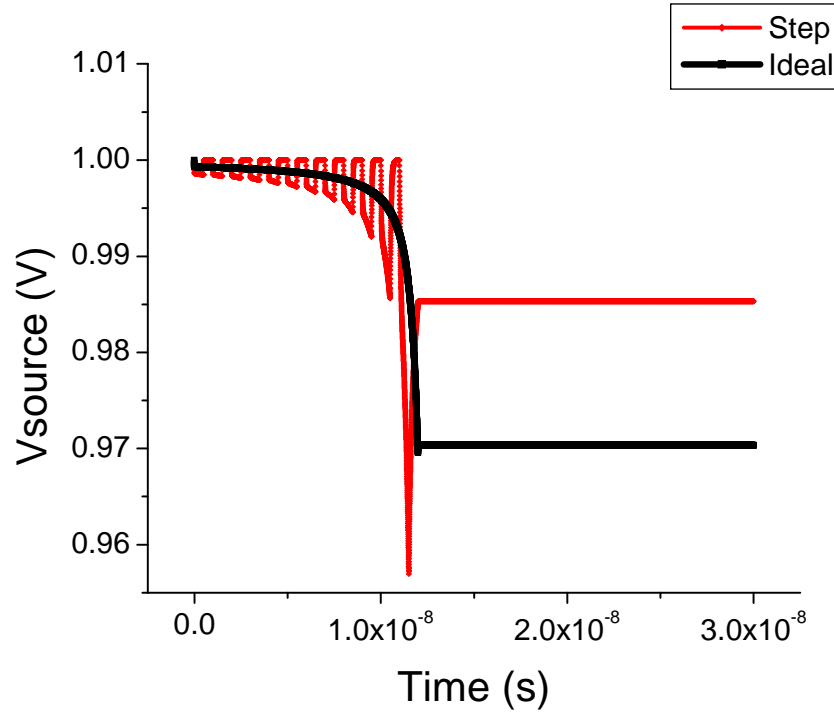
Figure 2.4 Source voltage as a function of time exhibits characteristics of charge injection and source-drain conduction. Parameter values used are from Table 2.1.

The figure describes the behavior of Vsource due to charge injection and source-drain

conduction. Initially when the gate is on, the transistor is in strong inversion and Vsource

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is equal to Vdrain, 1 V. When Vgate begins to decrease, charge injection causes Vsource

to decrease, however source-drain conduction allows for voltage recovery. As Vgate

approaches the threshold condition ($V_G = V_S + V_T$), I_{DS} is not large enough to fully

recover the voltage. Vsource continues to decrease until sub-threshold condition, where

there is not enough channel charge to induce significant error voltage. At this point,

Vsource flattens out and remains constant.

2.4.3 Clock Feedthrough

Clock feedthrough is also coupled with source-drain conduction because the

induced error voltage creates a potential difference between source and drain. Using

equations (2.4) and (2.7), the error voltage due to clock feedthrough can be written as

$$dV_{CF} = dV_{Col} - dV_{IDS} \tag{2.10}$$

or

$$dV_{CF} = \frac{dV_G \cdot C_{GS} \cdot C_S - I_{DS} \cdot dt(C_{GS} + C_S)}{C_S(C_{GS} + C_S)} \tag{2.11}$$

Once again, by applying the model assumptions to this equation, the behavior of source

voltage can be examined. Figure 2.5 displays Vsource as a function of time for the two

types of gate waveforms.
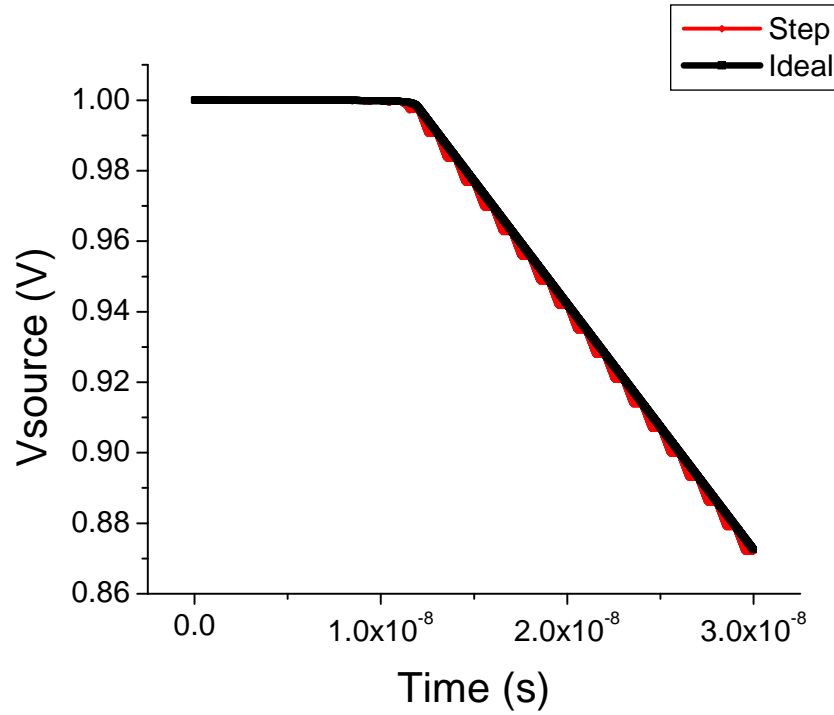
Figure 2.5 Source voltage as a function of time exhibits characteristics of clock feedthrough and source-drain conduction. Parameter values used are from Table 2.1.

The figure illustrates the behavior of Vsource due to clock feedthrough and source-drain conduction. When Vgate is higher than the threshold condition, Vsource is hardly affected by the coupling through overlap capacitance. During this period, the source-drain conduction recovers all of the voltage lost to clock feedthrough. However, once Vgate approaches the threshold condition, I_{DS} is not large enough to recover the voltage. From that point on, Vsource decreases linearly due to the voltage divider.

2.4.4 Combined Effect

After analyzing charge injection and clock feedthrough separately, the two mechanisms are combined to examine the total effect. The charge injection plot in Figure 2.4 is overlaid with the clock feedthrough graph in Figure 2.5 to form the plot shown in Figure 2.6.
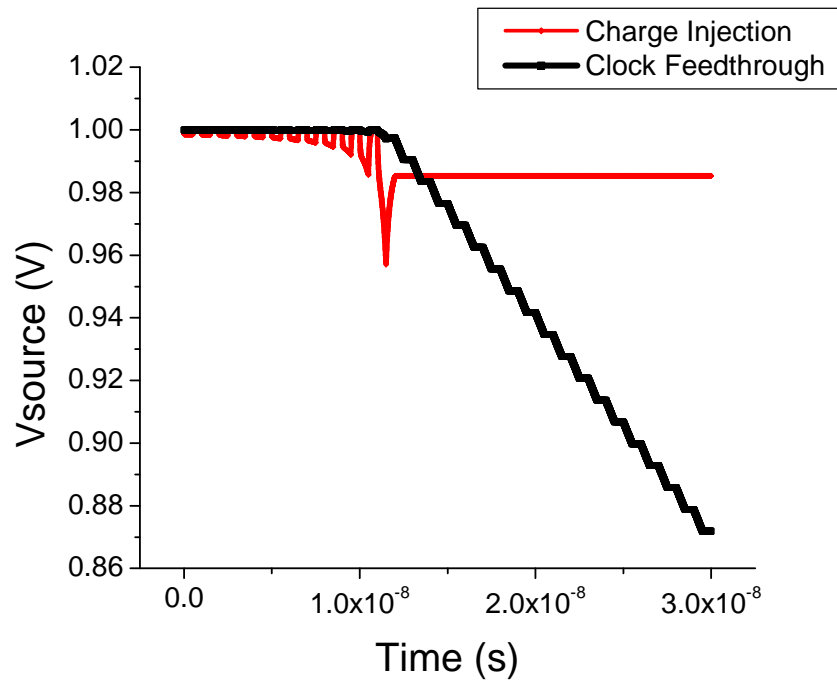
Figure 2.6 Charge injection and clock feedthrough components are overlaid in source voltage versus time plot. Parameter values used are from Table 2.1.

It is shown from the figure that for gate voltages above the threshold condition, charge injection is the main contributor to the error voltage, however in sub-threshold the clock feedthrough component is the main contributor. To model the combined effects of

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charge injection, clock feedthrough, and source-drain conduction, equations (2.3), (2.4), and (2.7) are combined. The error voltage due to the combined effects can be written as

$$dV = dV_{Qch} + dV_{Col} - dV_{IDS} \qquad (2.12)$$

or

$$dV = \frac{Q_{ch}(C_{GS} + C_S) + dV_G \cdot C_{GS} \cdot 2C_S - 2I_{DS} \cdot dt(C_{GS} + C_S)}{2C_S(C_{GS} + C_S)} \qquad (2.13)$$

Using the model assumptions, the behavior of source voltage is calculated and plotted in Figure 2.7. The transient response of Vsource is shown for an ideal gate ramp and a step approximation.
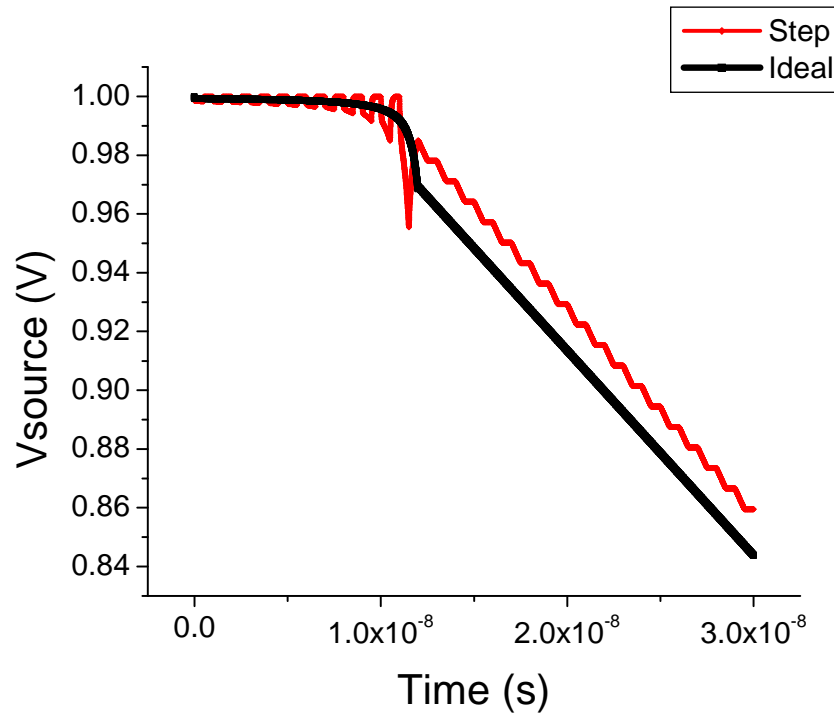
Figure 2.7 Source voltage as a function of time exhibits the combined effects of charge injection, clock feedthrough, and source-drain conduction. Parameter values used are from Table 2.1.

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Figure 2.7 reiterates the predominant interaction between charge injection and source-drain conduction when the gate voltage is above the threshold condition and the dominance of clock feedthrough when the gate is in sub-threshold.

All of the graphs leading up to this point have depicted the transient nature of charge injection and clock feedthrough. There are other important relationships that can be examined from the model data, such as how source voltage changes with gate voltage. In Figure 2.8, the data is re-plotted as Vsource versus Vgate.
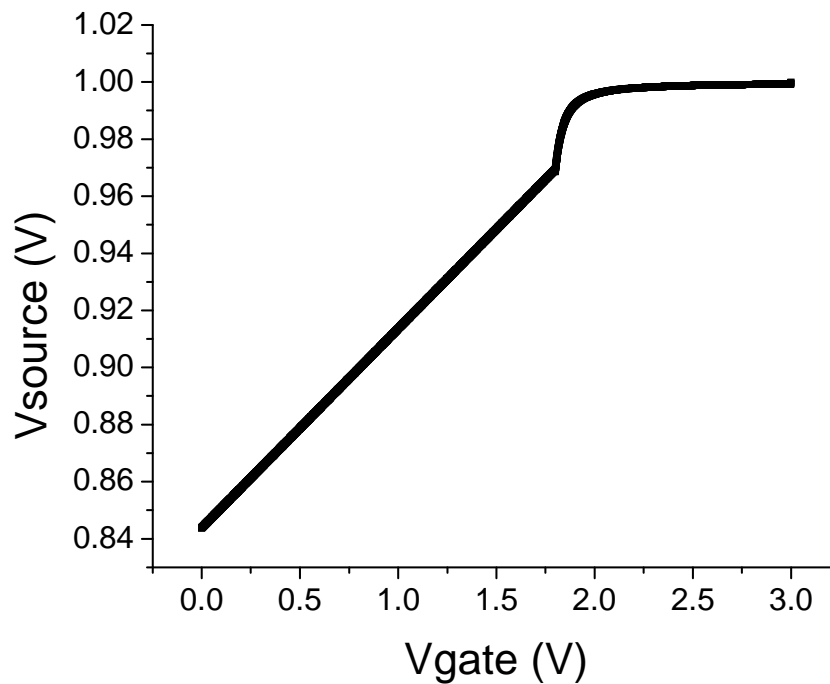
Figure 2.8 Source voltage as a function of gate voltage

The graph illustrates that when charge injection and source-drain conduction dominate, Vsource is dependent on Vgate in a non-linear fashion. This non-linear dependence

exists from 3 to approximately 1.8 V. As Vgate decreases from 1.8 to 0 V, Vsource decreases linearly with Vgate. Vsource decreases linearly due to clock feedthrough, which acts as a voltage divider. The transition point between the non-linear and linear regions is the threshold condition ($V_G = V_S + V_T$). In this case, it is when Vgate is approximately 1.8 V.

The model we developed can be verified and expanded upon by using Technology Computer Aided Design (TCAD) simulations. Not only can TCAD simulations model the distribution of channel charge more accurately, it can predict how charge injection and clock feedthrough are affected by various parameters, such as transistor operation, size, and geometry. The following chapters will discuss TCAD simulation methodology and results.

3 2D Simulation Methodology

This chapter discusses the methodology of 2D charge injection/clock feedthrough simulations using Synopsys [15] TCAD tools. Given present day memory and computer processing power, 2D simulations are relatively fast. Therefore, it is advantageous to explore charge injection/clock feedthrough as much as possible in the two-dimensional space. Parameters that can be examined using 2D simulations include transistor length, gate high level voltage, low level voltage, and fall time. Other effects such as width and explicit three-dimensional structures are examined using 3D simulations, discussed later.

Figure 3.1 illustrates a general TCAD simulation methodology that begins with process simulation and ends with electrical parameter extraction.
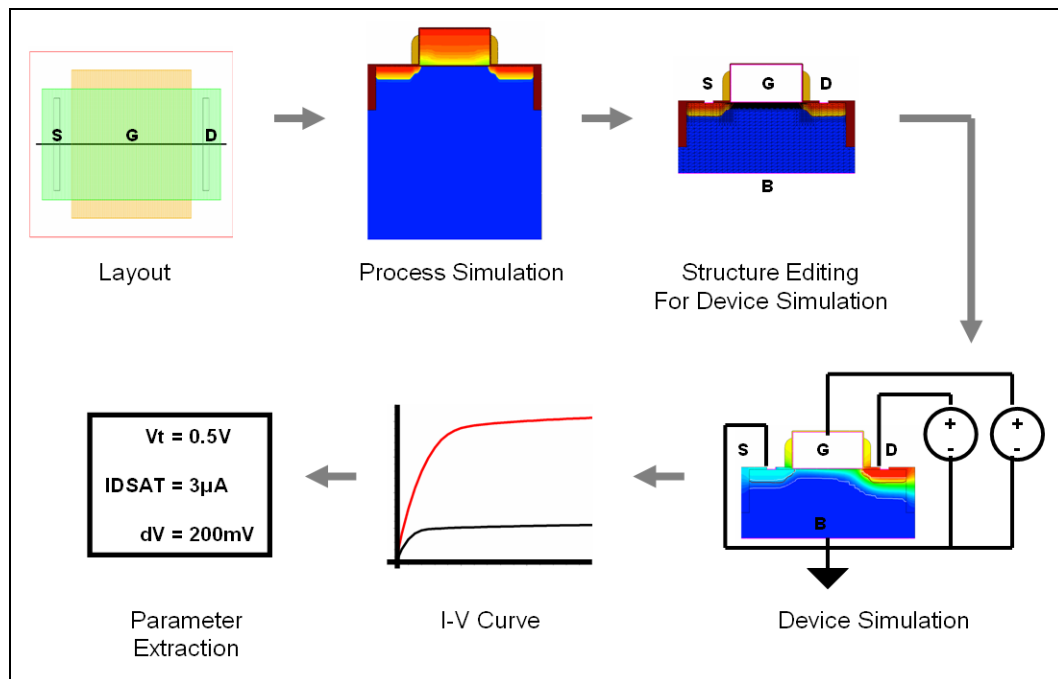
Figure 3.1 TCAD simulation flow begins with process simulation and ends with electrical parameter extraction

The TCAD flow begins with simulating a layout in process simulation to create a structure representing a semiconductor device. The structure is prepared for device simulation by remeshing and adding contacts. After device simulation is complete, the electrical response is captured in plot form. This plot is analyzed to extract electrical parameters. This methodology is implemented into the Synopsys TCAD framework.

3.1   Simulation Setup

This section identifies various Synopsys TCAD tools used to simulate charge injection and clock feedthrough. These tools, which include the process simulator, structure editor, device simulator, and curve plotting utility are integrated into the Sentaurus Workbench as shown in Figure 3.2.

LENGTH	CONTACTS			VG1	VG2		CAP	TFALL	VGH	VGL		Vtgm	dV
1.0um	1	--	--	--	1	2	--	5.81e-15	10e-9	3.0	-0.2	--	0.502	0.056
0.6um	1	--	--	--	1	2	--	5.81e-15	10e-9	3.0	-0.2	--	0.496	0.038
0.4um	1	--	--	--	1	2	--	5.81e-15	10e-9	3.0	-0.2	--	0.479	0.032
0.3um	1	--	--	--	1	2	--	5.81e-15	10e-9	3.0	-0.2	--	0.473	0.028

Figure 3.2 Charge injection/clock feedthrough simulations are setup in Sentaurus Workbench

The tool sequence in the workbench starts with the process simulator, Sentaurus Process, to simulate four transistor lengths: 1.0, 0.6, 0.4, and 0.3 µm. The Sentaurus Structure Editor creates contacts and optimizes the mesh for device simulation. Sentaurus Device runs a series of DC, AC, and transient mixed-mode simulations. The resulting I-V plots are analyzed by Inspect, the curve plotting and extraction tool. By performing the

complete simulation flow within the workbench, each transistor can be fully studied for its charge injection/clock feedthrough characteristics. Similar to the model, the focus of the simulations will pertain to the NMOS transistor.

3.2 Process Simulation

Process simulation creates a semiconductor device representation using modern semiconductor processing methods, such as diffusion, oxidation, etching, deposition, and implantation. Details and complexities of performing process simulation will be discussed in the following sections.

3.2.1 Layout Driven Process Simulation

Layout driven process simulation is an efficient method for creating various structures within one process flow. In order to utilize the tool's layout driven simulation capability, a layout must be provided along with a defined simulation domain. Figure 3.3 is an example of defining a cross section in a layout to be simulated by Sentaurus Process.
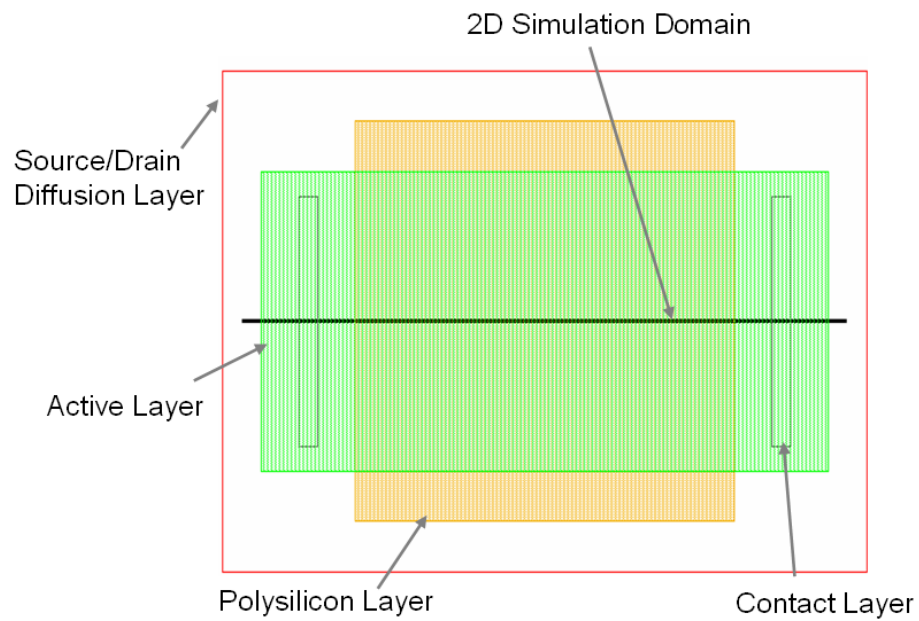
Figure 3.3 Defining the simulation cross section in the NMOS top view

Length is commonly studied for charge injection and clock feedthrough, so various transistor lengths are simulated using 2D process simulations. A parameter LENGTH is specified to the layout to allow for easy creation in Sentaurus Process. Figure 3.4 shows the transistors simulated with different channel lengths.
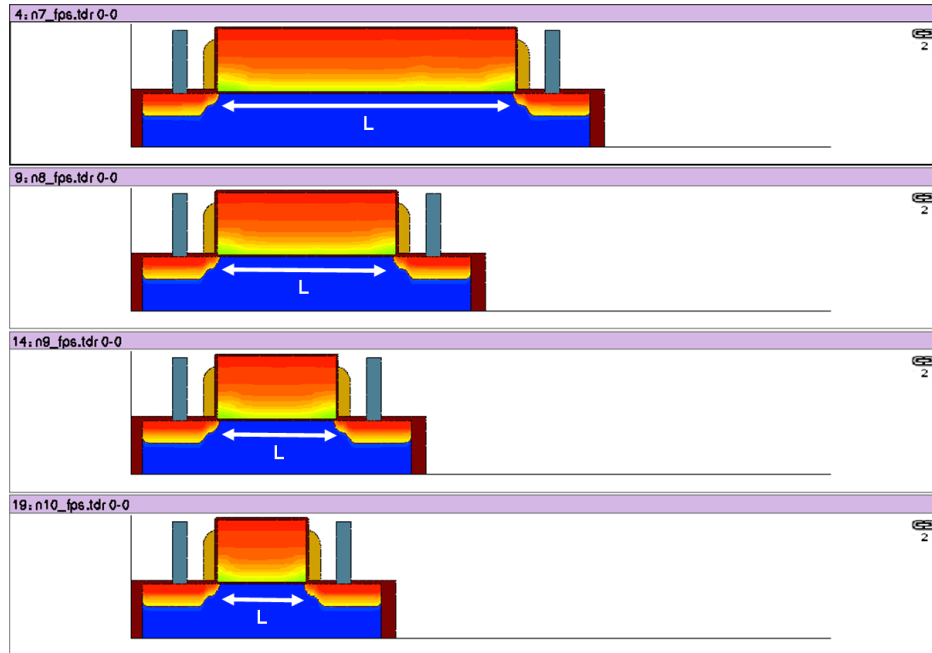
Figure 3.4 2D process simulations create NMOS transistors with various lengths to study charge injection and clock feedthrough

3.2.2 Models for Calibration

One of the challenges in process simulation is to reproduce an accurate representation of the semiconductor device. Models for a given technology are specified in the process simulator to ensure accurate results. This involves proper selection of diffusion models, implantation models, and boundary conditions.

For example, it is important to choose the point defect assisted dopant diffusion model when an anneal immediately follows an ion implantation step with a moderate dose [16]. When implantation models are selected, both analytic and Monte Carlo [17] models are considered. Analytic implantation is chosen over Monte Carlo implantation to reduce process simulation time. Finally, the segregation of dopants at interfaces is considered to accurately define a device's threshold. In later sections, I-V curves are compared to determine how well the process simulation is calibrated.

3.2.3 Meshing

TCAD simulators are based on finite element solutions to solve the non-linear partial differential equations. Therefore, good meshing techniques are required to perform numerically stable and accurate simulations. Optimum meshing is important to maintain accuracy without dramatically increasing process simulation time.

In a transistor, an initial mesh is defined by specifying the spacing in the vertical direction. Additional mesh refinements are necessary in critical areas of the device, such as the channel, source, drain, and lightly doped drain (LDD) regions. This technique is illustrated in Figure 3.5.
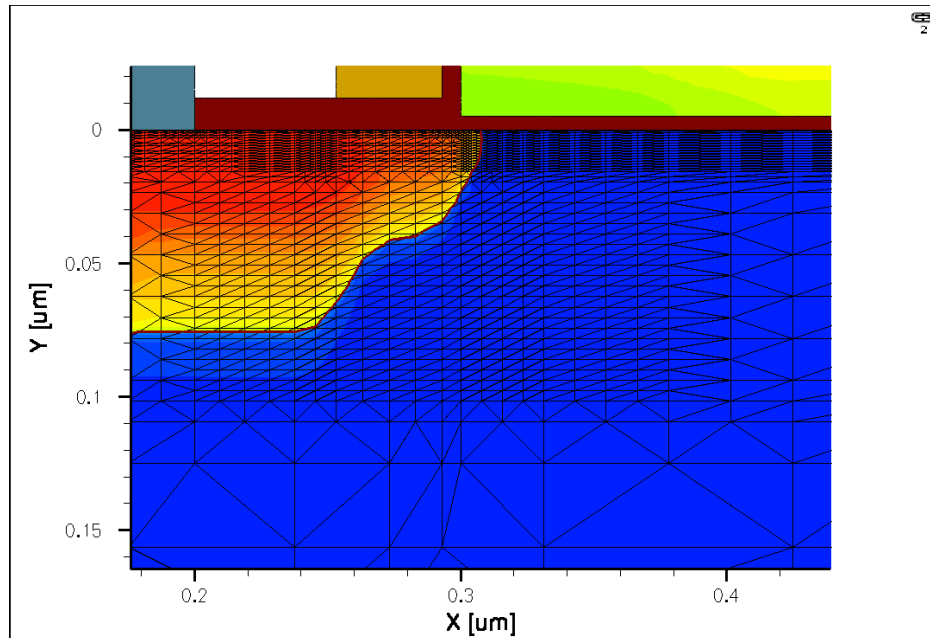
Figure 3.5 Mesh requirements are defined differently for different areas of the device. An initial vertical spacing is specified followed by denser mesh specifications in the channel, source, drain, and LDD regions.

3.2.4 Process Flow

Table (3.1) shows the process sequence in a typical deep-submicron CMOS process flow. Details such as thermal budget or the combination of species, doses, and energies for implantation are the intellectual property of each manufacturing company and differs from the process flow described here. However, the resulting doping profiles from simulations and actual silicon match.

Table 3.1 Simulated 0.18 μm CMOS process flow.

No.	Name	Description	Value	Unit
1	Active definition	Etch silicon using ACTIVE mask	0.25	μm
2	STI fill	Deposit oxide	0.25	μm
3	Vt adjust implant 1	Implant boron using 5keV energy	4.5×10^{12}	cm^{-2}
4	Vt adjust implant 2	Implant boron using 20keV energy	5.0×10^{11}	cm^{-2}
5	Field implant 1	Implant boron using 85keV energy	1.6×10^{13}	cm^{-2}
6	Field implant 2	Implant boron using 260keV energy	2.0×10^{13}	cm^{-2}
7	Gate oxide	Oxidation to grow 50 Å	90	min
			1000	°C
8	Polysilicon deposition	Deposit polysilicon	0.21	μm
9	Gate etch	Etch polysilicon using POLY mask	0.35	μm
10	Polysilicon reoxidation	Oxidation to grow 70 Å	8	min
			900	°C
11	LDD implant	Implant arsenic using 15keV energy	1.0×10^{14}	cm^{-2}
12	Anneal	Diffusion	10	sec
			1000	°C
13	Spacer deposition	Deposit nitride	0.04	μm
14	Spacer etch	Etch nitride	0.08	μm
15	Source/Drain implant	Implant arsenic using 25keV energy	1.0×10^{15}	cm^{-2}
16	Source/Drain RTA	Diffusion	10	sec
			1000	°C

The key steps in the process flow are shallow trench isolation (STI) formation followed

by well implantation to set a threshold voltage of 0.5 V. After 50 Å of gate oxide is

grown, polysilicon deposition and etch occur to form the transistor's gate. LDD

implantation is self aligned to the gate to reduce electric field, followed by nitride

deposition to form the sidewall spacer. After source/drain implantation, the damage is

annealed using rapid thermal anneal (RTA). Figure 3.6 shows the final structure after the

process simulation has completed. A vertical cut line in the center of the transistor's

channel displays the boron doping profile shown in Figure 3.7.
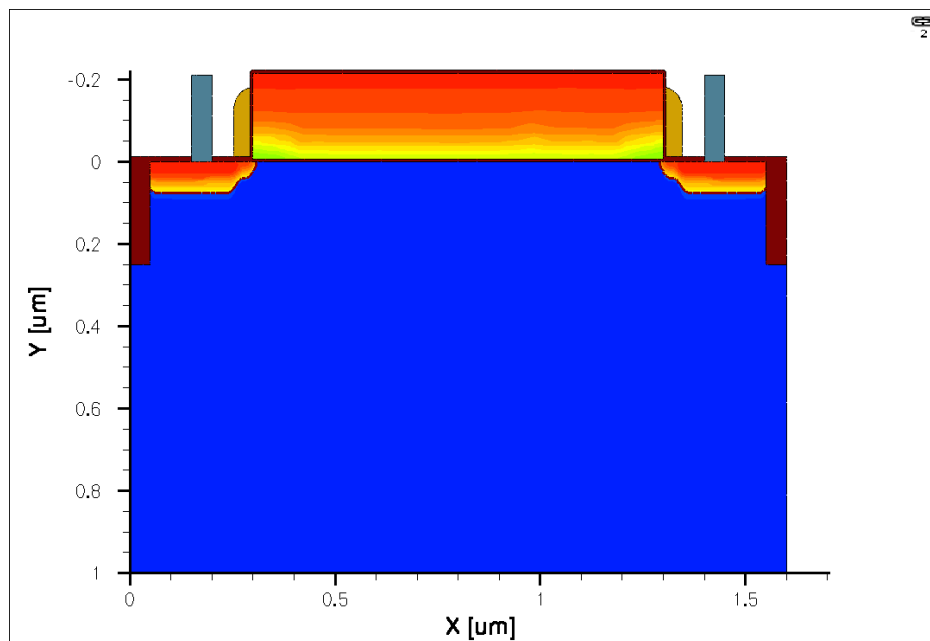
Figure 3.6 2D process simulation generates a full cross section of an NMOS transistor
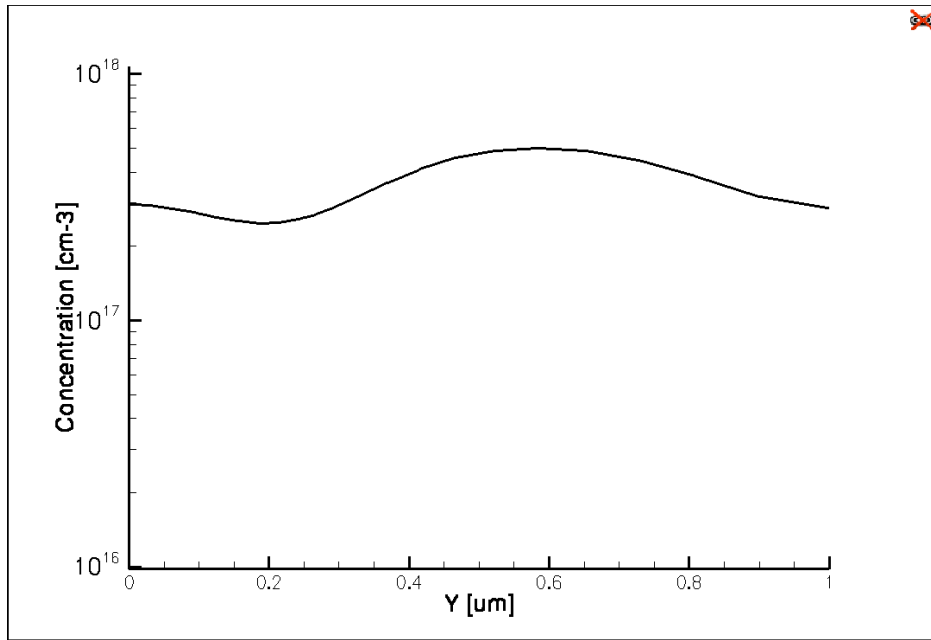
Figure 3.7 Boron doping profile in the center of the NMOS transistor. Left to right corresponds to top to bottom depth in Figure 3.6.

3.3   Structure Editing

In order to prepare a structure for device simulation, structure editing is performed using Sentaurus Structure Editor. The NMOS structure from process simulation is reduced in size by removing the lower portion of the substrate. Next, contacts are placed for the substrate, gate, source, and drain. After contact placement, the structure is ready to be remeshed

Since mesh requirements are different for process and device simulations, the structure editor is also utilized to remesh the structure prior to device simulation. Optimum mesh is important to resolve key regions of the transistor pertaining to charge injection and clock feedthrough; these areas include the inversion layer and overlap regions. To properly resolve the inversion layer, mesh in the gate oxide is 10 Å, followed

by a fine mesh in the first 300 Å of the channel. In the channel's first 10 Å the mesh

spacing is 2 Å, and as the channel depth increases to 300 Å the mesh spacing increases to

20 Å. The source and drain are remeshed to complete the NMOS device.

3.4   Device Simulation and Electrical Parameter Extraction

In order to fully understand the electrical response of a semiconductor device,

different device simulations are performed. Sentaurus Device is used to perform DC,

AC, and transient mixed-mode simulations. DC simulations provide I_D-V_G and I_D-V_D

curves, AC analysis generates C-V characteristics, and transient mixed-mode simulations

model charge injection/clock feedthrough. The resulting I-V plots are analyzed by

Inspect to extract electrical parameters. In the following sections, the models and math

parameter selections will be discussed for each of the device simulations.

3.4.1 I_D-V_G Simulation

Sentaurus Device simulates I_D-V_G to examine drain current as a function of gate

voltage for low drain bias. Knowing the threshold voltage is important in studying

charge injection and clock feedthrough. Standard device models [18] are selected to

simulate the DC nature of the transistor. The property of the n+ polysilicon gate is

specified with a work function difference of -0.55 eV. The Philips unified mobility

model [19], velocity saturation within high field regions [20], and degradation due to

surface roughness scattering are all activated to model mobility in silicon. Carrier

recombination in silicon is specified using Shockley-Read-Hall recombination with

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doping dependent lifetime [21]. Charge at the Si-SiO$_2$ interface is defined to have a

concentration of 2.0 x 10^{10} cm^{-3}.

The drain is first ramped to 250 mV and the gate is swept from 0 to 3 V; substrate

and source are both grounded. Since the simulations pertain to NMOS transistors, only

electron continuity and Poisson's equations are solved. Figure 3.8 shows the resulting I$_D$-

V$_G$ characteristics simulated in Sentaurus Device.
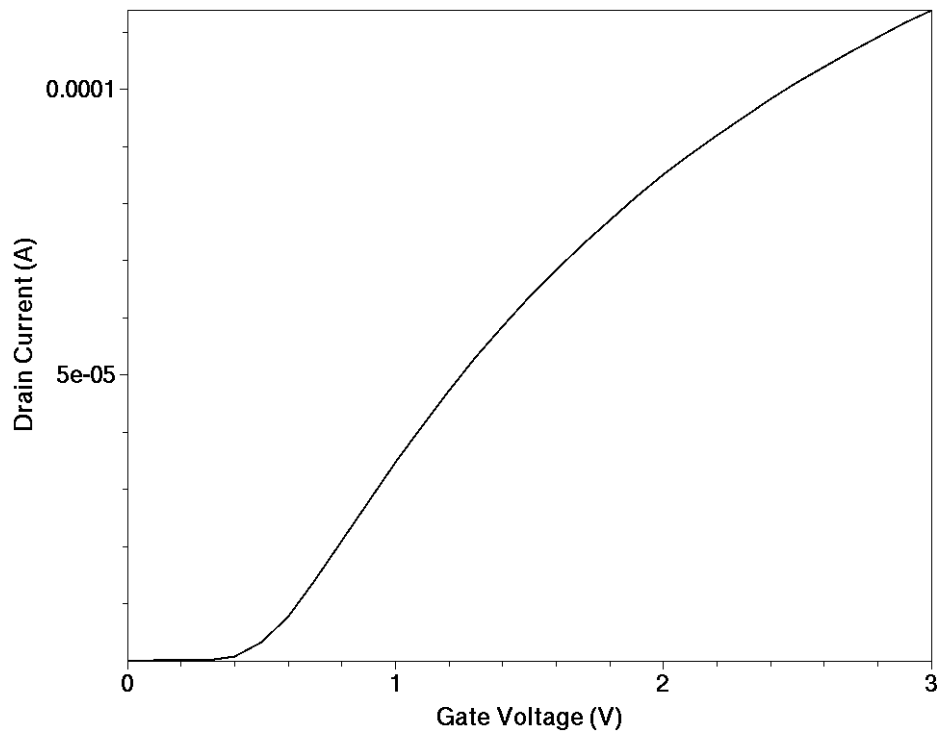
Figure 3.8 Sentaurus Device simulates drain current as a function of gate voltage for a 1.0 μm long NMOS created using the process flow from Table 3.1

As discussed in section 3.1, the workbench tool sequence is designed so that

Inspect follows the Sentaurus Device instance that simulates I$_D$-V$_G$. This allows Inspect

to load the I-V plot resulting from Sentaurus Device and extract threshold voltage.

Test structures fabricated in a 0.18 µm CMOS process are measured to verify threshold voltage. Figure 3.9 compares the simulated I_D-V_G characteristic against measurements of an NMOS transistor with W/L = 1.0 µm/1.0 µm. As shown in the plot, simulations have higher drain current than measurements. One possible source of the discrepancy can be attributed to contact resistance, which exists in the measurements.
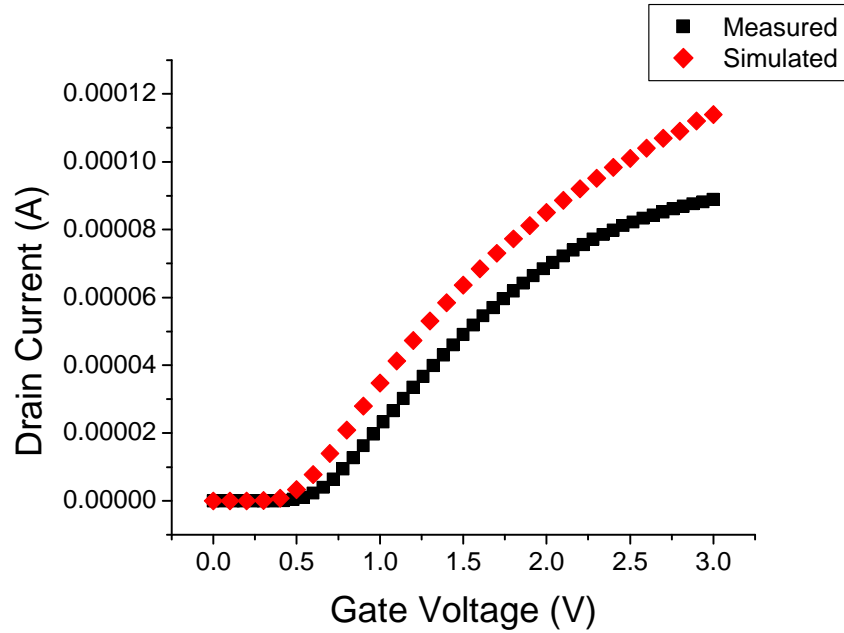
Figure 3.9 Comparing I_D-V_G between simulation and measurement of an NMOS transistor with W/L = 1.0 µm/1.0 µm

3.4.2 I_D-V_D Simulation

Sentaurus Device also simulates I_D-V_D to examine family of curve characteristics and saturation current. This DC simulation uses the exact set of properties, models, and mathematical solvers as the I_D-V_G simulation discussed in section 3.4.1. Sentaurus

Device simulates I_D-V_D for two gate biases, 1 and 2 V. The gate is first ramped to the

particular voltage and the drain is swept from 0 to 3 V; substrate and source are both

grounded. The resulting I_D-V_D curves are shown in Figure 3.10.
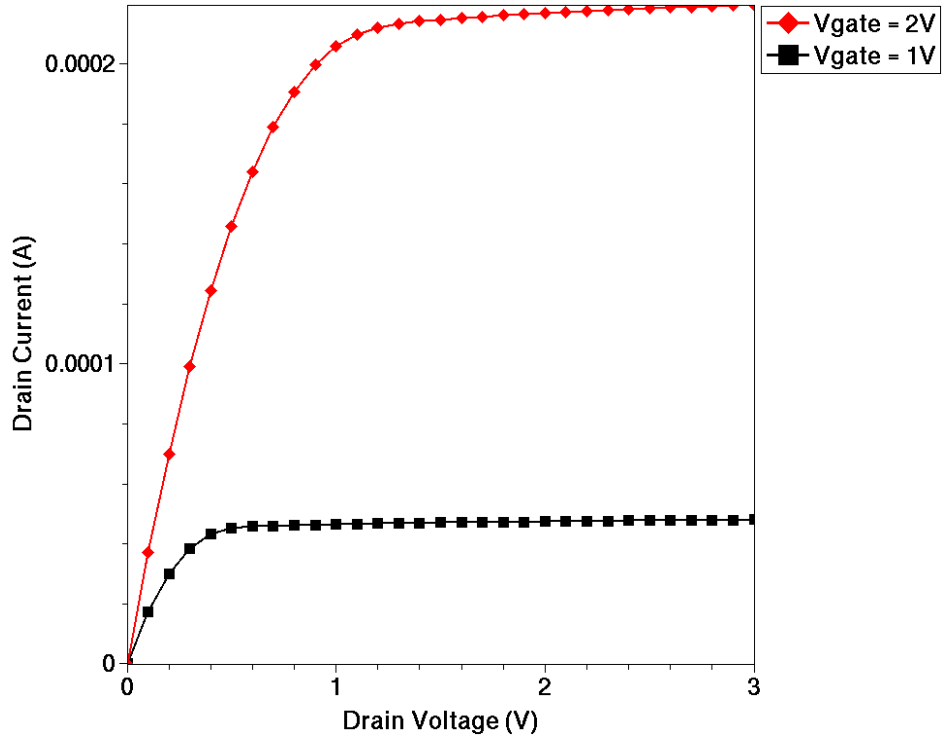
Figure 3.10 Sentaurus Device simulates drain current as a function of drain voltage for gate biases of 1 and 2 V

The test structures are measured to compare against simulations. Figure 3.11

compares the simulated and measured I_D-V_D characteristic when the gate bias is 2 V.

The plot shows good agreement between simulations and measurements. The higher

drain current seen in simulations can once again be attributed to contact resistance, which

exists in the measurements.
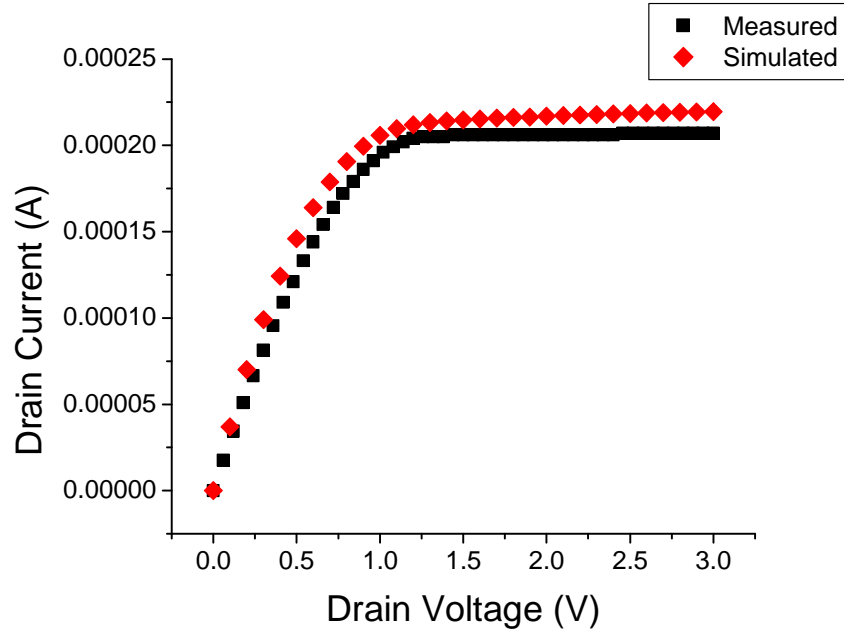
Figure 3.11 Comparison of simulated and measured I_D-V_D curves when the gate bias is 2 V. The NMOS transistor used for this comparison has W/L = 1.0 μm/1.0 μm.

3.4.3 Small-signal AC Analysis

Small-signal AC analysis is performed to simulate C-V characteristics and

estimate source capacitance. Knowing the various components of the source capacitance

is necessary to further analyze clock feedthrough. In small-signal AC analysis, the

device simulation computes small current change due to small change in voltage.

Capacitances in the transistor are extracted using the mixed-mode simulation

environment in Sentaurus Device.

The small-signal AC simulation uses the same set of properties and models as the

I_D-V_G simulation discussed in section 3.4.1. An area factor of 0.4 is specified to scale the

transistor width to 0.4 μm and the current accordingly. While the substrate and drain are

both grounded, the gate is ramped to -1 V prior to the C-V sweep. This accumulates

holes to the Si-SiO$_2$ interface and prevents channel electrons from contributing to the

capacitance. Small-signal AC analysis is activated while the source is swept from 0 to 1

V. The AC simulation is performed only for a single frequency of 1 MHz. The curve

shown in Figure 3.12 shows the C-V characteristics for gate-source overlap and total
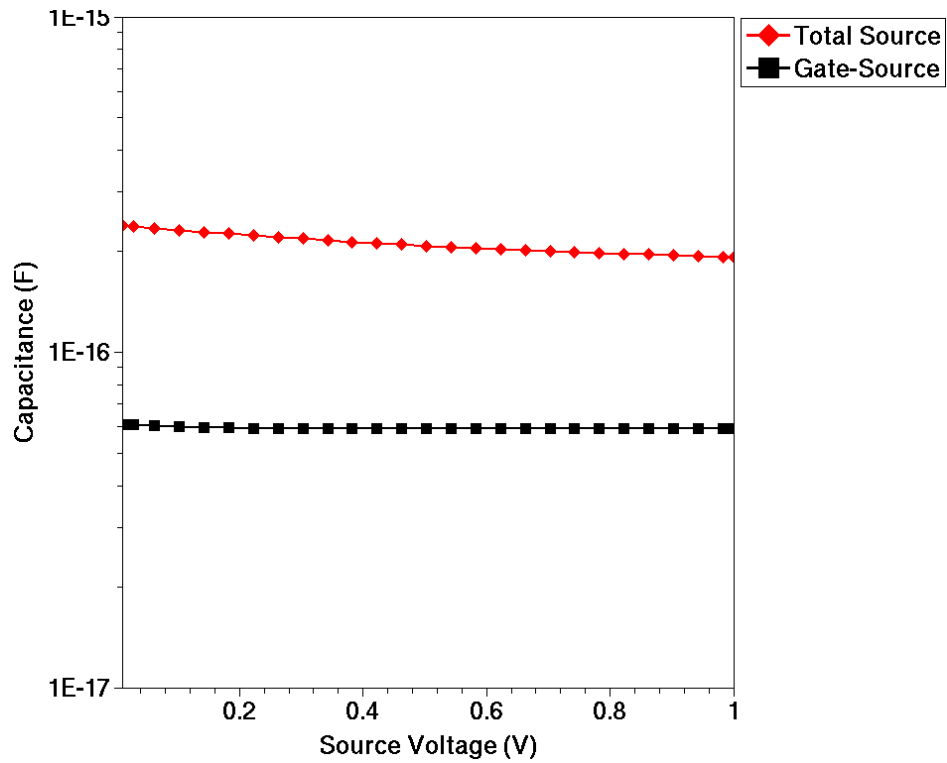
source.

Figure 3.12 Gate-source and total source capacitances as a function of source voltage

3.4.4   Charge Injection/Clock Feedthrough Simulation

This section describes the use of transient mixed-mode simulations to model

charge injection/clock feedthrough in a switched-capacitor circuit. Mixed-mode

simulation is similar to SPICE [22], an industry standard circuit simulator – it has the

capability to simulate small circuits with multiple elements, such as physical devices and

lumped components. Setting up a mixed-mode simulation in Sentaurus Device requires

defining individual elements in the circuit and a netlist connecting the devices [18]. The

netlist describes the switched-capacitor circuit shown in Figure 3.13, which includes two

voltage sources, a lumped capacitor, and an NMOS transistor. The NMOS transistor is a

physical device that derives from process simulation, while the voltage sources and

capacitor are compact model devices. The NMOS source is connected to a capacitor

totaling 6 fF, the drain is connected to a DC voltage source, and the gate is connected to a

time dependent voltage pulse.
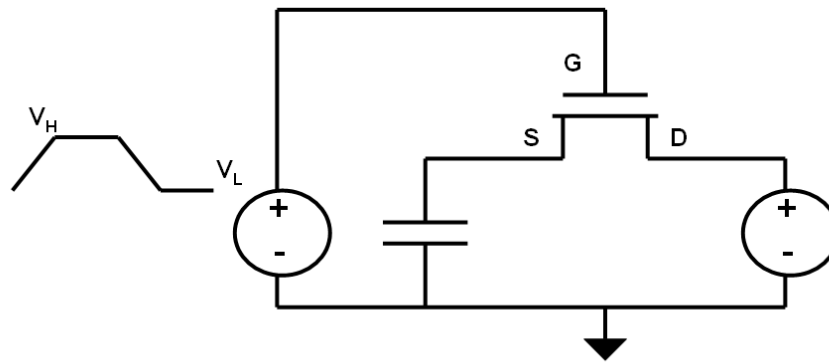
Figure 3.13 Circuit diagram to simulate charge injection using Sentaurus Device mixed-mode

The mixed-mode simulation uses the same set of properties and models as the I_D-

V_G simulation discussed in section 3.4.1. An area factor of 0.4 is specified to scale the

transistor width to 0.4 μm.

The device simulation begins ramping the drain to 1 V while the substrate is grounded. Using transient simulation, the gate is ramped from 0 to 3 V with a rise time of 10 ns, held high for 10 ns, and ramped down to -200 mV with a fall time that is specified by the TFALL parameter in the workbench. Electron continuity and Poisson's equations are solved for the device during this simulation. Figure 3.14 shows the resulting transient characteristic of the NMOS transistor.
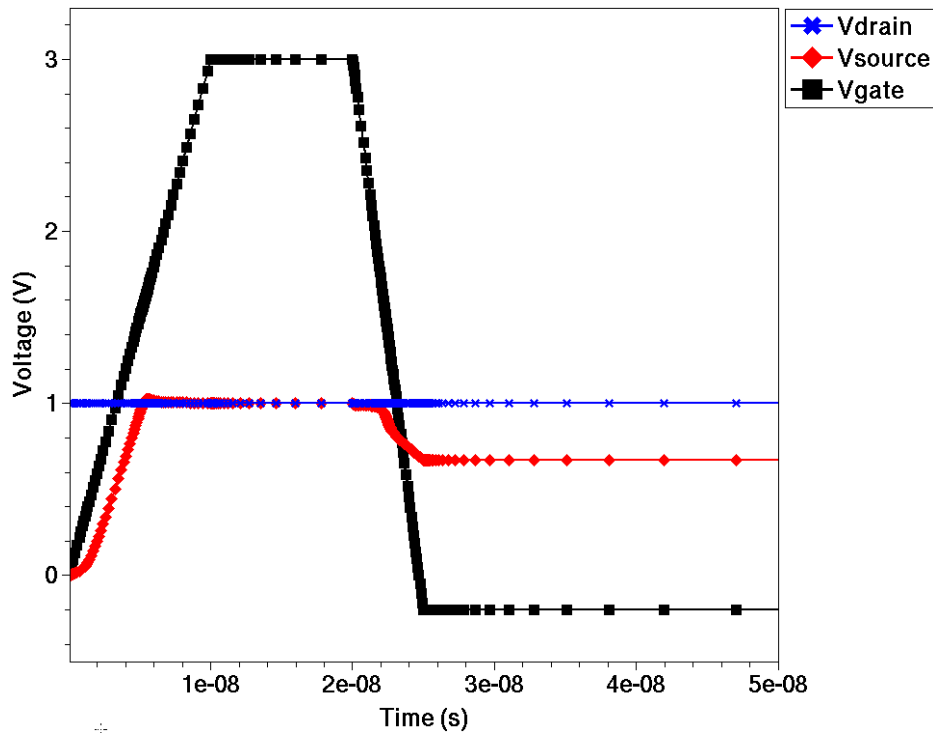
Figure 3.14 Transient characteristic of the source and drain as the gate turns on and off

Initially, when the gate is off, there is a difference between Vsource and Vdrain because the source is connected to a capacitor, while the drain is connected to a voltage source. When the gate is on, the transistor is in strong inversion and the source increases to the same voltage as the drain, 1 V. When the gate turns off, the combined effects of

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charge injection and clock feedthrough decrease Vsource, as discussed in Chapter 2. The

difference in Vsource from when the gate is on to off is defined as the error voltage, dV.

For the example shown in Figure 3.14, dV would be approximately 400 mV.

4 3D Simulation Methodology

This chapter discusses the methodology used to generate 3D structures to simulate charge injection and clock feedthrough. Given present day memory and computer processing power, 2D simulation is fast and used as much as possible. However, when it is necessary to capture effects in the third dimension, 3D simulation is utilized. Effects such as width and explicit three-dimensional structures are studied for charge injection and clock feedthrough.

Discussion of 3D simulation methodology focuses primarily on the setup of process simulation and the structure editor. Device simulation is nearly identical to the 2D setup and will be covered briefly.

4.1   Simulation Setup

The setup of 3D simulations is based off 2D simulations. For example, process flow, calibration models, and device simulations are nearly identical in 2D and 3D simulations. The main difference in 3D simulations is how the structure is created from process simulation. Challenges with 3D process simulation involve the meshing complexities with moving boundaries [23]. Therefore, present day 3D process simulators cannot stably perform the full processing steps that 2D simulators can. The Synopsys TCAD tools perform 3D process simulation by dividing the tasks between Sentaurus Process and Sentaurus Structure Editor [16]. During process simulation, Sentaurus Process performs all implantation and diffusion steps, and internally calls upon Sentaurus Structure Editor to perform etching and deposition.

The tool sequence for 3D charge injection simulation is similar to the 2D flow discussed in section 3.1. Figure 4.1 shows a portion of the Sentaurus Workbench used for 3D charge injection/clock feedthrough simulations.

	Type	TYPE	CONTACTS		WIDTH
					0.3um
					0.4um
		standard	1	--	0.6um
--	nMOS				1.0um
		annular	1	--	1.0um
		funnel	1	--	1.0um

Figure 4.1 Charge injection/clock feedthrough simulations are setup in Sentaurus Workbench

As shown in the figure, the tool sequence starts with Sentaurus Process to perform

process simulations for three different types of NMOS transistors: standard, annular, and

funnel-shaped. Sentaurus Structure Editor performs additional post processing to prepare

the structure for device simulation. The remaining portion of the tool flow is identical to

the 2D setup and is not shown in the figure. Sentaurus Device is utilized to perform a

series of DC, AC, and transient mixed-mode simulations and the resulting I-V plots are

analyzed by Inspect.

4.2   Standard Transistor Simulation

3D simulation is utilized to simulate the standard transistor with various widths.

In order to reduce simulation time, Sentaurus Process simulates one-quarter of the

transistor and Sentaurus Structure Editor performs resizing and reflection to form the full

transistor.

4.2.1 Process Simulation

Simulation of the standard NMOS begins by defining the 3D region to be

simulated by Sentaurus Process, as shown in Figure 4.2. By taking advantage of the

standard NMOS symmetry, only the gate and drain portions are simulated in 3D process

to save computational resources. The resulting structure is later reflected in Sentaurus

Structure Editor to form the full NMOS structure.
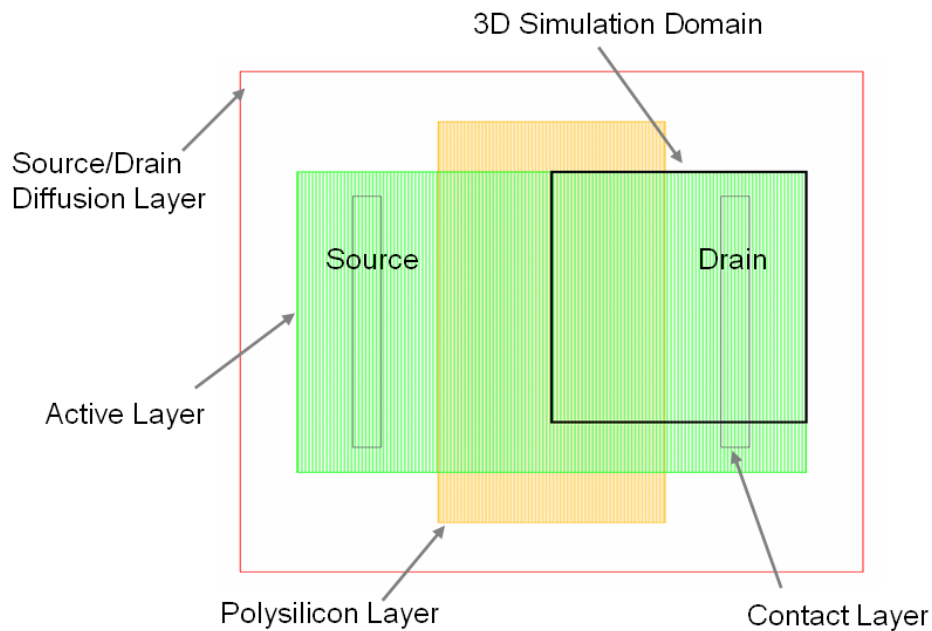
Figure 4.2 Defining the 3D process simulation domain in the standard NMOS top view

Width is commonly studied for charge injection/clock feedthrough, so various

transistor widths are analyzed. As shown in Table (4.1), transistors with 0.4 μm length

and widths ranging from 0.3 to 1.0 μm are examined. These different widths are

considered when the simulation domain is defined in the layout. Since 3D process

simulation is time consuming, only the largest transistor is simulated using process

simulation.

Table 4.1 Transistor sizes to examine the effect of width on charge injection/clock feedthrough.

Length (μm)	Width (μm)	Simulated using Sentaurus Process
0.4	0.3	No
0.4	0.4	No
0.4	0.6	No
0.4	1.0	Yes

As described in the table, Sentaurus Process simulates only the transistor with W/L = 1.0 μm/0.4 μm. One-quarter of this structure is generated, as shown in Figure 4.3. This structure will be reused in the structure editor to create transistors with smaller widths. This is discussed in further detail in the next section.
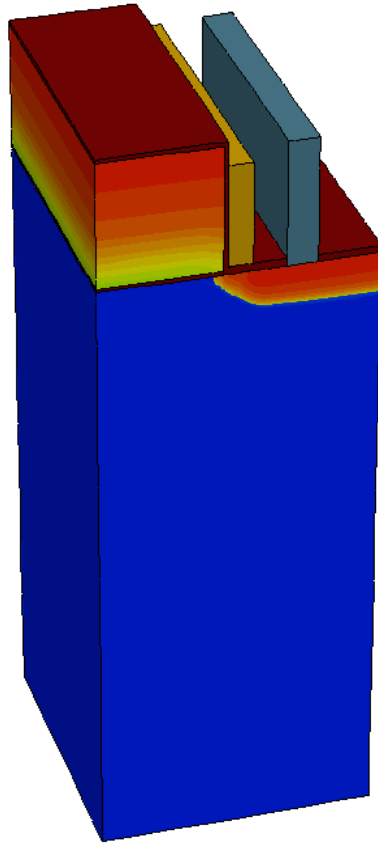
Figure 4.3 3D process simulation generates one-quarter of the widest transistor discussed in Table 4.1. This structure is created using the process flow from Table 3.1.

Meshing for 3D process simulation is similar to the 2D case. Meshing in the vertical direction begins with a fine mesh at the Si-SiO$_2$ interface and increases as depth increases. Mesh refinement boxes are specified for the transistor channel, source, drain, and LDD.

Mesh verification can be cumbersome because a 3D process simulation often takes hours to complete. To verify that the static mesh is acceptable without waiting for the entire simulation to complete, intermediate structure saves are utilized. Figure 4.4 shows the transistor saved after polysilicon gate formation. The saved structure reveals that the mesh refinement boxes are placed in the correct location and the mesh density is acceptable. The general mesh is coarse in order to reduce 3D process simulation time, however there is fine meshing in the channel, source, drain, and junction area.
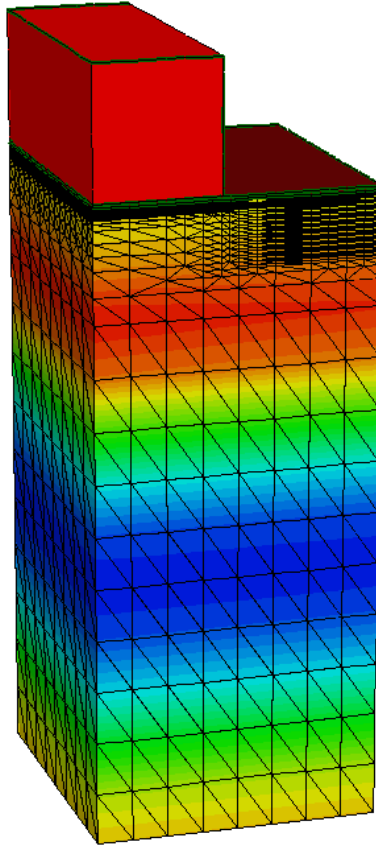
Figure 4.4 Meshing after polysilicon gate formation. The general mesh is coarse to reduce 3D process simulation time, but denser meshes are specified in the channel, source, drain, and junction regions.

The 3D process simulation uses the same process flow discussed in section 3.2.4.

Although the process flow is the same, some adjustments are made to reduce simulation

time. As shown in Figure 4.2, the simulation domain does not include the STI. STI is

omitted because it requires further mesh refinement at the interface and does not affect

charge injection/clock feedthrough.

4.2.2   Structure Editing

As discussed in section 4.2.1, to reduce simulation time only one structure is simulated in process simulation and the transistor width variants are created using the structure editor. Sentaurus Process takes the widest transistor, which has a width of 1.0 μm and length of 0.4 μm, and simulates one-quarter of it. This results in a structure that has a width of 0.5 μm and length of 0.2 μm. Since it is the largest transistor, all of the width variants can be derived from it. Table (4.2) specifies the resizing that is performed in Sentaurus Structure Editor to create the remaining widths.

Table 4.2 The structure editor resizes the largest transistor to create smaller width variants.

Initial W/L from process simulation (μm/μm)	Width resizing using the structure editor (μm)	Final W/L after reflection (μm/μm)
0.5/0.2	-0.35	0.3/0.4
	-0.30	0.4/0.4
	-0.20	0.6/0.4
	0	1.0/0.4

After the structure is resized, it is reflected across the width and length boundaries to create the full transistor.

Similar to the 2D methodology, Sentaurus Structure Editor performs post processing to prepare for device simulation. The size of the structure is reduced in the vertical direction by removing the lower portion of the substrate. After contacts are placed for the substrate, gate, source, and drain, the structure is remeshed.

4.2.3   Device Simulation

3D device simulations are similar to 2D simulations discussed in section 3.4, and the slight changes are in the AC and transient mixed-mode simulations. For 3D, both AC and transient mixed-mode simulations do not need to specify area factor because width is already accounted for. For 3D AC simulation, different mathematical solvers are used. The Block and ILS solvers [18] are specified to reduce AC device simulation time.

Since the 3D simulations are utilized to examine transistors with various widths and geometries, the source capacitances will be different. The AC simulations simulate the C-V characteristics for all these transistors and extract source capacitance. As alluded to in Chapter 2, since charge injection and clock feedthrough are dependent on overlap and total source capacitances, it is important to know the capacitances for each transistor. By knowing these capacitances, the lumped capacitor in the mixed-mode transient simulations can be adjusted accordingly so that charge injection/clock feedthrough comparison for the different transistors is fair.

4.3   Annular Transistor Simulation

To further investigate layout effects on charge injection, the annular transistor is explored. As shown in Figure 4.5, the annular transistor has a gate that is shaped like a ring. The source is self aligned to the inside of the ring, while the drain is formed on the outside of the ring. Due to this configuration, the gate-drain overlap capacitance is larger than the gate-source overlap capacitance.
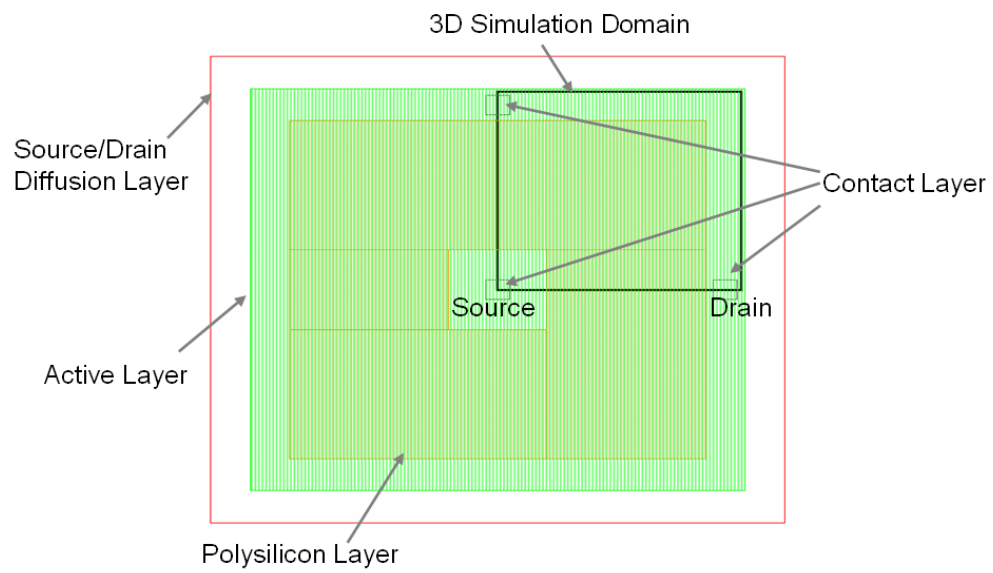
Figure 4.5 Defining the 3D process simulation domain in the annular top view

Similar to the standard NMOS, a simulation methodology is used to take

advantage of the annular transistor's symmetry. To reduce simulation time, Sentaurus

Process simulates only one-quarter of the transistor, which is shown in Figure 4.6.
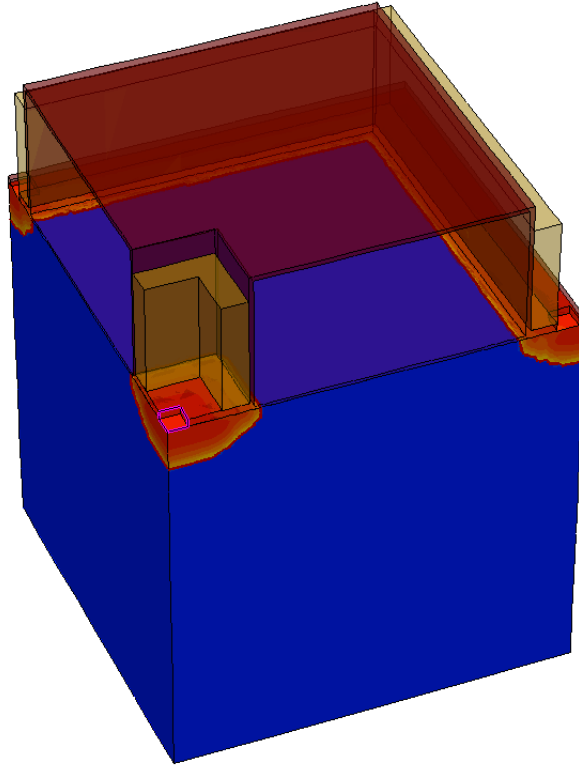
Figure 4.6 Sentaurus Process simulates one-quarter of the annular transistor. The nitride spacer and polysilicon gate are translucent for easier viewing.

The structure shown in Figure 4.6 corresponds to the simulation domain defined in Figure

4.5. The source is the n-type region in the inner portion of ring, while the drain is the n-

type diffusion on the outside of the ring. Meshing involves mesh definition for the small

source region and the drain region that is located around the perimeter of the transistor.

A fine mesh is specified for the channel, which is in the shape of a ring. After Sentaurus

Process generates one-quarter of the transistor, Sentaurus Structure Editor is used to

perform post processing for device simulation. During the post processing, the structure

is reflected across the width and length boundaries to form the entire annular transistor

shown in Figure 4.7.
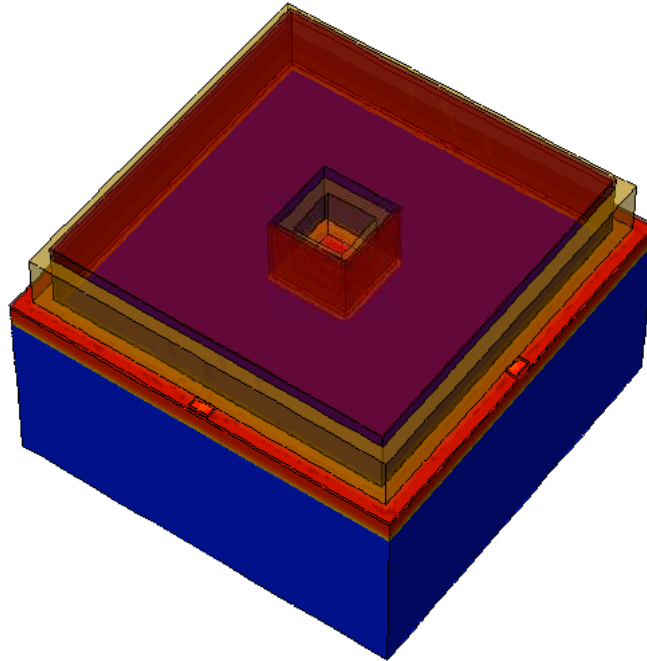
Figure 4.7 The full annular transistor structure after reflection in Sentaurus Structure Editor. The nitride spacer and polysilicon gate are translucent for easier viewing.

Figure 4.8 shows the source and drain diffusion regions in the annular transistor. A 2D

plane is positioned to show the center of the transistor.

Figure 4.8 The source and drain diffusion regions in the annular transistor. The nitride spacer, polysilicon gate, and oxide are not shown for easier viewing.

4.4 Funnel-shaped Transistor

The funnel-shaped transistor is simulated using 3D simulations to understand charge injection/clock feedthrough in an asymmetric transistor. A funnel-shaped transistor possesses a channel that is shaped like a funnel [24]. As shown in Figure 4.9, the funnel-shaped transistor resembles a standard self-aligned transistor with an active region that is graded across the channel. This funnel-shaped active region defines the source/drain and creates different widths on the source and drain side. Because of this, the gate-drain overlap capacitance is larger than the gate-source overlap capacitance. Since the transistor is asymmetric, the simulation shortcuts used for the standard and

annular transistors are not applicable for the funnel-shaped transistor; the 3D simulation

domain is defined to be the entire transistor.
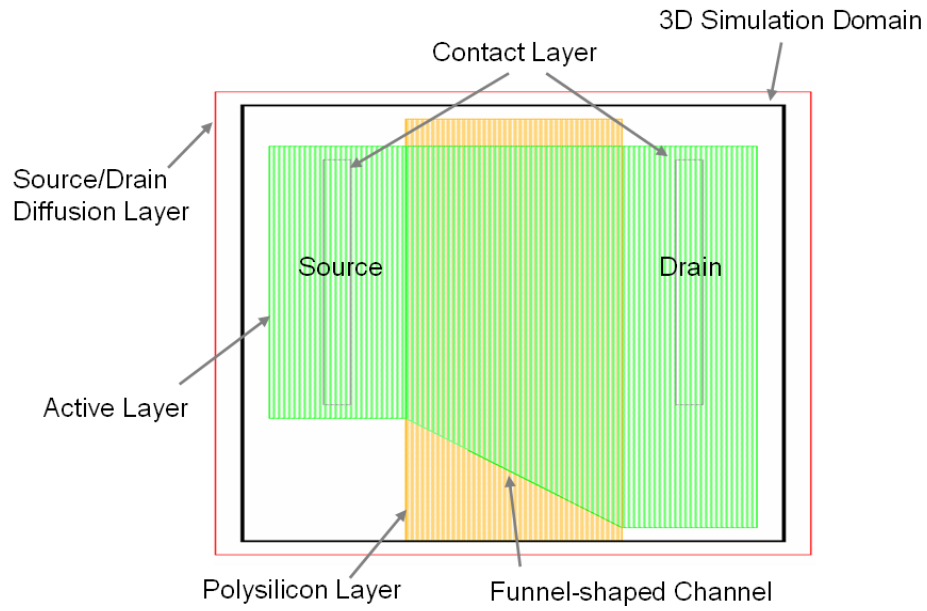
Figure 4.9 Layout and simulation domain of the funnel-shaped transistor

Since it is necessary to simulate the entire structure, a tradeoff is made to reduce meshing in order to reduce process simulation time. The mesh specification for the funnel-shaped transistor's channel is identical to the standard and annular transistors. However, the mesh for the source and drain is coarser in order to reduce mesh count and simulation time. Figure 4.10 displays the final structure at the end of Sentaurus Process simulation. The figure illustrates the asymmetric nature of the funnel-shaped transistor featuring the graded channel and different source and drain widths. In this figure, the nitride spacer and STI are translucent to show the asymmetric active region.
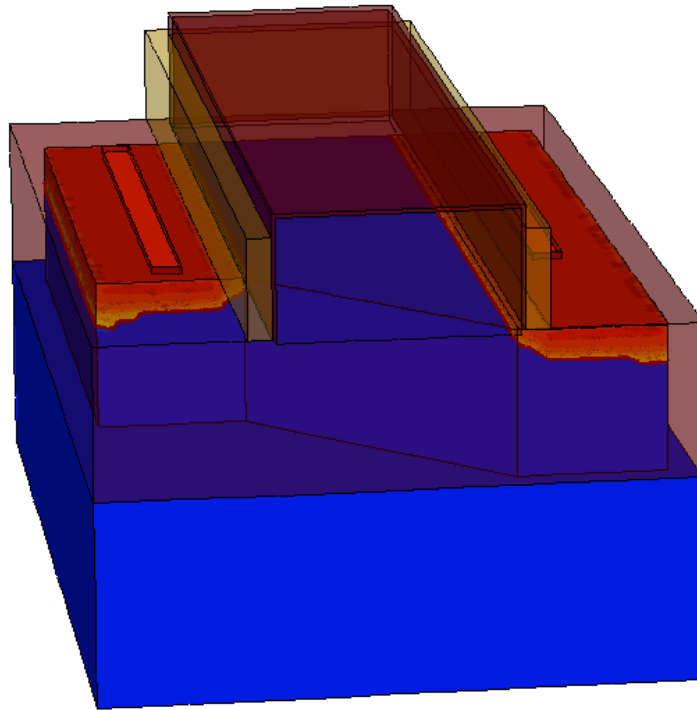
Figure 4.10 3D process simulation generates a full funnel-shaped NMOS transistor. The nitride spacer and STI are translucent for easier viewing.

Figure 4.11 displays the final funnel-shaped structure without any oxide, nitride, or polysilicon. Only silicon is displayed, revealing various n-type and p-type regions. The difference in gate-source and gate-drain overlap can be seen in this figure.
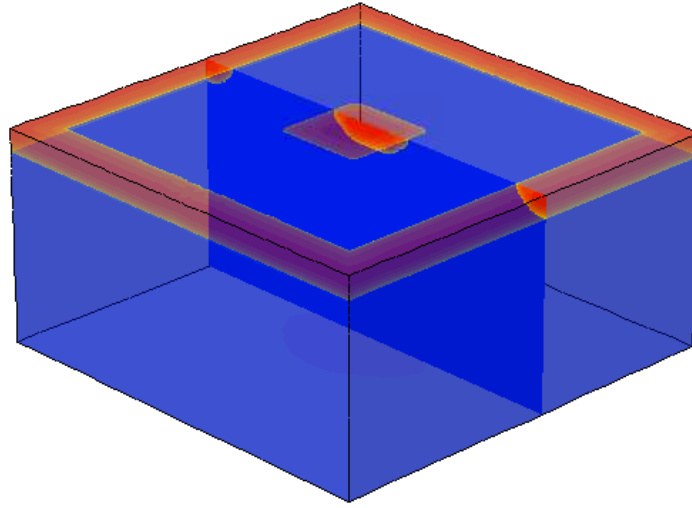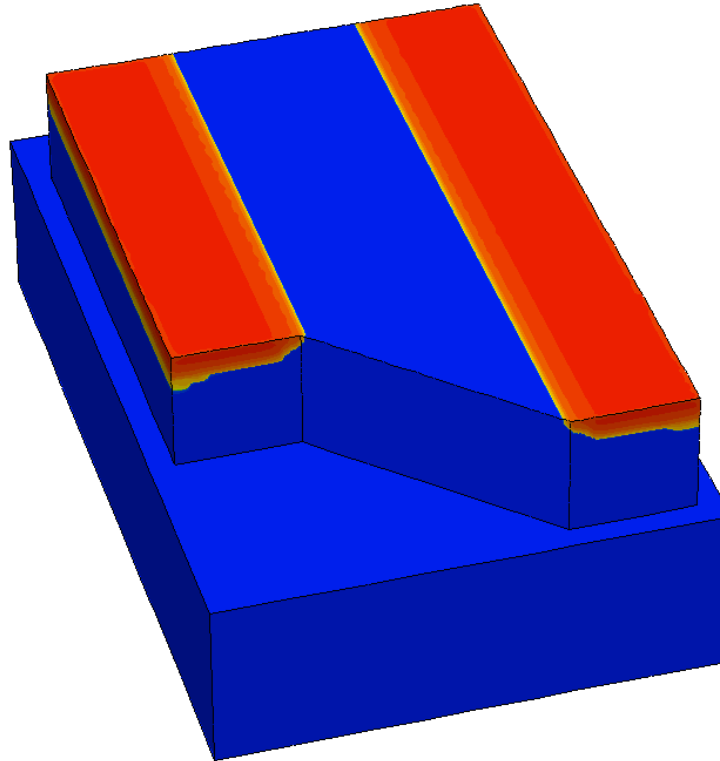

Figure 4.11 The source and drain diffusion regions in the funnel-shaped structure. The nitride spacer, polysilicon gate, and oxide are not shown for easier viewing.

Since Sentaurus Process simulates the entire funnel-shaped transistor, Sentaurus Structure Editor only performs basic post processing to prepare for device simulation. The size of the structure is reduced in the vertical direction, contacts are added, and the structure is remeshed. Reflection is not necessary for the funnel-shaped transistor.

4.5   Simulation Performance

This section compares the simulation performance of the various transistors created to study charge injection/clock feedthrough. A Linux workstation with four 3.0 GHz computer processors and 12 GB of memory is used to perform the TCAD simulations. Table (4.3) summarizes the number of vertices and run times for process and mixed-mode transient device simulations.

Table 4.3 Comparison of simulation time and number of vertices for different transistor types.

Simulation type	Transistor type	Process simulation		Device simulation	
		# vertices	Run time (hrs)	# vertices	Normalized Run time
2D	Standard NMOS	13,961	0.35	4,247	1.00
3D	Standard NMOS	32,218	3.00	59,645	72.53
3D	Annular NMOS	83,695	7.75	145,764	225.88
3D	Funnel NMOS	241,276	28.5	195,563	359.53

5   Simulation Results

This chapter discusses charge injection/clock feedthrough results from 2D and 3D simulations. The transistor's turn off characteristic is discussed in terms of how source voltage responses to both time and gate voltage. This is followed by a discussion of charge injection/clock feedthrough's dependence on transistor operation, size, and geometry. 2D simulations are used to examine the effect of gate high level voltage, low level voltage, fall time, and transistor length, while 3D simulations are utilized to explore the effect of transistor width and geometry, such as the funnel and annular transistors.

5.1 Source Voltage Response to Time and Gate Voltage

As discussed in section 3.4.4, the mixed-mode transient simulation models the transistor turning on and off to examine the transient nature of charge injection and clock feedthrough. In order to verify the simulated transient characteristics with the presented model, a strategy from section 2.4 is repeated. Using 2D simulations, the gate voltage is lowered from 3 V to -200 mV using an ideal gate ramp and a step approximation, as shown in Figure 5.1.
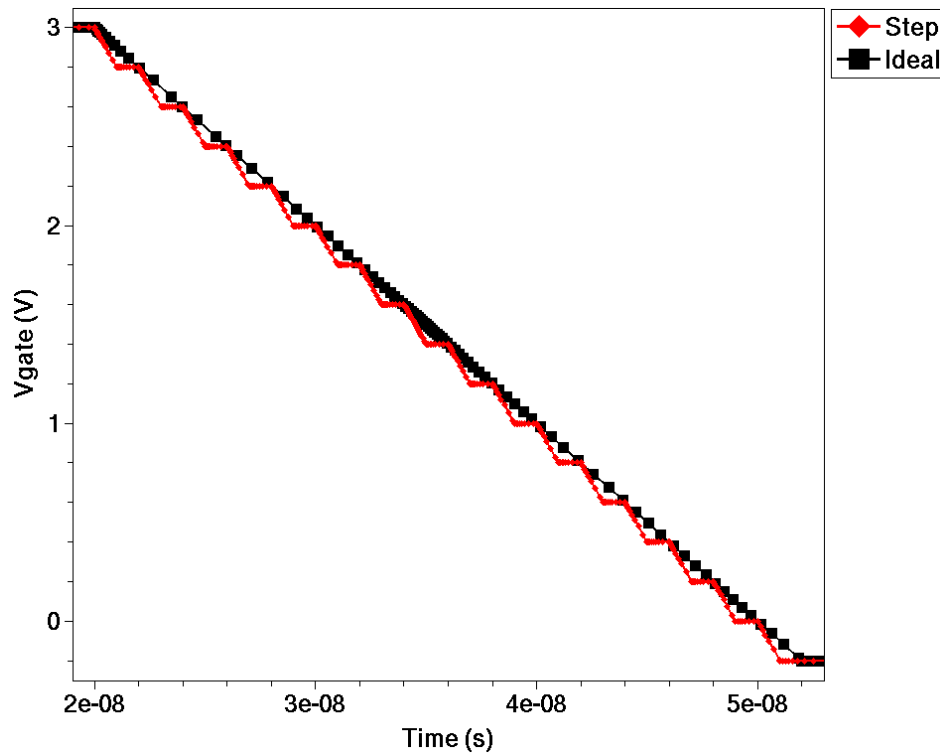
Figure 5.1 An ideal gate ramp is approximated by a series of steps to examine how source voltage responds. The ideal gate ramp transitions from 3 V to -200 mV in 31 ns. In the step approximation, the gate voltage decreases by 200 mV in 1 ns and remains constant for 1 ns.

The step approximation is used to exhibit the source voltage recovery due to source-drain conduction. The resulting transient response of Vsource is shown for both the ideal ramp and step approximation in Figure 5.2.
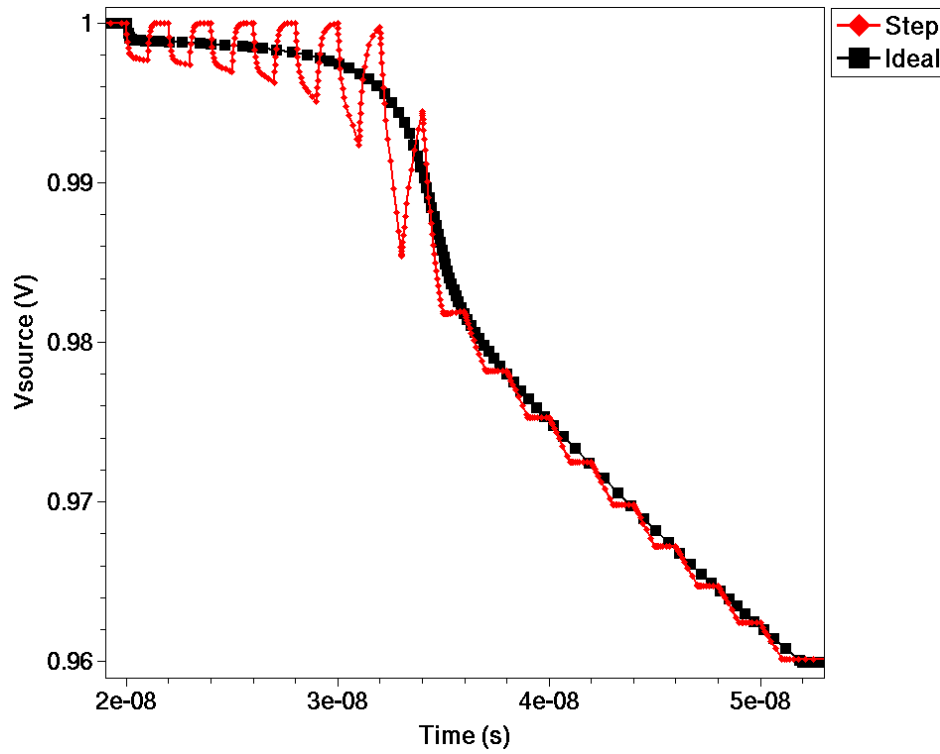
Figure 5.2 Source voltage responds to the ideal gate ramp and step approximation from Figure 5.1. The step approximation reveals voltage loss due to charge injection and recovery due to source-drain conduction.

The transient response of Vsource is similar to the model discussed in Chapter 2. As Vgate begins to decrease at t = 0, Vsource decreases mainly due to channel charge. Since there is a potential difference between source and drain, the current allows Vsource to recover the voltage loss. As Vgate approaches the threshold condition at approximately t = 34 ns, I_{DS} is not large enough to fully recover the voltage. Vsource continues to

decrease in sub-threshold condition, where the main contributor to voltage loss is gate-source coupling.

While the transient characteristic is very informative, it is equally insightful to analyze how source voltage changes with gate voltage. Figure 3.14 shows the simulation results from the mixed-mode transient simulation. However, in Figure 5.3 the data is re-plotted to only examine the transistor's turn off event, when the gate transitions from 3 V to -200 mV. Vdrain and Vsource are plotted as a function of Vgate.
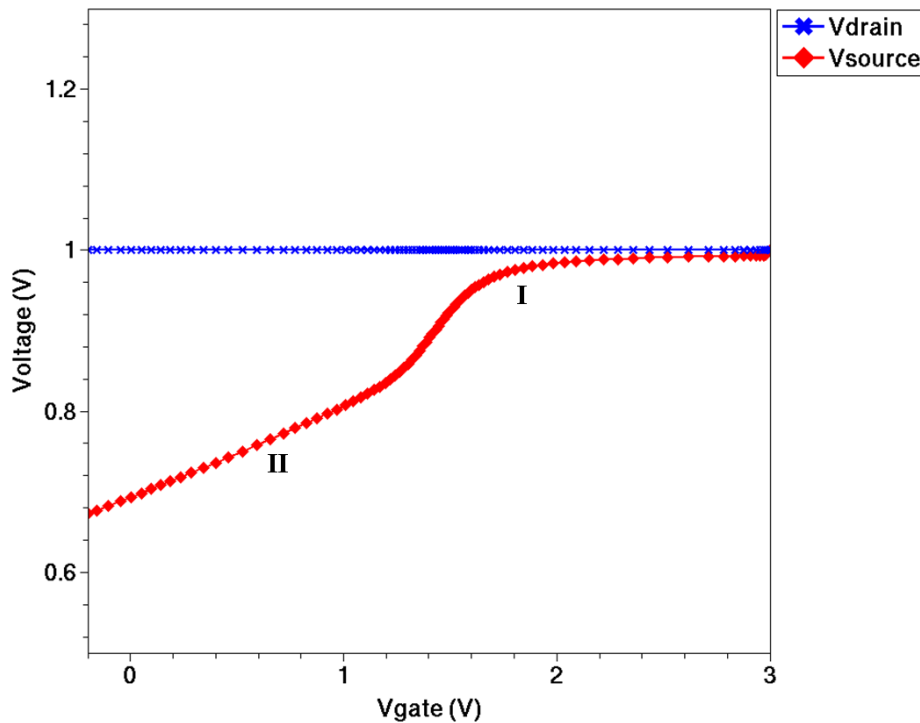
Figure 5.3 Source and drain voltages as a function of gate voltage. As gate voltage decreases, the source voltage transitions from Region I to Region II. Region I is defined as the period in which charge injection is the main contributor to error voltage. Region II is defined as the period in which clock feedthrough is the main contributor.

The response of Vdrain and Vsource is also similar to the behavior discussed in section 2.4.4. Vdrain does not change because the drain is connected to an ideal voltage source;

however Vsource is dependent on Vgate. As Vgate decreases from 3 V, Vsource transitions from a non-linear to linear dependency. The region of non-linear dependency, Region I, is due to the interaction between charge injection and source-drain conduction. The region of linear dependency, Region II, is due to clock feedthrough. The transition region between Regions I and II is the threshold condition ($V_G = V_S + V_T$). This plot type will be utilized in the following sections, as charge injection/clock feedthrough's dependence on transistor operation, size, and geometry are discussed.

5.2 Dependence on Transistor Operation

This section discusses the effect of transistor operation on charge injection and clock feedthrough. Transistor operation consists of the gate high level voltage (VGH), gate low level voltage (VGL), and gate fall time (Tfall).

5.2.1 Gate High Level Voltage

In order to examine the effect of VGH, the gate is turned off with VGH values varying from 4 to 2.8 V. As shown in Figure 5.4, a transistor with W/L = 0.4 µm/1.0 µm has the gate ramping from various VGH values down to -200 mV. In order to make a proper comparison, the gate fall rate is kept constant at 0.3 V/ns.
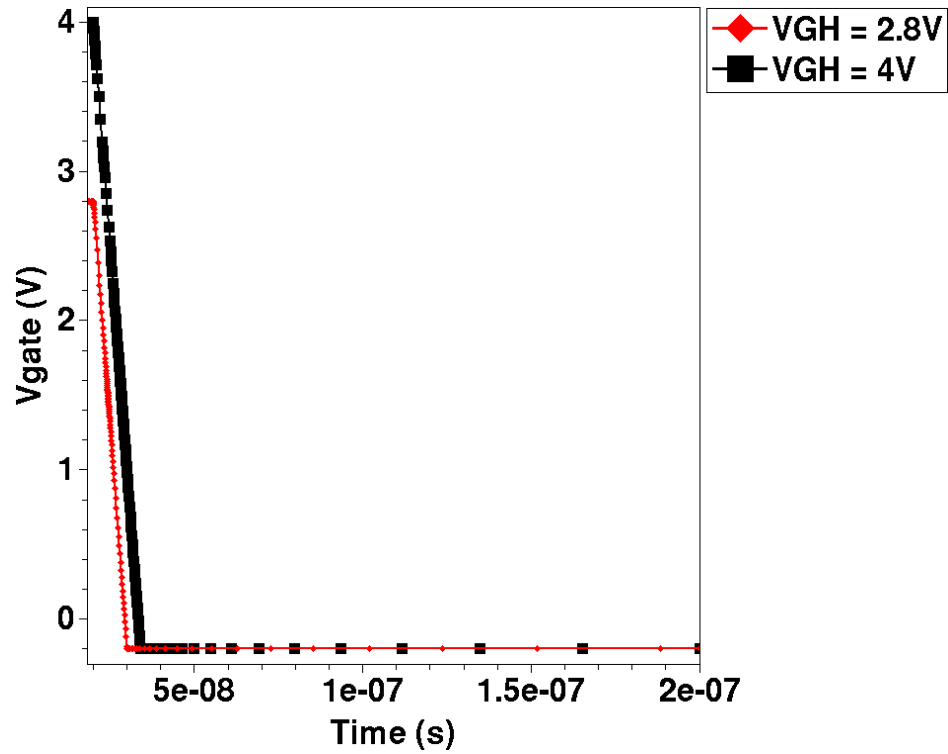
Figure 5.4 Gate voltage is turned off from VGH values of 4 and 2.8 V. In both cases, the gate voltage decreases down to -200 mV. Tfall values are 14 to 10 ns respectively to establish a constant gate fall rate of 0.3 V/ns.

The effect of VGH is shown in Figure 5.5, which plots Vsource as a function of Vgate for

VGH values of 4 and 2.8 V.
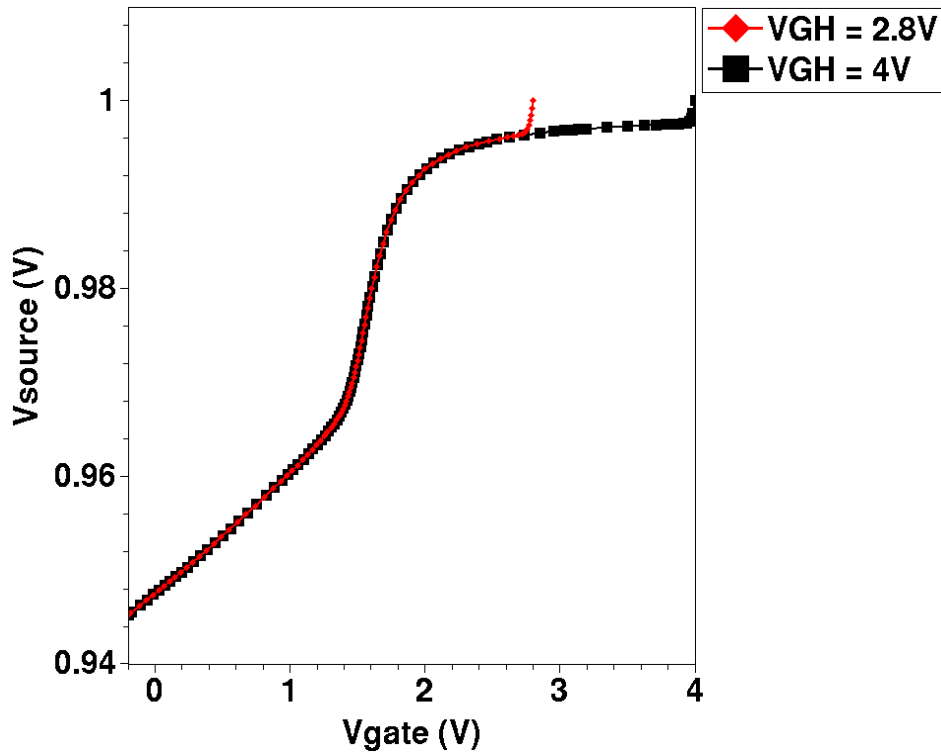
Figure 5.5 Source voltage as a function of gate voltage for VGH values of 4 and 2.8 V

Although VGH = 4 V started at a higher gate voltage than VGH = 2.8 V, the Vsource response is the same. Region I is identical once Vgate reaches 2.8 V, and Region II is the same. According to the model, a higher gate voltage would result in more channel charge and coupling through overlap capacitance, however the increase in charge injection and clock feedthrough is negated by the increased source-drain conduction. By plotting error voltage as a function of VGH in Figure 5.6, it can be shown that VGH has little effect on error voltage, assuming the transistor is operating in strong inversion.
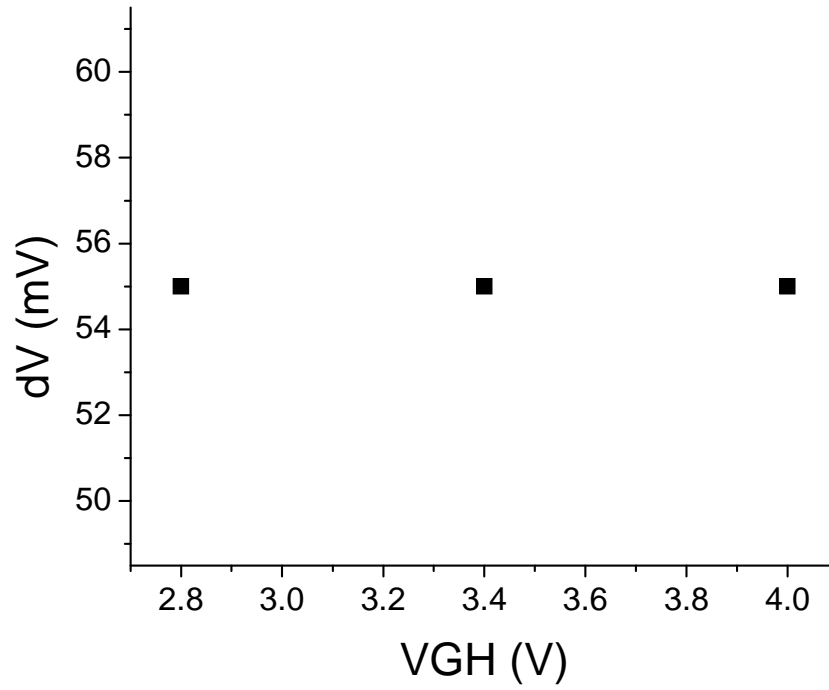
Figure 5.6 Error voltage as a function of VGH. The gate voltage decreases from VGH values of 4, 3.4, and 2.8 V down to -200 mV. Tfall values are 14, 12, and 10 ns respectively to establish a constant gate fall rate of 0.3 V/ns.

5.2.2 Gate Low Level Voltage

The gate voltage of a transistor with W/L = 0.4 µm/1.0 µm decreases from 3 V to

VGL values ranging from 0 to -1.2 V, as shown in Figure 5.7. In order to make a proper

comparison, gate fall rate is kept constant at 0.3 V/ns.
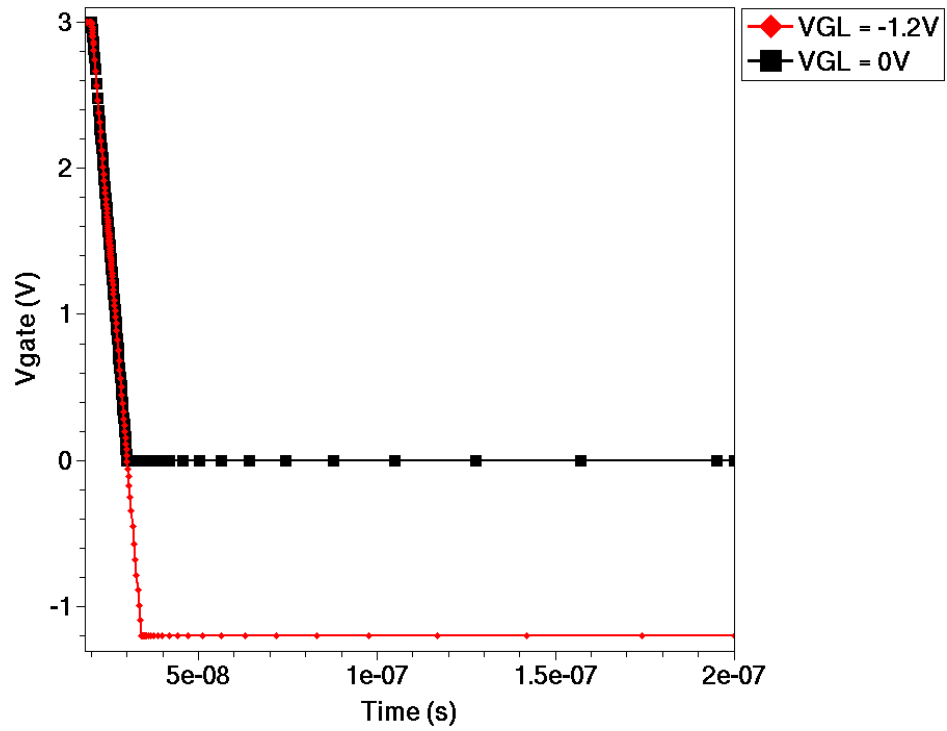
Figure 5.7 Gate voltage decreases from 3 V to VGL values of 0 and -1.2 V. Tfall values are 10 and 14 ns respectively to establish a constant gate fall rate of 0.3 V/ns.

The effect of VGL is shown in Figure 5.8, which plots Vsource as a function of Vgate for

VGL values of 0 and -1.2 V.
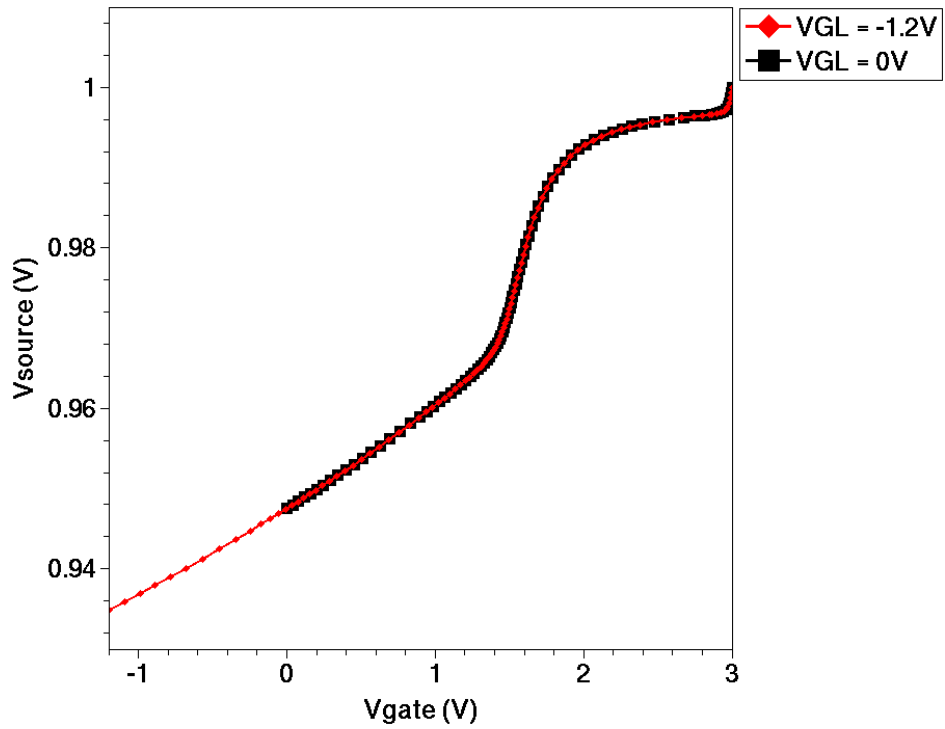
Figure 5.8 Source voltage as a function of gate voltage for VGL values of 0 and -1.2 V

As expected, Vsource decreases identically until Vgate reaches the VGL values in

Region II. When VGL is a lower value, Vsource continues to decrease due to clock

feedthrough. As shown in Figure 5.9, error voltage has a linear dependence on VGL due

to the voltage divider relationship for clock feedthrough (discussed in section 2.2).
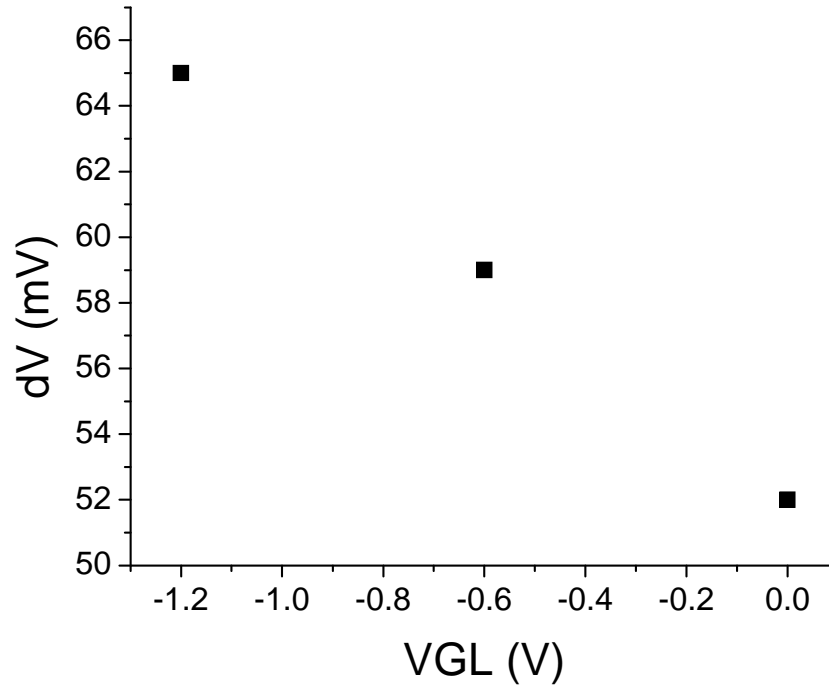
Figure 5.9 Error voltage as a function of VGL. The gate voltage decreases from 3 V to VGL values of 0, -0.6, and -1.2 V. Tfall values are 10, 12, and 14 ns respectively to establish a constant gate fall rate of 0.3 V/ns.

5.2.3 Gate Fall Time

This section examines the effect of Tfall on charge injection/clock feedthrough. The effect of different fall times is studied by keeping the voltage swing constant. The gate voltage of a transistor with W/L = 0.4 μm/1.0 μm decreases from 3 V to -200 mV with Tfall ranging from 500 ps to 100 ns. The result is shown in Figure 5.10, which plots Vsource versus Vgate for various fall times.
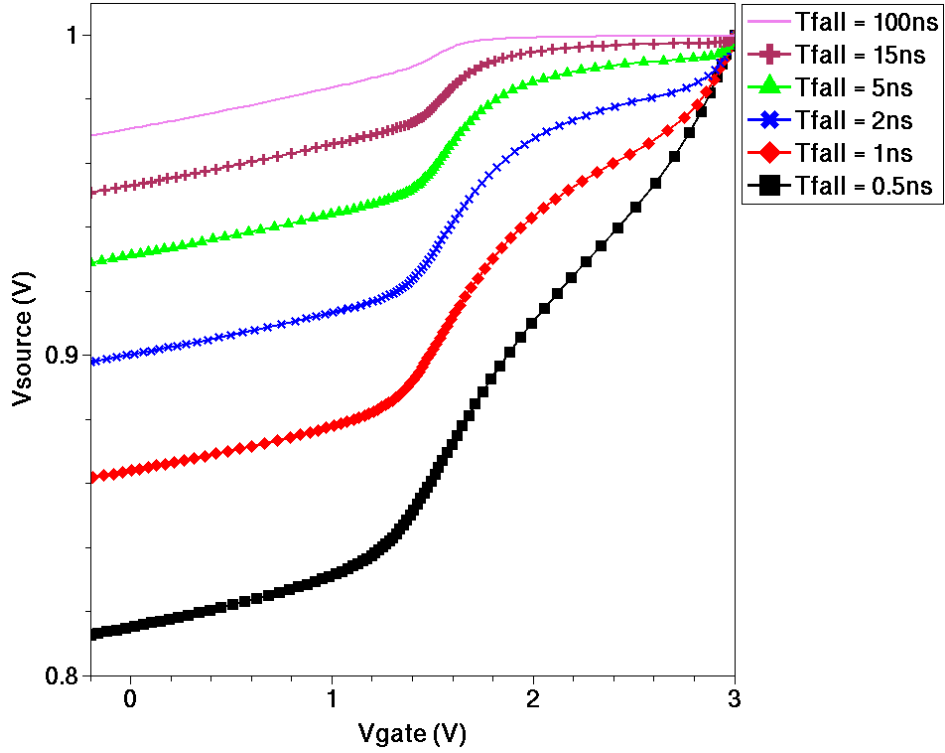
Figure 5.10 Source voltage versus gate voltage for Tfall ranging from 500 ps to 100 ns

The graph shows that Region I is greatly affected by Tfall. When Tfall is 100 ns, Vsource is insensitive to Vgate in Region I. As Tfall decreases, Vsource in Region I becomes more sensitive to Vgate; this is exemplified when Tfall is 500 ps. Region II on the other hand, is not affected by Tfall; Region II's slope is the same for all six cases.

Tfall affects Region I because it sets the amount of time I_{DS} can recover voltage loss due to charge injection. By decreasing Tfall, the source voltage decreases faster and there is less time for I_{DS} to recover voltage. Region II is not affected by Tfall because the coupling through overlap capacitance behaves as a voltage divider and hence is not a function of time. Source-drain conduction also does not play a role in Region II.

Figure 5.11 plots error voltage as a function of Tfall. This non-linear relationship is especially apparent for small Tfall values, in which error voltage is a strong function of Tfall.
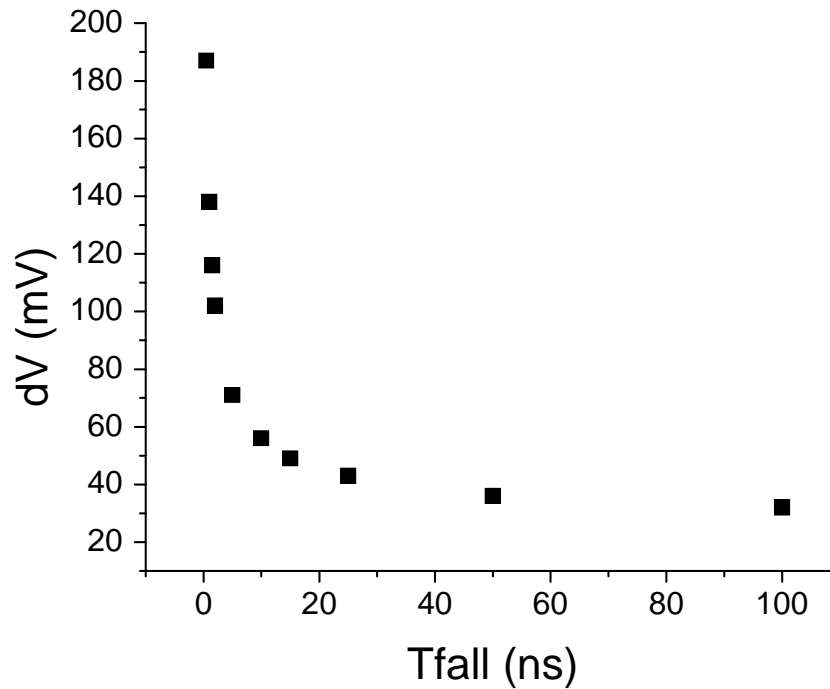
Figure 5.11 Error voltage as a function of Tfall. The gate voltage decreases from 3 V to -200 mV for Tfall values ranging from 500 ps to 100 ns.

5.3   Dependence on Transistor Size

This section discusses the effect of transistor size on charge injection/clock feedthrough. When circuit designers choose a transistor's W/L, considerations are made for various performance parameters, including charge injection/clock feedthrough. The

effect of transistor length is analyzed using 2D simulations, while 3D simulations are

utilized to study the effect of width.

5.3.1 Transistor Length

In order to examine the effect of length on charge injection and clock

feedthrough, NMOS transistors with width of 0.4 μm and lengths of 0.3, 0.4, 0.6, and 1.0

μm are simulated. The gate is turned off from 3 V to -200 mV with Tfall of 10 and 100

ns. Figure 5.12 plots the four transistors' Vsource versus Vgate characteristic for 10 ns

fall time.

Figure 5.12 Source voltage as a function of gate voltage when the gate decreases from 3 V to -200 mV with Tfall of 10 ns. The transistor width is 0.4 μm and lengths are 0.3, 0.4, 0.6, and 1.0 μm.

Regions I and II are examined to understand length dependency. For all lengths, Region II is identical and has the same slope. This is because the widths and gate-source overlaps are identical, therefore gate-source coupling is the same for all four cases.

In Region I, as length increases Vsource becomes more sensitive to Vgate. When transistor length increases, there is more channel charge that contributes to charge injection. In addition, as length increases source-drain conduction decreases. For longer lengths, Vsource requires more time to recover the voltage loss due to charge injection. This is illustrated in Figure 5.13, which reproduces this scenario except for a larger Tfall of 100 ns.
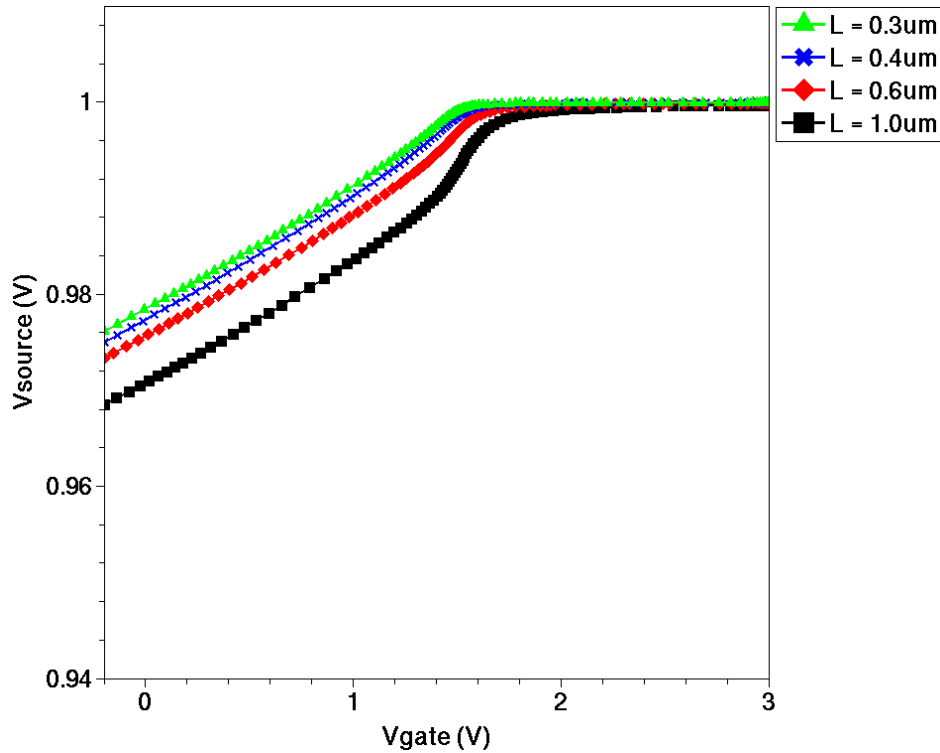
Figure 5.13 Source voltage as a function of gate voltage when the gate decreases from 3 V to -200 mV with Tfall of 100 ns. The transistor width is 0.4 μm and lengths are 0.3, 0.4, 0.6, and 1.0 μm.

When Tfall is 100 ns, Vsource is overall less sensitive to Vgate in Region I. As Tfall

increases, there is more time for I_{DS} to recover voltage loss. This relationship with

length and Tfall can be visualized in Figure 5.14, which plots error voltage as a function

of transistor length for Tfall values of 10 and 100 ns.

Figure 5.14 Error voltage as a function of transistor length for Tfall values of 10 and 100 ns

Error voltage increases in a linear fashion with transistor length, however the relationship

is stronger for smaller Tfall. For 10 ns Tfall, error voltage changes with length at a rate

of 39.8 mV/μm, while for 100 ns, the rate of change is 11.5 mV/μm.

5.3.2   Transistor Width

In order to examine the effect of width on charge injection/clock feedthrough, NMOS transistors with length of 0.4 μm and widths of 0.3, 0.4, 0.6, and 1.0 μm are simulated in 3D. The gate is turned off from 3 V to -200 mV with Tfall values of 10 and 100 ns. As discussed in section 4.2.3, during mixed-mode simulation the total source capacitances for each of these transistors are set to 6 fF to ensure the comparison is fair. Vsource is plotted as a function of Vgate in Figure 5.15.
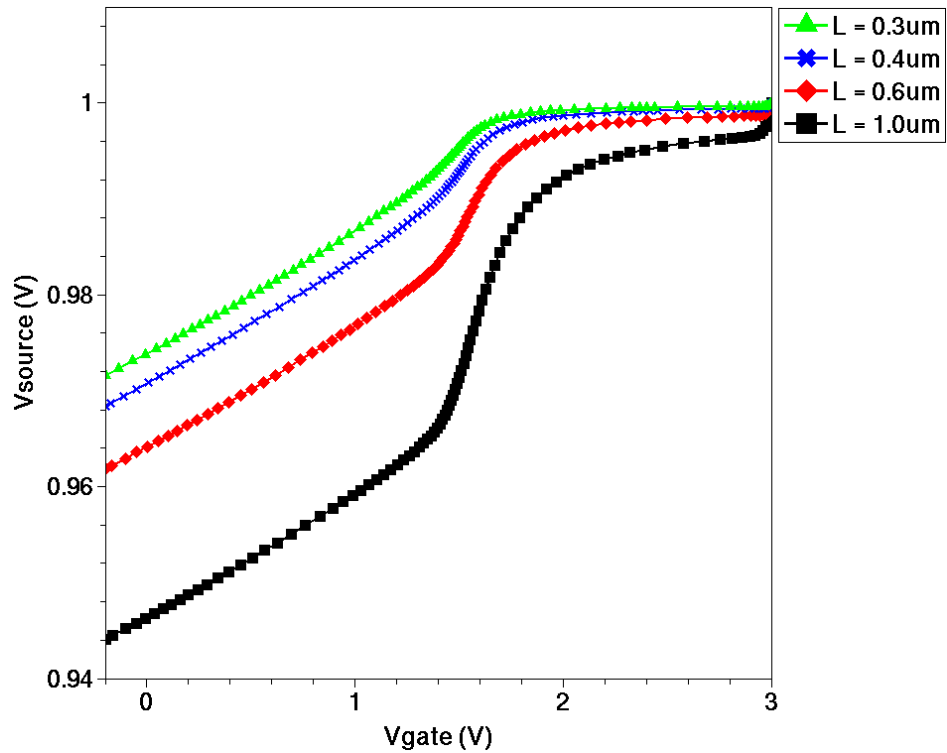

Figure 5.15 Source voltage as a function of gate voltage when the gate decreases from 3 V to -200 mV with Tfall of 10 ns. The transistor length is 0.4 μm and widths are 0.3, 0.4, 0.6, and 1.0 μm.

Regions I and II are analyzed to understand the width dependence. For all widths, Region I is identical and Vsource is insensitive to Vgate. Transistors with larger widths have more channel charge and overlap capacitance to induce charge injection and clock

feedthrough, respectively. This however is negated by I_{DS}, which increases with width to allow Vsource to recover voltage loss. Region II on the other hand, is affected by transistor width. As transistor width increases, the slope of Region II increases. This is explained by the increase in gate-source overlap and therefore clock feedthrough. The relationship with transistor width and Tfall can be visualized in Figure 5.16, which plots error voltage as a function of width for Tfall values of 10 and 100 ns.
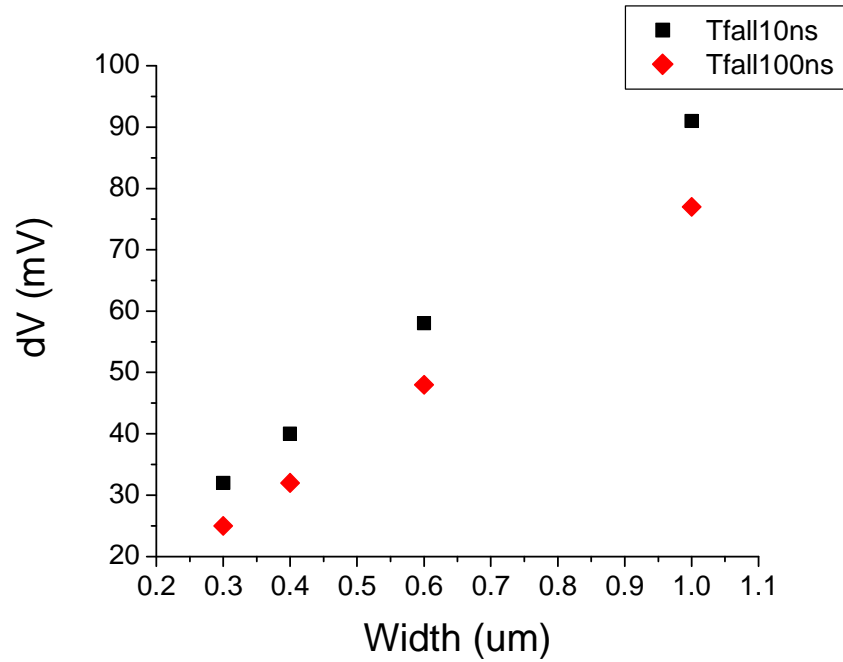
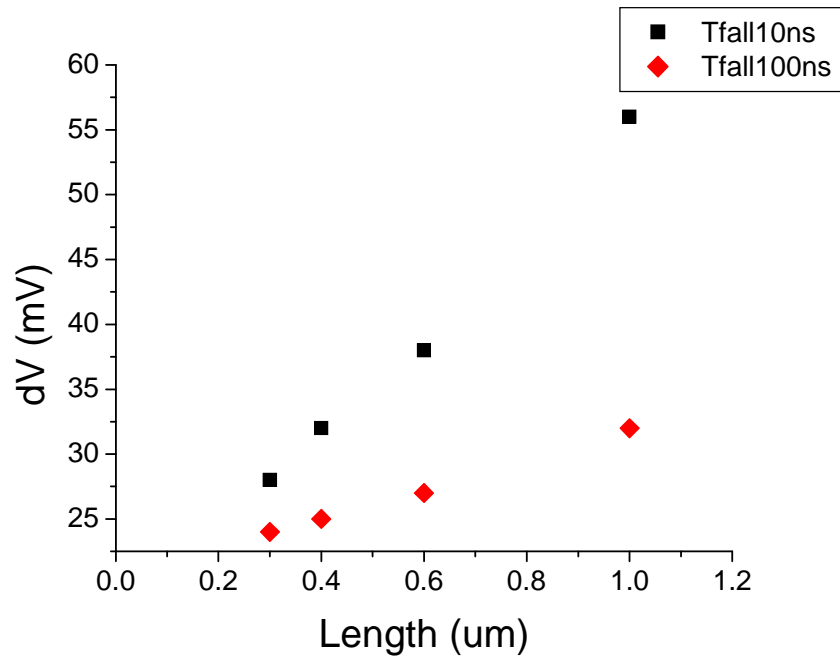**Figure 5.16 Error voltage as a function of transistor width for Tfall values of 10 and 100 ns**

Error voltage increases linearly with transistor width and the rate of change is slightly affected by Tfall. The rate of change is 84.6 mV/μm for 10 ns Tfall and 74.6 mV/μm for 100 ns.

5.4   Dependence on Transistor Geometry

This section compares charge injection/clock feedthrough for various transistor geometries. The standard, funnel, and annular transistors (discussed in Chapter 4) are compared in terms of error voltage and other performance parameters. As shown in Table (5.1), all three transistors have device dimensions of 1.0 μm/0.4 μm. Since the funnel and annular transistors are asymmetrical, the width is defined as the gate-source overlap.

Table 5.1 Comparison of widths and lengths for the standard, funnel, and annular transistors.

Type	Length (μV)	Drain Width (μm)	Source Width (μm)
Standard	0.4	1.0	1.0
Funnel	0.4	1.4	1.0
Annular	0.4	4.2	1.0

As discussed in section 4.2.3, during mixed-mode simulation the total source capacitances for each of these transistors are set to 6 fF to ensure a fair charge injection comparison.

Using 3D simulations, the standard, funnel, and annular transistors have the gate voltage lowered from 3 V to -200 mV with 10 ns Tfall. Figure 5.17 plots Vsource as a function of Vgate for these three transistor types.
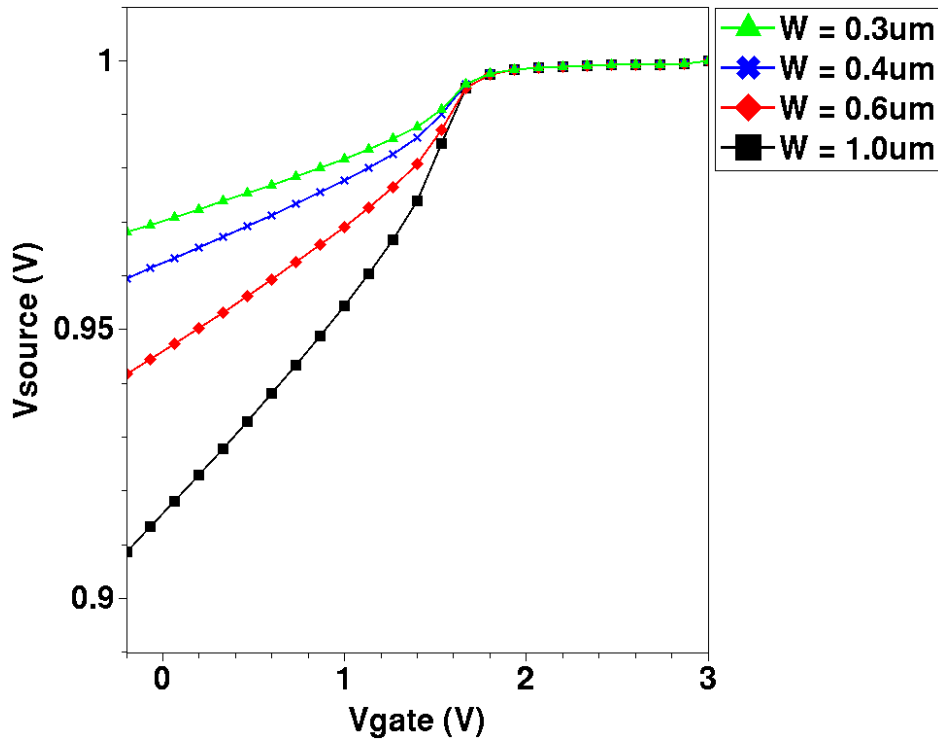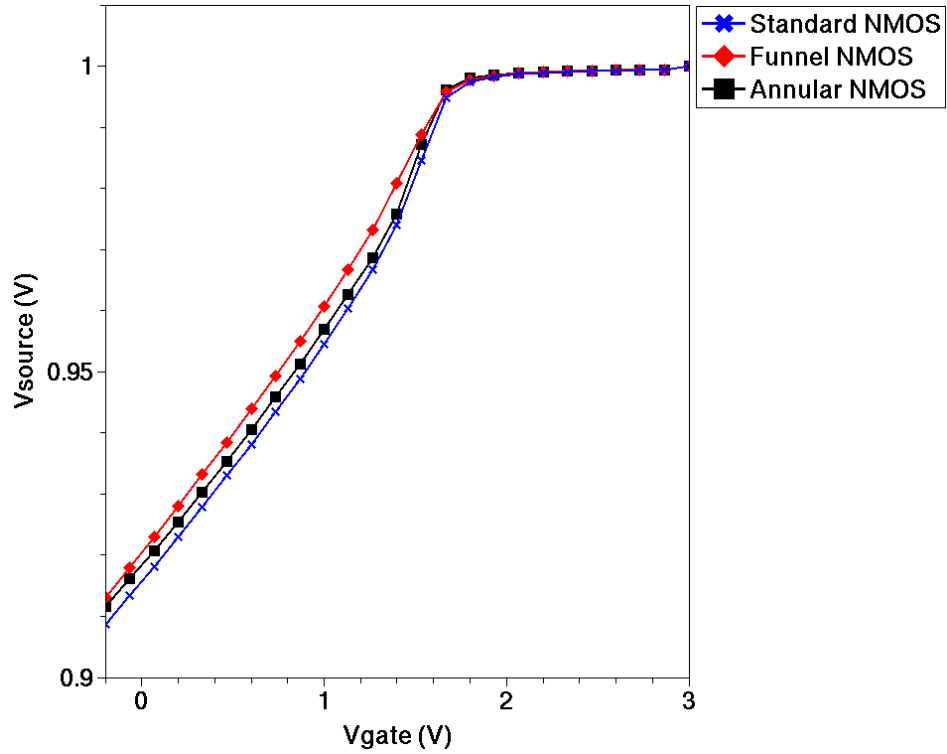
Figure 5.17 Source voltage as a function of gate voltage when the gate decreases from 3 V to -200 mV with Tfall of 10 ns. A comparison is made between the standard, funnel, and annular transistors.

The plot shows that the error voltage is very similar for all three transistors. Despite having different channel shapes and sizes, the charge injection characteristics are quite comparable for the standard, funnel, and annular transistors. Due to the transistors' various geometries, the channel charge and drive current are different. Figure 5.18 plots I_D-V_D when gate bias is 1 V for the three transistors.
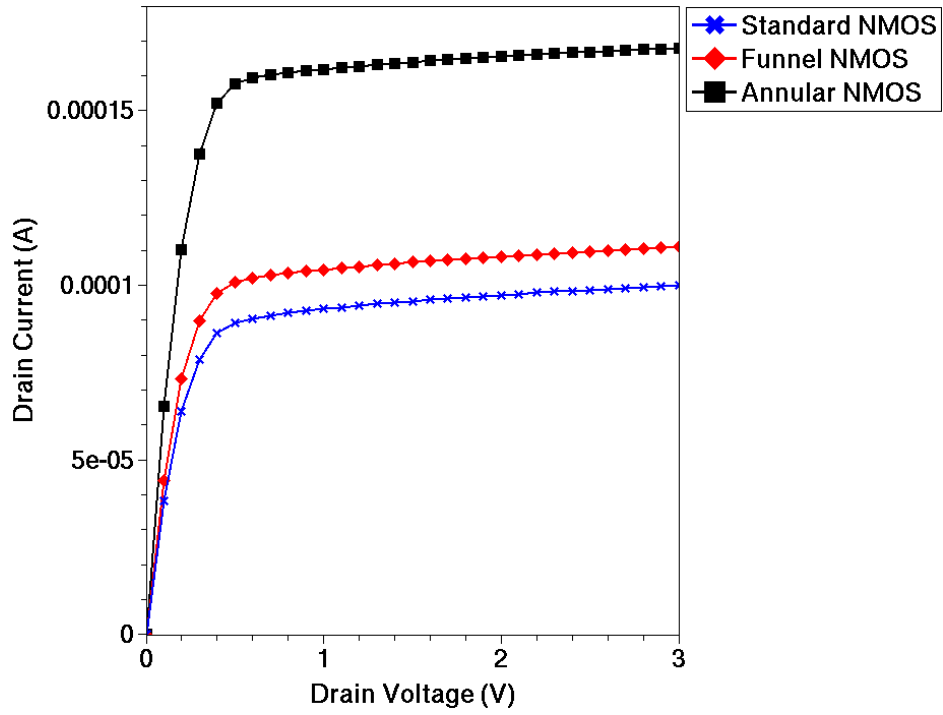
Figure 5.18 Drain current as a function of drain voltage for gate bias of 1 V. A comparison is made between the standard, funnel, and annular transistors.

Drain current is extracted from the plot when drain voltage is 3 V. The annular transistor

has the widest drain, therefore it has the largest drive current. This is followed by the

funnel and standard transistors. Table (5.2) compares error voltage, gate area, and drive

current for the three transistors.

Table 5.2 Comparison of various parameters among the standard, funnel, and annular transistors.

Type	Error Voltage (mV)	Gate Area (μm^2)	Drive Current (mA)
Standard	91	0.40	0.100
Funnel	87	0.48	0.111
Annular	88	1.04	0.168

The geometry effect is similar to the width effect discussed in section 5.3.2. The annular transistor has the largest gate area and most channel charge, but it has the highest source-drain current to offset the voltage loss; this explains the identical Region I characteristics in Figure 5.17. Region II has similar slopes because the gate-source overlap capacitance is the same, resulting in identical clock feedthrough characteristics.

6 Measurements

This chapter discusses test structure measurements performed to examine charge injection and clock feedthrough. The measurement methodology is detailed by first introducing the test structures fabricated in a 0.18 µm CMOS process. This is followed by an explanation of the measurement setup. After the measurement results are discussed, a comparison is made against the calculated and simulated data.

6.1 Charge Injection/Clock Feedthrough Test Structure

Figure 6.1 shows the test structure schematic designed to measure and verify charge injection and clock feedthrough. The circuit, which consists of five NMOS transistors and two MIM capacitors, is constructed to characterize the charge injection/clock feedthrough characteristics of transistor M1.

Figure 6.1 Test structure schematic designed to measure charge injection and clock feedthrough. The circuit consists of five NMOS transistors and two MIM capacitors. The circuit is designed using a 0.18 μm CMOS technology.

Vd4, Vg4, Vg1, Vd3, Vg3, Vdd, and Vgnd are inputs to the circuit and OutA and OutB

are outputs to the circuit. Transistors M4 and M3 are switches to reset capacitors C0 and

C1, while M0 and M2 are source followers to act as voltage buffers. Table (6.1) displays

the transistor W/L and capacitor values in the circuit.

Table 6.1 Values of the transistors and capacitors in the charge injection/clock feedthrough circuit.

Type	Name	Value	Unit
MIM capacitor	C0	6	fF
MIM capacitor	C1	6	fF
NMOS transistor	M4	0.40/0.30	µm/µm
NMOS transistor	M3	0.40/0.30	µm/µm
NMOS transistor	M2	0.42/0.40	µm/µm
NMOS transistor	M0	0.42/0.40	µm/µm
NMOS transistor	M1	0.40/1.0	µm/µm
		0.40/0.6	
		0.40/0.4	
		0.40/0.3	

As described in the table, the transistor length for M1 is varied from 0.3 to 1.0 µm in order to examine the effect of length on charge injection and clock feedthrough. Therefore, there are four circuits, and each circuit has a length variation of the M1 transistor.

As shown in Figure 6.1, the circuit is designed with considerations for symmetry. This is done so that charge injection/clock feedthrough can be measured in a variety of circuit configurations. Since the thesis focuses on a switched-capacitor configuration, the error voltage is measured on only one MIM capacitor. In these measurements, the capacitor of interest is C0. By keeping M3 on at all times, C1 will be held at a fixed voltage. To examine charge injection/clock feedthrough, the gate of M1 is clocked and

the signal is read out on OutA. The bias conditions are discussed in detail in section 6.2.
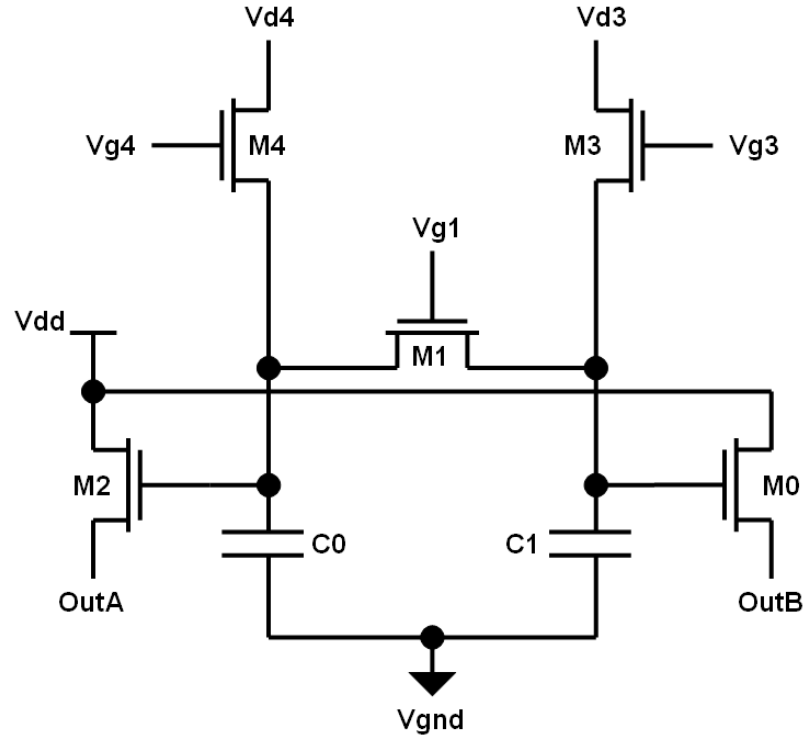
The layout of the circuit shown in Figure 6.2.
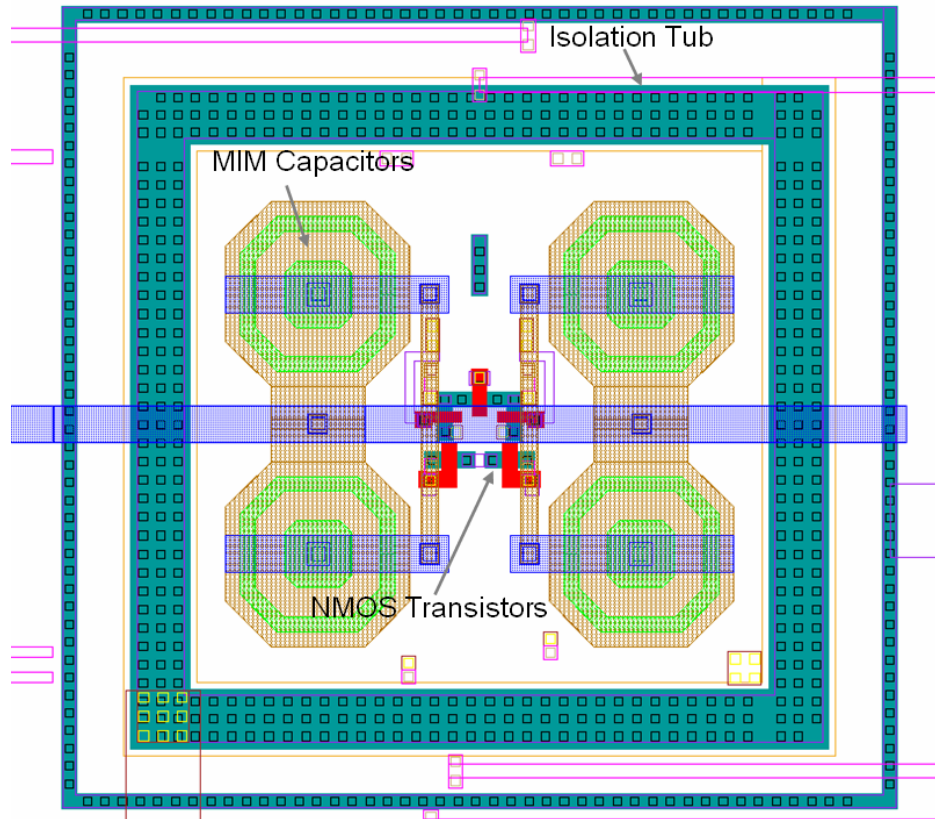
Figure 6.2 Test structure layout designed to measure charge injection and clock feedthrough. The circuit consists of five NMOS transistors and two MIM capacitors. The circuit is designed using a 0.18 μm CMOS technology.

The NMOS transistors reside in a p-type well that is separated from the actual substrate

by an isolation tub. Figure 6.2 shows the perimeter of the tub, however the bottom is not

shown. This n-type tub surrounds the circuit to provide substrate noise isolation. The

two MIM capacitors are placed in a symmetric fashion to ensure proper matching. The

test structure is fabricated using a 0.18 μm CMOS process and the die is packaged into a

144 lead pin grid array (PGA) package shown in Figure 6.3.
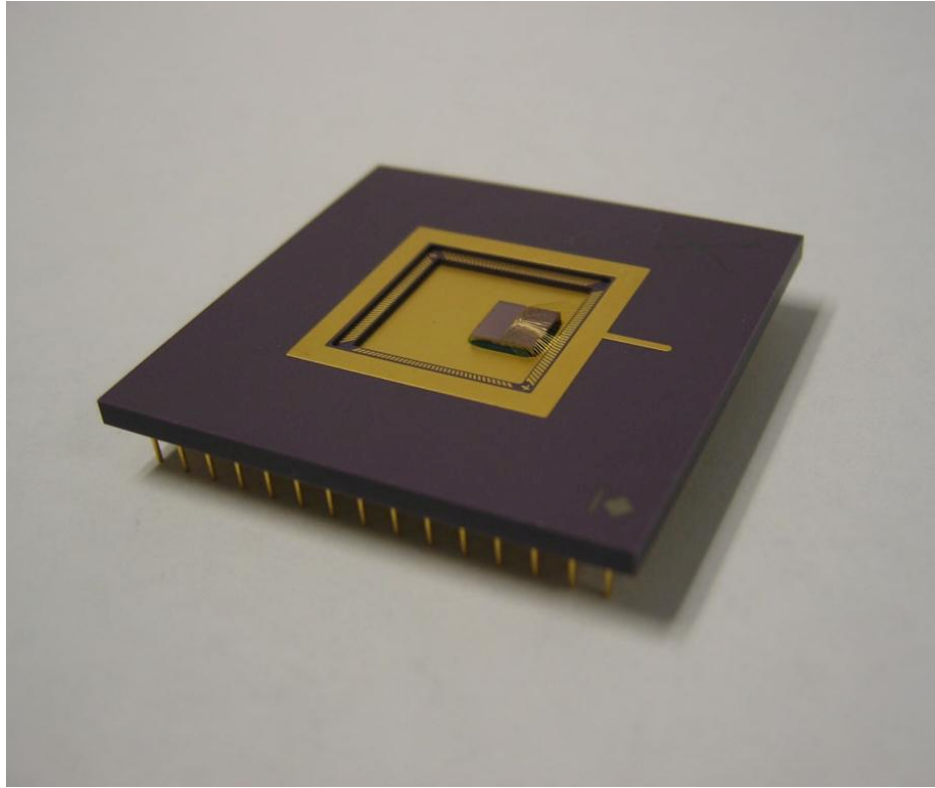
Figure 6.3 The test structure is fabricated in a 0.18 μm CMOS process and the die is packaged into a 144 lead PGA package

6.2 Measurement Setup

Figure 6.4 shows the test measurement system used to measure charge injection

and clock feedthrough.
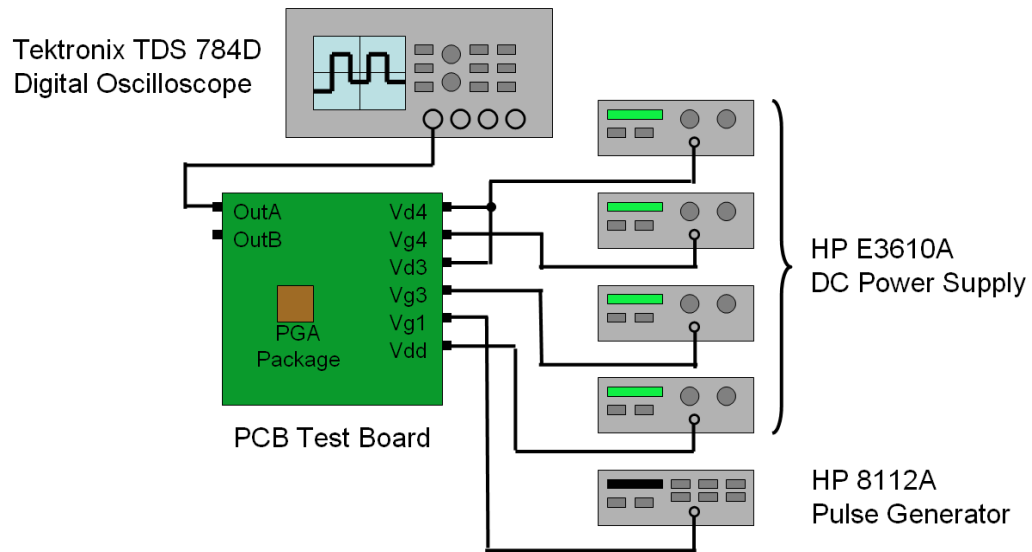
Figure 6.4 Test measurement setup for charge injection and clock feedthrough includes a pulse generator, oscilloscope, test board, and DC power supplies

The test measurement system required a pulse generator, oscilloscope, test board and DC

power supplies. A Tektronix TDS 784D digital oscilloscope was used to measure the

input signal Vg1 and the output signal OutA. Figure 6.5 displays the voltages applied to

measure the circuit.
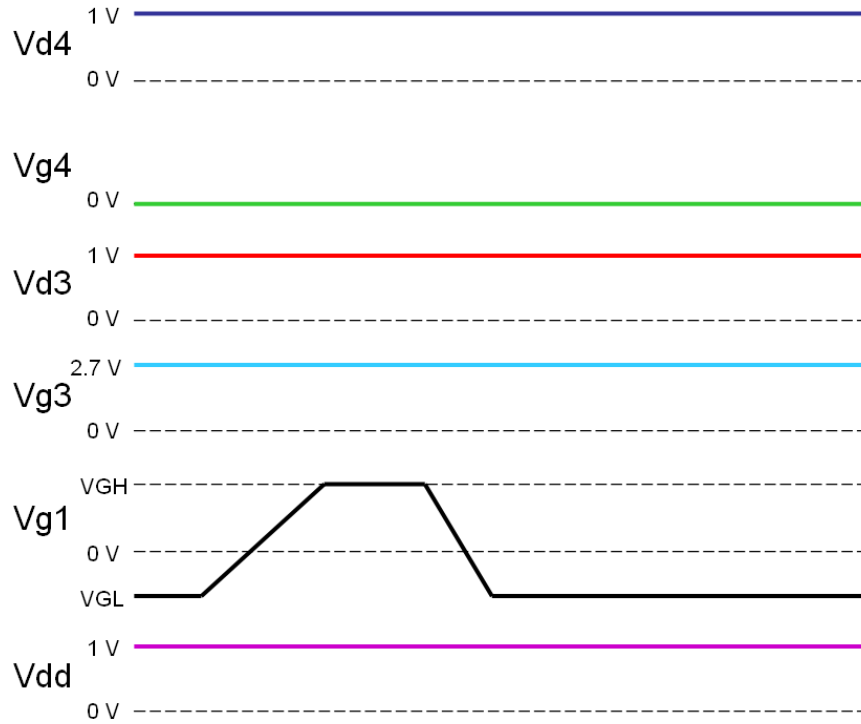
Figure 6.5 Voltages applied to the circuit to measure charge injection and clock feedthrough. All voltages except for Vg1 are provided by DC power supplies. The signal for Vg1 is provided by a pulse generator and has a rise time of 200 ns, fall time of 50 ns, period of 10 ms, and pulse width of 5 ms.

As mentioned earlier, since the focus of the measurements is charge injection and clock feedthrough in a switched-capacitor circuit, C0 acts as the sampling capacitor. Vg4 is 0 V to turn off M4 and transform C0 into a floating capacitor. Vg3 is 2.7 V to turn on M3 and Vd3 is 1 V to ensure that C1 is fixed at 1 V at all times. Vdd is 1 V to provide proper biasing to the source followers M0 and M2. All voltages except for Vg1 are provided by DC power supplies. Vg1 is provided by a pulse generator to turn M1 on and off and induce charge injection/clock feedthrough. The signal for Vg1 has a rise and fall time of

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200 and 50 ns respectively, period of 10 ms, and pulse width of 5 ms. The high and low levels are varied to explore their effects.

6.3   Measurement Results

This section discusses the charge injection and clock feedthrough measurement results. The effects of VGH, VGL, and transistor length are measured to compare against the calculated and simulated results.

6.3.1   Gate High Level Voltage

In order to examine the effect of VGH, the gate is turned off with VGH values ranging from 3 to 2.5 V. A transistor with W/L = 0.4 µm/1.0 µm has the gate ramping from various VGH values down to -200 mV with Tfall of 50 ns. The effect of VGH is shown in Figure 6.6, which plots error voltage as a function of VGH.
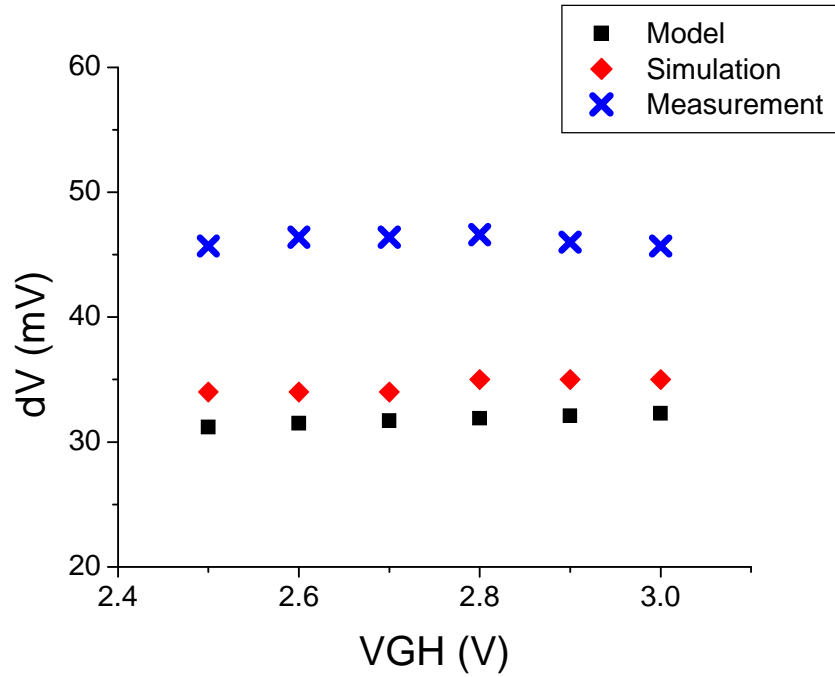
Figure 6.6 Error voltage as a function of VGH. The gate voltage decreases with VGH values of 3, 2.9, 2.8, 2.7, 2.6, and 2.5 V. The gate voltage ends at -200 mV and has a Tfall value of 50 ns.

The calculations, simulations, and measurements all show that VGH has little effect on error voltage, assuming the transistor is operating in strong inversion. The model and simulations show that error voltage decreases with VGH at rates of 2.1 and 2.6 mV/V, respectively. It is difficult however, to extract a relationship in the measured data due to measurement noise. It can be seen from Figure 6.6 that the model and simulations demonstrate good agreement. The error voltage from simulations is approximately 10% higher than the calculations. The measurements on the other hand, are approximately 45% higher than the calculations. Causes for the discrepancy between the model,

simulations, and measurements are likely due to differences in channel charge, source-drain conduction, and total source capacitance.

6.3.2 Gate Low Level Voltage

The gate voltage of a transistor with W/L = 0.4 µm/1.0 µm decreases from 3 V to VGL values ranging from 0 to -0.5 V. A Tfall value of 50 ns is selected to turn off the transistor. The effect of VGL is shown in Figure 6.7, which plots error voltage as a function of VGL.
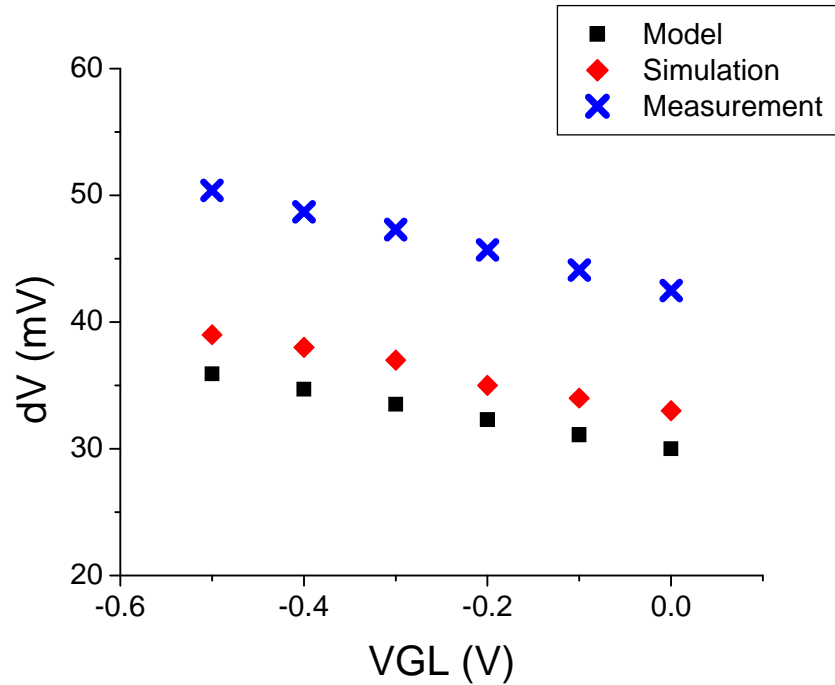
Figure 6.7 Error voltage as a function of VGL. The gate voltage decreases from 3 V to VGL values of 0, -0.1, -0.2, -0.3, -0.4, and -0.5 V. A Tfall value of 50 ns is selected to turn off the transistor.

The calculations, simulations, and measurements all show that decreasing VGL increases error voltage because of clock feedthrough. The model, simulations, and measurements

show that error voltage changes with VGL at rates of 11.9, 12.6, and 15.7 mV/V, respectively. Causes for the rate discrepancy between the model, simulations, and measurements are due to differences in gate-source and total source capacitances. These differences would affect the voltage divider ratio.

6.3.3 Transistor Length

NMOS transistors with width of 0.4 μm and lengths of 0.3, 0.4, 0.6, and 1.0 μm are measured to examine the effect of length on charge injection and clock feedthrough. The gate is turned off from 3 V to -200 mV with Tfall of 50 ns. Figure 6.8 plots error voltage as a function of transistor length for the model, simulations, and measurements.
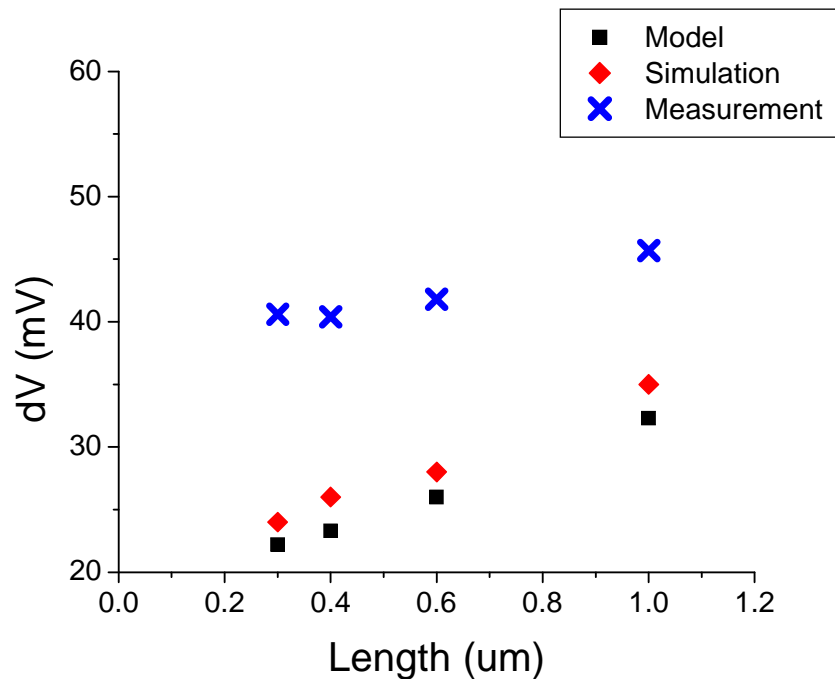
Figure 6.8 Error voltage as a function of transistor length. The gate voltage decreases from 3 V to -200 mV with a Tfall value of 50 ns.

The calculations, simulations, and measurements all show that increasing transistor length increases error voltage. The model and simulations show that error voltage increases with length at rates of 14.6 and 15.4 mV/μm, respectively. Although the linear fit in the measured data is not as great, measurements show a rate of 7.8 mV/μm. Causes for the lesser fit quality in the measured data are likely due to variations in total source capacitance and poly gate critical dimension (CD).

Comparing the calculated, simulated, and measured data shows that there is good qualitative agreement on the effect of various parameters on charge injection and clock feedthrough. The model and simulations especially show excellent quantitative and qualitative agreement.

7 Conclusion

The work presented in this thesis examined charge injection and clock feedthrough by developing a model and verifying it through simulations and test structure measurements. It is important to understand the mechanisms of charge injection and clock feedthrough because they limit the performance of switched-capacitor circuits, which form ADCs, DACs, and CMOS image sensor pixels.

A basic charge injection/clock feedthrough model was developed to identify the components that contribute to this phenomenon. In the model, the switched-capacitor circuit had an NMOS transistor's drain connected to a low impedance voltage source and the source connected to a sampling capacitor. When the transistor turns off, charge injection occurs because channel charge is dispersed into the source and drain. Clock feedthrough also occurs due to the coupling through gate-diffusion overlap capacitance. The combination of both mechanisms reduces the voltage on the sampling capacitor. The third mechanism, source-drain conduction, allows for voltage recovery until the transistor reaches sub-threshold condition. Our model reiterated the predominant interaction between charge injection and source-drain conduction when the gate voltage is above the threshold condition and the dominance of clock feedthrough when the gate is in sub-threshold. The model was useful in examining source voltage as a function of both time and gate voltage.

The model we developed was verified and expanded upon by using Synopsys TCAD simulations. TCAD simulations predicted how charge injection and clock

feedthrough are affected by various parameters, such as transistor operation, size, and geometry. 2D simulations were setup to examine the effect of transistor length, VGH, VGL, and Tfall. The simulation flow included process simulation, structure editing, device simulation, and electrical parameter extraction. 3D simulations were setup to understand the effect of transistor width and three-dimensional geometry, such as the annular and funnel-shaped transistors.

The simulation results verified our model by showing similar components of dispersal of channel charge, coupling through overlap capacitance, and source-drain conduction. By analyzing the dependence of charge injection and clock feedthrough on various parameters, it was determined that some parameters had an effect while others did not. In terms of transistor operation, VGH had little effect, while decreasing VGL or Tfall increased the error voltage. In terms of transistor size, increasing the width or length increased the error voltage. After comparing the standard, funnel, and annular transistors, it was shown that those different transistor geometries had little effect on charge injection and clock feedthrough.

Test structures were designed and fabricated in a 0.18 µm CMOS process to measure and verify charge injection and clock feedthrough. The test structure was designed with various transistor lengths to examine the effect of length. Measurements were performed to examine the effect of VGH, VGL, and transistor length. In all three measurement types, there was good trend agreement between the model, simulations, and measurements. The model and simulations showed good quantitative agreement, with simulations predicting error voltage to be approximately 10% higher than the

calculations. The measurements however, were approximately 45% higher than the

calculations. Causes for the discrepancy between the model, simulations, and

measurements were due to differences in channel charge, source-drain conduction, total

source capacitance, and measurement noise.

Further study can be carried out to verify charge injection and clock feedthrough

by designing and measuring more test structures. Due to limitations with lab equipment,

the effect of Tfall could not be measured. The lab limitations also resulted in a transistor

length effect that had a poor linear fit. Repeating the measurements with various lengths

would be important to verify that the length effect is indeed linear. Additional test

structures could also be created to verify the effects of width and transistor geometry.

Any further study in measuring charge injection and clock feedthrough would be

beneficial in verifying our model and simulations.

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