June 2010

CMOS090 SPICE MODELS DOCUMENTATION

CSMBE MODEL CARD

MODELING TEAM

CONTENTS

FIGURES INDEX

OVERVIEW

The Cmsbe device model is a physical model of a plate stacked capacitor. The results of Quickcap[1] simulations (or measurements) are used to calculate the specific and fringe capacitance between two consecutive metal layers. The capacitance value between two consecutive layers is calculated using the expression:

$$C = ca \times Area + cf0 \times Perimeter \qquad (1)$$

taking into account parsitic capacitance contributions due to access parts of the device[2].

The capacitive effect is mainly vertical. Compared to the equivalent device in the cmos065 technology kit product (Cstrip), the metal plates are not striped.

❑ Pins

This device has two pins (plus and minus). PLUS pin is always surrounded by an upper and a lower array (MINUS Pin) in upper and lower metal layers: consequently the number of metal layers required for this device is always an odd number (3 or 5). These metal layers can be:

- M1 (if bottom layer is Metal1)

- Thin metal (type X) layers available in the corresponding process option. This device does not involve thick metal layers.

plus = plus (used as signal pin, it is the intermediate metal level)

minus = minus (shield around the plus pin, it is the top-layer and bottom-layer levels)

❑ Model nomenclature

Cmsbe models are available only from metal1 to metal5 levels : M1-> M5

1. QuickCap is a parasitic capacitance extraction tool. It is used in applications that demand high 3D-extraction accuracy, such as process analysis, library cell characterization, parameter extraction and modeling, correlation studies, critical block design, and critical net analysis. QuickCap provides the high accuracy parasitic data required for accurate delay and signal integrity analysis, verification, and post-layout simulation.
2. See figure 3.

Cmsbe 2 pin capacitor model name is: **cmsbe** (for Capacitor Metal StacKed Back End).

The device instantiation includes the right configuration of metals used to perform the capacitor: bottom metal to top metal (only thin metal is used). It is important to inform the model about the right metal configuration: capacitance value depends on it.

DEVICE INSTANTIATION PARAMETERS

❑ Model CALL for the 2 pin Stacked plate Capacitor:

Xname **Plus_Pin** **Minus_Pin** **ModelName** carea=**capacitor_area** cperi=**capacitor_perimeter** botlayer=**bottom_layer** toplayer=**top_layer** mismatch=**mismatch_flag** mult=**MULT_value** lpe=**LPE_Value** tometer=**microns_to_meter** c=**capacitance_value**[1]

Plus_Pin	is the first capacitor terminal
Minus_Pin	is the second capacitor terminal
ModelName	cmsbe (string)
carea	is the desired PLUS layer area of the capacitor (float)
cperi	is the desired perimeter of the PLUS layer of the capacitor (see figure 2) (float)
botlayer	bottom metal layer used for the device (1, 2 or 3)
toplayer	top metal layer used for the device (3, 4 or 5)
mismatch	flag: to activate the mismatch effect for the device (0=disable, 1=enable)
mult	is the multiplication factor (parallel devices)
lpe	flag: is a user option to take into account the post-layout extraction mode (0,1, 2 or 3)
tometer	parameter used to transform distances in microns to meters unit (1 or 10e-6)
c	capacitance value (not used in the model)

1. The value specified here is not used in the model.

PCELL & LAYOUT

The layout of the plate stacked metal capacitor is a stack of 3 or 5 plate layers.

The plus plate (between two minus plates) is underlaped w.r.t the side of the minus plate in order to be insensitive against outside perturbations. Metal allowed for this capacitor are only metal 1 and thin metal (Metal X). Only odd number of metal layers are allowed.

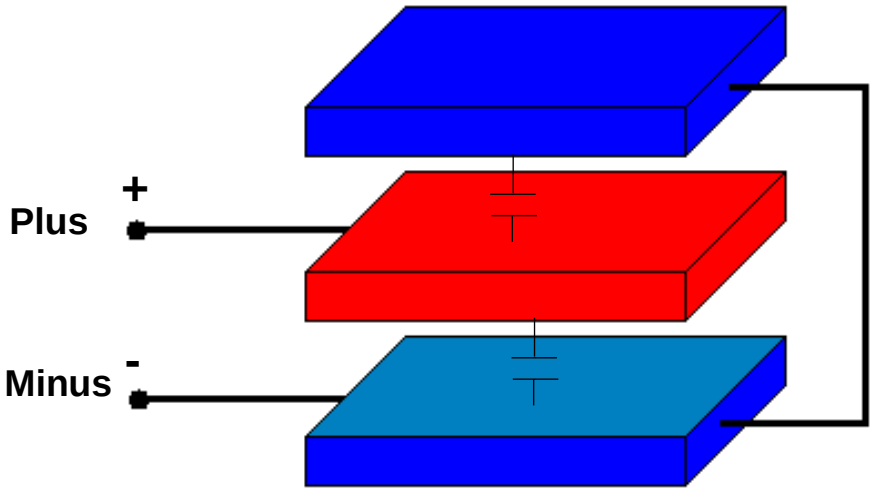

Figure 1 - 3D view of the core of cmsbe Pcell

The main capacitance is between the two terminals (Plus and Minus).

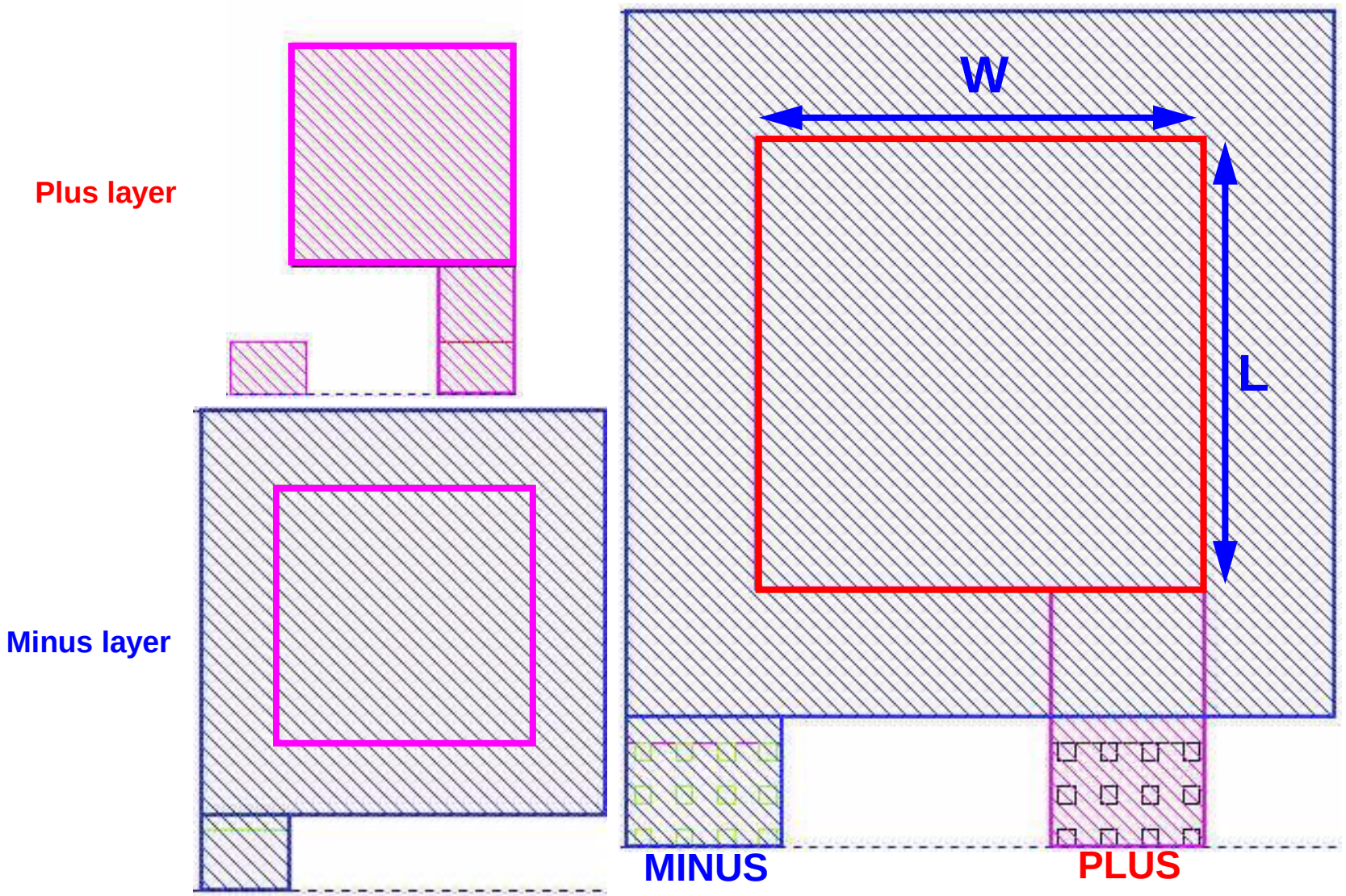

Figure 2 - Top view of cmsbe Pcell (Layout)

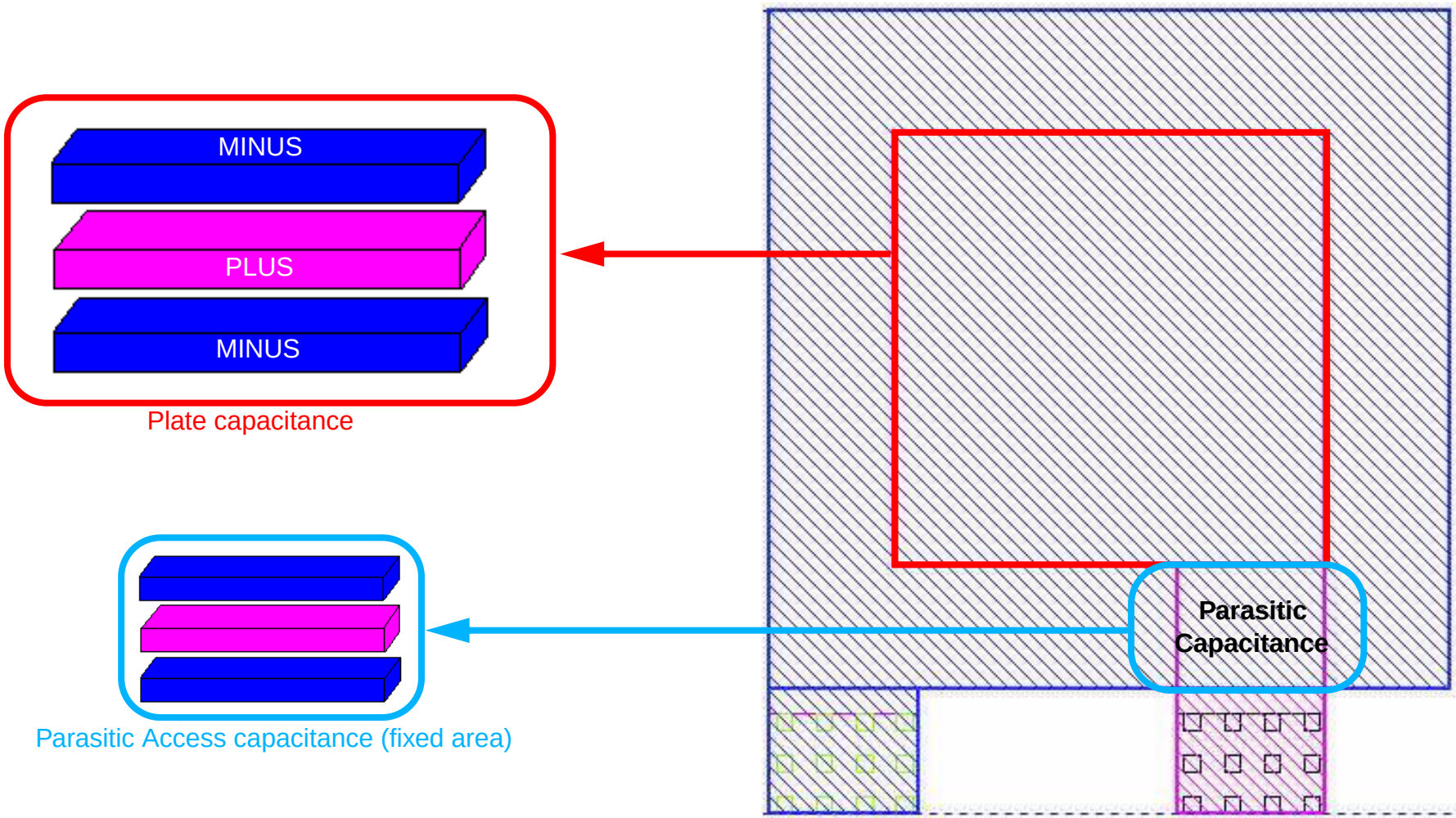

Figure 3 - Capacitance distribution

EQUIVALENT CIRCUIT SCHEMATICS

Capacitor model calculates the main capacitance which is accounted between the Plus/Minus terminals (Figure 1 and 3):

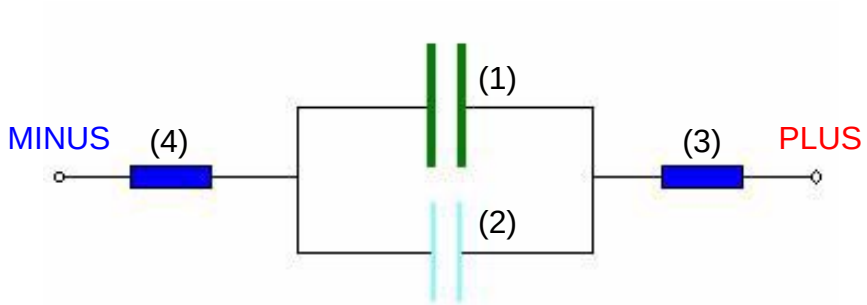

Figure 4 - Circuit diagram of cstrip device

- Cc (1): intrinsic (main) capacitor between the Plus/Minus terminals.
- Cap_para (2): parasitic capacitor between the plus and minus terminals due to acces to PLUS pin (see figure 3).

The model includes two series resistances:

rvalp (3): for the plus terminal. It takes into account the vias (VIA1X, VIA2X, VIA3X, VIA4X or VIA5X) and the metal levels resistance belonging to the plus layer.

rvalm (4): for the minus terminal. It takes into account the vias (VIA1X, VIA2X, VIA3X, VIA4X or VIA5X) and the metal levels resistance belonging to the minus layer.

CAPACITANCE CALCULATION

Capacitance value is written as (see figure 3):

$$\text{Capacitance} = n \times \text{Cm1mx} + m \times \text{Cmxmx} \qquad (3)$$

where:

n : is a number of m1-mx elementary vertical capacitors in a stacked device (0 or 1)

m : is a number of mx-mx elementary vertical capacitors in a stacked device (1, 2 or 3)

$$\text{Cm1mx} = \text{C1xplate} + \text{Cap1x\_para}$$

$$\text{Cmxmx} = \text{Cxxplate} + \text{Capxx\_para}$$

where:

C1xplate (Cxxplate) : main capacitance value of the plate layer (see figures 1 and 3)

$$\text{C1xplate} = \text{ca} \times \text{Area} + \text{cf0} \times \text{Perimeter}$$

Cap1x_para (Capxx_para) : capacitance value (fixed) of parasitic access (see figure 3)

$$\text{Cap1x\_para} = \text{ca} \times \text{Fixed\_Area} + \text{cf0} \times \text{Fixed\_Perimeter}$$

MODELED EFFECTS

GEOMETRY SCALING

The capacitance value of the device is calculated using the equation number 3. Its variation versus area for square shape[1] is shown in figure below:

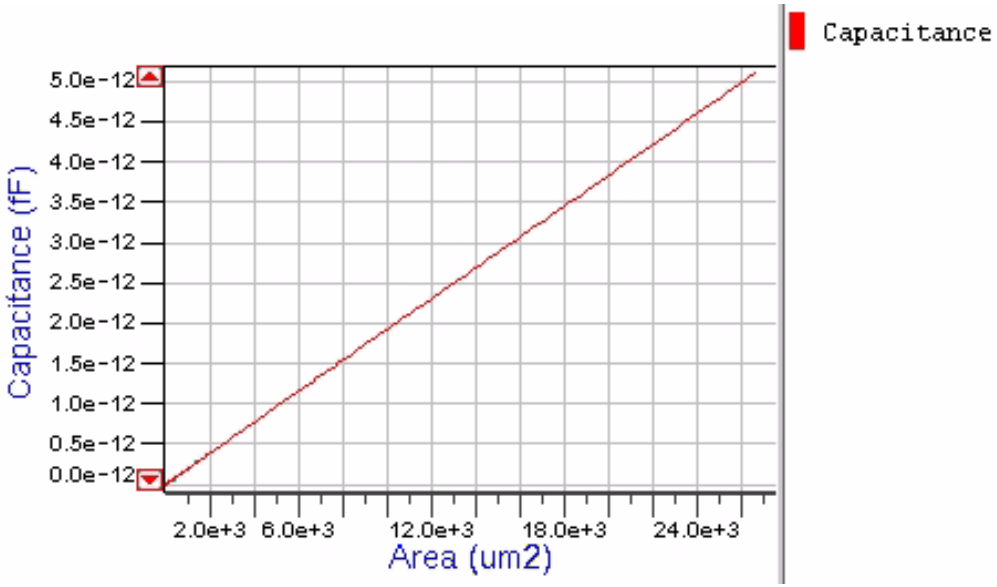

Figure 5 - Capacitance value versus Area (square capacitor)

Variation of specific capacitance for same geometry is shown in figure below:

1. Three metal levels are used in this simulation (M1-M3) Area = parameter *parameter and Perimeter = 4*parameter

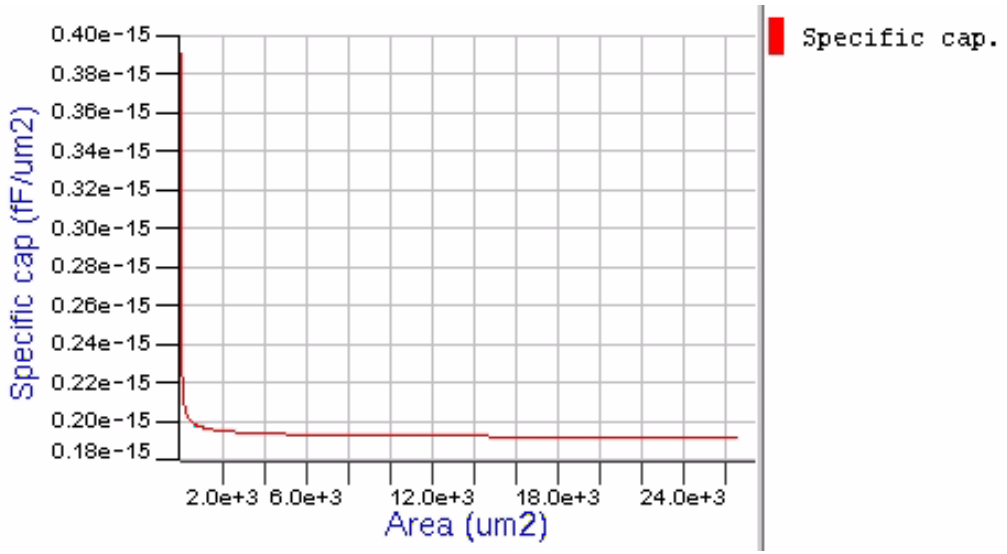

Figure 6 - Specific capacitance versus Area (square capacitor)

MISMATCH MODEL

A normal distribution is used to estimate the expected main capacitance value:

$$\text{Capacitance} = c0 \times (1 + \varepsilon)$$

where

- c0 : is the mean capacitance value given by the equation (3)
- ε : is a normal distribution with a standard deviation given by:

$$\sigma = \frac{c\_A}{\sqrt{2 \times c0}}$$

where

c_A : is the mismatch coefficient given by measurement values.

When c_A parameter is not specified no distribution is used and capacitance value is equal to c0.

The normal distribution is provided using the Eldo function: gauss

$$\varepsilon = 0 \qquad dev/gauss = 'fudge \times c\_A/(\sqrt{2 \times c0})'$$

where

fudge is a security parameter. It is used to be sure that the capacitance range covers measurements.

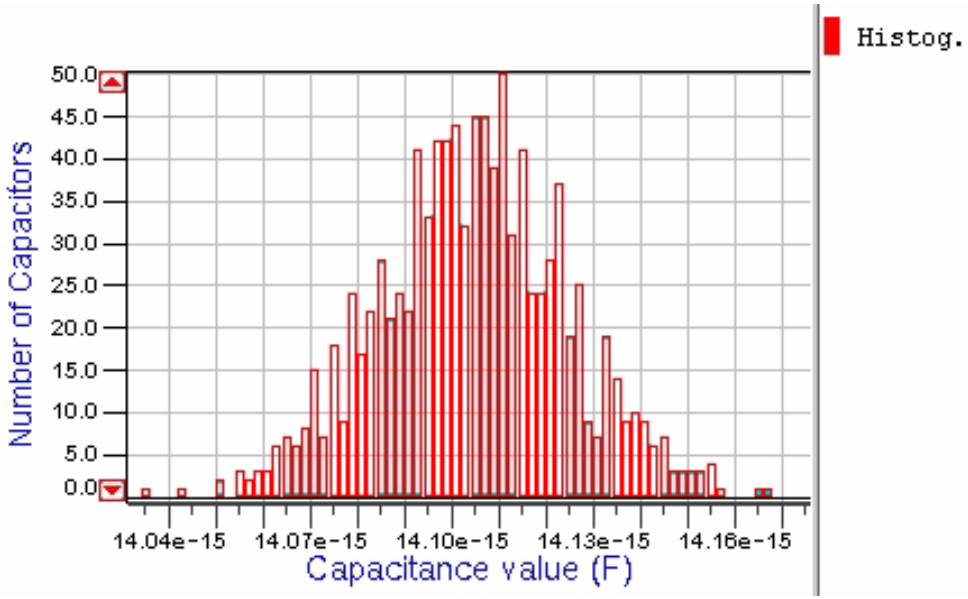

Figure 7 - Number of capacitors out of 1000 versus capacitance value

Example above is done for one cmsbe capacitor (Area = 64 ; Perimeter = 32 using 3 metal levels M1-M3) simulation gives roughly: 14.104fF as capacitance value.

Relative[1] Standard Deviation specified: 1.411M

Relative Standard Deviation simulated (1000 random selection using a Monte Carlo Analysis): 1.410M

1. Standard deviation = Relative Standard deviation * Capacitance value.

PARASITIC COMPONENTS

- **Series Resistors:**

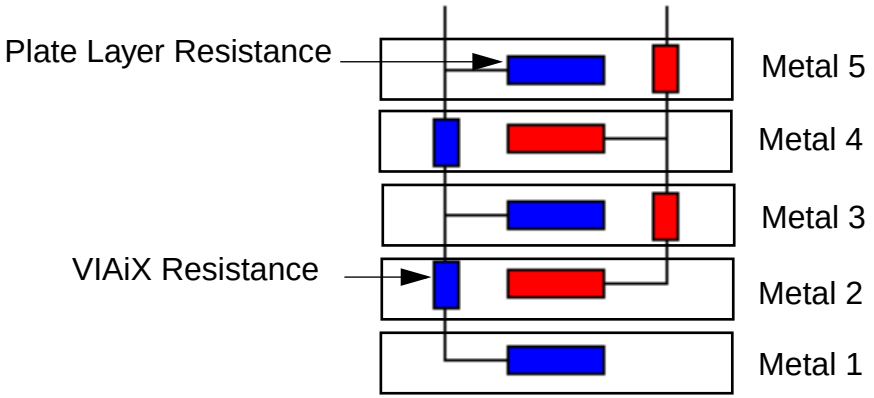

Figure 8 - Parasitic Resistors configuration for Pins: PLUS and MINUS

Plate Layer resistance: is the equivalent resistance of all one level layer

POST LAYOUT SIMULATION

The cmsbe model is managed by the LPE flag option, which permits to select the Resistor/Capacitor access modeling mode. See the following table depicting the proposed options :

LPE	Body	Access_R	Access_C	Extraction_mode
0	yes	yes	yes	--
1	yes	yes	no	C
2	yes	no	yes	R
3	yes	no	no	RC

The Front-End Model (F-E) :

cmsbe, a complete model which contains intrinsic and parasitic capacitances (between the Plus/Minus terminals) and parasitic series resistances (LPE=0).

The Back-End Model (B-E) :

The **cmsbe** B-E model is identical to the **cmsbe** F-E model concerning the main capacitance (LPE=1,2 or 3 according to the user choice) but it excludes parasitic resistors (LPE=2, 3).

CORNERS CONSTRUCTION

❑ Design Rule Manual parameters

rsq_M1_l, rsq_M2_5_l and rviax parameter corners are given by DRM

❑ Simulation parameters

Model coefficients ca1x, caxx, cf01x and cf0xx are extracted using Quickcap simulations (or measurements) and the expressions below:

$$C\_TYP = ca\_TYP \times Area + cf0\_TYP \times Perimeter$$

$$C\_MAX = ca\_MAX \times Area + cf0\_MAX \times Perimeter$$

$$C\_MIN = ca\_MIN \times Area + cf0\_MIN \times Perimeter$$

Figure below shows capacitance corners versus area. This result depends on the construction of MAX and MIN corners.

Simulations are done for a square cmsbe capacitor: L=W=2µm -> L=W=163µm

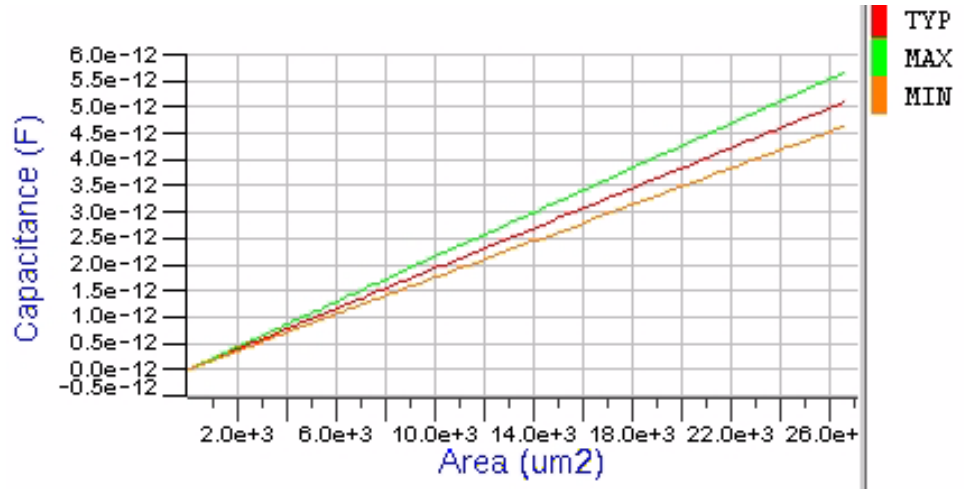

Figure 9 - Example of capacitance corners simulation (MAX and MIN)

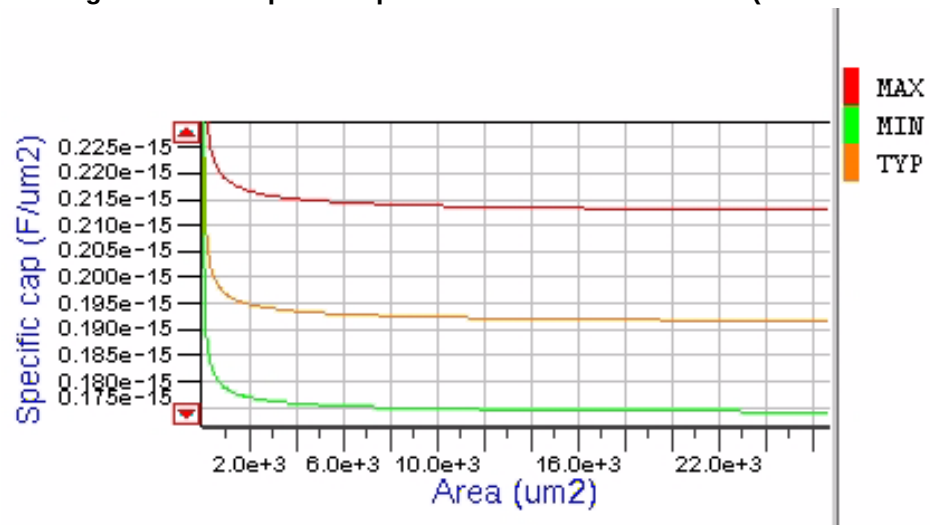

Figure 10 - Example of specific capacitance corners simulation (MAX and MIN)

MODEL PARAMETER LIST

careamin	(m2) Area min=lmin*wmin
careamax	(m2) Area max=lmax*wmax
careadef	(m2) Area def=ldef*wdef
cperimin	(m) Perm. mini= 2*(lmin+wmin)
cperimax	(m) Perim max= 2*(lmax+wmax)
cperidef	(m) Perim def= 2*(ldef+wdef)
wmin	(m) Minimal Width (Pcell)
wmax	(m) Maximal Width (square: 10pF)
wdef	(m) Width def (square: 100fF)
lmin	(m) Minimal Length doc1 (MiX.A.2)
lmax	(m) Maximal Length (10pF)
ldef	(m) Length def (square: 100fF)
wpar	(m) Width of parasitic block
lpar	(m) Length of parasitic block
nvia	() Number of contact vias
cdef	() botlayer=1 and toplayer=5
c_A	(sqrt(F)) for cap. mismatch
fudge	() Security parameter used to cover measurements
overlap	(m) Overlap between Plus and Minus layers (1µm in default)

ca1x	(F/m2) Specific capacitance (m1-mx)
caxx	(F/m2) Specific capacitance (mx-mx)
cf01x	(F/m) Fringe capacitance (m1-mx)
cf0xx	(F/m) Fringe capacitance (mx-mx)
rviax	(ohm) Rvia unit resistance X type
rsq_M1_l	(ohm/square) sheet Resistance of M1 (large W)
rsq_M2_5_l	(ohm/square) sheet Resistance of metals M2 to M5 (large W)
dw	(m) Width Offset
dl	(m) Length offset