DESIGN OF A HIGH-SPEED CMOS COMPARATOR

Master Thesis in Electronics System at
Linköping Institute of Technology
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Abstract

This master thesis describes the design of high-speed latched comparator with 6-bit resolution, full scale voltage of 1.6 V and the sampling frequency of 250 MHz. The comparator is designed in a 0.35 µm CMOS process with a supply voltage of 3.3 V.

The comparator is designed for time-interleaved bandpass sigma-delta ADC. Due to the nature of the target application, it should be possible to turn off the components to avoid the static power consumption. The comparator of this design implements the turn off technique when it is not in use. The settling time of the comparator is less than half the clock cycle which means it does not effect the functionality of the bandpass sigma-delta ADC in terms of speed.

The simulation results are derived using Cadence environment. The results show that the comparator has 6-bit resolution and power consumption of 4.13 mW for the worst-case frequency of 250 MHz. It fulfills all the performance requirements, most of them with large margins.

Keywords
Comparator, CMOS comparator, Sigma-delta ADC, Low power design, High-speed.

ABSTRACT

This master thesis describes the design of high-speed latched comparator with 6-bit resolution, full scale voltage of 1.6 V and the sampling frequency of 250 MHz. The comparator is designed in a 0.35 μm CMOS process with a supply voltage of 3.3 V.

The comparator is designed for time-interleaved bandpass sigma-delta ADC. Due to the nature of the target application, it should be possible to turn off the components to avoid the static power consumption. The comparator of this design implements the turn off technique when it is not in use. The settling time of the comparator is less than half the clock cycle which means it does not effect the functionality of the bandpass sigma-delta ADC in terms of speed.

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INTRODUCTION

This thesis presents the basic topologies, design decision and the theory needed to understand the latched comparator design issues and considerations. The purpose of this project is to design a latched comparator for single bit time-interleaved bandpass sigma-delta ADC in 0.35 µm process.

The main design consideration was the comparator speed and turn off technique when it is not in use. This is because the target application is supposed to be used for a band of different frequencies at a time and the components which are not in use should be turned off to avoid the static power consumption.

1.1 General information

A comparator, by definition is "a circuit that compares the two analog input signals and decodes the difference into a single digital output signal". Figure 1.1 shows the comparator symbol, where out is the single digital output as a result of comparison of two analog inputs in1 and in2.

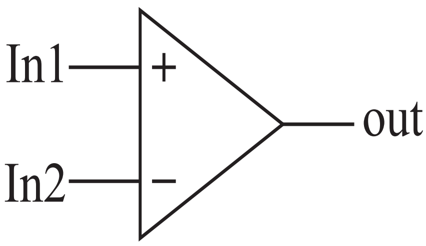

Figure 1.1: Comparator symbol.

The comparator is a critical part of almost all kind of analog-to-digital (ADC) converters. Depending on the type and architecture of the comparator, the comparator can have significant impact on the performance of the target application. The speed and resolution of an ADC is directly affected by the comparator input offset voltage, the delay and input signal range [4].

Depending on the nature, functionality and inputs, comparators are classified into different types i.e. voltage and current comparators, continuous and discrete time comparators etc. Some basic applications of comparators are analog-to-digital conversion, function generation, signal detection and neural networks etc.

1.2 Background

Due to the many comparator applications, researchers have designed and presented different architectures to fulfill the requirements. The following study gives an overview of some of the different comparator topologies examined during the pre-study. The outcome of the pre-study yields information, which topology to use.

1.2.1 A high-speed CMOS comparator with 8-bit resolution

A high-speed CMOS comparator is shown in figure 1.2. The comparator consists of three blocks, an input stage, a flip-flop and SR latch. The architecture uses two non-overlapping clocks ($\phi 1$ and $\phi 2$). The circuit operates in two modes, reset mode during $\phi 2$ and regeneration mode during $\phi 1$. During reset mode the inputs voltage difference is established at node A and B [1]. The regeneration happens during a short time when $\phi 1$ is rising and $\phi 2$ is falling. At the end of regeneration process the SR latch is driven to the digital output levels.

The design was implemented in a 1.5 µm CMOS technology operating at a ±2.5 V power supply with 8-bit of resolution and input range of 2.5 V [1]. At sampling rate of 65 MHz the chip exhibit offset voltage of 3.3 mV and a sensitivity 1.5 mV. At 65 MHz clock rate and input signal of 32.5 MHz, the comparator has total power consumption of 0.85 mW [1].

The design is appealing in context of power consumption, however it does not fulfill the requirements for this thesis work in term of speed.

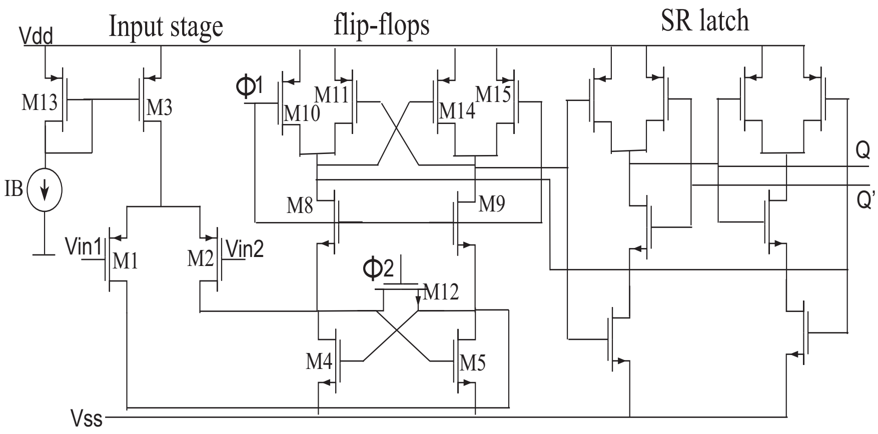

Figure 1.2: A high-speed CMOS comparator with 8-bit resolution.

1.2.2 A 6-bit 1 GHz acquisition speed CMOS flash ADC with digital error correction

Figure 1.3 shows the schematic of one of the 63 slices of the flash ADC with digital error correction. The comparator in figure 1.3 is designed for a 6-bit ADC converter. It consists of three parts, pre-amplifier, comparator and the nand-gate. The pre-amplifier at the comparator inputs consists of a differential amplifier with resistances as load. The pre-amplifier is used to reduce the input offset and kickback noise. The pre-amplifier amplifies the difference between input voltage and the reference voltage generated by the resistive ladder of the ADC [2].

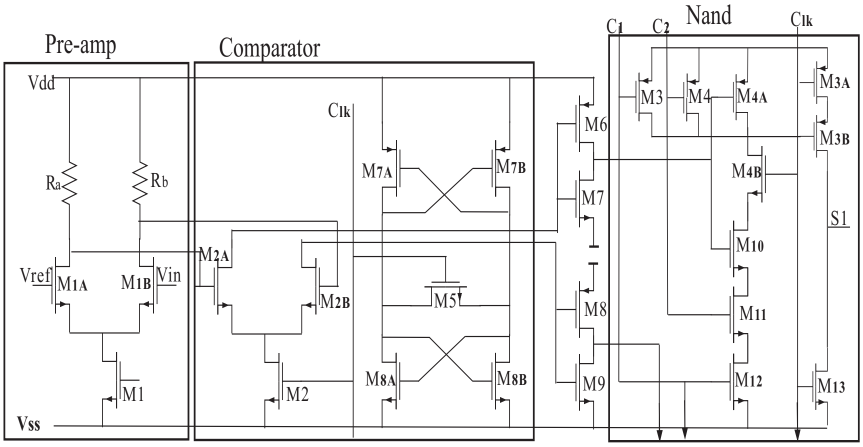

Figure 1.3: A 6-bit 1 GHz acquisition speed CMOS flash ADC slice schematic.

After the pre-amplifier the comparator generates the digital logic levels from the amplified inputs difference. During one clock phase, the regeneration nodes are charged proportionally to the amplifier outputs. In the next phase the voltage imbalance is amplified by the regeneration loop of the NMOSs and the PMOSs to digital levels. Using this architecture in an ADC with moderate resolution, a sample-and-hold circuit is not required [2].The nand gate at the end is used to select one of the 63 ROM-lines.

This architecture has been implemented in a 0.35 µm technology with 3.3 V power supply. The total power consumption (all the 63 slices of Flash ADC) of the pre-amplifier and comparator is 759 mW and digital part is 165 mW at input frequency of 141 kHz and 1 GHz sampling speed.

The power consumption of this architecture is very high. The single slice has the power consumption almost 12 mW which is considerable high for the comparator design of this thesis work.

1.2.3 A 0.35 µm CMOS comparator circuit for high-speed ADC applications

The comparator of the topology shown in figure 1.4 is used for high-speed ADC applications. It consists of a pre-amplifier, a latch and output sampler. The pre-amplifier shown in figure 1.4 has PMOS transistors as differential input pairs. One reason to use the PMOSs here is that the DC input is low. The output of pre-amplifier is mirrored to the latch.

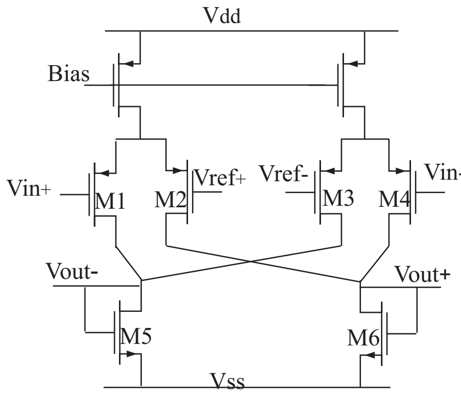

Figure 1.4: The schematic of pre-amplifier of CMOS comparator circuit for high speed ADC applications.

The latch consists of the cross coupled inverters connected to the ground through the clock as shown in figure 1.5. The latch operates in two modes, reset and evaluation, respectively. During reset phase, the latch output voltage is in the middle of the power supply rail voltages, which give a short regeneration time. The latch is activated during the evaluation phase (when the clock signal is high) and outputs are sampled before it goes to reset mode i.e. at the end of the evaluation phase.

The last part, the sampler, consists of a transmission gate and inverters as buffers. The transmission gate samples the latch during the evaluation phase and then the inverters amplifies the samples and buffers the outputs. The buffers keep the samples constant for a whole clock period, which relaxes the timing requirements, for the following stage (e.g. encoder) [3].

The comparator designed was fabricated in a 0.35 µm technology with a supply voltage of 3.3 V. The total power consumption of the comparator is 2 mW with 6 bit resolution at 1 GHz sampling frequency [3].

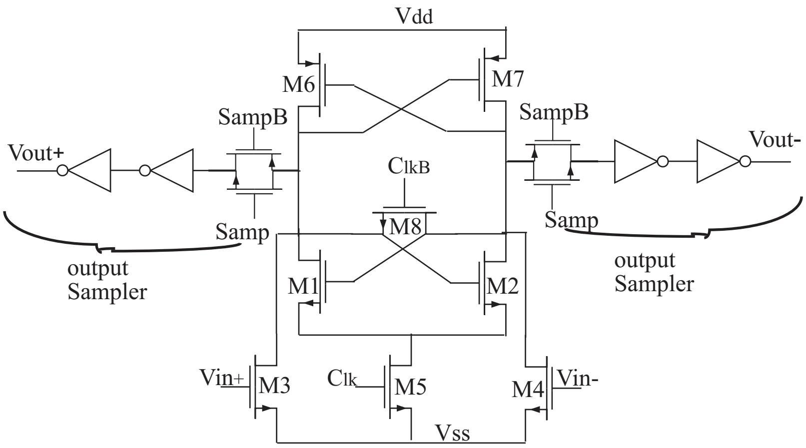

Figure 1.5: The schematic diagram of the latch part of CMOS comparator circuit for high speed ADC applications.

1.2.4 Performance analysis of optimized CMOS comparator

The comparator topology shown in figure 1.6 consists of two parts, CMOS latch circuit and S-R latch circuit. This design does not use a separate amplifier but the CMOS latch circuit does some amplification. I have selected this topology for my thesis work. One reason to select this topology is that the comparator does not use any separate amplifier and so the power consumption is less. I will discuss the design in more detail in chapter 3.

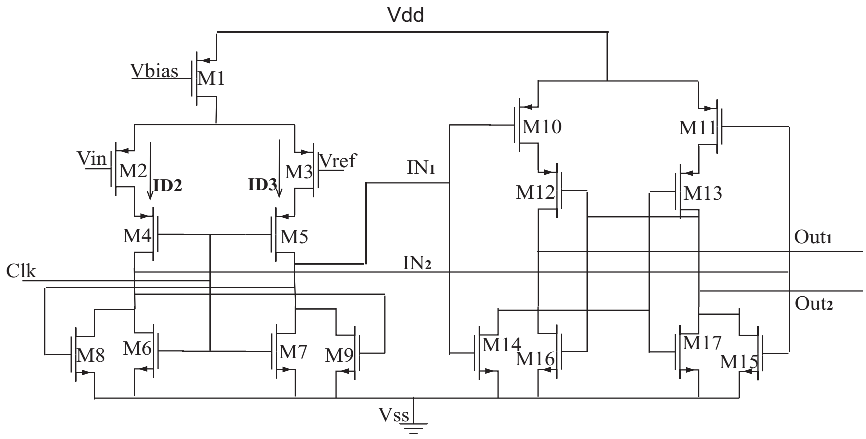

Figure 1.6: Performance analysis of optimized CMOS comparator.

The design operates at 2.5 V power supply at frequency of 500 MHz. At maximum sampling frequency, 500 MHz, the comparator achieves 10-bit resolution for 1 V differential with power consumption of 272 µW.

1.3 Scope of the work

The scope of this work is the design of a comparator for a time-interleaved bandpass Sigma-Delta ADC. The design is implemented in a 0.35 µm technology with 6-bits of resolution at a sampling frequency of 250 MHz. The main consideration is to minimize the power consumption and avoid the static power consumption by switching it off when it is not in use.

1.4 Outline

This thesis document is organized as in chapter 2 comparator related theory is presented along with some design issues used for this thesis work. Design details of the comparator and some performance measurements are discussed in chapter 3. The simulation results, conclusion and discussion are presented in chapter 4.

2

THEORY

This chapter gives the basic theory needed to understand the fundamental parts in comparator design. The purpose of this chapter is also to see how different components can contribute in comparator performance.

2.1 Pre-amplifier

The pre-amplifier is a circuit which is used to amplify the signal so that it can easily drive the load. In most latch comparator designs pre-amplifiers are also used to avoid the kickback effect from the latch and input referred offset [2].

The comparator design in this thesis work does not use a separate pre-amplifier but the CMOS latch performs the amplification. We will discuss more about the CMOS latch in chapter 3.

2.2 Comparator offset

Due to the mismatch between input transistors, the circuit exhibits a dc offset of different values. This value of dc offset depends on the mismatch of input and output voltages. The figure 2.1 shows a differential pair with perfect symmetry of input and output nodes, i.e. Vin =0 as well as Vout=0, hence the circuit has no offset error. On the other hand if the input is zero and output is not equal to zero, the circuit exhibits mismatch and suffers a dc offset. This dc offset is equal to the value of Vout when the input voltage (Vin) is zero, and is called the output referred offset.

The input-referred offset voltage can be defined as the input level which forces the output voltage to go to zero [6]. The offset can limit the performance of comparator and can make the system nonlinear. The precision

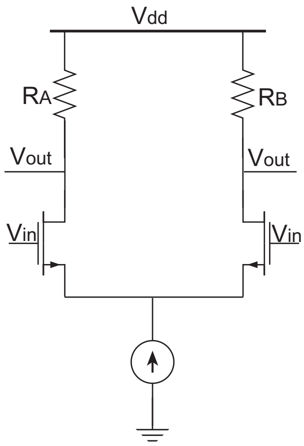

Figure 2.1: Differential pair with offset measured at the output.

of the comparator is also affected by the offset.

2.3 Kickback

During the regeneration process the latched comparator uses the positive feedback mechanism to scale the digital level. The voltage variations at the regeneration nodes are coupled to the inputs and disturb the input voltages. This disturbance is called the *kickback* noise. There are many solutions to this problem [7], a few techniques are discussed in chapter 2.3.1 through 2.4.4.

2.3.1 Sampling switches

A sampling circuit consists of a capacitor and switch (a MOS transistor) controlled by the clock. The sampling switch is placed before the comparator inputs. During the regeneration phase these switches are opened and disconnect the inputs from rest of the circuit [7]. The switches should be sized as small as possible compared to the total capacitances at the inputs to minimize the effect of charge injection [1].

2.3.2 Isolation transistors

Isolation transistors isolate the input differential pair from the regeneration process. Isolation transistors are usually a set of NMOS transistors controlled by the clock and placed between the drain of differential pair and regeneration outputs. During the regeneration phase the isolation transistors are switched off preventing the charge injection to the differential inputs. This technique results in low kickback noise.

2.3.3 Pre-amplifier

The pre-amplifier is the most commonly used solution placed in front of the comparator to reduce the kickback effect. The pre-amplifier also amplifies the input difference and reduce the input-referred offset[2]. The pre-amplifier may increase the gain and bandwidth of the system but power consumption is also increased.

2.3.4 Neutralization technique

This technique is used in the designs where differential inputs are directly connected to the regeneration nodes. Due to the non zero impedance of the circuit preceding the comparator, the inputs of the comparator are disturbed by the drain voltage variations of the differential pair. By adding the two capacitances between the gate and drain of the differential pair, as shown in figure 3.7, with a value equal to the Cgd of the differential pair will cancel the kickback noise [7]. This technique is further discussed in detail in chapter 3.

2.4 Parasitics

The parasitics play a critical role in analog designs. The ac behavior of the MOSFET is crucially effected of parasitics. The figure 2.2 shows a simple model to illustrate the parasitics of a MOSFET.

Between every two of four nodes of MOSFET, there exists a capacitance. The capacitance depends upon the gate voltage and it changes values according to the region of operations. The capacitances are; overlap capacitance between gate and source/drain, depletion capacitance between channel and substrate, oxide capacitance between gate and channel and junction capacitance

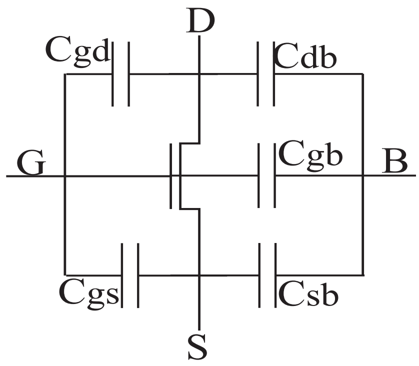

Figure 2.2: MOSFET parasitics capacitances.

between source/drain and substrate.

2.5 Metastability

Normally in all latching comparators metastability is a problem which occurs when the input is near the comparator decision point [9].

Comparator metastability occurs when very small signals appear at the input of a comparator close to the comparator decision point. Normally all kind of latching comparators exhibit this problem [9]. In such cases, the comparator is not able to make a decision, i.e latch its output to the stable point, within the allotted time. This metastability delay is random and could switch the output to the wrong logical levels which can cause system malfunction or failure. The figure 2.3 shows the voltage transfer characteristics of two back-to-back connected inverters. Each inverter has two stable points; Vdd or ground. The mid point where the two curves intercept each other is metastable point (MSP) as shown in the figure 2.3. Ideally the MSP of an inverter is at half of the input range i.e. Vdd/2. Now, if the input at the first inverter slightly deviates from Vdd/2, the output at the second inverter goes to one of the stable states. In this band of range the output is unpredictable and can switch to wrong logic level.

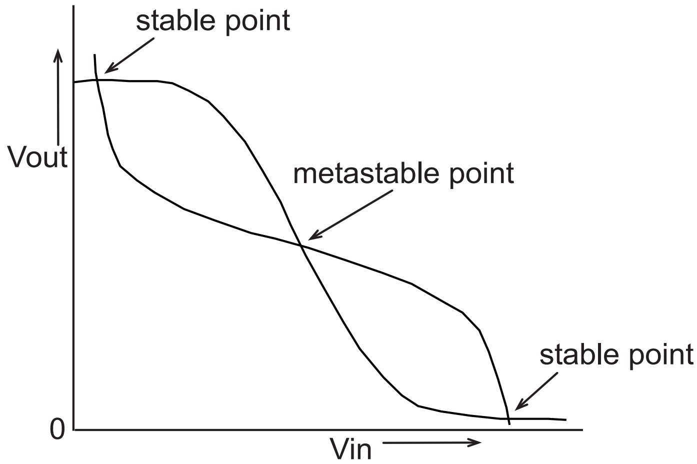

Figure 2.3: VTC of back-to-back connected two inverters.

3

DESIGN DETAILS

For this thesis work I have selected one of the topologies presented in chapter 1. The comparator design consists of two parts, the CMOS latch and SR latch as shown in the figure 3.1. There is no separate pre-amplifier in this design.

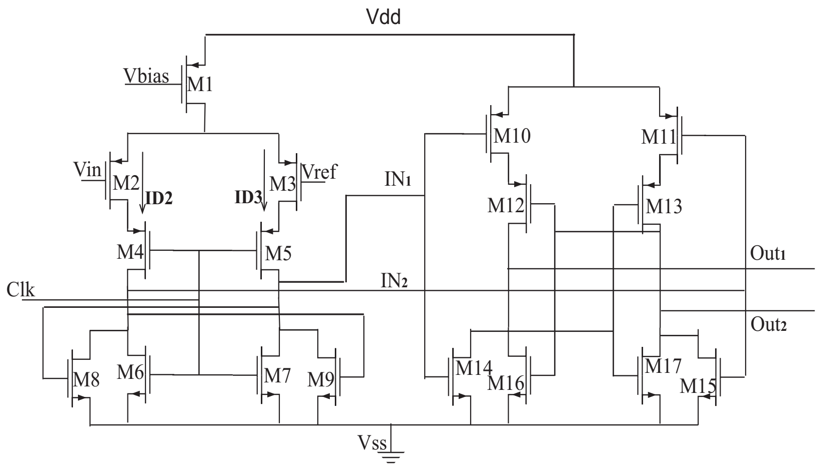

Figure 3.1: Comparator schematic

3.1 CMOS latch circuit

The CMOS latch circuit includes the biasing part, differential and regeneration part, as shown in figure 3.2, followed by the SR latch. The amplification is done by the PMOS differential pairs. In the following part we will discuss the CMOS design in more detail.

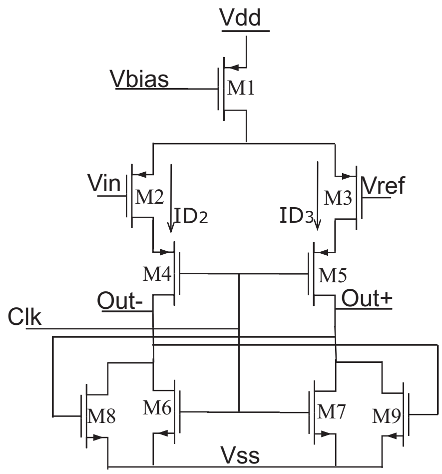

Figure 3.2: CMOS latch schematic.

3.1.1 Comparator Optimization

a) Transistors M1-M3

First, we will consider the PMOS differential pair [M1-M3]. As demonstrated in [5], the difference of current between differential and regenerations stage can be calculated as:

$$\Delta I = I_{D2} - I_{D3} = \frac{k}{2}\frac{W}{L}\Delta V \sqrt{\frac{4ID}{k\left(\frac{W}{L}\right)} - \Delta V^2} \tag{3.1}$$

From the equation 3.1, the PMOS transistors sizing can have significant effect on the comparator performance. Increasing the W/L ratio of PMOS transistors of differential pair{M1-M3} will produce the large ΔI [4]. If ΔI between differential pair and regeneration pair is large, it will cause either M8 or M9 to saturate for a small difference of input voltages (Vin and Vref). In this way the offset error can be reduced [4]. However if the ΔI is too large, NMOS transistors will not be able to drive the SR latch for noticeable time and SR latch will be disabled before the regeneration happens.

b) Transistors M4 & M5

PMOS transistors M4 and M5 are controlled by the clock and act as cascode device. Since the design does not use a separate pre-amplifier, these cascode transistors (also called isolation transistors) help to minimize the kickback effect by separating the inputs from the outputs during the regeneration process. These switches may limit the voltage swing and over load recovery.

c) Transistors M6 & M7

NMOS transistors M6 and M7 implement the switching transistors. The switching time of switching NMOS transistors is given by [8]

$$T_t = \frac{1}{f_t} = 2\pi \frac{V_t W L C_{js}}{I_D} \tag{3.2}$$

The equation 3.2 shows by decreasing the W/L ratio of switching transistors will increase the switching time and also speed up the regeneration process.

d) Transistors M8 & M9

NMOS transistors M8 and M9 implement a regeneration circuit [4]. The drain current of the two cross coupled NMOS transistors affect directly the SR latch as well as the regeneration process. If the W/L ratio of the NMOS transistors is too large, it will produce more drain current which yields fast regeneration. However too much drain current will discharge both nodes at the input of SR latch which will increase the offset voltage for proper operation [4].

3.2 SR Latch circuit

The SR latch is shown in figure 3.3. The basic function of the latch is to act as memory that keeps values for a whole clock period. It may also add some gain to the outputs. The latch provides an interface between analog and digital levels since the outputs of the comparator are digital. Otherwise if analog inputs are connected directly to the digital levels (the comparator outputs), the system becomes unstable. The digital levels can change quite much and can produce bounces even due to small noise spikes.

The ratio of PMOS and NMOS sizes effect the resolution as well as the gain of comparator. The SR latch in this design has optimum transistor values for good hysteresis calculation.

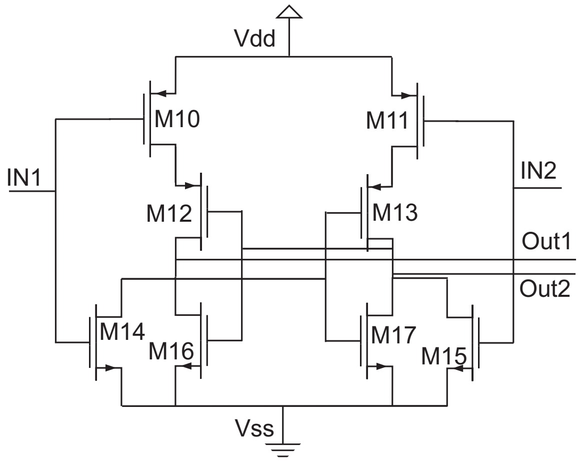

Figure 3.3: Schematic diagram of SR latch

3.3 Two phase operation

The comparator works in two phases, charging or amplification phase and re-generation phase during one cycle of comparison. Charging or amplification happens when the clock signal is low. During amplification phase the PMOS cascode pair or isolation transistors M4 and M5 turn on while the switching NMOS transistors M6 and M7 are disabled. Inputs are amplified and sampled at intermediate nodes (differential nodes).

During the period when clock is high, the NMOS switching transistors M6 & M7 turn on and regeneration occurs. The differential nodes are discharged to GND.

3.4 Gain and bandwidth of the comparator

The gain and bandwidth of the comparator depends on NMOS and PMOS transistors sizing as well as the biasing current to the comparator. By keeping the configuration, input DC voltage as 1.65 V and biasing current 200 μA, yield the following results. Gain is 5.9dB, -3dB cut-off frequency 731 MHz and unity gain frequency is 1.0 GHz.

3.5 Comparator turn off technique

Since the comparator is intended to be used in a time-interleaved bandpass sign-delta modulator, it is turned off when not in use to avoid the static power consumption. To turn off the comparator, two extra NMOS transistors are introduced as switches in the design as shown in the following figure 3.5. These NMOS switches are controlled by an external "enable" signal to turn "ON" and "OFF". If the enable signal is low i.e. 0, both transistor MT1 and MT2 turn off and disconnect the CMOS latch from biasing circuit and SR latch from GND. The comparator consumes almost no power when it is turned off.

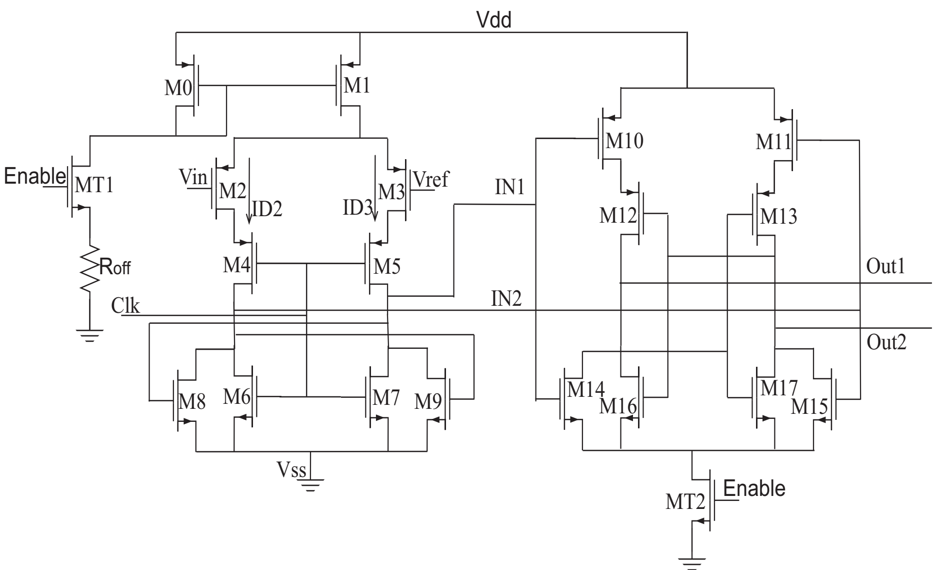

Figure 3.4: The comparator with turn off switches.

3.6 Settling time of the comparator

The settling time is the time the comparator takes to settle, after it is turned on, when the valid inputs are available at the input.

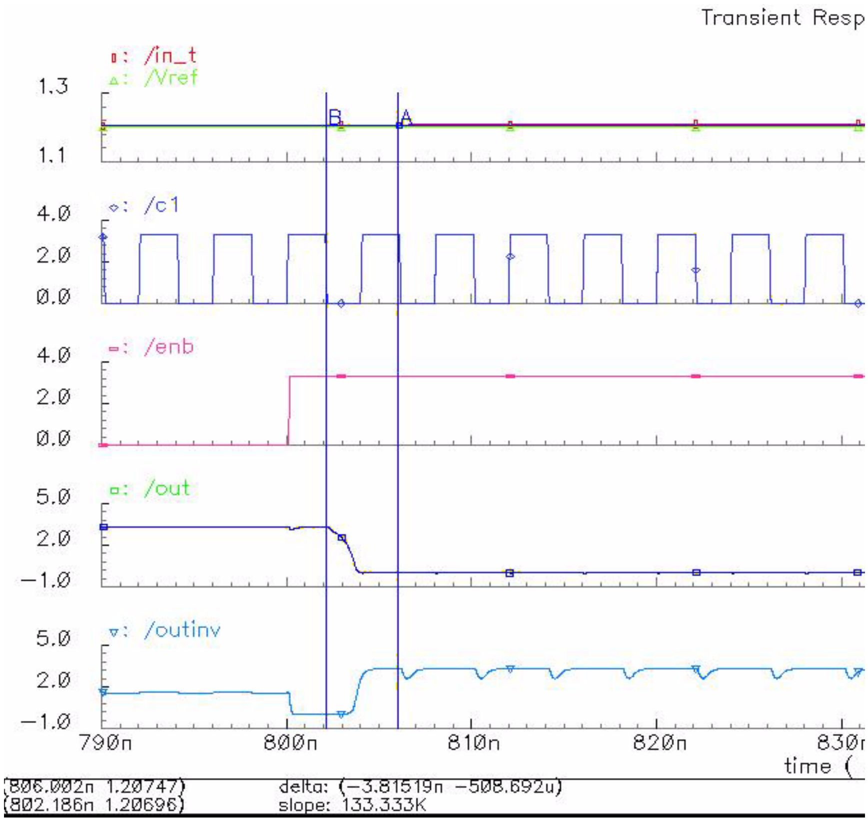

Figure 3.5: Settling time of the comparator.

The figure 3.6 shows the simulation waveform for the setting time of the comparator. The enable signal is turned on at the rising edge of clock. Since the inputs to the comparator are valid at this point, the comparator starts to work when the clock is high and gives the output at falling edge. Here, we can say that the settling time of the comparator is less than half the clock cycle.

3.7 Kickback noise

As discussed in chapter 2, the latched comparators use positive feedback mechanism for regeneration. The large variations on the regeneration nodes are coupled to the input of the comparator through the parasitic effect of transistors. Due to the large voltage variations at regeneration nodes, the comparator in this design uses isolation transistor to separate the differential pair from the regeneration nodes. The isolation transistors are clock enabled and disconnect the following part of circuit from the differential pair during the regeneration process.

Because of the large difference of the W/L ratio of isolation transistor and regeneration transistors, the comparator can have a kickback effect. To reduce this kickback effect in this design, I have tried the neutralization techniques [7].

The neutralization technique is used to the circuits in which differential nodes are directly connected to the regeneration nodes. Since the circuit preceding the comparator has non zero impedance, it gives the charge current for the C_{gd} parasitic capacitance of differential pair due to the variations at the differential nodes. This disturbance due to the charge currents is the *kickback* noise [7]. By adding the two capacitances with values $C_N = C_{gd}$ between the gate and drain of the differential pair, as shown in figure 3.7, the kickback noise is cancelled. The neutralization technique works when the voltages at drain of differential pair are complementary. By adding the capacitances, the charge currents comes from them (added capacitances) and not from the preceding circuit and neutralizes the variations of opposite drain nodes to the gates inputs in the way presented in figure 3.7.

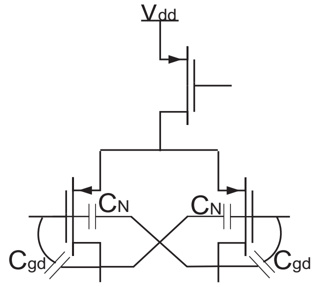

Figure 3.6: Neutralization technique.

However when this technique was implemented in this design, it had no effect on the disturbances at input nodes. One reason could be that the voltage variations at the regeneration nodes are not perfectly balanced and this technique is not enough in such kind of situation [7].

When the differential, non ideal, inputs were applied on the comparator inputs, the kickback suppression calculated was 12.2 dB with the load resistance of 300 Ω. The full scale voltage to kickback ratio with input resistance of 300 Ohm is 16:6 and 100 Ohm is 34.8:1 respectively.

4

SIMULATION RESULTS AND DISCUSSION

The latched comparator design has been simulated using Cadence tools for different parameter values. The full scale voltage of comparator is 1.6 V (0.4 V to 2.0 V). The comparator was optimized for the sampling frequency of 250 MHz. The comparator works up to the maximum frequency of 300 MHz for 6-bit resolutions.

4.1 Final simulations

Following figure 4.1 gives the pictorial explanation of comparator inputs. The output values are calculated by applying the ramp signal at the input of the comparator and a reference dc signal.

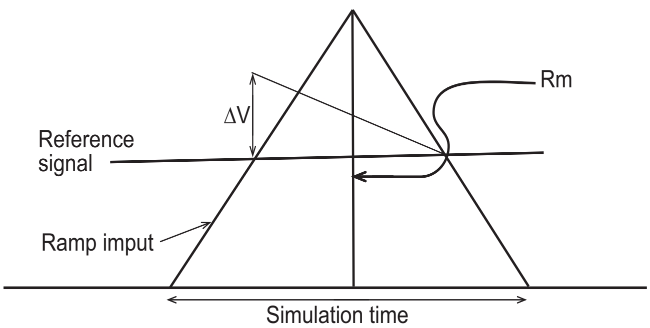

Figure 4.1: Comparator inputs model.

The following equation 4.2 shows how the resolution of comparator has been calculated. There N is the number of resolution, ΔV is voltage difference between rise and fall edge of the ramp signal and VFs is the full scale voltage.

$$\Delta V = \frac{VFs}{2^N} \tag{4.1}$$

$$N = \log 2\left(\frac{VFs}{\Delta V}\right) \tag{4.2}$$

The design has been simulated for different frequencies and reference values. The following table shows the results when a ramp signal is applied as an input. The simulation time has been calculated for different frequencies and the ramp signal of 0.2 V. The resolution (Rm) used for measurements is 0.1 mV. All the simulations values for this thesis work are derived using Cadence.

No.	Frequencies (MHz)	Ramp signal(v)	Ref. (v)	simulation time (us)	ΔV (mv)	Res. (N)
1	250	0.5 - 0.7	0.6	3.0	9.01	7.5
2	250	1.1 -1.3	1.2	3.0	1.56	9.96
3	250	1.8 - 2.0	1.9	3.0	0.596	11.39
4	300	0.5 - 0.7	0.6	3.0	24.1	6.059
5	300	1.1 - 1.3	1.2	3.0	13.05	6.943
6	300	1.8 - 2.0	1.9	3.0	19.55	6.35

4.2 The performance and design parameters

The performance and design parameters of the latched comparator are presented in Table 4.1. The values are taking by applying the non ideal inputs with load resistance of 300 Ω and 1.5 fF capacitance.

Power consumption	**4.136 mW**
Comparator Gain	**5.876**
-3dB cutoff frequency	**730.93 MHz**
Unity gain frequency	**1.021 GHz**
Input DC voltage	**1.65 V**
Comparator Biasing current	**201.2 μA**
Static power consumption	**81.08 pW**
Kickback suppression	**12.2 dB**

Table 4.1: Simulation results of the comparator

The power consumption was calculated both when the comparator was “ON” and “OFF” with sampling frequency of 250 MHz and 3.3 V power supply.

4.3 Conclusion and discussion

The purpose of this thesis work was to design a latched comparator for time-interleaved bandpass sigma-delta ADC with 6-bit resolution, sampling frequency of 250 MHz and full scale voltage of 1.5 V using 0.35 µm process with a supply voltage of 3.3 V. The simulation results in Table 4.1 show that the comparator fulfills the requirements.

Most difficult part in this design was optimization of NMOS and PMOS for proper operation and also the comparator turn off technique when it is not in use to avoid the static power consumption. But after careful analysis of simulation and designing at different points the goal was achieved. Also the comparator was successfully turned off with almost zero static power consumption.

The comparator fulfills all the other requirements with a good margin and has been simulated for worst cases. It can work up to the sampling frequency of

300 MHz. The reference signal was compared with a ramp input signal at ±0.1 V level from lower and upper boundary with satisfactory results.

ABBREVIATIONS

Following is the list of abbreviations used in this document.

ADC	Analog to digital converter
CMOS	Complementary metal oxide semiconductor
NMOS	Negative-channel metal oxide semiconductor
PMOS	Positive-channel metal oxide semiconductor
VTC	Voltage transfer characteristics

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