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Analysis of Two New Voltage Level Converters With Various Load Conditions

Mahendranath B and Avireni Srinivasulu, *SMIEEE*

***Abstract*—Application of level converter in dual supply voltage circuits is one of the most effective ways to reduce power consumption. To prevent static current, level converter is introduced as an interface at each low-to-high boundary. The design of an efficient level converter with least power consumption and overheads delay is one of the major design constraints. In this paper, two new level converter circuits with low power consumption are proposed for less propagation delay and load adaptability. The proposed level converter circuits are examined using cadence and the design parameters of a 180 nm CMOS process. The simulation results exhibit that proposed level converters can reduce propagation delay and increase speed over the existing circuits available. These level converters are simulated for different loads and operating conditions. The proposed level converters can operate at different values of V_{DDL} as +1 V, +1.8 V, +2 V and V_{DDH} of +3.3 V. The topology reports low sensitivity and has features suitable for VLSI implementation. The proposed circuits are suited for low power design without degrading performance.**

***Keywords*— Dual cascade voltage switch logic, level converter, low power, power dissipation, propagation delay**

I. Introduction

At present semiconductor device market demands the manufacture of storage devices having higher operating potentiality, and this triggers another surge in the switching speed. The power consumption has become a major issue on portable electronic systems. As a result, the level converter should have enough current to meet the requirements of transmission speed. This leads to considerable current fluctuations during a short time (d*i*/d*t*), which may raise switching noises on the power supply lines. In case of large capacitive loads, non-negligible voltage bumps are observed on the power supply lines. These are mainly due to the inductive bond wires, package and board traces, which may induce power supply and ground-bounce (switching noise or *L*d*i*/d*t* noise). This noise can also lead to data transition delay, oscillation at the end of signal transitions and cross-talk between adjacent signal lines. Moreover, it can even cause malfunctioning of the circuits that are connected to the same supply lines [1].

Due to quadratic relation between voltage and power consumption, reduction in the supply voltage is very effective in decreasing power consumption. However, that would be at the expense of the circuit delay. In order to lower the supply voltage without the degradation of system performance, Clustered Voltage Scaling (CVS) has been developed in which critical and non-critical paths of the circuit are grouped together [2]. In the CVS Scheme, by using low voltage (V_{DDL}) in the non-critical paths and using high supply voltage (V_{DDH}) in speed sensitive paths, the whole system of power consumption could be reduced without degrading the performance. Whenever an output from a low V_{DDL} cluster is to drive an input to a high V_{DDH} cluster, Level Conversion is required at the interface. The reason being the output from a low swing voltage (V_{DDL}) block cannot connect to a PMOS in a high swing voltage (V_{DDH}) block directly, since the PMOS cannot shut off with low voltage V_{DDL}. One of the main challenges in the CVS Scheme is to design Level Converters (LCs) with less power and overhead delay to interface low voltage (V_{DDL}) blocks with high voltage (V_{DDH}) blocks [3].

Despite the fact that level converter also consumes power, any formal technique that attempts to formulate the use of dual supply voltages for circuit design most possibly take the delay of and the power consumed into account. In other words, the level conversion must be accomplished by minimal delay and lower power consumption to achieve high performance CMOS circuits. Furthermore, a structure such as "V_{DDL} circuit - V_{DDH} circuit - V_{DDL} circuit - V_{DDH} circuit…" need a lot of level converters to be inserted at each "V_{DDL} circuit - V_{DDH} circuit" interface [4]. Hence both lowering the power consumed in the level converter and reducing the number of level converters as such becomes an important issue for the use of dual supply voltages. Care has been taken to design level converter accurately for lowering power consumption and propagation delay without degrading performance. In a traditional Dual Cascade Voltage Switching (DCVS), large delay has been resulted because of the contentions problem between different transistors on the level shifting path. This contention problem will lead to increase both in delay time and power consumption [5-13]. For practical purposes, a CMOS logic circuit with mixed gates operating on a lower supply voltage V_{DDL} and on a higher supply voltage V_{DDH} may be preferred. However, any gate operating on V_{DDH} and connected after the gate operating on V_{DDL} generates a short-circuit current.

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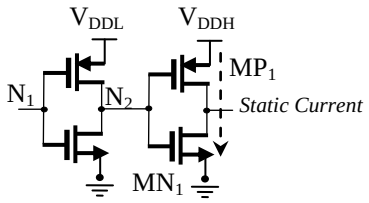

Fig. 1 Direct connection of V_{DDL} circuit and the V_{DDH} circuit

Figure.1 shows a CMOS logic circuit taking into consideration the output of first CMOS inverter is directly connected to the second CMOS inverter. The first CMOS inverter operates on lower supply voltage V_{DDL} and the second one on a higher supply voltage $V_{DDH.}$ If the input node N_1 of V_{DDL} circuit swings from high to low, the output node N_2 retains the reverse that is V_{DDL}. Subsequently, the logical high at node N_2 should turn off the pull-up transistor MP_1 and turn on the pull-down transistor MN_1. Although the voltage at node N_2 is high enough to activate the NMOS transistor MN_1, it cannot turn off the PMOS transistor MP_1 due to the fact that $V_{DDL} < V_{DDH} - |V_{th,P}|$. Therefore, there exist a static current flowing directly from the applied voltage source to ground through the path of MP_1 and MN_1. This static current also consumes power which is not desirable for low power application [6]. To restrict this unwanted power consumption, there should be a level converter circuit placed between V_{DDL} and V_{DDH} circuits. The main advantage of the level converter circuit is to reduce the static power consumption. Level converter transforms a logical high produced by a V_{DDL} circuit to the logical high for a V_{DDH} circuit. Thus, the condition of both networks MP_1 and MN_1 are activated at a time as described in Fig. 1 would not be possible, and the power consumption by the static current therefore gets eliminated. In order to achieve high performance CMOS circuits, the level converter circuit must be designed so as to have minimal delay and power consumption.

II. The Conventional Level Converters

The circuit diagram of conventional level converter is shown in Fig. 2. It is termed as Dual Cascade Voltage Switch (DCVS), interposed between gates operating on different supply voltages in a CMOS logic circuit, to prevent the short-circuit current and reduce power consumption. In this circuit there exists two cross coupled PMOS transistors MP_1 and MP_2 to generate the circuit load. The cross coupled PMOS transistor acts as a differential pair. As the output at one side gets pulled down, followed by opposite PMOS transistor to turn ON, and the output on that side will be plugged high. Below the PMOS load, there are two NMOS transistors MN_1 and MN_2 that are regulated by the input signal [7].

Although the level converter blocks the short circuit current, it consumes relatively large dynamic power while carrying out switching operation. If the CMOS logic circuit must have many level converters; the power consumption therefore would have increased to nullify the effort of decreasing the power consumption by using the two supply voltages V_{DDL} and V_{DDH}. Furthermore, this conventional level converter has relatively large delay as it has to rely on a contention between different transistors on the level conversion [7].

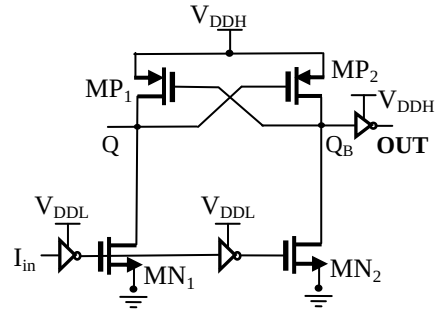

Fig. 2 Conventional level converter (DCVS)

Figure 3 shows the conventional level converter [6], with 12 transistors. This circuit has large power dissipation and propagation delay because it contains more number of transistors.

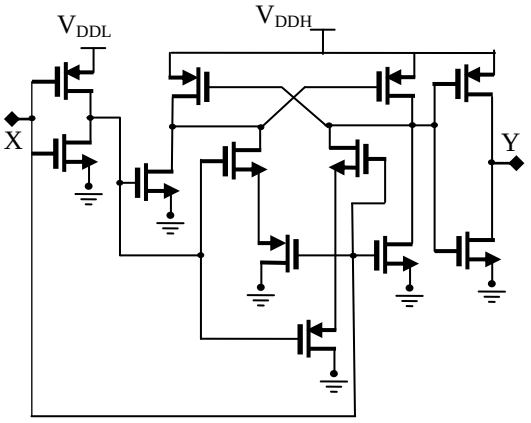

Fig. 3 Conventional level converter [6]

Figure. 4 shows the conventional level converter Standard Dual Cascade Voltage Switch (SDCVS) [7] which endorse the same cross coupled pair of PMOS transistors as DCVS with 14 transistors. The simulation profile of Fig. 4 has indicated the results in the higher propagation delay and power dissipation. To overcome these disadvantages, two new level converters with 10 transistors are proposed in this paper. These proposed circuits reduce the propagation delay and are shown in Fig. 5 and Fig. 6.

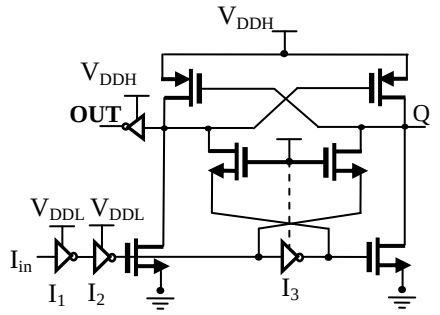

Fig. 4 Conventional level converter SDCVS [7]

The remaining sections of the paper are structured as follows. The new proposed level converter and circuit description is presented in section III. Simulation results and comparative conventional circuits are included in section IV. Finally, conclusion is included in section V.

III. PROPOSED LEVEL CONVERTERS

The proposed level converters are shown in Fig. 5 and Fig. 6. In these circuits, the level conversion circuit converts a signal V_{in} on the lower voltage side to a signal V_{out} on the higher supply voltage side; the signal V_{in} is transmitted to the inverted phase, which inturn generated by inverter constituted by transistors P_1 and N_1, ultimately transmitted to the gates of transistors N_2 and N_4. The respective gates of transistors P_2 and P_3 are cross connected to the drains of transistors P_3 and P_2, while the source of both transistors are connected to the higher supply voltage V_{DDH} and V_{03} is again connected to the gate terminals of P_4 and N_4 in the output stage, which is further connected to the higher supply voltage V_{DDH}. Here in this circuit the V_{in} signal is given as 0/1-V, 0/1.8-V and 0/2-V voltage levels and V_{DDH} is 0/3.3-V voltage level.

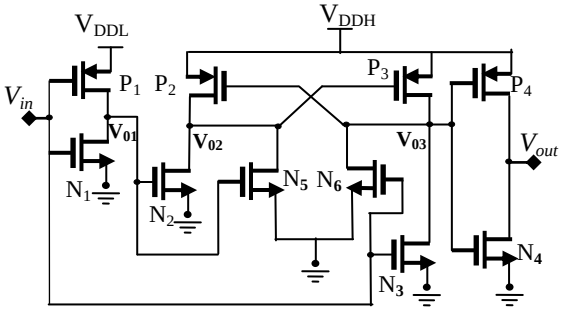

Fig. 5 Proposed level converter-1

The proposed level converter-1 is shown in Fig. 5, composed of inverter, DCVS logic and an output stage. It converts 0/1-V, 0/1.8-V and 0/2-V voltage swing to 0/3.3-V voltage swing. To reduce the body effect in Fig. 5, the bulk of the PMOS and NMOS transistors are connected to their source and drain terminals respectively. The proposed level converter employs the same cross-coupled pair of PMOS transistors as DCVS. Two NMOS transistors N_5 and N_6 are added to achieve high speed operation. These two transistors are connected to the gate terminals of P_2 and P_3 transistors to increase the switching speed of the output transition. In Fig. 5, P_1 and N_1 transistors acts as input inverter with low supply voltage level V_{DDL}. The output stage consists of PMOS P_4 and NMOS N_4. The node voltage V_{03} is connected to the gate terminal of transistor P_4 and N_4.

The circuit operates as follows: when the voltage level of input signal swings from high to low, the output voltage level of input inverter becomes the lower supply voltage V_{DDL}. Therefore, N_2 and N_5 transistors are turned ON; as a result, node V_{02} is then discharged to ground. Thus, P_3 is turned ON and then voltage level of node V_{03} becomes a higher supply voltage V_{DDH}. In this case, P_2, N_3 and N_6 transistors are turned OFF, and there by it has been made possible to prevent a short-circuit current from flowing between the higher supply voltage V_{DDH} and the ground. When the voltage level of the input signal is switched to logic high, the output voltage level of the input inverter becomes logic low. Therefore, N_3 and N_6 transistors are turned ON; as a result node V_{03} is then discharged to ground. In this case, transistor P_2 is turned ON and thereby, transistor P_3 turns OFF. There by transistors N_2 and N_5 are also turned OFF and made it possible to prevent a short-circuit current from flowing between the higher power supply voltage V_{DDH} and ground. It is thus clear that the output level transition in each input signal condition switches fast. These results contribute to faster output transition as well as contention problem on nodes V_{02} and V_{03}. As a result of this propagation delay time of the circuit gets reduced.

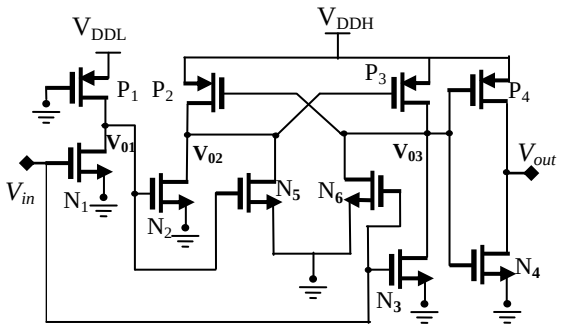

Fig. 6 Proposed level converter-2

Figure 6 display the proposed level converter-2 which is composed of pseudo inverter, DCVS logic and an output stage. It converts 0/1-V, 0/1.8-V and 0/2-V voltage swing to 0/3.3-V voltage swing. To reduce the body effect in Fig. 6 too the bulk of the PMOS and NMOS transistors are connected to their respective source and drain terminals. The proposed level converter employs the same cross-coupled pair of PMOS transistors as DCVS. Two NMOS transistors N_5 and N_6 are introduced to achieve high speed operation. These two transistors are connected to the gate terminals of P_2 and P_3 transistors to increase the switching speed of the output transition. In Fig. 6, transistor P_1 and N_1 transistor acts as input pseudo inverter with low supply voltage level V_{DDL}. The output stage consists of PMOS P_4 and NMOS N_4. The node voltage V_{03} is connected to the gate terminal of transistor P_4 and N_4.

Nextly, operation of the proposed level converter-2 is explained as follows. While the gate of PMOS P_1 transistor is connected to ground it will always be in ON condition. While the voltage level of input signal swings from low to high, the NMOS transistor N_1 turns ON and the voltage at node V_{01} is discharged to ground, so that the output voltage level of input inverter becomes low. Therefore, transistor N_3 and N_6 transistors are turned ON; as a result, node V_{02} is converted for supply of high voltage V_{DDH}. Thus, P_2 is turned ON and then voltage level of node V_{03} becomes a low. In this case, transistors P_3, N_2 and N_5 are turned OFF, and there by it is made possible to prevent a short-circuit current from flowing between the higher supply voltage V_{DDH} and the ground. When the voltage level of the input signal is switched to logic low, the output voltage level of the input inverter attains lower supply voltage V_{DDL}. Therefore, N_2 and N_5 transistors are turned ON; as a result node V_{03} then becomes higher supply voltage V_{DDH}. In this case, transistor P_3 is turned ON, and thereby, transistor P_2 to OFF. Moreover, transistors N_3 and N_6 are also turned OFF, and thereby, it is made possible to prevent a short-circuit current from flowing between the higher power supply voltage V_{DDH} and ground. It is thus clear that the output level transition in each input signal condition switches fast. These results provide faster output transition as well as contention into problems thrusting on nodes V_{02} and V_{03}. Consequently propagation delay time of the circuit becomes lesser than proposed level converter-1, with no short-circuit current flow; therefore it is possible to reduce the power dissipation.

IV. Simulation Results

The circuit in Fig. 5, Fig. 6 and low power level converter [6] and SDCVS [7] were simulated by using cadence and the model parameters of a 180 nm CMOS process. The simulations were carried out with pulse amplitude of +1 V, +1.8 V, +2 V and frequency of 1 MHz.

In order to observe the performance of the proposed level converters under various load conditions, the conventional and proposed circuits are simulated at load capacitance varying from 1 pF to 15 pF for +1 V input voltage and 1 pF to 25 pF for +1.8 V input voltage. Standard DCVS level converter in Fig. 2 suffers from the contention problem; therefore simulation results show maximum power and delay over head. On the other hand low power level converter [6] and standard SDCVS [7] level converter uses more transistors in its operation as compared to proposed level converters, that results in increase in power consumption and propagation delay.

The typical simulated input and output waveforms on the configuration of Fig. 5, with V_{DDL} = +1V, +1.8V, +2V, V_{DDH} = +3.3V and output load of C_L = 10 pF is presented in Fig. 7, 8, 10 respectively. It is evident from Fig. 7 simulated input and output waveforms are with amplitude of +1 V and +3.3V respectively with no voltage drop. For all the level converters the supply rail V_{DDL} of +1 V, +1.8V, +2 V, V_{DDH} of 3.3V and pulse input parameters shown in Table. I was used.

Figure 9 shows the simulated DC Response of proposed voltage level convrter-1 of Fig. 5. From Fig. 9 it is evident that the output voltage is varied with respect to input voltage.

The layout of the proposed voltage level converter-1 of Fig. 5 has been designed using Assura layout XL with 180 nm technology file. Layout of proposed voltage level converter-1 of Fig. 5 is shown in Fig 11. The area of the proposed voltage level converter-1 is 164.64 μm^2.

Fig. 12, 13, 15 shows the simulated waveforms on nodes V_{in}, V_{01}, V_{02}, V_{03} and V_{out} of the proposed level converter-2 with V_{DDL} = +1V, +1.8V, +2V, V_{DDH} = +3.3V and output load of C_L = 10 pF respectively. It is evident from Fig. 10 simulated input and output waveforms are with amplitude of +1 V and +3.3V respectively without any voltage drop. For all the level converters the supply rail V_{DDL} of +1 V, +1.8V, +2 V, V_{DDH} of +3.3V and pulse input parameters shown in Table. I was used. The aspect ratios of Fig. 5 and 6 transistors are given in table II.

Figure 14 shows the simulated DC Response of proposed voltage level convrter-2 of Fig. 6. From Fig. 14, it is evident that the output voltage is varied with respect to input voltage.

The layout of the proposed voltage level converter-2 of Fig. 6 has been designed using Assura layout XL with 180 nm technology file. Layout of proposed voltage level converter-2 of Fig. 6 is shown in Fig 16. The area of the proposed voltage level converter-1 is 170.79 μm^2.

TABLE I – Pulse Input Parameters

Voltage 1	+1 V, +1.8 V, +2V
Voltage 2	0 V
Delay Time	1 ps
Rise Time	2 ps
Fall Time	1 fs

TABLE II – Aspect Ratios of Fig. 5 and 6

Transistor	W (μm)	L (μm)
P_1- P_4	2	0.18
N_1-N_6	2	0.18

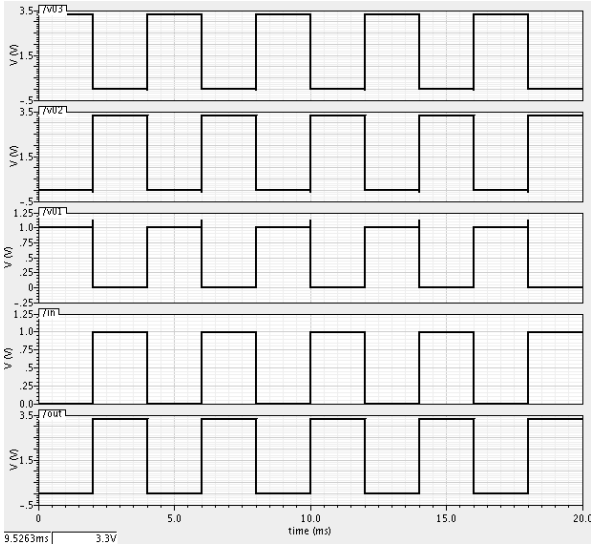

Fig. 7 Simulated input and output waveforms of Fig. 5 with load capacitance C_L= 5 pF (Supply rail voltages V_{DDH} = +3.3V and V_{DDL} =1 V).

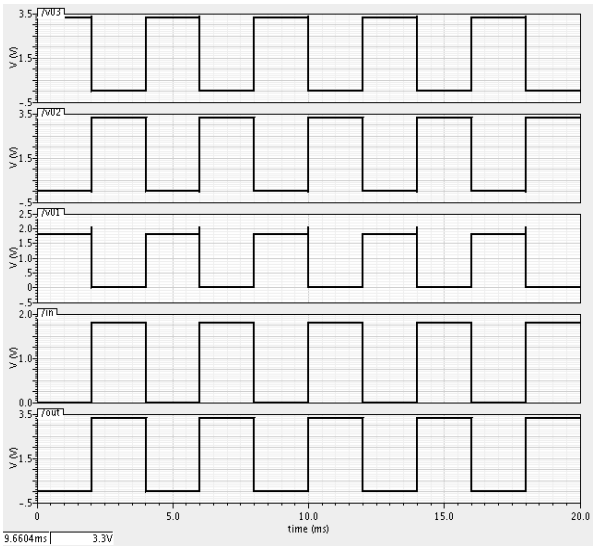

Fig. 8 Simulated input and output waveforms of Fig. 5 with load capacitance C_L= 10 pF (Supply rail voltages V_{DDH}=3.3V and V_{DDL}=1.8 V).

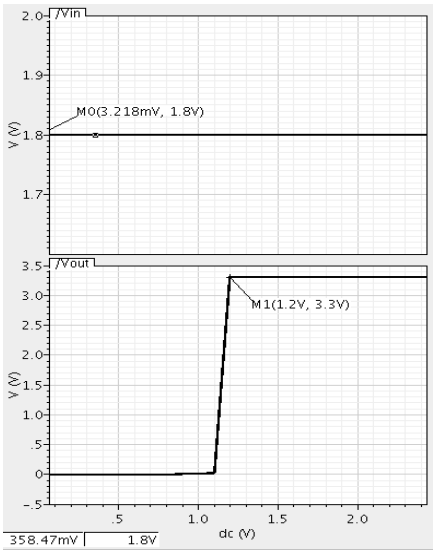

Fig. 9 Simulated DC response of Fig. 5 with load capacitance C_L= 10 pF (Supply rail voltages V_{DDH}= +3.3V and V_{DDL}= +1.8 V).

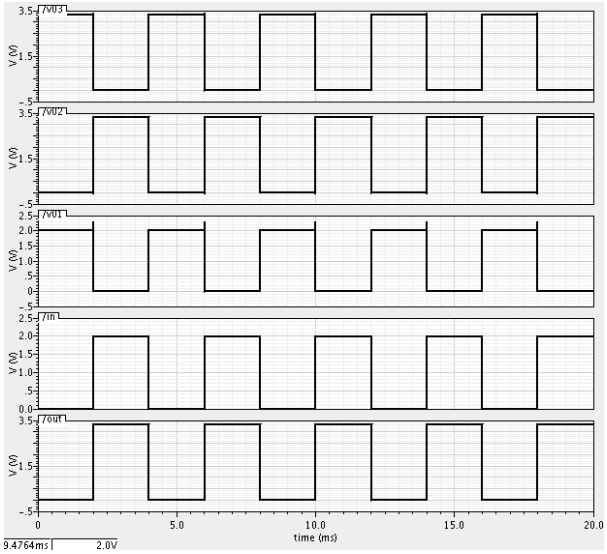

Fig. 10 Simulated input and output waveforms of Fig. 5 with load capacitance C_L= 20 pF (Supply rail voltages V_{DDH}=3.3V and V_{DDL} =2 V).

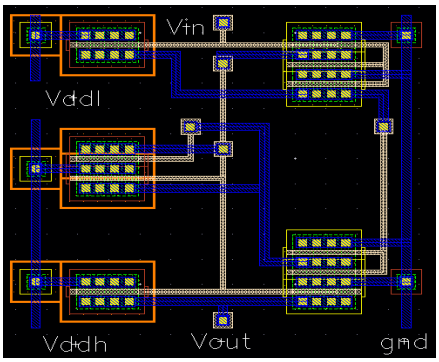

Fig. 11 Layout of proposed Fig 5

Figure 17 empowers the comparison of propagation delay for proposed level converters, low power level converter [6] and conventional SDCVS [7]. In Fig. 17 load capacitance is varied from 1 pF to 25 pF with input pulse amplitude of +1.8 V and frequency of 1 MHz. It is thus clear that the proposed level converters have less propagation delay and load adaptability than the earlier ones. From the simulation results, it is proved that the delay and power consumption in proposed level converters is very less as compared to that of in the standard DCVS, SDCVS and low power level converters. It is also observed that falling delay and rising delay in case of proposed level converter is much less as compared to the existing circuits. Accordingly, the proposed level converter circuits can be effectively applied to LSI high speed input-output circuit, as an interface between internal and external buses such as a server or exchanger, and as an interface circuit between optical devices for optical communication and an LSI, etc.

Table III represents the comparative study of propagation delay for the proposed level converters, low power level converter [6] and conventional SDCVS [7]. In Table II load capacitance is varied from 1 pF to 15 pF with input pulse amplitude of +1 V and frequency of 1MHz. From Table II also it is clear that there is a significant reduction of delay in the proposed level converter compared to the existing circuits.

Table IV shows the simulated values of the propagation delay for the proposed level converter-1 for different supply

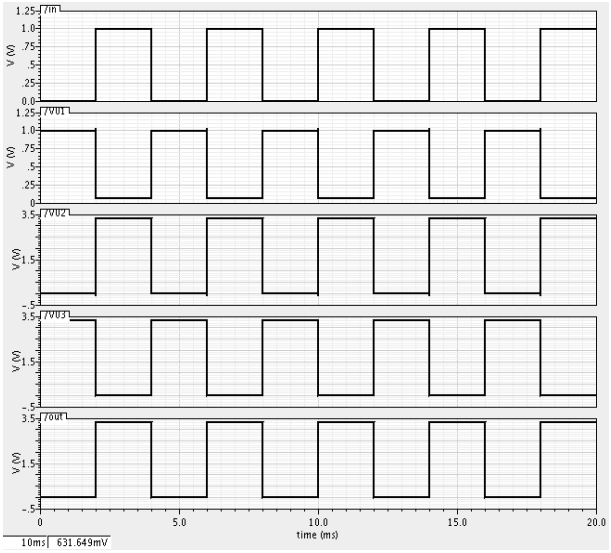

Fig. 12 Simulated input and output waveforms of Fig. 6 with load capacitance C_L= 5 pF (Supply rail voltages V_{DDH}= +3.3V and V_{DDL} = 1 V).

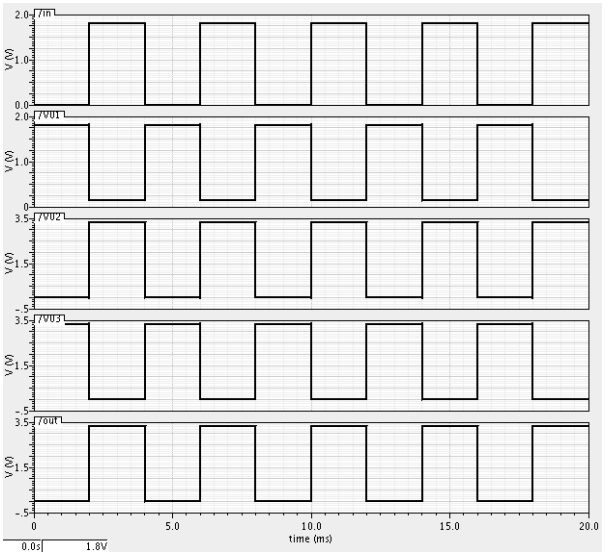

Fig. 13 Simulated input and output waveforms of Fig. 6 with load capacitance C_L= 5 pF (Supply rail voltages V_{DDH}=3.3V and V_{DDL}= 1.8 V).

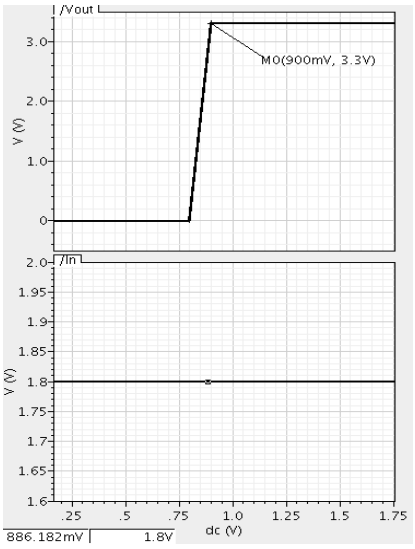

Fig. 14 Simulated DC response of Fig. 6 with load capacitance C_L= 10 pF (Supply rail voltages V_{DDH}= +3.3V and V_{DDL}= +1.8 V).

voltages V_{DDL} of (+1 V, +1.2 V, +1.8 V, and +2 V) and V_{DDH} of (+3.3 V, +5 V) with load capacitor C_L ranging from

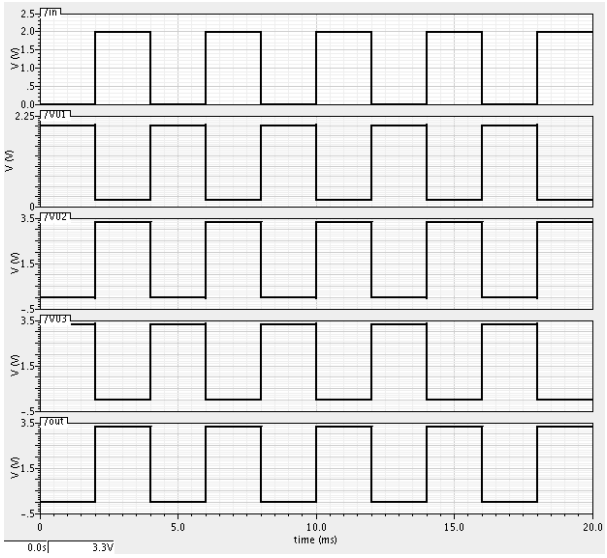

Fig. 15 Simulated input and output waveforms of Fig. 6 with load capacitance C_L= 5 pF (supply rail voltages V_{DDH}=+3.3V and V_{DDL}= +2 V).

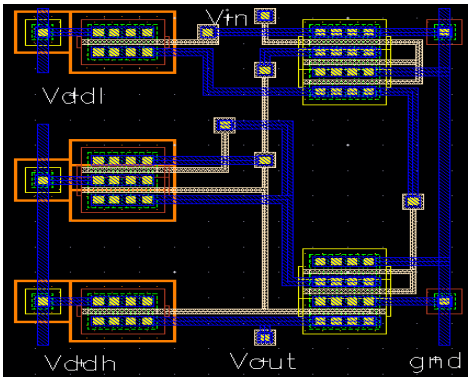

Fig. 16 Layout of proposed Fig 6

from 1 pF to 10 pF. It is also doubly clear that proposed level converters gives less propagation delay for low voltage and high voltage conversion and hence the proposed converter is very useful for low voltage and high voltage application such as PCI-X Interface.

Table V shows the simulated values of the propagation delay for the proposed level converter-2 for different supply voltages V_{DDL} of (+1 V, +1.2 V, +1.8 V and +2 V) and V_{DDH} of (+3.3 V, +5 V) with load capacitor C_L ranging from 1 pF to 10 pF. It is therefore clear that proposed level converter-2 of Fig. 6 gives less propagation delay for low voltage and high voltage conversion compared to proposed level converter-1 of Fig. 5 and hence the former is stated to have an edge over the later in efficiency and performance as well.

V. CONCLUSION

Two new level converters have been tested and designed with 180 nm CMOS Technology with V_{DDL} = +1 V, +1.8 V, +2 V and V_{DDH} = 3.3 V. It has resulted into minimizing the propagation delay and switching noise. The proposed level converters therefore can reduce the contention problem that existed in the conventional DCVS circuit. Also there is a reduction in the rising time and falling time in the proposed level converters when compared to conventional designs. Simulation results however show that the proposed designs have recorded less noise and less propagation delay, compared to previous designs. The topology reports low sensitivity and has features suitable for VLSI implementation.

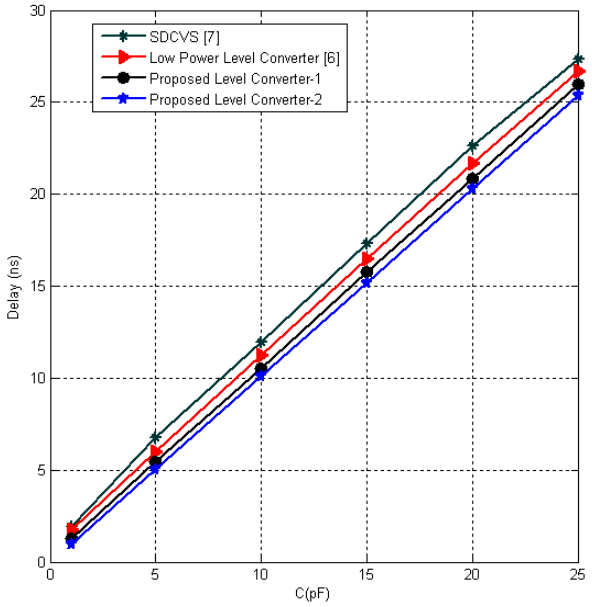

Fig. 17 Proposed level converters and conventional level converters propagation delay comparison for different loading conditions with V_{DDL} = +1.8V and V_{DDH} = +3.3 V.

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TABLE. III COMPARISON OF PROPAGATION DELAY FOR FIG. 5 FIG. 6 AND CONVENTIONAL LEVEL CONVERTERS FOR DIFFERENT LOAD CONDITIONS

Level Converters	**Supply Rail Voltages**		**Propagation Delay (ns)**			
	$+V_{DDL}$	$+V_{DDH}$	C_L=1 pF	C_L=5 pF	C_L=10 pF	C_L=15 pF
SDCVS [7]	1 V	3.3 V	4.553	9.767	15.04	19.68
LPLC [6]	1 V	3.3 V	4.627	8.631	14.3	15.9
Proposed Fig.5	1 V	3.3 V	4.868	8.376	13.28	16.54
Proposed Fig.6	1 V	3.3 V	2.998	7.169	12.41	15.13

TABLE. IV COMPARISON OF PROPAGATION DELAY FOR FIG. 5 WITH DIFFERENT LOAD CONDITIONS AND SUPPLY RAIL VOLTAGES

Supply Rail Voltages		**Capacitor Output load (C_L = 1 pF)**			**Capacitor Output load (C_L = 5 pF)**			**Capacitor Output load (C_L = 10 pF)**		
$+V_{DDL}$ (Volts)	$+V_{DDH}$ (Volts)	Rise Time (fs)	Fall Time (ps)	Delay (ns)	Rise Time (ps)	Fall Time (ns)	Delay (ns)	Rise Time (ps)	Fall Time (ns)	Delay (ns)
1	3.3	7.93	515.6	4.187	45.85	2.532	8.376	4.209	5.057	13.61
1.2	3.3	4.44	510	2.404	66.29	2.53	6.59	5.162	5.063	11.82
1.8	3.3	37.54	509.3	1.462	101	2.535	5.677	1.055	5.078	10.9
1.2	5	22.61	690.6	2.487	618	3.397	7.152	1.241	6.861	13.09
1.8	5	55.27	683.8	1.457	936.3	3.402	6.139	498.9	6.85	11.89
2	5	960.8	682.9	1.546	618	3.397	7.152	1.241	6.861	13.09

TABLE. V COMPARISON OF PROPAGATION DELAY FOR FIG. 6 WITH DIFFERENT LOAD CONDITIONS AND SUPPLY RAIL VOLTAGES

Supply Rail Voltages		**Capacitor Output load (C_L = 1 pF)**			**Capacitor Output load (C_L = 5 pF)**			**Capacitor Output load (C_L = 10 pF)**		
$+V_{DDL}$ (Volts)	$+V_{DDH}$ (Volts)	Rise Time (ps)	Fall Time (ps)	Delay (ns)	Rise Time (ps)	Fall Time (ns)	Delay (ns)	Rise Time (ps)	Fall Time (ns)	Delay (ns)
1	3.3	496	516.4	2.998	26.42	2.534	7.169	6.521	5.706	12.41
1.2	3.3	4.332	509.9	1.622	574.3	2.532	5.82	2.348	5.05	11.10
1.8	3.3	1.134	520.7	1.112	719.2	2.534	5.134	7.194	5.057	10.56
1.2	5	53.15	690.5	1.709	570.1	3.404	6.382	1.816	6.865	12.3
1.8	5	665	691.2	1.226	613.6	3.445	5.94	693.2	6.803	11.74
2	5	710.3	696.1	1.148	14.43	3.409	5.837	15.89	6.868	11.75

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