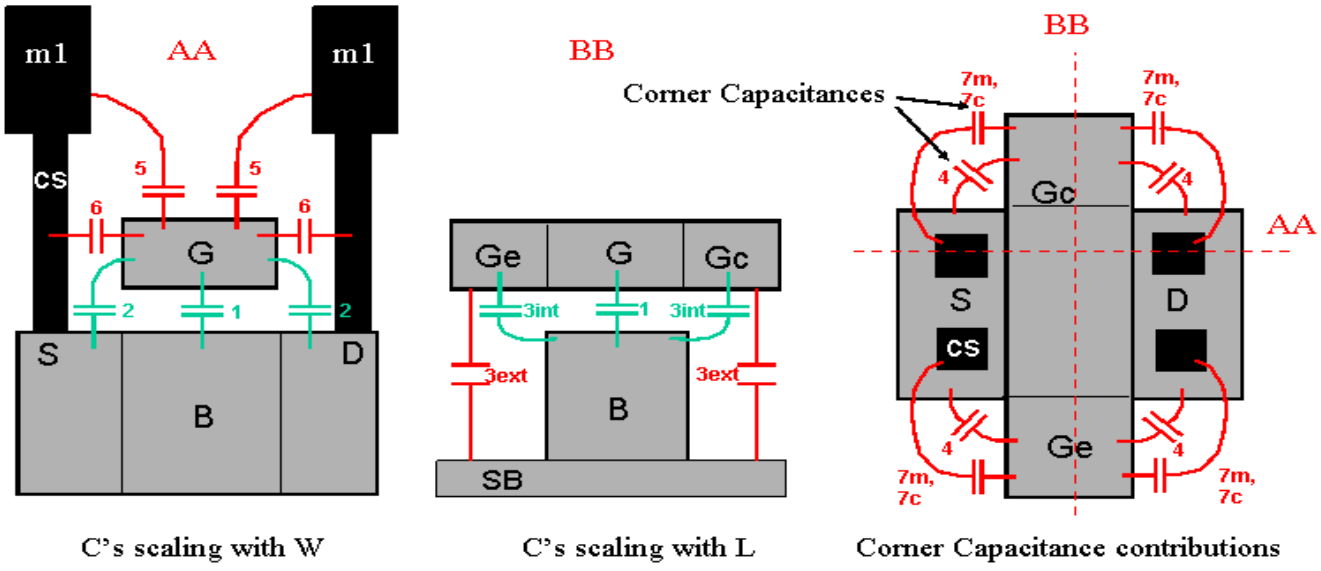
PARASITIC CAPACITANCE MODELLING FOR MOSFETS

1. PRINCIPLE

A methodology has been developed to take into account parasitic capacitance contributions such as poly-contact coupling and corner capacitances which can not be neglected anymore.

These parasitic capacitance are extracted from the PCELL MOS structure. Note that all parasitic capacitance till M1 are included in 90nm SPICE MOSFET models.

NB : refer to the model status file for LPE flag availability.



C's scaling with W | C's scaling with L | Corner Capacitance contributions

Capacitance drawn in green: Intrinsic capacitance included in SPICE model,
Capacitance drawn in red: Parasitic capacitance included in SPICE model.

2. MODEL EQUATIONS

Following C2, C4, C56 and C7 result in CF parameter whereas C3 is computed ad CGBO parameter. General equation is based on this format :

$C_i = C_{i0} + C_{il}*LPOLY + C_{iw}*WOD + C_{ilw}*LPOLY*WOD$

where

LPOLY stands for poly silicon length

WOD for active width.

2.1 Scaling versus W and L equations

2.1.1 Previous methodology used for GPs and SVT33 models

C2 = fudge_factor*[C20 + C2w*WOD]

C3 = fudge_factor*[C3int0 + C3intl*LPOLY]

C4 = C40 + C4w*WOD

C7 = not de embedded -> included in capacitance measurement

C56 = not de embedded -> included in capacitance measurement

Fudge_factor : factor to correct for depletion in Silicon. The simulations were performed with Raphael which considers only metals and dielectrics. The fudge factor was determined using TCAD simulations: fudge_factor = 0.8.

2.1.2 New methodology used for SVT25 model

C2 = fudge_factor*[C20 + C2w*WOD]

C3int = fudge_factor_c3*[C3int0 + C3intl*LPOLY]

C3ext = C3ext0 + C3extl*LPOLY

C4 = C40 + C4l*LPOLY + C4w*WOD

C7 = C7m + C7c = C70 + C7l*TANH(LPOLY/C7l0) + C7w*TANH(WOD/C7w0)

C56 = C5 + C6 = C560 + C56l*WOD*TANH(LPOLY/C56l0) + C56w*WOD.

Fudge_factor : factor to correct for depletion in Silicon. The simulations were performed with Raphael which considers only metals and dielectrics. The fudge factor was determined using TCAD simulations: fudge_factor = 0.8, fudge_factor_c3 = 0.3.

Equation parameters such as C7c for instance, can be different depending on whether standard or dogbone structures are considered.

3. NOMENCLATURE

No special nomenclature is dedicated to Parasitic Capacitance Modelling. Indeed these models are applied to all models present in the model card.

LP -> SVT, HVT and both SRAMs

SVT25.