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A High Efficiency ALL-PMOS Charge Pump for Low-Voltage Operations

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***Abstract*—This paper presents a high performance ALL-PMOS charge pump suitable for implementation in standard CMOS processes. And only low voltage PMOS transistors are used. With the switching substrate technique and boosted transistor, the influence of body effect is eliminated and output voltage is greatly increased. A twelve-stage charge pump circuit is fabricated in a 0.35-μm double-poly CMOS technology. Measurements at 3MHz have shown that for power supply voltages of 2V, 1.5V and 1V an output voltage of 15.5V, 10.4V and 3.6V can be generated respectively.**

***Index Terms*—Charge pump, standard CMOS process, power efficiency, boosted transistor, number of stage, low voltage**

I. INTRODUCTION

Driven by low power and system-on-chip applications, the integrated circuits nowadays are migrating to deep sub-micron technologies, where the supply voltage is often reduced to 1.5V or lower. Charge pump circuits are always required to obtain a voltage higher than the supply voltage, and especially have been used to generate high programming voltages in the nonvolatile memories, such as EEPROM and flash memories.

Most charge pumps are based on the circuit proposed by Dickson [1]. Fig.1 shows an n-stage Dickson charge pump with diode generating positive high voltage. It comprises of capacitors interconnected by diodes and coupled in parallel using two anti-phase clocks. The conventional Dickson charge pump is widely used in CMOS technology substituting the diode with a diode-connected MOSFET. However, due to body effect, the threshold voltage of transfer transistors increases, so the circuit is difficult to achieve high power efficiency.

To overcome this problem, several attempts have been made. A boosted charge pump is presented in [2] for generating positive high voltage. One auxiliary clock and one auxiliary transistor are used to boost the gate voltage during charge transfer operation, so the pumping gain can be

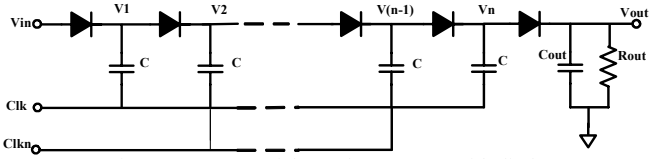

Fig 1. An n-stage Dickson charge pump with diode

improved because of the lower source-drain voltage of the charge-transfer transistors. Since all the substrate is biased to ground, the body effect still exists. And with the output voltage increasing, low voltage transistors have to be replaced by high voltage transistors due to the breakdown voltage limitation. Output voltage and power efficiency of charge pump is more degraded because of the higher threshold voltage of high voltage transistor. A triple-well process can solve this problem [3]. However, it is not always suitable in order to be compatible with other circuits.

An modified charge pump, implementing with only low voltage transistors, is presented in this paper. Two auxiliary substrate switches and a boosted transistor are used to eliminate body effect of the charge-transfer transistor and increase power efficiency. In Section II, operation principle and power assumption analysis of the proposed charge pump are explained. Section III describes simulation and measurement results of the charge pump circuit. And finally, the conclusion is presented in Section IV.

II. CIRCUIT DESIGN

A. Operation principle of the proposed charge pump

The proposed charge pump circuit is shown in Fig.2. Two auxiliary MOSFETs, M_{i3} and M_{i4}, are introduced to update the body voltage of charge-transfer transistor M_{i1}. The other auxiliary transistor M_{i2} is used to boost the gate-source voltage of the charge-transfer transistor. All the transistors' substrate is connected together in a stage. Fig.3 (a) presents the four-phase clocking schemes. The clocking scheme comprises two non-overlapping clock phases clk_1 and clk_2 for charging the pump capacitors C_p and two overlapping clock phases clk_3 and clk_4 for boosting the gate-

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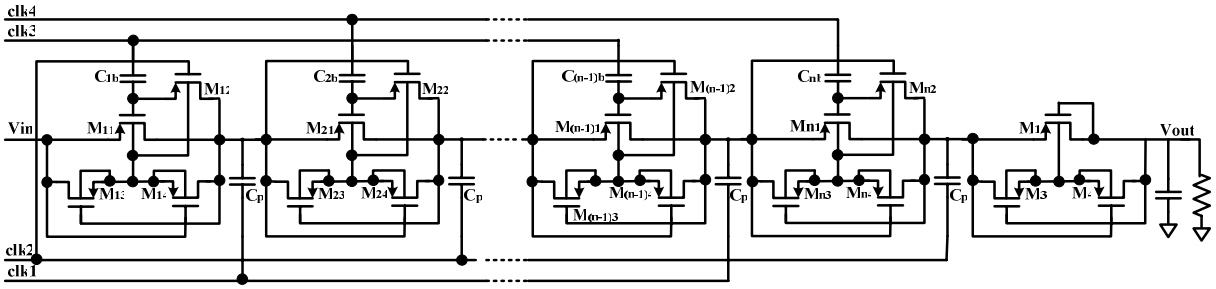


Fig.2. The proposed all-PMOS charge pump for generating positive high voltage

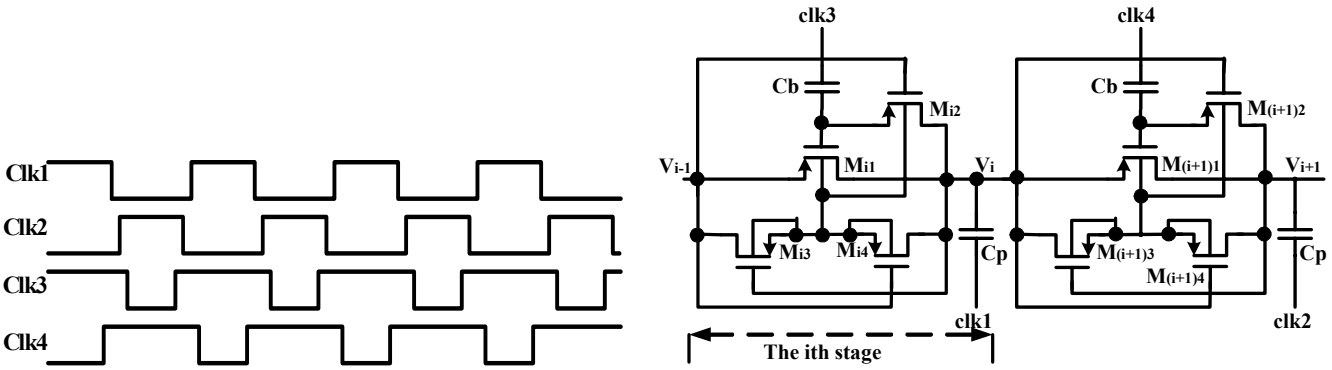


Fig.3. (a) four-phase clocking scheme, and (b) the ith stage of the proposed charge pump circuit.

source voltage of transistor M_{i1} during charge transfer operation.

Fig.3 (b) shows the ith stage of the proposed charge pump. During a first pump cycle, clk_1 is at a low level and couples node V_i to low level versus the pump capacitor C_p. At this clock phase clk_2 is high and couples node V_{i-1} and node V_{i+1} to high level versus the pump capacitor C_p, hence the boosted transistor $M_{(i+1)2}$ turns on and the gate of charge-transfer transistor in the (i+1)th stage is precharged so that $M_{(i+1)1}$ is turned off in time. At the same time, another boosted transistor M_{i2} is turned off. When clk_3 gets low, transistor M_{i1} operates in the linear region because of lower gate voltage. Thus the charge is transferred from the previous node V_{i-1} to the current node V_i, and both nodes are now at the same voltage level, except of a small voltage loss at M_{i1}.

During next pump cycle, node V_i is coupled to a high voltage level versus the pump capacitor C_p by clock phase clk_1 and node V_{i+1} to a low voltage level by clock phase clk_2. Because clock phase clk_3 is high and the gate of M_{i1} is precharged, the charge-transfer transistor M_{i1} is turned off. Transistor $M_{(i+1)1}$ do not transfer charge to V_{i+1} until clk_4 gets low. Anyway, the charge transfer operation between two pump capacitors is done during the boost cycles only. And the boosted transistor in ALL-PMOS charge pump is used to increase the gate-source voltage of charge-transfer transistor, and minimize its conductive resistor. So the output voltage of the charge pump effectively increases compared to conventional structures.

Neglecting transistor' mismatch, the voltage gain ΔV at each pumping node is identical and can be expressed as:

$$\Delta V = V_{dd} \cdot \gamma - I_O R_{ON} - \frac{I_O}{f \cdot (C_p + C_S)} \tag{1}$$

$$\gamma = \frac{C_p}{C_p + C_S + C_b} \tag{2}$$

and V_{out} of a positive charge pump with n stages can be calculated by the following:

$$\begin{aligned} V_{out} &= V_{dd} + n \cdot \Delta V - V_T \\ &= V_{dd} + n \cdot [V_{dd} \cdot \gamma - I_O R_{ON} - \frac{I_O}{f \cdot (C + C_S)}] - V_T \end{aligned} \tag{3}$$

where V_{dd} is the power supply and the input voltage of charge pump circuit, C_s is the sum of parasitic capacitor associated with each pumping node V_i, C_p is the pump capacitor, C_b is the gate-couple capacitor, and I_o is the load current, R_{on} is the conductive resistor of the charge-transfer transistor, f is the clock frequency, and V_T is the threshold voltage of the output transistor.

During one of the half cycle, when clk_1 is low and clk_2 is high, the output voltages of odd stages are lower than those of even stages. Then, transistors M_{i4} of odd stages are turned off and transistors M_{i3} are in weak conducting region. At the same time, transistors M_{i3} of even stages are turned off and transistors M_{i4} are in weak conducting region respectively. It means that all the transistors'

substrate nodes are always connected to higher level. Similarly, in the other half cycle, the substrate nodes are still in higher level. These two auxiliary substrate-switching transistors entirely eliminate the body effect of charge-transfer transistors, so the power efficiency is improved evidently. Since the voltage difference between source, drain and substrate node of PMOS transistor is always less than power supply, low voltage transistors in the proposed circuit are enough.

B. Power consumption analysis

In the steady-state condition, neglecting the parasitic capacitances in each node and the bottom-plate parasitic capacitance of the pump capacitor C_p, total current consump-tion of an ideal n-stage charge pump is given by [4]:

$$I_{power} = (n+1)\cdot I_o \tag{4}$$

I_o is the load current. Hence, the power consumption is independent of the pump capacitor, the threshold voltage of transistor and load capacitor, only depending on the number of stage and output load current. However, other current contributions due to charging and discharging all kinds of parasitic capacitances have to be taken into consideration in real charge pump.

All the capacitors including parasitic capacitances in the proposed charge pump are shown in Fig.4. To simplify the analysis, we suppose that the charge pump has been in steady state and every stage is completely identical. All the parasitic capacitances are classified into four parts, marked as C_1, C_2, C_3 (not shown in Fig.4) and C_{sg}. As shown in Fig.4, part C_1 includes all the couple capacitors between the adjacent stages. Part C_2 includes the parasitic capacitors between node V_i and the substrate, and those between node V_i and the gate of charge-transfer transistor M_{i1}. The bottom and upper-plate parasitic capacitors contribute to part C_3. Additional current has to be used to charge and discharge the substrate capacitor C_{sg}. So the current wasted to drive all the parasitic capacitances and the boost capacitors in each clock cycle is given by

$$\begin{aligned} I_{power-all} &= I' + I'' + I_{power} \\ &= (n+1)I_{out} + nf(C_s + C_b)\cdot\Delta V \end{aligned} \tag{5}$$

where C_s is the sum of all the parasitic capacitances., C_b is the boost capacitor. Judged by the preceding analysis, the proposed charge pump needs more current to drive the boost and parasitic capacitors in each stage. Thus to minimize the power consumption, the area of each auxiliary transistor and the boost capacitor should be designed as small as possible.

III. Simulation and Measurement Results

A. Simulation Results

In order to evaluate the proposed charge pump and compare it to the conventional charge pump, circuit simulations are performed using 0.35-μm CMOS process parameters. All the simulations are carried out at 2MHz. The values of pumping capacitors and boost capacitors in all the charge pumps are 3pF and 0.1pF, respectively.

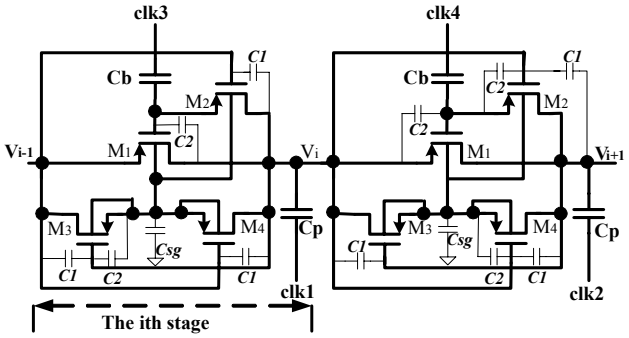


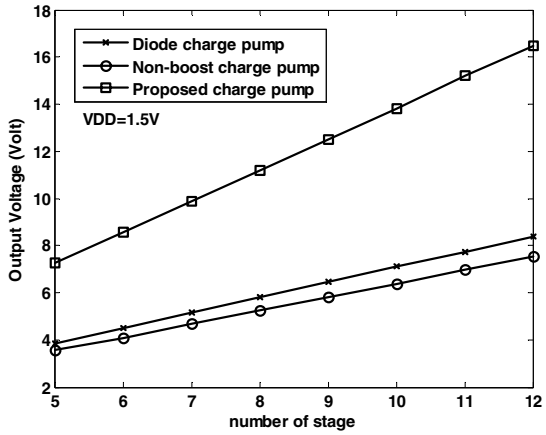
Fig.4. The parasitic capacitors in the ith stage charge pump

ALL the simulations are in a ideal case, not including parasitic capacitors. Fig.5 shows SPICE simulation comparison results for diode charge pump, non-boost charge pump [5] and the proposed charge pump. The output load current is 1μA in all cases. As shown in Fig.5 (a), we can see that for the proposed circuit, the output voltage is the highest for the same stage number. The proposed charge pump could reduce stage number and chip area for the applications of high output voltage and low power supply. The comparison results of power efficiency versus load current for the three circuits are given in Fig.5 (b). When load current is more than 0.9μA, the proposed charge pump has better power efficiency than the other two structures. A maximum power efficiency of 87.1% has been reached at load current of 2.5μA for power supply voltage of 1.5V.

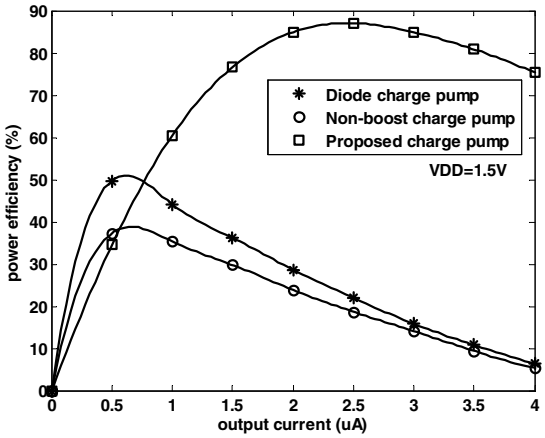
B. Fabrication and Measurements

The microphotograph of the proposed charge pump (including ring oscillator, four-phase clock generator) is shown in Fig.6. A twelve-stage charge pump has been implemented in a 0.35-μm double-poly CMOS technology (four metals) with supply voltage V_{dd}=1-2V. And the voltage controlled ring oscillator is used to generate the variable clock signal. It has a linear supply dependence and generates a 2MHz square waveform when operating at 1.5V. The conventional four-phase clock generator is used. The values of pumping capacitor and boost capacitor are identical with the simulation parameters.

A set of measurement has been performed at different clock frequency and supply voltage. A comparison between simulation results (assuming γ=0.9) and measurement results is shown in Figure.7. The measured



(a)



(b)

Fig.5. SPICE simulation comparison results for Diode charge pump, non-boost charge pump and proposed charge pump.

(a) Output voltage vs number of stage, (b) Power efficiency vs output current for 12-stage charge pump

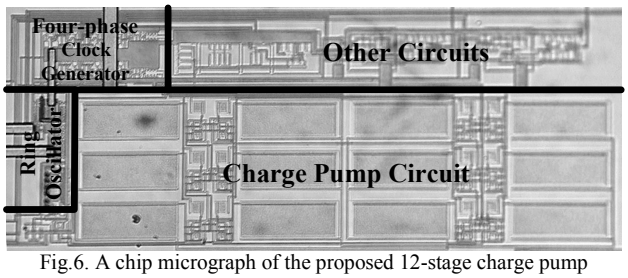


Fig.6. A chip micrograph of the proposed 12-stage charge pump

results are shown in solid lines. As shown in this figure, the output voltage is a function of the power supply voltage. For the power supply voltage of 2V, 1.5V and 1V, it can generate 15.5V, 10.4V and 3.6V at 3MHz clock frequency. The measured output voltages are lower than those predicted by simulation. This is due to the predicted inaccurate parasitic capacitor value and the degrading performance of the four-phase clock in the implementation.

IV. CONCLUSIONS

In this paper, a high efficiency charge pump circuit is presented. It is only composed of low voltage PMOS transistors. And the operation theories and power consumption are analyzed. The circuit does not suffer from the threshold voltage loss due to the linear operation of charge-transfer PMOS transistors so as to generate higher voltage than conventional charge pump structures for the same stage number, which makes it attractive to low voltage applications.

An ALL-PMOS charge pump for memory application has been manufactured. Measurement results have showed that the performance of the proposed charge pump successfully follows the above theoretical analysis.

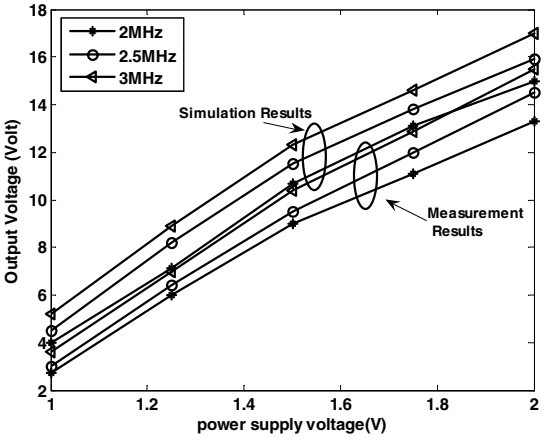


Fig.7. Simulated (γ=0.9) and measured output voltage of a 12-stage proposed charge pump at various power supply and switching frequency

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