# Design of a low power, high speed complementary input folded regulated cascode OTA for a parallel pipeline ADC

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***Abstract*— This paper presents a low-power, high speed complementary input folded regulated cascode operational transconductance amplifier (OTA) designed for the 10bit, 150MSPS parallel pipeline ADC. The OTA plays an important role in the ADC, because of its conversion rate and power consumption are limited by the performance of the OTA. The designed ADC in this paper employs parallel pipeline architecture based on double sampling sampled hold (DSSH) technique, and shares the OTA between two channels of the ADC. The folded cascode OTA consists of fully differential and regulated cascode gain boosting technique. Besides, a Common Mode Feed Back (CMFB) circuit was introduced and some methods are concerned to improve the performance. Then, by proper optimization of the layout design, OTA's mismatch was reduced up-to a great extent. With 1.8V power supply, using the CMOS9T5V 180nm process technology, the simulation shows that the open-loop gain of the OTA is 90.39 dB, the phase margin (PM) is 63.85° with the unity gain bandwidth (UGB) of 700.7 MHz. The power consumption of this OTA is only 3.24 mW, which significantly reduces the whole power consumption of the parallel pipeline ADC.**

***Keywords- OTA, regulated cascode, CMFB, DSSH, parallel pipeline ADC, and bandgap voltage reference.***

## I. INTRODUCTION

High-performance digital signal processor in various fields greatly promotes the development of high-speed, high-resolution data converters. The pipeline ADC becomes the main architecture of 8-14bit, 10-200MSPS ADCs, because its merits, such as conversion in turn, pipelined operation, make it maintain high speed and high resolution. Because of the higher precision and higher sampling rate than other kinds of ADC, the pipeline ADC is used extensively in the realm of high-speed digital transmission, digital image processing, DVB-H application etc. Since the individual ADC is hard to accomplish such kind of high-speed demand, the architecture of parallel pipeline ADC with several time-interleaved pipeline ADCs is an attractive alternative [1]-[3]. The block diagram of the parallel pipeline ADC is shown in Fig.1. The resultant circuit, so called regulated cascode or gain boosting amplifier is utilized in a current source, which is shown in Fig.7 [4]. Compare to telescopic topology, the folded cascode topology requires more power, but it offers large output swing and has good performance on common mode input range [4]-[5]. Also the special care was taken for enhancing the input common mode range by using complementary input configuration. For high gain, the architecture of a single stage amplifier with gain-boosted amplifier is a nice choice. However, the main drawback of the parallel pipeline ADC is the mass power consumption, large area, comparing with other kinds of ADCs. Therefore, we put our focus on the power consumption reduction during this design. The total power consumed by the parallel pipeline ADC depends mostly on the power-dissipation of the op-amp in the S/H module and the MDAC module. In that case, how to decrease the power of the op-amp becomes the most critical issue. A low-power op-amp, which is suitable for the S/H module and the MDAC module in the 10bit, 150MHz, and 2-channel pipeline ADC, is described in this paper.

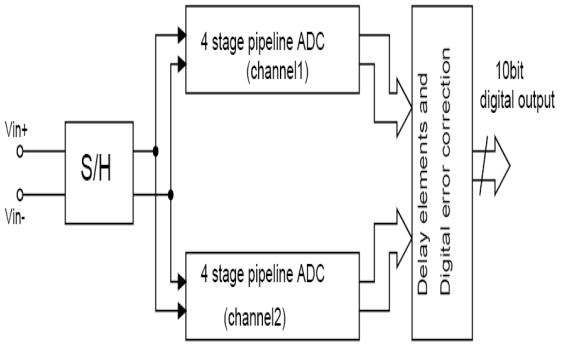


Figure 1. Block diagram of parallel pipeline ADC

In section II, the architecture of the parallel pipeline ADC, the DSSH circuit with its sampling clock cycle and the requirement of the op-amp for the parallel pipeline ADC are presented. Section III deals with the design of the op-amp, while section VI gives the circuit simulation results. The conclusion is given at last.

## II. THE ARCHITECTURE OF THE PARALLEL PIPELINE ADC

To decrease the complexity of the circuits and the design requirement of the sub blocks, the parallel pipeline ADC is adopted, as shown in Fig.1. The ADC of each channel consists of four pipeline stages of 2.5-bit each stage and a 4-bit flash ADC at the last stage, as shown in Fig.2. The two channel of the parallel pipeline ADCs is sharing the same op-amp. For pipeline1, the odd stages are worked in clk1 and the even stages are worked in clk2, working principle for

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pipeline2 is same as it is in pipeline1. Due to op-amp consuming the most percent of total power consumption of the ADC, this kind of architecture could greatly save power consumption, and decrease the offset and gain mismatch between two channels. Each pipeline stage outputs three-bit signals, the MSB as one bit of global digital outputs, and the LSB as the redundant bit to digitally correct the comparator offset. There is a redundant sign digit (RSD) correction block, the LSB of the first stage aligned with the MSB of the 2nd stage and so on [6].

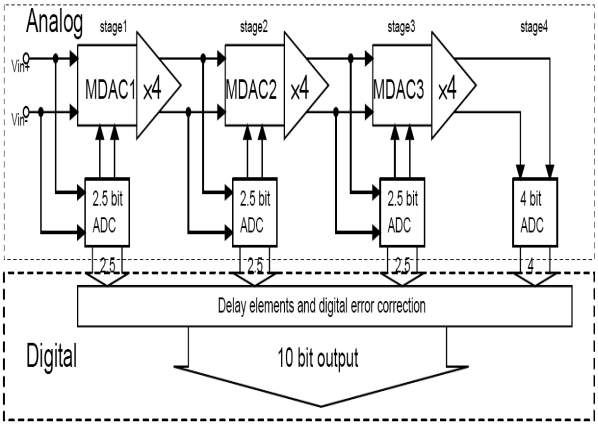


Figure 2. 2.5-2.5-2.5-4 bit Pipeline ADC for each channel

Fig. 2 shows the complete architecture design of the one sided pipeline ADC. The inter-stage MDACs are realized using switched capacitor techniques. The first, second, and third stages use a 2.5 bits flash ADC. The final stage is a full 4-bit flash ADC to slightly reduce the amplifier count by one. Fully differential signal and reference paths are used for the entire ADC. Clock generator and biasing circuits were also designed but are not considered here for brevity.

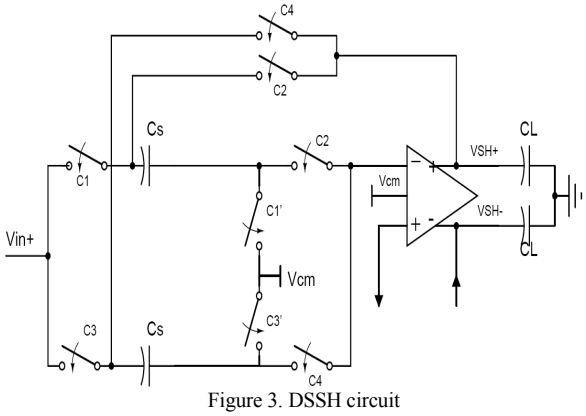


Figure 3. DSSH circuit

S/H amplifiers, comparators, digital delay, and correction logics all need the clock control. There are two kinds of sampling clocks in the 10-bit 150MSPS parallel pipeline ADC, one of which is 150MHz global clock, and the other is two-phase non-overlapping clocks of 75MHz used in each channel ADC. The 75MHz clocks are generated from the flip-flop triggers and two delayed cells of cross negative feedback using the global clock input. The global clock and the timing of the S/H amplifier of each channel are shown in Fig. 4. The core circuit of S/H amplifier using the double sampling technique is only one op-amp, as shown in Fig. 3. The same input signals are controlled by the different clock phases in two channels. Therefore, the rate of the final digital outputs can be twice higher than the rate of conventional pipeline ADC. The actual design adopts fully differential circuit to reduce the common mode noise on the power and the substrate. Every stage includes 3-bit sub flash ADC, 3-bit sub DAC, and S/H amplifier. Sub flash ADC generates 2.5-bit digital outputs from six low accuracy comparators, 3-bit DAC is controlled by the output of the flash ADC.

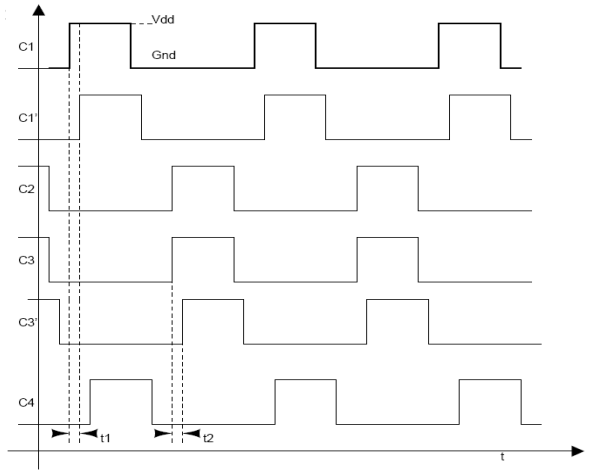


Figure 4. Clock distributions of the DSSH circuit

Also, there are in principle two types of noise in MOS circuits, thermal noise and 1/f (flicker) noise. The thermal noise is white, while 1/f noise is frequency dependent. 1/f noise dominates at low frequencies while the thermal noise is usually dominant for wide band circuits. The 1/f noise can also be decreased by circuits' techniques such as correlated double sampling. Therefore, the 1/f noise is neglected in the following. The sampling capacitor $C_S$ is limited by the $KT/C_S$ noise and matching. Because of the accuracy requirement, it has different requirements in different stages. If only considering the $KT/C_S$ noise, the signal-to-noise ratio of a pipeline stage can be expressed as

$$n^2_{KT/C} = \frac{KT}{Cs} = \frac{(V_{SWING}/2\sqrt{2})^2}{SNR} \quad (1)$$

The minimum size of the capacitors is determined by the $KT/C_S$ noise, which limits the SNR. The maximum signal swing VSWING, which is equal to $2V_{REF}$ is ($+V_{REF}$ to $-V_{REF}$) limited by the power supply and the designed op-amp. Performance of SC MDAC is primarily limited by the thermal noise generated by the sampling capacitors of the circuit. Noise is also contributed by the parasitic capacitances of the OTA. Generally, noises due to these parasitic capacitances are ignored while calculating the thermal noise of the multiplying digital to analog circuit

(MDAC). Let there are 'm' stages of pipeline ADC with resolution of each stages are n1, n2, n3,…, $n_m$. Thermal noise generated by the 1st stage is denoted by $V_{n1}^2$, for 2nd stage denoted by $V_{n2}^2$, and so on.

$$v_{n,1}^{\ 2} = \frac{KT}{2^{n1}.C_1} \tag{2}$$

$$v_{n,2}^{\ 2} = \frac{KT}{2^{n2}.C_2} \tag{3}$$

$$v_{n,i}^{\ 2} = \frac{KT}{2^{ni}.C_i} \tag{4}$$

Where, $C_{TOT,i} = 2^{ni}.C_i$ are total sampling capacitors of the individual stages [6]. Input referred noise due to the ith stage MDAC of the pipeline ADC will be modified according to the following equation

$$v_{n,inputi}^{\ 2} = \frac{KT}{G_1 G_2 ..G_{i-1} 2^{ni} C_i} \tag{5}$$

Where $G_i$s are gain factor of the MDACs of the individual stages. Since the input referred noise of the ADC occurring due to 1st stage is $v_{n,1}^{\ 2} = \frac{KT}{2^{n1}.C_1}$ (6)

So, the required condition for the 1st stage should be defined as

$$v_{n,1}^{\ 2} \le v_{n,quantization}^{\ 2} = \left(\frac{FS}{2^{n,TOT}}\right)^2 \times \frac{1}{12} \tag{7}$$

$$\frac{KT}{2^{n1}.C1} \le \left(\frac{FS}{2^{n,TOT}}\right)^2 \times \frac{1}{12} \tag{8}$$

$$C_1 \ge \frac{3.2^{2n,TOT+2} KT}{2^{n1} FS^2} \tag{9}$$

Thus, the thermal noise limitation helps determining the lower limit of the sampling capacitor of the 1st stage. Size of the sampling capacitors of the remaining stages can also be determined as in (5). Now, the 2nd stage will obey the condition $v_{n,2}^{\ 2} \le v_{n,1}^{\ 2}$.

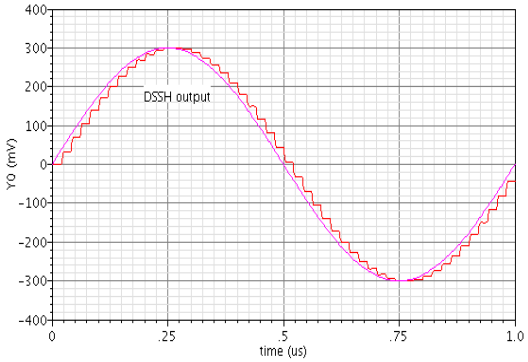

Figure 5. Output of the double sampling S/H circuit

## III. THE DESIGN OF THE OP-AMP

To achieve the desired gain, the op-amp is designed with the gain-boost architecture. A folded cascode with regulated cascode gain boosting technique is used in this design, is presented in Fig.7. The sampling speed of the ADC is specified as 150 MSPS. Employing double sampling makes sure that a clock of frequency fclk=75 MHz is required to achieve such sampling rate. Also to support such a sampling speed, the OTA must be verified with an input pulse train of equal frequency and must settle its output to a desired value within time T/2 where T = 1/fclk. Whether the settling-time of the op-amp is sufficient, enough to meet the requirement of this design is the concern.

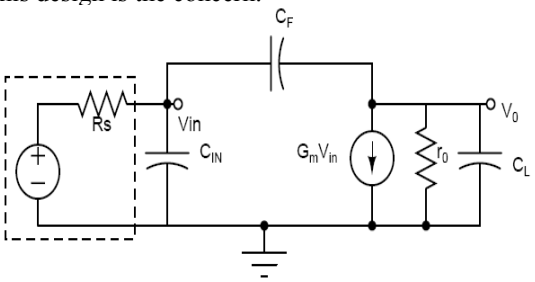

Figure 6. High frequency equivalent circuit of the OTA

$$UGB = 1/2\prod\tau \tag{10}$$

Where $\tau = r_o \times (C_F + C_L)$. (11)

Let, E is the peak to peak amplitude of the input pulse and allowable settling error is $E/2^N$. Here for this design N=10, and t=T/2. So the output voltage Vo(t) is given below

$$V_0(t) = E\left(1 - e^{-\frac{t}{\tau}}\right) \tag{12}$$

$$V_0(t) = E(1 - e^{-\frac{T}{2\tau}}) = E - \frac{E}{2^N} \Rightarrow \tau \le \frac{T}{2N \ln 2} \tag{13}$$

With $f_{clk}$=75MHz, OTA UGB requirement has been set as $UGB \ge 165.48\ \text{MHz} \approx 2.2 f_{clk}$.

Thus, for a clock speed of 75 MHz, OTA UGB requirement has been set as UGB ≥ 200 MHz. Also the open loop gain can be estimated as

$$\frac{ICMR}{A} \le \frac{ICMR}{2^{10}} \tag{14}$$

$$A_{dB} \ge 20\log 2^{10} \approx 60.206dB \tag{15}$$

In order to achieve satisfactory resolution from the ADC, the open loop gain of the OTA has been set as A(0) ≥ 61 dB. Here the designed OTA dc gain A(0) is well above the required value which has been checked for different process and corner analysis. To increase the ICMR of the OTA a standard technique often used is to apply complementary MOS transistor pairs at its input [4]. Using such input topology not only improves the ICMR but also the trans-conductance of the OTA, which in turn increases the slew rate (SR) and the UGB of the circuit.

The common-mode input voltage range of n-channel input pair is given by

$$V_{DSAT13} + V_{GS1,n} < V_{common,n} < V_{DD} - |V_{DSAT12}| \tag{16}$$

The common-mode input voltage range of p-channel input pair is given by

$$V_{DSAT7} < V_{common,p} < V_{DD} - |V_{DSAT14}| - |V_{GS1,p}| \quad (17)$$

Output swing is given by

$$V_{DSAT2} + V_{DSAT1} < OS < V_{DD} - |V_{DSAT5}| - |V_{DSAT4}| \quad (18)$$

Gain of the OTA is calculated as

$$Av = (gmip1,2 + gmin1,2) \times Rout \quad (19)$$

*Where,*

$$Rout1 = (gm4 \times rds4 \times rds5).(gm6 \times rds6) \quad (20)$$

$$Rout2 = (gm1 \times rds1 \times rds2).(gm3 \times rds3) \quad (21)$$

$$Rout = Rout1 || Rout2 \quad (22)$$

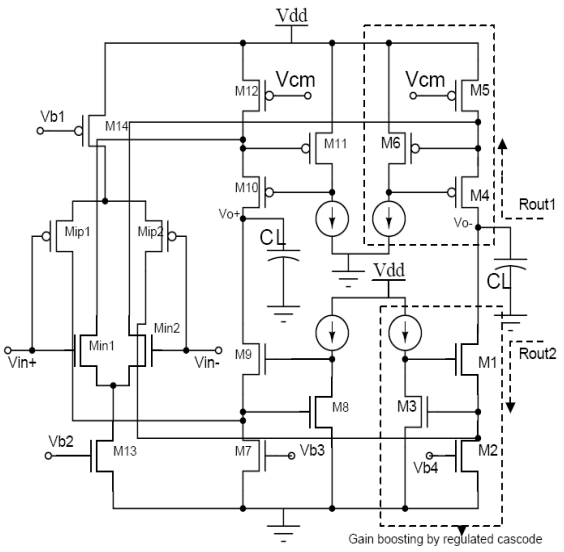


Figure 7. Folded regulated cascode OTA

Also, in order to reduce the power consumption, gain boosting has been performed by using regulated cascode load. When the input CM signal VICM is close to ground, pMOS input pair Mip1 and Mip2 does the trans-conductance action and nMOS input pair Min1 and Min2 goes to cut-off. On the other hand, as VICM reaches near VDD, Min1 and Min2 become effective, while Mip1 and Mip2 remain cut-off. Using regulated cascode load decreases the power consumption and die area usage to a great extent, while keeping the output impedance of the OTA high. As depicted in Fig. 7, transistor M3 and M6 acts as a booster for transistors M1 and M4. Enhancement of the transconductance Gm is evident from Fig.7 where an improvement by a factor of almost 2 can be found (Gm=gm1+gm2≈2gm).

## IV. CMFB CIRCUIT FOR OTA

In the Fig. 8 as shown Voc is very sensitive to mismatches and component variations, and the circuit is not practical from a bias stability standpoint. CM-sense block, the CM detector, calculates the common mode output voltage,

$$V_{OC} = (V_{01} + V_{02})/2 \quad (23)$$

This voltage is subtracted from the desired CM output voltage, VCM. The difference Voc-VCM is scaled by an amplifier with gain $a_{cms}$. Then a dc voltage VCSBIAS is added, and the result is $V_{cms}$, where

$$V_{cms} = a_{cms}(V_{oc} - V_{CM}) + V_{CSBIAS} \quad (24)$$

$V_{cms}$ drives a new op-amp input labeled CMC (for common-mode control). The CMC input is chosen so that changing Vcmc changes Voc but does not affect Vod if the circuit is perfectly balanced [7].

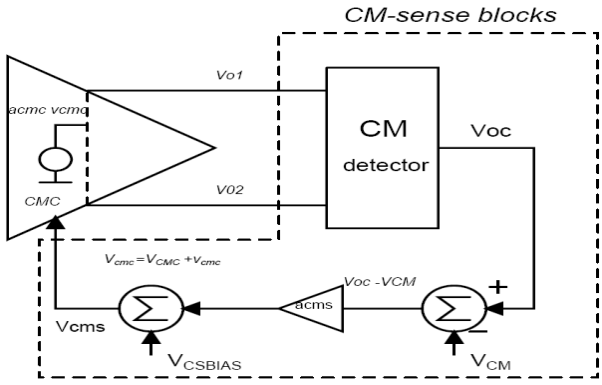


Figure 8. A conceptual block diagram of the CMFB circuit

Above, mentioned CMFB scheme shows good accuracy and it has been chosen while designing the OTAs of the presently discussed ADC. High accuracy of this CMFB circuit also ensures very low input referred offset voltage of the OTA. In order to design an OTA of high resolution accuracy must be of prime concern. The CMFB circuit used in the OTA is shown in Fig. 9. Thus, this CMFB scheme has been preferred over the low power switched-capacitor (SC) CMFB circuit like the one described in [8].

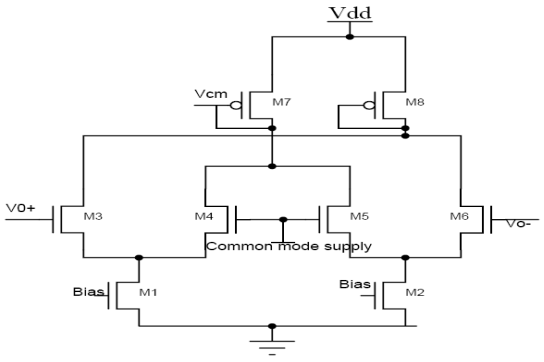


Figure 9. CMFB circuit used in OTA

## V. BANDGAP VOLTAGE REFERENCE (BGR)

Reference voltage or currents that exhibit little dependence on temperature prove essential in many analog circuits. It is interesting to note that, since most process

parameters vary with temperature, if a reference is temperature-independent, then it is usually process-independent as well.

Band gap voltage reference combine the positive TC of the thermal voltage with the negative TC of the diode forward voltage (the band gap energy, Eg of silicon decreases with increasing temperature). Effectively a voltage reference with zero TC, with this voltage reference it is simple matter to generate multiple voltage and current references [9].

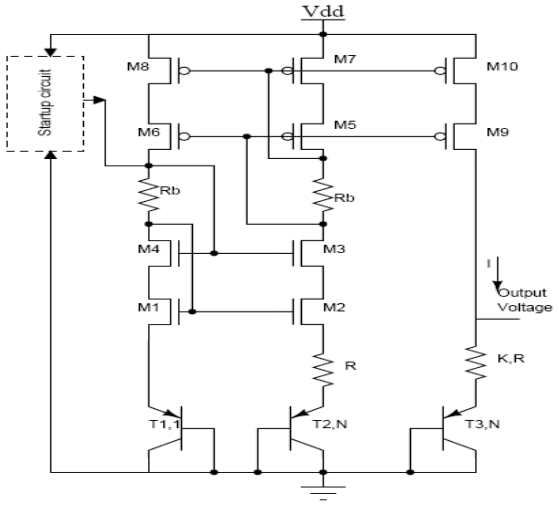


Figure 10. A band gap voltage reference

The circuit shown in the Fig.10 is a simple example of a band gap reference. In addition, this topology is used to reduce the overall power consumption of the OTA. The transistor T3 is a same size as T2. The current 'I' flows in the BGR circuit is given in (25), or

$$I = \frac{nV_T.\ln N}{R} \tag{25}$$

The reference output voltage with respect to ground is given by

$$V_{ref} = I.K.R + V_{BE3} \tag{26}$$

Or,

$$V_{ref} = (K.n.\ln N)V_T + V_{BE3} \tag{27}$$

The temperature coefficient (TC) of the band gap reference is zero when

$$\frac{\partial V_{ref}}{\partial T} = K.n.\ln N \underbrace{\frac{\partial V_T}{\partial T}}_{0.085mV/\circ C} + \underbrace{\frac{\partial V_{BE3}}{\partial T}}_{-1.5mV/\circ C} = 0 \tag{28}$$

For n=1and N=8 the factor K is 8.5 for a zero TC at 300˚K.

## VI. CIRCUIT SIMULATION RESULT

Simulation results of the folded regulated cascode OTA are determined at the typical temperature, and process corners. Frequency analysis of the OTA is shown in Fig. 11. This bode plot shows that dc gain of the OTA is 90.39 dB and gives a UGB of 700.7 MHz with 500fF load capacitance. Phase margin (PM) achieved with this load is 63.85□. Next, settling behavior of the OTA is checked by putting the OTA in a unity-gain closed loop. Transient behavior of the OTA was simulated by applying a 20 MHz square wave to it. Transient response of the OTA is shown in Fig. 12 and the rise time {tr(10%) to tr(90%)} comes out to be 2 ns.

Table: I

THE SPECIFICATIONS OF THE OP-AMP

| **Main characteristics** | **This Work** | **Ref[10]** | **Ref[11]** | **Ref[12]** |
|---|---|---|---|---|
| Power Supply (V) | 1.8 | 2.5 | 3.0 | 3.3 |
| DC Gain (dB) | 90.39 | 102 | 95 | 95 |
| Unity Gain Frequency (MHz) | 700.7 | 822 | 412 | 500 |
| Phase Margin (Degree) | 63.85 | 62.5 | 75 | 55 |
| Input common mode range(V) | 0.5-1.2 | ------ | -------- | ------ |
| Output Swing(V) | 0.5-1.2 | 2 | -------- | ------- |
| Power cons.(mW) | 3.24 | 35 | 12.8 | 14.5 |
| Settling time (ns) | 2 | 3.5 | 7.5 | ------- |
| CMRR(dB) | ≥ 60 | -------- | ------- | ------- |
| Load Capacitance(pF) | 0.5 | 4 | 1.9 | 0.5 |

Settling behavior shows that the settling error is □ =105.3 nV. This error is well within the 10 bits resolution error tolerance of 1.76 mV. The whole performance of the op-amp is shown in Table: I, comparisons with previous designs are also included [10], [11], and [12]. Common Mode Rejection Ratio (CMRR) of an OTA is defined as

$$CMRR(dB) = 20\log\frac{A_d}{A_c} \tag{29}$$

Where Ad, and Ac are differential and common mode gains respectively. This parameter is a measure of how well an OTA can reject the common mode signal at its output. A high CMRR value implies an excellent common mode noise rejection.

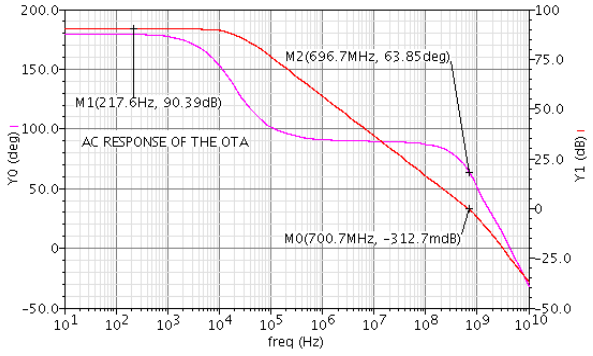


Figure 11. Frequency response of the OTA

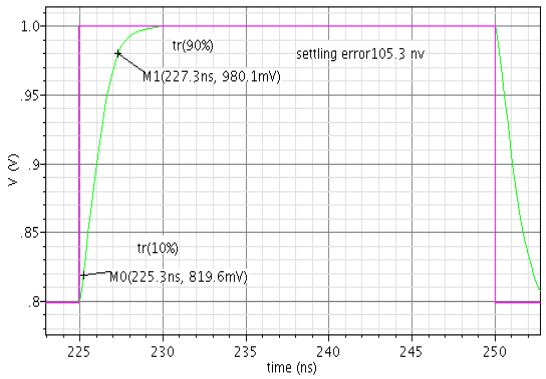


Figure 12. Square wave response of the OTA in unity gain mode

## VII. LAYOUT DESIGN

The layout of the OTA has been done in six metal, epi-digital CMOS n-well process and laid out using Cadence Virtuso. For the layout design, care has been taken for voltage matching and current matching. For the matched transistor common centroid with proper dummy transistor has been put [13]. Only the OTA layout has been shown in the Fig. 13.

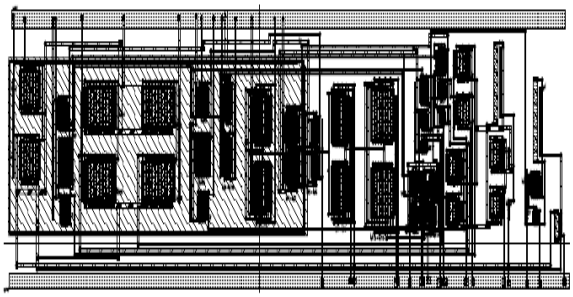

Figure 13. Layout of the OTA

## VIII. CONCLUSION

A differential folded regulated cascode CMOS operational trans-conductance amplifier is designed and simulated using CADENCE SPECTRE simulator, to realize pipelined ADC that requires only a 1.8-V supply voltage. The multilayer OTA chip is shown in Fig. 13. The architecture of parallel pipeline ADC with 2.5 bit per stage except the last stage is 4-bit flash ADC is described in this paper. A low power and fast settling op-amp is also included. Since the optimization of the time-interleaved technique, the op-amp is suitable for the S/H circuit and MDAC module in the 10bit, 150Msample/s 2-channel pipeline ADC. The total power consumed by this proposed op-amp is only 3.24 mW, which reduces the total power consumption of the parallel pipeline ADC significantly.

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