A Cascode Miller-Compensated Three-Stage Amplifier With Local Impedance Attenuation for Optimized Complex-Pole Control

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***Abstract*—This work presents a power- and area-efficient three-stage amplifier that is able to drive a large capacitive load. Removing the inner Miller capacitor and employing cascode Miller compensation in the outer compensation loop could extend the complex-pole frequency of a three-stage amplifier, but result in a high Q-factor. A local impedance attenuation block consisting of a series *RC* network is proposed to control the complex poles. This block attenuates the high-frequency resistance at the second-stage output and achieves an optimized tradeoff between the frequency and the Q-factor of the complex poles. As the low-frequency resistance remains unchanged, a high dc gain is maintained. Implemented in 0.13 μm CMOS process, the proposed design occupies an area of 0.0032 mm^2 and consumes a quiescent current of 10.5 μA. When driving a 560 pF capacitive load, it achieves a unity-gain frequency of 3.49 MHz, an average slew rate of 0.86 V/μs, and an average settling time of 0.9 μs.**

***Index Terms*—Cascode Miller compensation, complex poles, frequency compensation, large capacitive load, local impedance attenuation, Miller compensation, multistage amplifier, Q-factor.**

I. Introduction

MULTISTAGE amplifier design has always been an important research topic. As the sizes of devices shrink, the supply voltage becomes lower and the per-stage gain decreases. Cascode topology is no longer suitable for low-voltage design and multistage amplifiers have to be used to achieve sufficient DC gain. Multistage amplifiers can be very power-efficient in driving a large capacitive load, and some even achieve better relative bandwidth than single-stage amplifiers [1], [2]. Various analog circuits, such as output-capacitor-free (OCF) low-dropout regulators (LDRs) and active-matrix LCD column drivers, can be modeled as multistage amplifiers driving a large capacitive load. Many techniques developed for multistage amplifiers, such as damping-factor-control frequency compensation (DFCFC) [1] and active-feedback frequency-compensation (AFFC) [2], all find applications in OCF LDR designs [3], [4]. Despite the usefulness of multistage amplifiers, they suffer from stability problems. A three-stage amplifier has at least three high-impedance nodes, and each contributes a pole. Poor design could easily place these poles at low frequency and cause stability problems. Various frequency compensation techniques have been developed to ensure system stability [1], [2], [5]–[13]. Most of these structures are derived from the nested Miller compensation (NMC) [14] structure that uses simple Miller compensation in both of its inner compensation loop and outer compensation loop. In [1], [6], [8], and [12] , the inner Miller capacitor is eliminated. In [2], [9]–[11], simple Miller compensation in the outer compensation loop is replaced by more advanced compensation techniques such as cascode Miller compensation or current-buffer Miller compensation. Many of these designs suffer from either a limited complex-pole frequency ω_o or a large Q-factor. In this work, we eliminate the inner Miller capacitor and use cascode Miller compensation [15] in the outer compensation loop to increase ω_o, and employ a local impedance attenuation (LIA) block that consists of a series RC network at the output of the second stage [8] to control the complex poles. The proposed cascode local impedance attenuation (CLIA) design is able to achieve an optimized tradeoff between ω_o and the Q-factor.

The remainder of this paper is organized as follows. In Section II, we identify the major challenge of three-stage amplifier design and propose a method to address this challenge. In Section III, we discuss the structure, design considerations and implementation of the proposed design. In Section IV, we show the measurement results along with related discussions. In Section V, we conclude the design efforts.

II. Complex-Pole Control

Due to the high-impedance node at the output of each gain stage, a three-stage amplifier has at least three poles. Frequency compensation techniques redistribute the positions of the poles to ensure stability. In general, simple Miller compensation or its variants, such as RC Miller compensation, cascode Miller compensation and current-buffer Miller compensation, connects a compensation capacitor between the outputs of the first and the final stages to form the outer compensation loop. In some designs [6], [8], [10], one or two feed-forward paths are added to form a push-pull output stage to improve the transient performance or to create left half-plane zeros to improve frequency responses. The unity-gain frequency (UGF) of a three-stage amplifier, therefore, depends on the locations of the non-dominant poles and the availability of left half-plane zeros. It is desirable to push the non-dominant poles to high frequency or cancel

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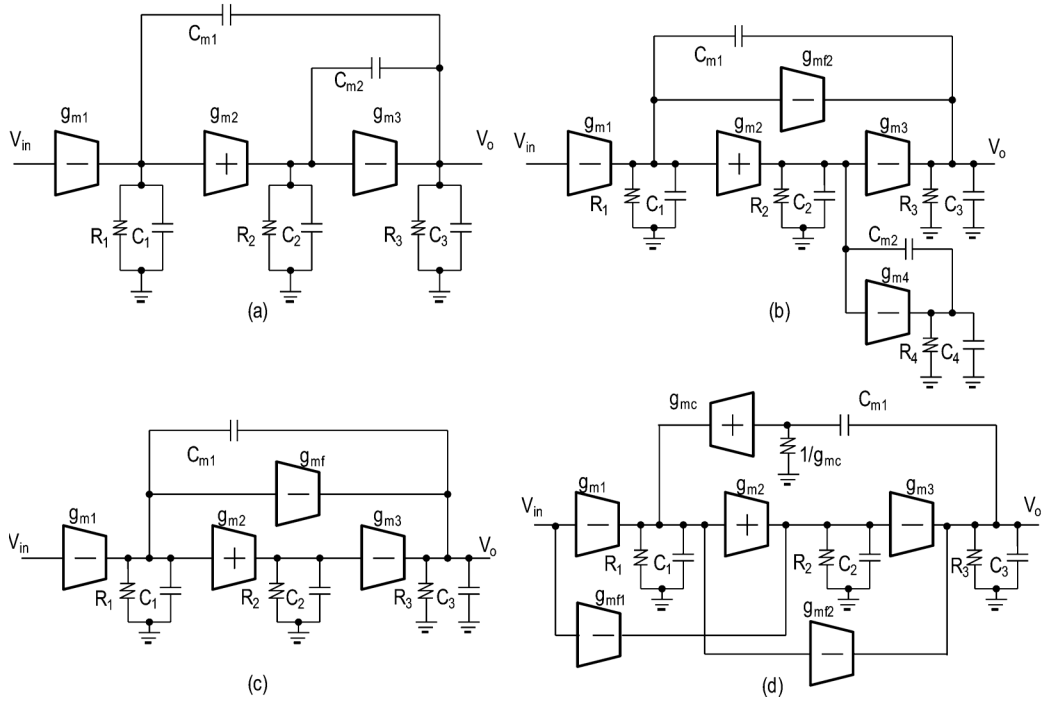

Fig. 1. Structures of some previous designs. (a) NMC amplifier. (b) DFCFC amplifier. (c) SMC amplifier. (d) CFCC amplifier.

them with left half-plane zeros in order to achieve a high UGF. In many designs, the non-dominant poles are complex poles and complete cancellation of a complex pole-pair with zeros is normally not possible. The key to UGF extension is therefore the control of the complex poles, that is, to increase the frequency of the complex poles ω_o and suppress the Q-factor. However, they are usually interrelated and cannot be controlled independently. Reducing the Q-factor is usually accompanied with the reduction of ω_o as well, and it is a major challenge to satisfy the conflicting requirements of increasing ω_o and suppressing the Q-factor at the same time. An optimized complex-pole control scheme should maintain a low Q-factor but keep ω_o as high as possible. It should also be area- and power-efficient as well as robust to process variations and device mismatches. In the following paragraphs, we review briefly some previous methods for controlling the complex poles.

Nested Miller compensation (NMC) [14] is the earliest and simplest frequency compensation structure for a three-stage amplifier that provides an effective way to control the complex poles. Fig. 1(a) shows the structure of NMC. The complex-pole frequency and its Q-factor are expressed as

$$\omega_o|_{\rm NMC} = \sqrt{\frac{g_{m2}g_{m3}}{C_{m2}C_3}} \tag{1}$$

and

$$Q|_{\rm NMC} = \frac{1}{g_{m3}-g_{m2}}\sqrt{\frac{g_{m2}g_{m3}C_3}{C_{m2}}} \tag{2}$$

where the parameters are easily identified in Fig. 1(a). The two Miller capacitors are relatively large that limit $\omega_o|_{\rm NMC}$ and thus the UGF of the amplifier, although the resulting Q-factor is low. Multi-gain-stages provide sufficient dc gain, but the UGF of the NMC amplifier is actually inferior to that of a single-stage or a two-stage amplifier. In NMC, $\omega_o|_{\rm NMC}$ is inversely proportional to $\sqrt{C_{m2}}$. It is therefore desirable to reduce or even eliminate C_{m2} in order to extend $\omega_o|_{\rm NMC}$. When C_{m2} is eliminated, the complex poles can be controlled either by using an additional control circuitry or by optimizing the design parameters. Fig. 1(b) shows the damping-factor-control frequency compensation (DFCFC) [1] structure. The complex-pole frequency and its Q-factor are

$$\omega_o|_{\rm DFCFC} = \sqrt{\frac{(g_{m2}g_{m3}+g_{mf2}g_{m4})}{C_2C_3}} \tag{3}$$

and

$$Q|_{\rm DFCFC} = \frac{1}{g_{m4}}\sqrt{\frac{(g_{m2}g_{m3}+g_{mf2}g_{m4})\,C_2}{C_3}} \tag{4}$$

where the parameters are easily identified in Fig. 1(b). By adjusting the value of g_{m4} in the damping-factor-control block, this structure is able to control the complex poles. With optimized design parameters as in the single-capacitor Miller compensation (SMC) structure [6] shown in Fig. 1(c), the Q-factor can even be reduced to 0.5 and the complex poles become two real poles. In general, the non-dominant poles are complex, and its frequency and Q-factor are calculated as

$$\omega_o|_{\rm SMC} = \sqrt{\frac{g_{m2}g_{m3}}{C_2C_3}} \tag{5}$$

and

$$Q|_{\rm SMC} = R_2\sqrt{\frac{g_{m2}g_{m3}C_2}{C_3}} \tag{6}$$

where the parameters are easily identified in Fig. 1(c). The complex-pole frequency of SMC is $\sqrt{C_{m2}/C_2}$ times higher than that of NMC, and is on the same order of that of DFCFC provided that $g_{m2}g_{m3}$ is much larger than $g_{mf2}g_{m4}$.

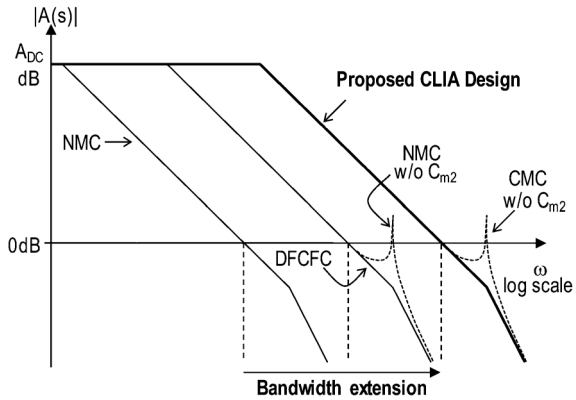

Fig. 2. Bandwidth extension in multistage amplifiers.

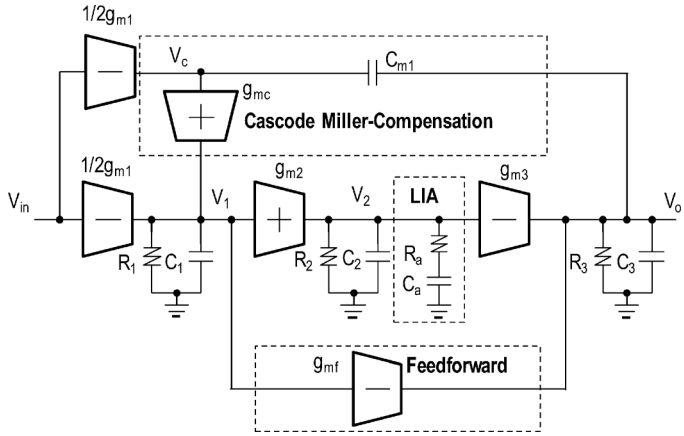

Fig. 3. Structure of the proposed three-stage amplifier.

The complex-pole frequency of SMC can further be extended by replacing simple Miller compensation by cascode Miller compensation (CMC). The resulting structure without the inner Miller capacitor C_{m2} is combined with one additional feed-forward path to form the cross feed-forward cascode compensation (CFCC) structure [10]. Fig. 1(d) shows the structure of CFCC. Provided that the additional feed-forward path does not modify ω_o, the complex-pole frequency and the Q-factor of the CMC-without-C_{m2} structure is the same as that of the CFCC structure and is given by

$$\omega_o|_{CFCC} = \sqrt{\frac{g_{m2}g_{m3}g_{mc}R_2}{C_1C_3}} \tag{7}$$

and

$$Q|_{CFCC} = C_{m1}\sqrt{\frac{g_{m2}g_{m3}R_2}{g_{mc}C_1C_3}} \tag{8}$$

where the parameters are easily identified in Fig. 1(d). Comparing (7) to (5) and (8) to (6), we find that replacing simple Miller compensation with cascode Miller compensation in the outer compensation loop improves the complex-pole frequency by a factor of approximately $\sqrt{g_{mc}R_2C_2/C_1}$, but results in a high Q-factor. In CFCC, a parasitic capacitor as large as several hundred fF at the output of the first stage is used to suppress the Q-factor and to lower the frequency of the second zero for improved frequency response. Designs such as those discussed in [9] and [16] also rely on a large capacitor at some internal nodes to control the complex poles to ensure stability. They use dedicated physical capacitors instead of parasitic capacitors. However, a large C_1 at the output of the first stage is likely to degrade both the small-signal and the large-signal performance, as will be explained in more details in Section III-C.

As shown in Fig. 2, removing the inner compensation capacitor increases the complex-pole frequency dramatically, but can result in a high Q-factor. DFCFC provides a way to control ω_o and its Q-factor to ensure stability. Replacing simple Miller compensation with cascode Miller compensation in the outer compensation loop further improves the complex-pole frequency, but also suffers from a high Q-factor. To fully exploit the benefit of cascode Miller compensation, a local impedance attenuation block is proposed to achieve an optimized control of the complex poles.

III. Proposed CLIA Amplifier

A. Structure

Fig. 3 shows the structure of the proposed three-stage amplifier. It consists of two inverting gain stages, a non-inverting gain stage, a cascode Miller compensation block, a local impedance attenuation block and a feed-forward block. With three gain stages in cascade, the amplifier has a high dc gain. Cascode Miller compensation eliminates the feed-forward signal path that exists in simple Miller compensation, creates a left half-plane zero and extends the complex-pole frequency. The LIA block consists of a series *RC* network (R_a and C_a). It reduces the high-frequency small-signal resistance at the second-stage output and provides an effective and robust way to control the complex poles. The Q-factor of the complex poles is modified to be proportional to $\sqrt{R_a}$ instead of $\sqrt{R_2}$ that is usually very large for low-power design. Since the low-frequency small-signal resistance at the second-stage output remains unchanged, a high dc gain is still maintained. There is a feed-forward path from the first-stage output to the last-stage input that enables a push-pull operation at the final stage and improves large-signal performance.

The proposed design appears to have common features with the impedance adapting compensation (IAC) structure [8] and the CFCC structure [10]; however, they differ from one another in a number of important ways and the same circuit block may even serve different purposes. In the IAC structure [8], a series *RC* network is used to split two nondominant real poles. In the proposed design, it is used to control the complex poles. According to [8], the first nondominant real pole is canceled by a zero for stability, and the large R pushes the second non-dominant real pole to high frequency, and the UGF can be extended. However, a large series resistor occupies more silicon area and results in larger parasitic capacitance at the output of the second stage, thus lowering the frequency of the third non-dominant pole. Furthermore, with a large series resistor, the pole-zero cancellation occurs at a low frequency that degrades settling times of the transient responses. The series resistor is chosen to be 750 kΩ in [8]. In the proposed design, a series resistor of 240 kΩ is used. The IAC structure uses simple Miller compensation, while

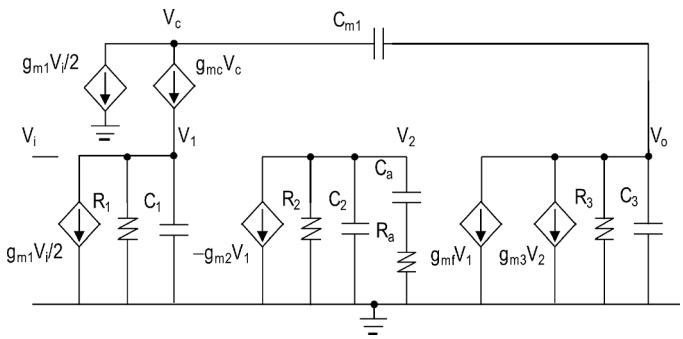

Fig. 4. Small-signal equivalent circuit of the proposed structure.

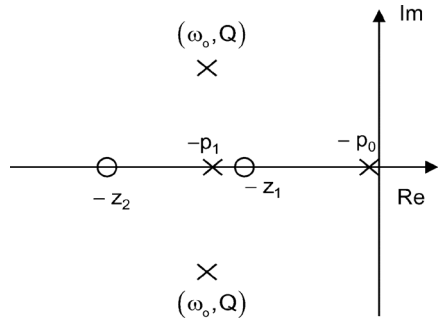

Fig. 5. Pole-zero distribution of the proposed design.

the proposed design uses cascode Miller compensation that extends the complex-pole frequency significantly, as will be explained in Section III-D. Compared with CFCC that has two feed-forward paths and a parasitic capacitor of several hundred fF to suppress the Q-factor, the proposed design has only one feed-forward path and uses a local impedance attenuation block to control the complex poles. The location of the second zero in CFCC is a function of the lumped parasitic capacitor at the first-stage output node. To move this zero to lower frequency, that parasitic capacitor has to be large.

B. Gain Function

Fig. 4 shows the equivalent small-signal circuit of the proposed design. The parameters g_{mi}, R_i, and C_i are the transconductance, output resistance and lumped output capacitance at the i^{th} gain stage, g_{mc} and g_{mf} are the transconductances of the cascode stage and the feed-forward block, and R_a and C_a are the resistance and capacitance of the LIA block. We note that capacitor C_3 includes both the parasitic capacitor at the last-stage output and the load capacitor C_L. The following facts are used to simplify the derivation of the gain function.

1) The per-stage gain $g_{mi}R_i$ of each i^{th} stage is much greater than 1.
2) The compensation capacitor C_{m1}, the LIA capacitor C_a and the last-stage capacitor C_3 are much larger than the lumped capacitances C_1 and C_2.

The gain function of the proposed amplifier is then given by

$$\begin{aligned}\frac{v_o}{v_i} &\approx \frac{A_{DC}\left(1+\frac{s}{z_1}\right)\left(1+\frac{s}{z_2}\right)}{\left(1+\frac{s}{p_0}\right)\left(1+\frac{s}{p_1}\right)\left(1+\frac{1}{Q}\frac{s}{\omega_o}+\frac{s^2}{\omega_o}\right)} \\ &= \frac{g_{m1}g_{m2}g_{m3}R_1R_2R_3(1+sR_aC_a)}{(1+sg_{m2}g_{m3}R_1R_2R_3C_{m1})(1+skR_aC_a)} \\ &\quad\times \frac{\left(1+\frac{sC_{m1}}{2g_{mc}}\right)}{\left(1+\frac{sC_1C_3}{kg_{m2}g_{m3}R_aC_{m1}}+\frac{s^2C_1C_3}{kg_{m2}g_{m3}g_{mc}R_a}\right)}\end{aligned} \tag{9}$$

where k is defined as

$$k = 1+\frac{C_3}{g_{m2}g_{m3}R_1R_aC_{m1}} \approx 1. \tag{10}$$

We identify p_1 and z_1 as

$$p_1 = \frac{1}{kR_aC_a} \tag{11}$$

and

$$z_1 = \frac{1}{R_aC_a}. \tag{12}$$

Pole-zero cancellation of $-p_1$ and $-z_1$ gives

$$\begin{aligned}\frac{v_o}{v_i} &\approx \frac{g_{m1}g_{m2}g_{m3}R_1R_2R_3}{(1+sg_{m2}g_{m3}R_1R_2R_3C_{m1})} \\ &\quad\times \frac{\left(1+\frac{sC_{m1}}{2g_{mc}}\right)}{\left(1+\frac{sC_1C_3}{g_{m2}g_{m3}R_aC_{m1}}+\frac{s^2C_1C_3}{g_{m2}g_{m3}g_{mc}R_a}\right)}.\end{aligned} \tag{13}$$

The dc gain A_{DC} and the dominant pole $-p_0$ are given by

$$A_{DC} = g_{m1}g_{m2}g_{m3}R_1R_2R_3 \tag{14}$$

and

$$p_0 = \frac{1}{g_{m2}g_{m3}R_1R_2R_3C_{m1}}. \tag{15}$$

The complex-pole frequency ω_o and the Q-factor are

$$\omega_o = \sqrt{\frac{g_{m2}g_{m3}g_{mc}R_a}{C_1C_3}} \tag{16}$$

and

$$Q = C_{m1}\sqrt{\frac{g_{m2}g_{m3}R_a}{g_{mc}C_1C_3}}. \tag{17}$$

The second zero $-z_2$ is created by the cascode Miller compensation that helps increase the phase margin and is given by

$$z_2 = \frac{2g_{mc}}{C_{m1}}. \tag{18}$$

Fig. 5 shows the pole-zero distribution of the proposed design.

C. Necessity and Effectiveness of the Proposed Complex-Pole-Control Method

Without local impedance attenuation, the corresponding ω_o and Q-factor are given, respectively, by

$$\omega_o|_{\text{no LIA}} = \sqrt{\frac{g_{m2}g_{m3}g_{mc}R_2}{C_1C_3}} \tag{19}$$

and

$$Q|_{\text{no LIA}} = C_{m1}\sqrt{\frac{g_{m2}g_{m3}R_2}{g_{mc}C_1C_3}}. \tag{20}$$

The capacitor C_3 is mainly due to the load capacitor. To reduce the Q-factor, we either need to reduce C_{m1}, g_{m2}, g_{m3} and R_2

or increase g_{mc} and C_1. Unfortunately, these parameters are in general interrelated, and they may not be adjusted independently to optimize the frequency response. Even though, it would still be helpful to have a qualitative understanding on how each parameter affects ω_o and the Q-factor. The transconductance and the small-signal resistance can be modified by adjusting the bias current. In general, the lumped capacitance at each node can be modified by changing the size of some related devices or by adding a dedicated physical capacitor. Reducing g_{m2} and g_{m3} will lower ω_o and reduce the slew rate, and will also increase the small-signal resistance at related nodes if the bias currents are reduced. Although increasing g_{mc} increases ω_o and reduces its Q-factor, the bias current has to be increased and is therefore not power-efficient. A large g_{mc} will also push the associated left half-plane zero to high frequency and reduce the phase margin. A smaller R_2 can be achieved by using a large bias current, but is likely to modify the second-stage transconductance as well. Decreasing C_{m1} will move the dominant pole to a higher frequency and stability issue arises. A large C_1 degrades both large- and small-signal performances. A large C_1 violates the usual assumption that C_1 is much smaller than the compensation capacitors and the load capacitor, thus complicating the analysis as high-order terms involving C_1 can no longer be ignored. These high-order effects will reduce the UGF of the design significantly, as can be easily verified by computer simulations. The bias current at the first stage is usually relatively small so that the gain-bandwidth product (GBW), calculated as g_{m1}/C_{m1}, is below the frequencies of the non-dominant poles to maintain sufficient phase margin. With a small bias current at the first stage, a large C_1 will limit the slew rate at the output of the first stage.

To fully exploit the benefit of cascode Miller compensation, a method to achieve optimized control of the complex poles is required. By using the local impedance attenuation block, ω_o and its Q-factor are modified to be proportional to $\sqrt{R_a}$ instead of $\sqrt{R_2}$. Fig. 6 shows how the complex poles vary with R_a when the series capacitance C_a is set to 0.347 pF. By adjusting R_a, we are able to achieve an optimized tradeoff between ω_o and the Q-factor. The local impedance attenuation block does not consume any quiescent current and therefore provides a power-efficient way to control the complex poles. We choose R_a to be 240 kΩ in our final design. The frequency responses of two different cases are plotted in Fig. 7 for comparison. Without the LIA block, the complex poles exhibit a high Q-factor and may even move to the right half-plane. With the LIA block, the Q-factor is reduced and the overall frequency response is optimized.

D. Benefits of Cascode Miller Compensation

By replacing cascode Miller compensation by simple Miller compensation, the proposed design reduces to the IAC structure if the resulting nondominant poles are real poles. To demonstrate the benefits of cascode Miller compensation over simple Miller compensation, both cases are simulated with all the devices parameters being the same except the compensation capacitor C_{m1}. The design with simple Miller compensation becomes unstable if the same C_{m1} is used. The resulting system can be made stable by increasing C_{m1} to 1.24 pF, but the UGF is reduced to 0.7 MHz. Fig. 8 shows the simulation results. Compared to the design with simple Miller compensation, the design with cascode Miller compensation reduces C_{m1} by five times while increases the UGF by five times.

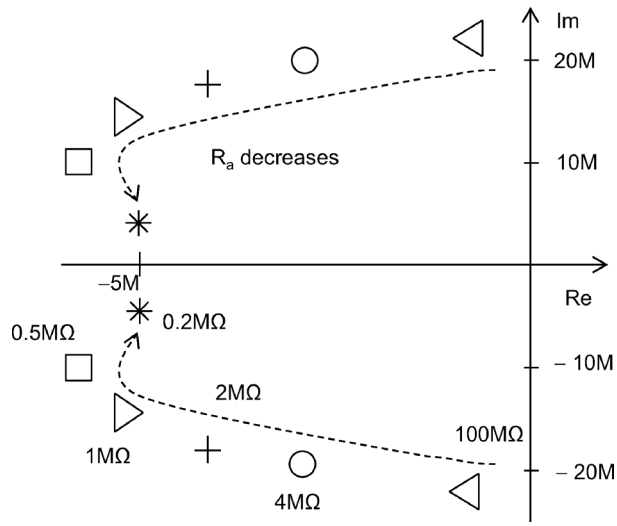

Fig. 6. Complex-pole movement as a function of R_a.

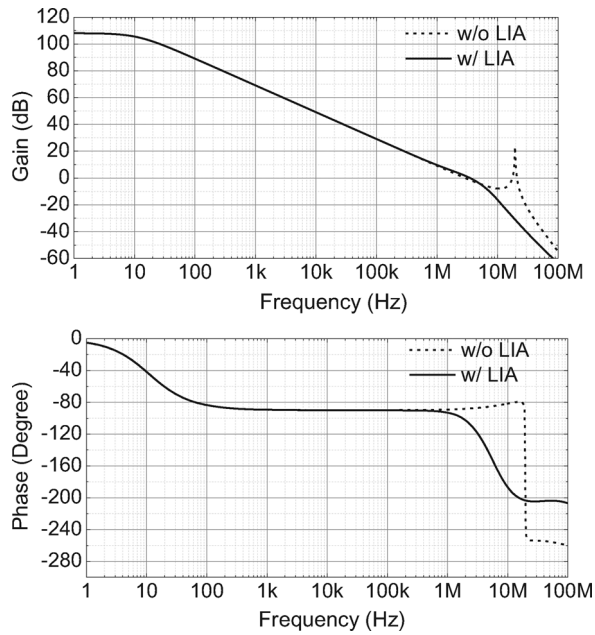

Fig. 7. Frequency responses with LIA and without LIA.

E. Stability and UGF Optimization

The stability condition of an amplifier is usually specified by gain margin and phase margin. In general, there can be many realizations that satisfy the stability condition for a given topology as there can be more free parameters than the constraints. Conventionally, most of the parameters are assumed to be fixed and equations are set up to solve for the remaining free parameters. In our design flow, we assume that R_a is fixed and identify g_{mc}, C_{m1}, C_a and ω_o as free parameters. For a maximally-flat frequency response, the Q-factor is $1/\sqrt{2}$. The UGF can be expressed as $\omega_{UGF} \approx g_{m1}/C_{m1}$ if single-pole roll-off frequency response is assumed. To maintain a phase margin

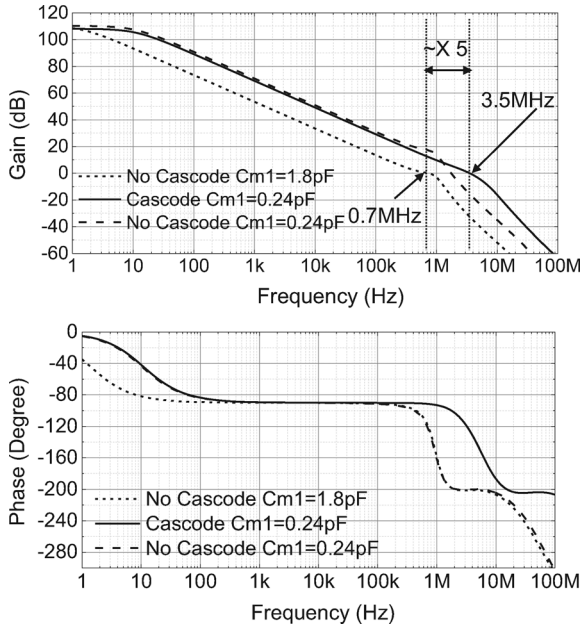

Fig. 8. Frequency responses with cascode Miller-compensation and with simple Miller-compensation.

(PM) of 60°, ω_o has to be $2\sqrt{2}\omega_{UGF}$ ($\omega_{UGF} = 2\pi \times UGF$, in rad s^{-1}) if zeros and high-frequency poles are ignored. There is one left half-plane zero after pole-zero cancellation of p_1 and z_1. This zero boosts the phase margin of the amplifier, and we can have ω_o lower than $2\sqrt{2}\omega_{UGF}$ while still maintain sufficient phase margin. As z_1 locates at a lower frequency than p_1, the phase margin is further increased and the UGF is extended. Let $\omega_o = M\omega_{UGF}$ with $M < 2\sqrt{2}$. Taking into account of the effect of the pole-zero cancellation, the UGF can be adjusted as $\omega_{UGF} \approx (p_1/z_1)(g_{m1}/C_{m1}) = \alpha g_{m1}/C_{m1}$. We note that α is equal to k that is defined in (10). The pole-zero cancellation is designed at a frequency close to ω_{UGF} such that it has negligible effect on the settling times. Let $z_1 \approx \beta\omega_{UGF}$ with β close to 1. With the assumptions above, the following constraints are established:

$$Q = \frac{1}{\sqrt{2}} \approx C_{m1}\sqrt{\frac{g_{m2}g_{m3}R_a}{g_{mc}C_1C_3}}, \tag{21}$$

$$\omega_o = M\omega_{UGF} \approx \alpha M\frac{g_{m1}}{C_{m1}}, \tag{22}$$

$$\omega_o = \sqrt{\frac{g_{m2}g_{m3}g_{mc}R_a}{C_1C_3}}, \tag{23}$$

$$z_1 = \frac{1}{R_aC_a} \approx \beta\omega_{UGF}. \tag{24}$$

Solving the equations above, we obtain

$$g_{mc} = \sqrt{2}\alpha M g_{m1}, \tag{25}$$

$$C_{m1} = \frac{1}{2^{1/4}}\sqrt{\frac{\alpha M g_{m1}C_1C_3}{g_{m2}g_{m3}R_a}}, \tag{26}$$

and

$$C_a = \frac{1}{2^{1/4}}\frac{1}{\beta R_a}\sqrt{\frac{MC_1C_3}{\alpha g_{m1}g_{m2}g_{m3}R_a}}. \tag{27}$$

The phase margin of the proposed design with pole-zero cancellation is given by

$$\begin{aligned} PM &\approx 180^\circ - \varphi(p_0) - \varphi(\omega_o) + \varphi(z_2) \\ &\approx 90^\circ - \tan^{-1}\left(\frac{\frac{\omega_{UGF}}{Q\omega_o}}{1 - \frac{\omega_{UGF}{}^2}{\omega_o{}^2}}\right) + \tan^{-1}\left(\frac{\omega_{UGF}}{z_2}\right). \end{aligned} \tag{28}$$

In deriving the equations above, high-order effects are ignored, approximations are used and some parameters can be layout dependent. The equations above can be used as guidelines during the design process, and accurate design parameters have to be determined with the assistance of computer simulations. The initial value of R_a can be obtained by sweeping the parameter as shown in Fig. 6. It may take several iterations to arrive at an optimized design. In the final design, we choose R_a to be 240 kΩ; and g_{mc}, C_{m1} and C_a are 18.74 μA/V, 0.24 pF, and 0.347 pF, respectively.

F. Transient Responses

The settling time of an amplifier consists of a slewing period and a quasi-linear period [17], [18]. The slew rate of an amplifier is limited by the values of the lumped capacitors at related nodes and the currents available to drive these capacitors. The compensation capacitor C_{m1} at the cascode node and the capacitor C_3 at the final stage output node limit the slew rate of the proposed design. We denote the currents available to drive C_3 and C_{m1} as I_{load} and I_{comp}, respectively. The slew rate SR of the amplifier is

$$SR \approx \min\left(\frac{I_{load}}{C_3}, \frac{I_{comp}}{C_{m1}}\right). \tag{29}$$

With a large load capacitor, I_{load}/C_3 is much smaller than I_{comp}/C_{m1} and the slew rate is limited by the load capacitor. The transient behavior during the quasilinear period depends on both the phase margin and the location of the pole-zero doublet. The phase margin is a function of the load capacitance and can only be optimized for a fixed load capacitor. In the proposed design, pole-zero cancellation is designed at a frequency close to ω_{UGF} so that they have negligible effect on the settling time.

G. Implementation

Fig. 9 shows the circuit implementation of the proposed design. The first stage is realized by transistors M_{10}-M_{18} where M_{11} and M_{12} are the input differential pair and M_{16} is the cascode transistor. The transconductance of the input differential pair and the cascode transistor are g_{m1} and g_{mc}, respectively. The noninverting second stage is realized by transistors M_{21}-M_{26}. Transistor M_{22} is used to increase the transconductance of the second stage [8]. The matching ratio between M_{23} and M_{24} is 1:3. Transistors M_{25} and M_{26} form a cascode configuration and provide the bias current to this stage. The transconductances of M_{21}, M_{23} and M_{24} are g_{m21}, g_{m23} and g_{m24}, respectively. The overall transconductance g_{m2} of the second stage is therefore $(g_{m21}/g_{m23})g_{m24}$. The third-stage consists of transistors M_{31} and M_{32}. Transistor M_{31} is connected to the first-stage output to form a feed-forward path, and M_{31} and M_{32} form a push-pull configuration to improve the slew rate. The

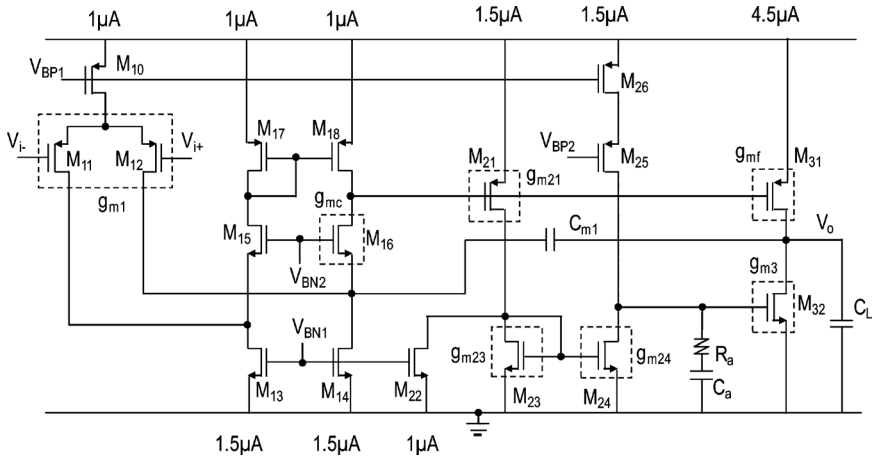

Fig. 9. Circuit implementation of the proposed design.

TABLE I
COMPONENT VALUES

M_{10}	2×(1/2)	M_{21}	2/0.2	M_{26}	3×(1/2)	R_a	247.56kΩ
M_{11},M_{12}	2/6	M_{22}	2×(0.4/3)	M_{31}	3×(2/0.2)	C_a	0.347pF
M_{17},M_{18}	2/1	M_{23}	0.5/0.5	M_{32}	2/0.2		
M_{15},M_{16}	1/1	M_{24}	3×(0.5/0.5)	C_L	560pF		
M_{13},M_{14}	3×(0.4/3)	M_{25}	3×(1/1)	C_{m1}	0.24pF		

Transistor sizes in μm/μm

TABLE II
CIRCUIT PARAMETERS

g_{m1}	4.34μA/V	g_{mf}	90.74μA/V	C_L	560pF
g_{m2}	89.15μA/V	g_{mc}	18.74μA/V	R_a	247.56kΩ
g_{m3}	100.8μA/V	C_{m1}	0.24pF	C_a	0.347pF

cascode Miller compensation capacitor C_{m1} is connected between the amplifier output and the source terminal of M_{16}. The local impedance attenuation block, consisting of a series capacitor C_a and a series resistor R_a, is connected to the output of the second stage. The transistor sizes and related design parameters are provided in Tables I and II, respectively.

IV. MEASUREMENT RESULTS AND DISCUSSIONS

The proposed design is fabricated in 0.13 μm CMOS technology, occupies a silicon area of 0.0032 mm^2 and its core circuitry consumes a quiescent current of 10.5 μA. The total on-chip capacitance is 0.587 pF (C_a = 0.347 pF, C_{m1} = 0.24 pF). Fig. 10 shows the measured frequency responses of the proposed amplifier with a load capacitor of 330, 560, 680, and 890 pF, respectively. The UGF decreases from 4.21 to 3.37 MHz, and the phase margin decreases from 58° to 38° as the load capacitor increases from 330 to 890 pF. Corner and Monte Carlo simulations are carried out to verify the robustness of the proposed design. The phase margins, gain margins, and UGFs at different corners and temperatures are simulated, and the results are summarized in Table III. A 3-σ Monte Carlo simulation results over process variations and

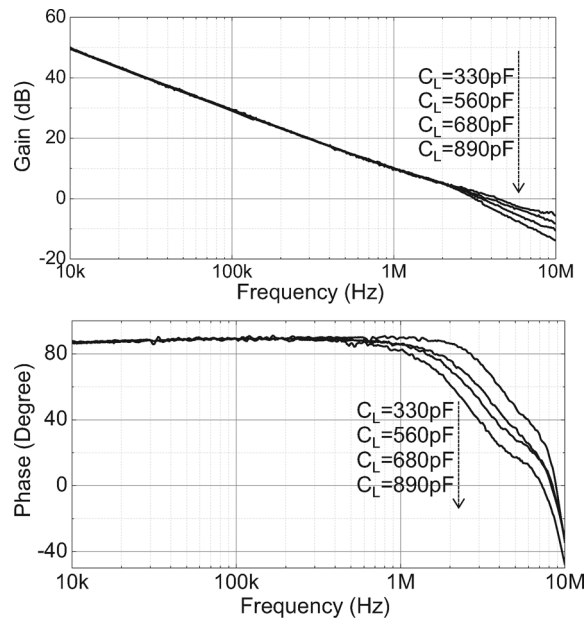

Fig. 10. Measured frequency responses.

device mismatches is summarized in Table IV. The load capacitor C_L of 560 pF is used in these simulations. Fig. 11 shows the measured transient responses to a 500 mV input step with the amplifier connected in unity-gain feedback configuration. Average slew rates of 1.35, 0.86, 0.67, and 0.57 V/μs are achieved with load capacitors of 330, 560, 680, and 890 pF, respectively.

To quantify the performance of an amplifier, several figure-of-merits are used. The small-signal figure-of-merit ($\mathrm{FoM_S}$) and large-signal figure-of-merit ($\mathrm{FoM_L}$) [9] are defined as

$$\mathrm{FoM_S} = \frac{\mathrm{UGF} \times C_3}{\mathrm{Power}} \tag{30}$$

and

$$\mathrm{FoM_L} = \frac{\mathrm{SR} \times C_3}{\mathrm{Power}}. \tag{31}$$

For designs whose slew rates are limited by internal capacitors, $\mathrm{FoM_L}$ is linearly proportional to C_3, while for designs whose

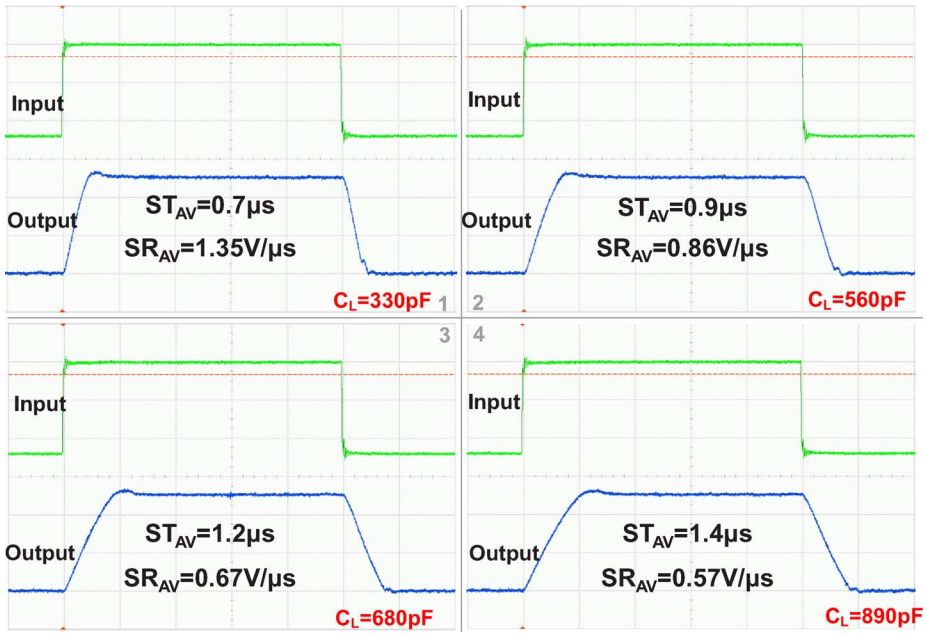

Fig. 11. Measured transient responses.

TABLE III
SIMULATION RESULTS AT DIFFERENT CORNERS AND TEMPERATURES

Corner	TT	FF	SS	SNFP	FNSP
T=–40°C					
PM (deg)	63.14	62.17	64.34	63.85	62.67
GM (dB)	5.705	4.6	6.412	4.503	6.646
UGF (MHz)	3.787	3.8	3.708	3.791	3.746
T=27°C					
PM (deg)	56.27	55.88	57.16	57.3	55.62
GM (dB)	6.549	6.21	6.755	5.951	7.058
UGF (MHz)	3.519	3.492	3.484	3.505	3.492
T=85°C					
PM (deg)	47.6	48.58	47.59	49.26	46.53
GM (dB)	6.69	6.952	6.49	6.535	6.857
UGF (MHz)	3.34	3.234	3.359	3.302	3.331

TT=Typical: FF=Fast NMOS & Fast PMOS:SS=Slow NMOS & Slow PMOS; FNSP=Fast NMOS & Slow PMOS; SNFP=Slow NMOS & Fast PMOS.

TABLE IV
3-σ MONTE CARLO SIMULATION RESULTS OVER PROCESS VARIATIONS AND DEVICES MISMATCHES

	PM (deg)	GM (dB)	UGF (MHz)	I_Q(μA)
Average	56.75	6.01	3.51	10.57
Standard Deviation	4.69	1.54	0.1	0.83
# of Runs	100	100	100	100

slew rates are limited by the load capacitor, $\mathrm{FoM_L}$ remains invariant regardless of the value of C_3 but can be increased by increasing the driving capability of the last stage, which can be achieved by increasing the sizes of the last-stage transistors. The slew rate of the proposed amplifier is limited by the load capacitor and $\mathrm{FoM_L}$'s of the measured results remain almost constant for different values of C_3. The complex-pole frequency ω_o is inversely proportional to $\sqrt{C_3}$ and the UGF can be regarded as a

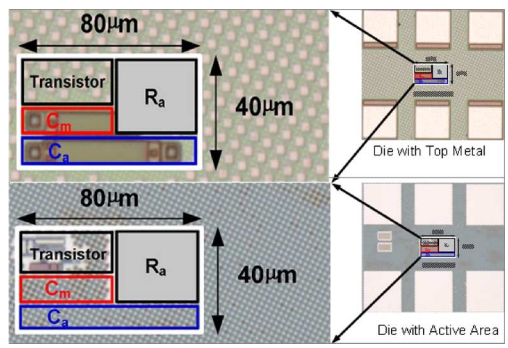

Fig. 12. Die microphotograph.

linear function of ω_o. As $\mathrm{FoM_S}$ roughly scales proportionally to $\sqrt{C_3}$ [9], one may obtain a better $\mathrm{FoM_S}$ by simply using a larger load capacitor. For fair comparison, a normalized small-signal figure-of-merit defined as $\mathrm{FoM_{SN}} = \mathrm{FoM_S}/\sqrt{C_3}$ is introduced in this paper. We note that better $\mathrm{FoM_{SN}}$ and $\mathrm{FoM_L}$ can be achieved by aggressive sizing of the transistors. This aggressiveness can be roughly measured as W/L per μA bias current at the last stage. The proposed three-stage amplifier can easily be modified to drive a larger load capacitor by increasing C_{m1}. Table V summarizes the performance metrics of the proposed design and other recently reported works. We note that [19] uses multiple low-gain stages and is essentially a single-stage amplifier. $\mathrm{FoM_{SN}}$ is not applicable in this case. The die microphotograph of the proposed design is shown in Fig. 12.

V. CONCLUSIONS

In this paper, we identify complex-pole control as the key to increase the unity-gain frequency of a three-stage amplifier. For designs with complex poles, ω_o and the Q-factor are usually two conflicting parameters in optimizing the UGF. By eliminating the inner Miller capacitor and employing cascode Miller

TABLE V
PERFORMANCE SUMMARY OF THE PROPOSED DESIGN AND SOME RECENT REPORTED DESIGNS

	[8] 2011	[10] 2012	[11] 2012		[12] 2014	[19] 2014	Proposed CLIA design			
Load C_L	150pF	500pF	1nF	15nF	500pF	15nF	**330pF**	**560pF**	**680pF**	**15nF** *
DC Gain	110dB	>100dB	>100dB		>100dB	84dB	**>100dB**			**>100dB** *
UGF (MHz)	4.4	2	1.37	0.95	1.34	0.013	**4.21**	**3.49**	**3.37**	**0.84***
Phase Margin	57°	52°	83.2°	52.3°	52.7°	90.2°	**58°**	**53°**	**45°**	**60°** *
I_{DD} (μA)	20	17	72	72	7	3	**10.5**	**10.5**	**10.5**	**10.5***
V_{DD}	1.5V	1.2V	2V		0.9V	1.2V	**1.2V**			**1.2V***
Power	30μW	20.4μW	144μW		6.3μW	3.6μW	**12.7μW**			**12.7μW***
Total On-chip Capacitor C_t	1.6pF	1.15pF	2.6pF		0.87pF	0pF	**0.587pF**			**1.377pF** *
Average SR (V/μs)	1.8	0.65	0.59	0.22	0.62	0.00037	**1.35**	**0.86**	**0.67**	**0.030***
Average 1% T_S (μs)	1.9	1.23	1.28	4.49	0.62	14444	**0.7**	**0.9**	**1.2**	**19***
Chip Area (mm^2)	0.02	0.0088	0.016		0.007	0.0013	**0.0032**			**0.0054#1**
Technology	0.35μm	65nm	0.35μm		0.18μm	0.18μm	**0.13μm**			
FoM_S	22000	49020	9514	98958	106349	54166	**109222**	**153648**	**180157**	**969230***
FoM_L	9000	15931	4097	22917	49206#2	1514	**34894**	**37642**	**35550**	**35142***
FoM_{SN}	1796	2192	301	808	4756	N.A.	**6012**	**6493**	**6909**	**7931***

*: simulated value; #1: estimated value; #2: with a slew helper.

compensation in the outer compensation loop, we are able to increase ω_o significantly. By using an LIA block, we are able to achieve an optimized tradeoff between ω_o and the Q-factor. The robustness of this design is verified by both corner simulation results and Monte-Carlo simulation results. The advantages of the proposed design over previous designs are discussed in details, verified by simulation results and further confirmed with measurement results.

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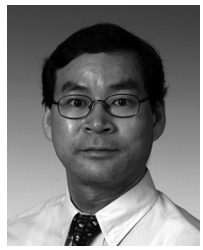

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