Control Electronics For Semiconductor Spin Qubits

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Future universal quantum computers solving problems of practical relevance are expected to require at least 10^6 qubits, which is a massive scale-up from the present numbers of less than 50 qubits operated together. Out of the different types of qubits, solid state qubits are considered to be viable candidates for this scale-up, but interfacing to and controlling such a large number of qubits is a complex challenge that has not been solved yet. One possibility to address this challenge is to use qubit control circuits located close to the qubits at cryogenic temperatures. In this work we evaluate the feasibility of this idea, taking as a reference the physical requirements of a two-electron spin qubit and the specifications of a standard 65 nm complementary metal-oxide-semiconductor (CMOS) process. Using principles and flows from electrical systems engineering we provide realistic estimates of the footprint and of the power consumption of a complete control-circuit architecture. Our results show that with further research it is possible to provide scalable electrical control in the vicinity of the qubit, with our concept.

I. INTRODUCTION

Quantum computing promises exponential speedup and memory enhancement for certain computational problems. However, applications such as Shor's algorithm will possibly require many millions of qubits for problem sizes where an advantage over conventional computers can be expected [1]. This large number mainly results from the need of making quantum systems robust against errors due to decoherence, i.e. against the loss of the information stored in the qubits caused by the interaction with the environment. The (theoretically) most established approach to counteract these errors relies on the redundant encoding of the fragile quantum information to enable error correction, resulting in an overhead of 10^2 to 10^5 in the number of physical qubits. Building on fabrication techniques that enable chips with billions of transistors, solid-state qubit implementations are promising candidates to support scaling to such large numbers. However, connecting and controlling such a large number of qubits represents a formidable engineering challenge.

Current experiments on the most scalable solid state qubits and processor demonstrators [2, 3] are operated at temperatures of 20-100 mK, and manipulated using room temperature signal generators, whose output is routed to the qubits via coaxial cables. As argued in Ref. [4], this approach will become very cumbersome beyond a few hundred qubits at the latest, and seems completely impractical for the large number of qubits eventually required. Even with a fairly compact PCI-type form factor for a single qubit controller, the control electronics would fill thousands of racks. Furthermore, it poses a rather fundamental connectivity challenge. For example, 10^6 UT34 coaxial cables with a diameter of 0.9 mm^2 each correspond to a total cross section of 0.6 m^2. Such cabling will impose an unacceptable heat load on the cryogenic end, and cannot be connected directly to the highly-integrated qubit chips. Current semiconductor technology is limited to die sizes of about 30 mm and connecting a number of cables with a total cross section much larger the wafer size would lead to a very complex wiring problem in the fan-out. Frequency multiplexing can help, but will likely be limited to a relatively small number of signals per cable, due to frequency crowding and throughput considerations.

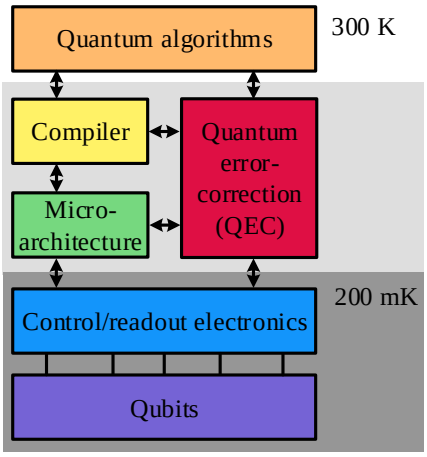

FIG. 1. General architecture of a quantum computer, going from a high-level description of a quantum algorithm, to the actual physical operation of the qubits in a layered architecture [5].

A proposed control solution is to rely on manipulating

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many qubits with the same signal [6, 7], possibly after selecting desired pulses and using modulators to tune the amplitude or phase of a pulse [8], or to switch the qubit resonance frequency. However, this approach requires that the qubits are very similar to each other (at least with respect to the drive frequency), which has not been demonstrated so far for solid-state qubits. Furthermore, it does not address the need of gate-defined spin-qubits in semiconductors, where several DC voltages at the corresponding gates have to be tuned, which is difficult to achieve with one bias line.

All the above challenges could be addressed with highly integrated control systems providing all required functionality in the immediate vicinity of the qubits, either on the same chip or with some form of chip-to-chip interconnection technology. The key advantage of this approach is that microfabricated interconnects could be used between the qubit and the control system. These to be researched interconnects would have a smaller diameter than pads and circumvent the external connectivity issue. Current state of the art can produce chip-to-chip interconnect with a pitch of $6\,\mu$min high volume production [9], but a pitch of $3\,\mu$m would be necessary. The general idea is consistent with the bigger vision of a layered architecture for quantum computer sketched in Fig. 1 [5]. In this scheme, quantum algorithms are described by a high-level programming language that is agnostic to the faulty quantum hardware and assumes both idealized qubits and operations. These algorithms are converted into their fault-tolerant version based on a specific quantum error-correction-code in a lower level of the quantum computer, and converted into a series of instructions that include both the execution of the algorithm, and the detection and corrections of errors. The instructions are translated into a series of control waveforms to be applied to the qubit by the control electronics, which should be located as close as possible to the actual qubits. The focus of this work is on this lower electrical layer and assumes well established qubits. Therefor a detailed study of the coherence of qubits is out of scope here.

Placing the qubit-control electronics at low temperature poses stringent constraints in terms of area and power consumption. Ideally, each qubit should be associated with a control unit whose footprint corresponds to the average interqubit spacing. Furthermore, the limited cooling power available at low temperature is a major challenge for this approach. Determining the requirements for such a dedicated controller is therefore a necessity for weighing the advantages and disadvantages of different options for controlling large numbers of qubits.

Works on cryoelectronic circuits relevant for qubit control are largely focused on specific functionalities such as pulse generators [10, 11], readout amplifiers [12–14], digital-to-analog converters (DACs) [15] and connectors [16]. In addition to these custom-designed integrated circuits, complete field-programmable gate arrays (FPGAs) were shown to remain largely operational at 4 K, and used for flexible implementations of key functionalities [17, 18] and some work on a more system level approach was done as well [19]. These approaches show that modern complementary metal-oxides-semiconductor (CMOS) technology can operate at low temperature, even if the resulting power consumption is currently too large for controlling a very large number of qubits below 1 K. Recent studies have made first steps to determine how the characteristics of individual electronics components change at low temperature [14, 20], which will be crucial for the design of optimized circuits.

Here, we present a well founded estimate of the area and power consumption of the control electronics for a single qubit. This estimate is based on the complete modeling of the control system, down to the level of elementary logic blocks (gates, flip-flops, etc.). For concreteness, we designed the control system having in mind the requirements of two-electron spin-qubits [21] (see Fig. 2), but much of the insight can also be transferred to other types of solid state qubits. For example adding an oscillator and a mixer could enable microwave signal generation as described similarly in [17], with additional microwave references needed. Our control system is able to translate digital commands from higher-level control-instances into analog control-waveforms applied to the qubit, and to supply stable DC-gate voltages as needed by semiconductor qubits. We estimate that, when implemented in current 65 nm technology, the circuit will have a footprint of the order of $180 \times 180\,\mu\text{m}^2$, and a power consumption of $190\,\mu$W per qubit. The latter comes mainly from the digital part of the control system, which could be possibly reduced up to four orders of magnitude by using a technology that is optimized for low temperature operation. In addition new technology nodes could improve the area to $20 \times 20\,\mu\text{m}^2$ and the power consumption to 700 nW . These results indicate that highly integrated control systems can be viable for at least 10^4 qubits, and identify the advances required to realize them for systems with various qubit numbers.

The remainder of this paper is organized as follows. In Sec. II we briefly summarize the operation of a two-electron-spin qubits and the requirements it imposes on the associated electronic control system. In Sec. III we present our design for the architecture of the control system. The estimated area and power consumption of this system are presented in Sec. IV, and further discussed in Sec. V. A summary and conclusion is given in Sec. VI.

II. SYSTEM REQUIREMENTS AND TARGET SPECIFICATIONS

A two-electron spin-qubit is realized by confining two electrons into a double gate-defined quantum dot (see e.g. Fig. 2). The latter is formed by exploiting the emergence of a two-dimensional electron gas (2DEG) at the interface between two semiconductors (e.g. $\text{GaAs}/\text{Al}_x\text{Ga}_{1-x}\text{As}$) or between a semiconductor and a dielectric (e.g. SiO_2), and by using metallic top-gates to deplete the 2DEG,

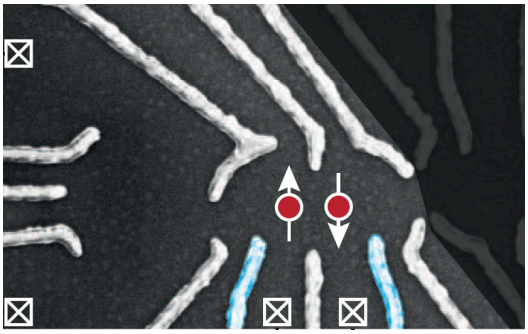

FIG. 2. Typical device layout of a two-electron qubit [21] in GaAs. The gray features correspond to the DC-gate electrodes used to form the two-electron-spin qubit in this work and the neighboring sensing dot (on the left). The blue features are the RF-gate electrodes used for fast qubit manipulation. The crossed boxes represent ohmic contacts to the leads.

creating gate-defined puddles of electrons (the quantum dots). The number of electrons in each dot can be controlled down to the single-electron regime via gate voltages. When occupied by two electrons, the double-dot can be operated as a singlet-triplet qubit, using the singlet $|\mathrm{S}\rangle = (|\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle)/\sqrt{2}$ and triplet $|\mathrm{T}_0\rangle = (|\uparrow\downarrow\rangle + |\downarrow\uparrow\rangle)/\sqrt{2}$ as states of the computational basis [22, 23], where the arrows $\uparrow$, $\downarrow$ describe the spin-state of the electron in each of the dots. The state of the qubit can be read out using a capacitively-coupled sensing dot, and exploiting Pauli blockade for spin-to-charge conversion [21]. Qubit operations can be performed acting on the exchange coupling J between the two electrons [23] by means of electric pulses applied to two dedicated gate-electrodes [24]. An advantage of this control mode is that it requires only baseband pulses (i.e. frequencies up to a few 100 MHz), eliminating the typical requirement of microwave control pulses of many other types of qubits.

A. Target system specifications

Common designs of two-electron qubits use up to six DC-gate electrodes for the qubit, and three for the sensing dot used for read-out (see Fig. 2). We assume that one of these (e.g. a plunger gate for the sensing dot) can be eliminated [25], leading to a total of eight different DC signals that have to be managed by the control system ($N_{bias} = 8$, see Tab. I). These DC signals are typically in the volt range ($V_{range,bias}$=1 V), while the resolution required to tune the qubit in the right operation regime is at the moment around 12 bits. The stability of these signals, defined as root mean squared (RMS) voltage fluctuation, has to be below the level of quasi-static charge noise. We chose it to be $3\,\mu$V [26].

The qubit is operated by applying control RF pulses to two dedicated electrodes. Each control pulse is formed by series of 16 different rectangular voltage pulses (samples). In current experiments, control pulses are produced by arbitrary waveform generators (AWGs), and have typically amplitudes of a few mV ($V_{range,RF} = 4\,\mathrm{mV}$), 10 bit resolution and 1 GHz sample rate, though a sufficient performance at 300 MHz can be expected. The qubits frequency dependent sensitivity to broadband (white) noise is given through its filter function [27], which shows a attenuating behaviour at higher frequencies [28]. The noise spectral density must be at most $0.4\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ which translates to an RMS stability value of $\delta V_{RF} = 8\,\mu$V (assuming a noise bandwidth of 400 MHz with regard to as in [28]). The effects of jitter have not been described in detail yet [29] and are the subject of current research.

Apart from generating the voltages to be applied to the DC and the RF gates, the control electronics must also be able to locally store the voltage configuration needed to define the qubit, as well as all the different control pulses used for qubit operation. With surface-code error correction operation in mind, we consider up to $N_{pulses} = 16$ different control operations, which includes initialization, readout, two-qubit gates with four neighboring qubits, and a few single-qubit gates [30]. Some of the longer operations may have to be composed of several sequences. The requirements for the control electronics discussed above, and summarized in table I, refer to parameters typical for GaAs-based devices, for which the control requirements have been studied in more detail than for Si-based devices. In particular, our assumptions regarding noise, time resolution and control amplitudes are largely based on the detailed simulations of qubit-control pulses of Ref. [28], which uses a realistic noise model based on the experiments of Refs. [31–33] on GaAs-based devices. With these parameters fidelities of 99.8 % were predicted, and experimental results have come close to these values [34]. These numbers exceed the error correction threshold, and come close to the target of about 99.9 % at which the overhead for quantum error correction becomes tolerable. As Si-based devices are less affected by dephasing caused by nuclear spins, they will probably allow a lower operating speed than what is reported in Tab. I, otherwise, the requirements will be very similar.

A complete electrical system for qubits will also have to include a solution for reading out qubits. As its performance requirements depend strongly on the readout approach at the qubit level (e.g. charge sensor [35] vs. gate-dispersive readout [36]) and on the analogue characteristics of the first amplifier stage, different kind of considerations are required than for qubit manipulation. Hence, the focus of the present work is entirely on the latter.

III. SYSTEM DESIGN

The general architecture of the qubit-control electronics is sketched in Fig. 3. It consist of four units dedicated to specific tasks. The managing component is a digital unit, which controls the other subunits and interacts with

TABLE I. Summary of current set of system specifications

Specification	Symbol	Value
Number of bias signals	N_{bias}	8
Bias range	$V_{range,bias}$	1 V
Bias stability	δV_{bias}	3 μV
Bias signal resolution	n_{bias}	12 bit
Number of RF signals	N_{RF}	2
RF amplitude	$V_{range,RF}$	4 mV
RF signal resolution	n_{RF}	10 bit
RF stability	δV_{RF}	8 μV
RF sample rate	$f_{sample,RF}$	300 MHz
RF pulse length	l_{pulse}	16 samples
Number of RF pulses stored	N_{pulses}	16

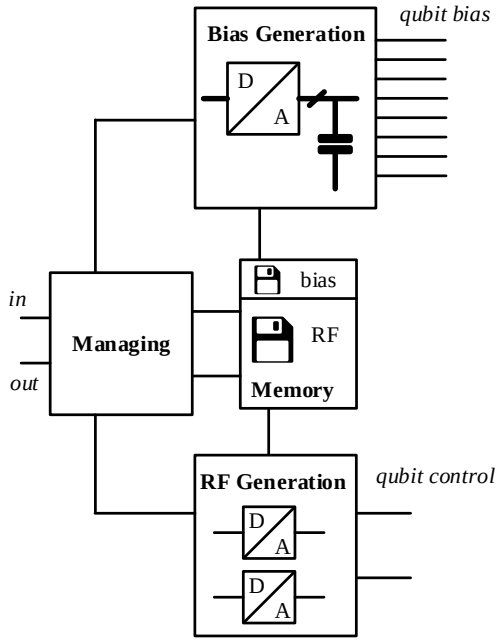

FIG. 3. Block diagram of the control electronics. The managing unit steers the whole system and interacts with the higher levels of the quantum computer architecture. The bias memory stores values of the bias that needs to be applied to the DC electrodes for defining the singlet-triplet qubit. These values are converted into voltages by the bias generation unit, which supplies the DC electrodes of the double dot. The RF memory stores the control pulses needed to operate the qubits, which are converted into analogue signals applied to the control gates by the RF generation unit.

the higher levels of the quantum computer stack [5]. The memory stores the voltage values to be applied to the DC-bias electrodes (bias memory) and the RF-pulse sequences needed for qubit operations (RF memory). The bias generation unit converts the digital values stored in the bias memory into voltages applied to the DC gate-electrodes, while the RF generation unit generates the analog control pulses from the sequences stored in the RF memory.

A. Memory

The bias memory contains nine registers, one for each DC electrode ($N_{bias} = 8$), plus an additional one that can be used to apply voltage ramps during the initial qubit-tune-up procedure [37]. The RF memory requires considerably more space to store $N_{pulses} \cdot l_{pulse} = 256$ words.

For the memory, we have chosen a design based on flip-flops (FF) as they are more robust with respect to variability in the component parameters than e.g. static random access memory (SRAM) cells, which would be much more economical in the number of transistors per bit. This conservative approach will facilitate the fast implementation of a functioning demonstrator circuit with currently commercially available technology. The resulting circuit design is shown in Fig. 4. The use of flip-flops in a shift register configuration allows for a serial writing process with low wiring complexity. A serial write operation shifts a data-word into one register from the input *data_in* in several clock cycles. The register is selected through a demultiplexer (DEMUX) with the corresponding address at *write_select*. The slow serial writing speed is not critical, because writing occurs only when a new set of pulse shapes/bias voltages is loaded into the memory outside of qubit operations.

The read process on the other hand is more time critical, and it is implemented as a parallel readout in both memory parts, which allows reading all bits of a register in a single clock cycle. For this, the output of each flip-flop is connected to a multiplexer (MUX). The select signal *read_select* determines the register whose values should be transmitted to the output *data_out*. The main difference between the bias and the RF memory is that the second includes also a second MUX connected to all flip-flops, with an associated *read_select* signal, which enables the parallel readout of two registers.

B. Bias Generation

The bias generation unit is shown in Fig. 5a. It is composed of a DAC followed by a sample-and-hold (s&h) circuit, which allows using a single DAC to supply several bias electrodes.

Determining the ultimate best DAC architecture for the control electronics of a qubit is a complex task, which goes beyond the scope of this work. There are several different ways of constructing a DAC [38] and each is characterized by a number of properties such as range, stability, linearity, monotonicity, and noise, as well as by a characteristic area and power consumption. Here we consider only these last three most relevant aspects, and compare the three designs presented in Fig. 6 (see

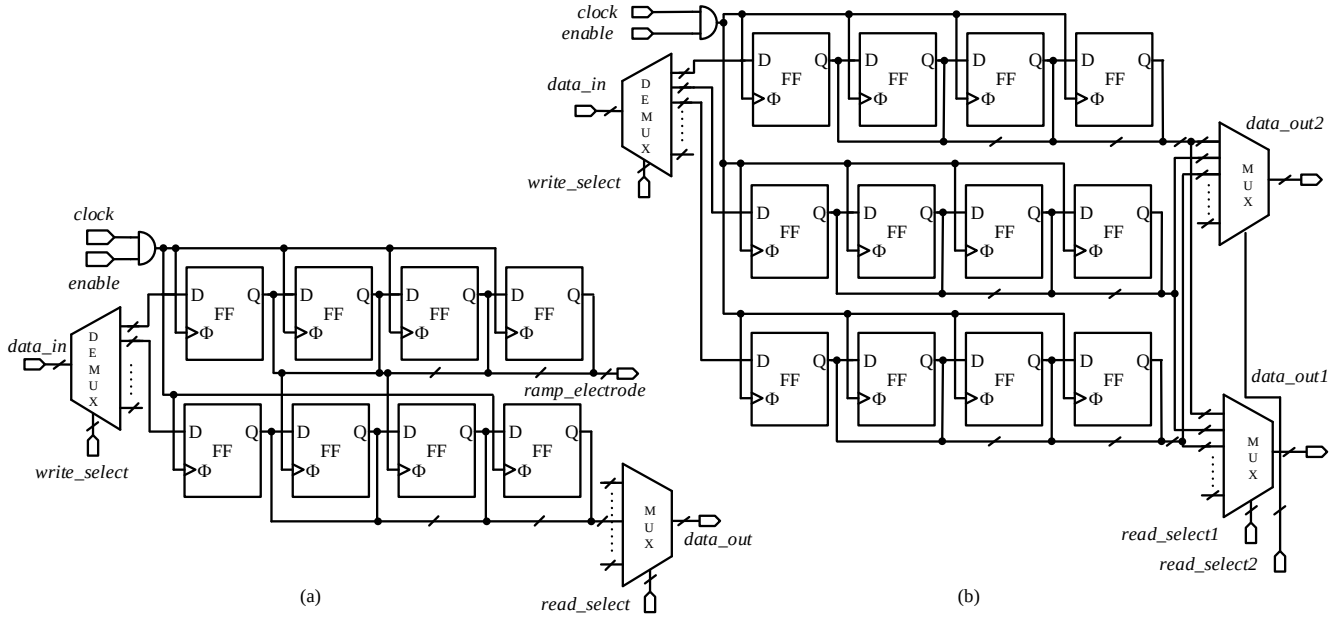

FIG. 4. Structure of a) two registers of bias memory, and b) three register of RF memory for the case of 4 bit resolution. In both cases, the registers have a serial write mechanism and a parallel readout. Read and write addressing is implemented through MUXs and DEMUXs. The output of the MUX *data_out* connects the memory to the DACs inside the bias- and RF-generation part, while the select signals come from the managing unit. Symbols are defined in Fig. 12c.

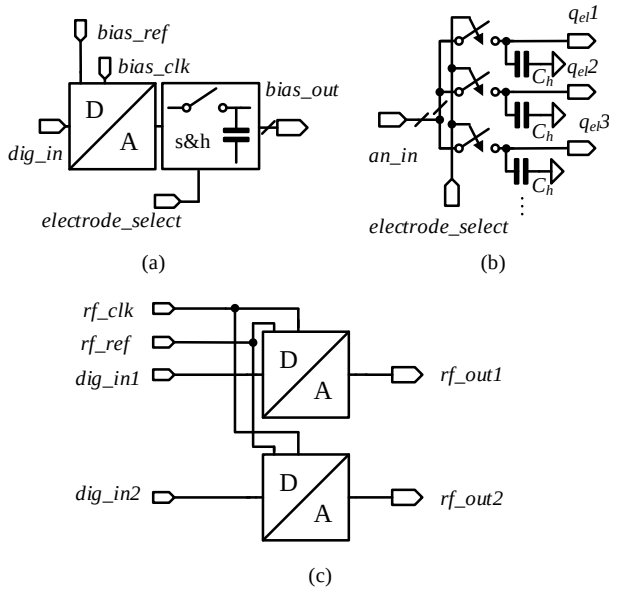

FIG. 5. (a) Structure of the bias generation unit. (b) Structure of the sample-and-hold for the bias generation unit. (c) Structure of the RF generation unit. Symbols are defined in Fig. 12c.

discussion in Sec. IV). These architectures are (i) the Kelvin Divider DAC (Fig. 6a), which uses a string of resistors as voltage dividers to tap different voltage levels from a voltage reference v_{ref}, (ii) the R-2R Ladder DAC (Fig. 6b), which adds up fractions of the reference voltage at the output, and (iii) the Cap DAC (Fig. 6c), which works as a capacitive voltage divider between a reference voltage v_{ref} and ground. The number of switches and resistors/capacitors needed for each DAC depends on the resolution n as given in Tab. II. We exclude from our analysis oversampling DACs, as they require significant additional circuitry and high clock frequency, as well as current-steering DACs, which are not very well suited for standard CMOS operation at cryogenic temperatures [39]. Leveraging the very high qubit impedance – which implies that next to no current needs to be delivered by the DACs – we do not include operational amplifier as output buffer of the DACs. Errors caused by the output load cause no concern, since they are constant and calculable, and can be compensated by pre-distortion. The pre-distortion can be done in the context of the anyway necessary tuning of the double dots which somewhat mitigates the effects of e.g. mismatch, as well.

The size of the unit elements of the DACs, R_u and C_u are constrained by the requirement that the variations of the output voltage due to Johnson noise are within the stability criteria summarized in Tab. I. For instance, the Johnson noise of the Cap-DAC, is approximately given by $\overline{v_n^2} = k_B T/C_{out}$, with $C_{out} \approx 2^{n/2} C_u$. For a 12 bit DC-bias DAC with $\delta V_n = 3\,\mu$V and T=200 mK, one obtains a lower bound of $C_u = 4.8$ fF. In the following, we assume for the Cap-DAC Metal-Insulator-Metal (MIM) capacitors with unit capacitance $C_u = 10$ fF, which is the minimal value allowed by the 65 nm CMO S technology considered for our estimates (see discussion in Sec. IV).

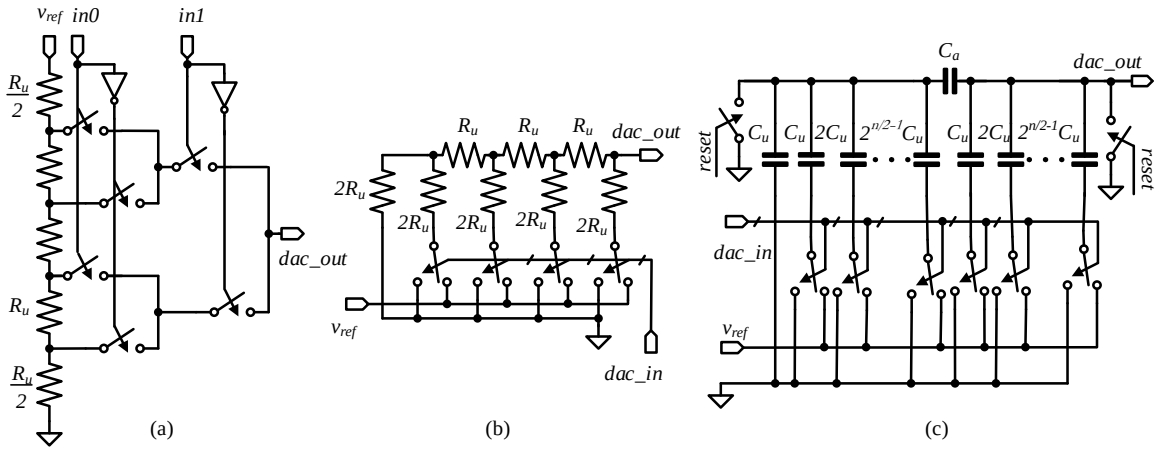

FIG. 6. Basic DAC types with reference voltages v_{ref}.The *dac_out* voltage range equals V_{range} which, as seen in (a), can differ slightly from v_{ref}. R_u denotes unit resistor, C_u unit capacitor. (a) 2 bit Kelvin Divider DAC consisting of one voltage divider string of resistors. b) 2 bit R-2R Ladder DAC adds up fractions of the reference of the voltage or current at the output. (c) n-bit capacitor based DAC (Cap DAC). Here $C_a = C_u \cdot 2^{n/2}/(2^{n/2}-1)$.

The Johnson-Nyquist noise of the resistor based DACs is approximately given by $\overline{v_n^2} = 4k_BTR_{out}B$, where B is the effective bandwidth. For the Ladder DAC, it is $R_{out} = R_u$, assuming a bandwidth of 10 MHz and T=200 mK one obtains an upper bound of $R_u \leq 81\,\mathrm{k}\Omega$. The output resistance of the Kelvin DAC is code-dependent and in the worst case scales $R_{out} = 2^{n-2}R_u$ [40]. giving $R_u \leq 160\,\Omega$ to remain within the noise requirements for a 12 bit DAC and $R_u \leq 5\,\Omega$ for 16 bit. For the resistors forming the Kelvin DAC, we assume poly-silicon resistors with resistance $R_u = 15\,\Omega$ for the starting comparison, which is again the minimal value set by the considered technology, keeping in mind that for $n = 15, 16$ this will violate the noise requirements. For the resistors of the Ladder DAC, we take instead the value $R_u = 150\,\Omega$, as lower values of R_u will lead to an excessive power dissipation (see discussion in Sec. IV). In this context the bandwidth is associated with the overall low pass behaviour of the circuit. For this reason the bandwidth value during the design is engineered to let the wanted signal (1.1 MHz) pass undistorted with margin (leading to B=10 MHz), while unwanted signals and noise at higher frequencies are suppressed. Since the intrinsic DAC bandwidth is expected to be considerably higher than 10 MHz, the resulting bandwidth could, for example, be lowered with additional capacitances connected in a low pass configuration.

The second element of the bias generation unit is a sample-and-hold circuit consisting of hold capacitors and CMOS switches (see Fig. 5b). Each hold capacitor, C_h, stores the voltage for a specific electrode, while the switches connect the DAC output to one capacitor at a time in order to change and refresh its value. The refresh happens in a cyclic manner to compensate for leakage-induced discharges to ground. Leakage through the switch gate is the only other probable interference with the stored voltage [41]. However, this could be diminished through the use of thick oxide transistors at this place [42, 43]. The s&h circuit additionally acts as a low-pass filter that decouples the qubit from high frequency noise and glitches e.g. originating from switching in the DAC. Also in this case, the minimal value of C_h is set by the requirement that the Johnson noise of the s&h, which is approximately given by $\overline{v^2} = k_BT/C_{out}$ with $C_{out} = C_h$, does not exceed the specified voltage stability δV_{bias}. Assuming $T = 200\,\mathrm{mK}$ for the electronics and $\delta V_{bias} = 3\,\mu\mathrm{V}$, this gives $C_h = 307\,\mathrm{fF}$. The value of C_h contributes to the calculation of the rate $f_{refresh}$ at which the voltage on the capacitors have to be refreshed to compensate for leakages. This sets the frequency at which all components associated with the bias generation work. For typical MIM capacitors with a dielectric thickness of 10-30 nm [44] and a maximal applied voltage of 1 V, the leakage current through the dielectric can be neglected with respect the leakage through the open switches with resistance R_{off} (see Tab. III). The refresh rate to meet the stability requirement is then given by

$$f_{refresh} = \frac{V_{range,bias}/R_{off}}{\delta V_{bias} \cdot C_{out}}. \tag{1}$$

where the numerator is the leakage current and the denominator the maximal charge that can be lost without compromising the stability of the voltage at the gate electrodes. For given values, one obtains $f_{refresh} = 1.1\,\mathrm{MHz}$. This frequency determines also the operation frequency of the bias DAC.

C. RF Generation

The RF generation unit is composed by two DACs, one for each RF electrode of the qubit as depicted in Fig 5 (c).

TABLE II. DAC elements for resolution n

	Kelvin	Ladder	Cap
Unit element	R_u	R_u	C_u (C_a)
Unit value	15 Ω	150 Ω	10 fF
No. unit elements	2^n	$3n$	$2 \cdot 2^{n/2} - 1$
No. switches	$2^{n+1} - 2$	$2n$	$2n$

This simple structure allows for fast waveform playback (300 MS/s, cf. table I). Similarly to what discussed in the previous section, the size of the unit components of the RF-DACs are determined by requiring that the voltage noise at DAC output is below the stability threshold. Using $n = 10$ bit, $B = 600$ MHz and $\delta V_{RF} = 8\,\mu$V, this leads to the bounds $C_u \geq 1.3$ fF and $R_u \leq 38\,\Omega$ (Kelvin) and $R_u \leq 10\,\text{k}\Omega$ (Ladder). In the following, we will take for the unit elements of the RF DAC the same values chosen for the bias DAC and summarized in Tab. III for a first comparison, even if for $n \geq 10$ the Kelvin DAC would produce too much noise. The bandwidth is set in accordance with the filtering behaviour of the qubit.

D. Managing Component

The managing component is a purely digital unit which steers the other units of the control electronics, interacting with the higher levels of the quantum computer and providing an interface to the memory. Its structure is described in detail in Appendix A.

IV. AREA AND POWER CONSUMPTION

To make concrete estimate of the area and power consumption of the control system described in the previous section, we take as reference a standard commercial 65 nm CMOS technology, which is well established and easily available for research purposes. The relevant parameters used are summarized in Tab. III. Here, the resistive and capacitive densities presented in the first block are effective densities, which include device terminals. The second block of parameters characterizes a typical transistor used as switches or in digital gates. The third block of parameters contains the minimal resistance of poly-silicon resistors, the minimal capacitance of integrated MIM capacitors, and the digital supply voltage $V_{dd} = 1$ V set by process restrictions. All parameters of these first three blocks, are characteristics of the considered CMOS technology, and derived from the models in the physical design kit (pdk). [45] The fourth block contains our choices for the sizes of the resistors and capacitors inside the bias and RF generation parts. The last block of parameters describes the dynamic behaviour of the circuits in our model, including the switching rate of logic switches and additional clock frequencies.

TABLE III. Parameters for 65 nm CMOS technology used in the estimates of area and power consumption.

Parameter	Symbol	Value
Resistive density	ρ_R	21.4 Ω/μm^2
Capacitive density	ρ_C	1.75 fF/μm^2
Mean transistor area	A_{MOS}	0.375 μm^2
Mean transistor cap.	C_{MOS}	150 aF
Mean transistor off res.	R_{off}	1 TΩ
Mean transistor on res.	R_{on}	5 kΩ
Min. Resistance	R_{min}	15 Ω
Min. Capacitance	C_{min}	10 fF
Digital supply voltage	V_{dd}	1 V
Hold cap. s&h bias gen.	$C_{h,bias}$	307 fF
Unit cap. bias DAC	C_u	10 fF
Unit res. RF DAC	R_u	150 Ω
Bias memory activity	$\sigma_{biasmem}$	0.306
RF memory activity	σ_{RFmem}	0.026
Managing comp. activity	σ_{con}	0.5
Clock freq. bias	$f_{clk,bias}$	2.22 MHz
Clock freq. RF	$f_{clk,bias}$	600 MHz

Knowing the number of basic components, their sizes, and the technology data, we can estimate the area demand of the control circuit [46]. With the added knowledge of the dynamic behaviour of the different circuit elements and of the system specifications, we can estimate the power consumption. The power consumption of the analogue parts of the DACs is approximately given by $P_R = V_{range}^2/R_{in}$ ($v_{ref} \approx V_{range}$) and $P_C = 0.5 \cdot f_{refresh} C_{in} V_{range}^2$, where V_{range} is the typical voltage supplied to the input and R_{in} and C_{in} are the input resistance and capacitance of the DACs respectively. The supplied voltages are equal to the signal amplitudes $V_{range,bias}$ and $V_{range,RF}$ as given in Tab. I. The power consumption of the digital parts and of the switches in the DACs is modeled as

$$P_{dig} = P_{switch} = \sigma \cdot f_{clk} \cdot V_{dd}^2 \cdot C_{gate}, \tag{2}$$

where C_{gate} is the total capacitance of the considered circuit or switches, f_{clock} the clock frequency, V_{dd} the applied potential, and σ is the activity of the circuit. The total capacitance is given by $C_{gate} = n_s \cdot C_{MOS}$ (Tab. III), with n_s the number of switches or logic transistors. Parasitic capacitances are not included [47]. For a simple switch $\sigma = 0.5$, which is also the maximum in common clocked, edge triggered logic. In the following we will conservatively assume $\sigma = 0.5$ for most digital circuits, except for the memory parts where σ can be derived from the circuit architecture with little effort (see Tab. III). Determining the precise activity of the other circuits would require extensive statistical simulation or testing. In Eq. 2 we neglect the short-circuit power consumption as well as the leakage power [48], since in the

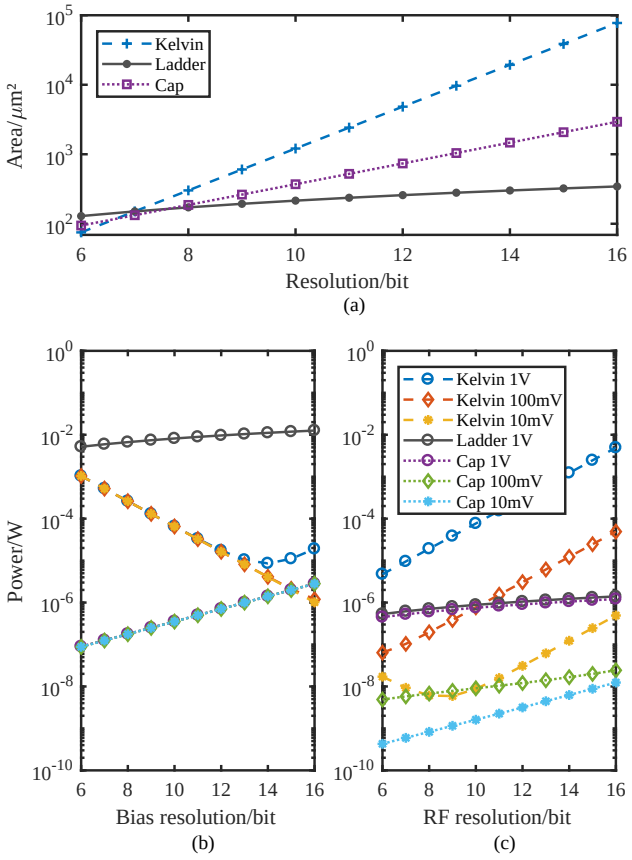

FIG. 7. Comparison of DACs with component dimensions as in Sec. III B and Sec. III C but with $R_{u,Ladder} = 150\,\Omega$ a) Area consumption of the different DAC architectures for different resolutions, independent of operating conditions b) Power consumption of the DAC architecture, under the operating condition of the bias generation unit ($V_{range} = 1\,\mathrm{V}$ and $f_{refresh} = 1.11\,\mathrm{MHz}$). c) Same as in b), but now considering the operating conditions of the RF generation unit ($V_{range} = 4\,\mathrm{mV}$ and $f_{refresh} = 300\,\mathrm{MHz}$).

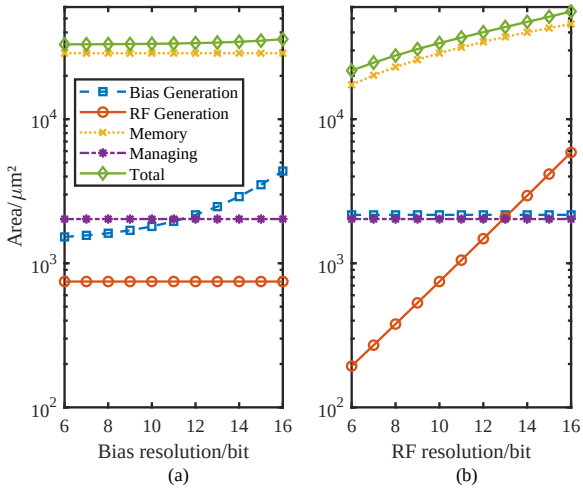

FIG. 8. Area consumption of the different components of the control electronics (labeled as in Fig. 3) for different values of the resolution of the bias signal (a) and of the RF signal (b). In panel a) the RF resolution is assumed to be 10 bits, while in panel b) the bias resolution is fixed to 12 bits.

considered technology they are small compared to the switching power P_{switch}, especially at cryogenic temperatures [41, 42, 49–52].

We first analyze the area and the power consumption of the three DAC architectures presented in Fig. 6. Current experiments employ a resolution of 12 and 10 bit for bias and RF-signals, respectively. However, since these specifications are likely to change in the future, we plot our results as a function of resolution n. The area required by the three types of DAC is represented in Fig. 7a, and clearly point at the Ladder DAC as the most area-saving architecture, even with a unit resistance significantly larger than the one of the Kelvin DAC. The power consumption of the three DACs is plotted in Fig. 7b and c, distinguishing between the typical operation conditions of the bias generation unit ($V_{range} = 1\,\mathrm{V}$ and $f_{refresh} = 1.11\,\mathrm{MHz}$) and of the RF generation unit ($V_{range} = 4\,\mathrm{mV}$ and $f_{refresh} = 300\,\mathrm{MHz}$). The power consumption is also plotted for several different supply voltages for the Cap and Kelvin DACs, as this has a major quantifiable impact on their dissipation and lower V_{dd} may become available for future technologies optimized for cryogenic operation [4]. Vice versa, the power required by the Ladder DACs has little variation with V_{dd} and is only plotted for $V_{dd} = 1\,\mathrm{V}$, which is the supply voltage in the current technology.

In Fig. 7b,c the Kelvin DAC shows at times a counter intuitive behaviour of the power consumption over the resolution. The reason is that while n is rising also R_{in} increases, leading to a lower power consumption with a fixed R_u. For higher resolution however the power consumption of the switches inside the DAC dominates the total power consumption, thus leading to an increase.

The Cap DAC turns out to be the most power saving architecture, achieving a power consumption of around $10^{-7}\,\mathrm{W}$ for a DAC in the bias generation condition and a consumption in the range of $10^{-9}\,\mathrm{W}$ for the RF generation condition. This is in part thanks to the fact that this type of DAC has only dynamic power consumption, in contrast to resistor-based designs with static power consumption. The somewhat higher area consumption of the Cap DAC is compensated for by the significantly lower power consumption in case of the bias operation condition. For the RF operation condition the potential for a significant power reduction for smaller V_{dd}, in contrast to the Ladder DAC, is the criteria for the choice of the Cap DAC. In all the following estimates, we will therefore assume the DAC of the bias generation unit and the RF generation unit to be a Cap DAC.

We now turn discussing the behavior of the whole control electronics. The total area consumption is shown in

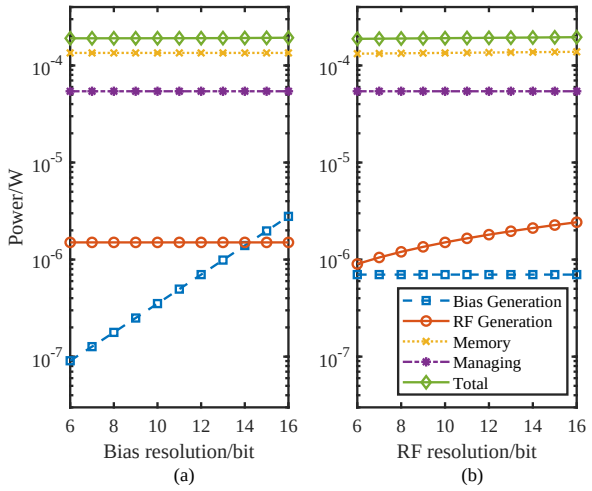

FIG. 9. Power consumption of the different components of the control electronics (labeled as in Fig. 3) for different values of the resolution of the bias signal (a) and of the RF signal (b) using $V_{dd} = 1\,\mathrm{V}$. In panel a) the RF resolution is assumed to be 10 bits, while in panel b) the bias resolution is fixed to 12 bits. Both panels refer to the power consumption during qubit operation. In contrast to Fig. 7, the bias generation power includes the DAC and the s&h, and the RF generation power includes the power of two DACs

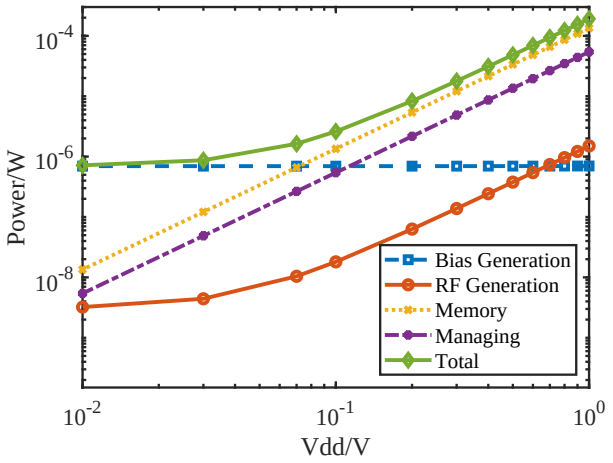

FIG. 10. Power consumption of the different components of the control electronics (labeled as in Fig. 3) for different values of the digital supply voltage V_{dd}. The bias resolution is set to 12 bit while the RF resolution is assumed to be 10 bit and the figure again refers to the power consumption during qubit operation. For $V_{dd} < 70\,\mathrm{mV}$ the bias generation unit dominates the total power consumption

Fig. 8 as a function of the resolutions of the bias and the RF signals. For the typical resolutions used in current experiments (bias resolution = 12 bits and RF resolution = 10 bits) the control electronic would occupy an area of roughly $3.3 \cdot 10^4\,\mu\mathrm{m}^2$, with the largest share taken up by the memory which is the only part with a significant dependence on the resolution.

The estimated power consumption of the whole control electronics in the so–called "qubit operation regime", when the qubit is manipulated by RF pulses to perform various operations (e.g. logical gates), is shown in Fig. 9. In this regime, the clock frequency of the digital circuit elements f_{clk} entering Eq. 2 is determined by f_{refesh} of the associated analog parts of the DACs, with $f_{clk,bias} = f_{clk,biasmem} = f_{clk,biasgen} = 2 \cdot f_{refresh,bias} = 2.22\,\mathrm{MHz}$ and $f_{clk,RF} = f_{clk,RFmem} = f_{clk,RFgen} = 2 \cdot f_{refresh,RF} = 600\,\mathrm{MHz}$. The factor 2 is included because sequential synchronous logic gates are edge triggered (e.g. by the rising edge) and thus their outputs operate at half the clock frequency. The subunits of the managing component are running on different frequencies, as detailed in App. A. The total power consumption of the circuit with the current specifications ($V_{dd} = 1\,\mathrm{V}$,$V_{range,bias} = 1\,\mathrm{V}$,$V_{range,RF} = 4\,\mathrm{mV}$, $f_{refresh,bias} = 1.11\,\mathrm{MHz}$, $f_{refresh,RF} = 300\,\mathrm{MHz}$) is around $1.9 \cdot 10^{-4}\,\mathrm{W}$, with almost no dependence on the resolution (see Fig. 9). More than 95 % of this is due to digital circuits, with the bias and the RF generation units accounting only for a few μW.

Lowering the supply voltage as shown in Fig. 10 drastically reduces the percentage of the total power consumption the digital circuits and especially the memory and managing unit have. Below 70 mV the bias generation part consumes the most power.

TABLE IV. Area and power consumption for different technology and architecture options included in the model: flip-flop memory (FF), SRAM memory (S), V_{dd} =digital supply voltage, Node=CMOS technology generation

Settings				
Node/nm	65	65	65	14
V_{dd}/V	1	1	100m	10m
Architecture	FF	S	S	S
Area/μm^2				
Bias Gen A.	$2.2 \cdot 10^3$	$2.2 \cdot 10^3$	$2.2 \cdot 10^3$	$1.1 \cdot 10^1$
RF Gen A.	$7.5 \cdot 10^2$	$7.5 \cdot 10^2$	$7.5 \cdot 10^2$	$3.8 \cdot 10^0$
Memory A.	$2.9 \cdot 10^4$	$2.6 \cdot 10^3$	$2.6 \cdot 10^3$	$2.1 \cdot 10^2$
Managing A.	$2.0 \cdot 10^3$	$1.7 \cdot 10^3$	$1.7 \cdot 10^3$	$7.0 \cdot 10^1$
Total A.	$3.3 \cdot 10^4$	$7.2 \cdot 10^3$	$7.2 \cdot 10^3$	$3.0 \cdot 10^2$
Power/W				
Bias Gen P.	$7.0 \cdot 10^{-7}$	$7.0 \cdot 10^{-7}$	$7.0 \cdot 10^{-7}$	$7.0 \cdot 10^{-7}$
RF Gen P.	$1.5 \cdot 10^{-6}$	$1.5 \cdot 10^{-6}$	$1.8 \cdot 10^{-8}$	$3.2 \cdot 10^{-9}$
Memory P.	$1.3 \cdot 10^{-4}$	$5.0 \cdot 10^{-5}$	$5.0 \cdot 10^{-7}$	$3.6 \cdot 10^{-9}$
Managing P.	$5.4 \cdot 10^{-5}$	$2.8 \cdot 10^{-5}$	$2.8 \cdot 10^{-7}$	$2.2 \cdot 10^{-9}$
Total P.	$1.9 \cdot 10^{-4}$	$8.1 \cdot 10^{-5}$	$1.5 \cdot 10^{-6}$	$7.0 \cdot 10^{-7}$

V. DISCUSSION AND OUTLOOK

The estimates of area and power consumption presented in the previous section clearly point at some of the most relevant technological challenges that the vision of a quantum computer as illustrated in Fig. 1 will have to face.

According to our analysis, the control electronics for a single qubit will occupy an area which is about four orders of magnitude larger than the current qubit footprint associated with the average interqubit spacing. The qubit distance allowing for entangling is up to a few microns for charge-coupled semiconductor qubits [53] and less than $1\,\mu$m for exchange coupled semiconductor qubits [54]. Larger spacings are possible when using cavity coupling [55–57] and for superconducting qubits. This discrepancy limits the possibility of placing the control electronics directly on top of each qubit in a scalable way with the specific design considered so far. The memory unit consumes the most area of all components, as depicted in Fig. 8, which is also not greatly changed through a decrease in resolution of bias or RF signals. However, a significant area reduction is explored in Tab. IV by comparing two different memory types, the current flip-flop (F) and SRAM (S).

SRAM is a much more area efficient, low-latency and non-volatile memory architecture, whose memory cells have a typical size of $0.5-0.7\,\mu\text{m}^2$ in a 65 nm technology [58], compared to the current $10\,\mu\text{m}^2$ of a flip-flop. However, SRAM functionality is based on sensitive analog device-properties, which are not yet well characterized at low temperatures. If SRAM proves reliable functionality at cryogenic temperatures, the area of the memory could be reduced by one order of magnitude (Tab. IV).

Moving from the current 65 nm technology to a smaller node like a 14 nm technology will reduce the area of a logic transistor by a factor of 24 and the SRAM cell by a factor of 7 [59, 60]. The capacitor and resistor densities are not directly affected by CMOS scaling, but the capacitive density could potentially be increased by a factor of more than 200 through the use of so called trench capacitors [61, 62].

In summary, exploiting the discussed and currently available technologies it should be possible to reduce the area consumption of the control electronics from $3.3\cdot10^4 \approx 180\times180\,\mu\text{m}^2$ to $3.0\cdot10^2 \approx 20\times20\,\mu\text{m}^2$ (Tab. IV). Some additional leeway for reducing the area discrepancy between qubit and electronics is offered by the not yet modeled stacking of dies, and by the current efforts of implementing long–range coupling of qubits, which would extend the footprint of the qubit. Literature suggests that a coupling range of $10\,\mu$m might be feasible [53, 63, 64]. Altogether, this indicates that with future research the area matching of qubit footprint and control electronics is in reach.

For the power consumption, our estimates indicate that with current technologies the control electronics would consume around $190\,\mu$W. This has to be compared with the cooling power of the cryostats hosting the quantum computing systems. Current cryogen-free dilution refrigerators supply up to a few mW at 200 mK, less than 1 W at 1 K, and a few W at 4 K. The cryogenic qubit control systems considered here would then be suitable for a 5 qubit demonstrator system (Tab. V).

TABLE V. Number of controllable qubits for different quantifiable scenarios: T_{el} = operating temperature of electronics, $\dot{Q}$ = cooling power, No. Qubits = $\dot{Q}$ / dissipation, architecture: flip-flop memory (FF), SRAM memory (S). The analog component sizes and derived parameters are adjusted for 1.8 K, if needed.

T_{el}	$\dot{Q}$	Architecture	Node	V_{dd}	No. Qubits
200 mK	1 mW	FF	65 nm	1 V	5
200 mK	1 mW	S	14 nm	100 mV	328
200 mK	1 mW	S	14 nm	10 mV	$1.4\cdot10^3$
1.8 K	1 W	S	65 nm	1 V	$1.3\cdot10^5$
1.8 K	10 W	S	14 nm	10 mV	$6.1\cdot10^8$

The already discussed options for the area optimization SRAM and the shrinking of the feature size present a complementary reduction in power consumption by approximately two third. In addition, a considerable reduction of power could be achieved by reducing the operating voltage of the digital elements, see Tab. IV. Reducing V_{dd} from 1 V to 100 mV, which may be possible with reasonable process modifications to shift the transistor threshold voltage, would reduce the dissipation due to digital circuitry by a factor 100. This would in turn allow the operation of more than three hundred qubits. This number is already very inconvenient to achieve with standard dilution refrigerators and a control based on room temperature electronics. Reducing V_{dd} to 10 mV, which is physically possible but requires major re-optimization of transistors for cryogenic operation [4, 65], the power consumption of the digital circuits could be reduced to the nW regime, while the total power consumption is at 700 nW. In this case, the analog bias generation unit would become the by far the major source of dissipation (see Tab. IV last column).

Another possible approach to relax the constraints on the power consumption is to thermally isolate qubits from the electronics while allowing high-density, microfabricated interconnects. Increasing the operating temperature of the control electronics would in fact considerably relax the constraints on the thermal budget and allow the operation of hundred thousand, or even billions of qubits, see Tab. V. Using a Helium liquifier plant, it should be even possible to deliver at least 100 W around 2 K (as an extreme example, each cooling plant used at LHC provides a cooling power of 2.4 kW at 1.8 K [66]).

For a possible scale up to qubit numbers in the range of millions, with reasonable cooling effort, additional strategies are needed to bring down the power consumption of the bias generation. The digital parts of the unit con-

sume negligible power at this point with $P_{bias} \approx P_C$, the power consumption of the periodically charged capacitors, leaving

$$P_{bias} = \frac{f_{refresh}}{2}(C_{in,DAC}V_{range,bias}^2 + C_{s\&h}\delta V_{bias}^2). \quad (3)$$

Using Eq. 1 and the known parameter values the second summand can be neglected giving

$$P_{bias} \approx \frac{C_{in,DAC}}{2 \cdot R_{off}\delta V_{bias}C_{s\&h}}V_{range}^3. \quad (4)$$

For R_{off} the conservative room temperature value 1 TΩ has been used in the model taking no leakage reduction at cryogenic temperatures into account. With an anyhow necessary optimization of the technology for low supply voltages in addition to that, the leakage current and the resulting effective R_{off}, at least for selected transistors, can be expected to change by two orders of magnitude [67]. The voltage range V_{range} in which the qubit has to be tuned depends not only on the requirements of the qubit but also on the uniformity of the substrate. A reduction from 1 V to 0.5 V would already lead to a power reduction of nearly one order of magnitude due to the cubic term. With an additional reduction of the resolution from 12 bit to 8 bit a reduction by a factor of 32 can be achieved. With these two changes the power consumption of the bias generation is safely in the nW range even if other possibilities for power reductions with less impact, such as fewer gate electrodes and a further increase of $C_{s\&h}$ (with an area trade-off), remain unexplored. Other strategies to further reduce area and power consumption are subjects of current research, and include the possibility of sharing units (e.g. some subunits of the managing component or the memory) between different qubits, functional optimization

VI. CONCLUSION

The work at hand represents a concrete feasibility analysis of a scalable integrated control system for spin qubits. We derived the systems specification from the requirements of a GaAs spin qubit and developed a dedicated electrical system using an exemplary 65 nm CMOS process. The most significant properties regarding the scalability, the area and power consumption, were investigated in detail for the complete system as well as all subunits. In addition the estimations of area and power consumption were extrapolated to a current state of the art 14 nm process. The results show that the power consumption presents a bigger challenge for scalability than the area, which is at $3.2 \cdot 10^2 \mu m^2$. For a possible reduction of the power consumption the effect of reducing the digital supply voltage V_{dd} from currently 1 V to 10 mV was detailed. This lowers the expected power consumption of all subunits, except for the bias generation, into the nW regime. However, our assumptions have been conservative in general, and with taking a slightly more optimistic estimation of the transistor leakage current at cryogenic temperatures also the bias generation power consumption could be reduced to the nW range, as well.

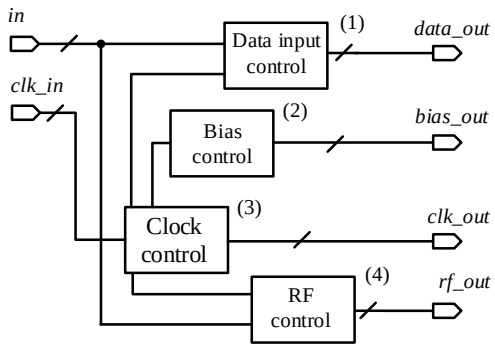

FIG. 11. Block diagram of the managing component.

With the 2019 to be available 12 nm node of the fully-depleted silicon-on-insulator (FD-SOI) CMOS technology expected to run on $V_{dd} = 200$ mV [68], a tool for a first scale up is in reach. With this technology, and the currently available 1 mW of cooling power at 200 mK, more than 300 qubits are anticipated to be controllable through the system this work proposes. This shows the near future advantage of dedicated integrated electronics since it would be quite cumbersome to control that amount of qubits with room temperature electronics. An increase in cooling power to 1 W, for example through thermal isolation of qubit and electronics, would already expectably enable the control of more than 10^5 qubits. The same would be true if the qubits could be moved to higher temperatures [7, 69], as the electrical requirements would be similar. Additional more long term improvements, such as a dedicated cryogenic CMOS process, would even lift these qubit numbers into the range of at least 10^8. This highlights the achievable and concrete steps to reach full scalability with this concept.

Appendix A: Managing Component

The managing component consists of different subunits, each dedicated to a specific task, as depicted in Fig. 11.

The data input control unit manages the reception of data and directs it to the correct memory part (Fig. 12). Data is received in data words of the form shown in Fig. 12b, with a first header bit of '1' and the second bit defining the data type, i.e. bias or RF voltage information. The next part of the data word contains an 8 bit long address to account for $256 = 2^8$ accessible registers in the RF memory. The data to be stored in the memory is located in last part of the data word, whose length is set by the required voltage resolution in the system.

Data words arrive serially at the *serial_in* input, and get written into flip-flops connected as a shift register.

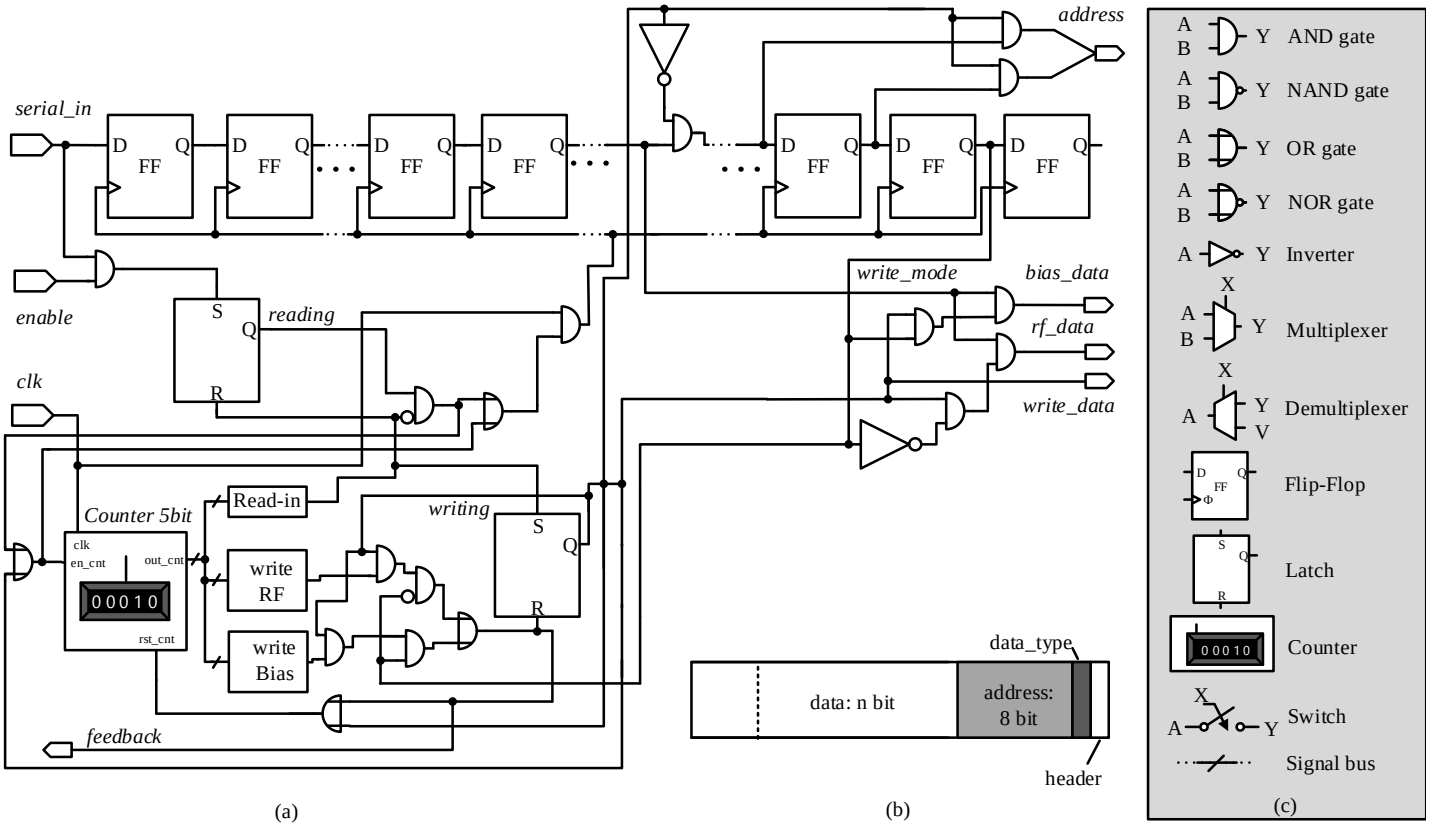

FIG. 12. a) Structure of the *data input control* unit, which receives voltage information to be stored in the memory, and distributes it with the corresponding address to the appropriate memory part b) Structure of the data word. c) Legend of the symbols used the block diagrams presented in the paper.

When the transmission begins with the arrival of the header bit, a 5 bit counter is started to time the reception of the data [70]. This happens through counting cycles of the clock signal *clock* which drives the data reception. The right number of passed clock cycles is determined by combinatorial logic, in combination with the counter which ends the data reception.

At the end of the reception, the data address is available at the *address* bus connected to the respective *write_select* inputs of the memory (see Fig. 4). The write process to the memory is stared with a logical '1' at *write_data* connected to the *enable* input at the memory. The data itself is transported via the *bias_data* and *rf_data* outputs to the *data_in* inputs of the memory. The timing of the writing process is determined again by the counter and some combinatorial logic. The end of the transmission and following writing process is signaled by an acknowledgment signal at the $feedback$ output. The data-input-control unit is only active when bias voltages or sequences are changed, and not during the "qubit operation regime" considered in Sec. IV. For this reason, its power consumption is not included in the results of Fig. 9 and Tab. IV,V. For a RF resolution of 10 bit and a bias resolution of 12 bit, the power consumption of the data-input-control unit is $1.8 \cdot 10^{-4}$ W, with negligible dependence on the maximum system resolution.

The clock control unit receives stable digital reference–signals of different frequencies, and routes them to the other subunits. Its structure is shown in Fig. 13a. The use of in total two inverters (buffers) in each signal path enhances edge steepness, thus improving signal quality. The global clock signals, used also for general timing, are produced in a different stage of the quantum-computer architecture at higher temperatures. For minimization of power consumption, the digital control-units run at the minimal frequency dictated by the corresponding analog part. Following this principle, we link the clock frequency of the bias control unit to the clock of the bias generation unit, with $f_{clk,bias} = 2.22\,\mathrm{MHz}$ and the clock frequency of the RF control unit to the frequency of the RF generation part, with $f_{clk,RF} = 600\,\mathrm{MHz}$. The frequency of the data–input–control unit can in principle be chosen arbitrarily but, to minimize the number of clock frequencies, we set it equal to $f_{clk,RF}$. Taking $f_{clk,bias}$ instead of $f_{clk,RF}$ is also a possible choice, but it slows down the data read-in by two orders of magnitude. The reduced power consumption through the lower frequency is no major advantage as long as possible temperature increase is lowered again before qubit operation.

The bias control unit has the structure shown Fig. 13b

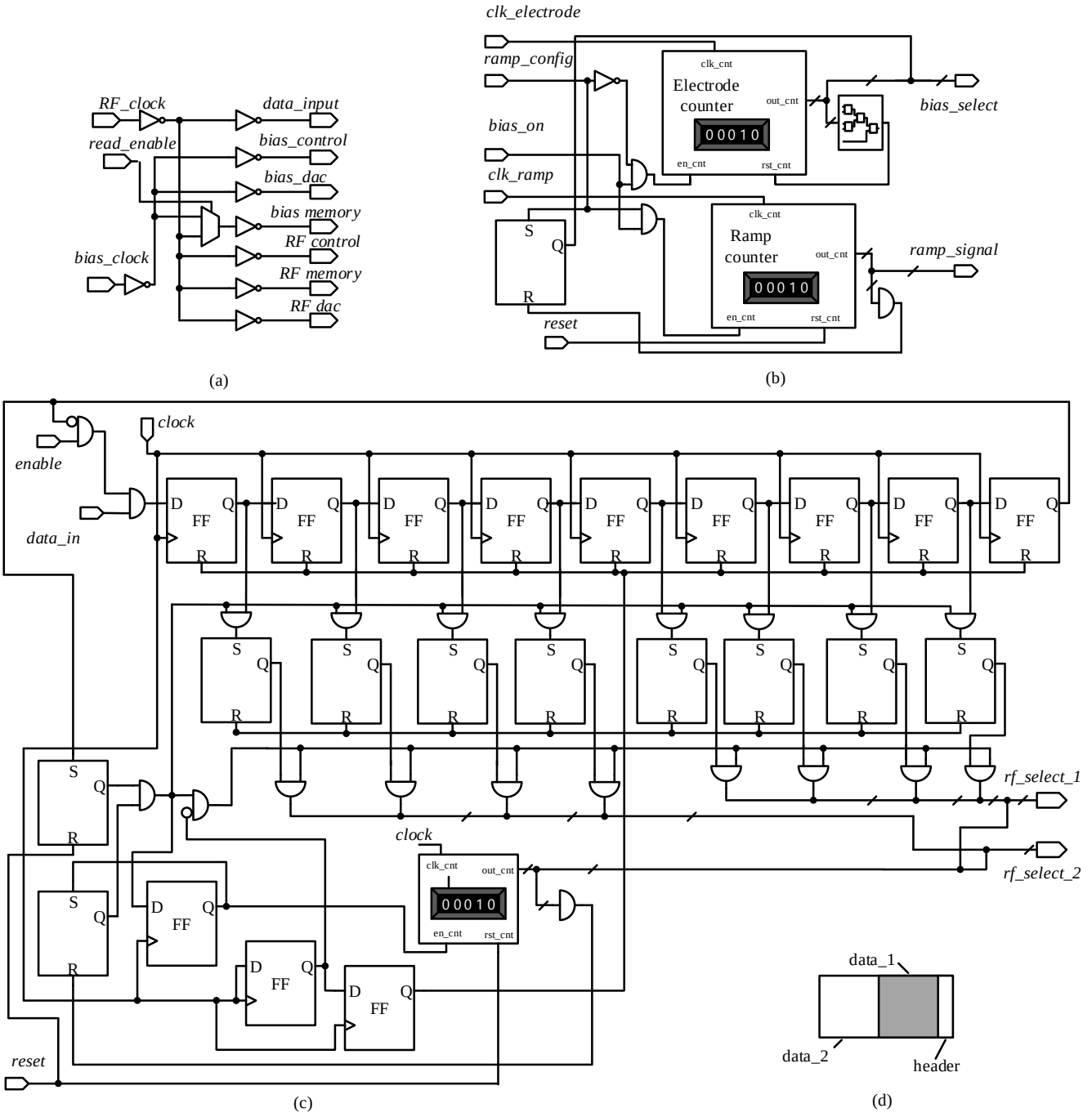

FIG. 13. a) Concept of the *clock control* unit, which distribute clock signals to the other subunits of the managing component. The inverters help improving edge steepness. b) Structure of the *bias control* unit, which steers the tuning of the qubit and the refresh of the voltages applied to the qubit electrodes. c) Concept of the *RF control* unit which, receives instructions on the sequences to apply for qubit operations. d) Structure of the RF data word.

and manages the generation of bias signals through preparing the digital signal inputs of the bias generation unit. It either reads values from the bias memory (see Fig. 4a during gate operation or provides voltages values itself during dot tuning.

If *ramp_config* is logical '0', the bias control unit is in the "refresh mode", and the voltages on all qubit electrodes get periodically refreshed during qubit operation. In this mode the *bias_select* output of the bias-control unit is connected not only to the *read_select* input of the bias memory, but also to the *electrode_select* input of the bias-generation unit. This ensures that the voltage level

stored in a certain memory register is available at the *dig_in* (Fig. 5) input of the bias generation unit and the right voltage is applied to the right qubit electrode. The periodicity is achieved with an automatic reset of the counter, which counts through all electrodes.

If *ramp_config* is logical '1', the unit is in the "tuning mode", which allows applying a voltage ramp to one of the electrodes forming the double dot – a procedure which is necessary for the initial tuning-up of the qubit in the right operation regime [37]. In this case, the output *ramp_signal* is connected to the input of the bias generation unit, and the ramp counter generates a digital stepwise ramp, which is converted into an analog voltage ramp by the bias generation unit. In the mean while, the *electrode_select* input of the bias generation unit is connected to the *data_out* of the memory, and determines to which electrode the voltage ramp is applied. The address of the electrode is stored in one bias memory register and the read availability at *data_out* is activated through the *bias_select* output. The electrode counter is deactivated in this mode.

Finally, the structure of the RF control unit is shown in Fig. 13c. This unit is responsible for applying gates and their associated pulses to the qubit while the succession of gates is determined by the higher levels of the quantum computer. Since the voltage values of all $N_{pulses} = 16$ sequences with their length of samples $l_{pulses} = 16$ (see Sec. II A, Tab. I) are stored in the RF memory (Fig. 4) only the information on which sequences to be applied needs to be communicated. The RF control unit serially receives data words in the form of Fig. 13d containing two sets of data next to a header. Each data set contains two 4 bit sequence identifiers (IDs) with $2^4 = 16$ unique IDs from '0000' to '1111' each for one RF electrode. The reception of the data works as with the data input control. When the sequences applied before are finished (*end_sequ* ='1') the values from the flip-flops are transferred to the array of latches leaving the flip-flops free for a new data input immediately. At the same time the complete sample addresses are constructed one after one from the IDs and the sample counter indicating the number of the sample in the current sequence. The addresses are supplied to the *read_select1,2* memory inputs via the *rf_select1,2* outputs with the memory outputs in turn *data_out1,2* connected to the *dig_in* inputs of the RF generation unit supplying the digital voltage values to be converted to analog voltages.

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