

Interconnects & Nanowires

Heterogeneous Integration
&
Interconnection Techniques

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SPRING 2021

Outline

- Introduction
- Heterogeneous Integration
- Interconnection Techniques

Introduction

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Systems has driven innovations in both semiconductor and packaging technologies to response the simultaneous demand for:

- Faster data rate
- Lower power consumption
- Smaller components
- Higher level of integration
- High power handling capabilities

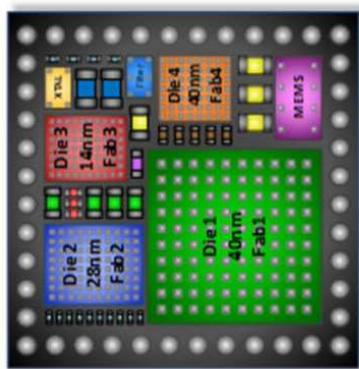
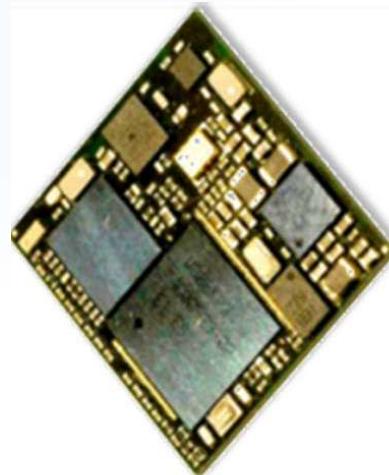
Like a Kid in Candy Store, We Want it All ... and Now!

On the semiconductor front:

	Large-scale integration	Analog/digital mixed signal capabilities	Low cost	High-frequency performance	Higher power handling capabilities
Silicon (Si)-based CMOS	✓	✓	✓		
BiCMOS (SiGe and CMOS)		✓		✓	
III-V semiconductors (gallium arsenide (GaAs), gallium nitride (GaN))		✓		✓	✓

Heterogeneous Integration

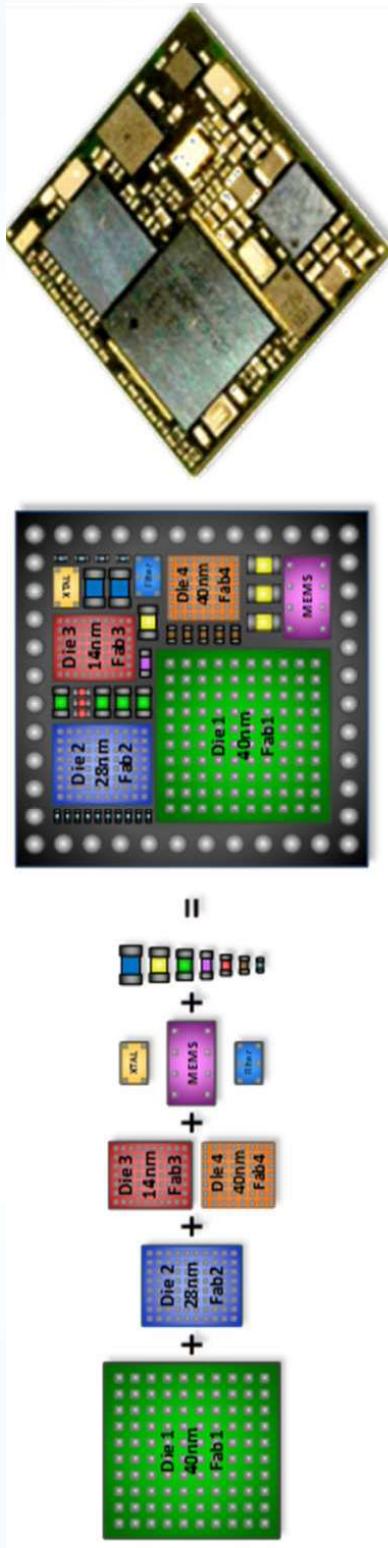
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Source: ASE [1]

Heterogeneous Integration

- Heterogeneous Integration refers to the integration of separately manufactured components into a higher-level assembly (System in Package – SiP) that, in the aggregate, provides enhanced functionality and improved operating characteristics.
- In this definition, components should be taken to mean any unit, whether **individual die**, **MEMS device**, **passive component** and **assembled package** or **sub-system**, that are integrated into a single package.



Die + Heterogeneous

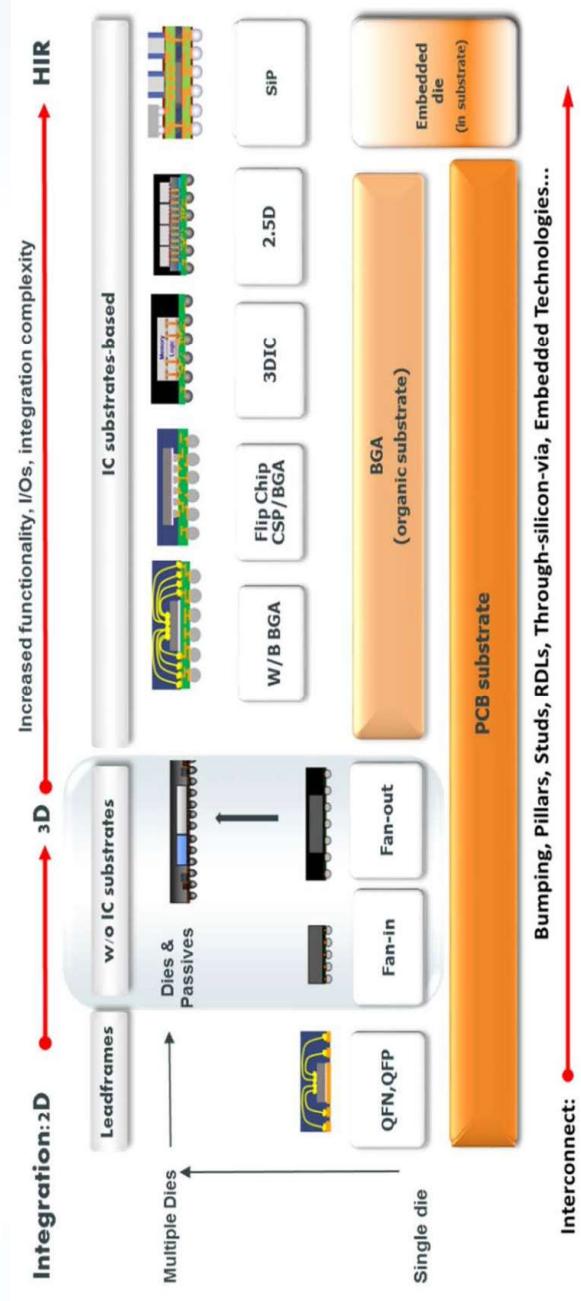
System in Package (SiP)

Heterogeneous Integration and System in Package (SiP). Source: ASE

Heterogeneous Packaging Platforms

Some packaging platforms that can be used for heterogeneous integration classify as **heterogeneous integration using:**

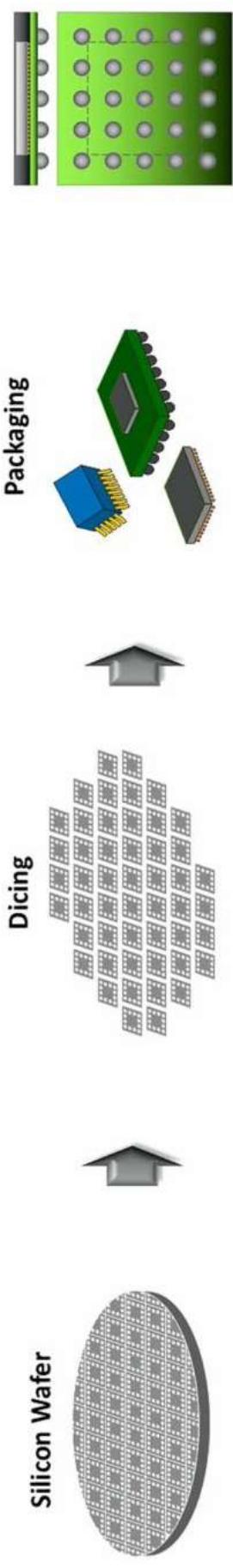
- a. Wafer Level Package (WLP)
- b. Co-fired Ceramic
- c. Organic Package Technology
- d. Additive manufacturing (AM)
- e. Interposer Technology



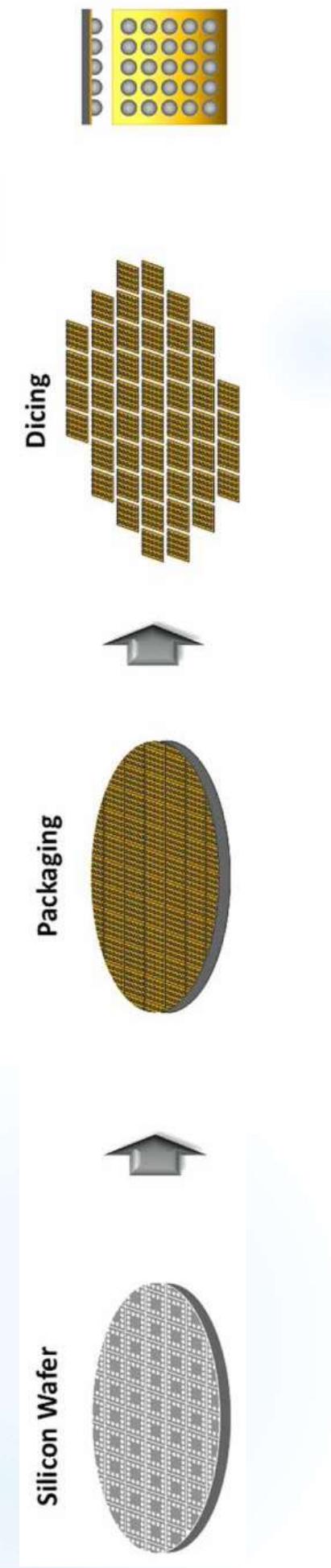
Source: Heterogeneous Integration Roadmap, HIR Overview and Executive Summary, 2019

Semiconductor Packaging Trends

Traditional packaging process flow

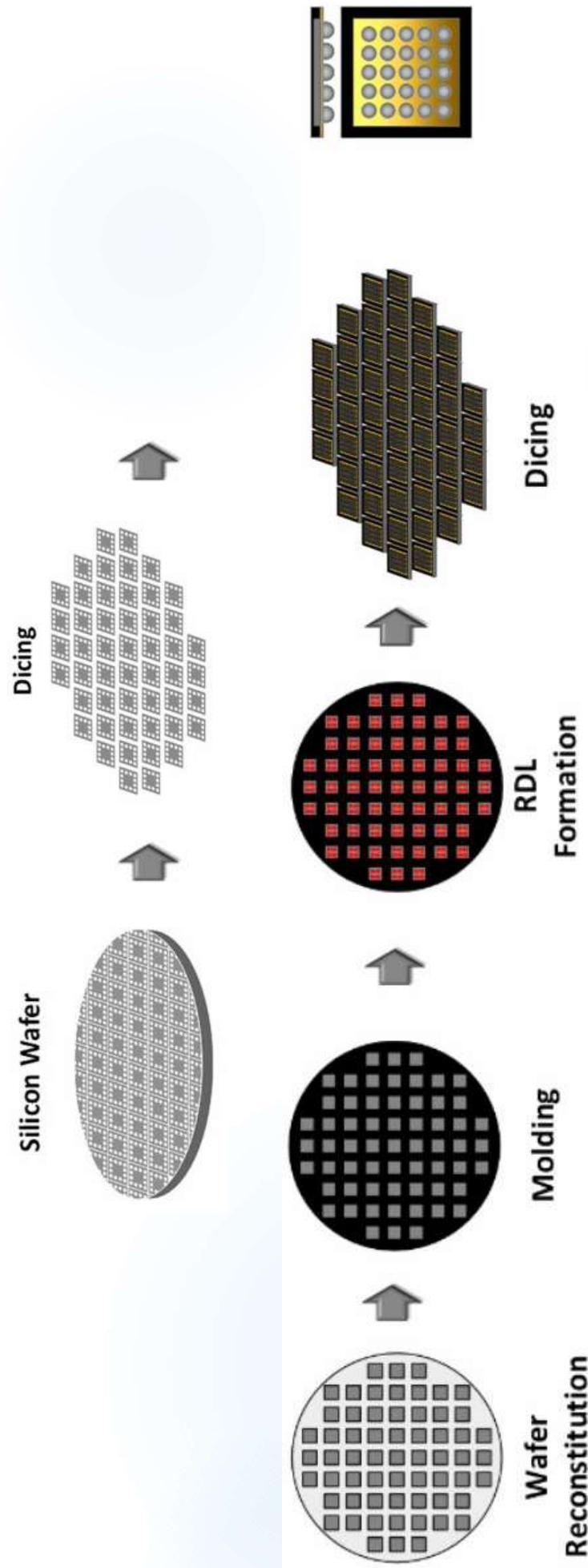


Wafer level packaging process flow



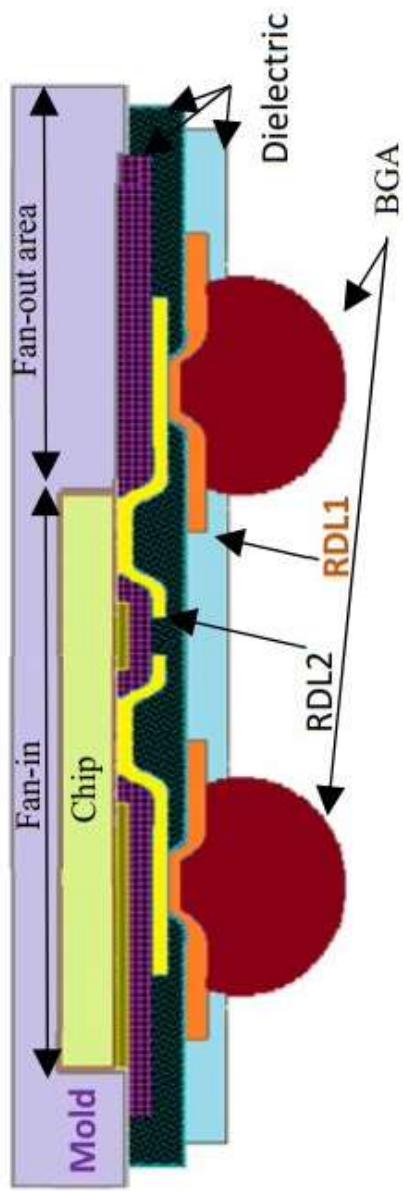
Semiconductor Packaging Trends

eWLB (WL fan-out) packaging process flow



Semiconductor Packaging Trends

Embedded Wafer Level Ball Grid Array

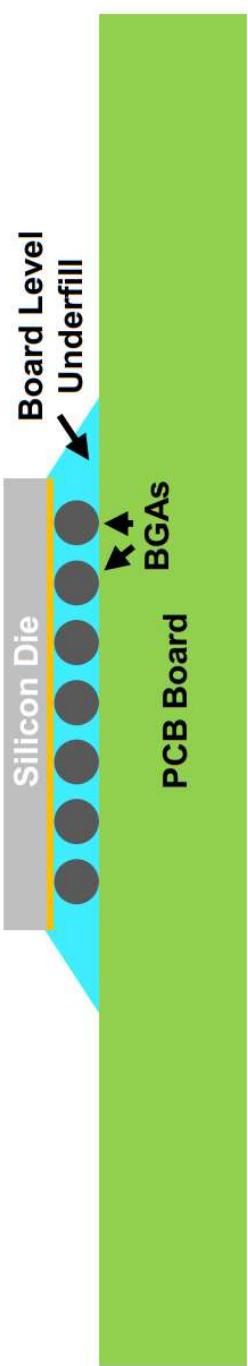


Early Infineon eWLB baseband fan out (2009)

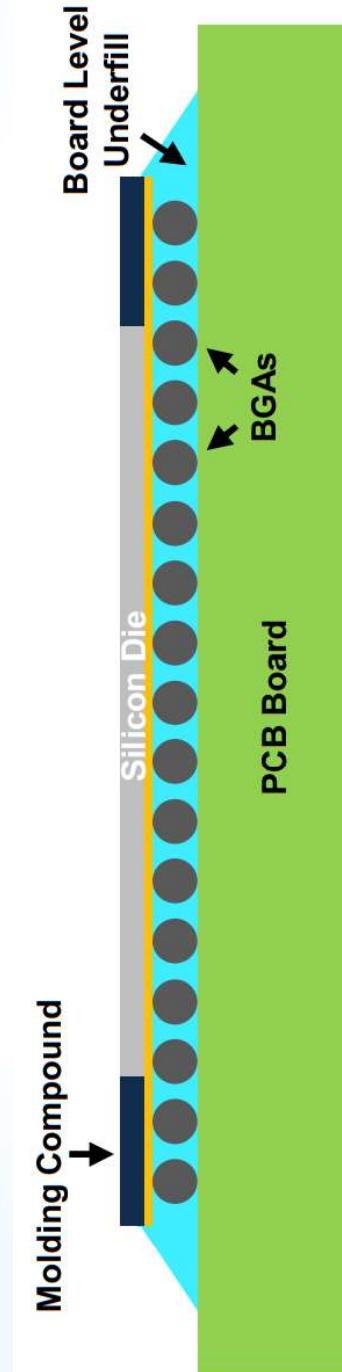
All process steps for the generation of the package are performed on the wafer

Semiconductor Packaging Trends

WLCSP vs. eWLB



Structure of a WLP Package



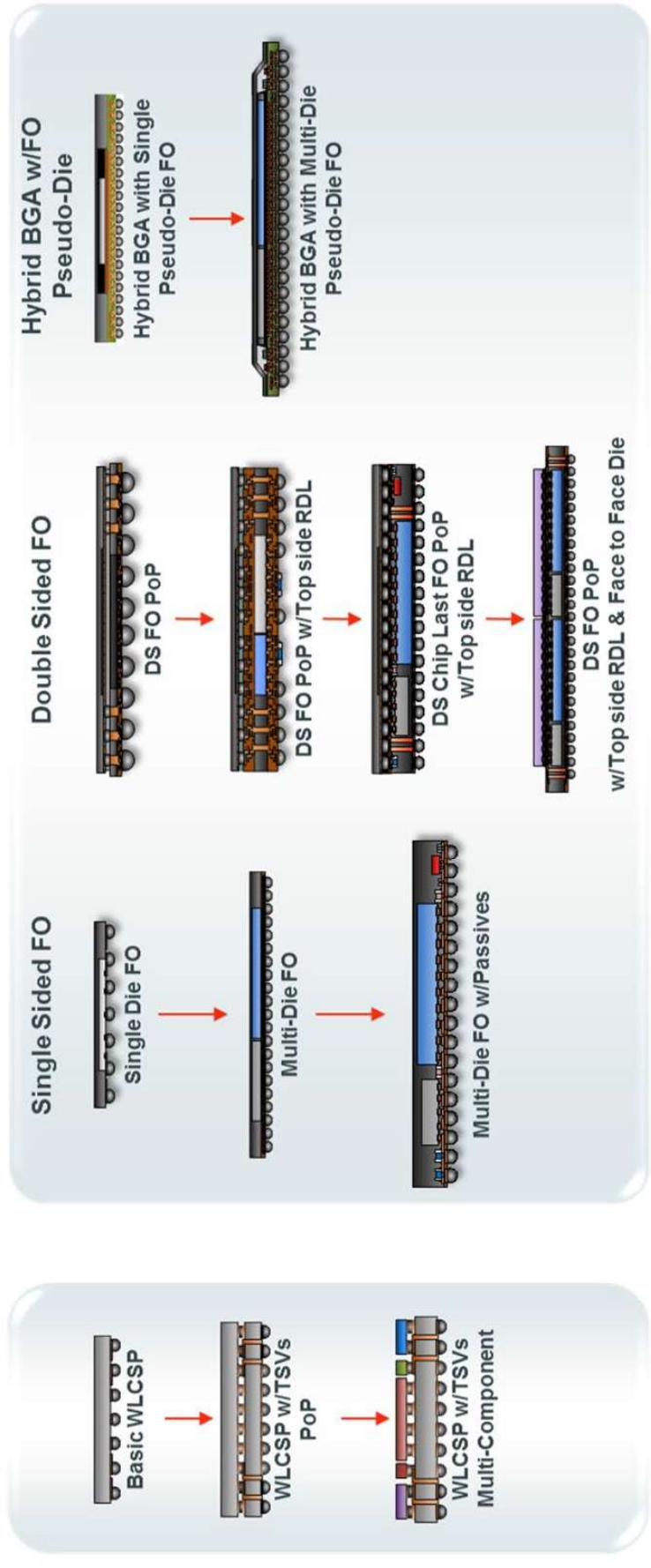
Structure of a eWLB (FOWLP) Package

Heterogeneous Packaging Platforms

a. Heterogeneous integration using WLP

WLCSP

Fan Out



Source: Heterogeneous Integration Roadmap (HIR), Wafer Level Packaging, 2019

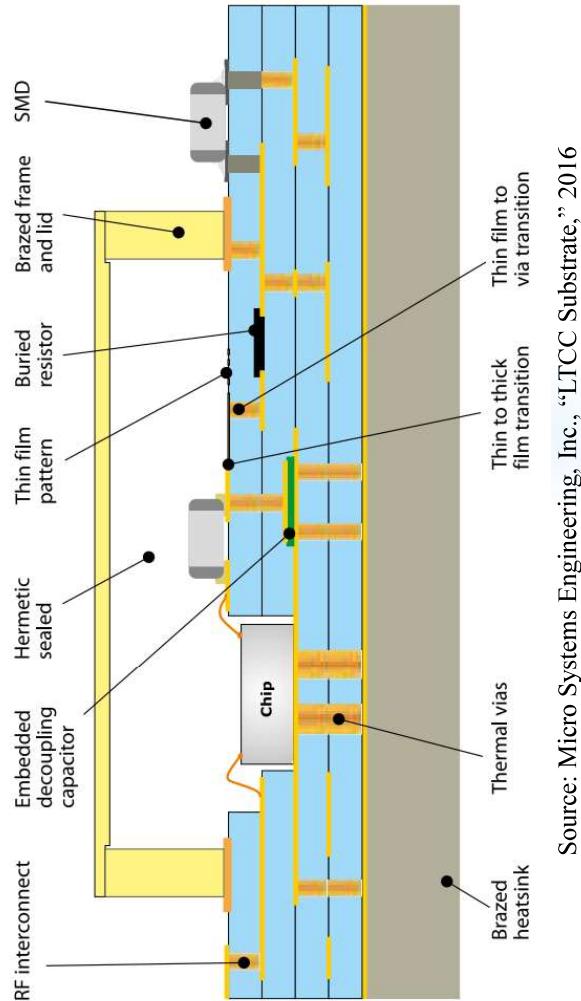
Heterogeneous Packaging Platforms

b. Heterogeneous integration using Co-fired Ceramic

Co-fired ceramic devices are **monolithic, ceramic microelectronic devices** where the entire ceramic support structure and any conductive, resistive, and dielectric materials are fired in a kiln at the same time.

Co-firing { **low temperature** (below 1,000 °C) **high temperature** (around 1,600 °C)

low temperature co-fired ceramic (LTCC) technology



Lower peak temperature of LTCC permits the co-firing with **highly conductive** materials (silver, copper, and gold).

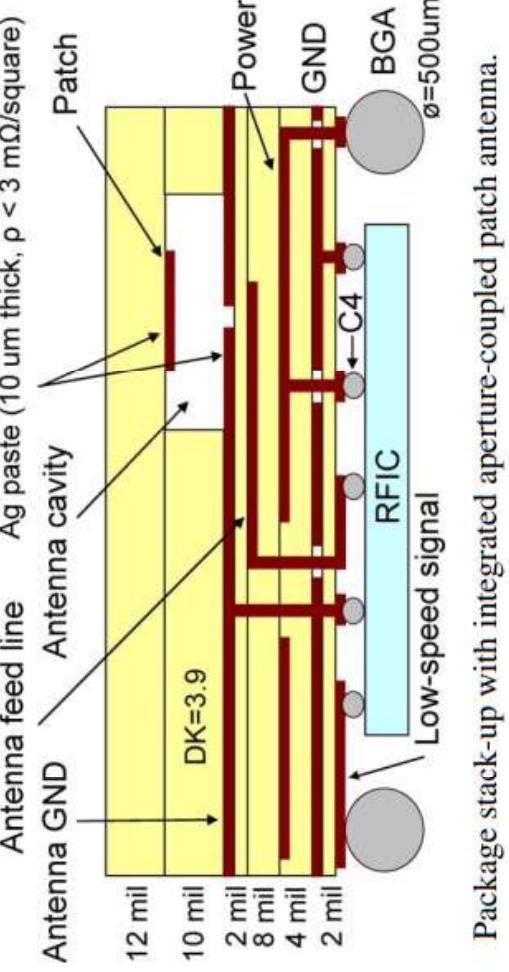
Source: Micro Systems Engineering, Inc., "LTCC Substrate," 2016

Heterogeneous Packaging Platforms

b. Heterogeneous integration using Co-fired Ceramic

- A low-cost, fully-integrated antenna-in-package solution for **60 GHz** phased-array systems is demonstrated.
- **Sixteen patch antennas** are integrated into a **28 mm * 28 mm** ball grid array (**288-pin**) together with a flip-chip attached transmitter or receiver IC.
- The packages have been implemented using **low temperature co-fired ceramic (LTCC)** technology.

- An air cavity is used beneath the aperture-coupled superstrate patch antenna to **improve bandwidth and radiation efficiency**.
- One structure that had to be carefully optimized is the flip chip transition, as it directly affects the **antenna bandwidth**.
 - ✓ a **smaller pad**, a **larger pitch** and a **smaller bump diameter** are generally preferred.



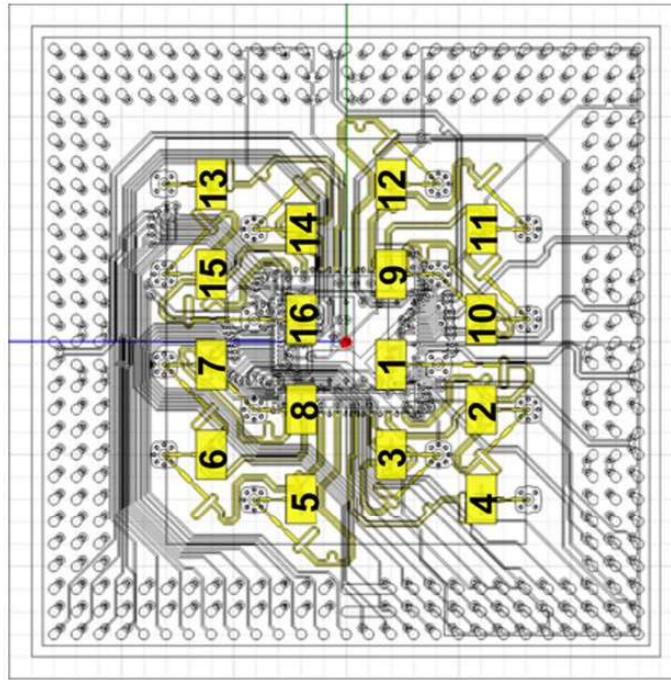
Item	Dimension
Pad size	100 um
pad pitch size	250 um

Package stack-up with integrated aperture-coupled patch antenna.

Heterogeneous Packaging Platforms

b. Heterogeneous integration using Co-fired Ceramic

- One disadvantage of flip-chip **BGA packaging** is the **poor thermal dissipation**, because the thermal connection between the silicon and package is mainly the connecting bump on the pads.
- To reduce the **thermal resistance**, this chip should have as **many ground bumps in the neighborhood of thermal source**, for example the TX chain.

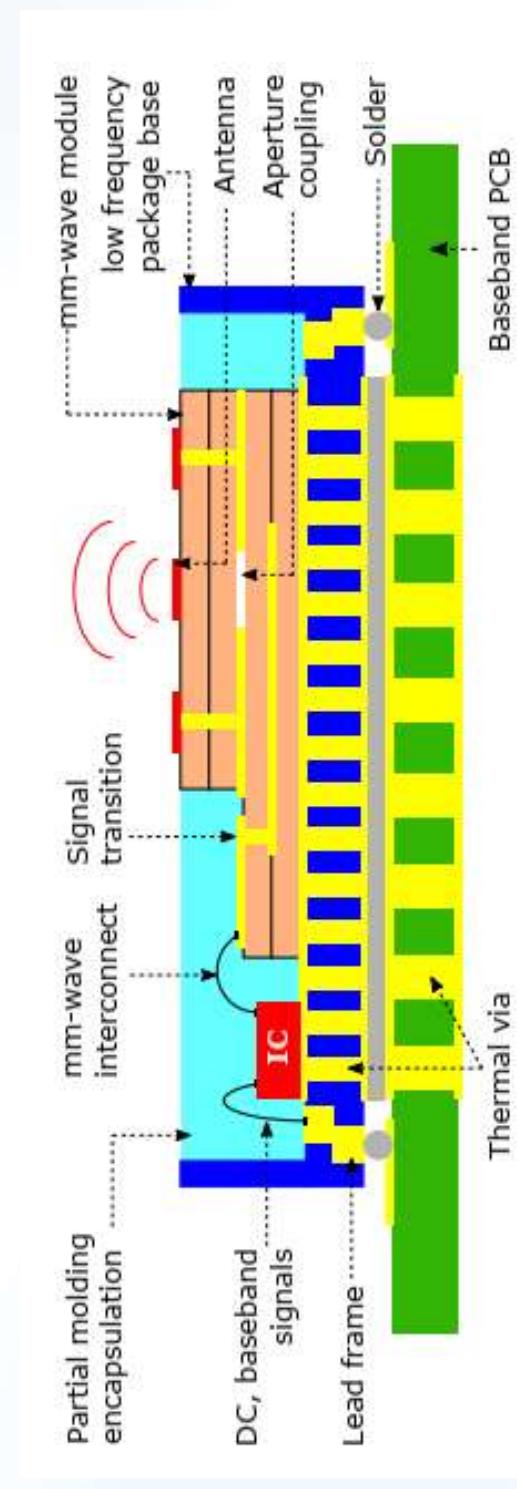


HFSS model of Tx package with 60 GHz interconnects highlighted in yellow (package size = 28 mm × 28 mm, antenna GND = 27 mm × 27 mm).

Heterogeneous Packaging Platforms

b. Heterogeneous integration using Co-fired Ceramic

- A fully integrated single-chip transceiver having higher element counts and reduced power consumption per element can simplify **system design** and **reduce cost**. [3]
- However, implementation of the TX and RX as separate chips can simplify **thermal management** and improving **isolation**.



Integrating a **122 GHz** silicon germanium (SiGe) radar transceiver chip in an LTCC based (System-in-Package (SiP)) (20018)

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Heterogeneous Packaging Platforms

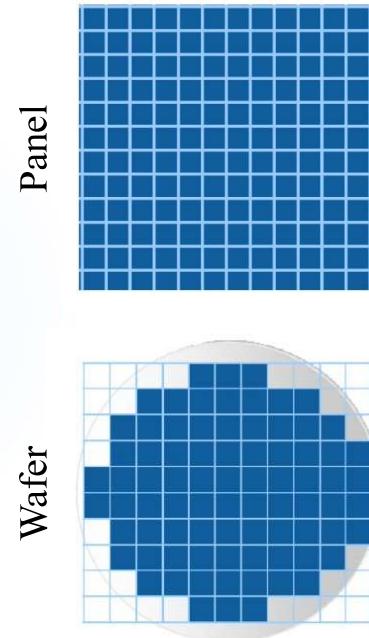
c. Heterogeneous integration using Organic Package Technology

➤ There are various organic materials such as:

- Liquid crystal polymer (LCP)
- Polyimide
- Rogers RO3003

➤ Organic material offer:

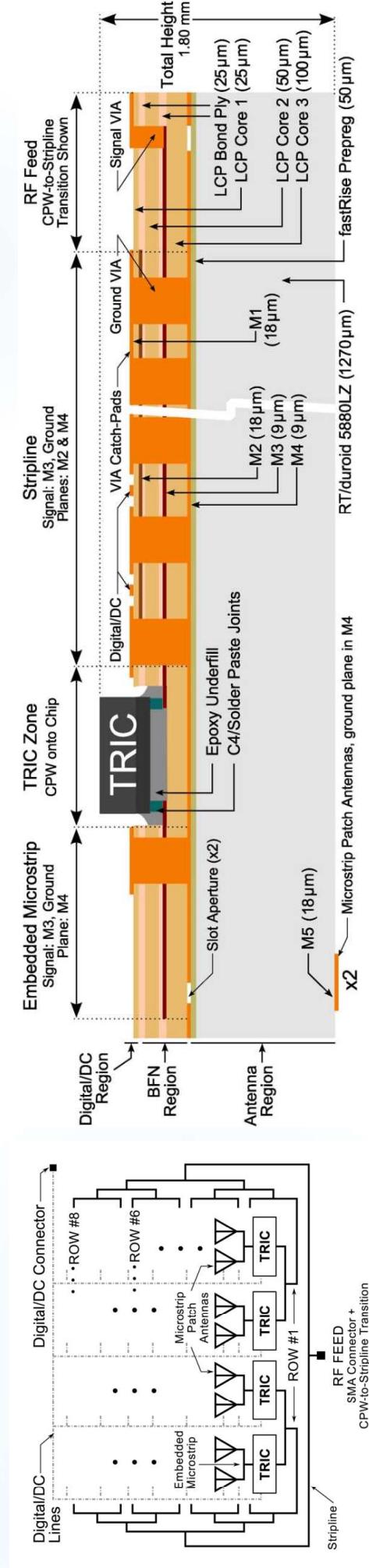
- Low loss
- Low cost
- Compatibility with large area PCB panel format processing →
- Low melting temperature (around 300 °C) compared with LTCC



Heterogeneous Packaging Platforms

c. Heterogeneous integration using Organic Package Technology

- 32 SiGe, transmit/receive integrated-circuit (TRIC) modules have been flip-chip bonded to the array board.
- Each SiGe TRIC drives a pair of slot-coupled microstrip patch antennas that form an **8 × 8 rectangular array**.
- All components are packaged in an organic substrate stack of **liquid crystal polymer (LCP)** and **RT/Duroid 5880LZ**.
- The organic package occupies an area of **30.5cm × 25.4cm** and has a total thickness of only **1.80 mm**.



An Ultra-Thin, High-Power, and Multilayer Organic Antenna Array With T/R Functionality in the X-Band, IEEE Transactions on Microwave Theory and Techniques, 2012

Heterogeneous Packaging Platforms

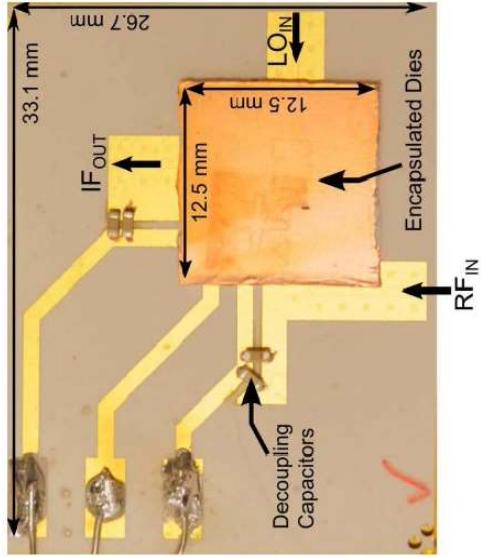
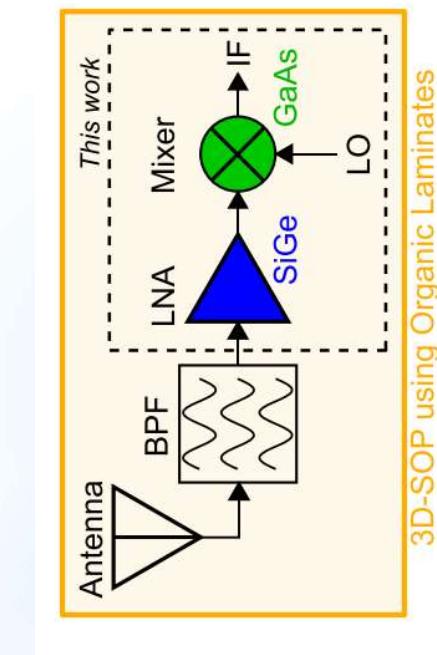
c. Heterogeneous integration using Organic Package Technology

A heterogeneous **wideband receiver (4–14 GHz)** has been designed and fabricated.

It is composed of:

- a flip-chip bonded SiGe BiCMOS low-noise amplifier (LNA)
- a ribbon bonded GaAs MESFET double-balanced mixer

Both chips are embedded within an organic packaging laminate (RO3003)



Encapsulated Organic Package Technology for Wideband Integration of Heterogeneous MMICs, IEEE Trans. Microw. Theory Techn., 2017

Heterogeneous Packaging Platforms

d. Heterogeneous integration using Additive Manufacturing (AM)

- Additive manufacturing (**AM**), and specifically the so-called **direct write technologies**, may provide a viable solution for the packaging of mm-wave electronics.
- With AM techniques, structures need **not be limited** to a **flat plane**, and the technology is capable of tailoring a design to a specific application.
- Additive manufacturing (AM) refers to a wide class of 3D printing technologies ranging from laser-based metal printing approaches to the jetting of photocurable resins.

Some considerable additive manufacturing technologies are:

- **Inkjet printing**
- material extrusion
- powder bed fusion
- binder jetting
- vat photo-polymerization
- directed energy deposition
- sheet lamination



Heterogeneous Packaging Platforms

d. Heterogeneous integration using Additive Manufacturing (AM)

The design of the 3D interconnects is composed of the following elements:

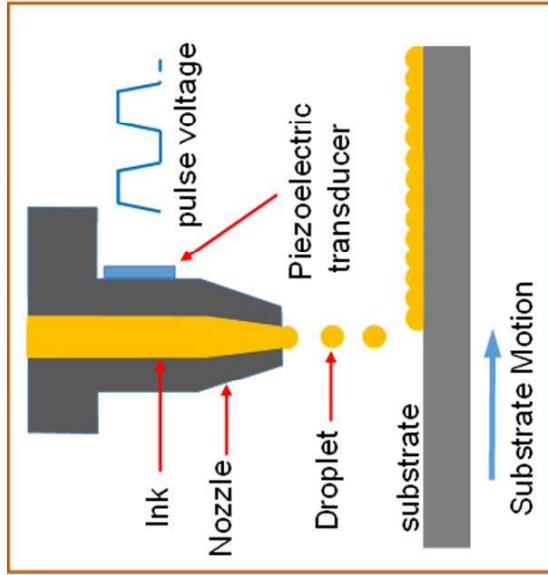
- 1- A packaging substrate
- 2- A die attach material
- 3- An IC die
- 4- A dielectric ramp structure
- 5- Transmission lines



Cross-section of inkjet-printed 3D interconnect

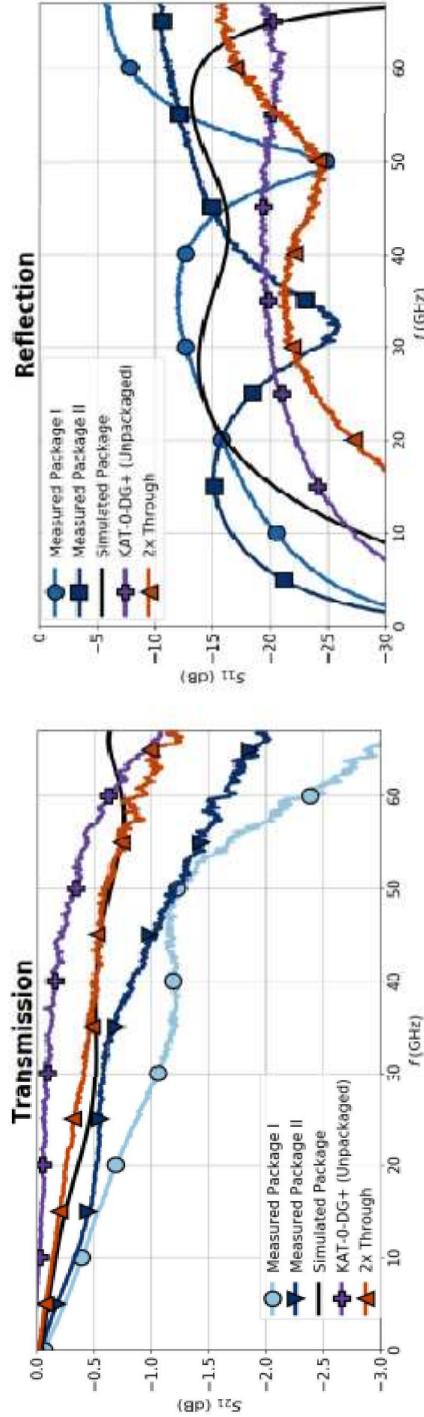
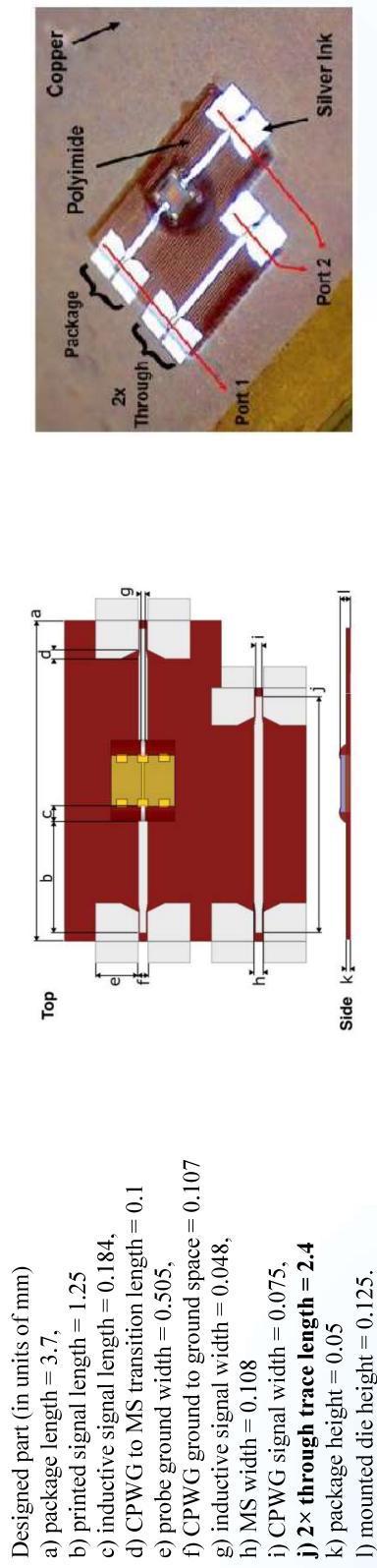
"Inkjet-printed 3D interconnects for millimeter-wave system-on-package solutions," 2016

Inkjet printing technology



Heterogeneous Packaging Platforms

d. Heterogeneous integration using Additive Manufacturing (AM)

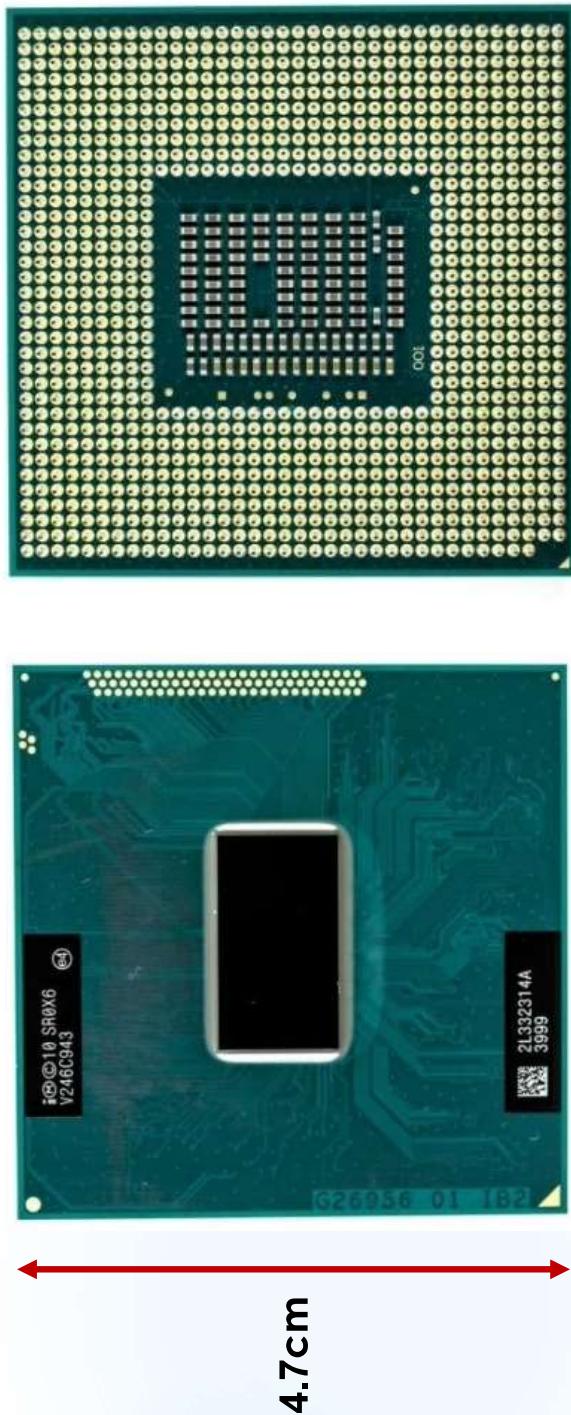


“A Chip-First Approach to Millimeter-Wave Circuit Packaging,” IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS, 2019.

Heterogeneous Packaging Platforms

e. Heterogeneous integration using Interposer Technology

- An interposer is an electrical interface routing between one socket or connection to another.
- The purpose of an interposer is to spread a connection to a wider pitch or to reroute a connection to a different connection.

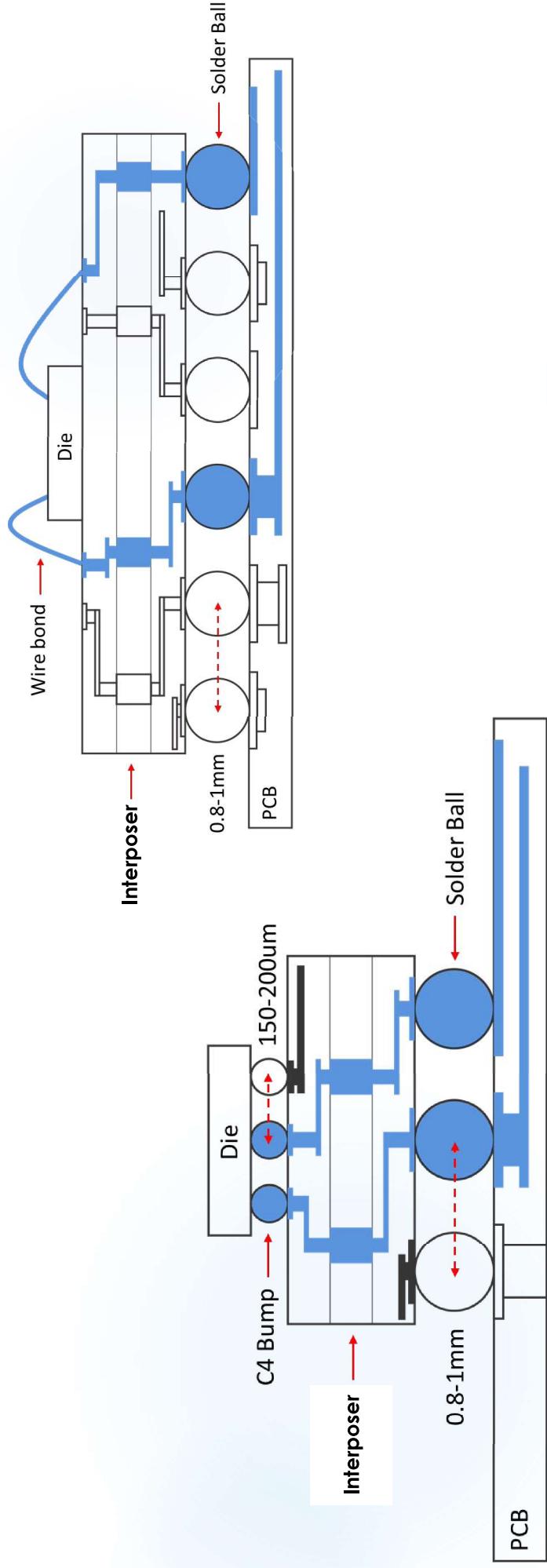


intel 2 Cores i7-3540M SROX6 Socket G2 **PGA988B** Laptop CPU Processor 3GHz 4MB

Heterogeneous Packaging Platforms

e. Heterogeneous integration using Interposer Technology

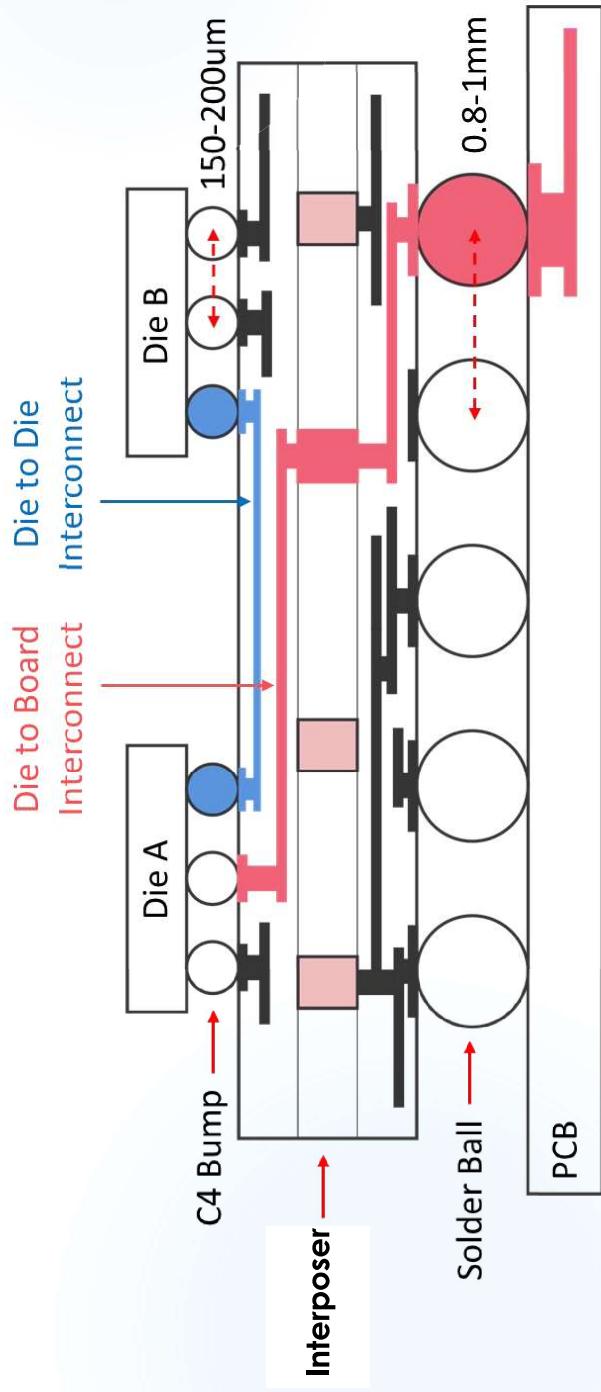
- Main stream packaging solutions for die to board communication using interposer technology:



Heterogeneous Packaging Platforms

e. Heterogeneous integration using Interposer Technology

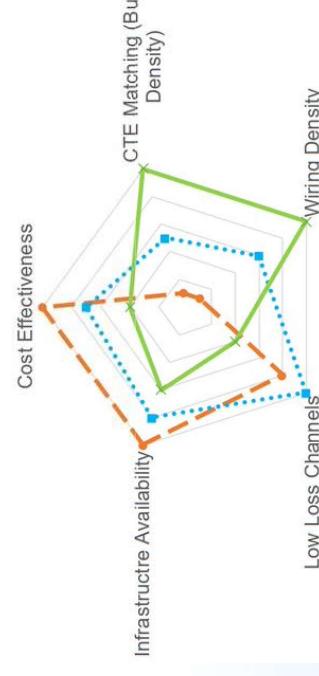
- New applications of interposer technology as a packaging solution for heterogenous integration:



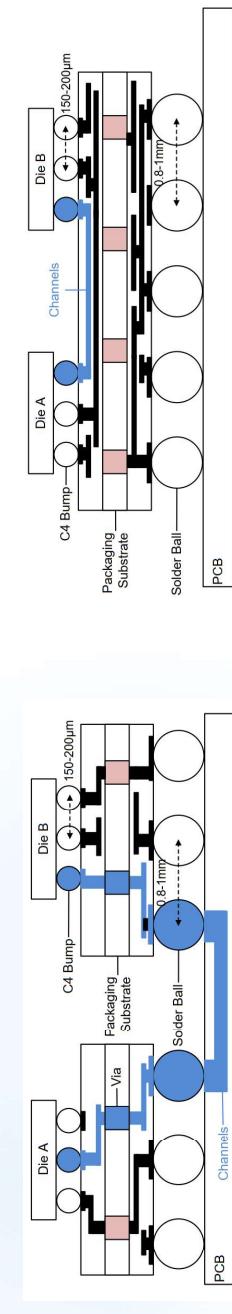
Heterogeneous Packaging Platforms

e. Heterogeneous integration using Interposer Technology

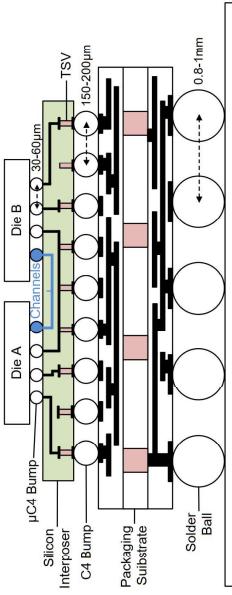
➤ Comparison between **organic substrates** and **silicon interposers** with respect to **regular PCBs**:



Packaging solution	Connection to die	Trace width and spacing resolution	Loss @ 10GHz	Cost
Organic Substrate	Flip-chip mounted using C4 bumps (150 – 200 um pitch)	>20um	1 dB for 4.5mm channel	Cheap
Silicon Interposer	Flip-chip mounted using uC4 bumps (30 – 60 um pitch)	Sub-micrometer	10 dB for 20mm channel	Expensive
Regular PCBs				



Conventional chip-to-chip communication where two chips communicate through interconnects on a **PCB**.



First main stream packaging solution for die-to-die communication (sharing a **organic** packaging substrate between multiple chips).

Second main stream packaging solution for die-to-die communication (using a **silicon** interposer on top of the packaging substrate to create the interconnects between multiple chips).

Heterogeneous Packaging Platforms

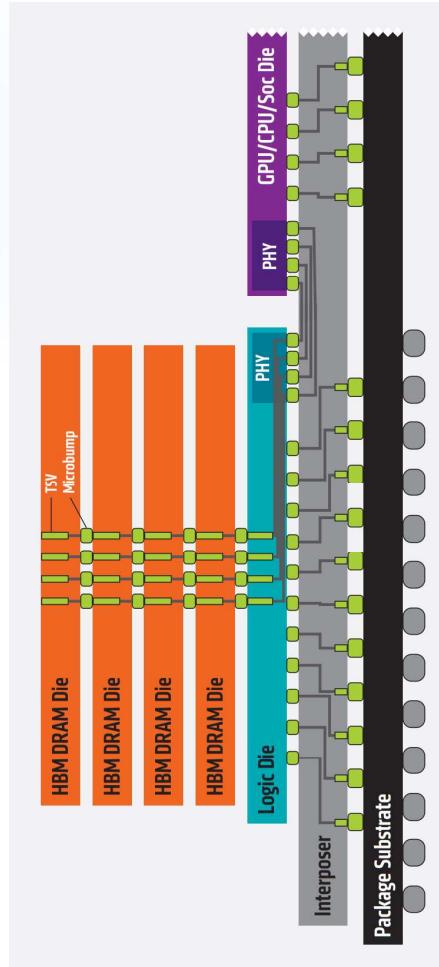
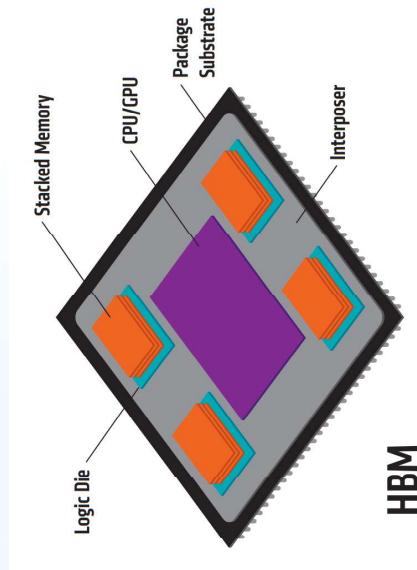
e. Heterogeneous integration using Interposer Technology

- Low dielectric-constant materials, including polymers and some ceramics, are being used as **interlayer dielectrics** for **multilayer interconnect** substrates.

- Very fine conductor lines
- Small vias
- Short electrical paths



- Electrical performance improved
- Increase the packaging density

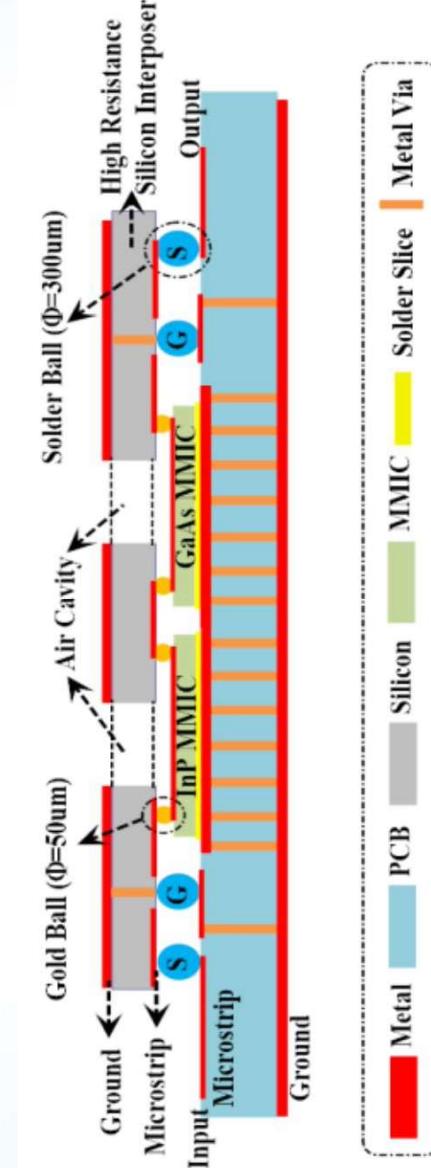


AMD has reported approximately 40% reduction in silicon fabrication cost along with improved system-level performance through 2.5D integration (2017)

Heterogeneous Packaging Platforms

e. Heterogeneous integration using Interposer Technology

- Silicon interposer package solution is proposed for MMIC heterogeneous integration.
- The GaAs/InP MMICs are integrated to the silicon interposer by the gold ball flip-chip technique. Then, the whole silicon interposer with the heterogeneous integrated MMICs is assembled to the PCB top layer by the solder ball flip-chip technique.
- In this proposed silicon interposer package solution, the microwave signal can be transmitted from the PCB to the heterogeneous integrated MMICs without deterioration.



The cross section view of the silicon interposer package for MMIC heterogeneous integration

Interconnection techniques



Package interconnects classification

- As system integration migrates from “**on-chip**” to “**in-package**”, I/O signal integrity (SI) and package-level power distribution effectiveness become essential to sustaining system advancement.
- Package interconnects may be classified as:
 - a. Die-Die Interconnects
 - b. On-package Die-Die Interconnects
 - c. Die-to-Package Interconnects (**First Level Interconnect**)
 - d. Within-Package Interconnects
 - e. Package-to-Board (Motherboard) Interconnects (**Second Level Interconnect**)
 - f. POP (Package-on-Package) Interconnects (Vertical Interconnects)

Package interconnects classification

a. Die-Die Interconnects

Interconnects between stacked die that enable vertical interconnects between multiple die in a 3-D stack. These may be further sub-categorized as:

- Wafer-to-Wafer attach process
- Die-to-Wafer attach process
- Die-Die attach process

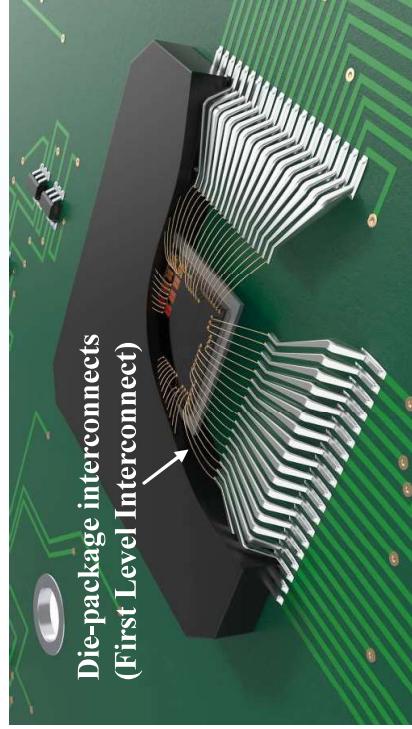
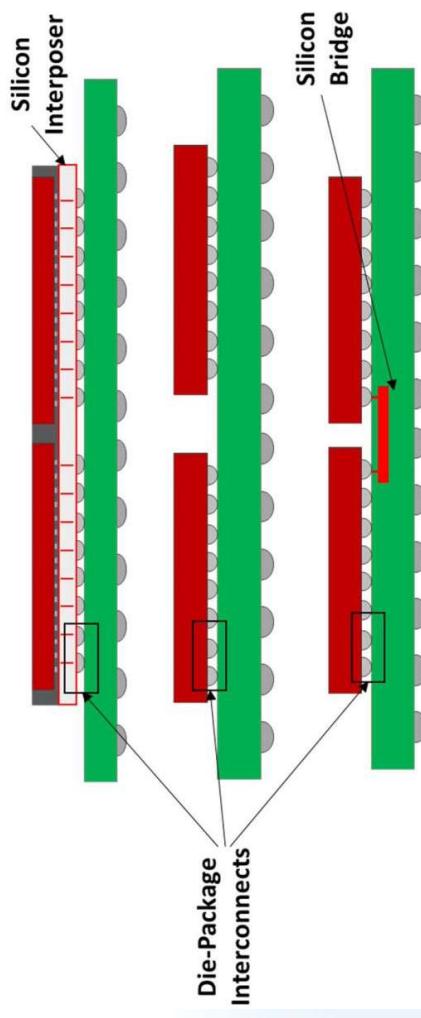
b. On-package Die-Die Interconnects

Interconnects between die within the package that enable lateral connections

Package interconnects classification

c. Die-to-Package Interconnects (First Level Interconnect)

Interconnects between the die and the package, typically known as the first level interconnect (FLI)



Die-Package Interconnect Pitch Roadmap

Year of Production	2018	2019	2020	2021	2022	2023	2024
Au Wire bond - Single in-line (μm)	40	35	35	30	30	30	30
Cu wire – single inline (μm)	40	35	35	30	30	30	30
Flip chip array, low end & consumer	150	150	130	130	130	130	130
Flip chip – cost performance	110	110	110	100	100	100	90
Flip chip – high performance	110	100	100	90	90	90	90

Heterogeneous Integration Roadmap (HIR), 2019.

Package interconnects classification

d. Within-Package Interconnects

Interconnects within the package that enable lateral connections between two nodes or electrodes.

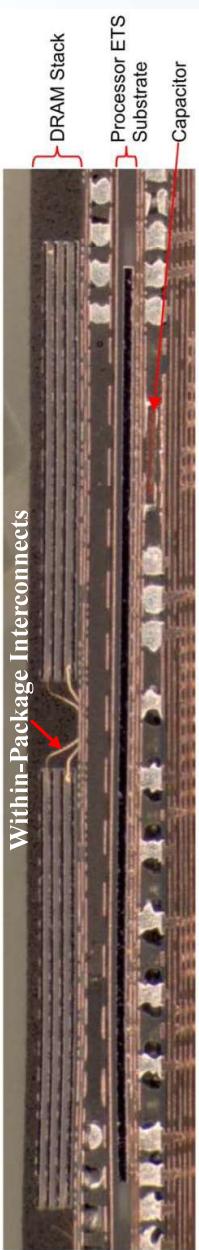
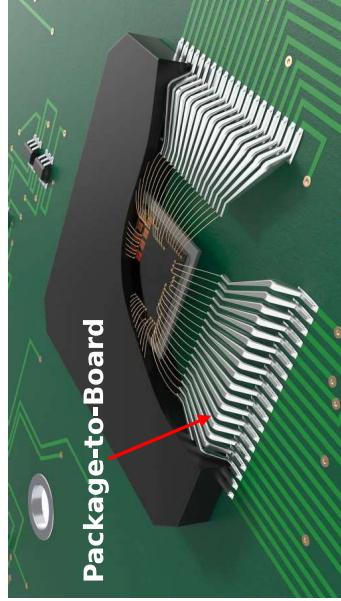
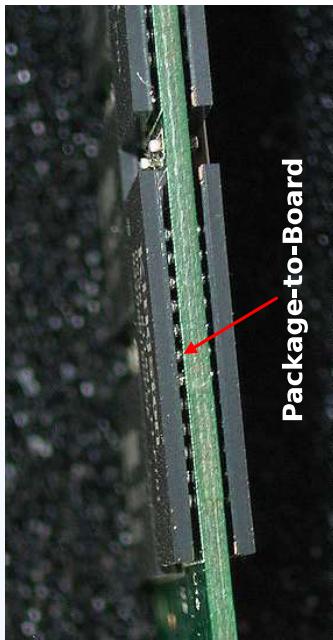


Photo source: Prismark/Binghamton University

PoP cross-section for Qualcomm 855 processor in Samsung Galaxy 10 Smart Phone

e. Package-to-Board (Motherboard) Interconnects (Second Level Interconnect)

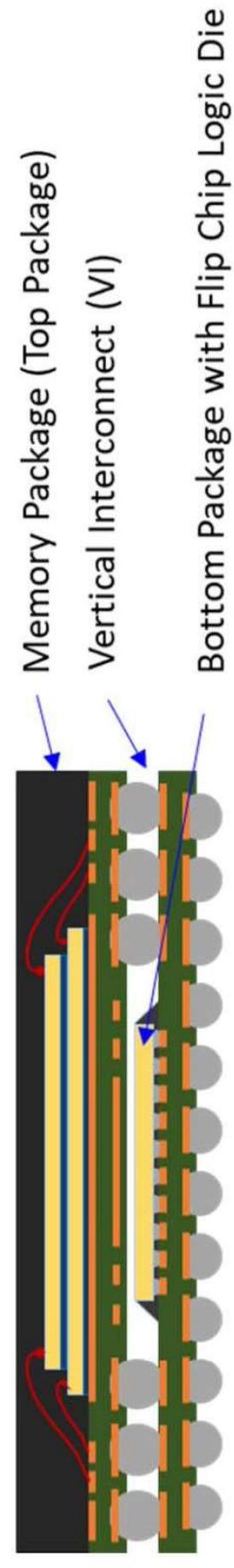
Interconnects between the package and the next level, which is typically the motherboard, are referred to as the second level interconnect (SLI)



Package interconnects classification

f. POP (Package-on-Package) Interconnects (Vertical Interconnects)

The PoP construction allows for packages to be placed on top of other packages using peripheral package interconnects, also referred to as VI (Vertical Interconnects).



Typical Package-on-Package Architecture

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Most Popular Interconnects Techniques

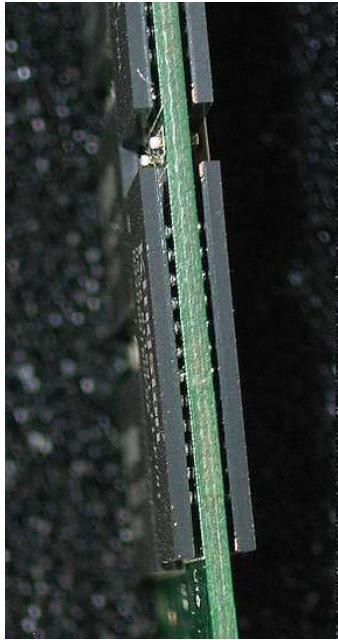
- When increasing density, i.e. reduced line pitch combined with increasing signal speeds, there will be great concerns about signal quality due to increased crosstalk caused by the reduced line spacing.
- Different interconnect strategies have been proposed to develop solutions that minimize impact to signal integrity and provide physical links with improved power efficiency.

Most Popular mm-wave interconnects techniques:

Wire bonding techniques



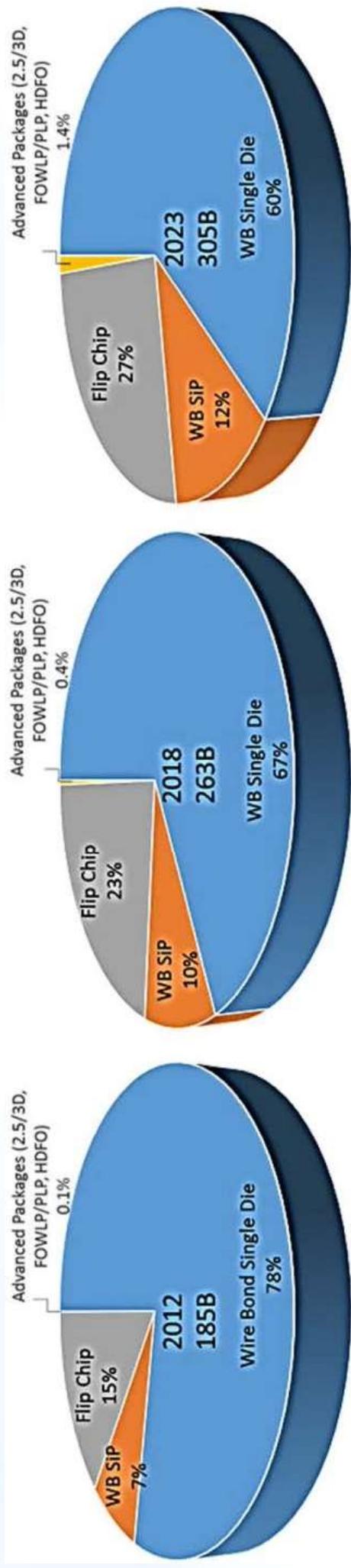
Flip chip techniques



Wire bonding methods

- Conventional methodologies typically use wire bonds to form interconnects between the chip and the board.
- Wire bonding continues to be the most dominant interconnection technology used in the electronic packaging industry due to its **low cost**, **high yield rate**, **design flexibility** and **proven reliability**.

semiconductor package growth by different interconnect methods



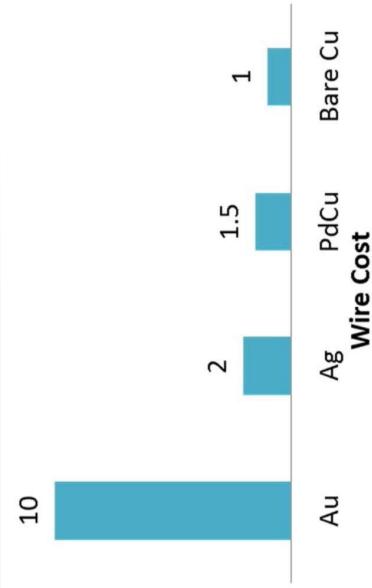
Semiconductor package unit growth by interconnect type. IC Package Shipment excluding Discrete, LED and Opto. Source: Prismark May 2019

Wire bonding methods

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- Wire bonding continues to drive toward:
 - lower cost
 - improved productivity
 - increased interconnect density
 - improved process monitor, real time control, and defect and factory management

- **Lower cost**
 - One of the biggest trends in wire bonding is replacing Au wire with lower-cost Cu and Ag wire.



Relative cost for different type of wires, based on 25um diameter wire (Source: Heraeus and Tanaka). 94% Ag alloy is used in the comparison.

By switching to a lower-cost wire, package cost can be reduced by 20%

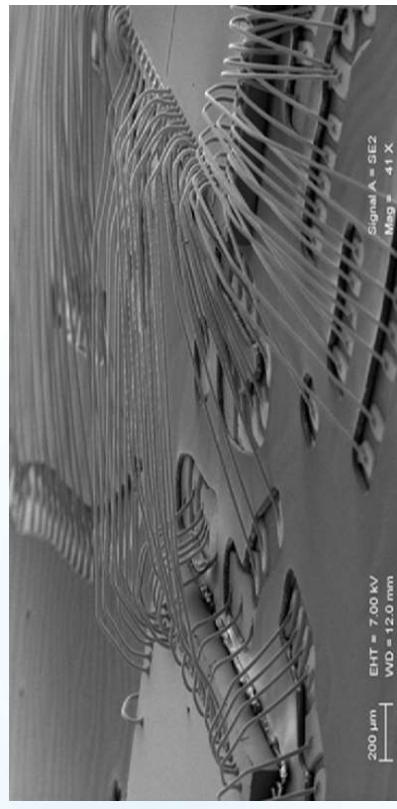
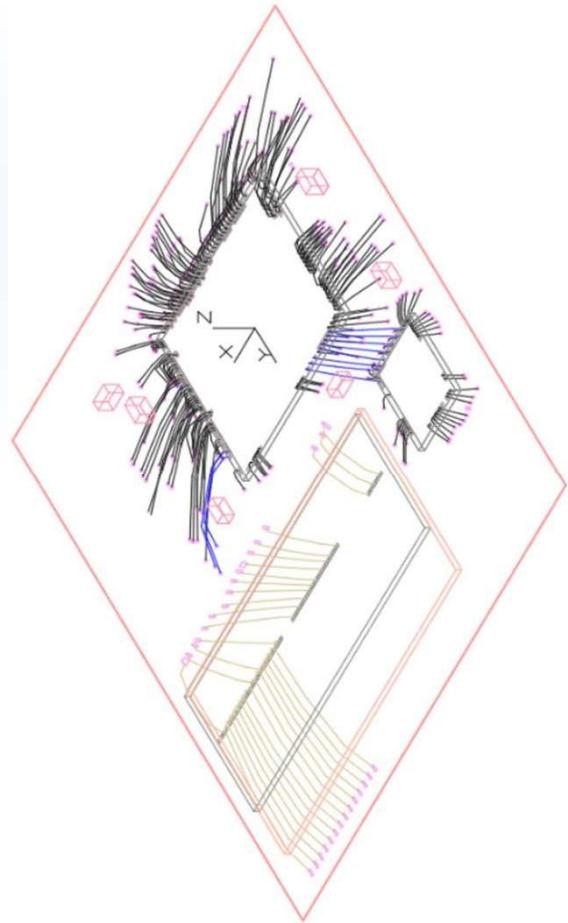
Wire bonding methods

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► Higher productivity

Through the years, wire bonders went through many technology advances to improve the speed of wire bonding.

3D loop design and clearance-check software, along with the wire loop model on the wire bonder side, reduce loop optimization time significantly.



Advanced multiple tier looping and die-to-die bonding loops

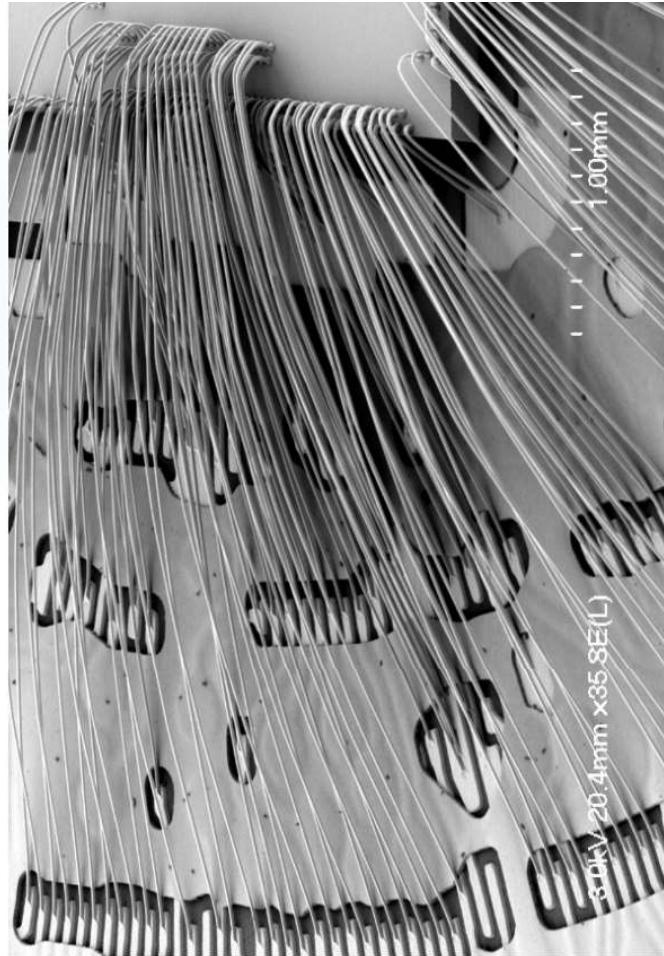
3D loop design and clearance check software

Wire bonding methods

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► Increase Interconnect Density

1. Fine pitch capability (The current finest pitch capability is **35um** in-line bond pad pitch)
2. Multitier pad designing (a **50um bond pad pitch** device with **4 pad rows** is a common configuration for packages over **1000 I/Os**)
3. Multiple-chip module and System in Package
4. Vertically stacking semiconductor devices
5. Wire bonded Vertical Interconnects



2. High density multi-tier package

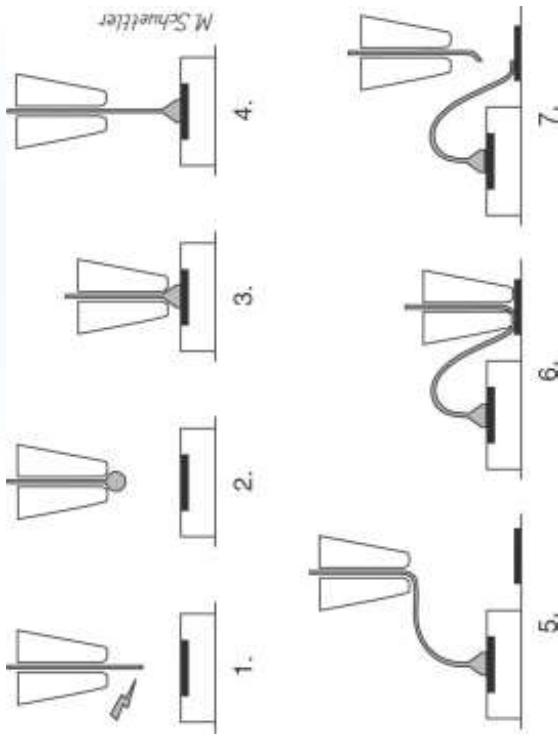
Wire bonding methods

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3. Stand-Off-Stitch Bond (SSB) process is more and more common on devices such as multi-chip modules, stack die and LED devices

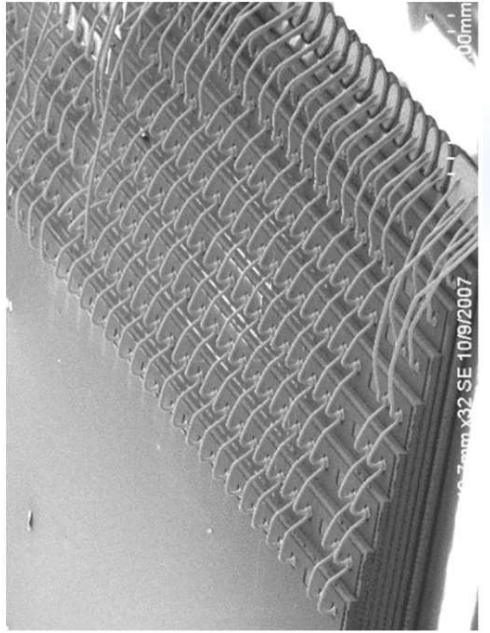


Bonding Method

Wire bonding methods

► Increase Interconnect Density

1. Fine pitch capability (The current finest pitch capability is **35um** in-line bond pad pitch)
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3. Multiple-chip module and System in Package
4. Vertically stacking semiconductor devices
5. Wire bonded Vertical Interconnects

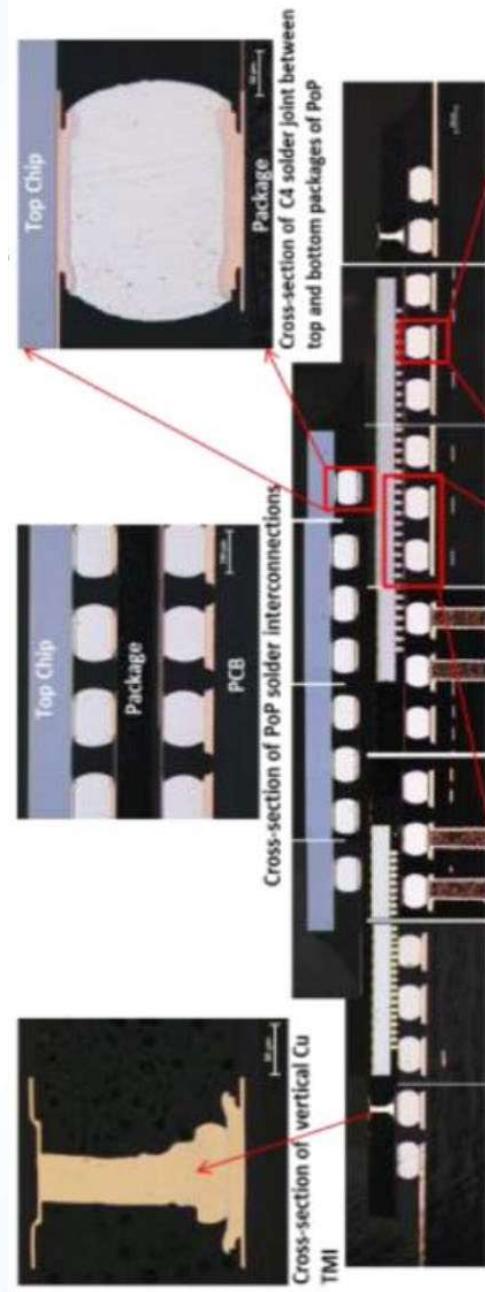


4. Examples of bonding on overhang die & Example of a stacked-memory device

Wire bonding methods

► Increase Interconnect Density

1. Fine pitch capability (The current finest pitch capability is **35um** in-line bond pad pitch)
2. Multitier pad designing (a **50um bond pad pitch** device with **4 pad rows** is a common configuration for packages over **1000 I/Os**)
3. Multiple-chip module and System in Package
4. Vertically stacking semiconductor devices
5. Wire bonded Vertical Interconnects



5. Cross section of assembled FOWLP package with wire bonded Vertical Interconnects

Wire bonding methods

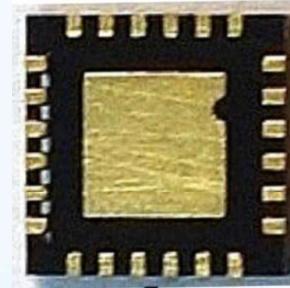
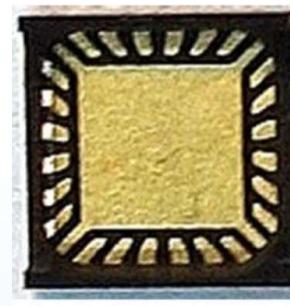
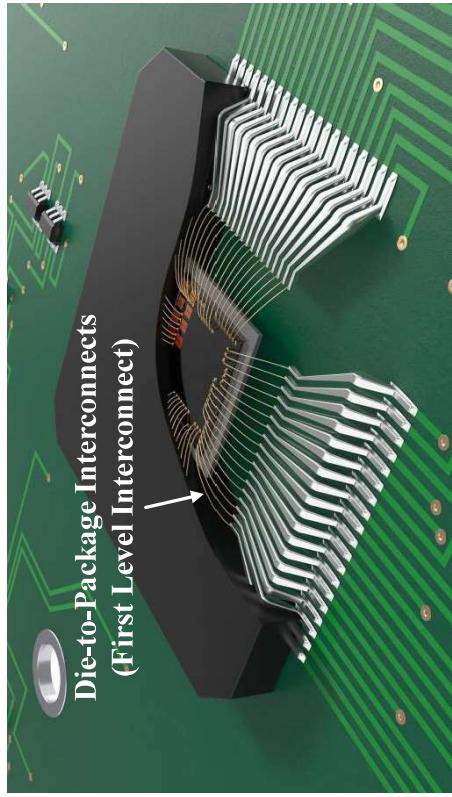
➤ Improved process monitor, real time control, and defect and factory management

A new generation of smart bonding and looping processes have been developed in response to the new challenges facing the industry including the **transition to Cu wire bonding**, and the increasing need for **real-time monitoring** and closed-loop control.

The **autonomous wire bonder** is a real driver for advanced wire bonding technologies in the next five years.

Wire bonding as first-level interconnection

- The quad flat pack nonlead (QFN) With a plastic molding compound package has been widely used for RF ICs owing to its **simple** and **low parasitic design**.
- Conventionally, **wire bonding** has been the most popular **first-level interconnection** choice.
- Wire bonding is mostly ineffective at frequencies **above 20 GHz**, owing to the impedance mismatch from the **self-inductance** of the bonding wires and the **shunt capacitance** from the pads and molding.

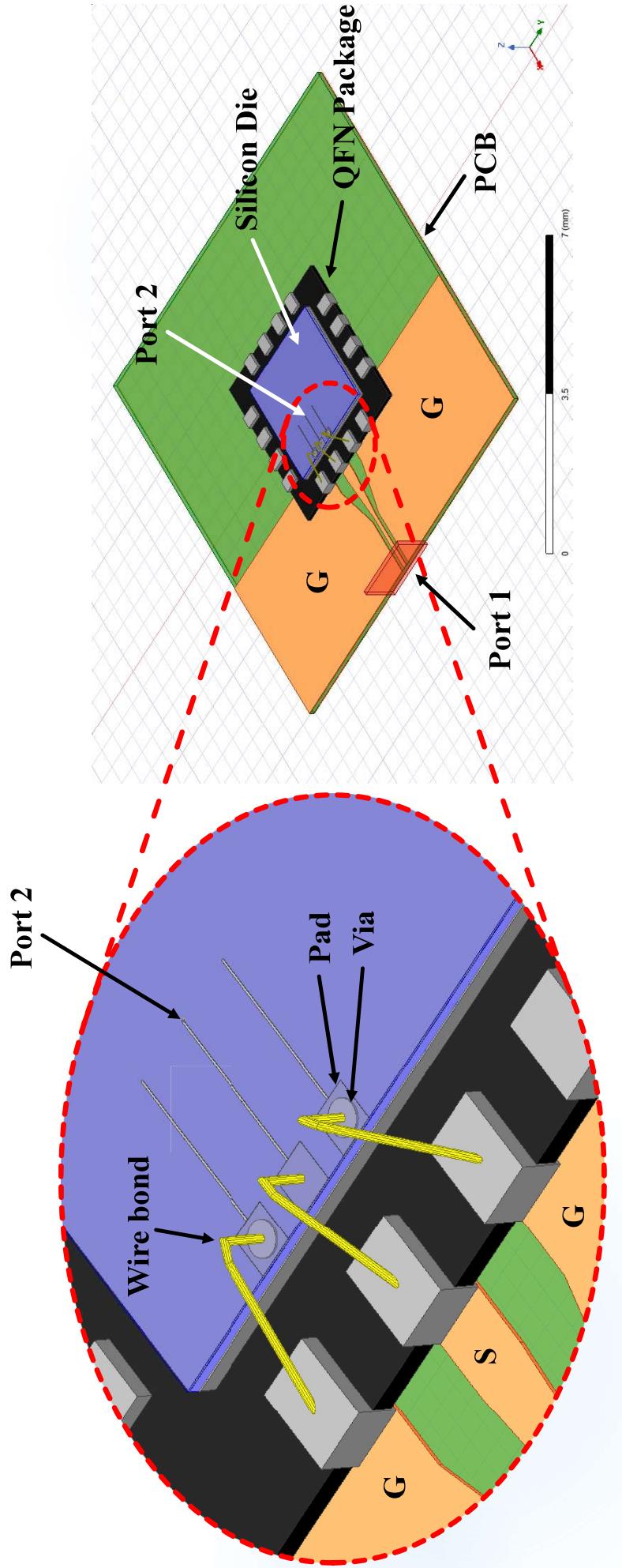


(a) (b)

QFN package structure. (a) Bottom view. (b) Top view
before encapsulation.

Simulation of Wire Bond Interconnect Detail of Simulation Structure

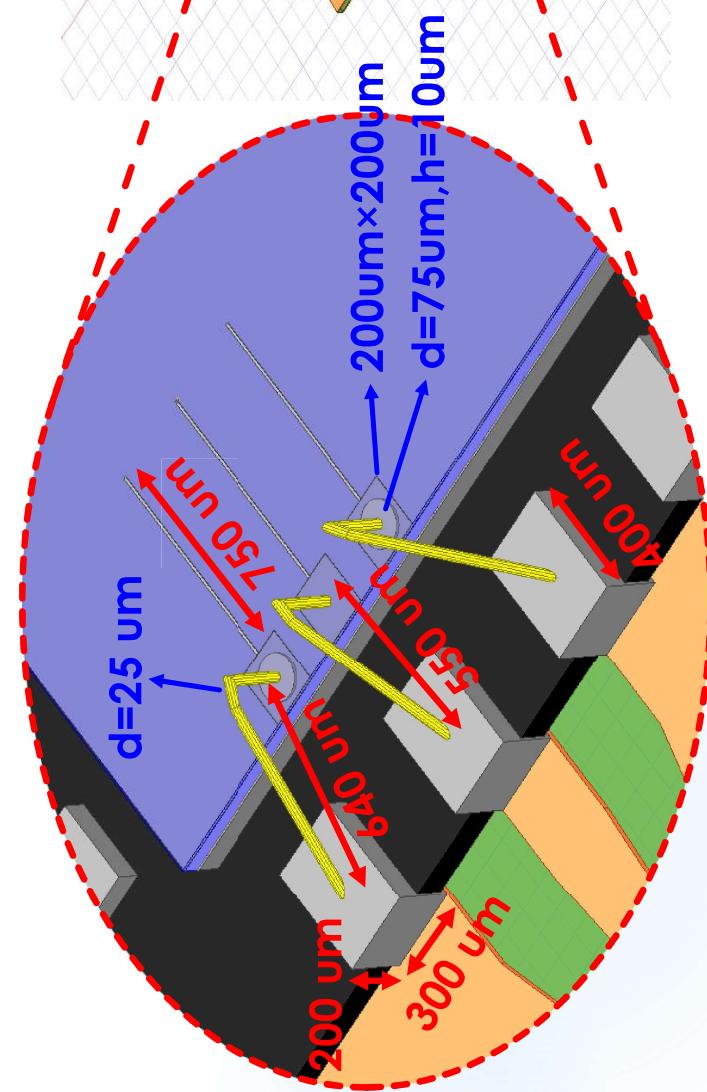
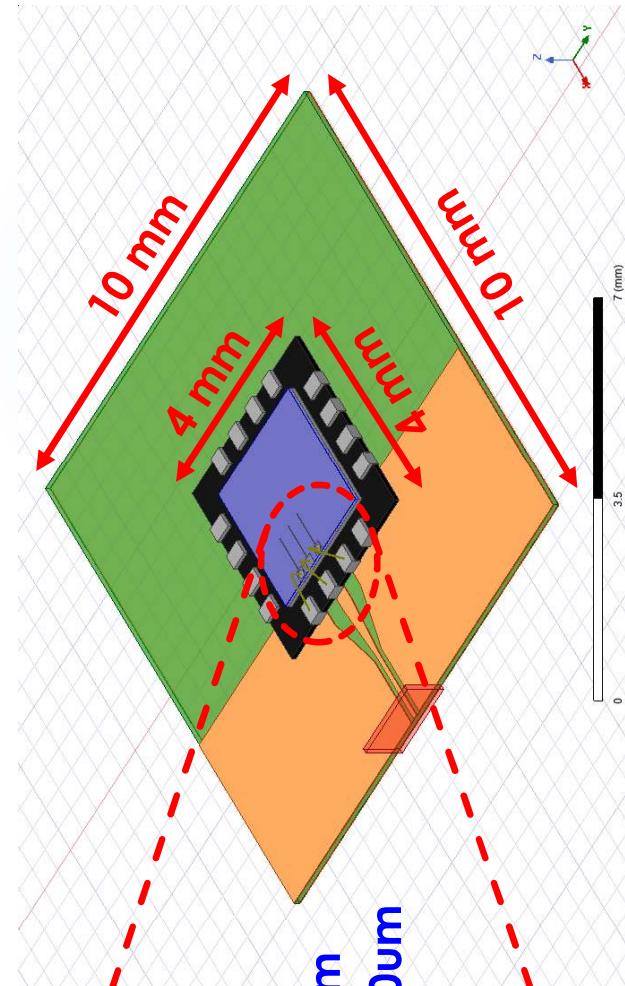
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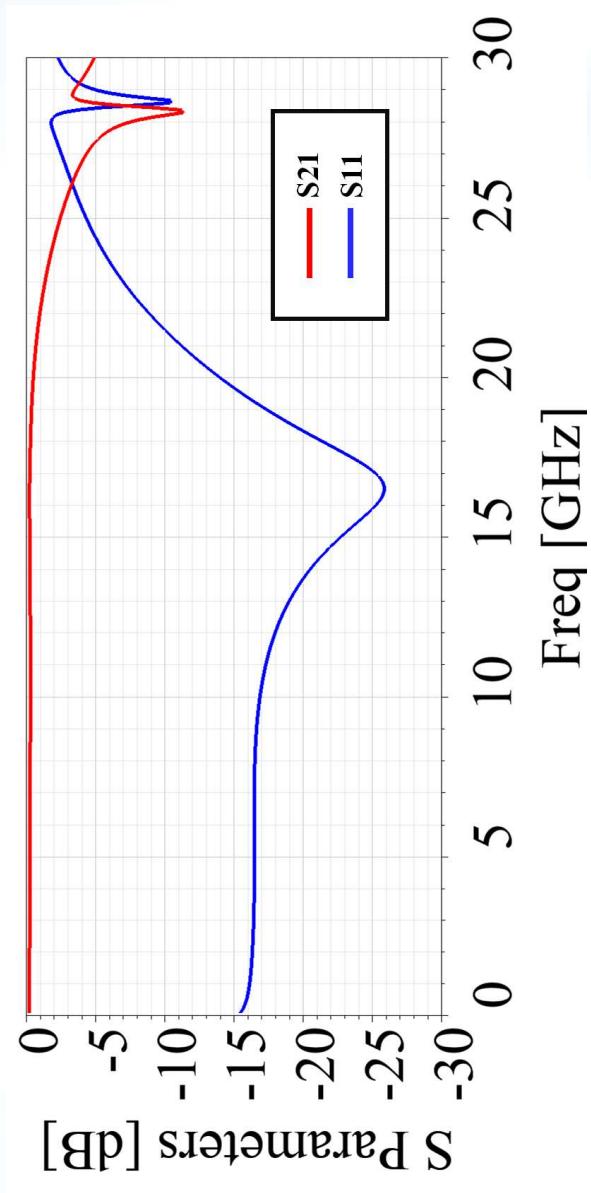
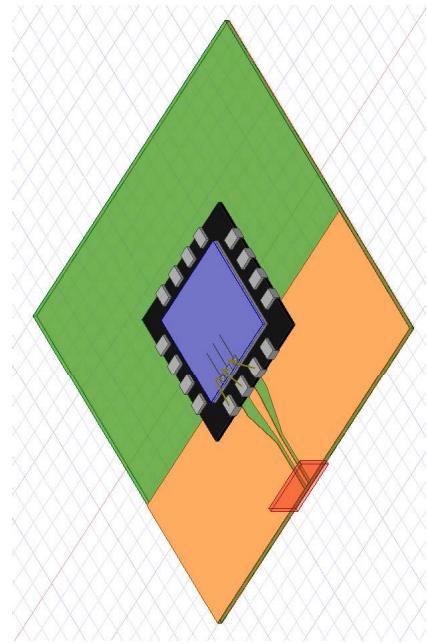
Simulation of Wire Bond Interconnect

Detail of Simulation Structure

47



Simulation of Wire Bond Interconnect Scattering Parameters



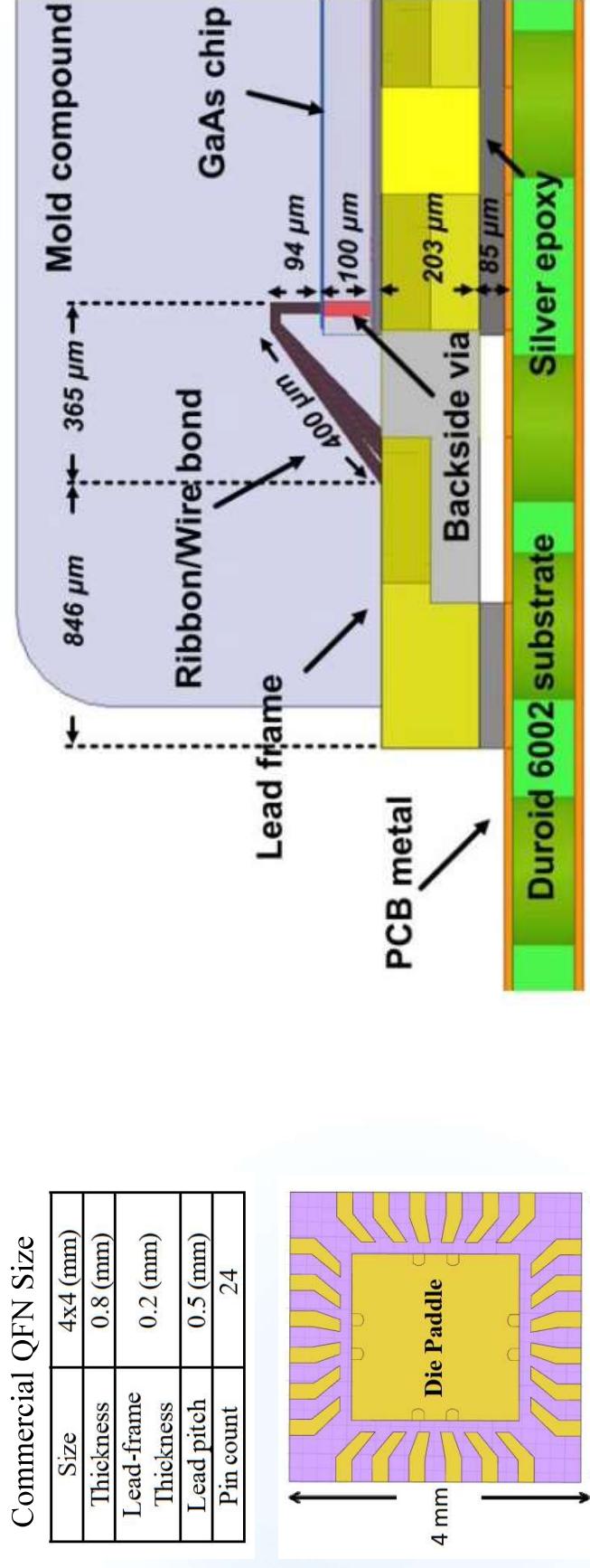
Wire bonding in QFN package

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- Full chip-package-board co-design of bonding transition for a QFN package was conducted from 0.1 to **66 GHz**.

Commercial QFN Size

Size	4x4 (mm)
Thickness	0.8 (mm)
Lead-frame Thickness	0.2 (mm)
Lead pitch	0.5 (mm)
Pin count	24



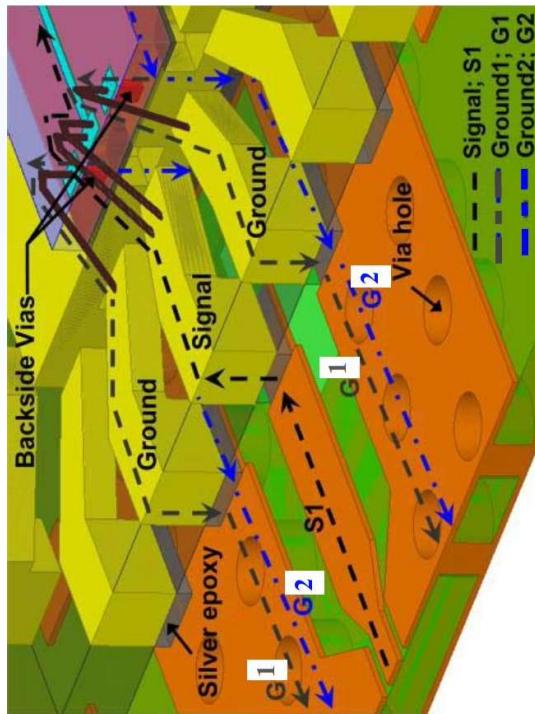
commercial 24-pin QFN package top view

Full Chip-Package-Board Co-design of Broadband QFN Bonding Transition Using Backside via and Defected Ground Structure, 2014.

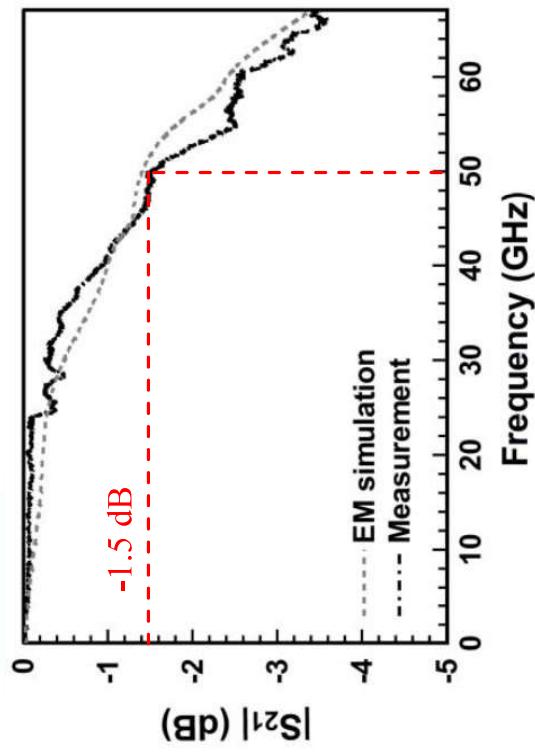
Side view of the QFN package structure after encapsulation

Wire bonding in QFN package

- First two ground paths in parallel were used to improve the operating frequency of the commercially available QFN to 50 GHz by minimizing the signal inductance at the IC-to-package interface.



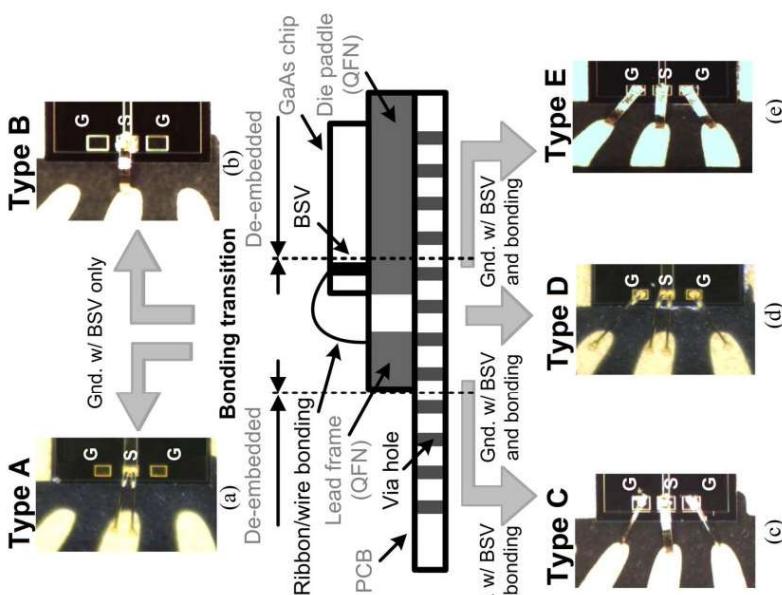
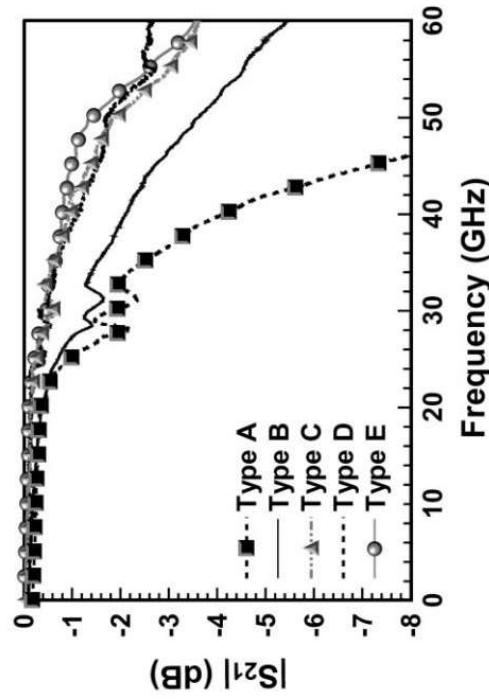
The EM simulated and measured insertion loss of the QFN transition employing the dual ground paths design



Signal and ground flow between the PCB and GaAs chip through the coplanar wire bond interconnect

Wire bonding in QFN package

- Types A and B clearly reveal the reduction of insertion loss by the ribbon.
- A comparison of Types B and C clearly reveals the effectiveness of the dual ground path.
- The afore-mentioned benefits of the ribbon can be obtained by comparing Type C, Types D and E.



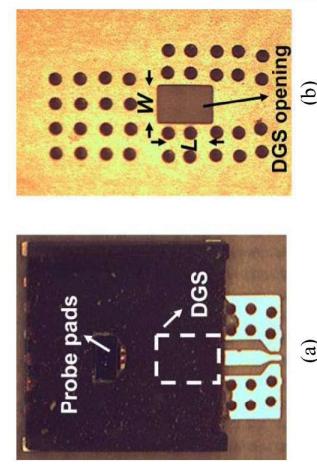
Photographs of five different types of bonding. (a) Type A: two round wires in parallel on the signal pad. (b) Type B: single ribbon bond on the signal pad. (c) Type C: a round wire on each ground pad and a gold ribbon bond on the signal pad (ribbon length = 465 μm). (d) Type D: a round wire on each ground pad, two round wires in parallel on the signal pad (length = 375 μm). (e) Type E: a ribbon bond on ground and signal pads (length = 465 μm). All ribbon and round wires were made of Au.

	Type A	Type B	Type C	Type D	Type E
*BW S ₁₁ (GHz)	31.1	37.1	49.8	50	53
*BW S ₂₁ (GHz)	27.3	35	50.1	50.3	51.8

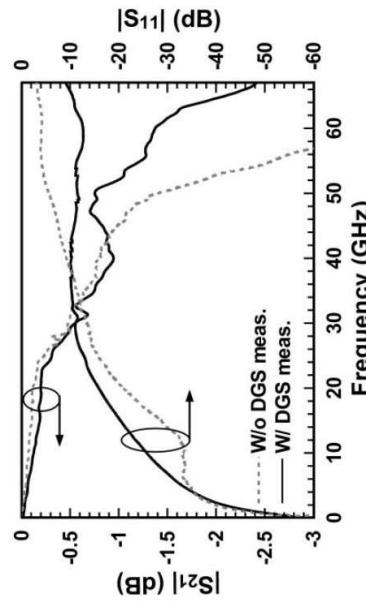
* Criteria used: $|S_{11}| = -10 \text{ dB}$ for BW|S₁₁|; $|S_{21}| = -1.5 \text{ dB}$ for BW|S₂₁|. Unit: GHz

Wire bonding in QFN package

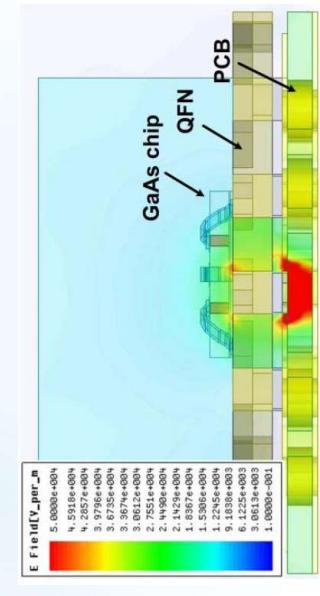
► Second, A high impedance DGS, being inductive itself, was used to compensate for the capacitive nature of the transition at 50GHz.



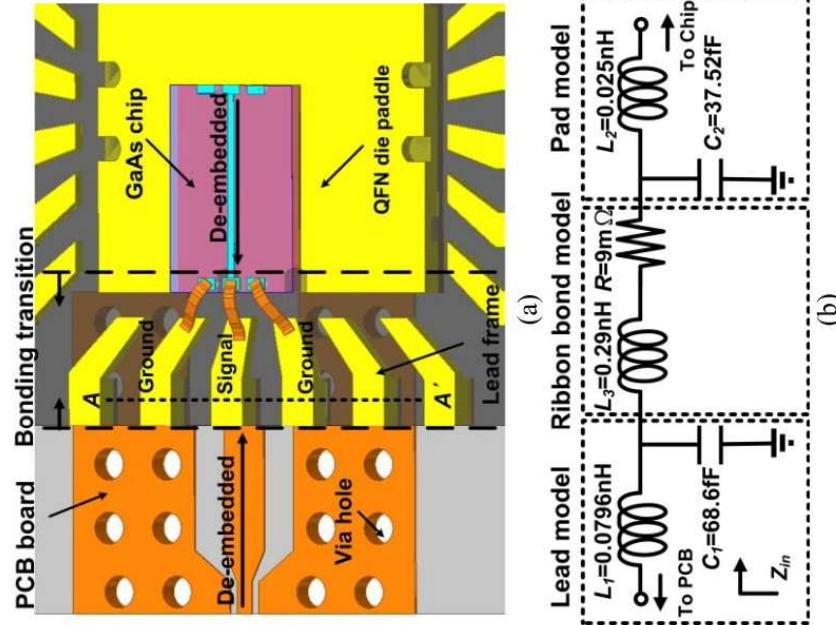
(a) Top view of the QFN package on board and with DGS. (b) Bottom view shows the DGS.



Comparison of measured and simulated results of transitions with and without the DGS



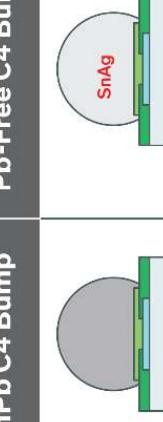
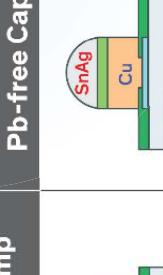
(a) Electric field magnitudes along $A-A'$ for Fig. 9(a) at 50 GHz. (a) Without a DGS. (b) With a DGS.



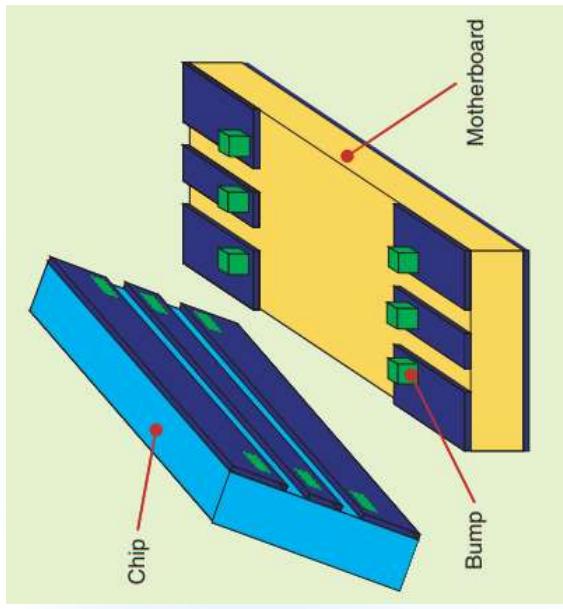
Chip-to-package-to-board illustration. (a) QFN on board without DGS configuration. (b) Equivalent π model of bonding transition at 50 GHz

Flip chip methods

- Flip-Chip transition has become a promising technique over bond-wire in the microwave and millimeter wave frequency, due to its features of **short** and **stable** electrical interconnection.
- But require strict mechanical constraints in their practical implementation and risk parasitic detuning.

Structure	SnPb C4 Bump	Pb-Free C4 Bump	Cu Pillar + Pb-free Cap	Cu μ -Pillar + Pb-free Cap
				
Diameter	75 – 200 μm	75 – 150 μm	50 – 100 μm	10 – 30 μm

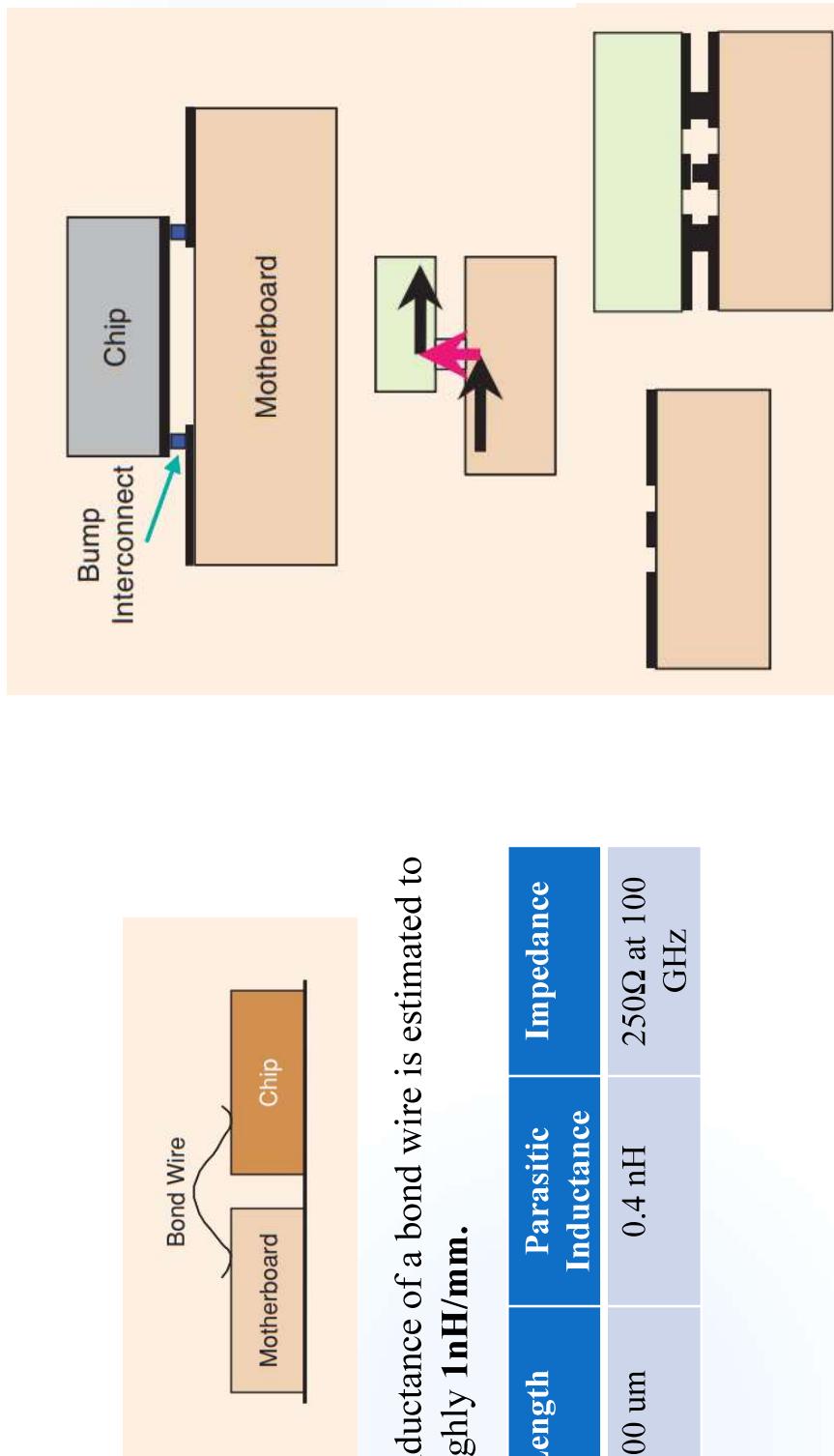
Old Technology Current Technology Next-Generation Technology



Lucy Wei - Marketing Manager, Advanced Packaging Technologies - December 08, 2016

Comparing Flip-Chip and Wire-Bond

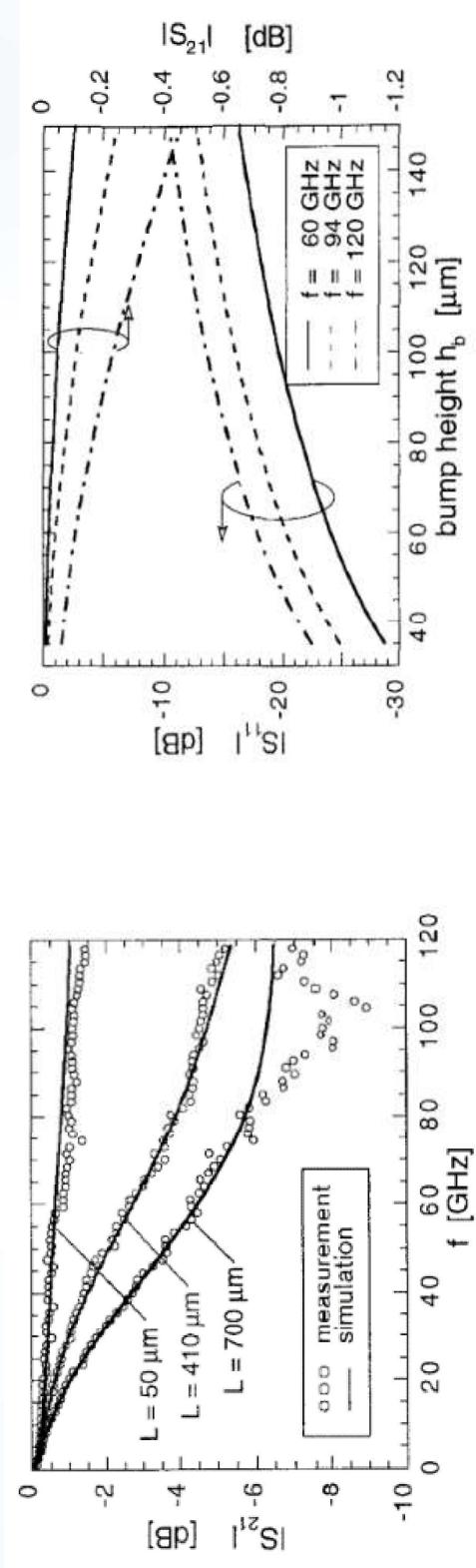
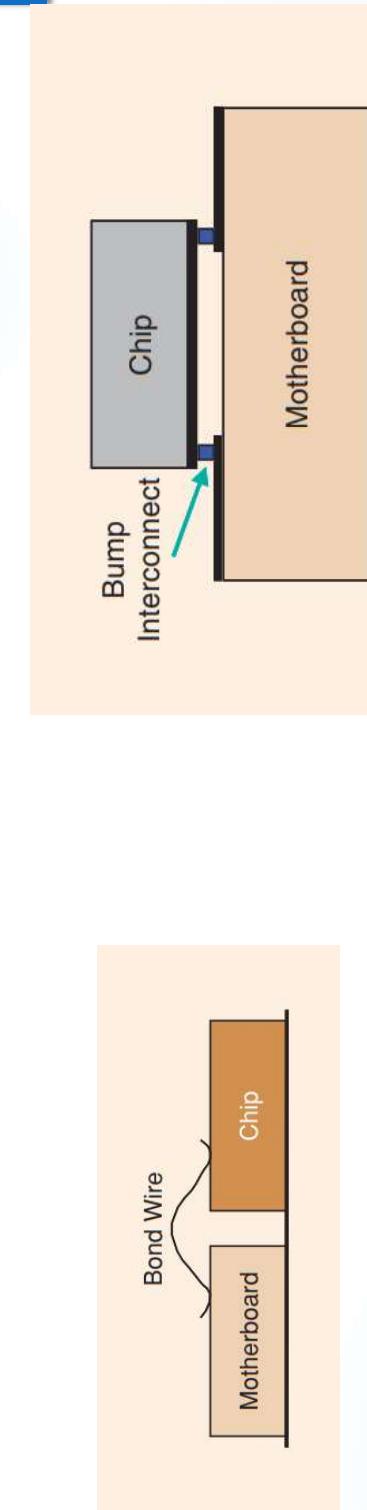
54



The inductance of a bond wire is estimated to be roughly 1nH/mm .

Length	Parasitic Inductance	Impedance
400 um	0.4 nH	250Ω at 100 GHz

Comparing Flip-Chip and Wire-Bond

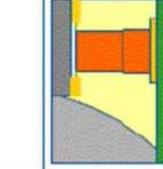
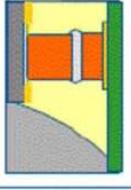
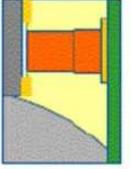
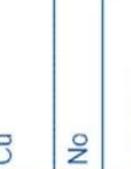


Measured and simulated insertion loss vs frequency for flip chip and bond wire interconnections

“Millimeter-wave performance of chip interconnections using wire bonding and flip chip.” IEEE MTT-S Digest, 1996.

Flip chip types

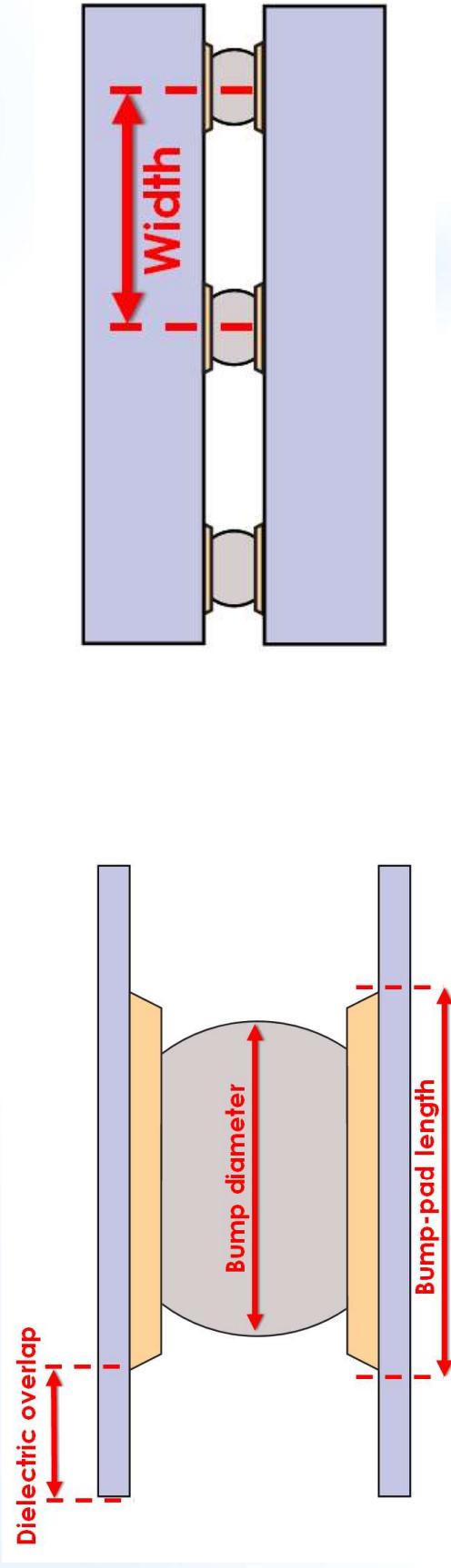
- The interconnect decision will depend on the bump pitch, power, speed/frequency requirements and die size.

Bonding Method	C4 FC (Controlled Collapse Chip Connect)	C2 FC (Chip Connect)	TC/LR (Local Reflow) FC	TC FC
Schematic Diagram				
Major Bump Pitch Range at Application	> 130 um	140 um ~ 60 um	80 um ~ 20 um	< 30 um
Bonding Method	Conventional Reflow	Reflow with Cu pillar	Thermal Compression with Cu pillar	Thermal Compression
Bump Metallurgy	Solder (SnAg or SnAgCu)	Cu + Solder (SnAg or Sn)	Cu + Solder (SnAg or Sn) Cap	Cu
Bump Collapse	Yes	No	No	No
Underfill Method	- Capillary - No flow	- Capillary - No flow - Wafer Level	- No flow - Wafer Level	- No flow - Wafer Level

The main types of flip chip interconnects

Flip chip methods considerations

- As frequency goes higher, the parasitic effects of the flip-chip transition may result in performance degradation.
- There are **some main issues** that determine the **reflection** at the bump interconnect:
 - Bump diameter
 - Bump-pad area (length and width)
 - Dielectric overlap between chip and motherboard
 - **Total width of the transition** (determined by the distance between signal and ground bump)



Flip chip methods considerations

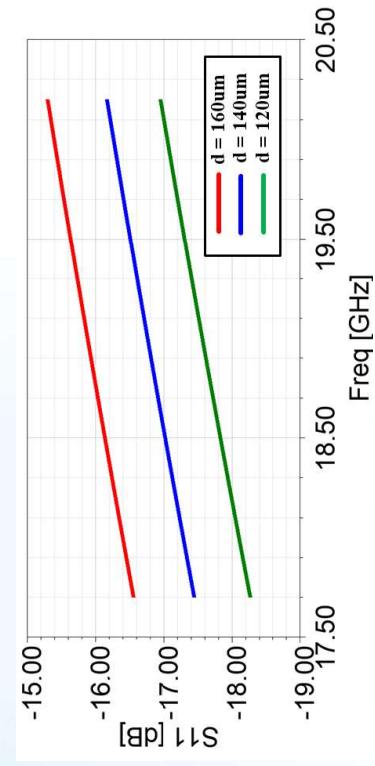
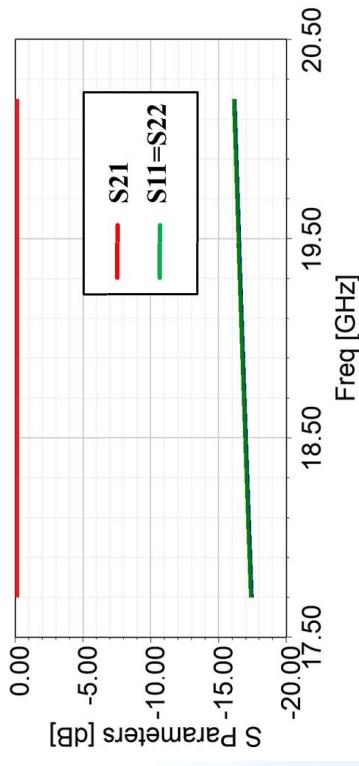
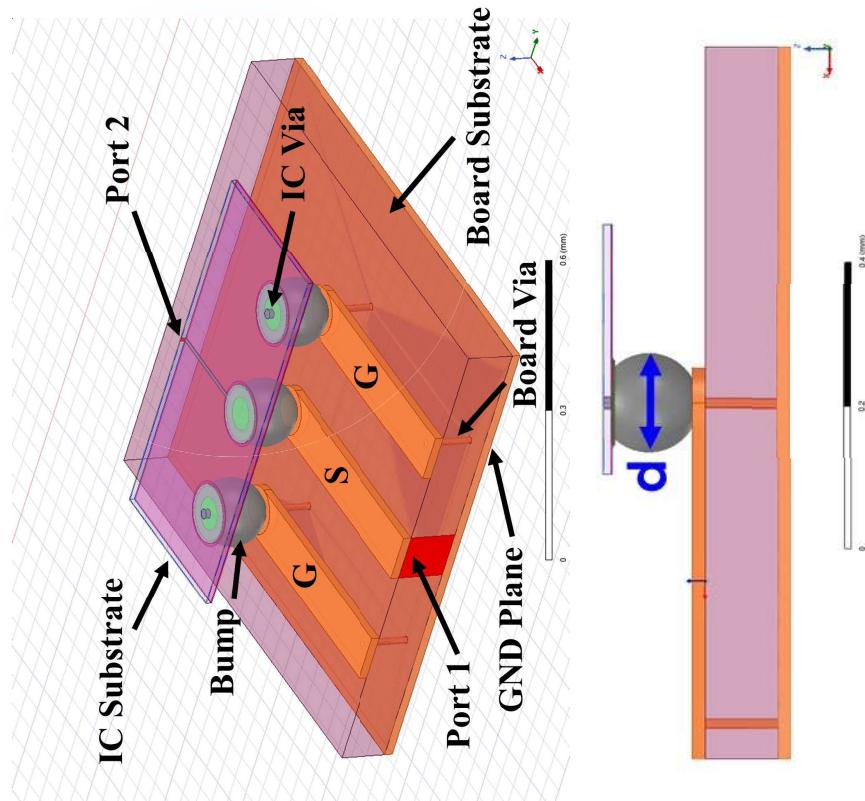
Effect of bump interconnect parameters on reflection:

	Size Variation	Reflection	Consideration
Bump diameter *	10um reduction (35 to 25 um)	less than 1 dB reduction (at 70GHz)	Use small-diameter bumps and keep the pad as small as possible.
Bump pad-length in propagation direction	10um reduction (60 to 50 um)	~ 1 dB reduction (at 70GHz)	In practice, overlap dimensions below 50um are unrealistic.
Dielectric overlap of chip and motherboard	50um enlargement (0 to 50um)	~ 2 dB enlargement (at 70GHz)	
Total width of the transition (The distance between signal and ground bumps (center–center))	70um enlargement (100 to 170um)	~ 2 dB reduction (at 70GHz)	The return loss can be further improved to a certain extent by choosing a larger distance between signal and ground bumps.

* Bump height was found to be of minor importance for reflections.

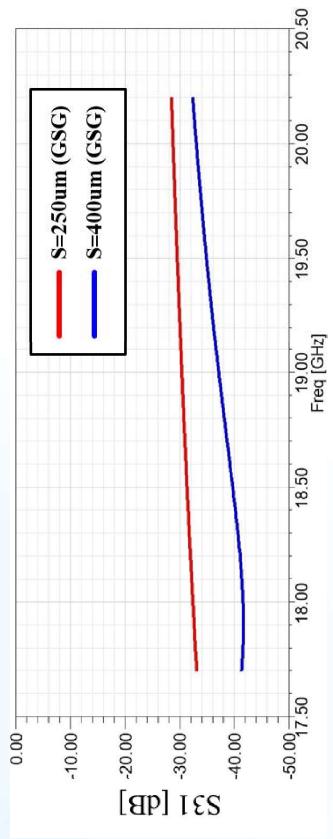
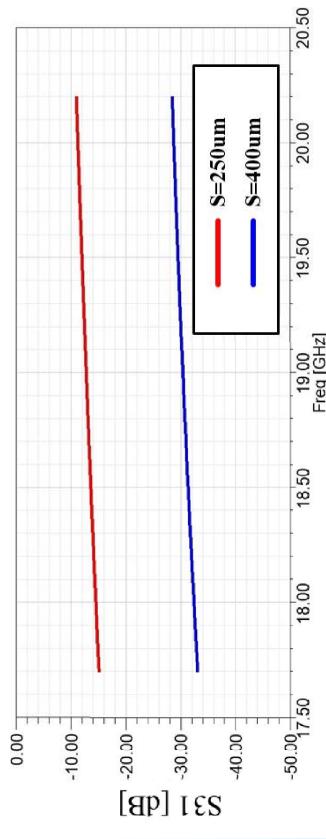
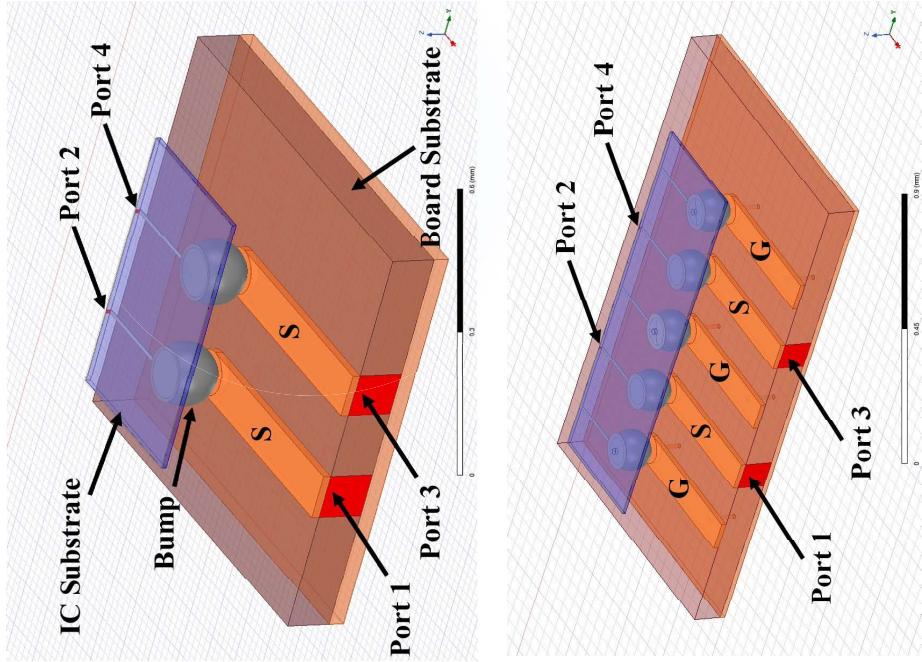
Simulation of Flip-Chip Structure

- Simulation results of insertion loss and return loss for K-band (17.7 – 20.2 GHz) are shown.



Simulation of Flip-Chip Structure

- Simulation results of crosstalk for K-band (17.7 – 20.2 GHz) are shown.



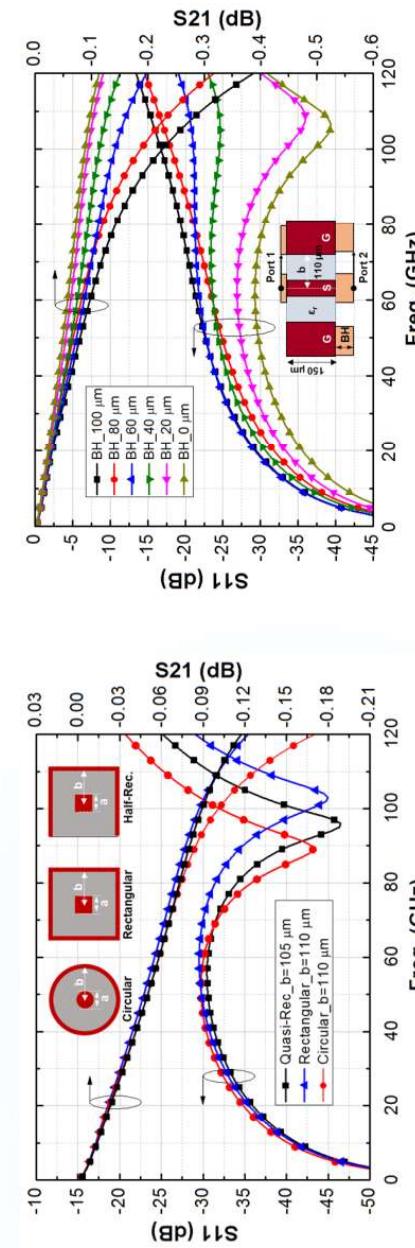
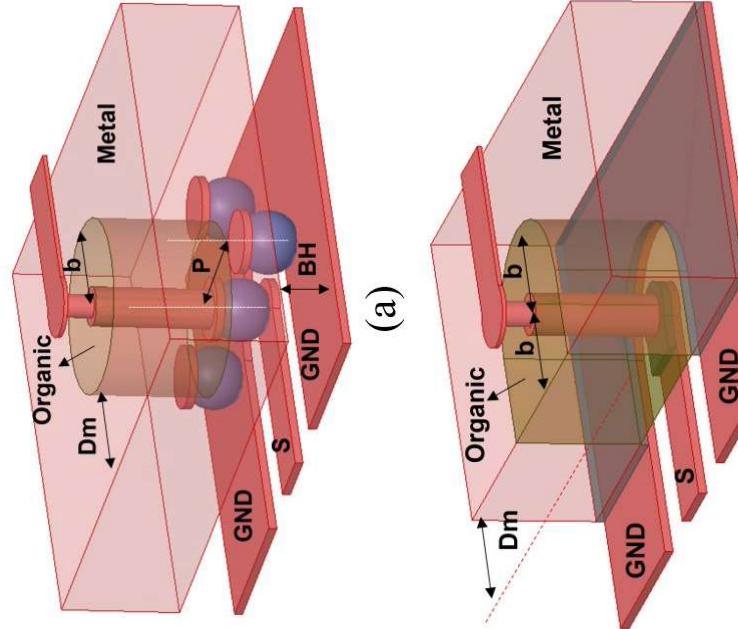
Results of Simulation

Frequency Band	S Parameters	
	S21	S11
17.7-20.2 GHz	~ - 0.2 dB	~ - 20 dB
27.5-30 GHz	~ - 0.3 dB	~ - 15 dB

Variable	Variation	Effect
Bump Diameter	20 μm reduction	Reflection improvement around 1 dB
Bump pitch	$\pm 10\mu m$	Bump pitch was found to be of minor importance for reflections
Pad Geometry	GGGSG SS	Isolation improvement around 20 dB -

Flip chip methods

- A **quasi-coaxial through-silicon-via** (TSV) is presented for millimeter-wave integrated circuit (IC) packaging.
- The quasi-coaxial-via (Q-COV) structure in which one side ground metal is removed can **minimize the interconnect length** when it is mounted, in comparison to the coaxial-via (COV) structure.



EM simulation results of vias. (a) S-parameters of the circular coaxial, rectangular and rectangular quasi-coaxial vias. (b) S-parameters for various bump heights of the circular COV, as shown in Fig. 1(a) ($a = 50 \mu\text{m}$, $b = 110 \mu\text{m}$, $p = b + a/2$, $\epsilon_r = 3.4$).

► Vertical signal transition. (a) COV. (b) Q-COV.

(2019)

“Ultrawideband Signal Transition Using Quasi-Coaxial Through-Silicon-Via (TSV) for mm-Wave IC Packaging,” IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS, 2019.

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- [2] Yongrong Shi, Dengyun Shao, Wenjie Feng, Junzhi Zhang and Ming Zhou, “Silicon Interposer Package for MMIC Heterogeneous Integration Based on Gold/Solder Ball Flip-Chip Technique,” Transactions on Components, Packaging and Manufacturing Technology, 2019.
- [3] Akanksha Bhutani, Benjamin Gottel, Andreas Lipp and Thomas Zwick, ‘Packaging Solution based on Low Temperature Co-fired Ceramic Technology for Frequencies Beyond 100 GHz’, IEEE Transactions on Components, Packaging and Manufacturing Technology, 2018.
- [4] Michael Thomas Craton and Premjeet Chahal, “A Chip-First Approach to Millimeter-Wave Circuit Packaging,” IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS, 2019.
- [5] Jong-Min Yook, Young-Gon Kim, Wansik Kim, Sosu Kim and Jun Chul Kim, “Ultrawideband Signal Transition Using Quasi-Coaxial Through-Silicon-Via (TSV) for mm-Wave IC Packaging,” IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS, 2019.
- [6] Andrea Jentzsch and Wolfgang Heimrich, “Theory and Measurements of Flip-Chip Interconnects for Frequencies up to 100 GHz,” IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, VOL. 49, NO. 5. 2001.

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- [7] T. Krems, W. Haydl, H. Massler and J. Rudiger, “Millimeter-wave performance of chip interconnections using wire bonding and flip chip,” IEEE MTT-S Digest, 1996.
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- [9] Yi-Chieh Lin, Wen-Hsian Lee, Tzyy-Sheng Horng and Lih-Tyng Hwang, “Full Chip-Package-Board Co-design of Broadband QFN Bonding Transition Using Backside via and Defected Ground Structure,” IEEE TRANSACTIONS ON COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY, VOL. 4, NO. 9, 2014.
- [10] To-Po Wang and You-Fu Lu, “Fast and Accurate Frequency-Dependent Behavioral Model of Bonding Wires,” IEEE Transactions on Industrial Informatics, 2017.

thank you