



Milad Seyedi

ELECTRONIC RESEARCHER

OBJECTIVE

My career objective is to engage in impactful research within the electronic engineering domain, particularly focusing on enhancing de-embedding techniques to improve signal integrity. My deep interest in this field, fostered during my master's research, drives my passion for precision and reliability. Concurrently, I aspire to contribute to the advancement of high-speed serial links, IC packaging, and measurement techniques. Collaborative research projects offer a platform to push boundaries and expand scientific knowledge, with the ultimate goal of benefiting the industry and society through contributions that drive technological progress.

CONTACT

PHONE:

+989189805650

WEBSITE:

Website goes here

EMAIL:

miladseyedi994@gmail.com

SIKILLS

Hardware Des. Language	Proficient	Verilog
	Intermediate	VHDL
Software	Altium Designer, ADS, HFSS, ISE Design Suite, HSPICE, PSPICE, ISE Design Suite, Panda, IDLE Python, STM Studio, AVR Code vision, Microsoft Office	
Programming Language	Proficient	Python, MATLAB, C
	Intermediate	C++, Linux
Language	Kurdish	Native
	Farsi	Native
	English	Proficient

EDUCATION

University of Tehran (UT) 2020/9 – 2023/4

- M.SC. IN ELECTRICAL ENGINEERING (ELECTRONIC)
- GPA: 17.05/20.00
- Thesis: Analysis of Interconnects' De-embedding Methods and Developing Synthesized Time-Domain Response Based L-2L De-embedding for Distributed Circuits Applications
- Supervisors: Professor Nasser Masoumi & Dr. Samad Sheikhaei

Urmia University 2013/9 – 2017/8

- B.SC. IN ELECTRICAL ENGINEERING (ELECTRONIC)
- GPA: 16.36/20.00
- Thesis: Design and Implementation of a Gesture-Controlled Device Using Image Processing and Embedded Hardware- score 20/20
- Supervisors: Dr. Morteza Mousazadeh

INTERESTED AREA

- High Speed Serial Links
- De- embedding/Calibration Techniques
- IC Packaging
- Signal Integrity

PUBLICATION

Journal Papers

- **M. Seyedi**, **N. Masoumi**, and **S. Sheikhaei** (2023), Investigating Test Structure Dimensions Impact on De-Embedding method Accuracy for On-Wafer Transmission Lines, under progresses
- **M. Seyedi**, **N. Masoumi**, P. Namaki (2023), and **S. Sheikhaei**, [2X-Thru De-Embedding Method Using Time Domain Impedance Response for S-Parameter Characterization of DUT in Broadband PCB](#), Ready to submit
- Pouya Namaki, **Nasser Masoumi**, **Milad Seyedi**, and **Mohammad-Reza Nezhad Ahmadi** (2023), [An Extended L-2L De-embedding Method for Modeling and Low Return-Loss Transition of Millimeter Wave Signal Through Silicon Interposer](#), Submitted on IEEE Transactions on EMC.

Conference Papers

- **Milad Seyedi**, **Nasser Masoumi**, and **Samad Sheikhaei** (2023), [T-Type L-2L De-Embedding Method For On-Wafer T-Model Transmission Line Network](#), Ready to submit

ACADEMIC PROJECTS

M.Sc. Thesis

- Implementation, Modification, and Visualization of Advanced De-Embedding Techniques
 - Developed L-2L methods: on-wafer T-type, on-PCB.
 - Introduced 2x-thru de-embedding via impedance response.
 - Demonstrated coding, advanced analysis, signal processing skills.
 - Designed software for method comparison.
 - Implemented, visualized in Python (NumPy, TKinter, Scikit-RF) and MATLAB

B.Sc. Thesis

- Real-Time Hand Detection and Device Control
 - Applied OpenCV for live hand detection.
 - Leveraged Raspberry Pi as core processor.
 - Controlled devices using gestures.
 - Designed embedded hardware for streamlined control.

High Speed Interconnect Course

- Enhanced Signal Integrity At 60Ghz
 - Designed A Flip-Chip Interconnect Topology Using HFSS Ansys Simulator For 60ghz Data Transfer, Optimizing Signal Integrity Through Bump-Microstripline-Bump Configuration.

High Speed Serial Link Course

- FIR 4-PAM Equalization for Transceiver and Receiver
 - Designed FIR-based 4-PAM equalization to expand data transfer range on a specific channel using ADS.

EXPERIENCE

Teacher Assistant

- UT 2020 – 2023
M.Sc. Courses
 - High Speed Interconnect (Two semesters Chief TA)
 - High Speed Serial Link
 - VLSI (Two semesters)
- Urmia University 2013 – 2018
B.Sc. Course
 - Electronic Circuit I & II
 - Circuit Theory I & II
 - FPGA-Verilog

Research Assistant

- SOFTWARE DESIGNER, CST-Lab, Tehran University 2021 – 2023
 - Designed a Python-based de-embedding software with 26 methods, surpassing industry standards of 2-3 methods.
 - Culmination of three years' work under Prof. Nasser Masoumi, yielding three papers (2 journal, 1 conference).
 - Demonstrated expertise in de-embedding techniques and software engineering, advancing the field's capabilities.
- RESEARCH COLLABORATOR, [CIARS Lab, University of Waterloo](#) 2021 – 2022
 - Collaborated internationally with Pouya Namaki under [Prof. Mohammad-Reza Nezhad-Ahmadi's](#) supervision.
 - Extended L-2L de-embedding to analyze bump effects on signal integrity in interposer flip-chip technology.
 - Co-authored a research paper, titled "[An Extended L-2L De-embedding Method for Modeling and Low Return-Loss Transition of Millimeter Wave Signal Through Silicon Interposer](#)", which was published in [IEEE Transactions on EMC](#), showcasing the findings and contributions of the research.
- TEST ENGINEER – [DBS project to Cure Parkinson's Disease Project](#) 2020 – 2021
ACSDC Lab, Tehran University
 - Integral part of a team led by Profs. Omid Shoaee, Samad Sheikhaei, and Shahin Jafarabadi Ashtiani.
 - Developed testing platform for new [IC generation](#) aimed at Parkinson's disease treatment.
 - Designed 9 specialized PCBs, including a central motherboard, to generate and measure electronic signals for diced ICs.
 - Collaborated with Dr. Samad Sheikhaei in ACSDC lab, contributing to innovative advancements.
 - Supported critical project goals by providing essential testing infrastructure.

Work Experience

- THERMOSTAT PCB DESIGNER – Part time 2023
[SEDNA COMPANY](#)
 - Designed PCBs for smart thermostats with IoT platforms at Sedna, a leading player in Iran's thermostat sector.
 - Led design for notable models:
 - [Telesto](#)
 - [Volkan](#)
 - [Selena](#)
 - [All-in-One-Eris](#)
 - **RESEARCH:** Implemented a rigorous standard [CHECKLIST](#) for PCB design and testing, aligned with Sedna's principles.
 - Collaborated across teams, optimizing hardware-software integration to drive technological advancements.
- [TECHNICAL PRODUCT MANAGER](#) - Electronic Board Design – Part time 2022
[SEDNA COMPANY](#)
 - Led design of versatile electronic board for combi boilers.
 - Enabled multiple functionalities through software programming, ensuring hardware compatibility.
 - Aligned design with [CEI EN 60730](#) and [UNI EN 298/2012](#) standards.
 - Collaborated cross-functionally for holistic product development.
 - Extended project to develop electrical boiler product.
- HARDWARE DESIGN ENGINEER – Part time 2015 – 2017
[IMENARA PERSIAN COMPANY](#)
 - Designed dedicated DSP processor PCB tailored for CCVT cameras, to optimize their image processing capabilities.
 - **RESEARCH:** Designed Power over Ethernet (PoE) hardware 12VDC, 24VAC / 28W, streamlining camera installations by transmitting power and data through a single cable.
 - Implemented [IEEE 802.3 at Class2](#) standard to provide efficient PoE functionality.
 - [IAP.NSD-P4537R](#)
 - [IAP.NSD-P4220 WR](#)
 - [IAP.NSD-P4220 WS](#)
 - [IAP.NSD-P3210](#)
 - [IAP.NSD-P4230 WS](#)
 - Spearheaded the development of a IOT test room and instruments, enabling thorough testing of cameras in various corner conditions.
 - Additionally, contributed to the design of car GPS systems, expanding hardware design expertise to diverse technological domains.

HONORS AND ACHIEVEMENTS

2020 - **Ranked 82th**, in the Iranian university entry exam for master students of electronic engineering of participants of the Iranian university entry exam
2017 - **Ranked 4th GPA**, among graduating students of Electronic Engineering major in B.Sc. at Urmia University
2013 - **Ranked within top 1.5%**, of 180000 participants of the Iranian university entry exam
2008 - **Gold Medalist**, International Karate Championship, England
[2007 – 2009] - **Three-time Gold Medalist**, National Karate Championship
[2007 – 2009]- **Member of National Karate Team**

REFERENCES

[Professor Nasser Masoumi](#), Professor, Department of Electrical and Computer Engineering, School of Engineering, UT, Tehran, Iran, NMasoumi@ut.ac.ir, nmasoumi@uwaterloo.ca

[Dr. Samad Sheikhaei](#), Assistant Professor, Department of Electrical and Computer Engineering, School of Engineering, UT, Tehran, Iran, Sheikhaei@ut.ac.ir

[Dr. Morteza Mousazadeh](#), Assistant Professor, Department of Electrical and Computer Engineering, Urmia University, Urmia, Iran, m.mousazadeh@urmia.ac.ir