De-embedding Techniques for Evaluation of Die-Die Interconnect structure on the Interposer Technology

Interconnect Course Project

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28.4.1400

Outline

- Introduction
- Cascade Based De-embedding
  - TRL Method
  - 2X Thru Method
  - 1X Fixture Method
- Lumped Equivalent Circuit Model Based
  - L_iL_j Method
  - Hybrid Method
  - **L-2L Method**
    - Use L-2L method form large line's length (PCB Trace + Bump)
    - Electromagnetic Characteristics of Multiport TSVs Using L-2L De-Embedding Method and Shielding TSVs
- Conclusion

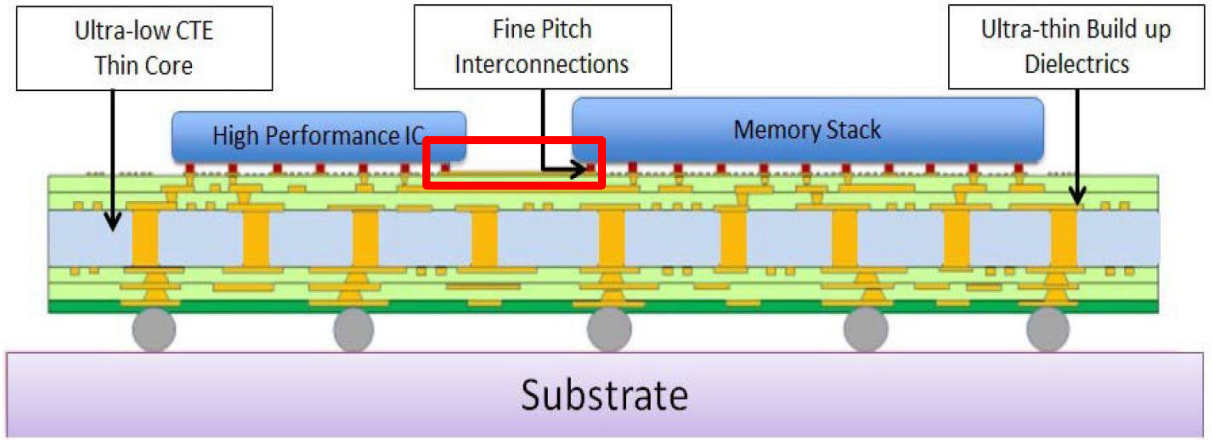
Introduction

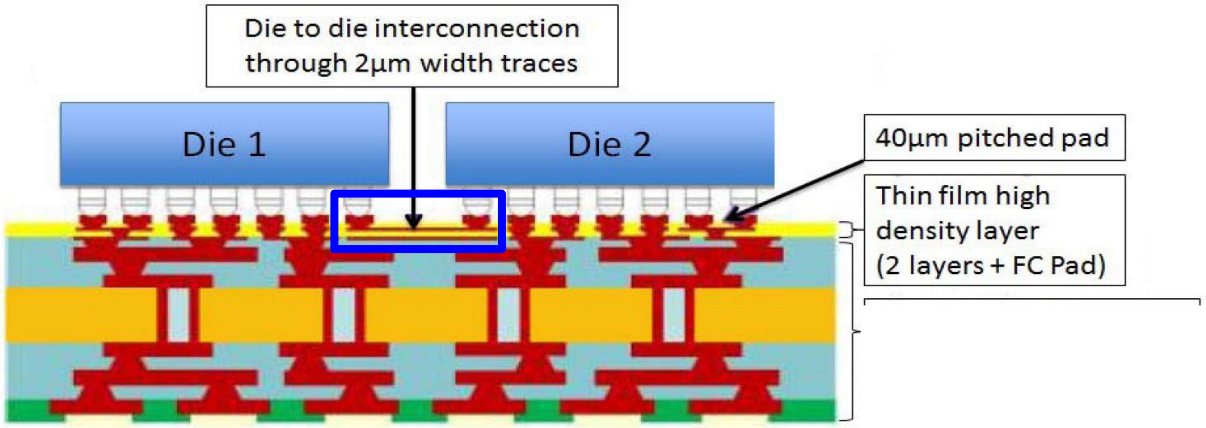
- An "**interposer**" is an electrical interface (substrate) used for routing between one socket or connection to another socket or connection.

- In the search for **low-cost interposer technology, organic is one promising** candidate. It is typically manufactured by the conventional wet etching process.

- The **minimum line and spacing of 2 μm** has been achieved in the **traditional organic** multichip package.

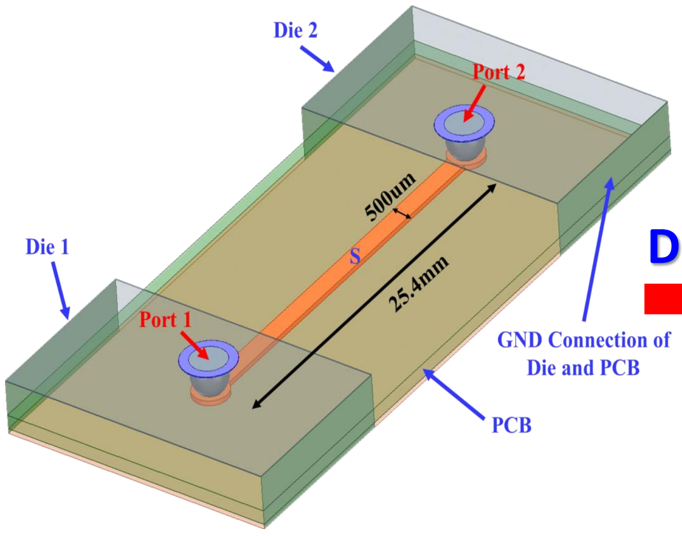
- when a chip is mounted on an organic interposer, either using **wire-bonding** or **flip-chip** technique, the **solder balls** on the package will give some stand-off to the component that will result in **improved reliability.**



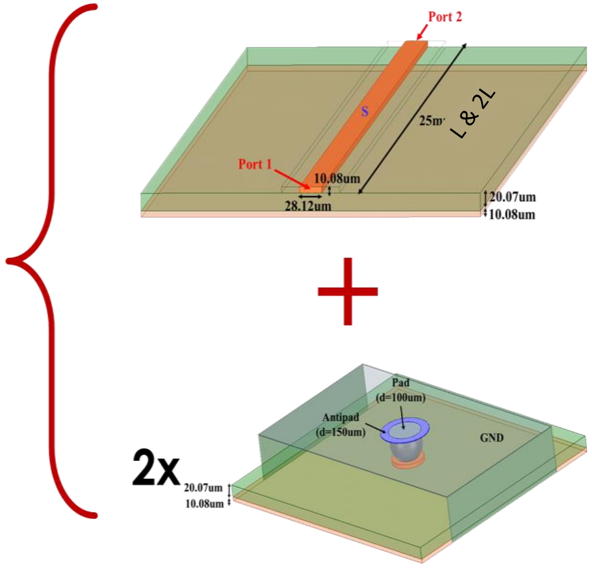


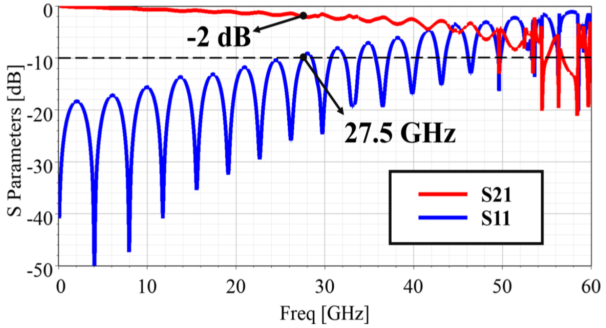
Ref: Interposer Technologies for High-Performance Applications IEEE TRANSACTIONS ON COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY, 2017

De-embedding Technique



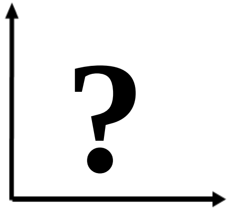
De-embedding



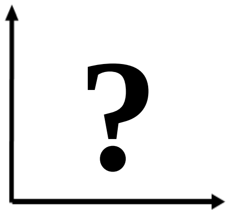


S Parameters of Trace + Bumps

De-embedding



S Parameters of Trace



S Parameters of Bumps

De-embedding Applications:

- Simulation Debugging.
- Fixture's Error Removal.
- Access to inaccessible structures.

Ref: Technical report, 2020 by Pouya Namaki and Nasser Masoumi

Types of De-embedding Methods

The extreme importance of accurate parasitic de-embedding techniques to RF device characterization has already been established. In general, the parasitic contributions of device-under-test (DUT) structures mainly arise from probe pads, the interconnection lines connected to the intrinsic on chip DUT structure. **De-embedding techniques can be classified as two groups:**

- **The first group is called the cascade based technique for large DUT structures:**
  - **TRL**
  - **2X Thru**
  - **1X Fixture**

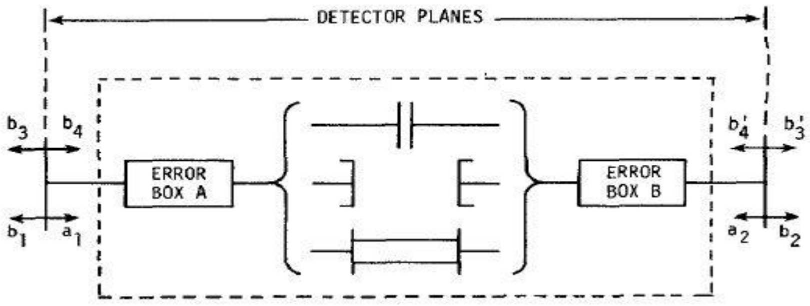
- **The second group is called the lumped equivalent circuit model based technique for short DUT structures:**
  - **L_iL_j**
  - **Hybrid Method**
  - **L-2L**

Ref: H. Cho, "A Novel Transmission-Line De-embedding Technique for RF Device Characterization," in IEEE Transactions on Electron Devices, vol, 2009

Cascade Based De-embedding Methods

- **TRL:** While a minimum of **three measurements** (under different excitation conditions, i.e., values of a_2/a_1) are required in each of the **thru** and **line** connections, only a single measurement is required with the **reflect** connection (for line measuring, the **line** must be **lossless** or **$S_{12} = S_{21}, = 0$**.)

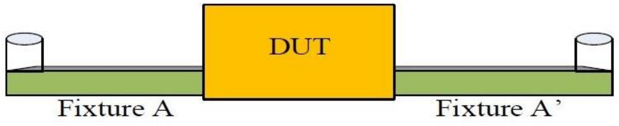
$$T_{DUT} = [T_{Error\ Box\ A}]^{-1} \times [T_{Total}] \times [T_{Error\ Box\ B}]^{-1}$$



Ref: Thru-Reflect-Line: An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer, 1979

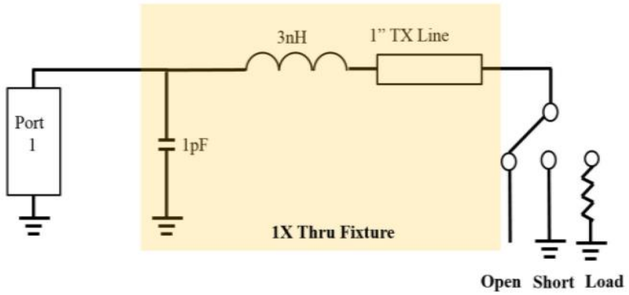
- **2X Thru:** the S11 left and right fixtures are calculated from **the time domain**, while the S21 and S22 fixtures are obtained from the wave peeling algorithm. **only 2X thru pattern is needed.**
  - Symmetry in the 2x Thru is assumed.
  - Minimum spacing between discontinuities in the 2x Thru is needed.

$$T_{DUT} = [T_{Fixture\ \_\ A}]^{-1} \times [T_{Total}] \times [T_{Fixture\ \_\ A'}]^{-1}$$



- **1X Fixture:** This proposed de-embedding method only **requires two calibration patterns** to obtain the DUT S-parameter, as depicted in the Figure. In this design, **1X left and 1X right are not necessarily symmetric**, and are **characterized separately**.

$$T_{DUT} = [T_{Fixture\ \_\ A}]^{-1} \times [T_{Total}] \times [T_{Fixture\ \_\ B}]^{-1}$$



Ref: 2X-Thru, 1X-Reflection, and Thru-Line de-embedding: Theory, sensitivity analysis, and error corrections, 2019

lumped equivalent circuit model based

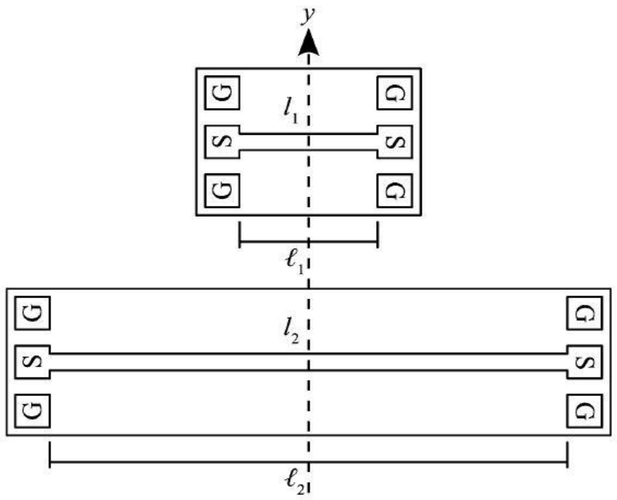
- **L_iL_j:** The L_iL_j de-embedding method also **requires the measurement of two transmission lines**. These transmission lines, however, may be any two different lengths; one transmission line does not have to be double the length of the other. Further, **probing pads are only modeled** as a shunt admittance, **Y=jωC**. Individual pads are still assumed to be symmetric. Using **ABCD parameters**, a transmission line of length i can be represented as the following cascade of ABCD matrices:

$$ABCD_{meas\_Li\&Lj}=ABCD_{LP}ABCD_{Li\&Lj}ABCD_{RP}$$

$$ABCD_{hybrid}=ABCD_{meas\_Lj}ABCD_{meas\_Li}{}^{-1}=ABCD_{LP}ABCD_{Lj-Li}\,ABCD_{LP}{}^{-1}$$

$$Y_{hybrid}=Y_{Lj-Li}+\begin{bmatrix} Y & 0 \\ 0 & -Y \end{bmatrix}=\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}$$

$$Y_{Lj-Li}=\frac{Y_{hybrid}+Swap(Y_{hybrid})}{2}$$



Ref: De-embedding transmission line measurements for accurate modeling of IC designs, (in IEEE Transactions on Electron Devices, 2006)

- **Hybrid Method:** For the proposed hybrid de-embedding method, the measurement of three transmission lines is required. One line is of **length L**, another is of **length 2L**, and the final line is a short line of **length Li**. Similar to the L-2L de-embedding technique, probing pads are modeled with both a shunt admittance and a series impedance. However, the proposed hybrid method switches the order of these lumped parasitic so that the **series impedance is first**. The **shunt admittance then follows the series impedance**, as shown in the Fig.

$$ABCD_{thru}=ABCD_{meas\_}ABCDmeas_{\_2L}{}^{-1}ABCD_{meas\_L}$$

$$=ABCD_{LP}ABCD_{RP}$$

$$ABCD_{2L\ no\ Z}=ABCD_{Z}{}^{-1}\,ABCD_{meas\_2L}\,ABCD_{Z}{}^{-1}$$

$$ABCD_{L\ no\ Z}=ABCD_{Z}{}^{-1}\,ABCD_{meas\_L}\,ABCD_{Z}{}^{-1}$$

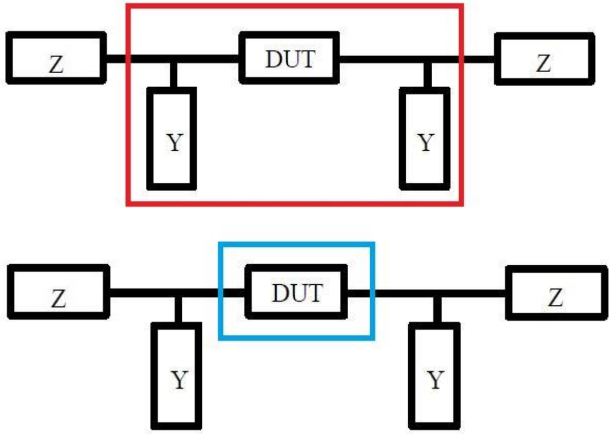
$$ABCD_{Li\ no\ Z}=ABCD_{Z}{}^{-1}\,ABCD_{meas\_Li}\,ABCD_{Z}{}^{-1}$$

$$ABCD_{2L-Li\ (Hybrid)}=ABCD_{2L\ no\ Z}ABCD_{Li\ no\ Z}{}^{-1}$$

$$ABCD_{L-Li\ (Hybrid)}=ABCD_{L\ no\ Z}ABCD_{Li\ no\ Z}{}^{-1}$$

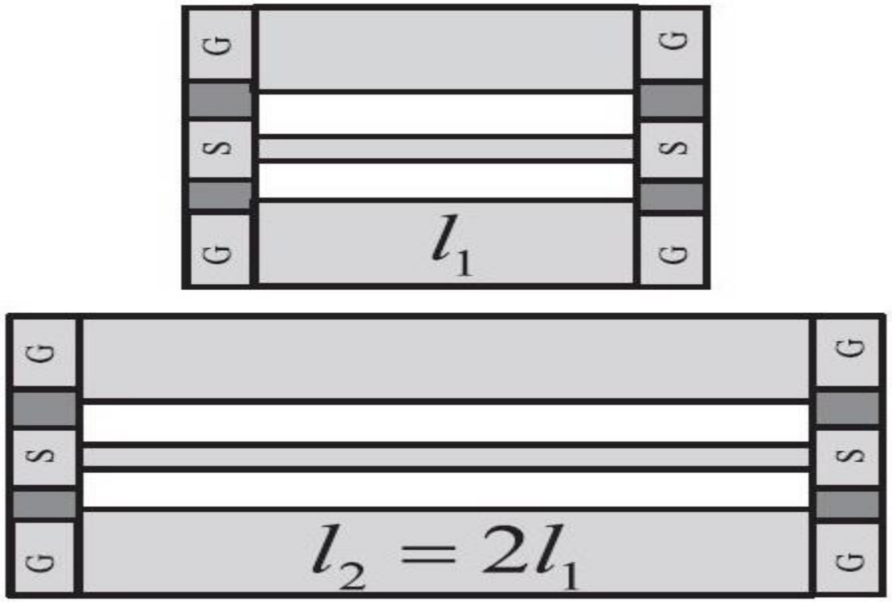
$$Y_{2L-Li}=\frac{Y_{2L-Li\ (Hybrid)}+Swap(Y_{2L-Li\ (Hybrid)})}{2}$$

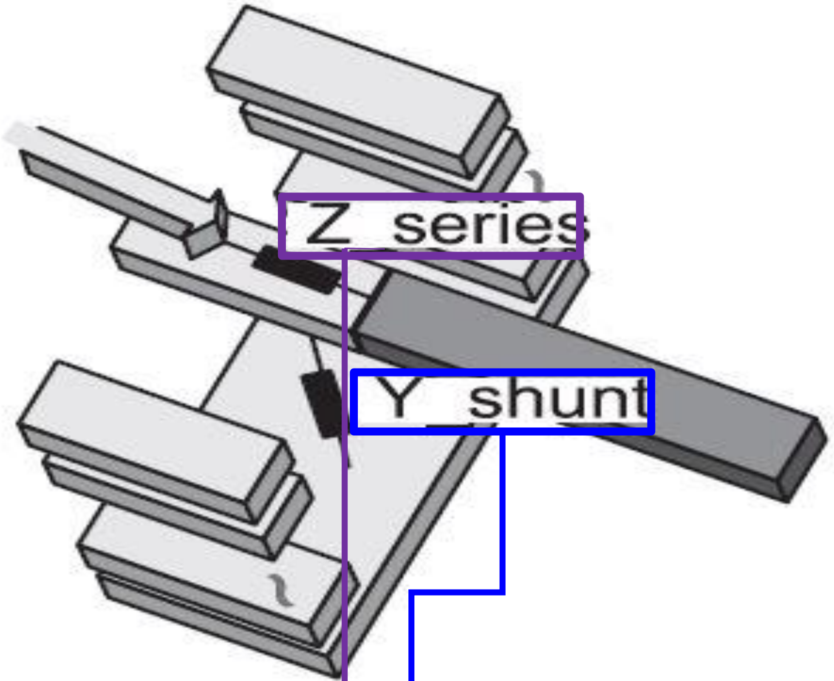
$$Y_{L-Li}=\frac{Y_{L-Li\ (Hybrid)}+Swap(YL_{-Li\ (Hybrid)})}{2}$$



Ref: De-embedding techniques for transmission lines: An exploration, review, and proposal, 2013

L-2L Method (1)





Ref: Evaluation of a Multi-Line De-embedding Technique up to 110GHz for Millimeter-Wave CMOS Circuit Design

$$ABCD_{meas\_L}=ABCD_{LP}ABCD_{L}ABCD_{RP}$$

$$\boxed{ABCD_{LP}}=ABCD_{Y}ABCD_{Z}$$

$$\boxed{ABCD_{RP}}=ABCD_{Z}ABCD_{Y}$$

$$ABCD_{Y}=\begin{bmatrix}1 & 0\\ Y & 1\end{bmatrix} \rightarrow Y=j\omega C$$

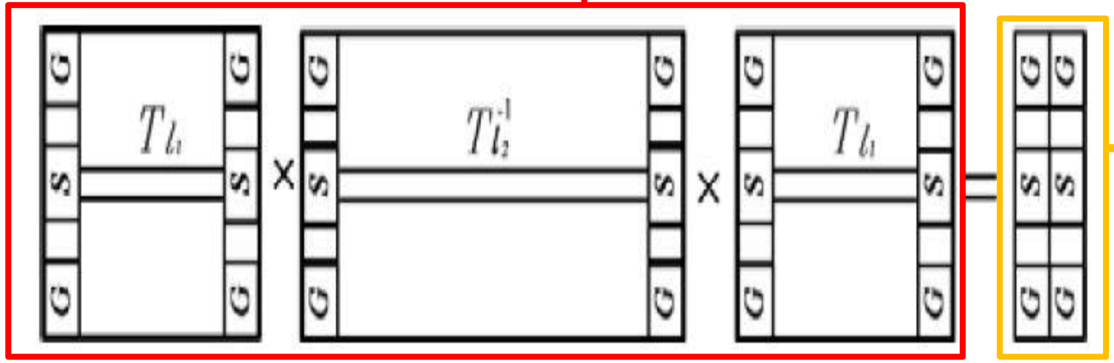
$$ABCD_{Z}=\begin{bmatrix}1 & Z\\ 0 & 1\end{bmatrix} \rightarrow Z=R+j\omega L$$

Where,
$ABCD_{LP}$ *represents the matrix of the left pad;*
$ABCD_{L}$ *represents the matrix of the txline of length L;*
$ABCD_{RP}$ *represents the matrix of the right pad.*

Where,
$ABCD_{Y}$ *represents the shunt admittance;*
$ABCD_{Z}$ *represents the series impedance.*

Ref: De-embedding techniques for transmission lines: An exploration, review, and proposal, 2013

L-2L Method (2)

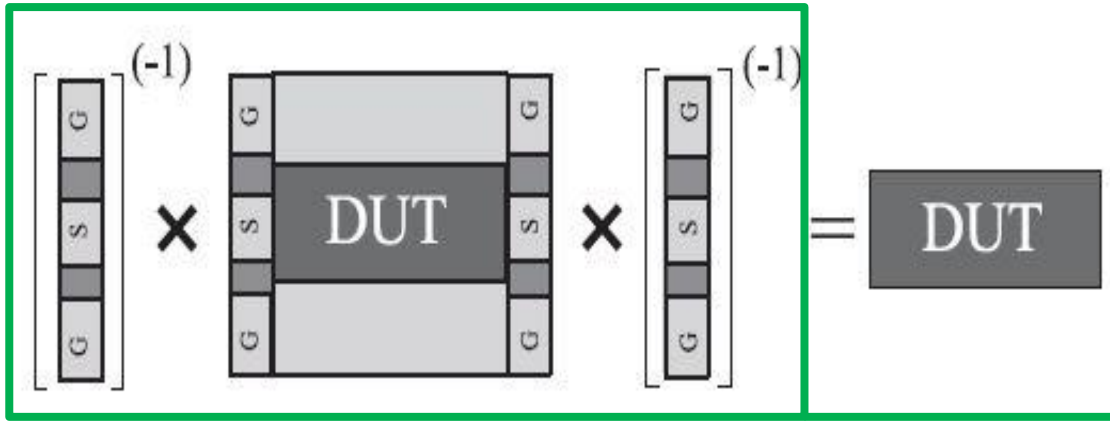


$$ABCD_{thru} = ABCD_{meas\_L} ABCD^{-1}_{meas\_2L} ABCD_{meas\_L}$$
$$= ABCD_{LP} ABCD_{RP}$$
$$= \begin{pmatrix} 2Y_{\text{shunt}}Z_{\text{series}}+1 & 2Z_{\text{series}} \\ 2Y_{\text{shunt}}(Y_{\text{shunt}}Z_{\text{series}}+1) & 2Y_{\text{shunt}}Z_{\text{series}}+1 \end{pmatrix}$$

Ref: Evaluation of a Multi-line De-embedding Technique for Millimeter-Wave CMOS Circuit Design_ Proceeding of Asia-Pacific Microwave Conference

$$\boxed{\begin{aligned} ABCD_{LP} &= ABCD_Y ABCD_Z \\ ABCD_{RP} &= ABCD_Z ABCD_Y \end{aligned}}$$

$$ABCD_Y = \begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix}$$
$$ABCD_Z = \begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix}$$



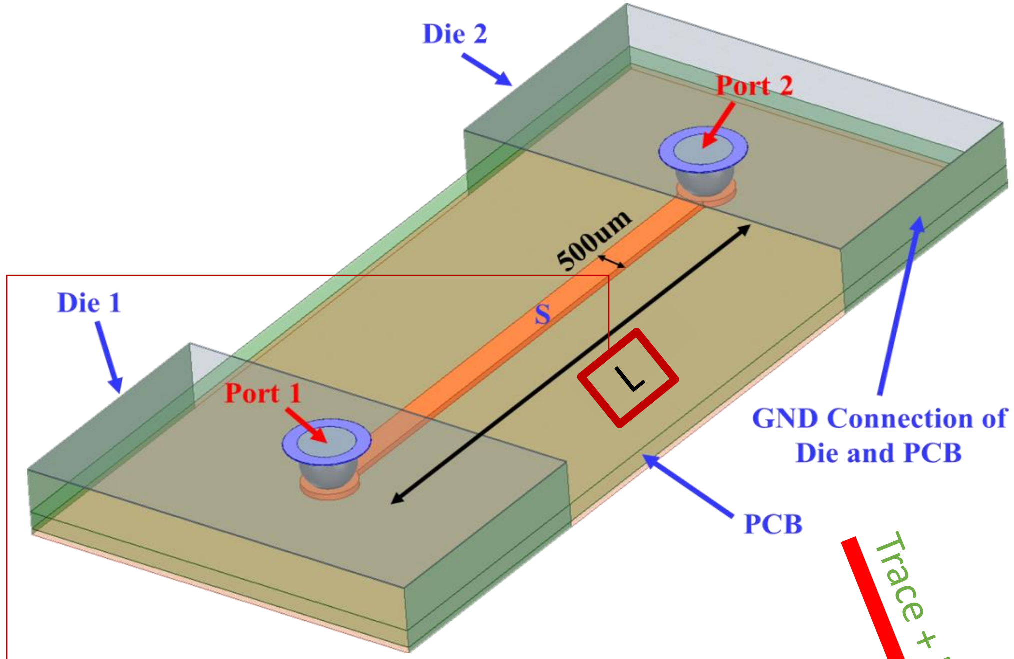
$$ABCD_{meas\_L} = ABCD_{LP} ABCD_L ABCD_{RP}$$

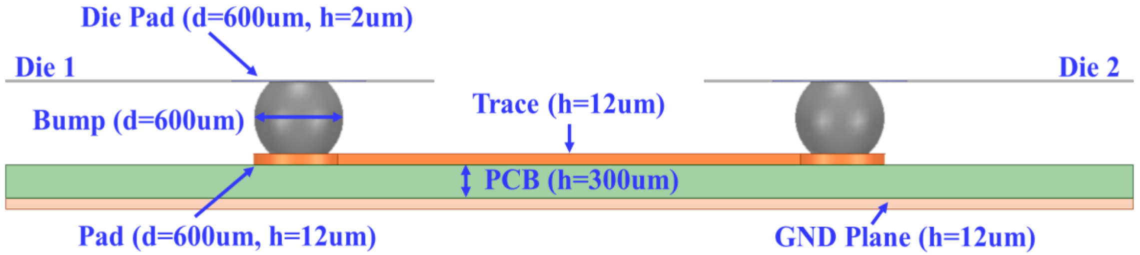
$$ABCD_L = ABCD^{-1}_{LP} ABCD_{meas\_L} ABCD^{-1}_{RP}$$

Ref: Evaluation of a Multi-Line De-embedding Technique up to 110GHz for Millimeter-Wave

Ref: De-embedding techniques for transmission lines: An exploration, review, and proposal, 2013

Trace + Bump Structure and Simulation





S11=S22 , S21=S12

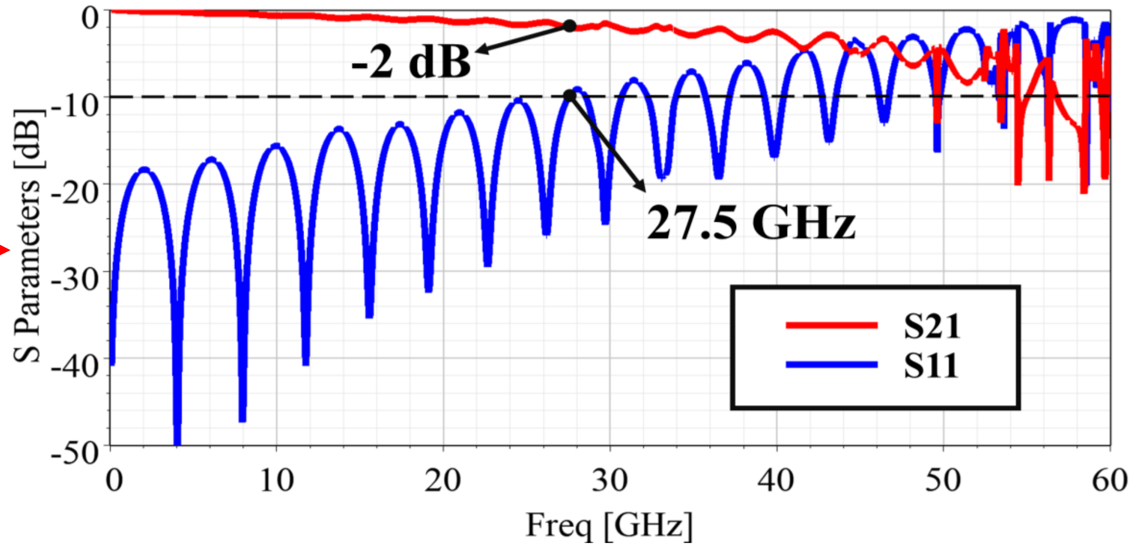
L-2L
Method

1
L: 12.7mm
2L: 25.4mm

2
L: 1.5mm
2L: 3mm

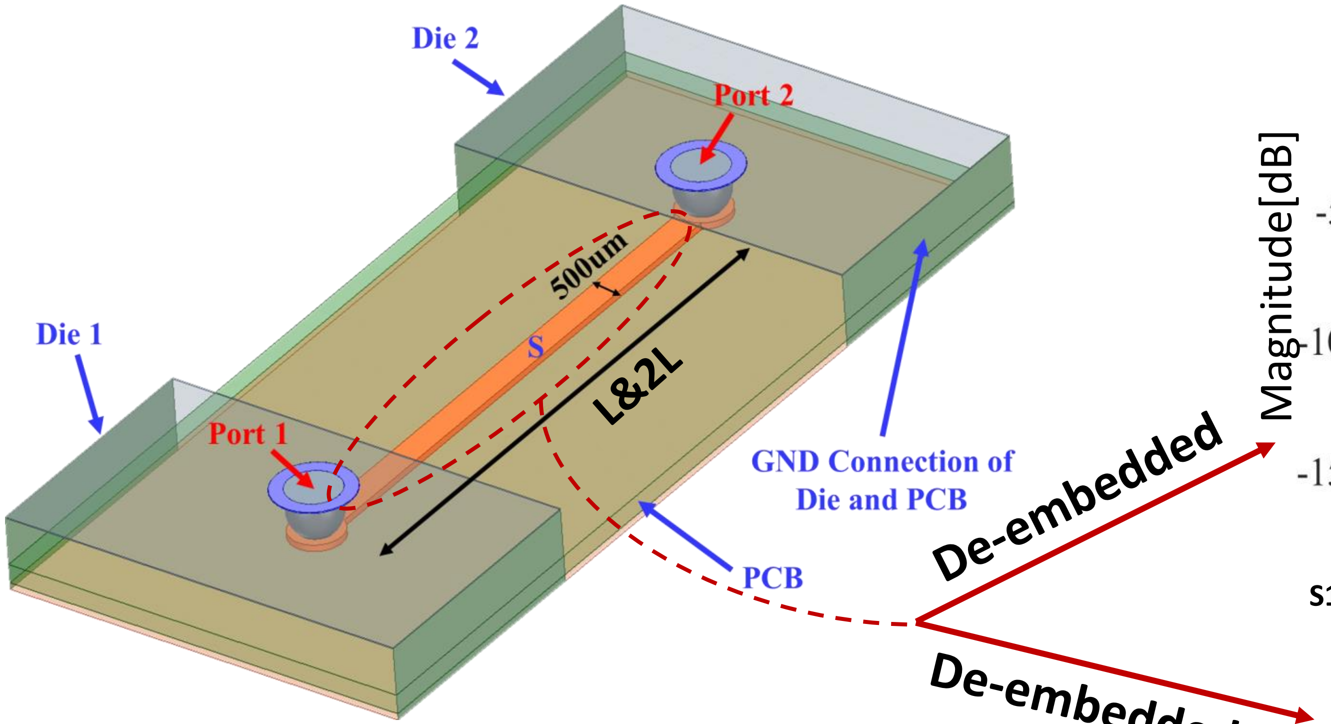
Trace + Bump

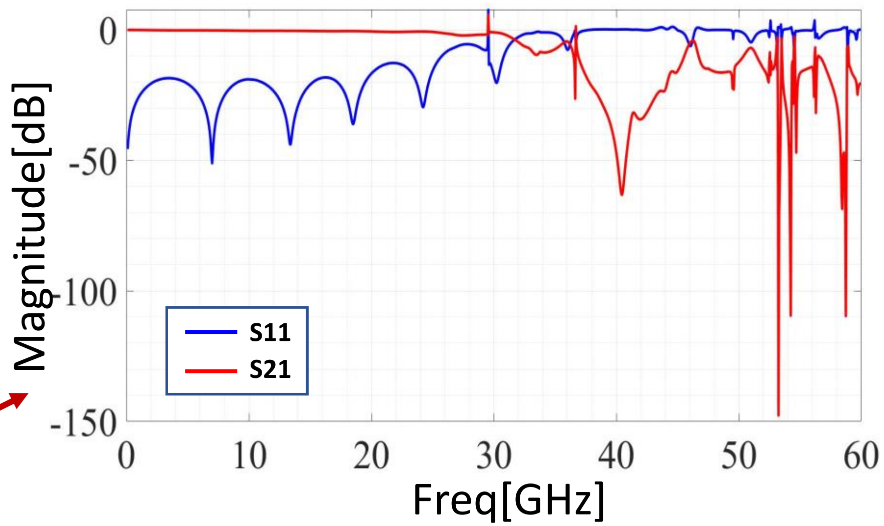
S-Parameters



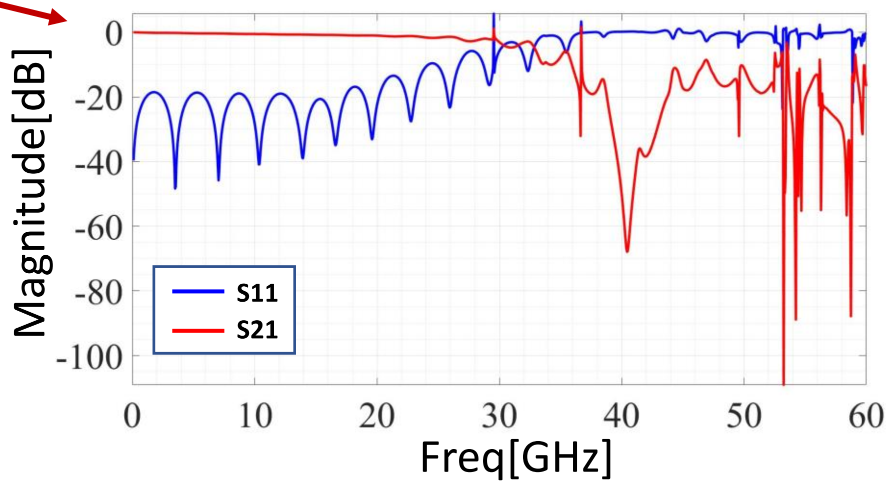
Ref: Technical report, 2020 by Pouya Namaki and Nasser Masoumi

1: S-Parameter Extraction Traces By L-2L Method





S11 and **S21** of the line with a Length of L (**12.7mm** or half Inch)



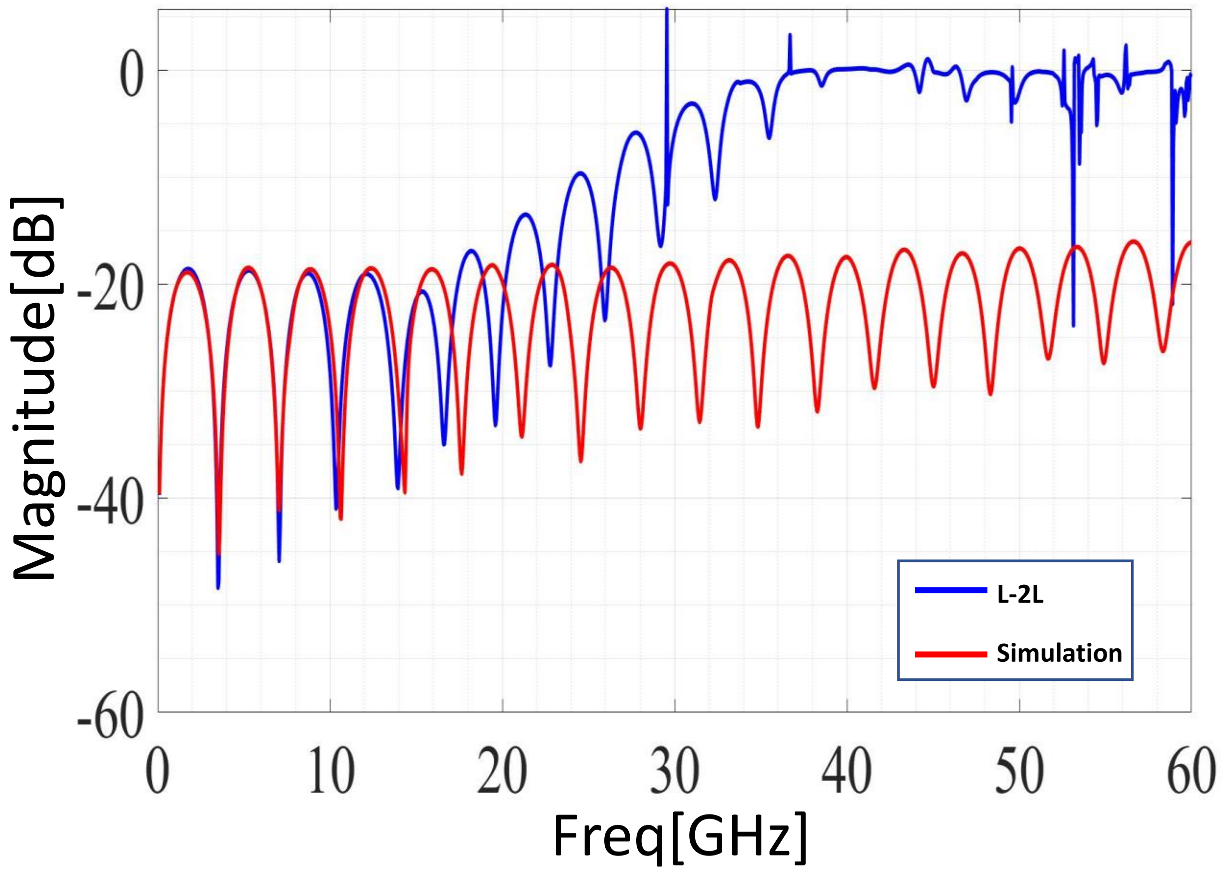
S11 and **S21** of the line with a Length of 2L (**25.4mm** or an Inch)

S-Parameter extracted of trace from L-2L Method:

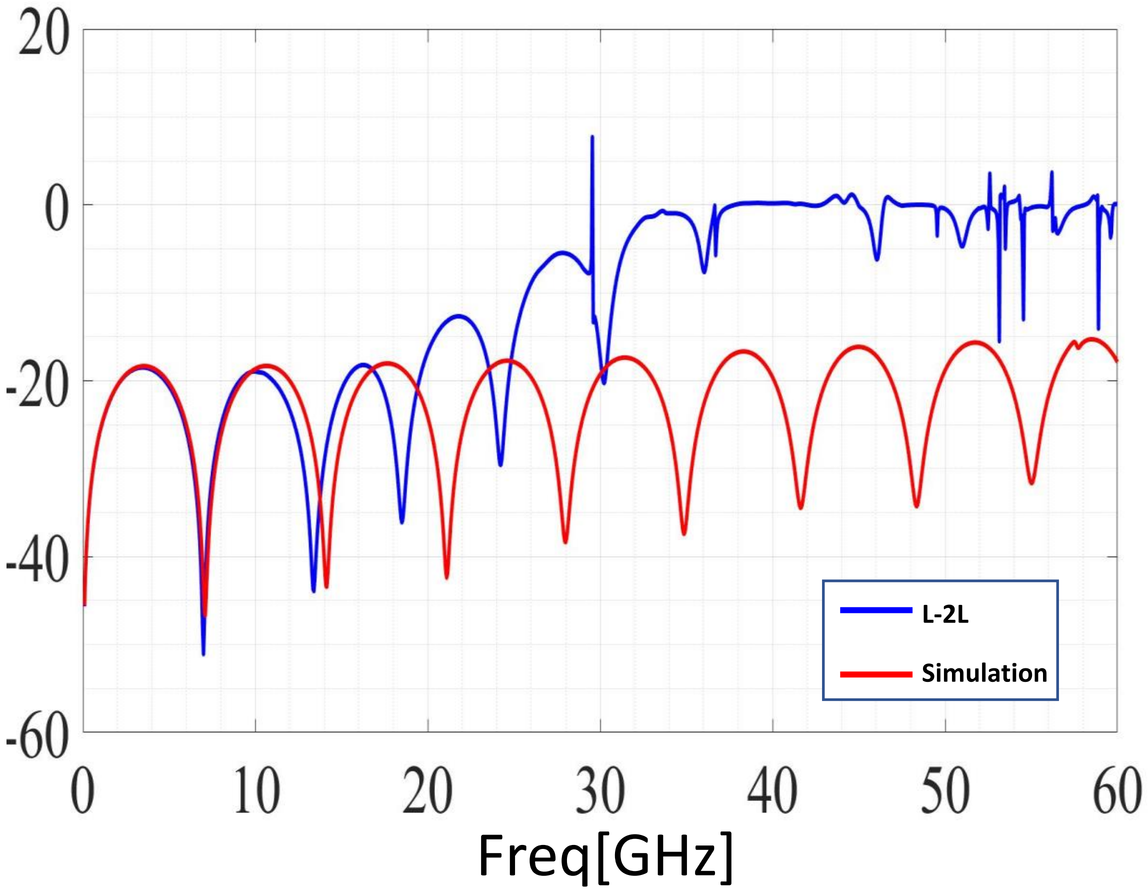
- L = 12.7mm (half inch)
- 2L = 25.4mm (an inch)

Ref: Technical report, 2020 by Pouya Namaki and Nasser Masoumi

S-Parameter Extraction Traces By L-2L Compare to Simulation

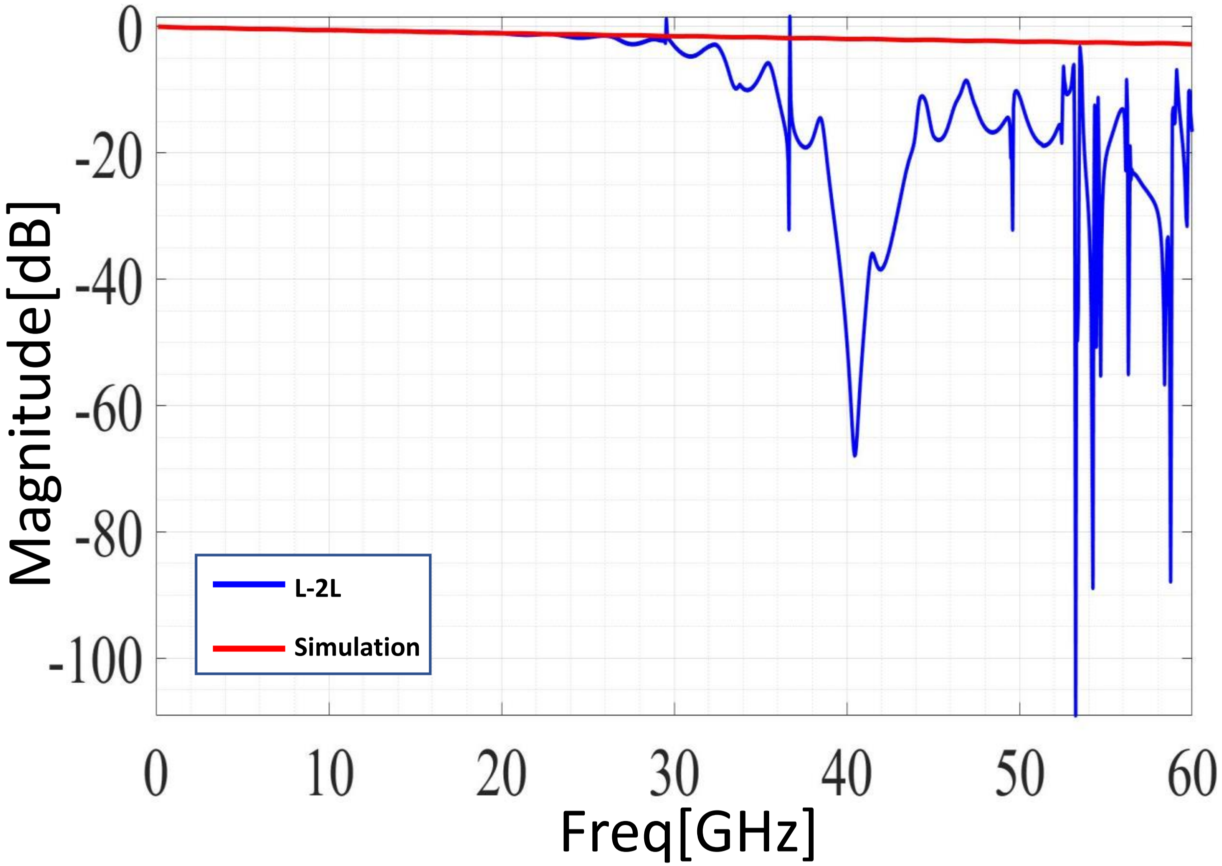


S11 of line with length of 2L from **L-2L method** and **simulation**

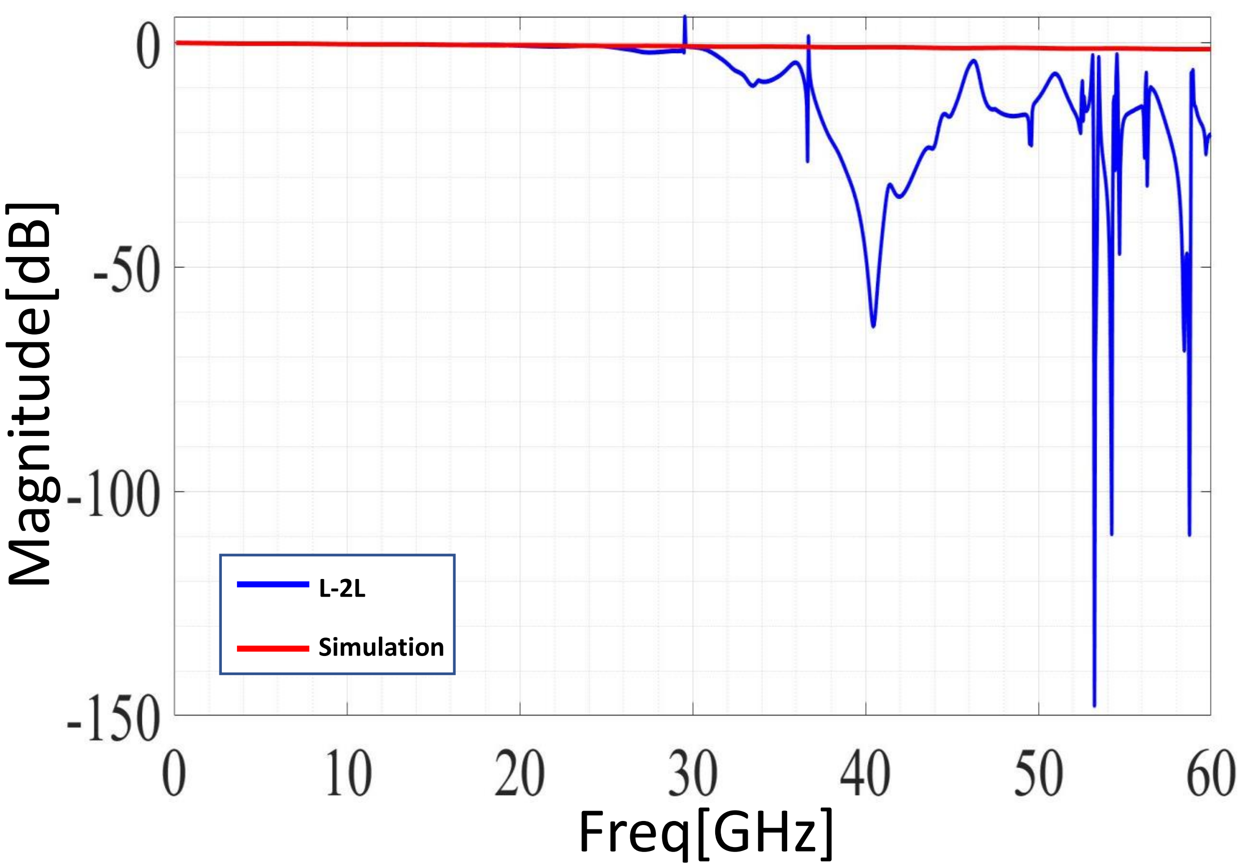


S11 of line with length of L from **L-2L method** and **simulation**

S-Parameter Extraction Traces By L-2L Compare to Simulation (2)

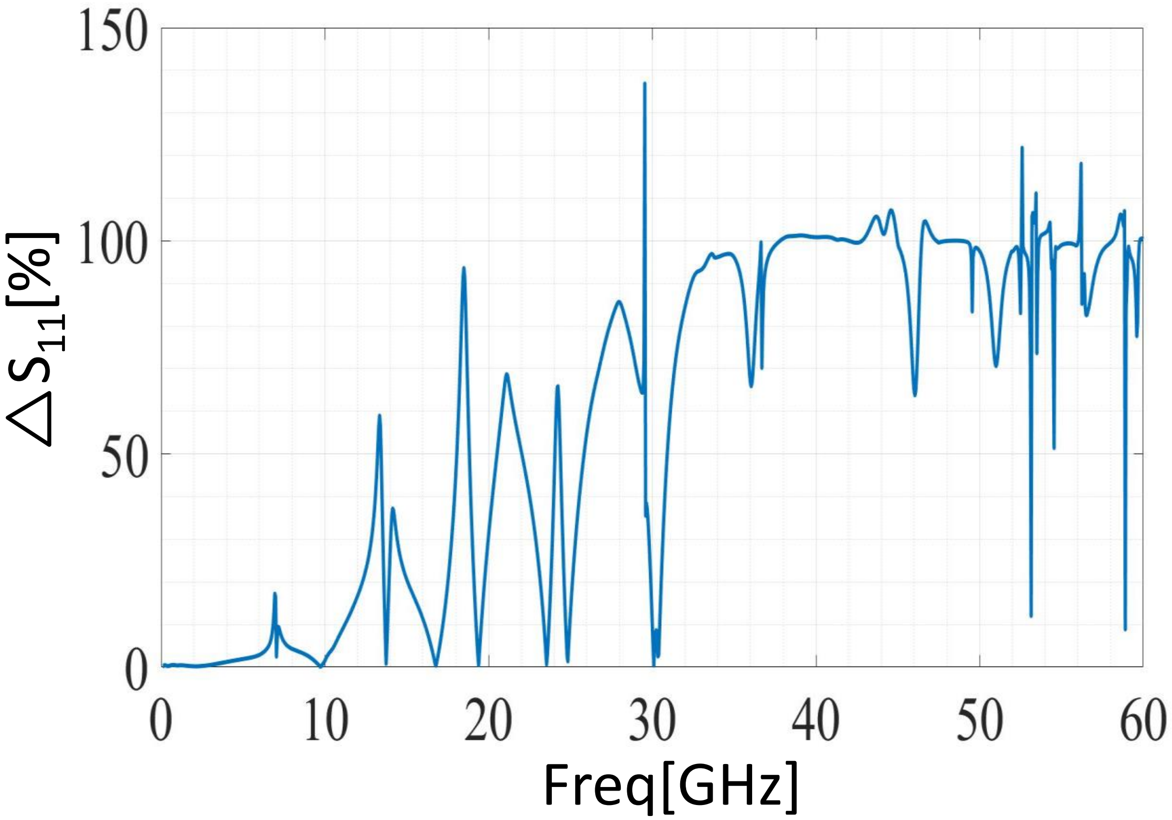


S21 of line with length of 2L from **L-2L method** and **simulation**

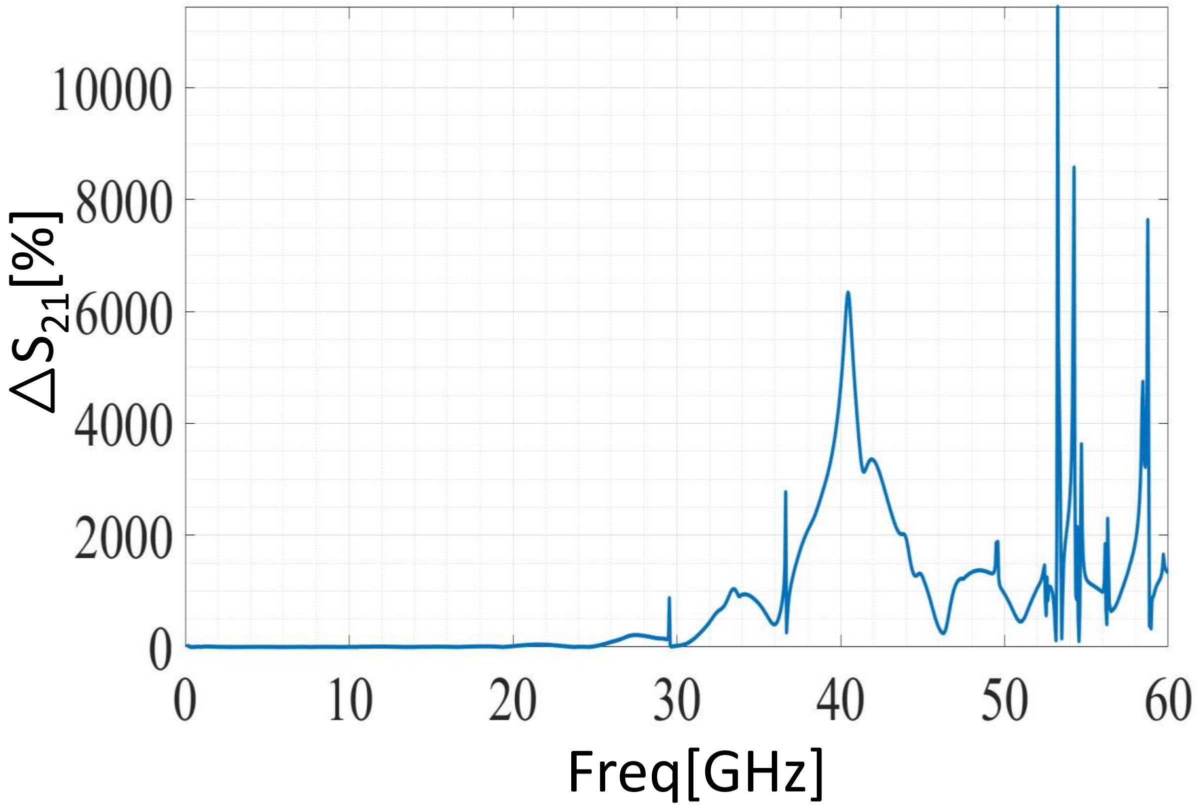


S21 of line with length of L from **L-2L method** and **simulation**

Error of L S-Parameter Due Frequency

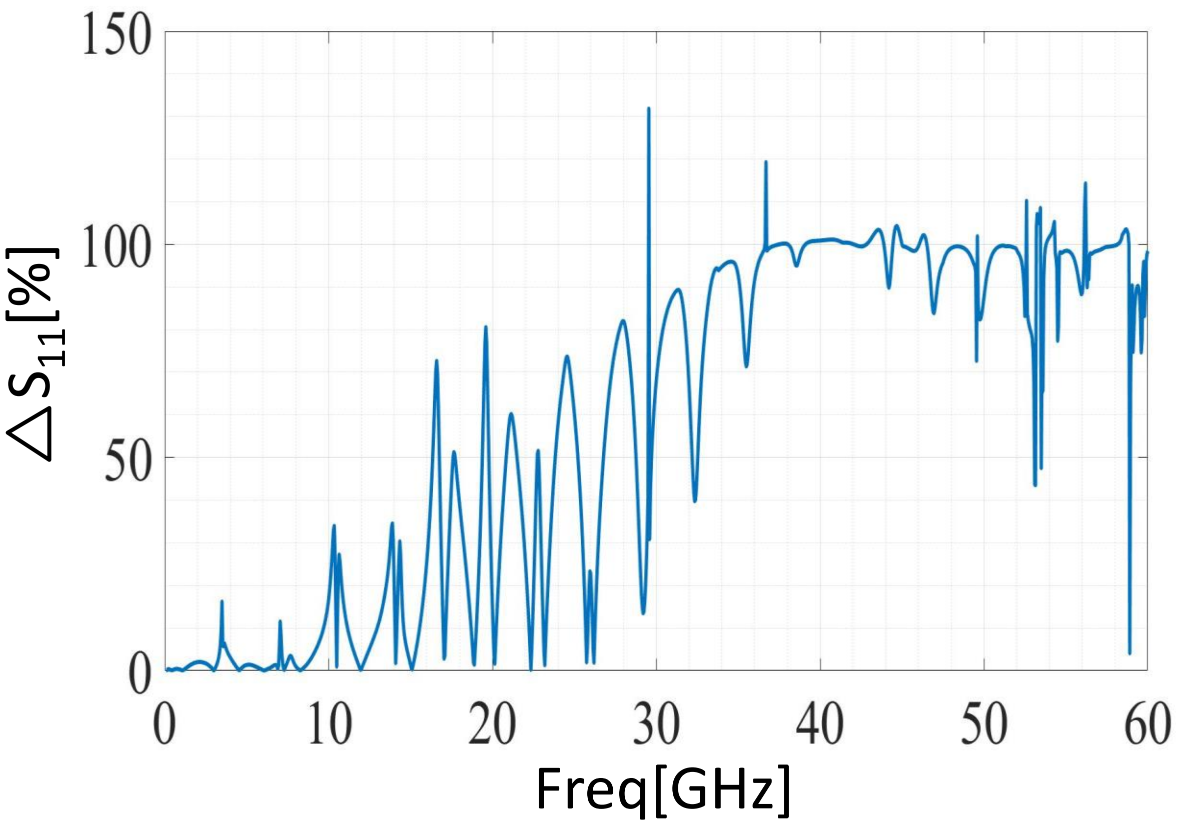


S_{11} error of L (12.7mm) line

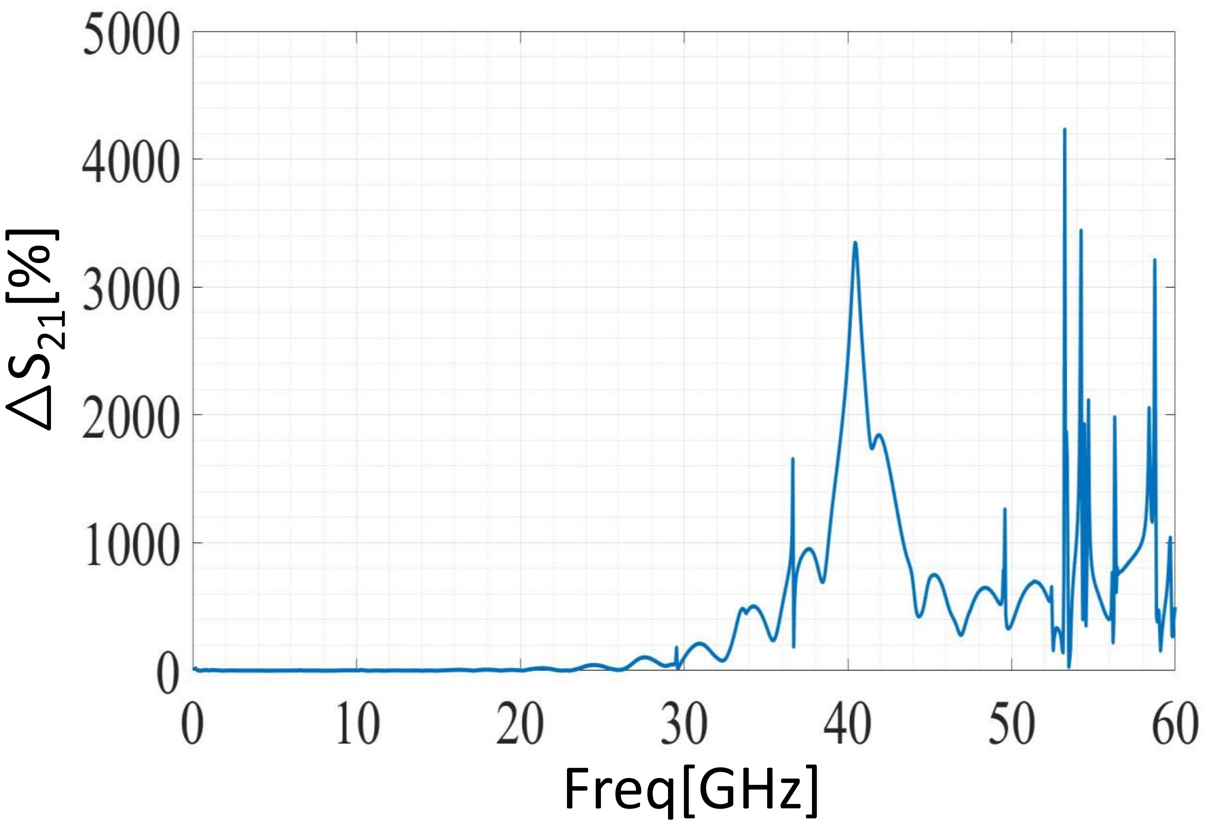


S_{21} error of L (12.7mm) line

Error of 2L S-Parameter Due Frequency



S_{11} error of 2L (25.4mm) line

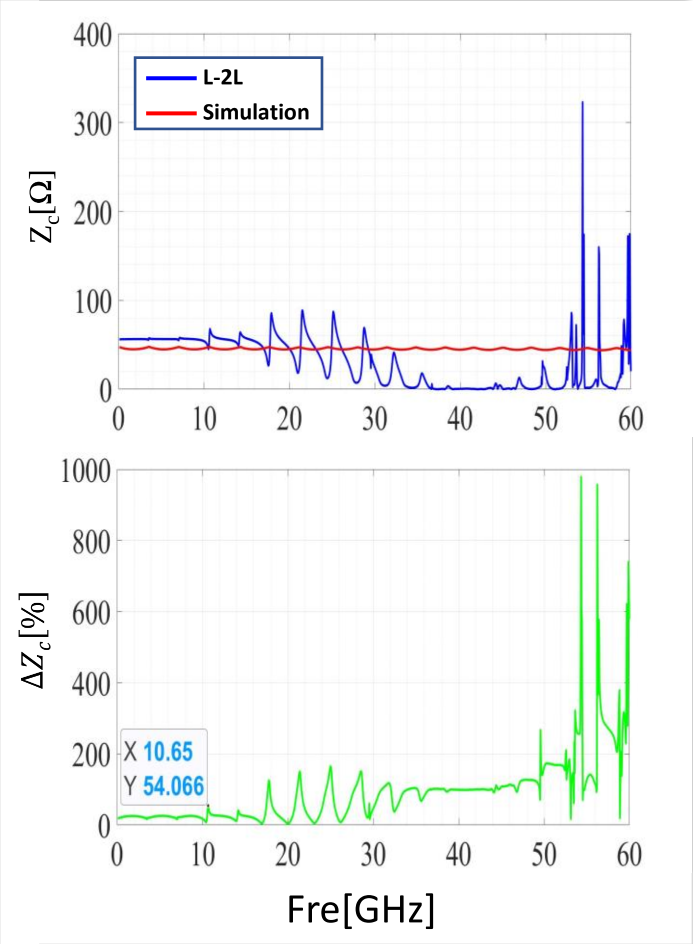


S_{21} error of 2L (25.4mm) line

Characteristics Line's Impedance

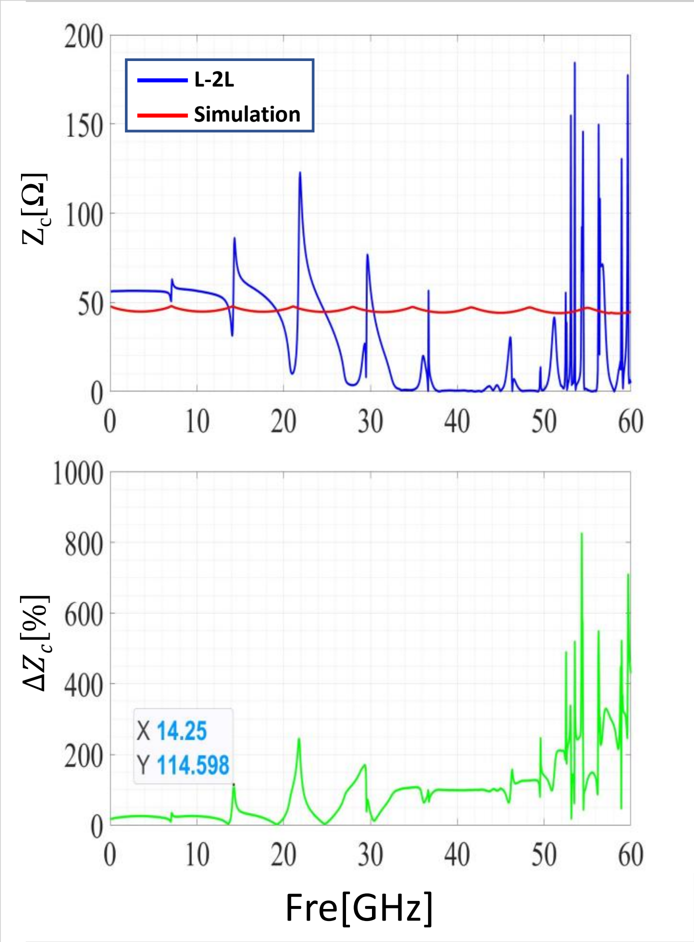
The computation's error of characteristics impedance causes in **10.65Ghz** (2L)

$$Z = Z_0\left\{\frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2}\right\}^{\frac{1}{2}}$$



The computation's error of characteristics impedance causes in **14.25Ghz** (L)

$$Z = Z_0\left\{\frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2}\right\}^{\frac{1}{2}}$$



The Error Created By Increasing Length of the Line

- By using the measured S-Parameter the parasites of the pad can be calculated which is modeled as a **π–type** lumped constant circuit. However, in through-only method, **the length of the through-line is required to be very short** to match with the π–type lumped model.
  - $\Delta = \left|\frac{X^{L-2L} - X^{L}}{X^{L}}\right|$
- In lumped group method, an extra grounded metal strip, which adds **resistance and inductance to the short structure**, is used as a connection between the two ports.

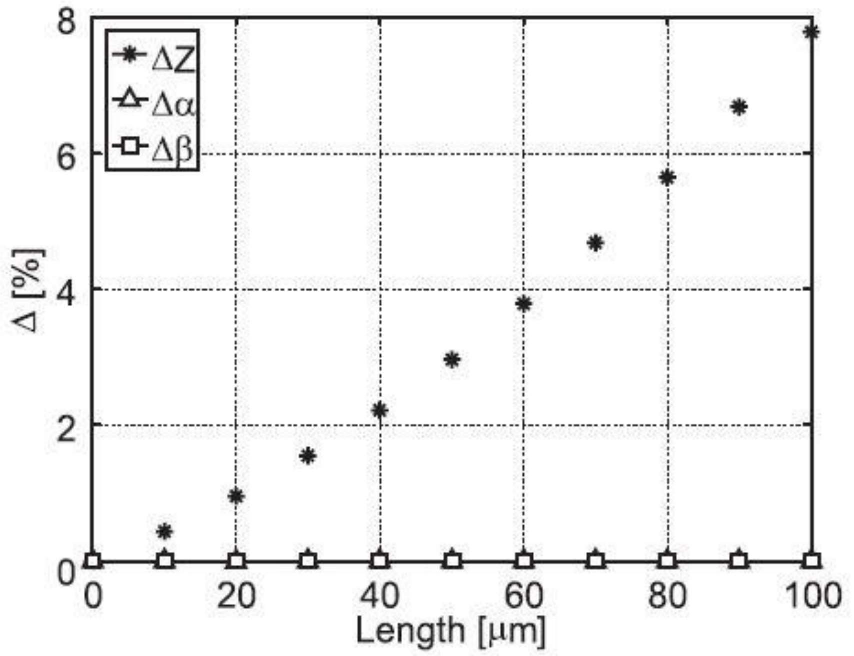


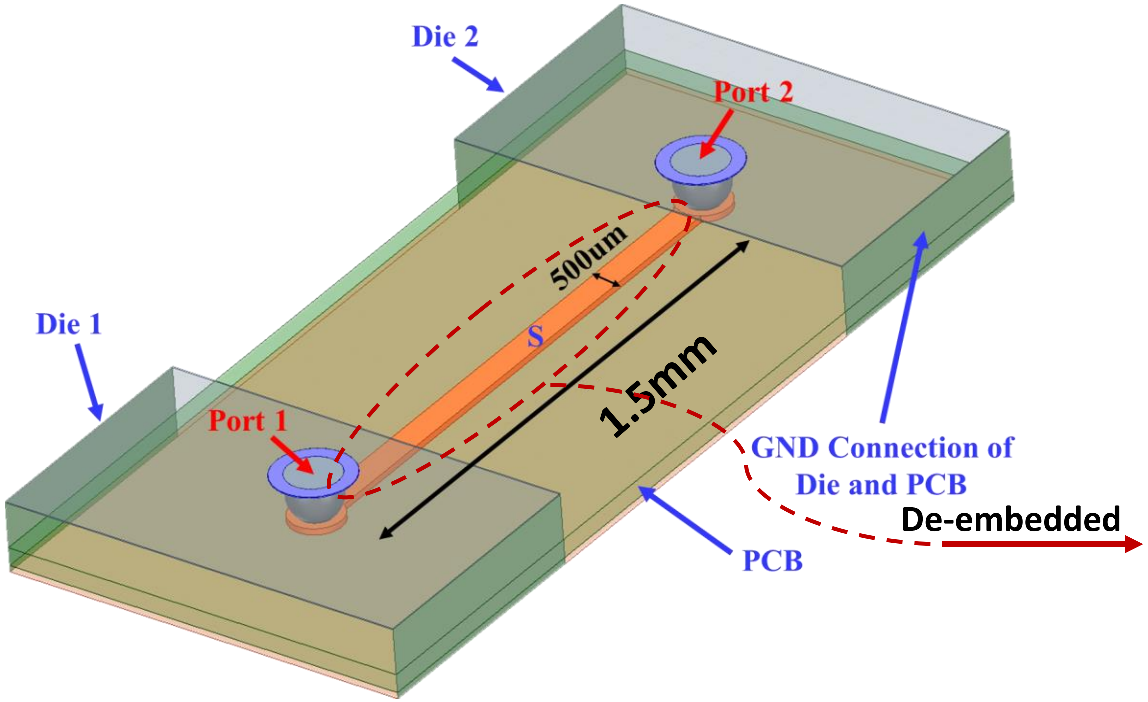
Fig. 4 Calculated results by using through-only method.

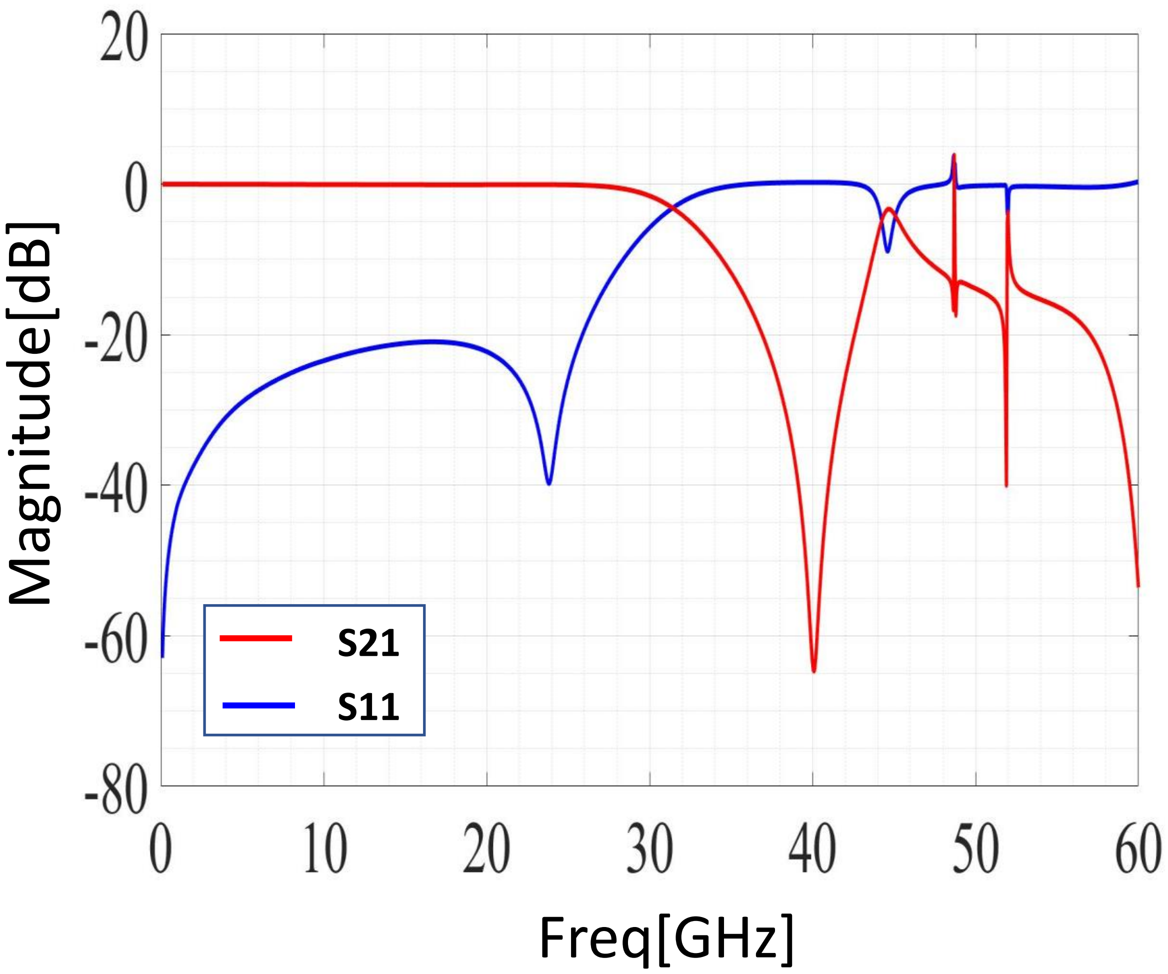
- **The parasitic contribution** of the extra grounded metal strip **cannot be ignored if the frequencies are high or if the DUT structures are large**.

Ref: H. Cho, "A Novel Transmission-Line De-embedding Technique for RF Device Characterization," in IEEE Transactions on Electron Devices, vol, 2009

Ref: Ning Li," Evaluation of a Multi-Line De-Embedding Technique up to 110 GHz for Millimeter-Wave CMOS Circuit Design" , February 2010 IEICE Transactions

2: S-Parameter Extraction Traces By L-2L Method





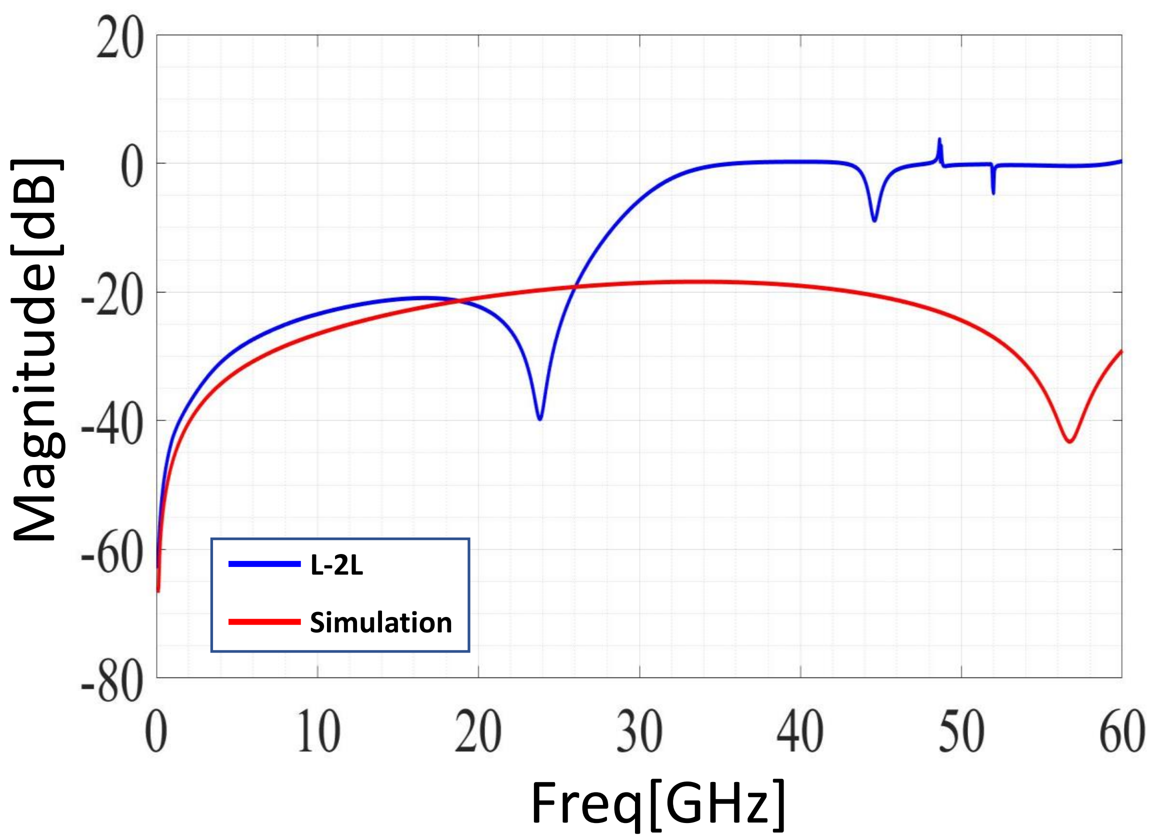
S11 and **S21** of the line with a Length of L (**1.5mm**)

S-Parameter extracted of trace from L-2L Method:

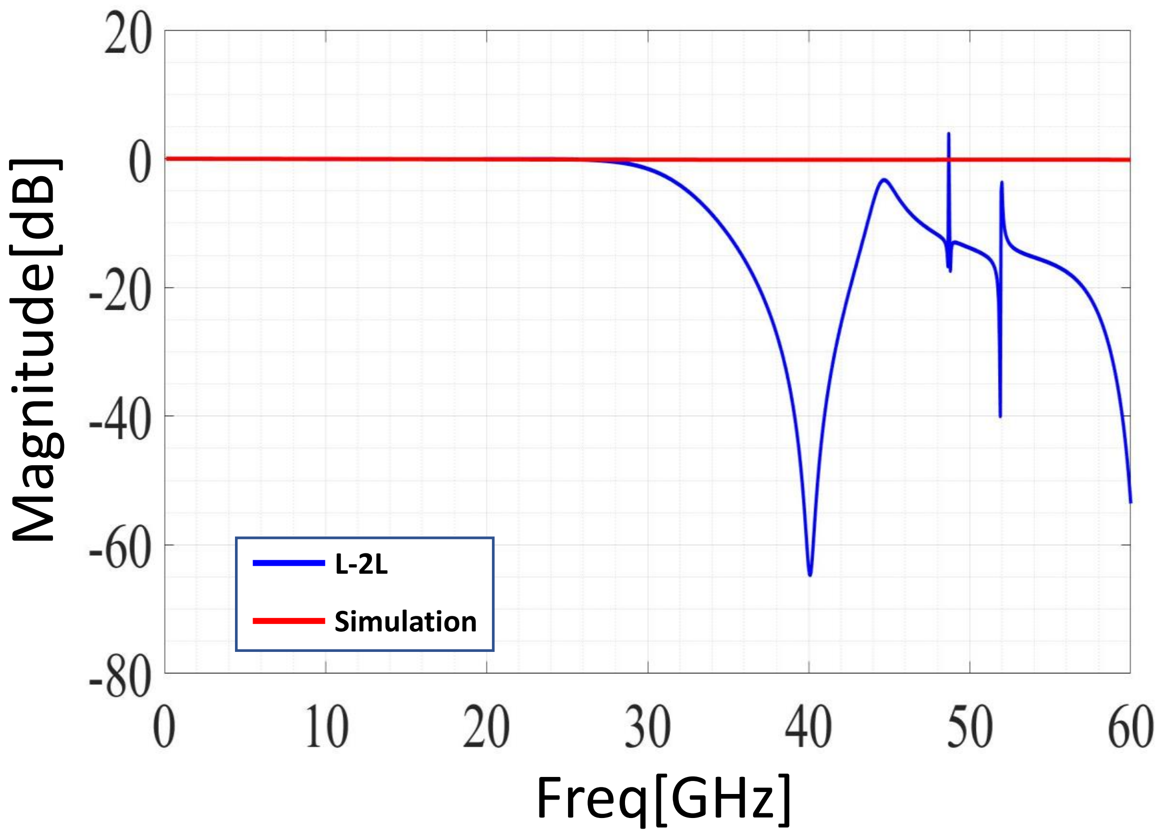
- L = 1.5mm
- 2L = 3mm

Ref: Technical report, 2020 by Pouya Namaki and Nasser Masoumi

S-Parameter Extraction Traces By L-2L Compare to Simulation

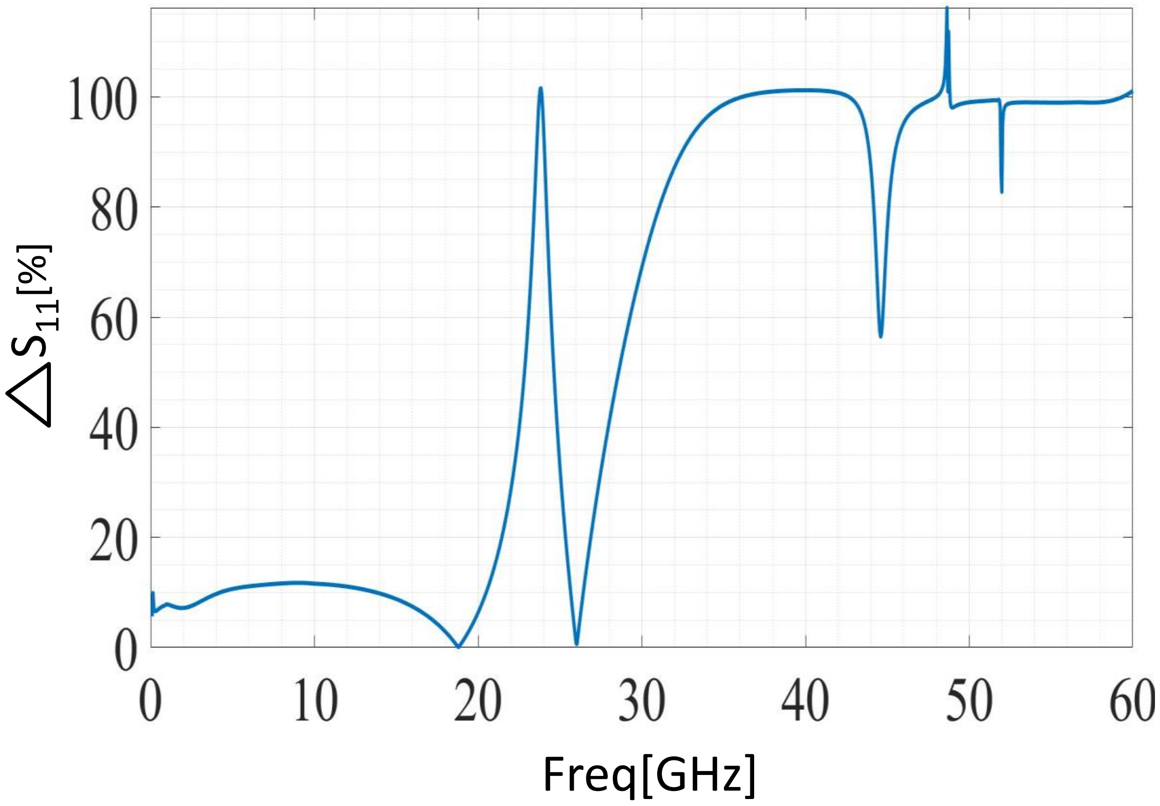


S11 of line with length of L from **L-2L method** and **simulation**

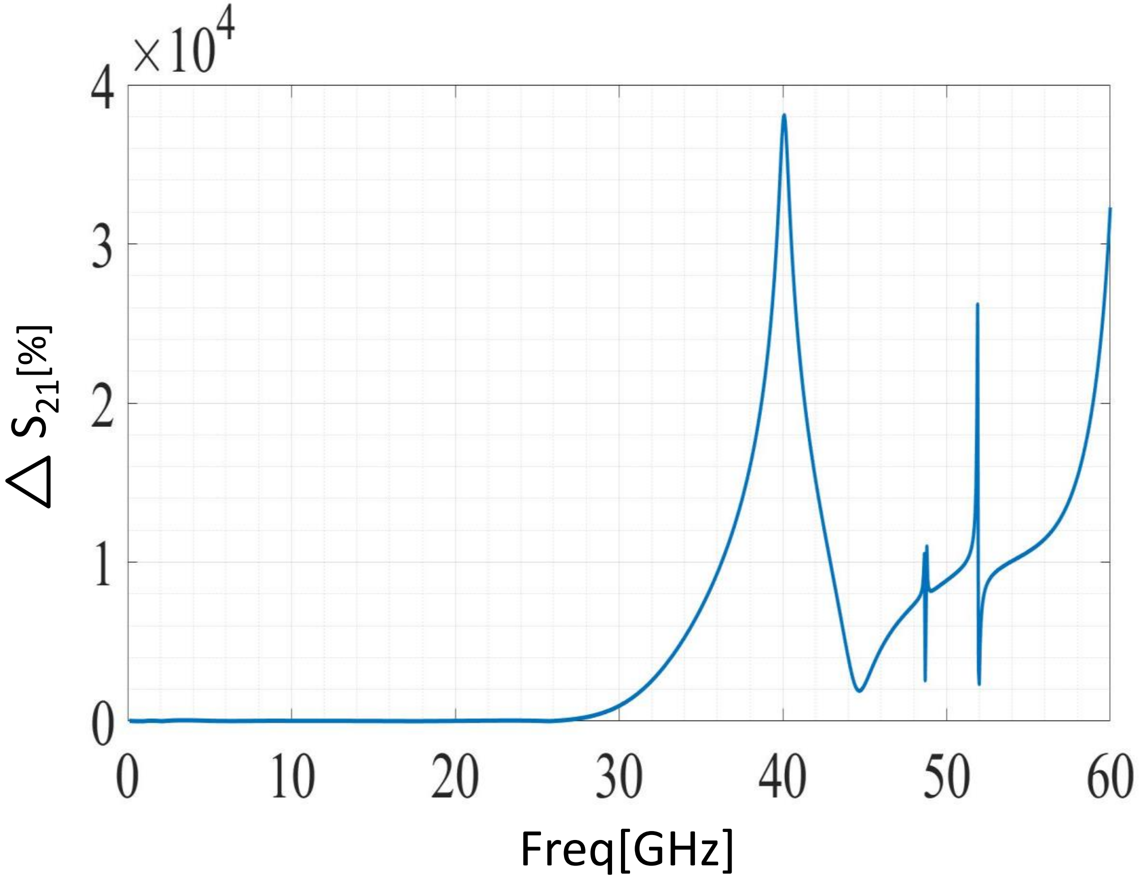


S21 of line with length of L from **L-2L method** and **simulation**

Error of Line’s S-Parameter



S_{11}’s error of L (1.5mm) line



S_{21}’s error of L (1.5mm) line

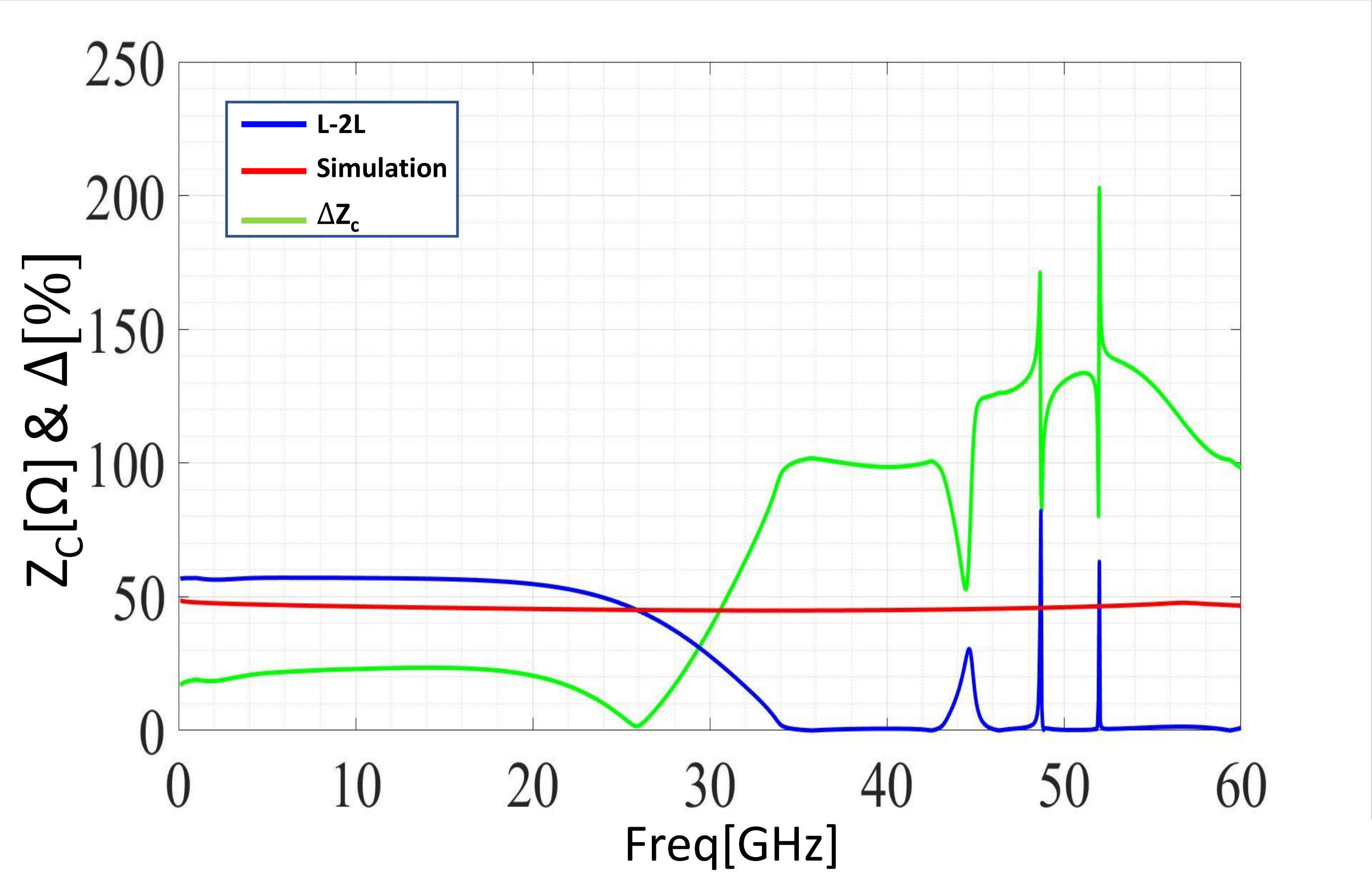
Characteristics Impedance of Line

The computation's error of characteristics impedance causes in **18.8Ghz (L)**

$$Z = Z_0 \left\{ \frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2} \right\}^{\frac{1}{2}}$$

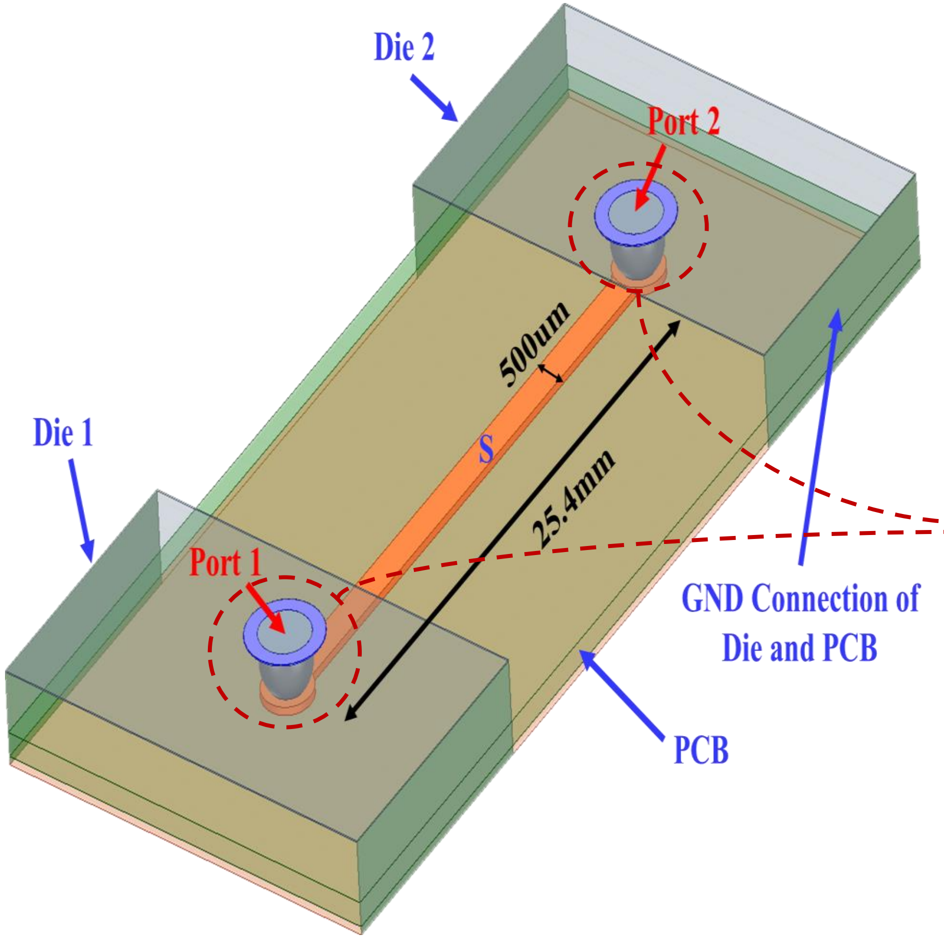
L-2L Method Accuracy:

- L = 25.4mm → 10.65GHz
- L = 12.7mm → 14.25GHz
- L = 1.5mm → 18.8GHz



Characteristics impedance of L line

S-Parameter Extracted Bump By L-2L Method

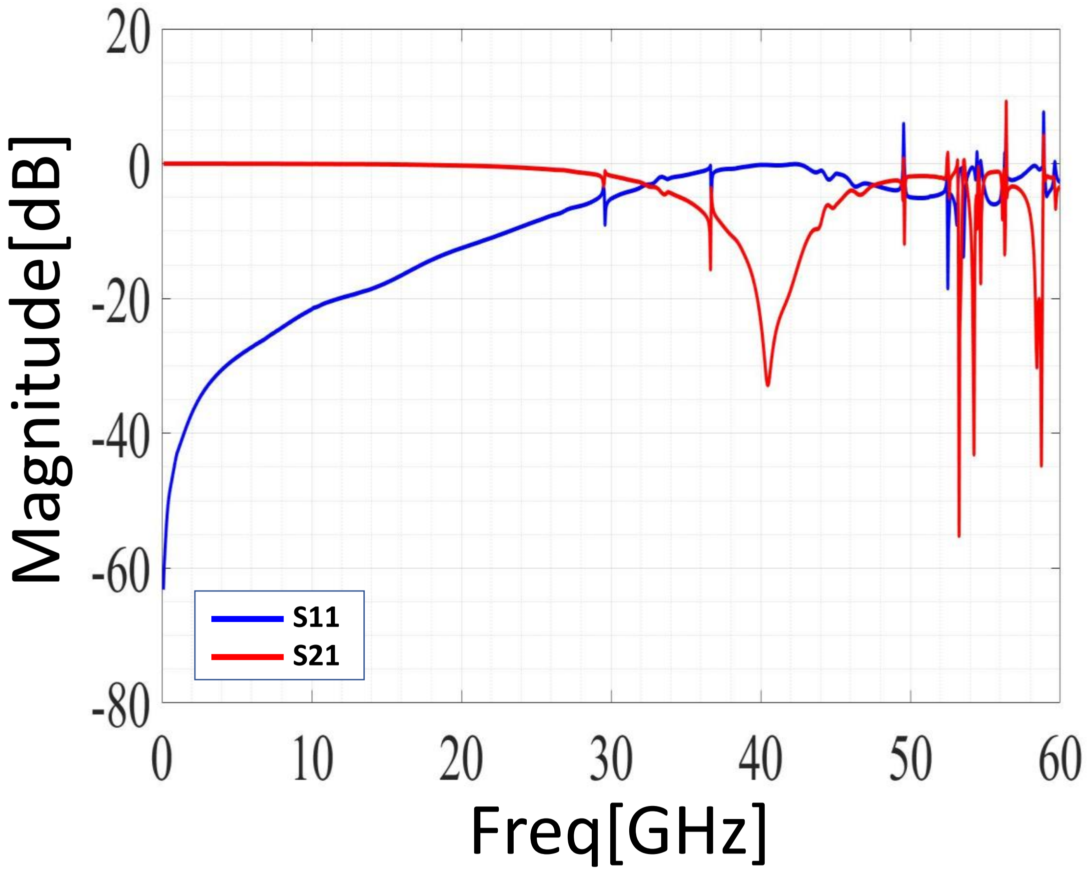


Ref: Technical report, 2020 by Pouya Namaki and Nasser Masoumi

De-embedded

S11 = S22

S21 = S12



Electromagnetic Characteristics of Multiport TSVs Using L-2L De-Embedding Method and Shielding TSVs

This paper presents: An L-2L de-embedding method for characterizing the electromagnetic properties of through silicon vias (TSVs) in 3-D ICs. (this is the first paper that discusses the use of de-embedding method for multiport TSVs.)

- Use of **L-2L** de-embedding method for **multiport TSVs**.
- **Proposed**: Modified structure.
- The performance of the designed structures **with and without shielding TSVs** is examined via both full-wave simulation and the measurements.

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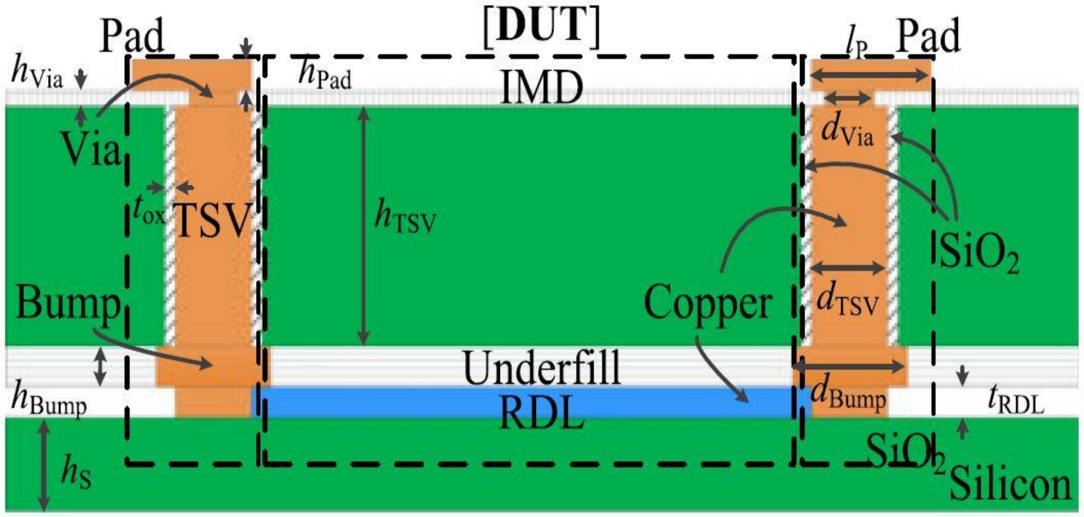
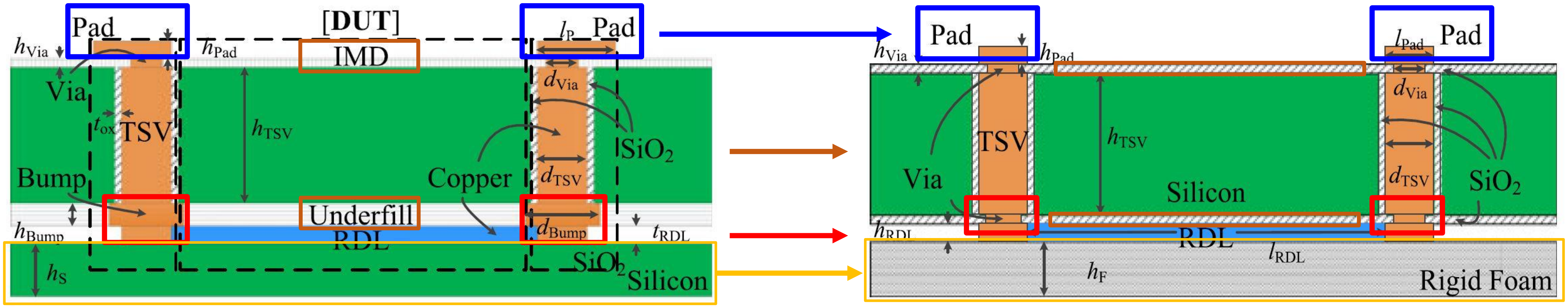
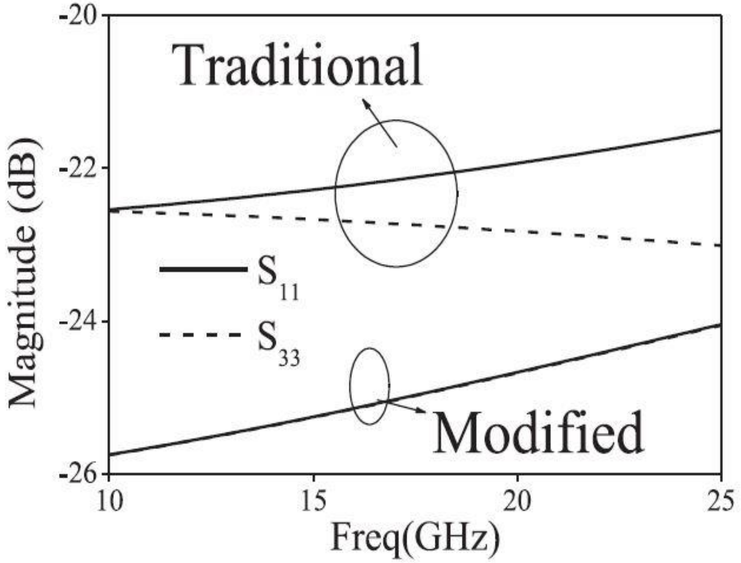


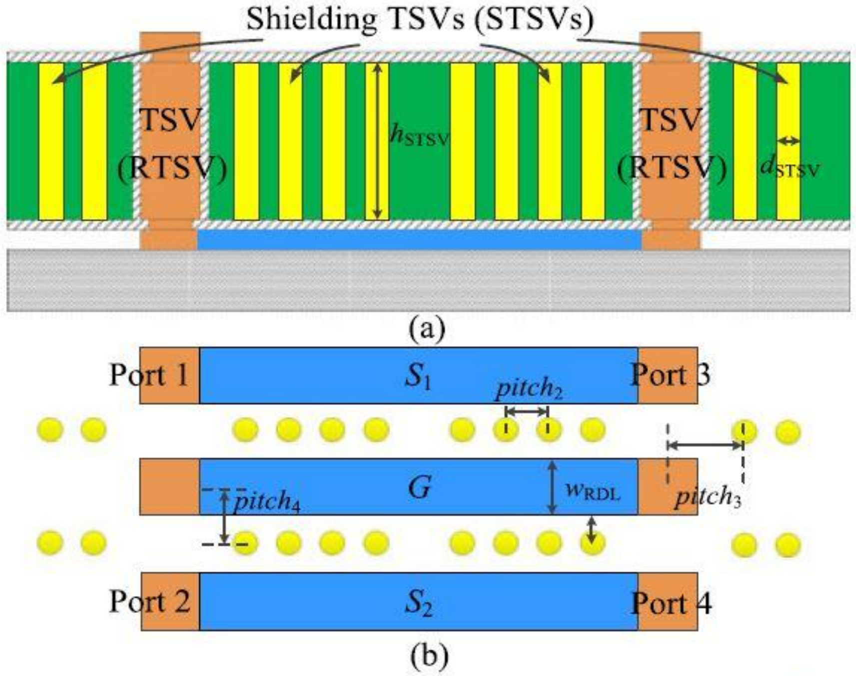
Traditional and Proposed Structures

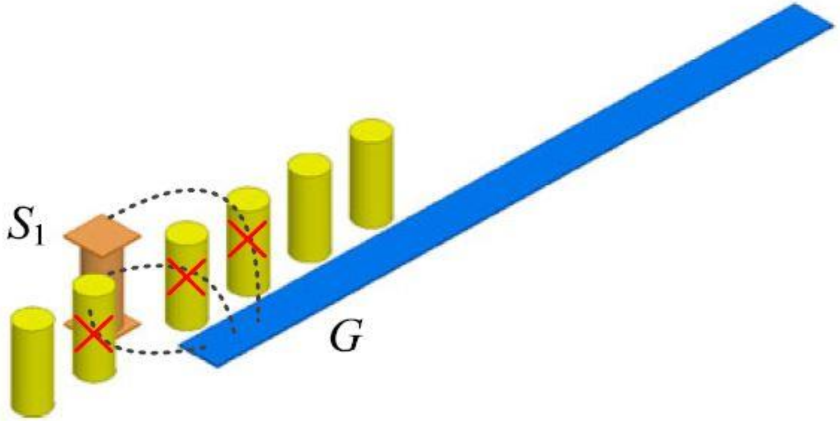


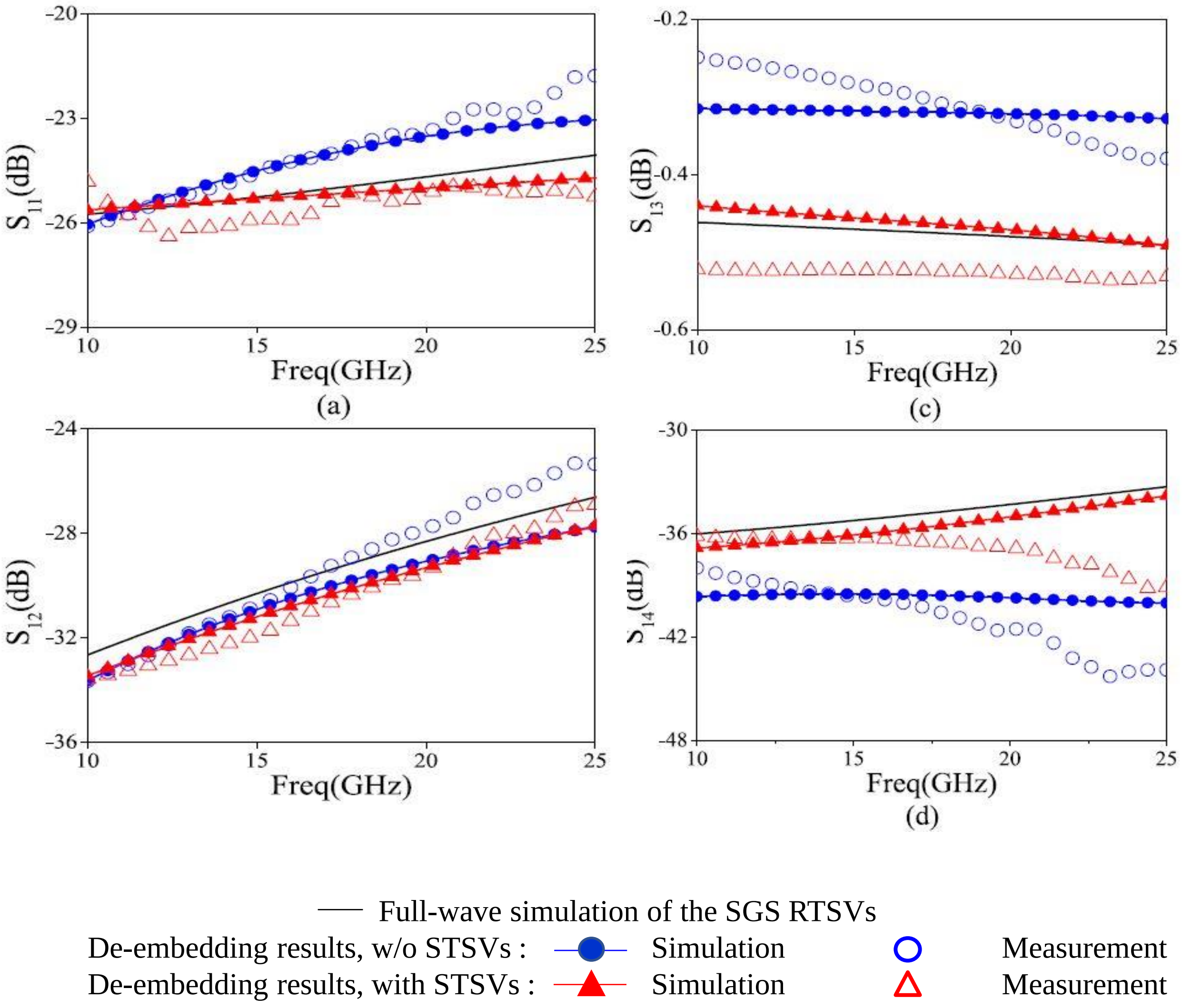
- **Pad**: The **length of pads** decreased
- **Between TSV and RDL**: **Bump** replaced by the **Via**
- **Substrate**: **Silicon** is change to a layer of **Rigid foam**
- **Insulation material**: The **insulation material** used in the **layer between pads** and **the silicon and the layer between the silicon and RDL** are chosen to be **SiO2**.
- The **height of RDLs** is changed to be the same as that of the pads



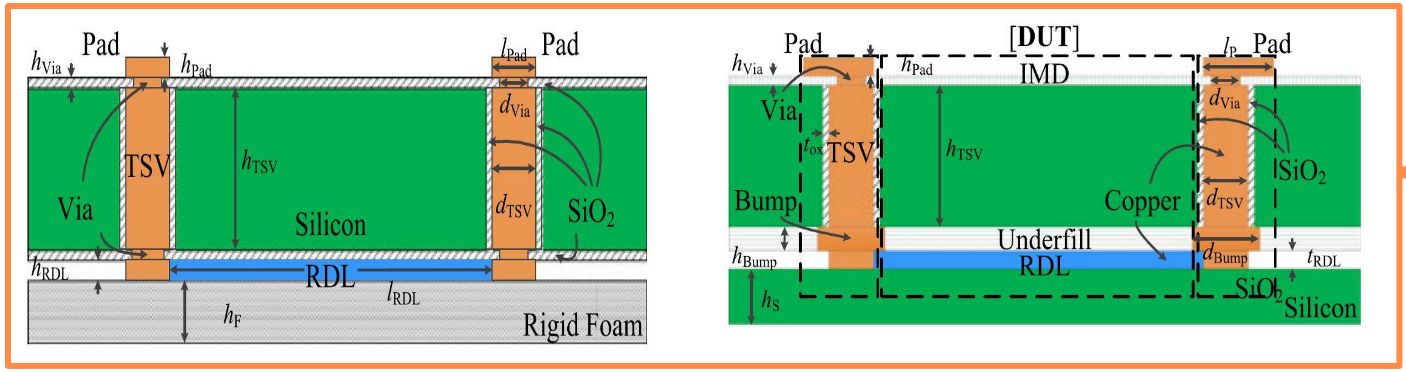
Structure with the Shielding TSVs





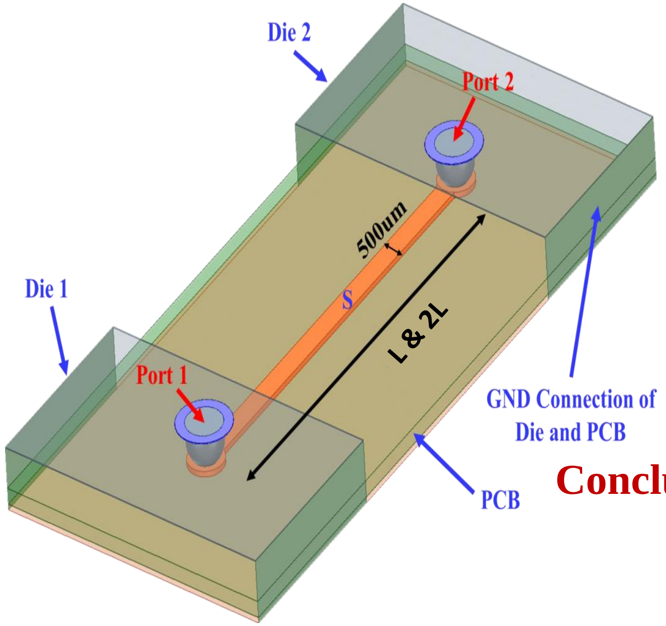


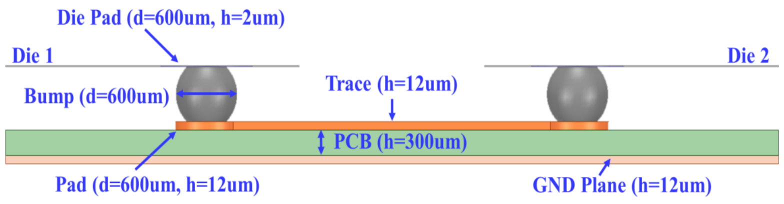
Conclusion: Comparison to the Bump-Trace-Bump Structure



Material Parameters and Dimensions

Design Parameter	Dimension	Material Parameter	Value
Pad thickness (h_{pad})	2 μm	Conductivity of Si	10 S/m
Pad length (l_P)	60 μm	Conductivity of copper	5.95 $\times$ 10^7 S/m
Pad length (l_{pad})	50 μm	Conductivity of IMD	0 S/m
Via height (h_{via})	0.5 μm	Conductivity of SiO_2	0 S/m
Via diameter (d_{via})	35 μm	Conductivity of Underfill	0 S/m
TSV height (h_{TSV})	100 μm	Conductivity of Foam	0 S/m
TSV diameter (d_{TSV})	40 μm	Relative permittivity of Si	11.9
Pitch between TSVs ($pitch_1$)	100 μm	Relative permittivity of copper	1
Pitch between TSV and STSV ($pitch_2$)	65 μm	Relative permittivity of IMD	1
Pitch between STSVs ($pitch_3$)	80 μm	Relative permittivity of SiO_2	4
Pitch between STSVs and RDL ($pitch_4$)	50 μm	Relative permittivity of Underfill	1
SiO_2 thickness (t_{ox})	0.5 μm	Relative permittivity of Foam	1
Bump height (h_{Bump})	5 μm	Relative permeability of Si	1
Bump diameter (d_{Bump})	30 μm	Relative permeability of copper	1
RDL thickness (t_{RDL})	1 μm	Relative permeability of IMD	1
RDL thickness (h_{RDL})	2 μm	Relative permeability of SiO_2	1
Substrate height (h_S)	200 μm	Relative permeability of Underfill	1
Substrate height (h_F)	5 mm	Relative permeability of Foam	1





Conclusion:

1. Certainly bump better act in high frequency range than TSV.
2. Width of trace should be thinner.
3. Length of trace should be shorter.
4. Bump could be smaller

✓ In high frequency range this method is accurate for **Die-interposer-Die** not for **Die-PCB –Die.**

Future Work

- Use 2X Thru Method for Bump-Trace-Bump Structure

- Automatic Fixture Removal (AFR)

- Comparison of this methods

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