



I am Milad Seyedi, a dedicated researcher specializing in High-Speed Interconnect Analysis, High-Speed Measurement Methods, and Electronics. My deep passion is to continuously expand my knowledge in these fields, immersing myself in the intricate mathematics that comes with high-speed measurement challenges. In addition, my research focus centers on developing algorithms aimed at tackling these complex challenges and finding innovative solutions.

I am an M.Sc. in Electrical Engineering (Electronic major) from the University of Tehran, Iran, and currently a Research Assistant at CSTLab and ACSDCLab under the supervision of Dr. Nasser Masoumi & Dr. Samad Sheikhaei

Throughout my academic journey, I have consistently sought to harmonize mathematical precision with the practical and theoretical dimensions of electronics, offering a unique perspective and valuable skills that can help any electronic research team.

PUBLICATIONS

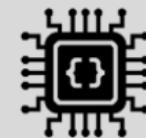
Journal Papers

- **M. Seyedi, N. Masoumi, and S. Sheikhaei** (2023), Investigating Test Structure Dimensions Impact on T-Type L-2L De-Embedding Accuracy for On-Wafer T-Model Transmission Lines, Under progresses.
- **M. Seyedi, N. Masoumi, P. Namaki (2023), and S. Sheikhaei**, 2X-Thru De-Embedding Method Using Time Domain Impedance Response for S-Parameter Characterization of DUT in Broadband PCB, submitted on Elsevier AEU .
- Pouya Namaki, Nasser Masoumi, **Milad Seyedi**, and Mohammad-Reza NezhadAhmadi (2023), An Extended L-2L De-embedding Method for Modeling and Low Return-Loss Transition of Millimeter Wave Signal Through Silicon Interposer, Published on IEEE Transactions on EMC.

Conference Papers

- **Milad Seyedi, Nasser Masoumi, and Samad Sheikhaei** (2023), T-type L-2L De-Embedding Method for On-Wafer T-model Transmission Line Network, submitted on ICEE.

MY SPECIALITIES



RESEARCH

PCB DESIGNING

C PROGRAMMING

ANALYSIS & MEASUREMENT
HIGH SPEED INTERCONNECTION

PYTHON PROGRAMMING

SKILLS

Hardware Des. Language	Proficient	Verilog
	Intermediate	VHDL
Software	Altium Designer, ADS, Ansys HFSS, ISE Design Suite, HSPICE, PSPICE, ISE Design Suite, Panda, IDLE Python, ARM STM Studio, AVR Code vision, Microsoft Office	
Programming Language	Proficient	Python, MATLAB, C
	Intermediate	C++, Linux
Language	Kurdish	Native
	Farsi	Native
Language	English	Proficient

EDUCATION AND WORKING EXPERIENCE



- October 2022**
PM and Senior Hardware Designer
SEDAN Company, Tehran, Iran
- September 2020**
Faculty of Electronic and Computer
University of Tehran, Tehran, Iran
- June 2015**
Hardware Designer
ImenAra Company, Urmia, Iran
- September 2013**
Faculty of Electronic and Computer
Urmia University, Urmia, Iran
- February 2008**
Gold Medal Karate Championship
England, Harvey Hadden Stadium

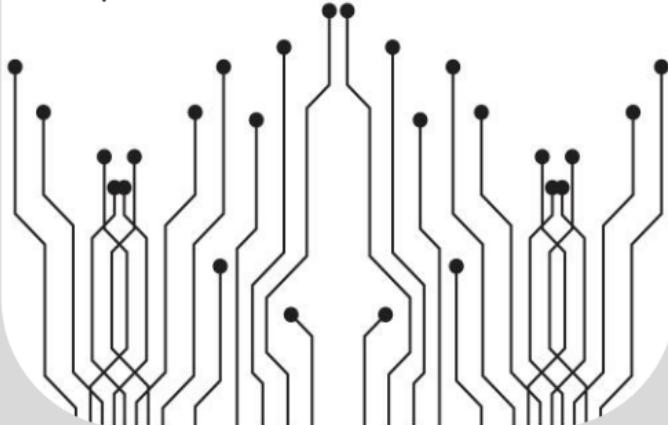
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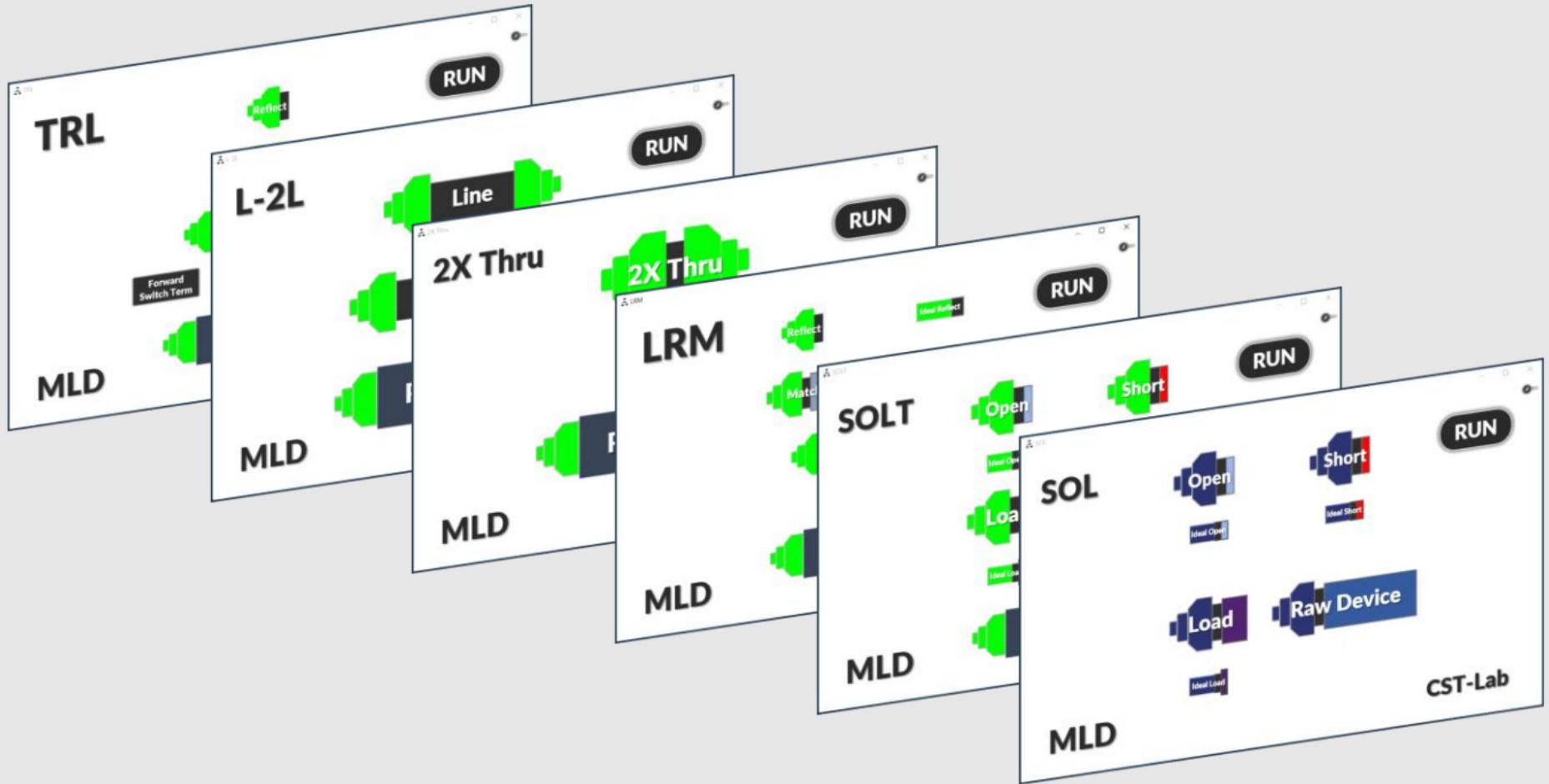
De-embedding Methods

Unveiling Hidden Truths in Signals

De-embedding methods are indispensable in modern technology due to their ability to untangle the complexities introduced by measurement setups, revealing the true nature of devices or phenomena. These techniques encompass a variety of approaches across fields like electronics, communications, and electromagnetic analysis. From TRL and SOLT calibration to TDR de-embedding and electromagnetic simulation-based methods, they all share the common goal of removing unwanted effects such as impedance mismatches, connectors, and cables. Moreover, the significance of software tools capable of performing de-embedding cannot be overstated. These software solutions facilitate the efficient and accurate extraction of essential data from measurements and simulations, enabling engineers and researchers to make informed decisions, optimize designs, and push the boundaries of technological advancements with precision and confidence.

MLD De-embedding Software

I have developed software using Python programming language as the final outcome of my master's thesis, which can be used to apply various one-port, two-port, and three-port de-embedding methods to their respective structures.

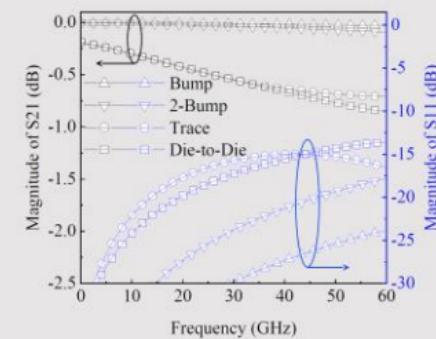
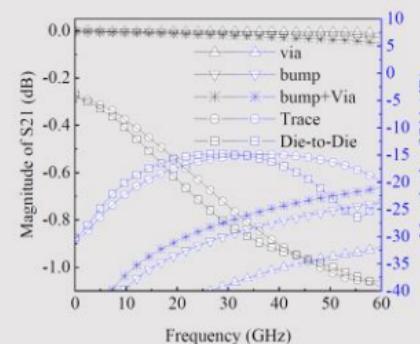
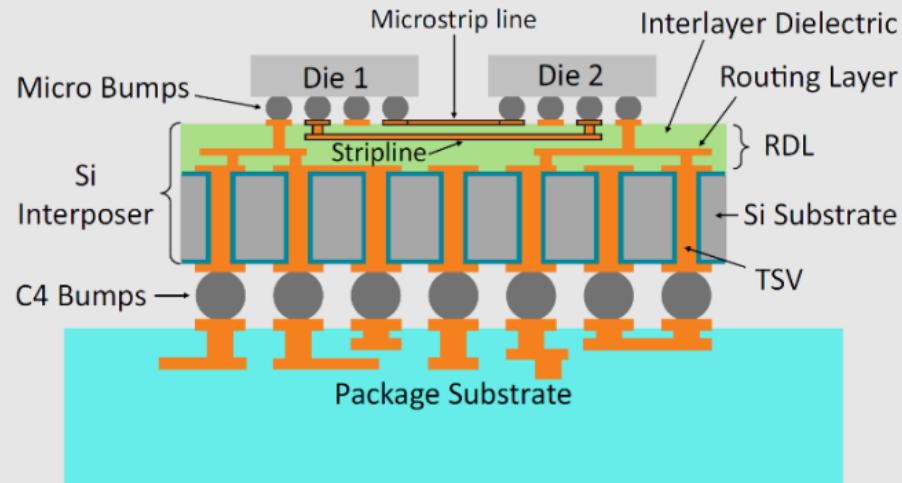


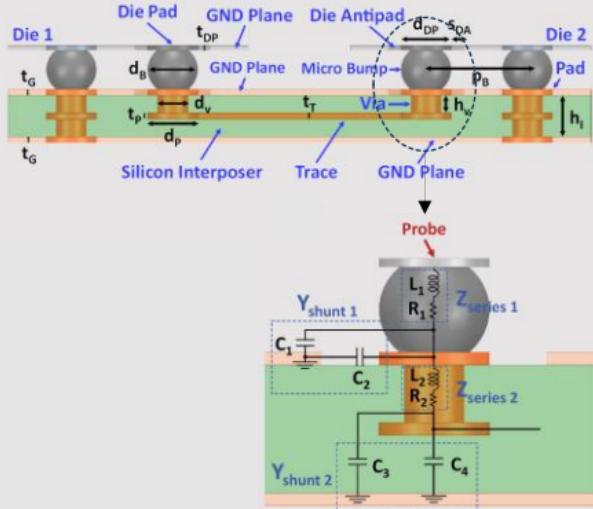
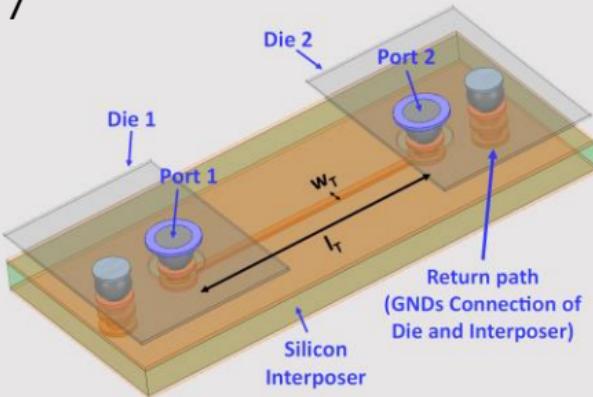
Flip-Chip Technology

Flip-chip technology is an advanced packaging method for integrated circuits (ICs) where the semiconductor die is flipped upside down and directly attached to the package substrate using solder bumps. This approach offers several advantages, including higher I/O density, improved electrical performance due to shorter interconnects, better thermal management, reduced package size, and enhanced reliability compared to traditional wire bonding. The process often involves the use of underfill material to strengthen solder joints and protect against contaminants. Flip-chip technology is commonly employed in various electronic devices, especially those requiring high performance, miniaturization, and efficient heat dissipation, making it a crucial component of modern semiconductor manufacturing.

Flip-Chip Technology on Interposer Substrate

Interposers utilizing flip-chip technology are specialized components crucial for semiconductor packaging, allowing the integration of multiple chips in compact configurations, particularly in advanced multi-chip modules and 3D packaging setups. They serve as substrates between semiconductor dies, employing flip-chip technology to form interconnected stacks or side-by-side arrangements. Varieties include silicon, organic, and glass interposers, each with specific cost, performance, and thermal characteristics. Interposers enable 3D integration, high signal density, effective thermal management, and the integration of diverse die types. This project was carried out in collaboration with teams from the CIARS laboratory at the University of Waterloo, Canada, and the CSTLab laboratory at the University of Tehran, Iran. The results of this research were published in an article entitled "[An Extended I-2L De-embedding Method for Modeling and Low Return-Loss Transition of Millimeter Wave Signal Through Silicon Interposer](#)" in the IEEE Transactions on EMC journal.



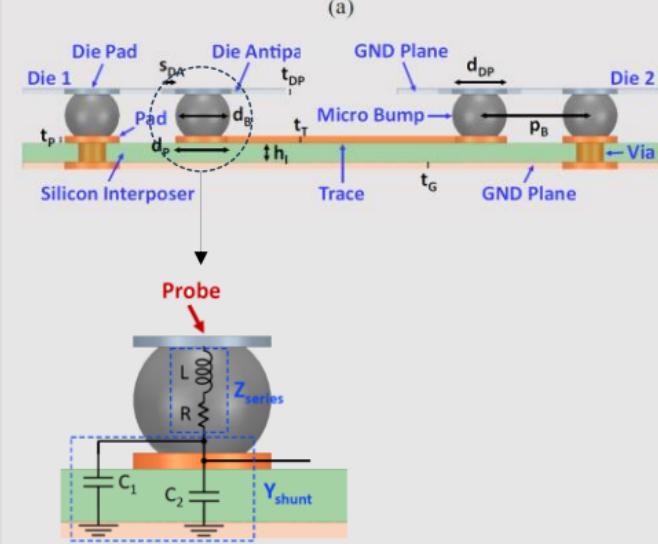
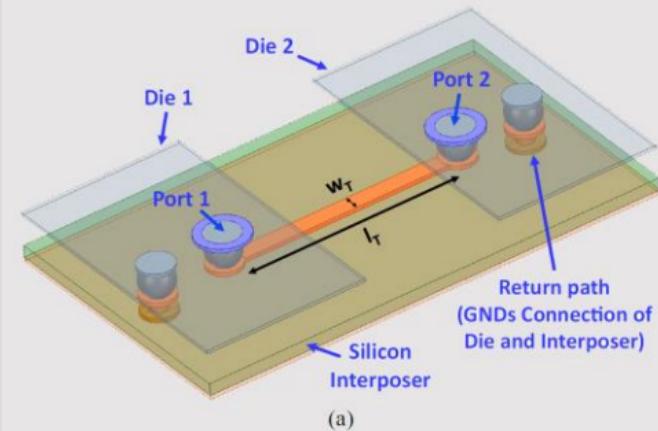


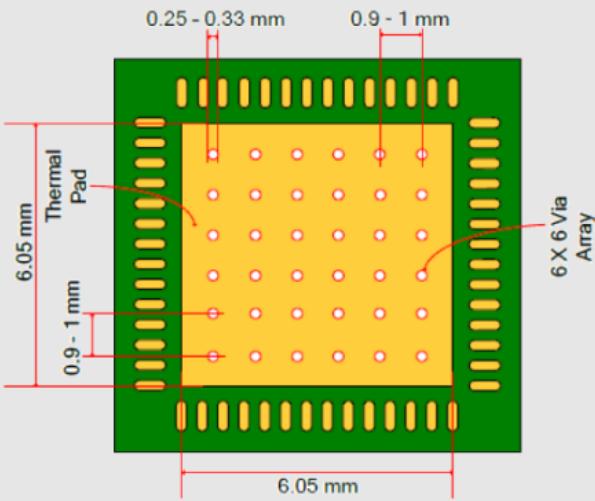
Flip-Chip Die-to-Die Interconnect

I conducted a simulation of the Die-to-Die Connection on interposers within flip-chip technology using Ansys HFSS. In this simulation, I employed Ansys HFSS to model and analyze the intricate electromagnetic behavior of the interposer's connections between semiconductor dies. This allowed me to assess signal integrity, impedance matching, and electrical performance, ensuring the reliable operation of the multi-chip module.

Bump and Micro-Via RLC Modeling

I employed RLC modeling using de-embedding methods to analyze and simulate the electrical behavior of bumps and micro-vias in my interconnect designs. Utilizing Resistor (R), Inductor (L), and Capacitor (C) elements, I accounted for their electrical resistance, inductance, and capacitance properties. This provided me with the means to assess signal integrity, impedance matching, and electrical performance in the context of my more extensive electronic systems, like semiconductor packages or interconnecting components. For more details you can click [here](#).

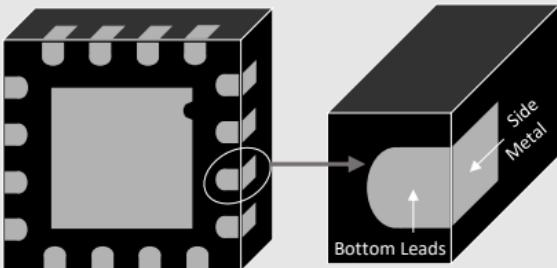




IC QFN Packaging

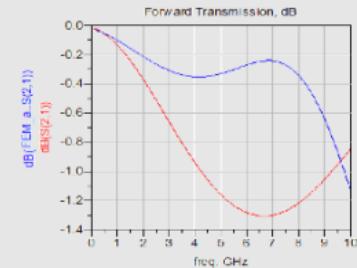
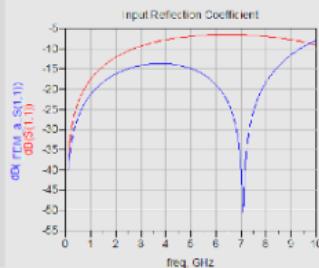
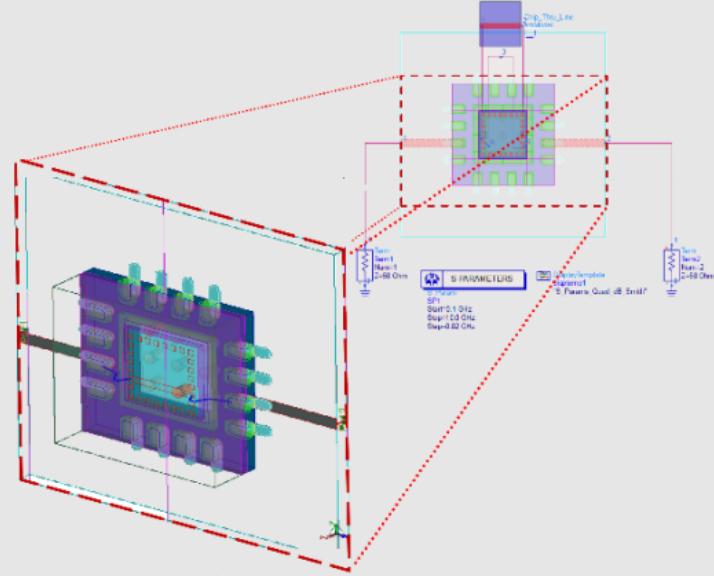
QFN (Quad Flat No-Lead) IC packaging is a compact and cost-effective semiconductor packaging technology characterized by its leadless design with metal pads on the bottom surface. QFN packages efficiently dissipate heat, making them suitable for power-hungry ICs, and their small footprint is ideal for space-constrained applications. These packages are widely used in various industries, including consumer electronics, telecommunications, and automotive, for devices such as microcontrollers, power management ICs, and RF components, simplifying the soldering process and reducing manufacturing costs.

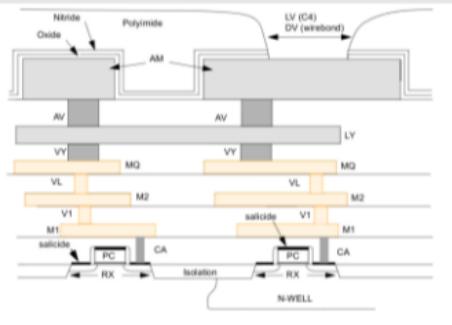
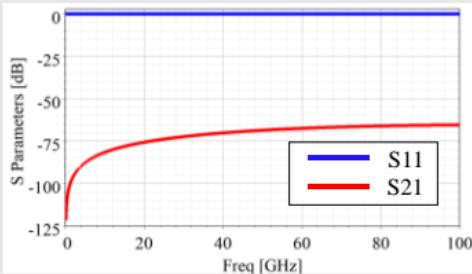
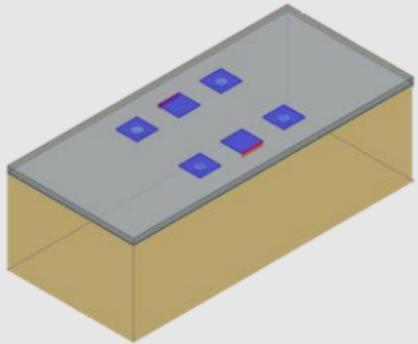
Standard Lead Design



Design QFN Package

I designed a QFN IC package optimized for microwave applications and conducted ADS simulations spanning 0 to 10 GHz to assess its performance. The package was meticulously designed for signal integrity, minimal parasitics, and effective heat dissipation, making it ideal for high-frequency microwave applications. These ADS simulations ensured its suitability for modern microwave systems.



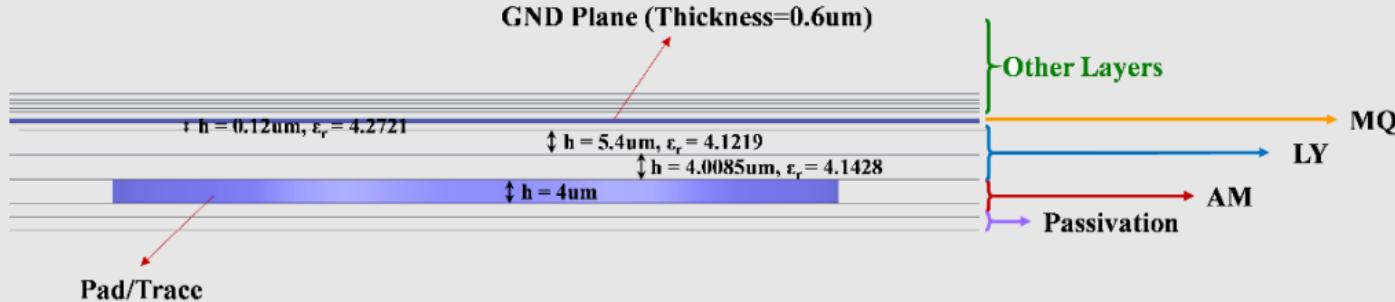
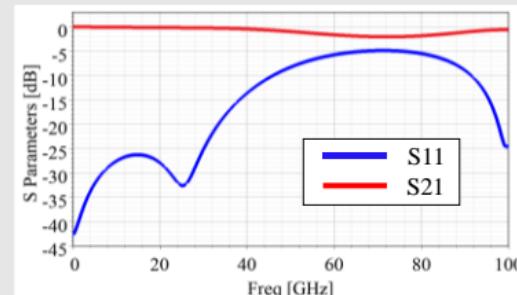
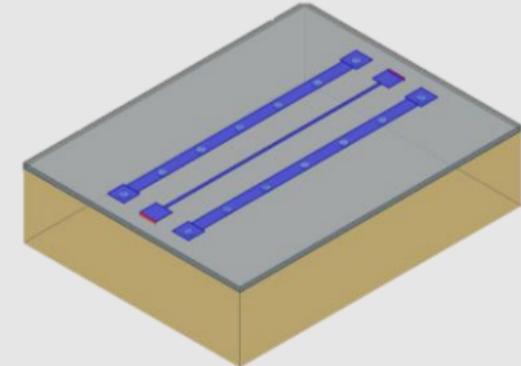


The Most Useful Structure in High-Speed Interconnections

The pad-microstrip trace-pad structure in integrated circuits (ICs) is a fundamental configuration crucial for high-frequency applications. It consists of signal pads on the IC die connected to microstrip transmission lines on the PCB or package substrate, followed by another set of signal pads. This design ensures controlled impedance, minimizing signal reflections and impedance mismatches, which is vital for preserving signal integrity in high-frequency environments. Additionally, it reduces electromagnetic interference (EMI) emissions, minimizes ground bounce effects, facilitates impedance matching, and ensures consistent signal propagation delay, making it indispensable for reliable and efficient high-frequency circuit operation, including RF communication, microwave devices, and high-speed digital systems.

Analysis of the Structure

I simulated this structure using Ansys HFSS software and analyzed it using de-embedding methods. The details of the study work will be explained on the following page.



T-type L-2L De-Embedding Method for On-Wafer T-model Transmission Line Network

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Abstract— This paper presents an extensive evaluation for a new type of the L-2L de-embedding method applied to on-chip de-embedding. We derive analytical formulas to discuss and verify the accuracy of the improved and extended method called the T-type L-2L de-embedding. The case study structure to apply the new method consists of a microstrip line combined with two left- and right-side pads. For the simulation of the structures, HFSS 3D electromagnetic (EM) simulator is used. The results show that the T-type L-2L exhibits better accuracy compared with the other on-wafer de-embedding methods for a device under test (DUT).

Key words— L-2L de-embedding, IC pad, Microstrip line, S-Parameters, Device Under Test (DUT).

I. INTRODUCTION

To obtain the actual characteristics of a DUT, the parasitic effects of the fixtures and on-wafer interconnects must be removed using a de-embedding method. Today, for reliable measurements of circuits in the silicon-integrated technology for millimeter and sub-millimeter wave frequencies no solutions are provided except the de-embedding methods [1]. To extract S-parameters of a DUT, the de-embedding methods generate emendations of the passive structures and active circuits in the millimeter and sub-millimeter frequencies range. Thus, a de-embedding step must be performed to derive the intrinsic parameters of the DUT.

The frequency de-embedding methods are classified into three types according to their de-embedding performance [2]. Cascaded Matrix Based Model (CMBM), Lumped Equivalent Circuit Model (LECM), and Cascaded Matrix with Lumped Equivalent Models (CMLEM). In the CMBM, the fixtures and interconnect parasitics are calculated differently, and the mathematical operations on each test structure are performed to obtain the DUT characterization. These methods are accurate in de-embed large-scale structures (compared to the wavelengths of $\lambda_{max} > 0.1\lambda$) and long transmission lines. For this class of de-embedding methods, the standard Thru-Reflect-Line (TRL) [3], Short-Open-Load-Thru (SOLT) [4], and 2x-Thru [5] de-embedding methods can be mentioned. Using this class of methods at the IC level is costly due to space limitations [1]. The second and third classes of de-embedding methods are suitable for IC-level structures and are called wafer-level de-embedding [1]. These methods are used to de-embed the DUT with lengths very small compared to the considered wavelength. The LECM methods are very simple compared to the other de-embedding methods and are utilized for low-frequency ranges. The Short (S) [6] and Open-Short (OS) methods [7] are among this categorization. The CMLEM methods cost more than LECM methods because they cover a much higher frequency range. For the CMLEM class, L_1L_2 [8]

and the n-type L-2L [9-13] de-embedding methods can be mentioned. The method is revised to decrease its sensitivity to measurement errors for the on-chip de-embedding [9]. The performance of various interconnects with different dielectric materials on glass was evaluated in [10]. The [11] validates an L-2L de-embedding for TMW RF characterization up to 50GHz with varying TMW structures. In [12] utilized the L-2L de-embedding method to enhance signal integrity for the flip-chip structure on a heterogeneous silicon interposer surface. L-2L de-embedding was used for characterization in the 40-170 GHz frequency range. However, the n-type L-2L method is compatible with the RAW device (not de-embedded), which is considered a s-model two-port network. The authors in [13] have presented the methods to apply the L-2L method based on the model of the pads (fixtures), x-type, T-type, and double T-type. The methodologies of [13] to apply L-2L are complicated. In this paper, we propose a simple L-2L de-embedding method proportionate to the RAW devices, which is considered as a T-model network. We call the method, the T-type L-2L method. The validity of this method is compared with the n-type L-2L method and ANSYS HFSS simulated DUT.

The structure of this paper is followed as: The detail of the RAW device is discussed in Section II. Section III describes the conventional wafer-level de-embedding. The implementation and methodology of T-type L-2L de-embedding are discussed in Section IV. Section V presents the final conclusion.

II. STRUCTURE DETAILS

The largest dimensions of discontinuity structures to employ the on-wafer de-embedding methods must be much smaller than the considered wavelength [1], this means that these structures can be modeled as lumped elements. The rule of thumb from empirical tests states that a lumped element circuit representation holds true as long as the wavelength λ at the highest frequency f of interest remains very large to the structure's physical size Length (e.g., Length $< \lambda/20$). The wavelength in a specific medium of electromagnetic wave is related to its frequency, effective permittivity of the medium ϵ_{eff} , and the free-space light velocity $c_0 \approx 2.998 \times 10^8 \text{ m/s}$ by the well-known formula

$$\lambda = \frac{c_0}{f\epsilon_{eff}}$$

A material with a high permittivity polarizes more in response to an applied electric field than a material with a low permittivity, thereby storing more energy in the material. The difference is that ϵ_{eff} is measured in a non-homogeneous material (a mixture of different materials having different relative permittivities ϵ_r). Because in the microstrip

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This paper presents an extensive evaluation for a new type of the L-2L de-embedding method applied to on-chip de-embedding. We derive analytical formulas to discuss and verify the accuracy of the improved and extended method called the T-type L-2L de-embedding. The case study structure to apply the new method consists of a microstrip line combined with two left- and right-side pads. For the simulation of the structures, HFSS 3D electromagnetic (EM) simulator is used. The results show that the T-type L-2L exhibits better accuracy compared with the other on-wafer de-embedding methods for a device under test (DUT).

The method

To obtain the actual characteristics of a DUT, the parasitic effects of the fixtures and on-wafer interconnects must be removed using a de-embedding method. Today, for reliable measurements of circuits in the silicon-integrated technology for millimeter and sub-millimeter wave frequencies no solutions are provided except the de-embedding methods. To extract S-parameters of a DUT, the de-embedding methods generate emendations of the passive structures and active circuits in the millimeter and sub-millimeter frequencies range. Thus, a de-embedding step must be performed to derive the intrinsic parameters of the DUT. For more details click [here](#).

2X-Thru De-Embedding Method Using Time Domain Impedance Response for S-Parameter Characterization of DUT in Broadband PCB

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Abstract—This article introduces a unique application of the 2X-Thru de-embedding method, where it utilizes the impedance response of a structure—deviating from its conventional usage. The method is employed to mitigate the influence of Sub-Miniature version A (SMA) connectors in broadband printed circuit board (PCB) systems. Two 50Ω microstrip lines are created on RO3003 laminates, accompanied by 1092-03A-6 edge-type 2.92mm female end launch connectors serving as error boxes on the designated transmission lines (test structures). To simulate these structures, the HFSS 3D electromagnetic (EM) simulator, renowned for its accuracy in real-world comparisons, is utilized. The method presents a sequential S-parameter model for the structure formed by the SMA connectors and the transmission lines. This enables discontinuous fixture S-parameter extraction up to 40 GHz. The precision of the method's extracted S-parameters is validated by comparing the obtained results from the microstrip line trace simulation with the outcomes of the de-embedding method applied to the test structures. The error between the de-embedded trace and the simulated one is minimal, measuring under 0.3 dB.

Keywords—2X-Thru, de-embedding method, SMA connector, printed circuit board (PCB), microstrip line, scattering

1 INTRODUCTION

To achieve accurate determination of the S-parameters of a Device Under Test (DUT) operating in the millimeter and sub-millimeter frequency ranges, de-embedding methods are employed. These methods serve to rectify the impact of passive structures and active circuits introduced by fixtures and interconnect parasitics [1]. The de-embedding process is essential to extract the intrinsic parameters of the DUT. De-embedding methods are categorized into three primary classifications, each defined by its distinct performance attributes: methods operating in the frequency domain, methods within the time domain, and methods that combine both frequency and time domains.

De-embedding methods in the frequency domain are classified into three principal categories, each delineated by its performance characteristics [2]: Cascaded Matrix-Based Model (CMBM), Lumped Equivalent Circuit Model (LECM), and Cascaded Matrix with Lumped Equivalent Models (CMLEM).

CMBM category involves a meticulous separation of the effects attributed to fixtures and interconnect parasitics. Through mathematical operations performed on measurements from each distinct test structure, the characterization of the DUT is deduced. CMBM methods exhibit pronounced accuracy when dealing with expansive structures, where the maximum structure length (L_{max}) is

greater than 0.1 times the wavelength (λ) [2]. Examples of methods in this category include the standard Thru-Reflect-Line (TRL) [3–6], Short-Open-Load-Thru (SOLT) [6, 7], and Line-Reflect-Match (LRM) [5, 6] de-embedding methods. However, implementing CMBM methods at the integrated circuit (IC) level can be costly due to space limitations [1].

LECM methods are well-suited for IC-level structures and are employed in advanced de-embedding [1]. LECM methods are simpler compared to other de-embedding methods and are particularly useful for low-frequency ranges. Illustrative methods within this classification encompass Open (O) and Open-Short (OS) [6–10] approaches.

CMLEM category encompasses more intricate methods capable of spanning a broader frequency spectrum. While CMLEM methods entail higher costs relative to LECM counterparts, they are adept at de-embedding DUTs with dimensions significantly smaller than the wavelengths of interest. Examples of CMLEM methods comprise L₁L₂ [11] and the x-type L-2L de-embedding techniques [12–15].

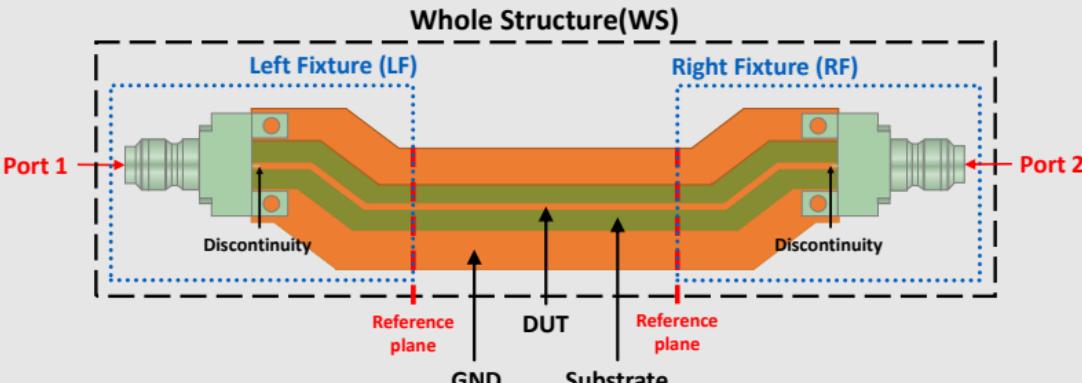
The subsequent de-embedding category pertains to time domain methods; this classification is known as “time gating” [16]. Time-domain gating involves the precise definition of a specific time window during which the objective is to exclude undesired responses, subsequently presenting the refined outcome in the frequency domain. Conceptually, gating can be envisioned as the multiplication of the time-domain response by a mathematical function, which takes on a value of one exclusively within the designated region of interest and remains at zero outside this interval. The gated time-domain function is then subject to a forward transformation, effectively rendering the frequency response while excluding the influence of other time domain responses [16].

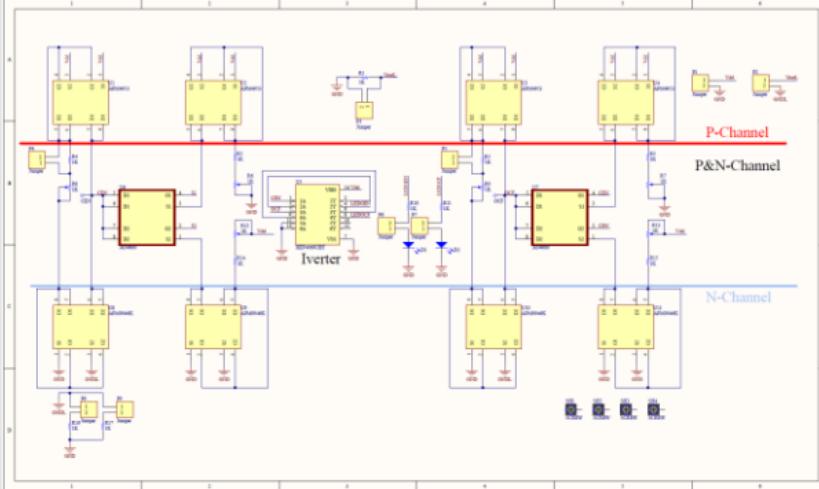
The third category of de-embedding methods represents a convergence of two distinct realms: the time domain and the frequency domain. In these methods, the underlying principle involves leveraging the response characteristics, specifically the S-parameters, of de-embedding structures. These structures are designed to facilitate the extraction of the Device Under Test (DUT), which is the component or system of interest. In this approach, both the time domain and frequency domain aspects are integrated. The frequency domain elements draw from the first category of de-embedding methods, while the focus lies on analyzing the response characteristics of structures at various frequencies. On the other hand, the time domain aspect borrows from the second category, which involves time-gating techniques to isolate relevant responses while excluding unwanted ones.

2X-Thru De-Embedding Method Using Time Domain Impedance

Response for S-Parameter Characterization of DUT in Broadband PCB

This article introduces a unique application of the 2X-Thru de-embedding method, where it utilizes the impedance response of a structure—deviating from its conventional usage. The method is employed to mitigate the influence of Sub-Miniature version A (SMA) connectors in broadband printed circuit board (PCB) systems. For this purpose, two 50Ω microstrip lines are created on RO3003 laminates, accompanied by 1092-03A-6 edge-type 2.92mm female end launch connectors serving as error boxes on the designated transmission lines (test structures). To simulate these structures, the HFSS 3D electromagnetic (EM) simulator, renowned for its accuracy in real-world comparisons, is utilized. The method presents a sequential S-parameter model for the structure formed by the SMA connectors and the transmission lines. This enables discontinuous fixture S-parameter extraction up to 40 GHz. The precision of the method's extracted S-parameters is validated by comparing the obtained results from the microstrip line trace simulation with the outcomes of the de-embedding method applied to the test structures. The error between the de-embedded trace and the simulated one is minimal, measuring under 0.3 dB. For more details click [here](#).

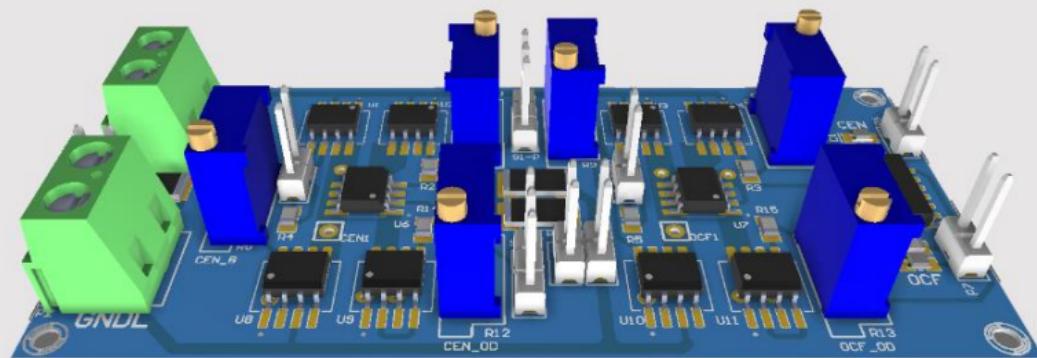
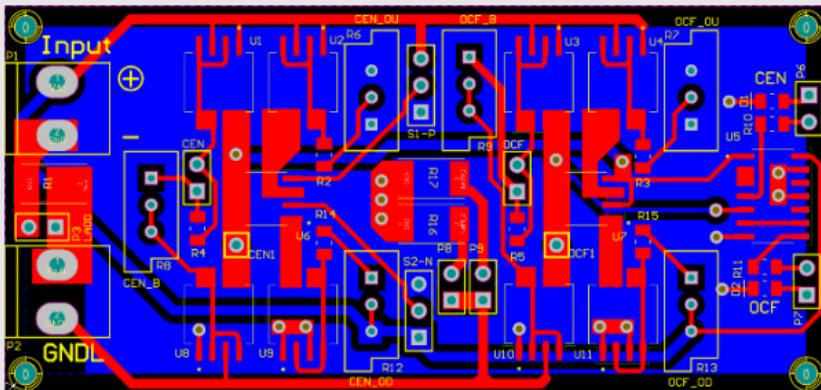


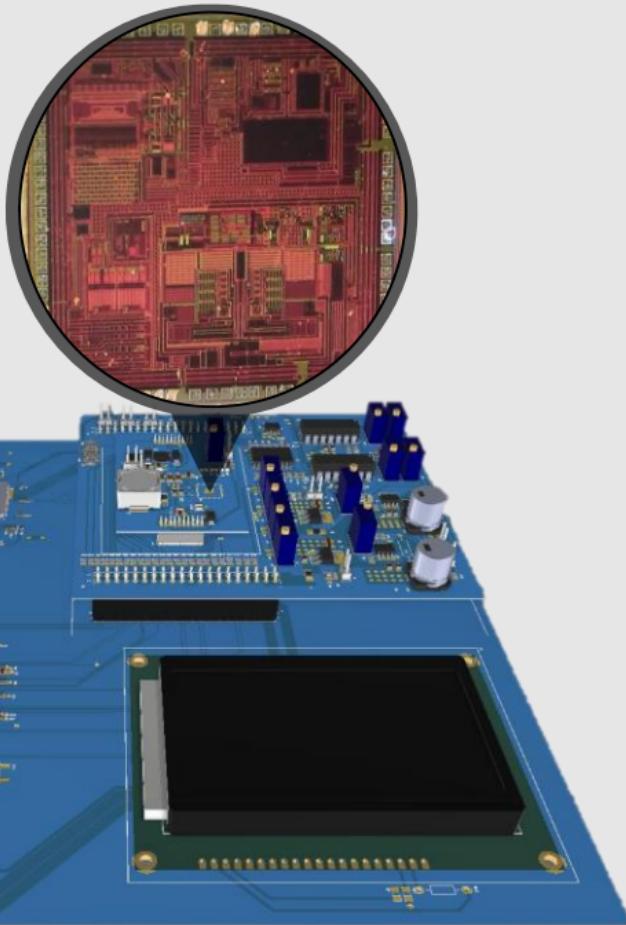


Low Power Overcurrent Detection

The overcurrent detection circuit safeguards electrical systems by monitoring current flow. Key components include a current detector, amplification stage, threshold setting, comparator, and tripping mechanism. When current exceeds the threshold, it triggers actions like circuit disconnection to prevent damage and ensure safety. This circuit is used in circuit breakers, low power device, power supplies, and battery management.

The overcurrent protection circuit is equipped with 20 transistors, carefully designed to fulfill all specified conditions and requirements. These transistors play a crucial role in the circuit's operation, ensuring that it can effectively detect and respond to overcurrent situations, safeguarding the connected electrical systems or devices.





Deep Brain Stimulation

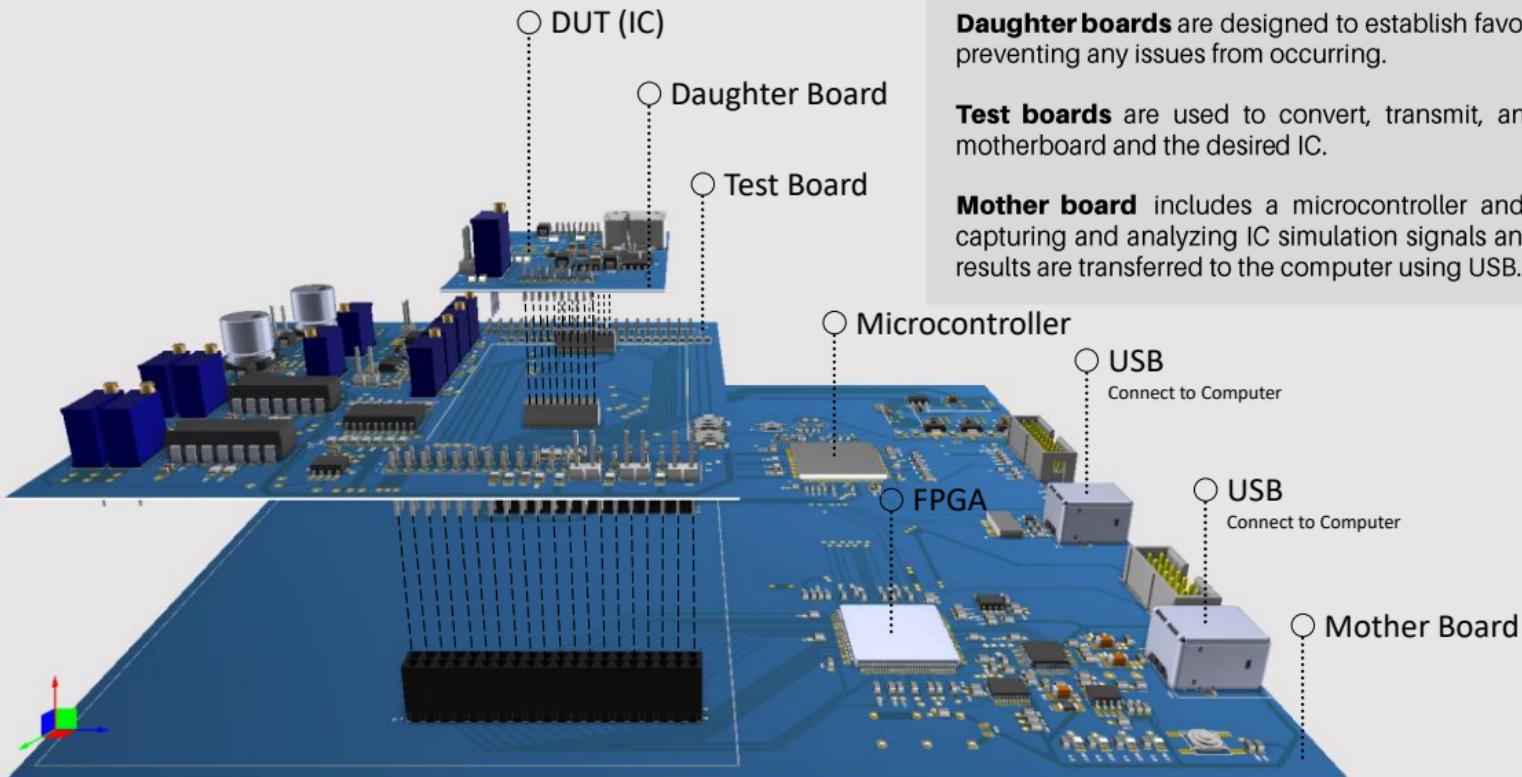
Deep Brain Stimulation (DBS) is a therapeutic technique involving the use of an implantable medical device to alleviate the symptoms of certain neurological disorders, including Parkinson's disease. It works by delivering electrical stimulation to specific areas of the brain through electrodes, effectively regulating abnormal neural activity. This treatment can help manage symptoms such as tremors, rigidity, and bradykinesia (slowness of movement) in individuals with Parkinson's disease and related conditions. A part of the IC has been patented; you can click [here](#) for more information.

The project

The Deep Brain Stimulation (DBS) project was initiated to address the treatment of Parkinson's disease. This extensive undertaking was launched at Tehran University in 2018, led by a collaborative team comprising professors from the Faculty of Electrical, experts in metallurgy, and faculty members from Tarbiat Modares University and Sahand University. The team's ultimate objective was the development of an integrated circuit (IC) at the IC level to advance the DBS technology.

My Role in the Project

Due to limitations in our laboratory equipment for testing and measuring 5 diced ICs, we encountered difficulties in conducting IC tests. To address this challenge, I developed a platform (test boards) designed specifically for testing diced ICs. This platform allows us to assess the performance of diced ICs thoroughly by testing each of their individual components.



Test Boards

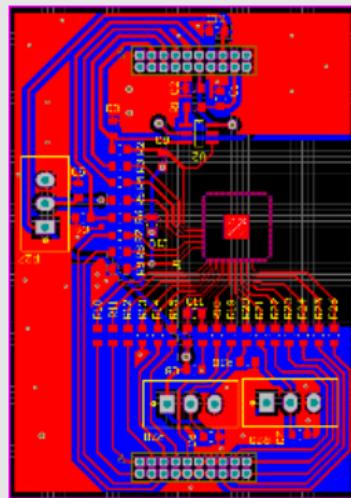
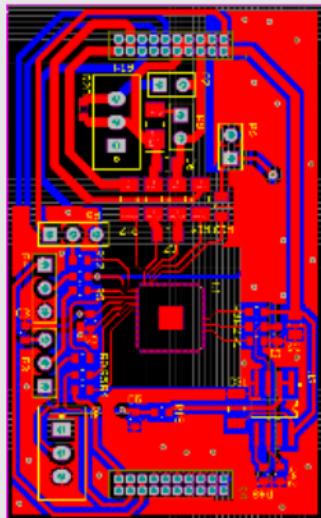
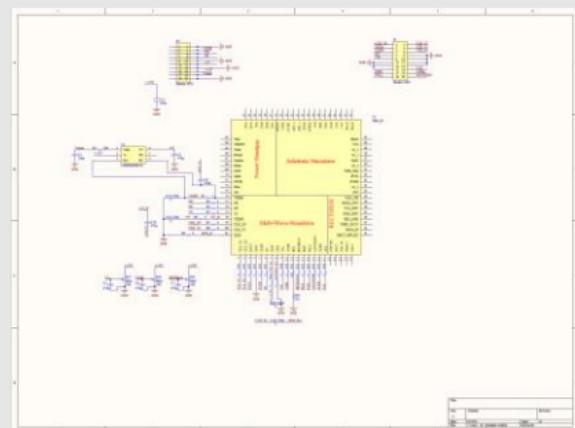
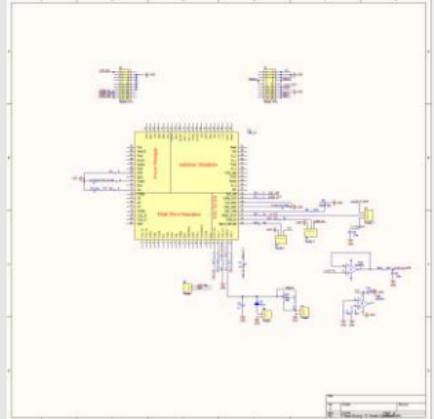
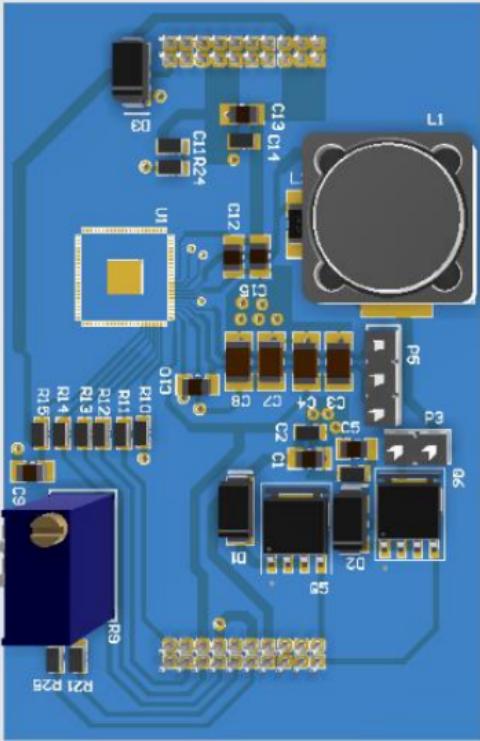
This substrate comprises several stacked electronic boards, with the diced IC positioned on the topmost one. These boards are defined as follows:

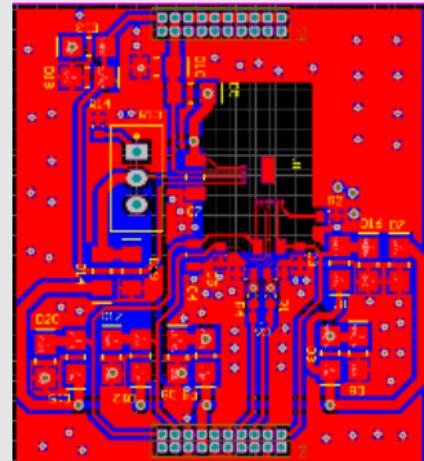
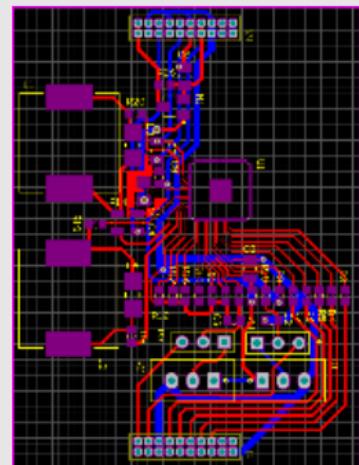
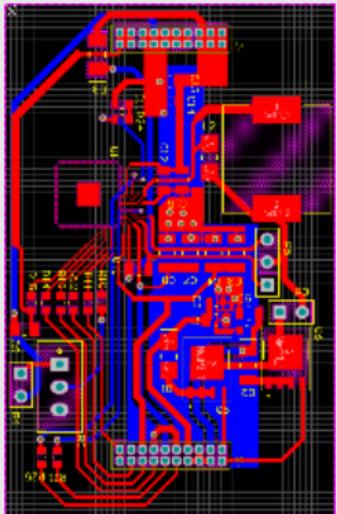
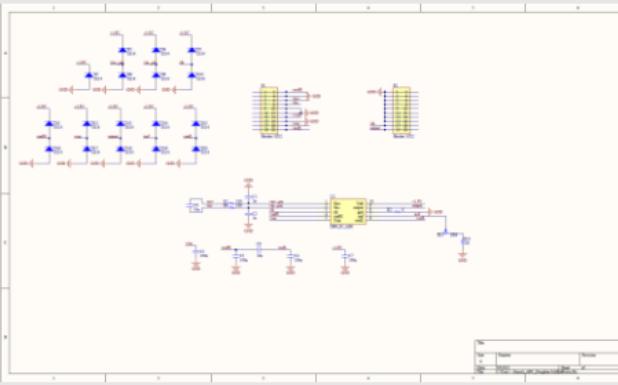
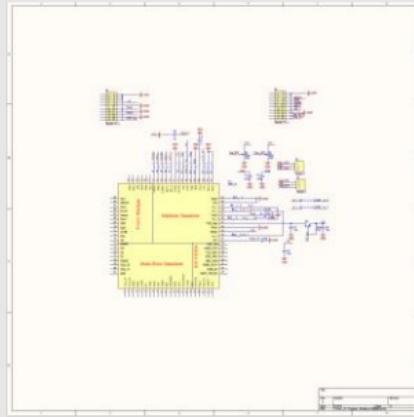
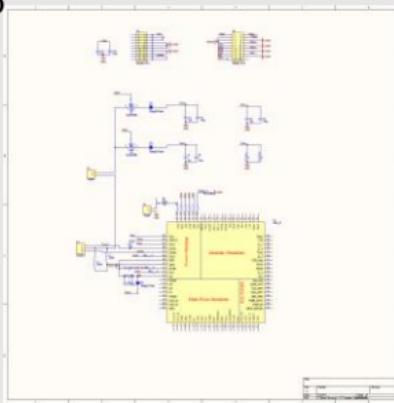
Daughterboards are designed to establish favorable working conditions for ICs, preventing any issues from occurring.

Test boards are used to convert, transmit, and receive signals between the motherboard and the desired IC.

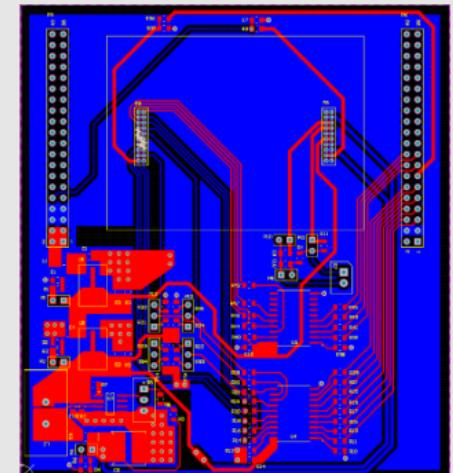
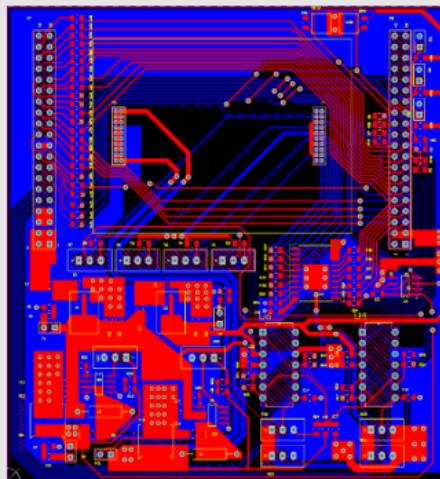
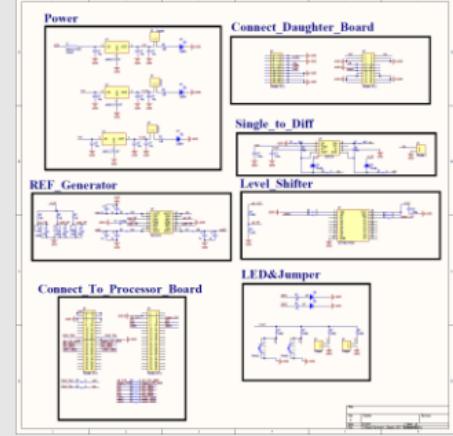
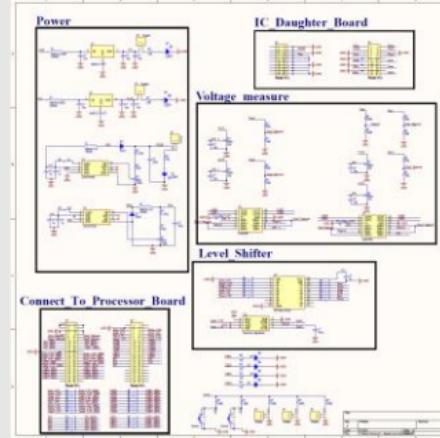
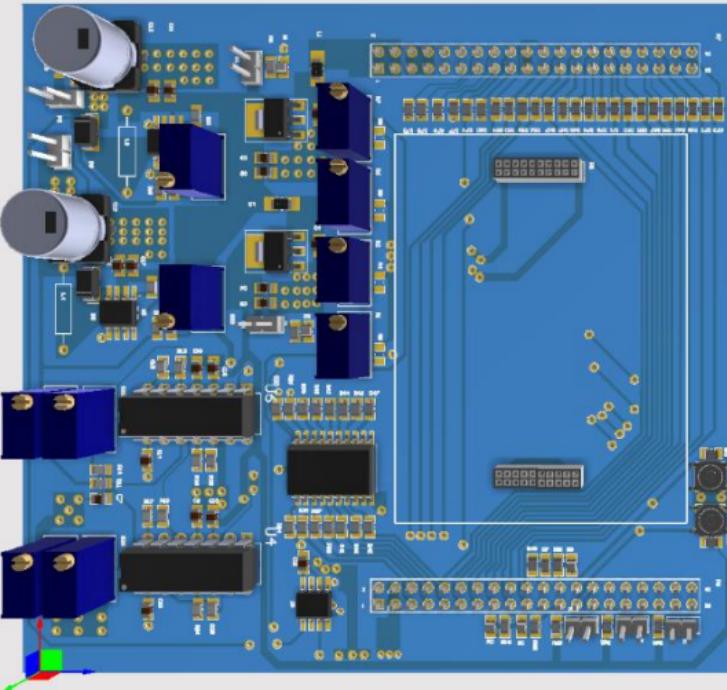
Mother board includes a microcontroller and an FPGA, which are used for capturing and analyzing IC simulation signals and response signals. The analysis results are transferred to the computer using USB.

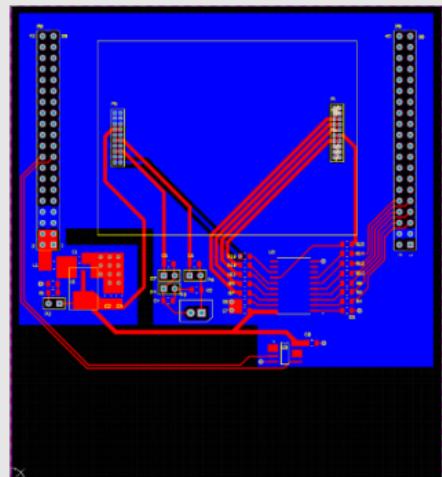
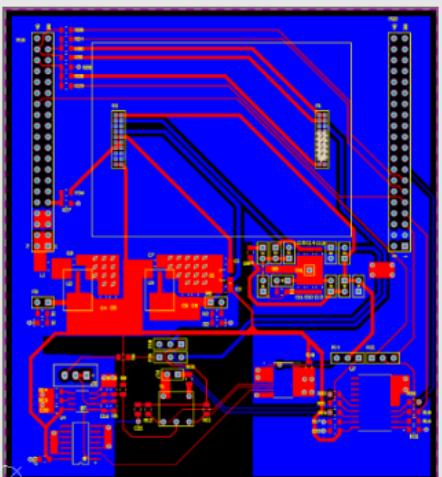
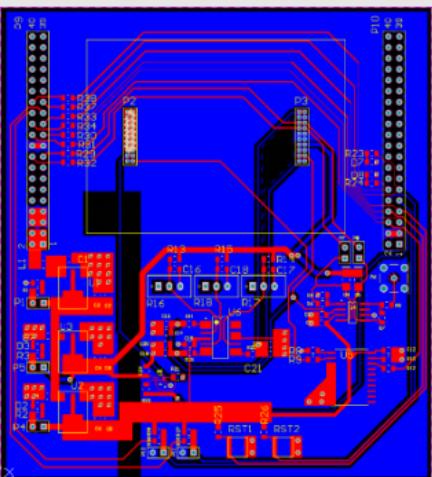
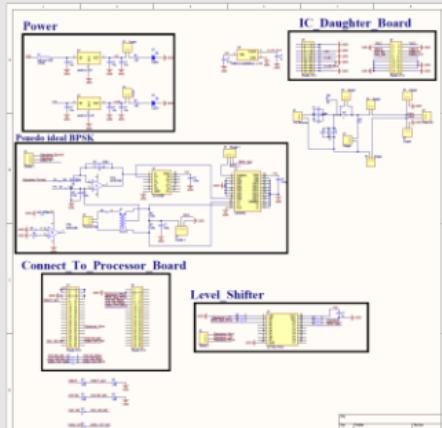
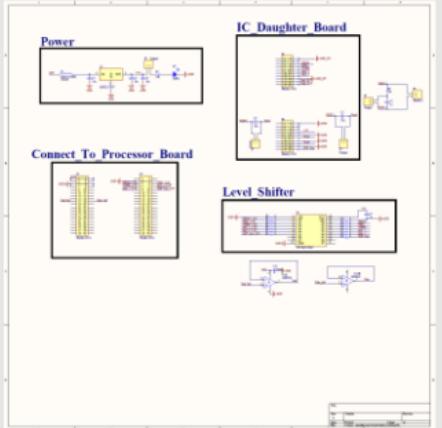
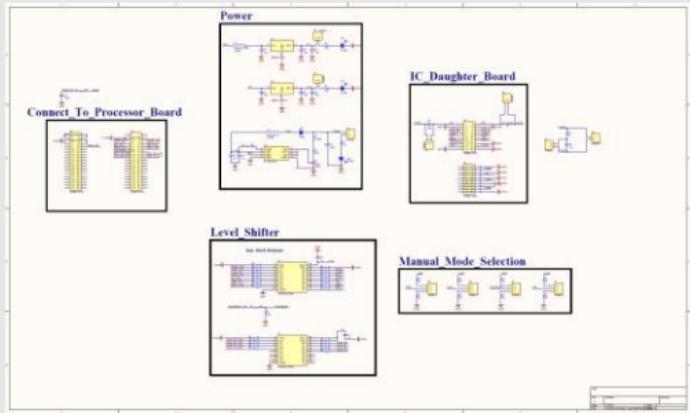
Daughter Boards



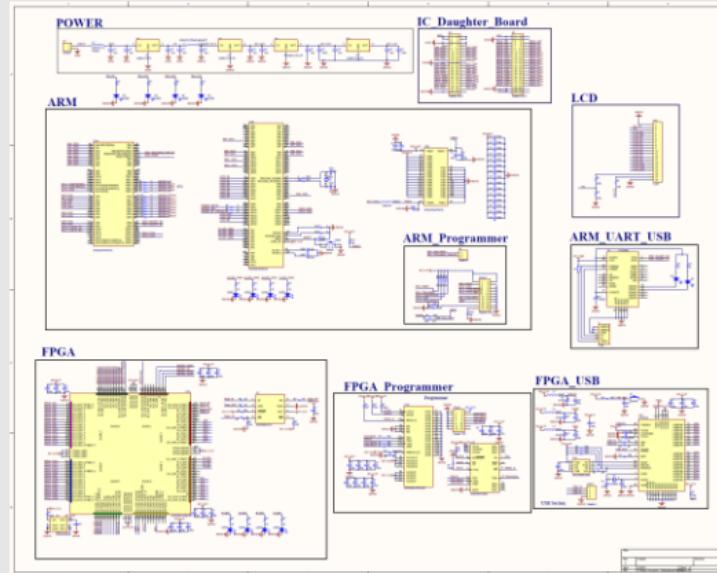
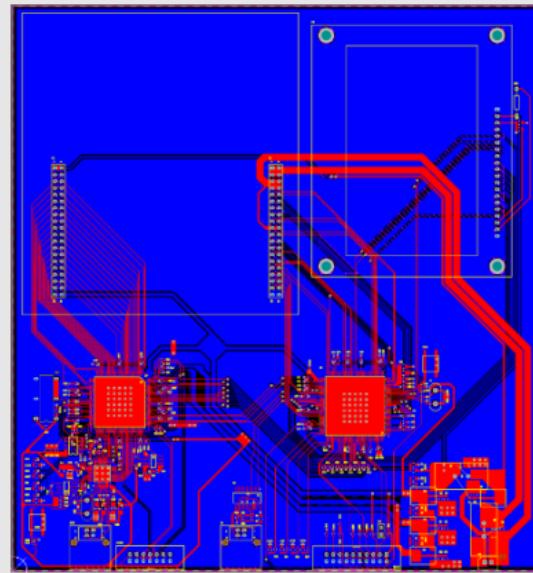
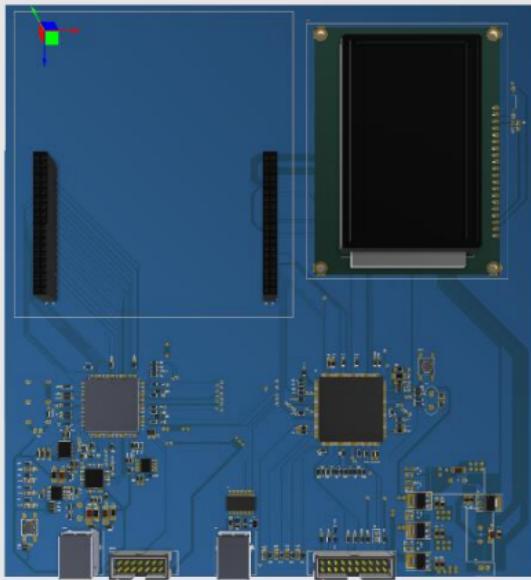


Test Boards





Mother Board



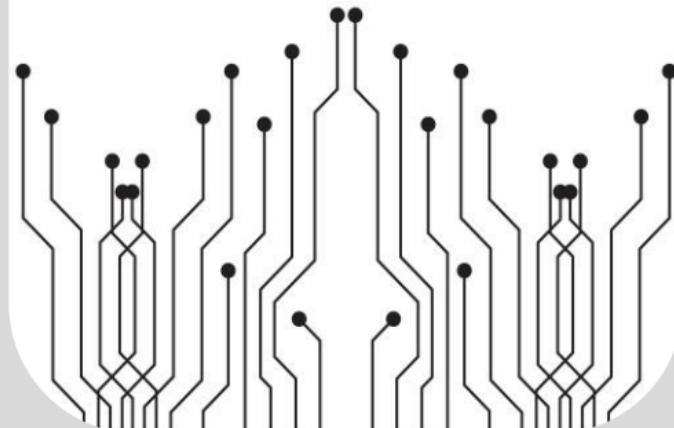
SEDNA COMPANY

2022-2023

PCB and Testing Checklist 21

Smart Thermostat 22

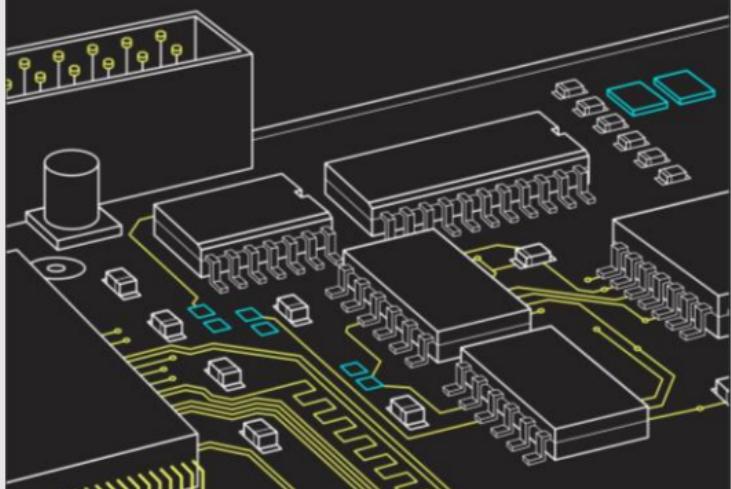
IOT Combi Boiler 24





The PCB Design Development Checklist

By: M. Seyedi



PCB and Testing Checklist

Checklists are essential tools in both the PCB design and testing phases of mass production. During the design phase, they help reduce errors, ensure compliance with industry standards, optimize costs, and enhance performance. In the testing phase, checklists play a vital role in quality assurance, functionality verification, fault identification, traceability, consistency, efficiency, documentation, and continuous improvement. By systematically guiding designers and testers, checklists contribute to the production of high-quality and reliable PCBs while streamlining processes and maintaining regulatory compliance.

SEDNA's Checklist

According to my review of this company's products, I identified significant issues related to hardware and testing, as well as problems with the output files from the final product for mass production. As a result, I created a checklist for the company to address these issues and prevent their recurrence. This checklist has since become an internal standard for the hardware design of the company's products. Items considered is based on following sections:

- PCB Specification
- PCB Check
- Design Check
- BoM Check
- Gerber Check
- Output Files
- Board Test before Sending Files for Mass Production
- Sample Board Test before Mass Production

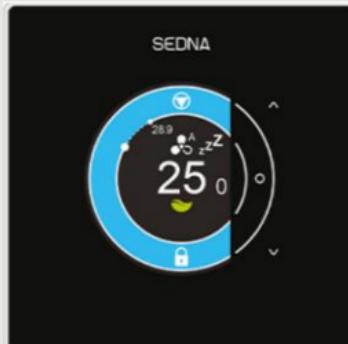
For more details you can click [here](#).



Telesto



Selena



Volkan



All-in-One-Eris

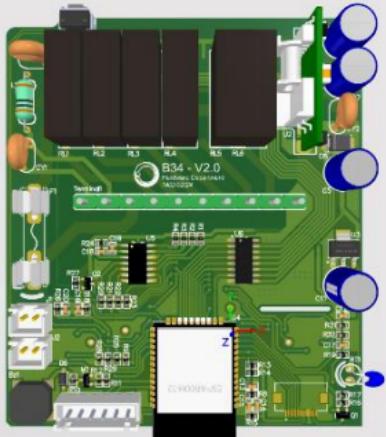
Smart Thermostat

Smart thermostats, with a delicate and high-tech design, are the SEDNA's air conditioning thermostat series. These products with a beautiful and modern appearance, as well as smart features, provides a wide range of functions for user. Moreover, containing different options and features, brings prosperity and comfort to consumers' everyday life.

These thermostats use MODBUS communication protocol. Hence, they can act as HMI for BLDC/induction or other motors' drives. As a result, using its own features and scenarios, it can control AC systems and evaporative coolers via the drive unit installed in them.

My Role in the Projects

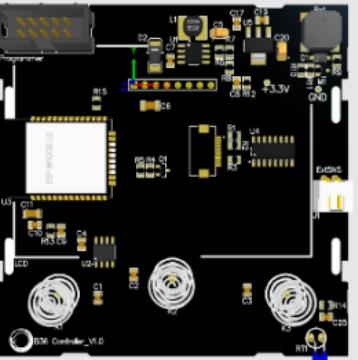
During my tenure at Sedna, a prominent player in Iran's thermostat industry, I had the privilege of spearheading the PCB design efforts for a range of cutting-edge smart thermostats integrated with IoT platforms. This experience allowed me to lead the design of several notable thermostat models, including [Telesto](#), [Volkan](#), [Selena](#), and [All-in-One-Eris](#) each of which embodied innovative technologies and advanced functionality to enhance user comfort and energy efficiency. These achievements underscored my commitment to delivering high-quality, forward-thinking solutions in the ever-evolving field of smart home automation.



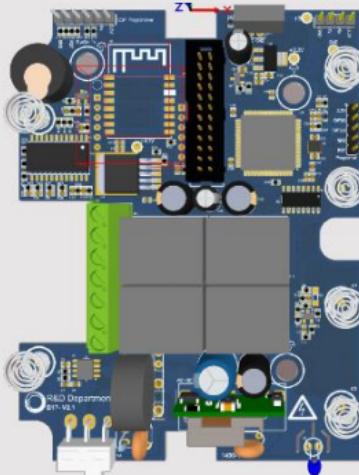
Telesto



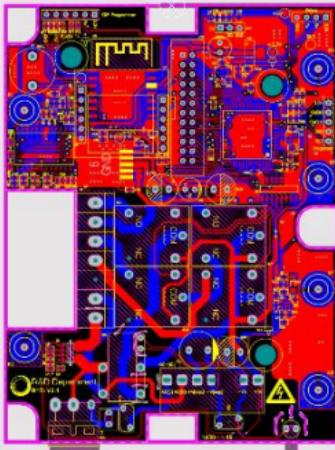
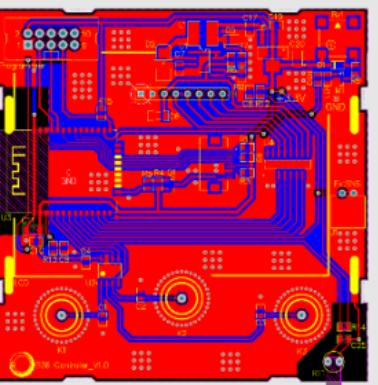
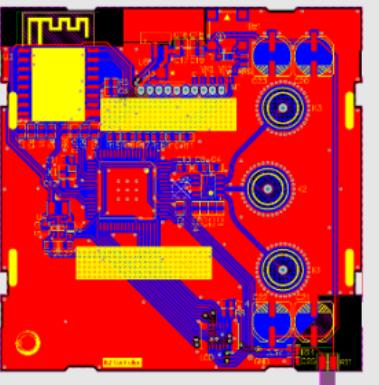
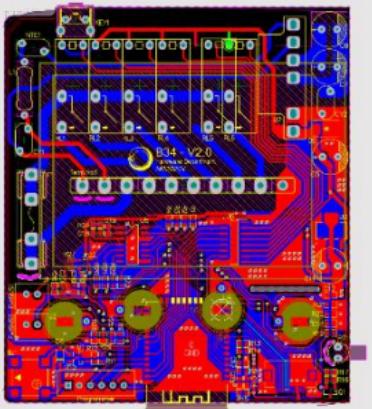
Volkan



Selena



All-in-One-Eris





IoT Combi Boiler

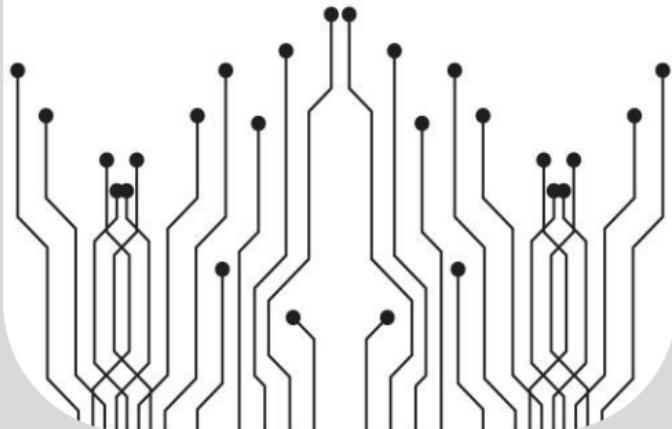
An IoT combi boiler is a modern heating system that combines a traditional combi boiler with Internet of Things technology. It offers remote monitoring and control through smartphone apps and web interfaces, enabling users to adjust heating settings, view energy usage, and receive maintenance alerts. These boilers optimize energy efficiency, predict maintenance needs, and integrate with smart home ecosystems, providing convenience, energy savings, and enhanced comfort. They collect data on heating patterns and offer insights for reducing energy consumption. IoT combi boilers are part of the growing trend toward connected and efficient home heating solutions. For more details you can click [here](#).

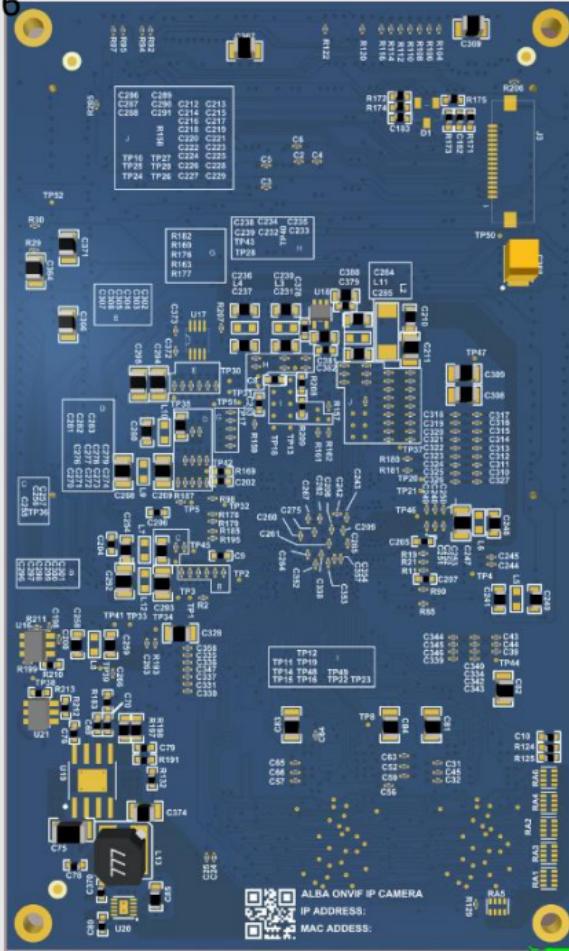


IMENARA COMPANY

2015-2017

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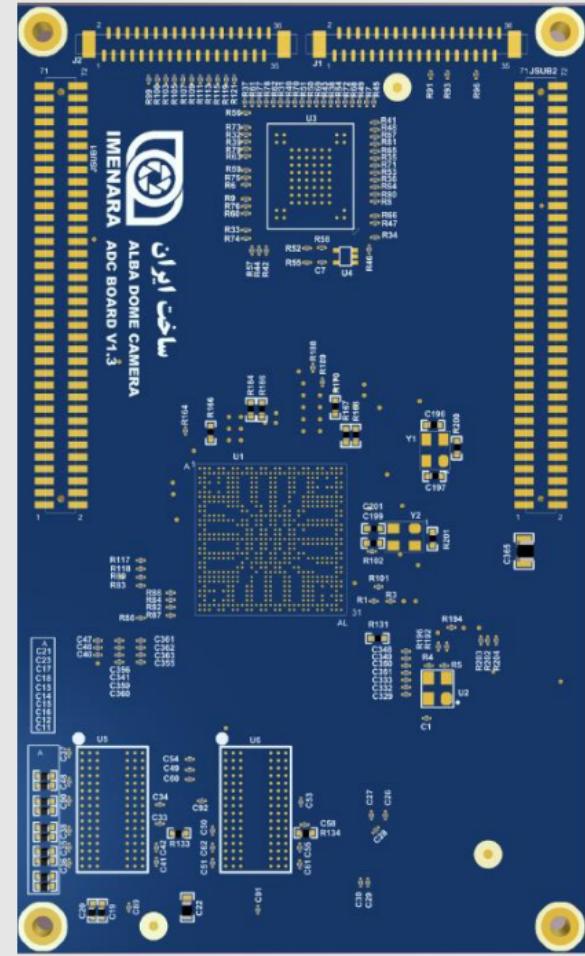


DSP in CCTV Camera

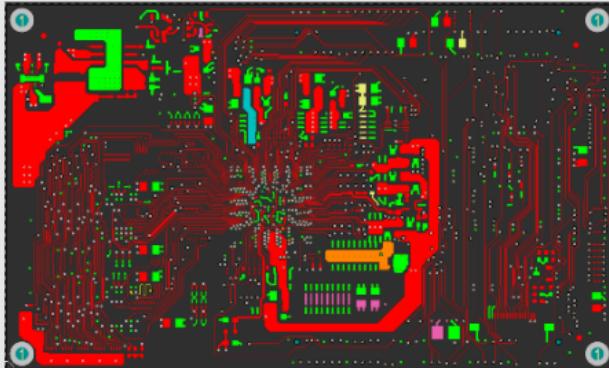
Digital Signal Processing (DSP) in cameras involves the application of various signal processing techniques to optimize image and video quality. It encompasses tasks like noise reduction, color correction, auto-focus, image stabilization, exposure control, face detection, HDR imaging, video processing, and low-light enhancement. DSP enhances the overall performance of digital cameras by ensuring cleaner, more vibrant images, advanced features, and creative possibilities for photographers and videographers.

DSP Chip PCB Design

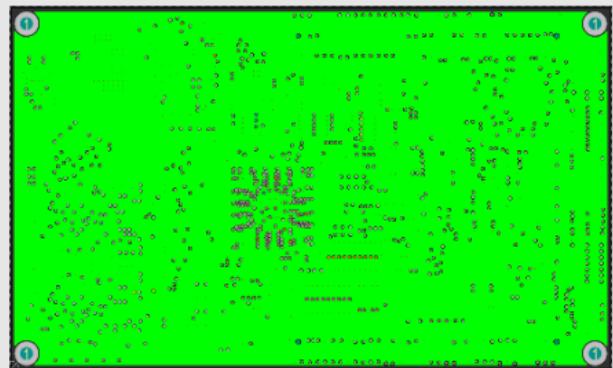
Designing a PCB layout for a DSP chip involves careful placement of components, attention to power distribution, signal integrity, and thermal considerations, while adhering to EMC/EMI compliance and grounding guidelines. When I undertook the task of designing a PCB for a DSP chip in the past, I adhered to routing and manufacturing constraints, maintained clear signal return paths, and diligently documented the process. Prototyping and iterative design became crucial steps for me to verify functionality and performance. This complex undertaking has now been completed, ensuring the reliable operation of the DSP chip within the electronic system.



27



Top



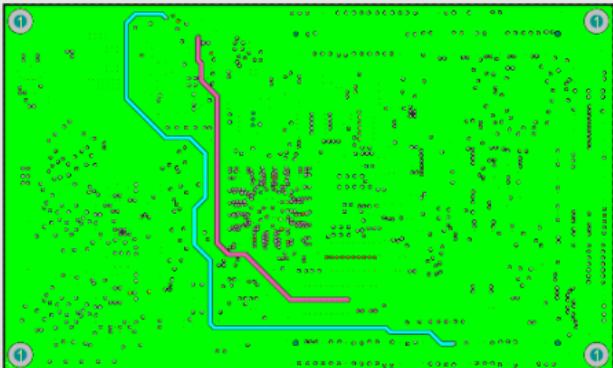
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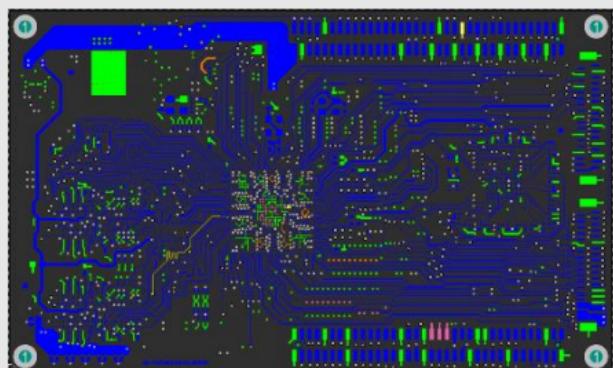
L3



L4



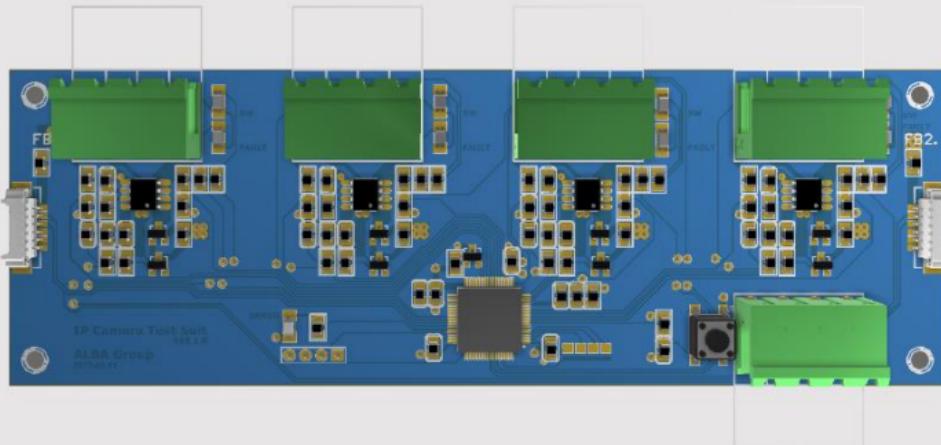
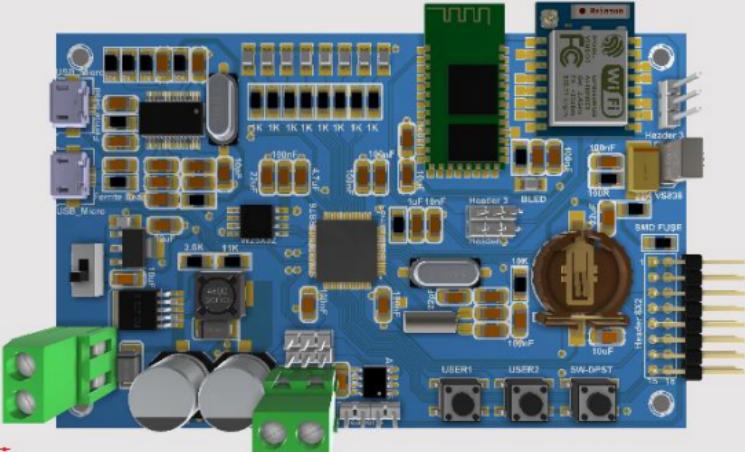
L5



Bottom

IOT CAMERA TEST ROOM





IoT Camera Test Room

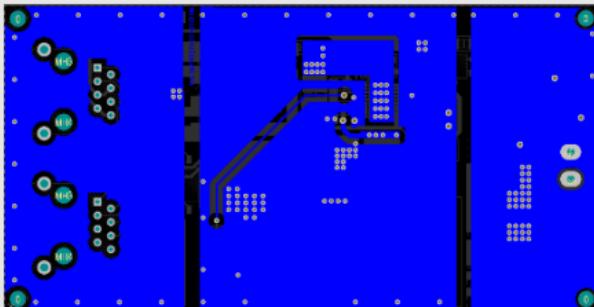
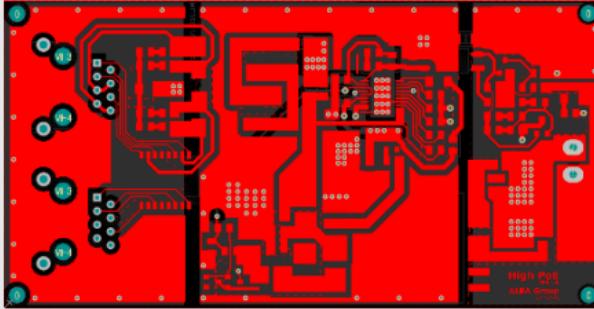
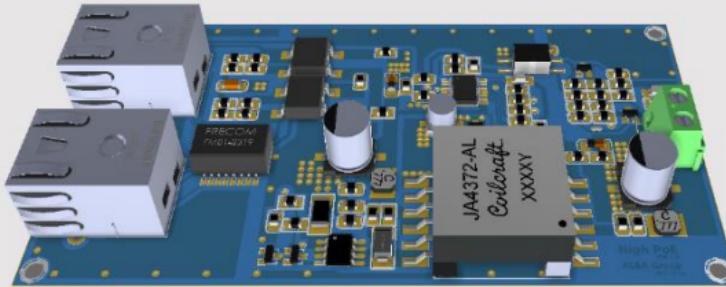
The IoT CCTV (Closed-Circuit Television) camera test room is a specialized facility designed for testing and quality assurance of Internet of Things (IoT) cameras used for surveillance and security purposes. These test rooms are essential in the development, calibration, and certification of IoT CCTV cameras to ensure their reliability, functionality, and compliance with industry standards.

Camera Testing Aspects

Camera testing involves several crucial aspects to ensure reliable performance. First, it requires maintaining a controlled environment, carefully regulating lighting, temperature, humidity, and background noise levels to guarantee consistent and accurate testing conditions. This controlled setting sets the foundation for rigorous evaluations, including lighting simulation, resolution and image quality assessments, field of view evaluations, and IR illumination testing. These assessments collectively gauge the camera's performance under various circumstances, ensuring it captures clear, accurate, and detailed images in different lighting conditions, wide areas without distortion, and low-light scenarios using infrared technology.

Comprehensive Evaluation

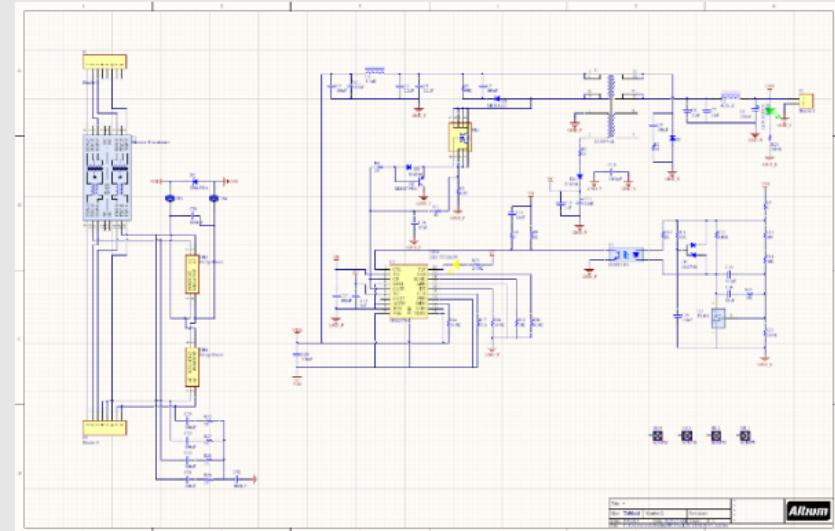
Camera testing encompasses network connectivity assessment, security analysis, compliance validation, and firmware/software evaluation. This ensures the camera's quality, security measures, industry alignment, and compatibility, with performance benchmarking for a comprehensive performance assessment.

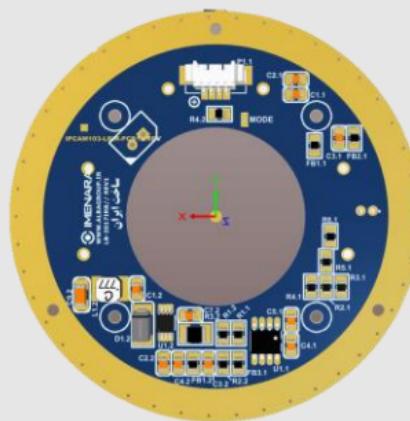
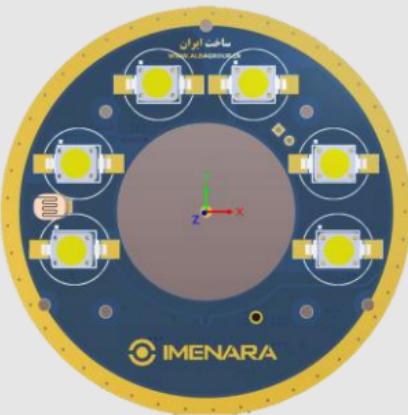


Power over Ethernet

Power over Ethernet (PoE) is a technology that sends both data and electrical power over the same Ethernet network cable. It's commonly used to power devices like IP cameras, phones, and access points, eliminating the need for separate power cables. PoE standards define power levels and safety features, and PoE devices negotiate power requirements when connected.

- ❖ PoE standards: IEEE 802.3af, IEEE 802.3at, and IEEE 802.3bt set power limits and voltage levels.
- ❖ Auto-negotiation ensures proper power delivery.
- ❖ Safety features prevent overloading and electrical issues.





Infrared light

Infrared light (IR) is light with a wavelength longer than what the human eye can see, making it invisible to us. It is emitted by all objects and can be used to determine their temperature. Infrared technology, initially developed for military night vision, is now widely used in devices like TV remotes and security cameras for nighttime surveillance.

How the IR works

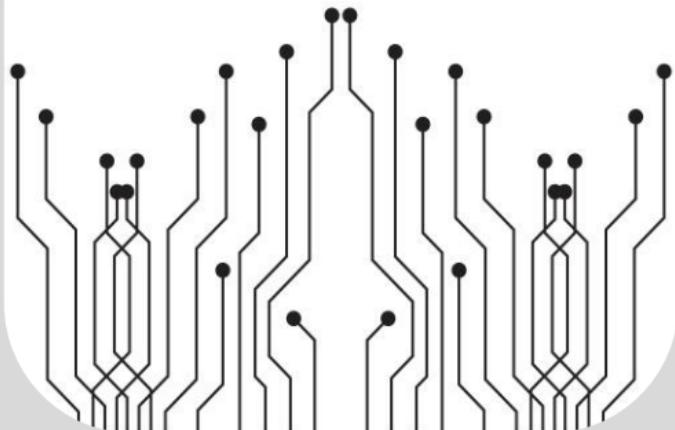
The IR security camera uses infrared light to capture images, even in low light or nighttime conditions. It detects thermal energy from objects and converts it into electronic images based on temperature. These cameras have evolved to provide high-quality images, with features like high pixel count (up to 76,800 pixels), interchangeable optics, auto and manual focus, rapid light adaptation, wide-angle coverage, and independent rotation systems for better visualization.

Sport Activity

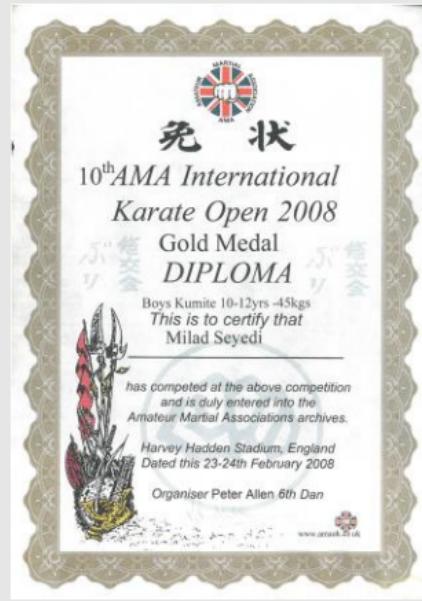
2008

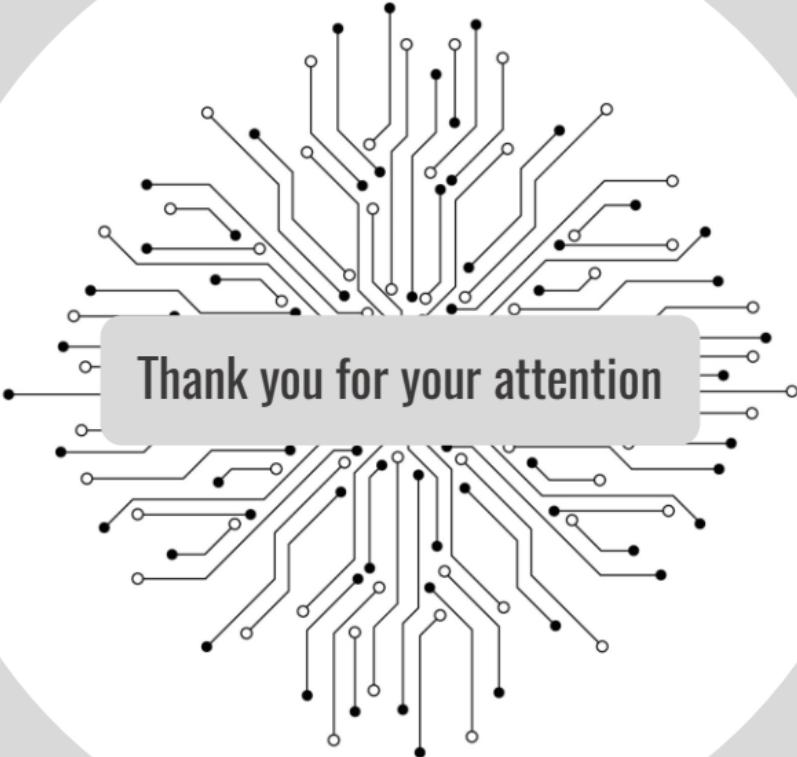
Gold Medalist at the England Karate World

Championships 33



Gold Medalist at the England Karate World Championships





Thank you for your attention