**Date: 13/09/2025 Timing: 9:30 am to 4:15 pm**

**Long Hour Design (LHD) – Digital Circuit Layouts in Microwind**

**Task:**

**Design and implement the following digital circuits using the Microwind Tool by creating their transistor-level layouts, simulating functionality, and verifying outputs: CO2, CO3**

1. 4-bit Full Adder
2. 8×1 Multiplexer
3. 1-bit Magnitude Comparator
4. 4-bit Serial-In Serial-Out (SISO) Register

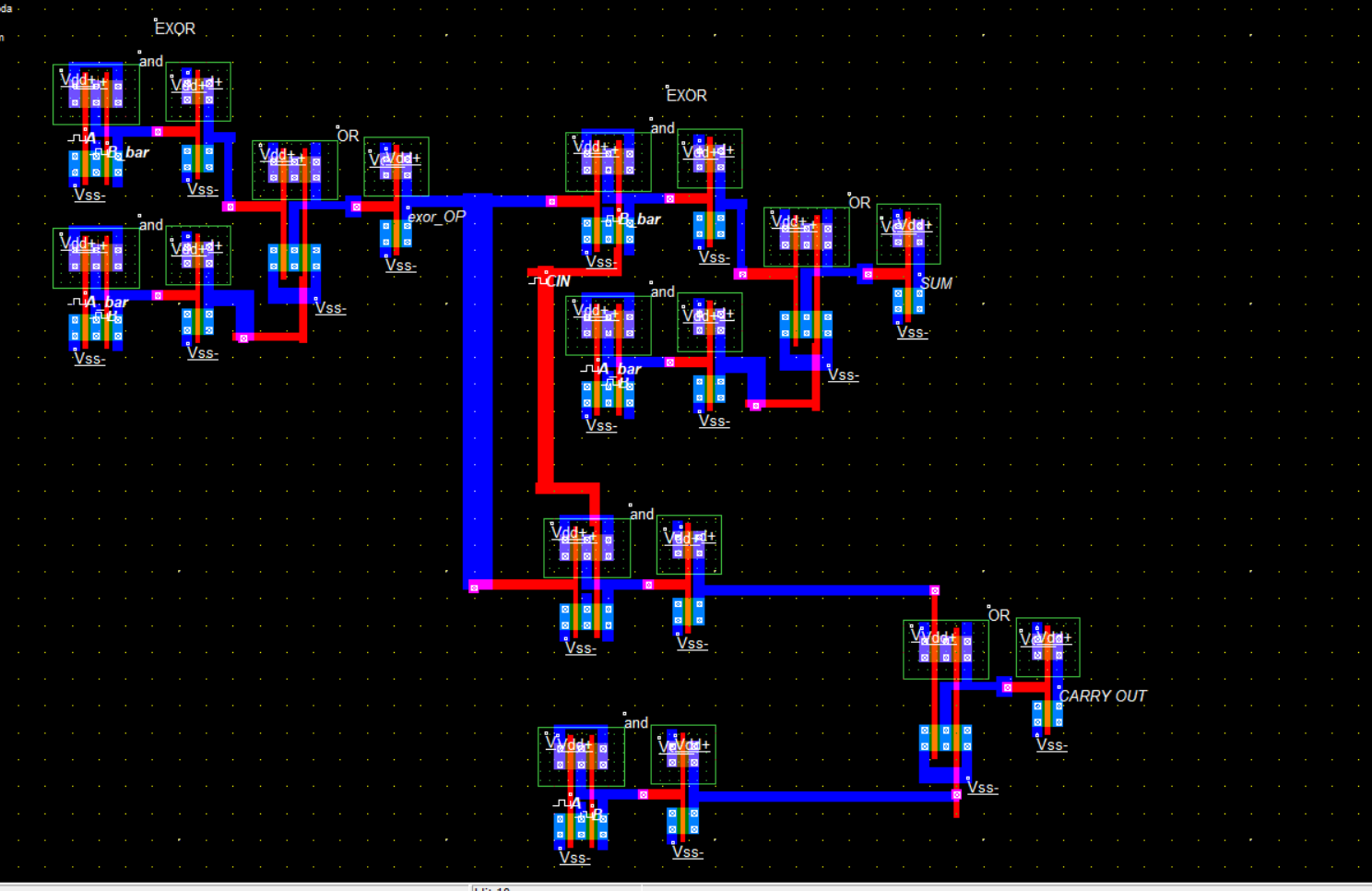
**Submission Requirements**

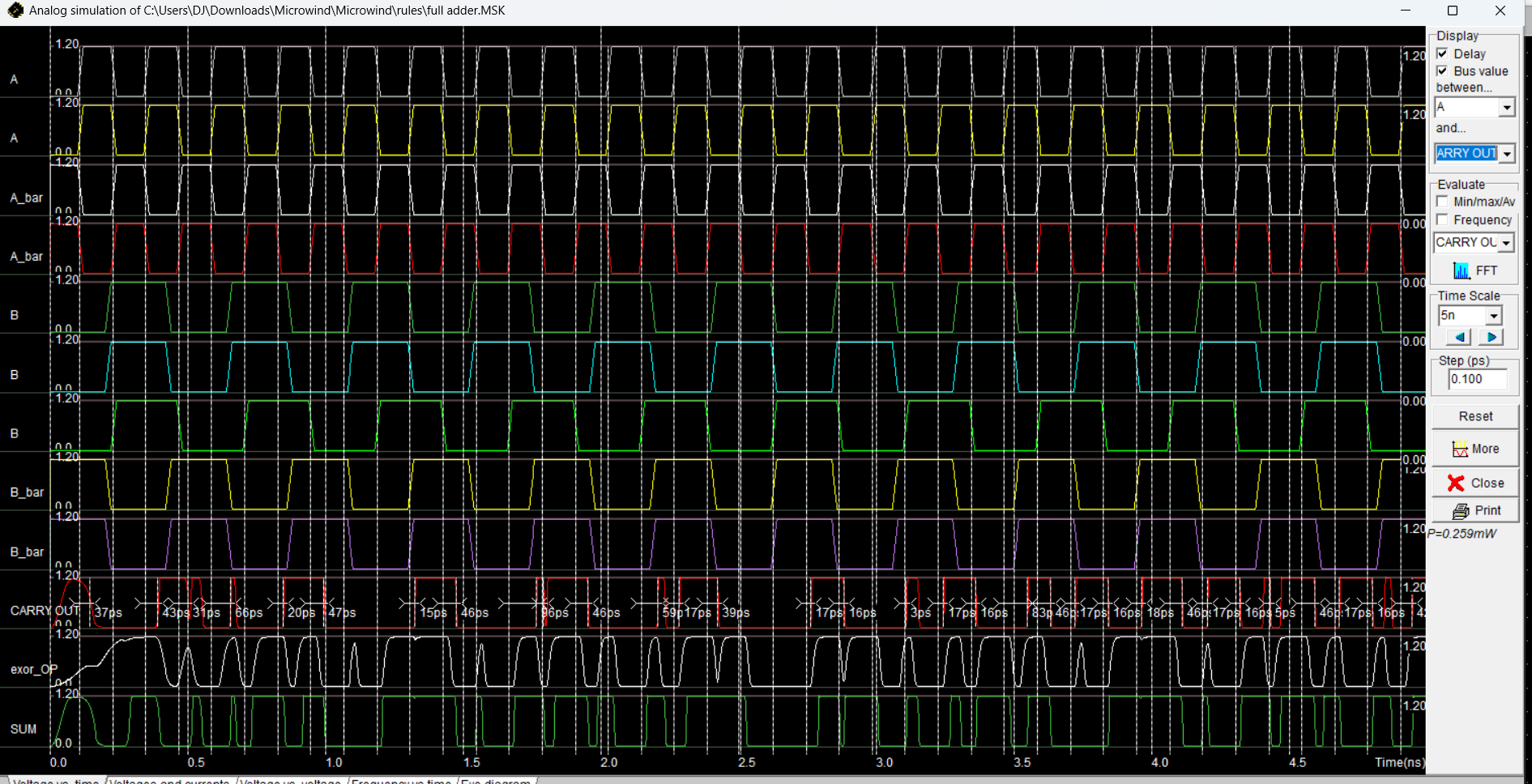
* Microwind project file (.msk) and screenshots of layout.
* Timing diagrams of functional verification.
* A short report (3–5 pages) containing:
* Circuit diagrams, truth tables, logic equations.
* Layout screenshots with annotations.
* Simulation results (timing diagram / waveform).
* Observations and conclusion.

**Rubric (30 Marks)**

|  |  |  |
| --- | --- | --- |
| Criteria | Description | Marks |
| 1. Circuit Understanding | Truth tables, logic design, and block diagrams showing clarity of each circuit. | 6 |
| 2. Layout Design in Microwind | Correct transistor-level layout, proper connections, and adherence to CMOS rules. | 10 |
| 3. Simulation & Results | Functional verification with waveforms and timing diagrams matching expected output. | 7 |
| 4. Documentation & Submission | Well-structured report with GitHub repository link containing .msk files, screenshots, and report. Neat presentation and timely submission. | 7 |
|  |  |  |

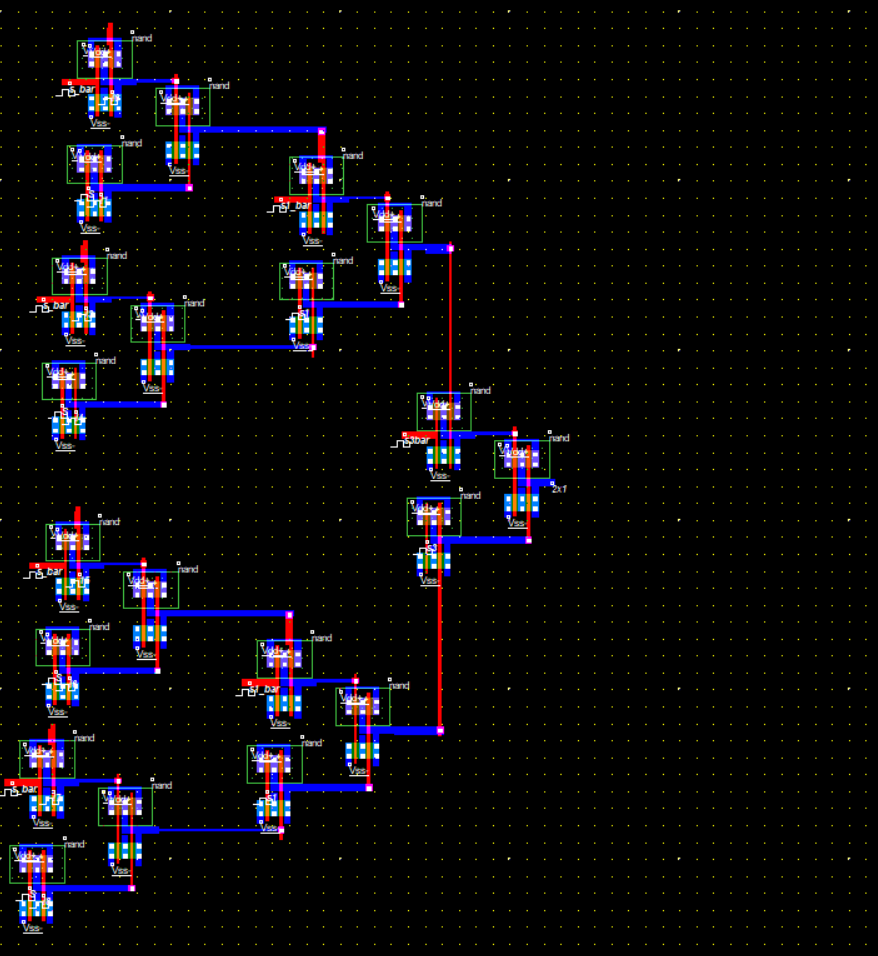
**Student Name: Milan Jani Enrollment No:92301733041 Division: 5EK1**

**Q1. Full Adder  
microwind circuit:  
**

**Output waveform  
**

**Boolean eqn: (A.b\_bar) + (A\_bar . B)**

**Conclusion : It was made by using 2 exor and 2 AND and 1 OR gate.**

**Q2. 8x1 Multiplexer  
=>** I have made this using 2x1 mux for that we need 7 2x1 mux **microwind circuit diagram  
**

**Output waveform:  
A screen shot of a computer

AI-generated content may be incorrect.**

**For one 2x1 mux I am using 3 nand gates.**

**Boolean eqn : y=** D0​⋅S2​​⋅S1​​⋅S0​​+D1​⋅S2​​⋅S1​​⋅S0​+D2​⋅S2​​⋅S1​⋅S0​​+D3​⋅S2​​⋅S1​⋅S0​+D4​⋅S2​⋅S1​​⋅S0​​+D5​⋅S2​⋅S1​​⋅S0​+D6​⋅S2​⋅S1​⋅S0​​+D7​⋅S2​⋅S1​⋅S0​​

**Conclusion:** 3 nand gates are used to make one 2x1 mux and then I used 7 2x1 mux to fullfilll the criteria of 8x1 mux.