

# **COCOA: Collaborative Compendium on Analog Integrated Circuits**



# Table of contents

<b>Preface</b>	<b>1</b>
<b>Acknowledgements</b>	<b>3</b>
<b>Contributors</b>	<b>5</b>
<b>Copyright</b>	<b>7</b>
<b>Conventions</b>	<b>9</b>
<b>I. Learn to Crawl — Square-Law Transistors, Biasing and Small-Signal Analysis</b>	<b>11</b>
<b>1. Introduction</b>	<b>13</b>
1.1. Mixed-Signal Integrated Circuits . . . . .	14
1.1.1. Example: Single-Chip Radio . . . . .	14
1.1.2. Example: Photodiode Interface Circuit . . . . .	16
1.2. Managing Complexity . . . . .	17
1.3. Two-Port Abstraction for Amplifiers . . . . .	19
1.3.1. Amplifier Types . . . . .	21
1.3.2. Unilateral versus Bilateral Two-Ports . . . . .	25
1.3.3. Construction of Unilateral Two-Port Models . . . . .	27
1.4. Integrated Circuit Design versus Printed Circuit Board Design . . . . .	34
1.5. Prerequisites and Advanced Material . . . . .	35
1.6. Notation . . . . .	36
<b>2. Summary</b>	<b>37</b>
<b>3. Problems</b>	<b>39</b>
<b>4. Introduction</b>	<b>41</b>
4.1. First-Order MOSFET Model . . . . .	41
4.1.1. Derivation of I-V Characteristics . . . . .	41
4.1.2. P-Channel MOSFET . . . . .	50
4.1.3. Standard Technology Parameters . . . . .	51
4.2. Building a Common-Source Voltage Amplifier . . . . .	52
4.2.1. Voltage Transfer Characteristic . . . . .	52
4.2.2. Load Line Analysis . . . . .	55
4.2.3. Biasing . . . . .	57
4.2.4. The Small-Signal Approximation . . . . .	60
4.2.5. Transconductance . . . . .	63

*Table of contents*

4.2.6. P-Channel Common-Source Voltage Amplifier . . . . .	67
4.2.7. Modeling Bounds for the Gate Overdrive Voltage . . . . .	68
4.2.8. Voltage Gain and Drain Biasing Considerations . . . . .	69
4.2.9. Sensitivity of the Bias Point to Component Mismatch* . . . . .	73
4.3. Channel Length Modulation . . . . .	74
4.3.1. The $\lambda$ -Model . . . . .	76
4.3.2. Common-Source Voltage Amplifier Analysis Using the $\lambda$ -Model . . . . .	78
4.4. Two-Port Model for the Common-Source Voltage Amplifier . . . . .	82
4.5. Summary . . . . .	84
4.6. References . . . . .	84
4.7. Problems . . . . .	85
<b>II. Learn to Walk — Real Transistors, Noise, Mismatch, and Distortion</b>	<b>89</b>
<b>5. Introduction</b>	<b>91</b>
<b>III. Dare to Run — Knowledge Base for State-of-the-Art Circuits</b>	<b>93</b>
<b>6. Introduction</b>	<b>95</b>
<b>IV. References</b>	<b>97</b>
<b>References</b>	<b>99</b>

# Preface

This open-source book is meant to be a collaborative effort, bringing together insights from students, professionals, and the broader community of analog integrated circuit designers. It will leverage the new possibilities associated with open-source process design kits (PDKs) and open-source chip design software to build up a knowledge base with reproducible examples in a “live and dynamic” online format.

As of its initial creation in August 2024, it is merely a skeleton with the following structure.

- Part I: Learn to crawl — Square-law transistors, biasing and small-signal analysis
- Part II: Learn to walk — Real transistors, noise, mismatch, and distortion
- Part III: Dare to run — Knowledge base for state-of-the-art circuits

Part I is dedicated to learning about powerful abstractions that are necessary to analyze and design analog integrated circuits. This initial exposure is driven with the simplest possible transistor models so that we can focus on fully understanding these abstractions and don’t get distracted by second-order effects that will only become meaningful later on. An added and important side benefit is that we can perfectly match hand calculations and simulations, which not only validates our methods, but also abandons the widespread misconception that circuit simulators rely on some form of “magic” to produce their outputs.

Part II turns expands our horizon to analog circuits with modern transistors, which usually do not obey square-law equations. The good news is that all major abstractions, analysis and design approaches still apply. We just need to abandon the idea of predicting the transistor characteristics with simple equations, and instead rely on lookup tables or advanced model expressions (e.g., EKV-based). Additionally, this is a good time in the overall learning process for dealing with the major pain points of analog design: noise, mismatch and distortion. We review these impairments for the most important circuit primitives, forming a scalable basis for understanding larger circuits.

Part III is meant to capture “deep dives” on commonly used circuits. It will be a forum where you can learn, for example, about the “best” way of going about the design of a bandgap reference, an LC voltage-controlled oscillator, or a successive approximation ADC. This part will undoubtedly be in constant flux and ideally thrive on pointers to reproducible open-source design repositories, simulation data, layouts, etc.



# Acknowledgements

This project was inspired by Vijay Janapa Reddi's CS249R Book and borrows from its implementation. Special thanks to James T. Meech for getting this work off the ground (by porting Chapter 1 of Part I to Quarto).



# **Contributors**

We extend our sincere thanks to the diverse group of individuals who have generously contributed their expertise, insights, and time to improve both the content and codebase of this project.

Boris Murmann

James T. Meech



# **Copyright**

Unless otherwise stated, this work is licensed under Creative Commons Attribution 4.0 International (CC BY 4.0). You can find the full text of the license [here](#)

Contributors to this project have dedicated their contributions to the public domain or under the same open license as the original project. While the contributions are collaborative, each contributor retains the copyright for their respective contributions. All trademarks and registered trademarks mentioned in this book are the property of their respective owners.

The information provided in this book is believed to be accurate and reliable. However, the authors, editors, and publishers cannot be held liable for any damages caused or alleged to be caused either directly or indirectly by the information contained in this book.



# Conventions

Please follow these conventions as you contribute to this online book:

## 1. Clear Structure and Organization:

- **Chapter Outlines:** Begin each chapter with an outline that provides an overview of the topics covered.
- **Sequential Numbering:** Utilize sequential numbering for chapters, sections, and subsections to facilitate easy reference.

## 2. Accessible Language:

- **Glossary:** Include a glossary that defines technical terms and jargon.
- **Consistent Terminology:** Maintain consistent use of terminology throughout the book to avoid confusion.

## 3. Learning Aids:

- **Diagrams and Figures:** Employ diagrams, figures, and tables to visually convey complex concepts.
- **Sidebars:** Use sidebars for additional information, anecdotes, or to provide real-world context to the theoretical content.

## 4. Interactive Elements:

- **Colabs and Projects:** Integrate exercises and projects at the end of each chapter to encourage active learning and practical application of concepts.
- **Case Studies:** Incorporate case studies to provide a deeper understanding of how principles are applied in real-world situations.

## 5. References and Further Reading:

- **Bibliography:** Include a bibliography at the end of each chapter for readers who wish to delve deeper into specific topics.
- **Citations:** Maintain a consistent style for citations, adhering to recognized academic standards like APA, MLA, or Chicago.

## 6. Supporting Materials:

- **Supplementary Online Resources:** Provide links to supplementary online resources, such as video lectures, webinars, or interactive modules.
- **Datasets and Code Repositories:** Share datasets and code repositories for hands-on practice, particularly for sections dealing with algorithms and applications.

## 7. Feedback and Community Engagement:

## *Conventions*

- **Forums and Discussion Groups:** Establish forums or discussion groups where readers can interact, ask questions, and share knowledge.
- **Open Review Process:** Implement an open review process, inviting feedback from the community to continuously improve the content.

### **8. Inclusivity and Accessibility:**

- **Inclusive Language:** Utilize inclusive language that respects diversity and promotes equality.
- **Accessible Formats:** Ensure the textbook is available in accessible formats, including audio and Braille, to cater to readers with disabilities.

### **9. Index:**

- **Comprehensive Index:** Include a comprehensive index at the end of the book to help readers quickly locate specific information.

Implementing these conventions can contribute to creating a textbook that is comprehensive, accessible, and conducive to effective learning.

## **Part I.**

# **Learn to Crawl — Square-Law Transistors, Biasing and Small-Signal Analysis**



# 1. Introduction

With the development of the integrated circuit, the semiconductor industry is undoubtedly the most influential industry to appear in our society. Its impact on almost every person in the world exceeds that of any other industry since the beginning of the Industrial Revolution. The reasons for its success are as follows:

- Exponential growth of the number of functions on a single integrated circuit.
- Exponential reduction in the cost per function.
- Exponential growth in sales (economic importance) for approximately forty years.

This growth has led to ever-increasing performance at lower prices for consumer electronics such as cellular phones, personal computers, audio players, etc. The computational power available to the individual has increased to the point that it has changed the way we think about problem solving. Communication technology including wired and wireless networks have fundamentally changed the way we live and communicate.

The innovation responsible for these impressive results is the integration of electronic circuit components fabricated in silicon **integrated circuit** (IC) technology. Today, many of the ICs shaping new applications contain both analog and digital circuitry, and are therefore called mixed-signal integrated circuits. In mixed-signal ICs, the analog circuitry is typically responsible for interfacing with physical signals, and concerned for example with the amplification of a weak signal from an antenna, or driving a sound signal into a loudspeaker. On the other hand, digital circuitry is primarily used for computing, enabling powerful functions such as Fast Fourier Transforms or floating point multiplication.

This module was written as an introduction to the analysis and design of analog integrated circuits in **complementary metal-oxide-semiconductor** (CMOS) technology. In this first chapter, we will motivate this subject by looking at an example of a mixed-signal IC and by highlighting the need for a systematic study of the fundamental principles and proper engineering approximations in analog design.

## 💡 Chapter Objectives

- Provide a motivation for the study of elementary analog integrated circuits.
- Provide a roadmap for the subjects that will be covered throughout this module.
- Review fundamental concepts for the construction of two-port circuit models.

## 1. Introduction

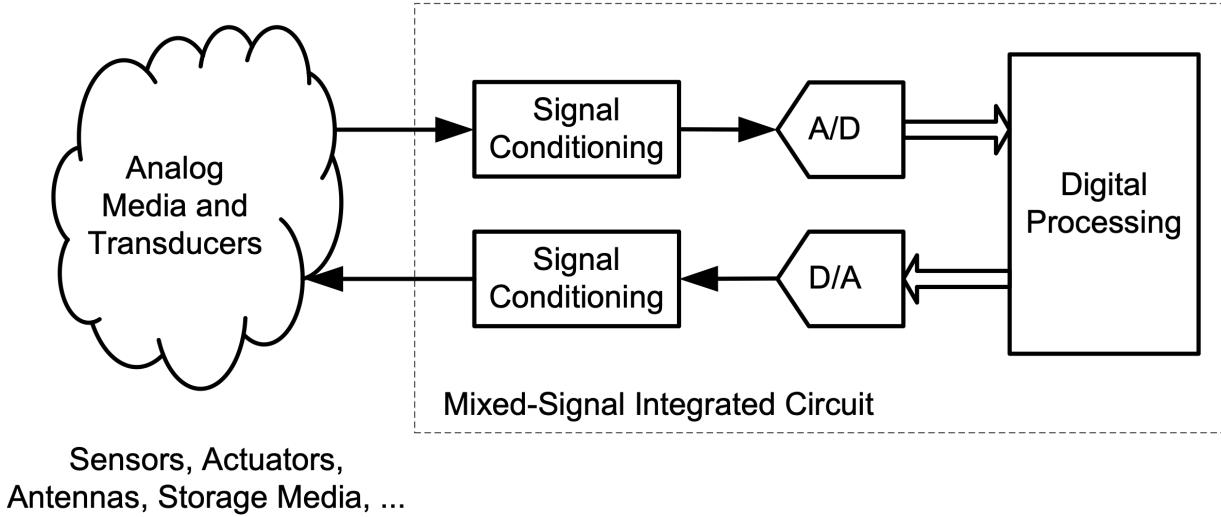


Figure 1.1.: Block diagram of a mixed-signal system.

### 1.1. Mixed-Signal Integrated Circuits

Figure 1.1 shows a generic diagram of a mixed-signal system, incorporating a mixed-signal integrated circuit. To the left of this diagram are the transducers and media that represent the sources and sinks of the information processed by the system. Examples of input transducers include microphones or photodiodes used to receive communication signals from an optical fiber. Likewise, the output of the system may drive an antenna for radio-frequency communication or a mechanical actuator that controls the zoom of a digital camera. At the boundary between the media and transducers are typically signal conditioning circuits that translate the incoming and outgoing signals to the proper signal strength and physical format. For instance, an amplifier is usually needed to increase the strength of the receive signal from a radio antenna, so that it can be more easily processed by the subsequent system components. In most systems, the signal conditioning circuitry interfaces to analog-to-digital and digital-to-analog converters, which provide the link between analog quantities and their digital representation in the computing back-end of the system.

#### 1.1.1. Example: Single-Chip Radio

The block diagram of a modern mixed-signal integrated circuit is shown in Figure 1.2 (see (Staszewski et al. 2008)). This design incorporates most of the circuitry needed to realize a modern cellular phone. For instance, it contains a front-end low-noise amplifier (LNA) to condition the incoming antenna signal. The amplified signal is subsequently frequency shifted, converted into digital format and fed into a digital processor. Even though the block diagram in Figure 1.2 looks quite complex, all of its elements can be mapped into one of the blocks of the generic diagram of Figure 1.1.

Figure 1.3 shows the chip photo of the single-chip radio, with some of the system's key building blocks annotated. As evident from this diagram, the digital logic dominates the area of this particular IC. This situation is not uncommon in modern mixed-signal ICs, not least because

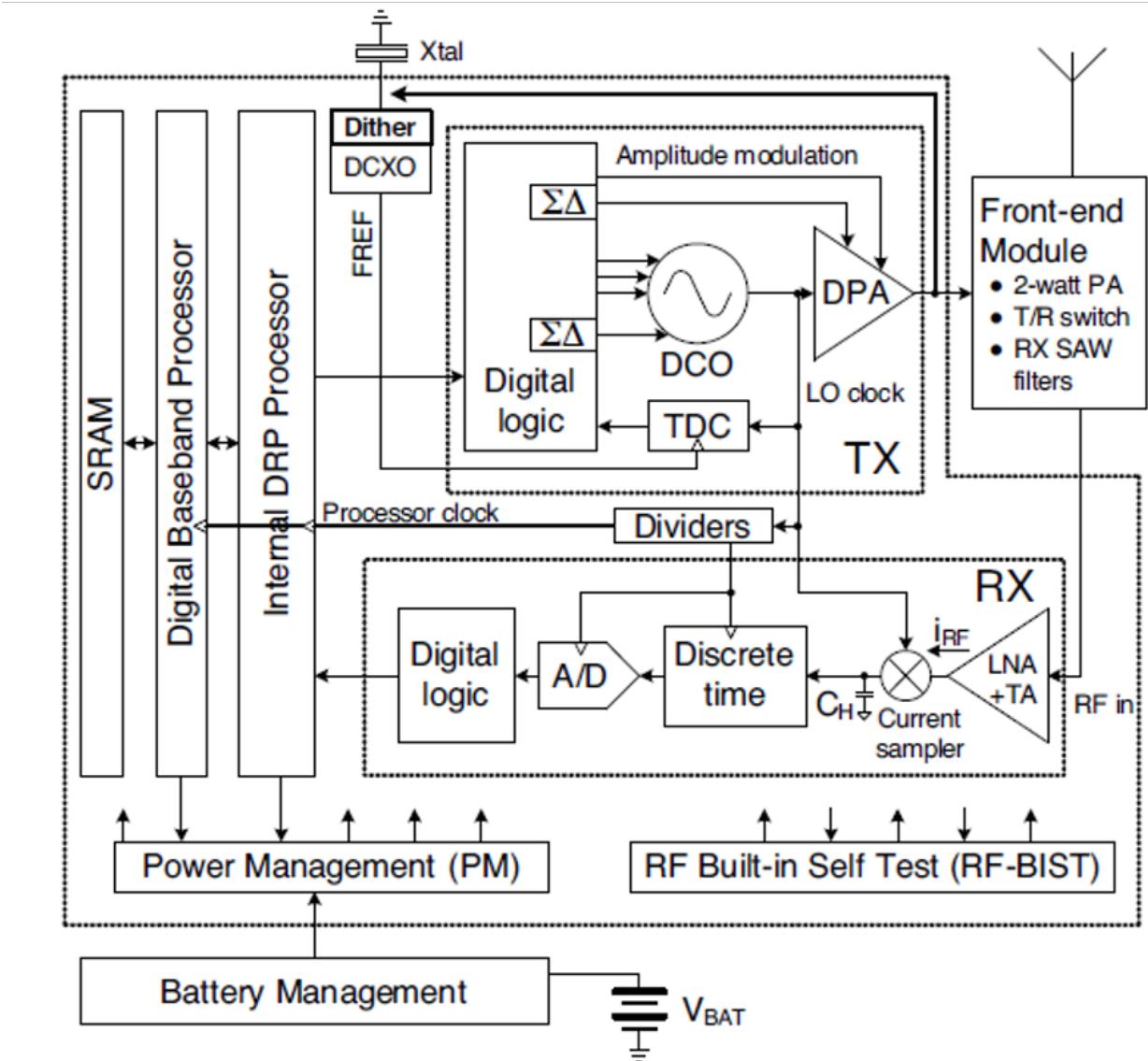


Figure 1.2.: Block diagram of a single-chip radio ((Staszewski et al. 2008)).

## 1. Introduction

the utilized digital algorithms have reached an enormous complexity, requiring millions or tens of millions of logic gates.

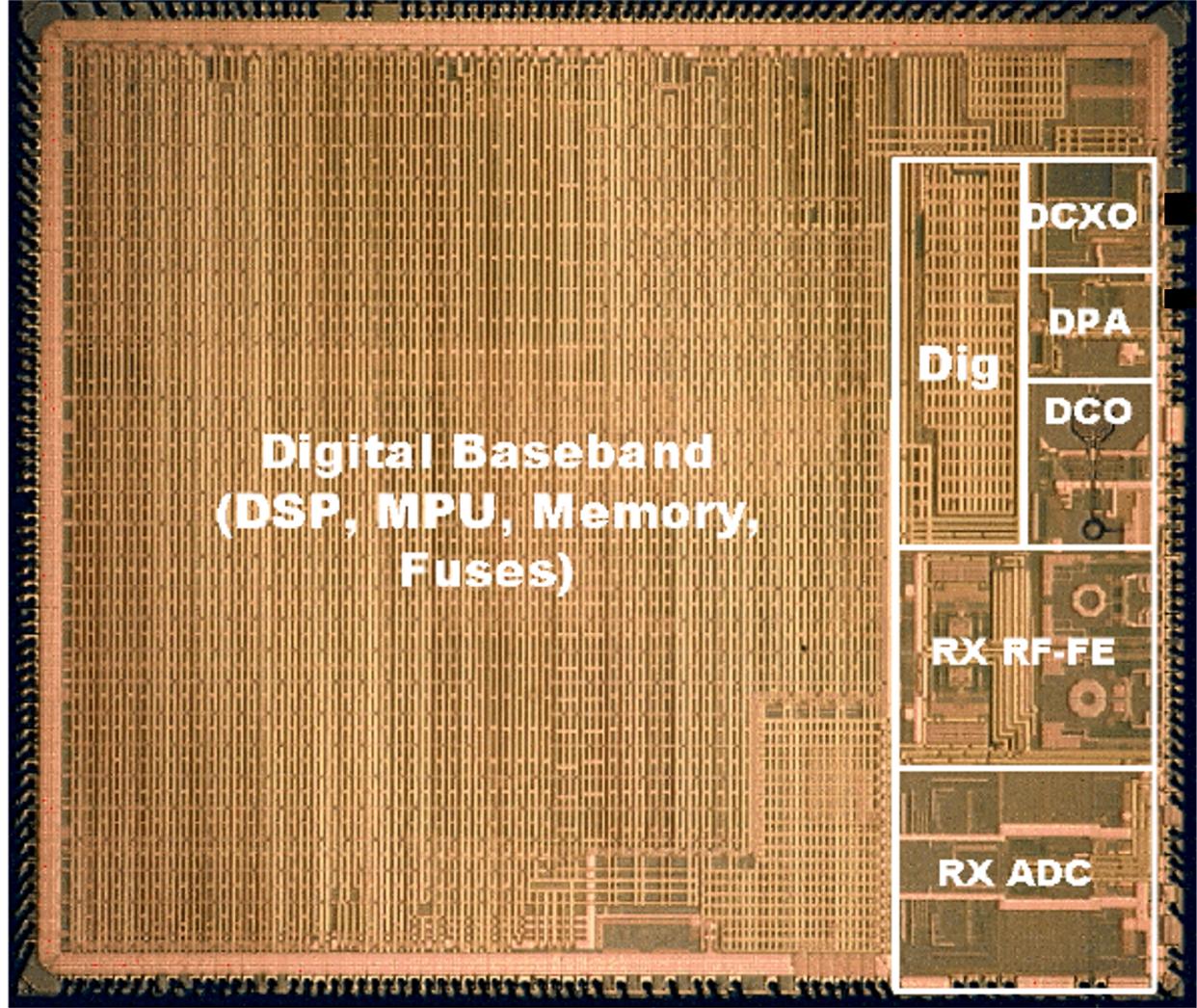


Figure 1.3.: Chip photo of a single-chip radio ((Staszewski et al. 2008)).

Despite the dominance of digital logic within most systems, the analog interface components are equally important, as they determine how and how much information can be communicated between the physical world and the digital processing backbone. In many cases, the performance of the signal conditioning and data conversion circuitry ultimately determines the performance of the overall system.

### 1.1.2. Example: Photodiode Interface Circuit

Figure 1.4 shows an example of a signal conditioning circuit that plays a critical role in fiber-optic communication systems. In such a system, a photodiode is used to convert light intensity to electrical current ( $i_{IN}$ ). In order to condition the signal for further processing, the diode current is converted into a voltage ( $v_{OUT}$ ) by a so-called **transimpedance amplifier**. This amplifier must

be fast enough to process the incoming light pulses, which often occur at frequencies of multiple gigahertz. In addition, the amplifier must obey certain limits on power dissipation, or the system may become impractical in terms of heat management or power supply requirements.

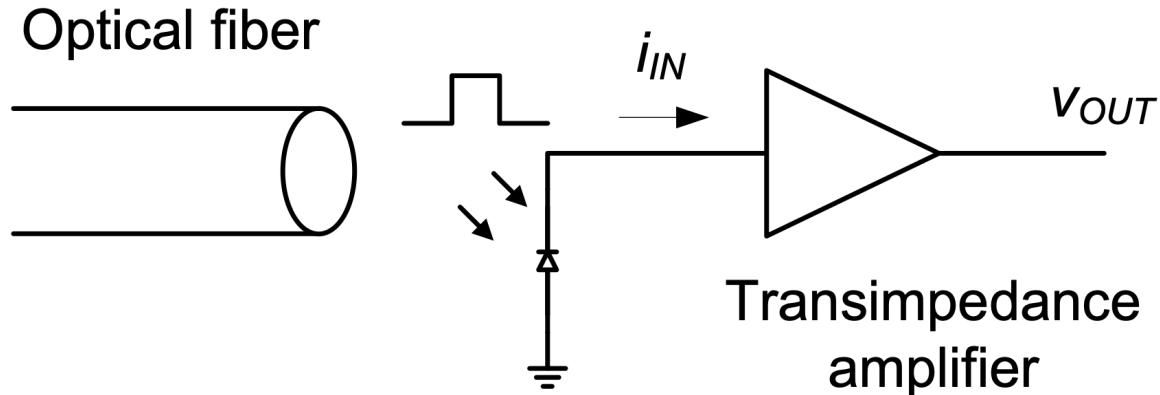


Figure 1.4.: Photodetector circuit for fiber-optic communication.

Limitations in speed and power dissipation are, in general, among the main concerns in the interface circuitry of mixed-signal systems. Since new products tend to demand higher performance, the analog designer is constantly concerned with the design and optimization of system-critical building blocks, aiming for the best possible performance that can be achieved within the framework of the target application and process technology.

A specific example for the circuit realization of a transimpedance amplifier is shown in Figure 1.5. It consists of three transistor stages, each of which serves a specific purpose and design intent. This is true for most amplifier circuits; even though the full schematic of a particular realization may be complex, it can usually be broken up into smaller sub-blocks that are more easily understood. Specifically, for the amplifier of Figure 1.5, the experienced designer will recognize that the circuit consists of a cascade connection of a **common-gate**, **common-source**, and **common-drain** stage. These sub-blocks form the basis for a large number of analog circuits, and can be viewed as the “atoms” or fundamental building blocks of analog design. In this module, you will learn to analyze these blocks from first principles, and to reuse the gained knowledge for the design of more complex circuits. The circuit of Figure 1.5 will be analyzed in detail in Chapter 6 of this module, building upon the principles covered in Chapters 2–5.

## 1.2. Managing Complexity

As evident from the example of Section 1-1-1, modern integrated circuits are highly complex and require a hierarchical approach in design and analysis. That is, a modern integrated circuit is far too complex to be fully understood and analyzed in a single sheet schematic at the transistor level. Typically, a mixed-signal IC is represented by a block diagram as the one shown in Figure 1.2. At the level of this description, suitable specifications are derived for each block, which may itself contain several sub-blocks. The blocks and sub-blocks are then designed and optimized until they meet the desired target specifications.

1. Introduction

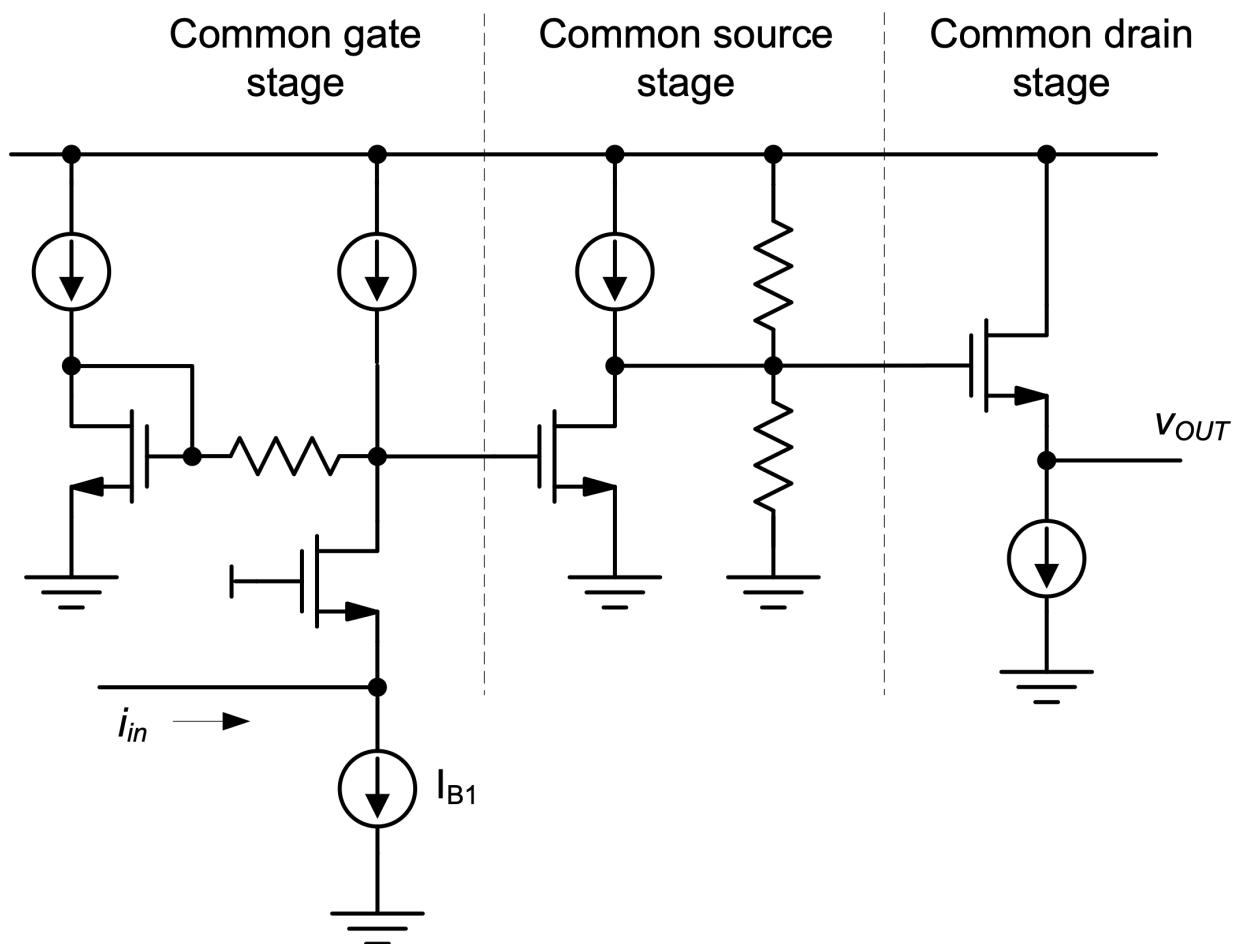


Figure 1.5.: Example realization of a transimpedance amplifier.

Figure 1.6 illustrates examples of the various levels of abstraction that come into play in the design of a modern integrated circuit. At the highest level, the constituent elements can be partitioned into analog and digital blocks. An example of a high-level analog block is an analog-to-digital converter, whereas a microprocessor is an example of a large digital block. These blocks themselves contain smaller functional units, as, for example, operational amplifiers in the case of an analog-to-digital converter. The operational amplifiers themselves contain the aforementioned elementary transistor stages, which are the main subject of this module.

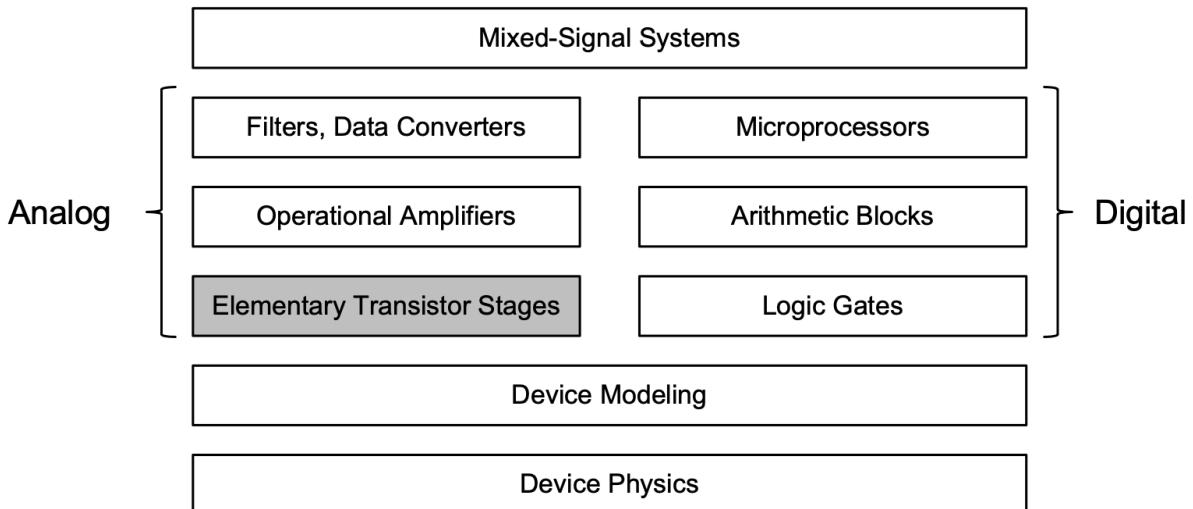


Figure 1.6.: Levels of abstraction in integrated circuit design.

Interestingly, even at the level of elementary transistor stages, is often not possible to work with a perfect model or description of the circuit. This is particularly so because the physical effects in the constituent transistors are highly complex and often impossible to capture perfectly with a tractable set of equations for hand analysis. Therefore, making proper engineering approximations in transistor modeling is an important aspect in maintaining a systematic design methodology. For this particular reason, the presentation in this module follows a “just-in-time” approach for the modeling of transistor behavior. Rather than deriving a complete transistor model in an isolated chapter (as done in most texts), we begin with only the basic device properties and increase complexity throughout the module upon demand, and where needed to gain further insight and accuracy. With this approach, the reader learns to appreciate the complexity of a refined model, and will be able to assess and track potential limitations of working with simplified models.

### 1.3. Two-Port Abstraction for Amplifiers

High-level system block diagrams, such as Figure 1.2 , are typically drawn as unidirectional flowcharts and do not capture details about the electrical behavior of each connection port and how certain blocks may interact once they are connected. Unfortunately, electrical signals are not unidirectional, and connecting two blocks always means that there is some level of interaction through the voltages and currents at the connection points.

## 1. Introduction

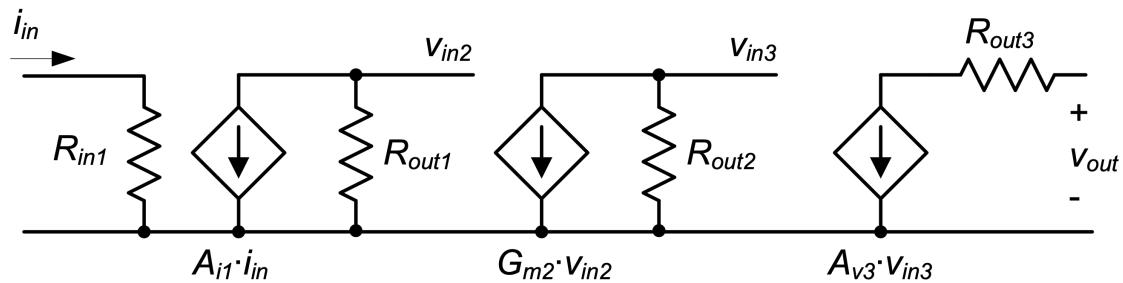


Figure 1.7.: Two-port model of the transimpedance amplifier circuit in Figure 1.5.

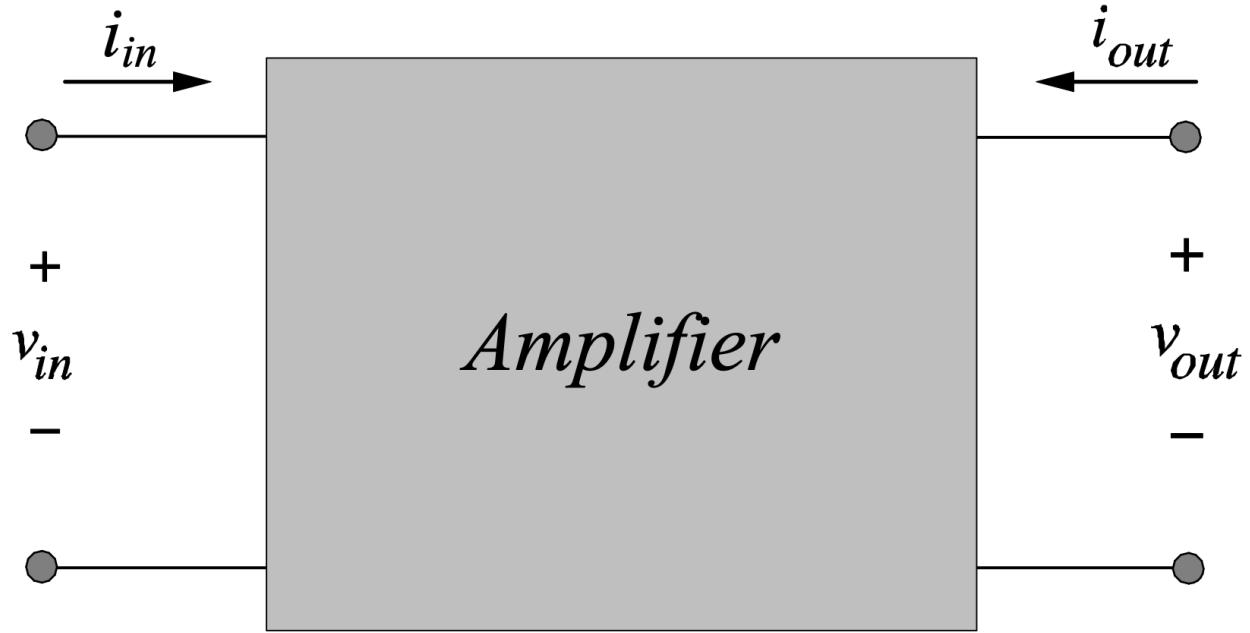


Figure 1.8.: General amplifier two-port.

The commonly used linear two-port modeling abstraction for amplifiers and amplifier stages allows the designer to take these effects into account while maintaining a high level of abstraction. For instance, the circuit of Figure 1.5 can be approximately modeled as shown in Figure 1.7 (the details on obtaining this model are discussed later in this module). Each stage of the overall amplifier is represented via a simplified circuit model that captures its essential features. Once this model is created, the interaction among stages can be analyzed at this high level of abstraction, without requiring detailed insight on how each stage is implemented. The two-port modeling approach is particularly useful in the design of amplifiers, as it can help shape the thought process on how the various stages should be configured to optimize performance. In the following subsections, we will review some of the basic concepts of amplifier two-port modeling used in this module.

### 1.3.1. Amplifier Types

In this module, we model amplifier circuits as blocks that have an input and output port, where the term “port” refers to a pair of terminals. For each port, we can define input and output currents and voltages as shown in Figure 1.8. Depending on the intended function, we distinguish between the four possible amplifier types listed in Table 1-1. For example, an amplifier that takes an input current and amplifies this current to produce a proportional output voltage is called a transresistance amplifier. In this context, it is important to emphasize that in a general practical amplifier circuit, the input and output ports will always carry both nonzero voltages and currents, and there exist transfer functions between all possible combinations of input/output variables. What truly defines the type of an amplifier is what the circuit designer deems as the main quantities of interest in the amplifier’s application.

Table 1.1.: Amplifier types.

Amplifier Type	Input Quantity	Output Quantity
Voltage Amplifier	Voltage	Voltage
Current Amplifier	Current	Current
Transconductance Amplifier	Voltage	Current
Transresistance Amplifier	Current	Voltage

Now, in order to model the inner workings of each amplifier type, we can invoke the four corresponding two-port amplifier models shown in Figure 1.9. Each amplifier model has an input and output resistance (or more generally, a frequency dependent impedance) and a controlled source to model the amplification.

- In the **voltage amplifier model**, the controlled source is a voltage-controlled voltage source. Ideally, the input resistance is infinite (open circuit, no current flow). The ideal output resistance is zero (ideal voltage source).
- The **current amplifier model** has a current-controlled current source. Ideally, the input resistance is zero (short circuit, no voltage across the input port) and the output resistance is infinite (ideal current source).
- The **transconductance amplifier model** has a voltage-controlled current source. Ideally, the input resistance is infinite (open circuit, no current flow). The ideal output resistance is also infinite (ideal current source).

## 1. Introduction

- The **transresistance or transimpedance<sup>1</sup> amplifier model** has a current-controlled voltage source. Ideally, the input resistance is zero (short circuit, no voltage across the input port). The ideal output resistance is also zero (ideal voltage source).

From these four models and their ideal behavior, we note that the two-ports containing a voltage-controlled source should ideally have large input resistance ( $R_{in}$ ). This minimizes the signal loss due to resistive voltage division between the source voltage ( $v_s$ ) and the control voltage ( $v_{in}$ ). In contrast, the two-ports that use a current-controlled source should have small input resistance to minimize the signal loss due to current division between the source current ( $i_s$ ) and the control current ( $i_{in}$ ). In this context, “large” and “small” refer to the value of  $R_{in}$  relative to the source resistance ( $R_s$ ).

On the output side, if the variable of interest is a voltage, the output resistance ( $R_{out}$ ) should be small so that only a small amount of the amplified voltage is lost through the division with the load ( $R_L$ ). Conversely, for a current output, the output resistance should be large to minimize current division losses. Again, “large” and “small” are taken as relative measures comparing  $R_{out}$  to  $R_L$ .

Consider for example the voltage amplifier of Figure 1.9(a). To calculate the transfer function of the overall circuit ( $v_{out}/v_s$ ), the input voltage, including its source resistance, is connected to the input of the two-port model and the load resistance is connected to the output. The full circuit is shown in Figure 1.10.

Applying the voltage divider rule at the input and output of the circuit gives

$$\frac{v_{out}}{v_s} = \left( \frac{v_{in}}{v_s} \right) \cdot A_v \cdot \left( \frac{v_{out}}{v_x} \right) = \left( \frac{R_{in}}{R_{in} + R_s} \right) \cdot A_v \cdot \left( \frac{R_L}{R_L + R_{out}} \right) \quad (1.1)$$

As we can see from this expression, the overall voltage gain is maximized when the amplifier has a large input resistance (relative to  $R_s$ ) and a small output resistance (relative to  $R_L$ ). For the ideal case of infinite input resistance and zero output resistance,  $v_{out}/v_s$  becomes equal to  $A_v$ .

For the sake of compact notation, we will often want to use a symbol for the overall circuit gain. The notation used in this module uses primed variables to distinguish between the gain of the controlled source and the gain of the overall amplifier circuit. For example, for the above-discussed voltage amplifier we define  $A'_v = v_{out} / v_s$ . This notation is meant to emphasize the connection between the two symbols.  $A'_v$  is usually smaller than  $A_v$ , but can approach  $A_v$  for ideal source and load configurations.

### Example 1-1: Transfer Function Transconductance Amplifier.

For the transconductance amplifier circuit in Figure 1.11, calculate the overall transconductance  $G'_m = i_{out} / v_s$ .

### SOLUTION

Applying the voltage divider rule at the input and the current divider rule at the output yields the following result:

$$G'_m = \frac{i_{out}}{v_s} = \left( \frac{v_{in}}{v_s} \right) \cdot G_m \cdot \left( \frac{i_{out}}{i_x} \right) = \left( \frac{R_{in}}{R_{in} + R_s} \right) \cdot G_m \cdot \left( \frac{R_{out}}{R_L + R_{out}} \right)$$

---

<sup>1</sup>The term transimpedance is sometimes used to refer to an amplifier that is primarily meant to realize a transresistance. Referring to “impedance” highlights the fact that the transfer function will usually be frequency-dependent.

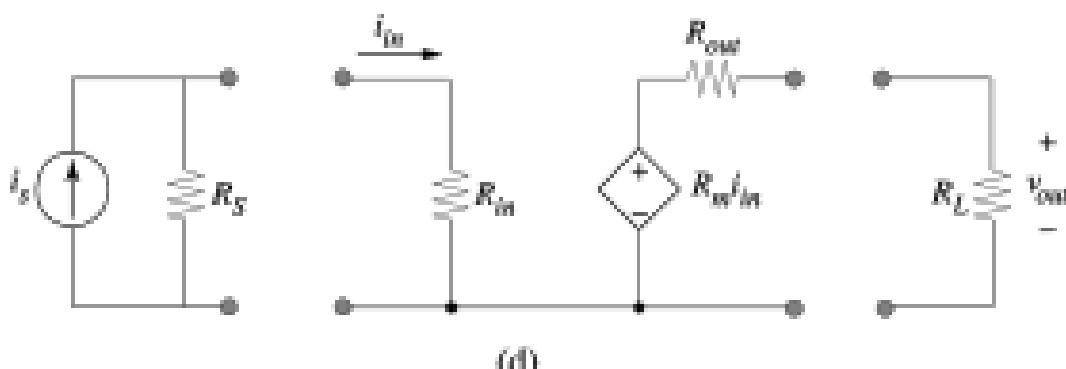
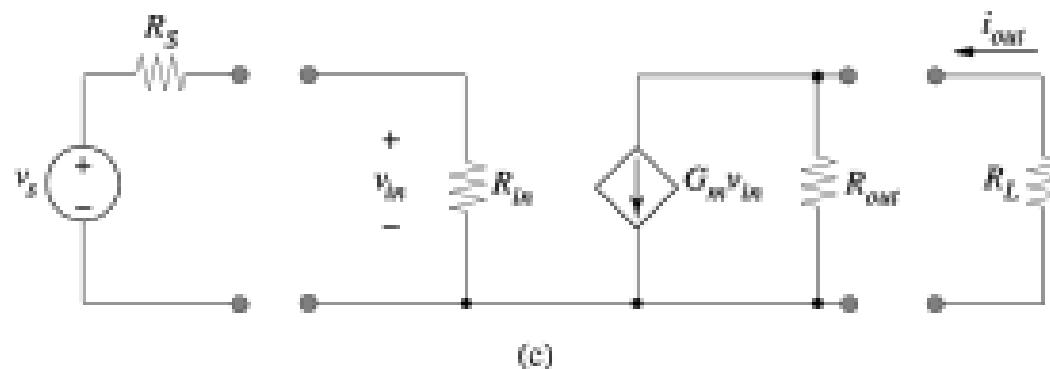
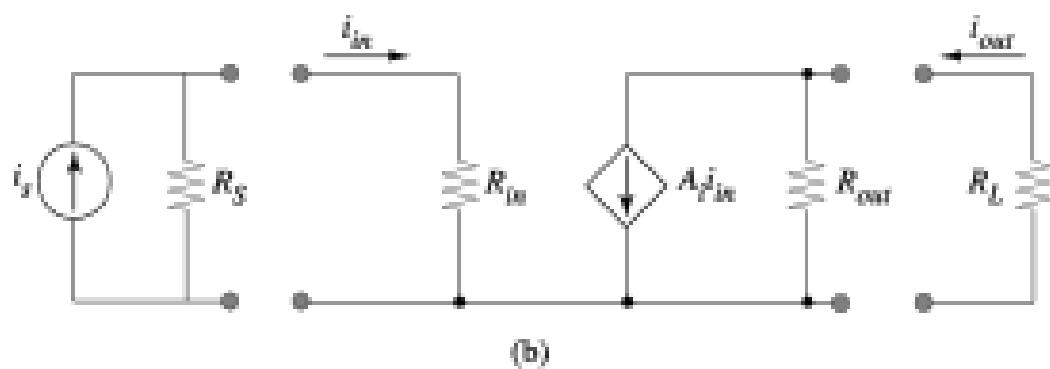
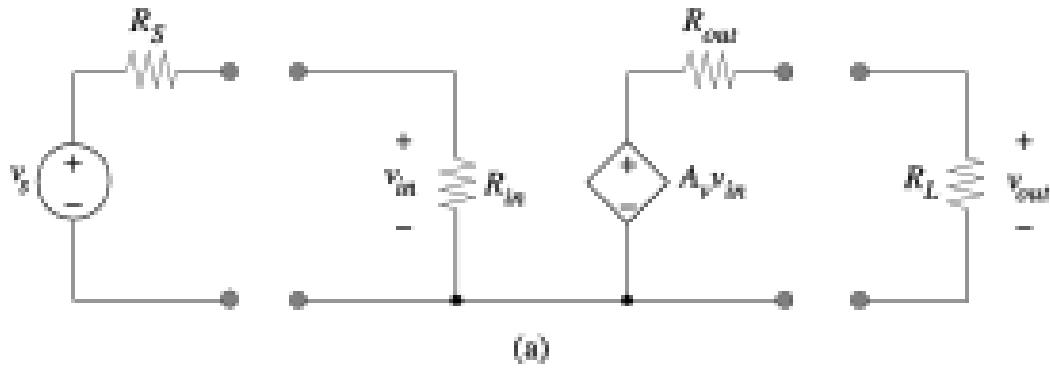


Figure 1.9.: Two-port amplifier models with input source and load: (a) voltage amplifier, (b) current amplifier, (c) transconductance amplifier, and (d) transresistance amplifier.

1. Introduction

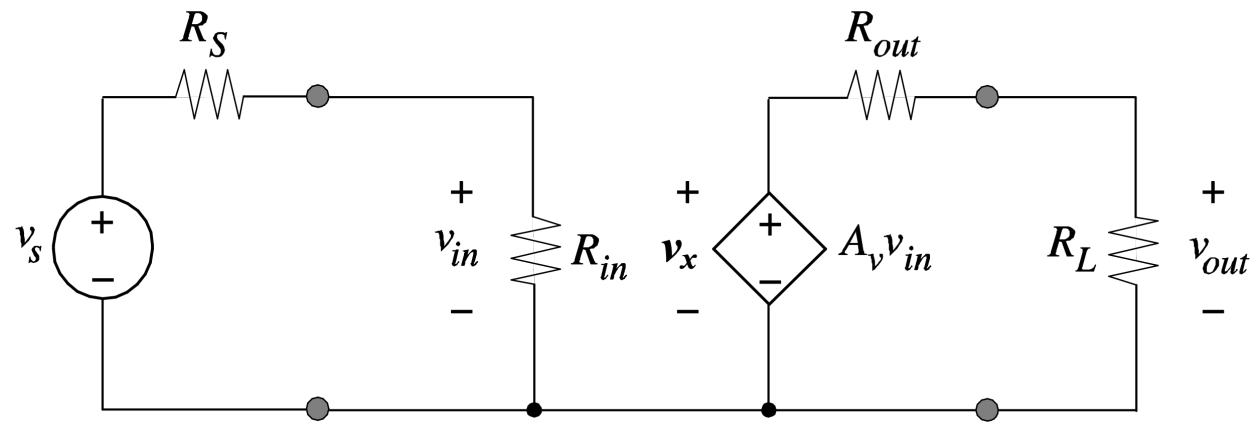


Figure 1.10.: Voltage amplifier with connected source and load resistances.

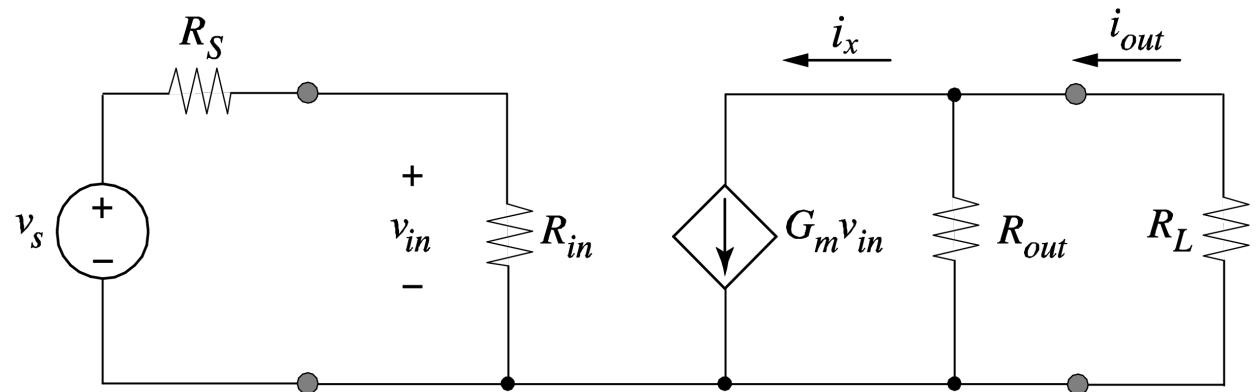


Figure 1.11.: Figure Ex 1-1

Thus, the overall transconductance gain is maximized when the amplifier has a large input resistance (relative to  $R_s$ ) and a large output resistance (relative to  $R_L$ ). For the ideal case of infinite input and output resistances,  $G'_m$  becomes equal to  $G_m$ .

As a final remark for this sub-section, it is important to recognize that all of the models in Figure 1.9 can be used interchangeability to describe the exact same electrical behavior (see Problem P1-1). For instance, a voltage amplifier model can be converted into a transconductance amplifier model by applying a Thevénin to Norton transformation for the controlled source.

A corollary to this equivalence is that we can for example use a transconductance amplifier model to describe a voltage amplifier circuit. This is illustrated through the circuit of Figure 1.10, which is electrically equivalent to that of Figure 1.10 (see Problem P1-2). Note that the output is taken as the voltage across the output port instead of the output current; this indicates that the circuit is viewed as a voltage amplifier. Just as in the original circuit of Figure 1.10, we require a large input resistance and small output resistance for this circuit to maximize the overall voltage gain.

The choice of amplifier model depends on several factors. At first glance, it seems natural to model each amplifier type using its “native” model that directly corresponds to the intended function. For example, we could always describe a voltage amplifier using the corresponding voltage amplifier model that contains a voltage controlled voltage source. However, as we shall see throughout this module, it is sometimes more convenient to align the amplifier model with the physical amplification mechanism or a structural feature of the underlying transistor circuit. For instance, the common-source voltage amplifier discussed in Chapter 2 naturally invokes a transconductance-based model due to the physical model of the employed transistor.

### 1.3.2. Unilateral versus Bilateral Two-Ports

All of the two-port models shown in Figure 1.9 are called **unilateral**, because they can only propagate a signal from the input port to the output port and not the other way around. For instance, injecting a current into the output port of the current amplifier of Figure 1.9(b) will not induce a current at the input port. Unfortunately, many practical transistor circuits are not unilateral, and exhibit **bilateral** behavior when analyzed in detail, and especially at high frequencies.

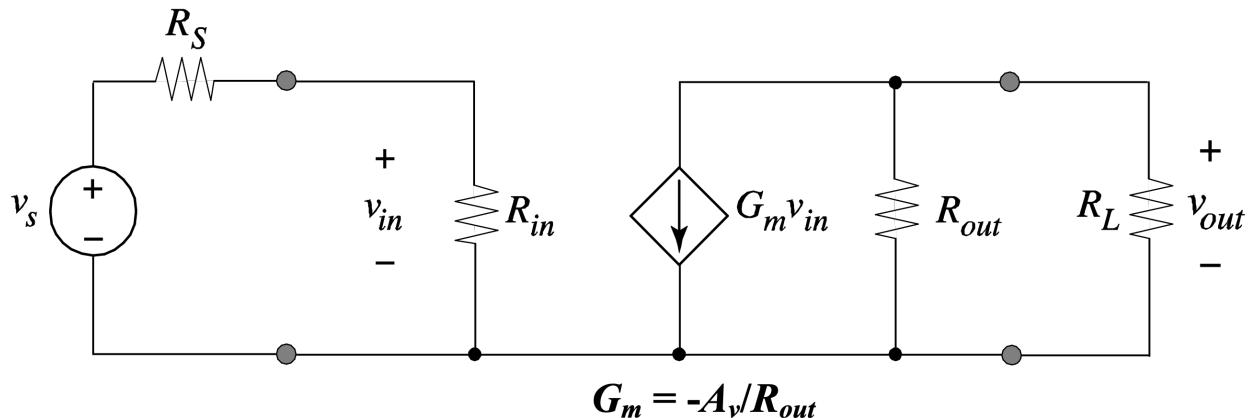


Figure 1.12.: Voltage amplifier with an underlying transconductance amplifier model

**Figure 1-12**

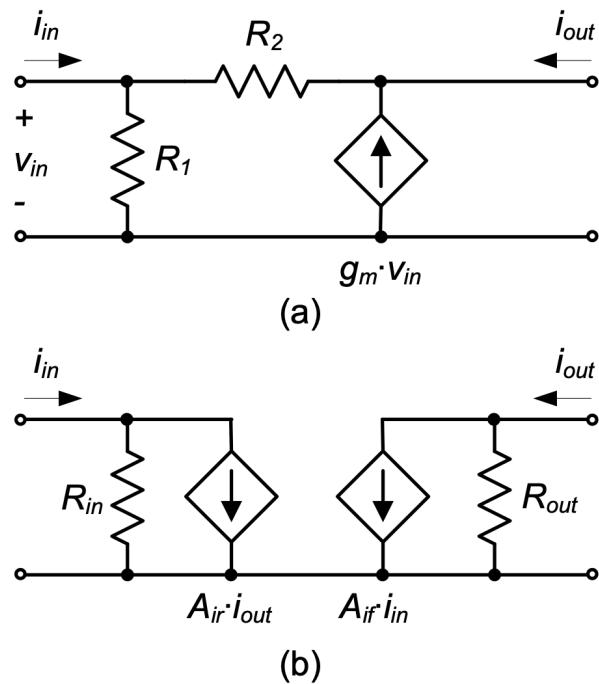


Figure 1.13.: (a) Example of a bilateral current amplifier. (b) Corresponding bilateral current amplifier two-port model.

An example of a bilateral current amplifier is shown Figure 1.13(a). Note that in this circuit, resistor  $R_2$  couples the input and output networks and it can therefore transfer currents in both directions. Consequently, the unilateral model of Figure 1.9(b) cannot perfectly represent this circuit. When it is desired to capture the bilateral behavior, the two-port model in Figure 1.13(b) could be employed in principle. Here, the controlled source  $A_{ir}$  models the reverse current transfer from the output back to the input. Alternatively, one could employ other bilateral and more general two-port models based on admittance parameters ( $Y$ ), impedance parameters ( $Z$ ), and hybrid or inverse-hybrid parameters ( $H$  or  $G$ ); see advanced circuit design texts such as (Gray et al. 2009). These models are particularly useful when reverse transmission (i.e., feedback from the output to the input) is incorporated in the circuit as part of the intended design.

There are two reasons why we will work exclusively with unilateral two-port approximations in this module. First, the circuits considered are designed primarily to implement forward gain rather than reverse gain; feedback circuits are not treated in this module. For example, referring to the model of Figure 1.13(b), the reverse gain  $A_{ir}$  will be negligibly small in any current amplifier circuit that we will consider. Second, a clear drawback of working with bilateral two-port models would be a significant increase in analysis complexity. As we have seen in Example 1-1, the overall transfer function of a unilateral two-port circuit can be written by applying simple voltage and current divider rules. This also extends to cascade connections of multiple two-ports. For example, the overall transfer function of the circuit in Figure 1.7 is easily written by inspection, without requiring extensive algebra. With reverse transmission included, the transfer function analysis will generally require solving a linear system of equations. In light of the fact that we do not intend to design circuits in this module that have significant reverse transmission, this increase in complexity is not welcome, and would also hinder us from developing intuition from inspection-driven analysis.

### 1.3.3. Construction of Unilateral Two-Port Models

We will now describe the general procedures to calculate the controlled sources, as well as the input and output resistances, for the unilateral two-port models of Figure 1.9. The approach is based on applying test voltages and currents to find the desired model parameters.

The most important parameter of any amplifier circuit is its gain. To identify the gain parameters for the models of Figure 1.9(a)-(d), we apply the tests shown in Figure 1.14(a)-(d), respectively.

- To calculate the gain term  $A_v$  of a voltage amplifier model, we apply a test voltage at the input with zero source resistance and measure the open-circuit output voltage.  $A_v = v_{oc}/v_t$  is therefore also called the **open-circuit voltage gain**.
- To calculate the gain term  $A_i$  of a current amplifier model, we apply a test current at the input with infinite source resistance and measure the short-circuit output current.  $A_i = i_{sc}/i_t$  is therefore also called the **short-circuit current gain**.
- To calculate the gain term  $G_m$  of a transconductance amplifier model, we apply a test voltage at the input with zero source resistance and measure the short-circuit output current to find  $G_m = i_{sc}/v_t$ .
- To calculate the gain term  $R_m$  of a transresistance amplifier model, we apply a test current at the input with infinite source resistance and measure the open-circuit output voltage to find  $R_m = v_{oc}/v_{it}$ .

## 1. Introduction

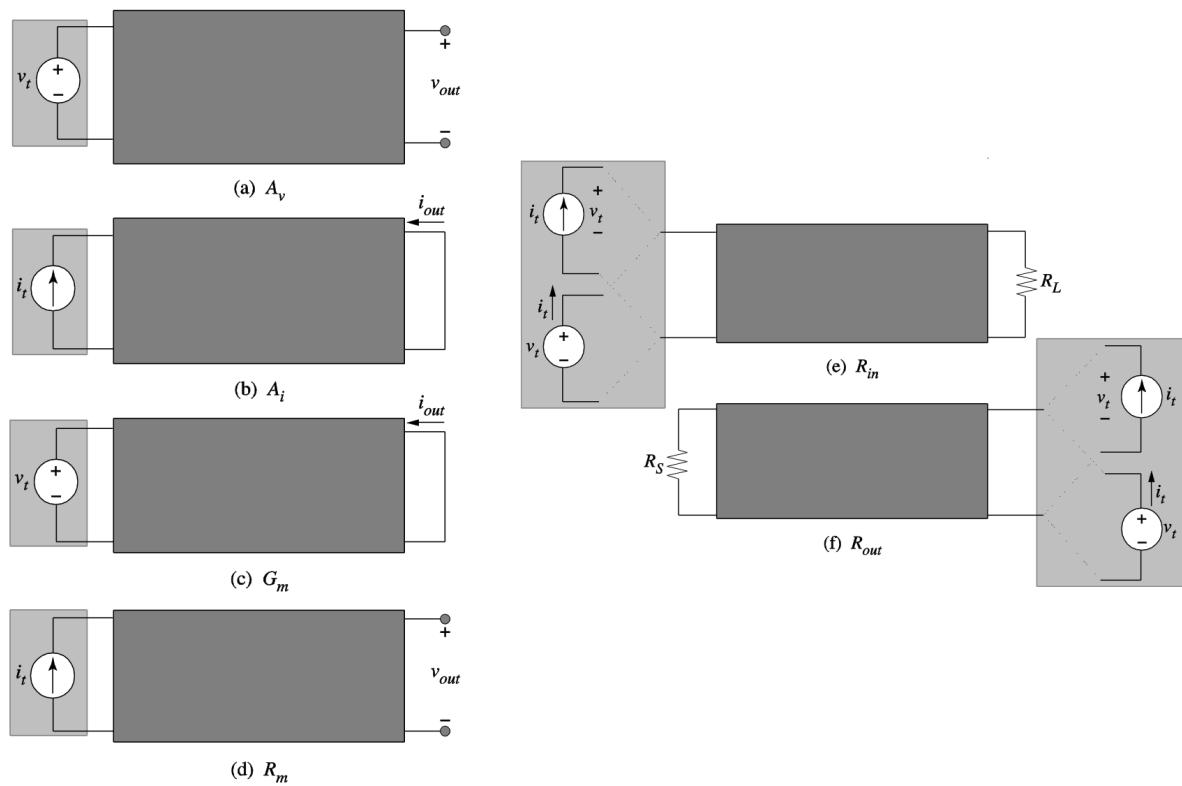


Figure 1.14.: Method to calculate two-port amplifier model parameters: (a) voltage gain  $A_v$ , (b) current gain  $A_i$ , (c) transconductance  $G_m$ , (d) transresistance  $R_m$ , (e) input resistance  $R_{in}$ , and (f) output resistance  $R_{out}$ .

The rationale behind these tests can be understood by considering, for example, the case of the voltage amplifier model of Figure 1.9(a). When driven with an ideal voltage source, the effect of any resistance at the input port is eliminated, and the controlled source is directly stimulated by the applied test source (without any voltage division). Likewise, by measuring the resulting output voltage open-circuited, any resistance in series with the controlled source has no effect and the measurement therefore accurately extracts the parameter  $A_v$ . Similar explanations apply to the test cases for the remaining amplifier models.

The test setup for extracting the input and output resistances for all amplifier models is shown in Figure 1.14(e), and (f), respectively.

- To calculate the **input resistance**  $R_{in}$  we apply a test voltage and measure the current coming from the test source, or apply a test current and measure the voltage across the test source. In this test, the load resistance ( $R_L$ ) must be connected to the output port as shown in Figure 1.14(e).
- To calculate the **output resistance**  $R_{out}$ , we apply either a test voltage or a test current source at the output port and measure the respective current or voltage from the source. Here, the input source must be set equal to zero. This means that input voltage sources are shorted and input current sources are open-circuited. Only the source resistance ( $R_S$ ) is left across the input terminals as shown in Figure 1.14(f).

The above procedures extract the input and output resistances perfectly and without any approximations, even if the circuit is bilateral. As we shall see through the examples below,  $R_{in}$  and  $R_{out}$  do not depend on  $R_L$  and  $R_S$ , respectively, in a perfectly unilateral amplifier. However, this is not the case in a bilateral amplifier, and therefore the general procedure includes  $R_L$  and  $R_S$  in the test setup.

In summary, the above procedures for measuring unilateral two-port model parameters aim at finding the best possible unilateral representation of an arbitrary amplifier circuit, which itself may or may not be unilateral. The obtained models are approximate when the amplifier is bilateral, since they do not include a controlled source that captures reverse transmission from the output back to the input. In most cases considered in this module, the reverse transmission term is negligible. Exceptions will be highlighted and treated as appropriate.

### Example 1-2: Two-Port Model Calculations for a Unilateral Amplifier

For the transconductance amplifier in Figure 1.15, calculate the following two-port model parameters: the transconductance  $G_m$ , the input resistance  $R_{in}$ , and the output resistance  $R_{out}$ . Also, compute the overall transfer function  $G'_m = i_{out} / v_s$ .

#### SOLUTION

To find the transconductance, we short the output port and apply an ideal test voltage source ( $v_t$ ) at the input (see Figure 1.15). From this circuit, we see that

$$G_m = \frac{i_{sc}}{v_t} = \frac{g_m v_x \cdot \frac{R_3}{R_3+R_4}}{v_t} = \frac{g_m v_x \cdot \frac{R_2}{R_1+R_2} \cdot \frac{R_3}{R_3+R_4}}{v_t} = g_m \cdot \frac{R_2}{R_1+R_2} \cdot \frac{R_3}{R_3+R_4}$$

Next, to find  $R_{in}$ , we apply a test voltage at the input and connect the load resistance  $R_L$  at the output (Figure 1.16). From this circuit, we find that the input resistance is simply the series

## 1. Introduction

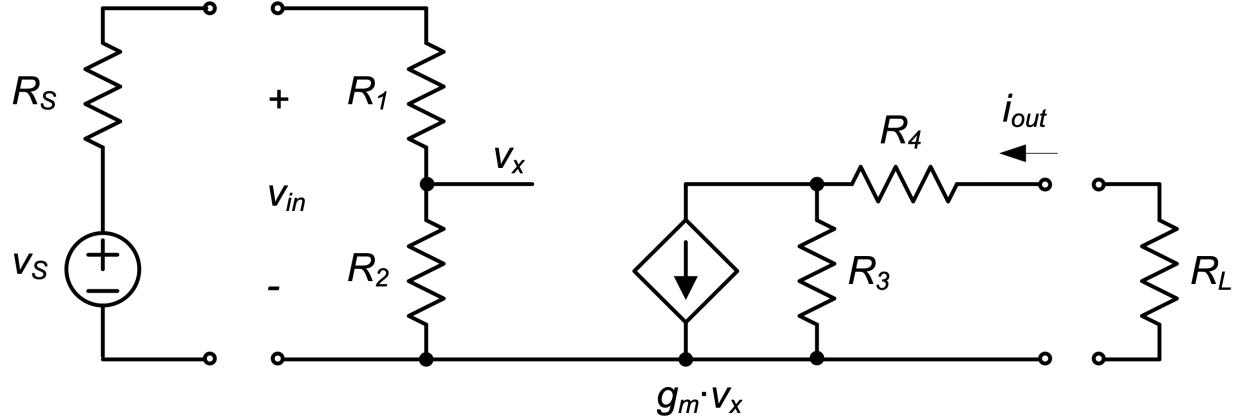


Figure 1.15.: Figure Ex1-2A

connection of  $R_1$  and  $R_2$ , i.e.,  $R_{in} = R_1 + R_2$ . Note that the output network does not influence this result.

Finally, to find  $R_{out}$ , we apply a test voltage at the output and connect the source resistance  $R_s$  across the input port (the source  $v_s$  is replaced by a short), (see Figure 1.16(c)). In the resulting circuit,  $v_x$  must be zero, because no current is flowing in the input network. Thus, the controlled source carries no current and we conclude that  $R_{out} = R_3 + R_4$ .

In order to compute the transfer function of the complete circuit, we can reuse the result obtained in Example 1-1.

$$G'_m = \frac{i_{out}}{v_s} = \left( \frac{R_{in}}{R_{in} + R_s} \right) \cdot G_m \cdot \left( \frac{R_L}{R_L + R_{out}} \right)$$

Substituting  $G_m$ ,  $R_{in}$ , and  $R_{out}$  from the above calculation yields the final result.

$$G'_m = \frac{i_{out}}{v_s} = \frac{g_m R_2 R_3}{(R_1 + R_2 + R_s)(R_L + R_3 + R_4)}$$

In the preceding example, we have seen that the source and load resistances have no effect on the extracted two-port parameters. In the following example, we will investigate a bilateral circuit to show that in general, the input and output resistances depend on  $R_s$  and  $R_L$ , which must therefore always be included in the general two-port modeling calculations.

### Example 1-3: Two-Port Model Calculations for a Bilateral Amplifier

For the current amplifier in Figure 1.13(a), calculate the following unilateral two-port model parameters: the current gain  $A_i$ , the input resistance  $R_{in}$ , and the output resistance  $R_{out}$ . Also, compute the overall transfer function  $i_{out}/v_s$  using the obtained unilateral two-port model. Compare the result to a direct KCL-based analysis of the transfer function. Assume that the circuit is driven by a current source with resistance  $R_s$  and loaded by a resistance  $R_L$ . For algebraic simplicity, assume  $R_1 = 1 / g_m$  (this case corresponds to the common-gate amplifier circuit covered in Chapter 4).

### SOLUTION

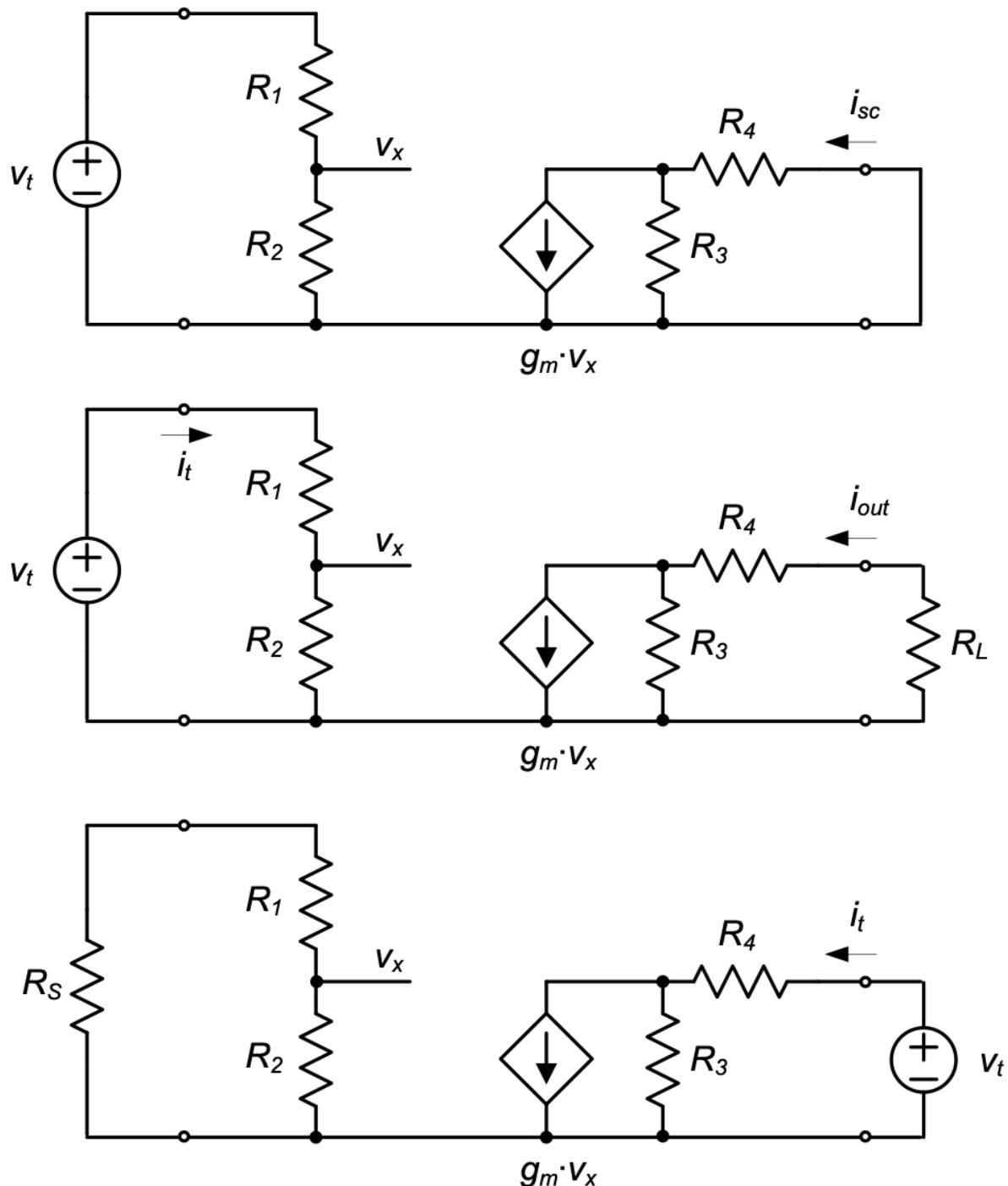


Figure 1.16.: Figure Ex1-2B

## 1. Introduction

To find the current gain  $A_i$ , we short the output port and apply an ideal test current source ( $i_t$ ) at the input (see Figure 1.17(a)). From this circuit, we see that

$$v_{in} = \left( g_m + \frac{1}{R_2} \right)^{-1} \cdot i_t$$

and

$$i_{sc} = -\left( g_m + \frac{1}{R_2} \right) \cdot v_{in}$$

Thus,  $A_i = i_{sc}/i_t = -1$ .

Next, to find  $R_{in}$ , we apply a test voltage at the input and connect the load resistance  $R_L$  at the output (Figure 1.17(b)). From this circuit, we note that the input resistance is not easily identified by inspection. Hence we write KCL for the two nodes of the circuit ( $v_t$  and  $v_{out}$ ).

$$0 = -i_t + g_m v_t + \frac{v_t - v_{out}}{R_2}$$

$$0 = -g_m v_t + \frac{v_{out}}{R_L} + \frac{v_t - v_{out}}{R_2}$$

Solving this system of equations yields

$$R_{in} = \frac{v_t}{i_t} = \frac{R_2 + R_L}{1 + g_m R_2} = \frac{1 + \frac{R_L}{R_2}}{g_m + \frac{1}{R_2}}$$

Note from this result that  $R_{in}$  depends on  $R_L$ , as mentioned previously; this dependency stems from the bilateral structure of the circuit. Also note that  $R_{in}$  approaches  $1/g_m$  when  $R_2$  is large compared to  $R_L$  and  $\$ 1 / g_m \$$ . We will revisit this important point in Chapter 4, in the context of a common-gate amplifier circuit.

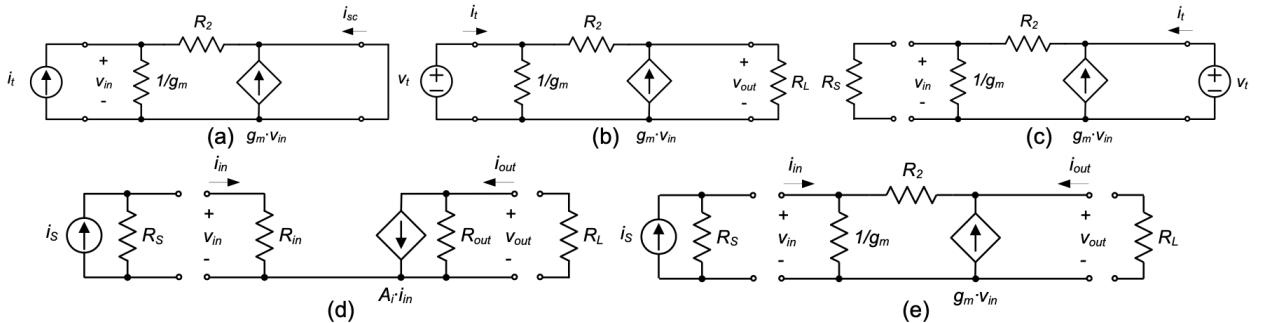


Figure 1.17.: Figure Ex1-3

Now, to find  $R_{out}$ , we apply a test voltage at the output and connect the source resistance  $R_S$  across the input port Figure 1.17. Again, we must write KCL at the two circuit nodes and solve the resulting system of equations. This yields

$$R_{out} = \frac{v_t}{i_t} = R_2 R_S + g_m R_2 R_S$$

Again, note that  $R_{out}$  is a function of  $R_S$ ; this is the case for any bilateral circuit.

Finally, to compute the transfer function based on the obtained unilateral model, we consider the circuit shown in Figure 1.17(d). By inspection, we see that

$$A'_i \frac{i_{out}}{i_s} = \left( \frac{R_S}{R_{in} + R_S} \right) A_i \frac{R_{out}}{R_L + R_{out}}$$

Substituting  $A_i$ ,  $R_{in}$ , and  $R_{out}$  from the above calculation into this expression yields

$$A'_{i,Two-Port} = \frac{i_{out}}{i_s} = \frac{R_S(1 + g_m R_2)(R_2 + R_S + g_m R_2 R_S)}{(R_L + R_2 + R_S + g_m R_2 R_S)^2}$$

We now wish to compare this result to the accurate transfer function of the circuit, obtained by direct calculation and without approximating the circuit as a unilateral two-port. For this purpose, we consider the full circuit shown in Figure 1.17(e) and write KCL for its two nodes.

$$0 = -i_s + g_m v_i n + \frac{v_{in}}{R_S} + \frac{v_{in} - v_{out}}{R_2}$$

$$0 = -g_m v_{in} + \frac{v_{out}}{R_L} + \frac{v_{out} - v_{in}}{R_2}$$

Solving this system of equations for  $v_{out}$  and substituting  $i_{out} = -v_{out}/R_L$  yields

$$A'_{i,Exact} = \frac{i_{out}}{i_s} = \frac{i_{out}}{i_s} = \frac{R_S(1 + g_m R_2)}{R_L + R_2 + R_S + g_m R_2 R_S}$$

The discrepancy factor between the two results is given by

$$\frac{A'_{i,Two-Port}}{A'_{i,Exact}} = \frac{R_2 + R_S + g_m R_2 R_S}{R_L + R_2 + R_S + g_m R_2 R_S} = \frac{1 + R_S \left( \frac{1}{R_2} + g_m \right)}{1 + \frac{R_L}{R_2} + R_S \left( \frac{1}{R_2} + g_m \right)}$$

From this result, we see that the discrepancy factor approaches unity (no error) when  $R_2$  is much larger than  $R_L$ , a condition that is often satisfied in practice (the ideal load for a current amplifier is a short circuit). In this case, the unilateral two-port model will accurately describe the behavior of the circuit.

The outcome of the above example captures the main spirit in which we justify relying on unilateral two-port models in this module. Even though the considered amplifier is strictly speaking bilateral, a unilateral model describes its behavior to within the desired engineering accuracy, provided that reasonable boundary conditions hold.

## 1. Introduction

### 1.4. Integrated Circuit Design versus Printed Circuit Board Design

In the design of analog circuits, the underlying technology has a significant impact on the choice of architecture, because it tends to restrict the availability and specification range of the underlying active and passive components. For instance, a designer working with discrete components on a printed circuit board may be subjected to the following constraints:

- Limit the component count below 100 elements to achieve a small board area.
- Resistors can be chosen in the range of  $1\Omega$ – $10M\Omega$ .
- Capacitors can be chosen in the range of  $1\text{pF}$ – $10,000\text{ F}$ .
- The resistor and capacitor values match to within 1–10%.
- The available (discrete) bipolar junction transistors match to within 20% in their critical parameters.

In contrast, the designer of a CMOS system-on-chip may face the constraints summarized below:

- Avoid using resistors; use as many MOSFET transistors as needed (within reasonable limits, on the order of hundreds to several thousands) to realize the best possible circuit implementation.
- Capacitors can be chosen in the range of  $10\text{ fF}$ – $100\text{ pF}$ .
- The critical parameters in the MOSFET transistors be made to match to within 1%, but vary by more than 30% for different fabrication runs.
- Capacitors of similar size can match to within 0.1%, but vary by more than 10% for different fabrication runs.

As a consequence of the vastly different constraints that apply to the design of analog circuits in CMOS technology, the resulting practical and preferred circuit architectures differ substantially from the ones that would be used in a printed circuit board design. For example, a discrete voltage amplifier may utilize large AC coupling capacitors to simplify and decouple the biasing of the individual gain stages (see example in Figure 1.18). In contrast, it is typically not possible to use AC coupling techniques (except for very high-frequency designs) in integrated circuits, primarily due to the restriction on maximum capacitor size.

The material covered in this module is primarily concerned with analog integrated circuit design. While this choice does not affect many of the key principles used in the analysis and the discussed circuits, it does affect the architectural choices made in arriving at a practical design. For instance, large AC coupling capacitors are not used throughout the discussion. Also, where appropriate, we will invoke certain assumptions about the typical matching of component parameters in CMOS to eliminate impractical design choices.

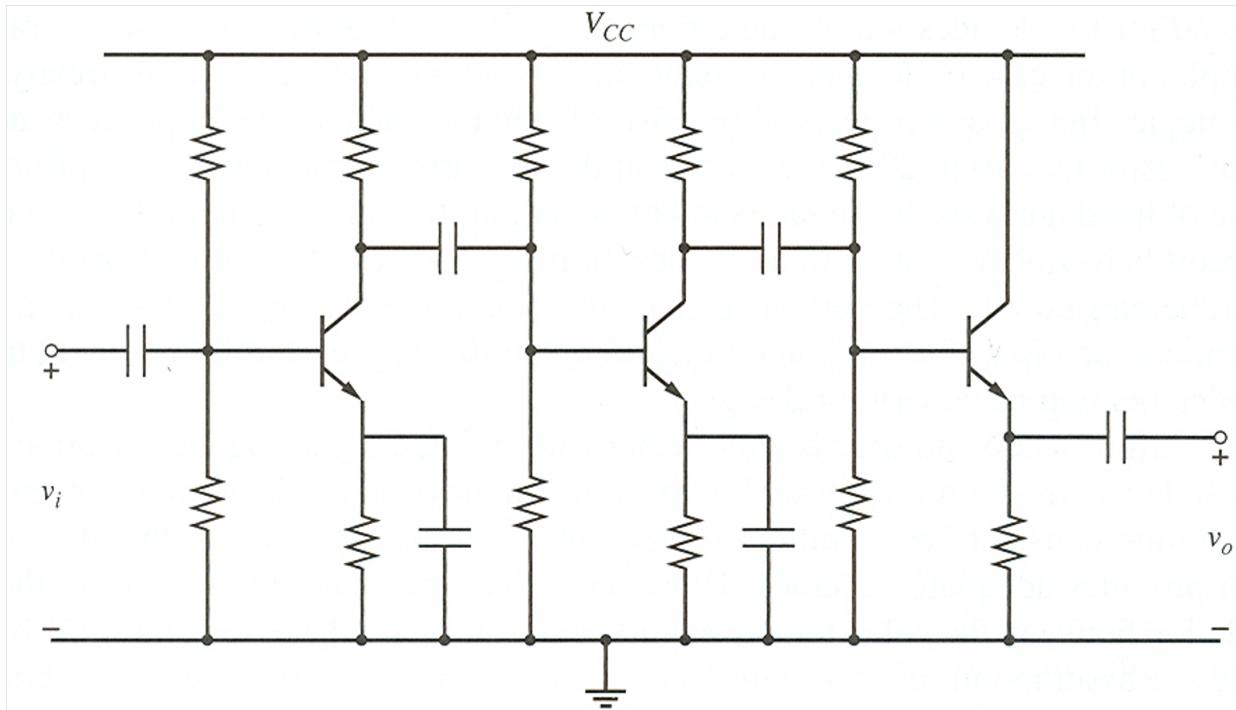


Figure 1.18.: Example of a discrete amplifier circuit using bipolar junction transistors (BJTs).

## 1.5. Prerequisites and Advanced Material

The reader of this module is expected to be familiar with the basic concepts of linear circuit analysis (see (Ulaby and Maharbiz 2013)), including

- Passive components (resistors, capacitors)
- Kirchhoff's voltage and current laws (KVL and KCL)
- Independent and dependent voltage and current sources; Thevénin and Norton representation of controlled sources
- Two-port representation of circuits; calculation of port resistances and frequency dependent impedances
- Manipulation of complex variables and numbers
- Phasor analysis and Laplace domain representation of passive circuit elements
- Bode plots

The derivations of device models in this module assume familiarity with basic solid-state physics and electrostatics as treated in introductory texts on solid-state device physics (see (Robert 2003)). A few sections of this module are marked with an asterisk (\*) to indicate advanced material that may in some cases go beyond the learning goals of an introductory course. These sections can be skipped at the instructor's discretion without affecting the overall flow and context.

## 1.6. Notation

This module follows the notation for signal variables as standardized by the IEEE. Total signals are composed of the sum of DC quantities and small signals. For example, a total input voltage  $v_{IN}$  is the sum of a DC input voltage  $V_{IN}$  and a small-signal voltage  $v_{in}$ . The notation is summarized below.

- Total quantity has a lowercase variable name and uppercase subscript
- DC quantity has an uppercase variable name and uppercase subscript
- Small-signal quantity has a lowercase variable name and lowercase subscript

## 2. Summary

This chapter offered a brief motivation for the topics covered in this module, which focuses on the analysis and design of elementary amplifier stages in CMOS technology. These elementary stages can be viewed as the “atoms” of analog circuit design and a thorough understanding of the blocks is a necessary prerequisite for the design of advanced analog circuits design, as for instance in the context of large systems-on-chip. At all levels of circuit design, complexity is managed using hierarchical abstraction and model simplification using proper engineering approximations. The unilateral two-port models reviewed in Section 1-3 and used throughout this module, are an example of such abstractions.

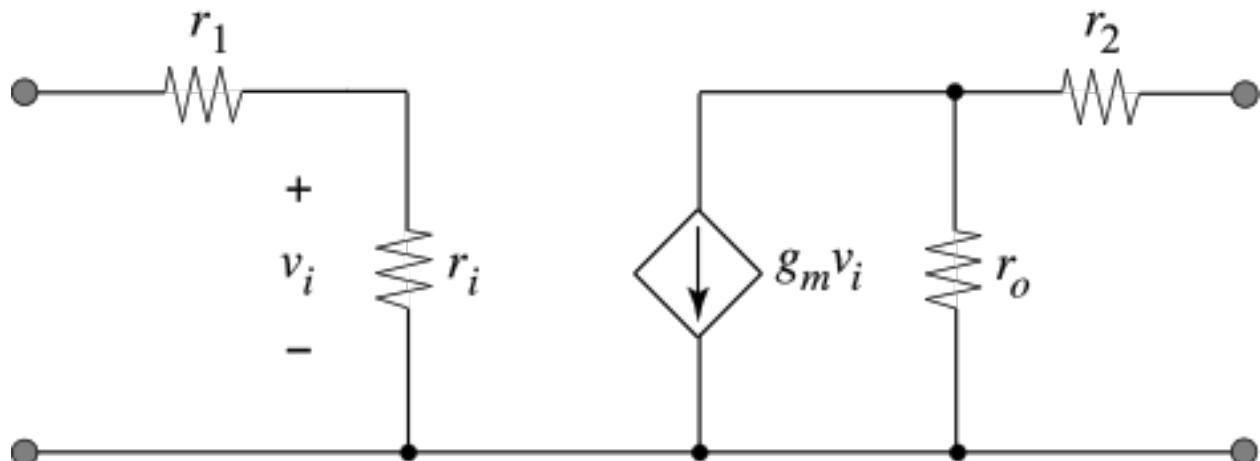


Figure 2.1.: Figure P1-1



## 3. Problems

**P1.1** Given the amplifier circuit in Figure 2.1 (a) Find the input and output resistance. (b) Construct an equivalent circuit using a voltage amplifier two-port model and determine all model parameters symbolically. (c) Repeat part (b) for a current amplifier model. (d) Repeat part (b) for a transconductance amplifier model. (e) Repeat part (b) for a transresistance amplifier model.

**P1.2** Convince yourself that the circuits of Figure 1.10 and Figure 1.12 are equivalent by showing symbolically that both circuits have the same overall voltage gain  $A'_v = v_{out} / v_s$ .

**P1.3** You are given an input voltage source with a source resistance,  $R_S$ . (a) Use the unilateral voltage amplifier two-port model found in P1.1 to find the overall voltage gain when the amplifier is driving a load resistor  $R_L$ . (b) Specify whether the resistances  $r_1, r_i, r_o, r_2$  in the small signal model should be increased, be decreased, or remain the same to improve the overall voltage gain.

**P1.4** You are given an input current source with a source resistance,  $R_S$ . (a) Use the unilateral current amplifier two-port model found in P1.1 to find the overall current gain when the amplifier is driving a load resistor  $R_L$ . (b) Specify whether the resistances  $r_1, r_i, r_o, r_2$  in the small-signal model should be increased, be decreased, or remain the same to improve the overall current gain.

**P1.5** Given the circuit model in Figure 3.1 for an amplifier circuit (a) Find the input and output resistance. (b) Construct a two-port model for a unilateral voltage amplifier. (c) Construct a two-port model for a unilateral current amplifier. (d) Construct a two-port model for a unilateral transconductance amplifier. (e) Construct a two-port model for a unilateral transresistance amplifier.

**P1.6** Consider the two-port model of a voltage amplifier as shown in Figure 1.9(a) with the following parameters:  $A_v = 10$ ,  $R_{in} = 5 \text{ k}\Omega$ , and  $R_{out} = 100 \Omega$ .

- Draw the two-port model for a transresistance amplifier by conversion from the voltage amplifier model.
- Draw the two-port model for a transconductance amplifier by conversion from the voltage amplifier model.
- Draw the two-port model for a current amplifier by conversion from the voltage amplifier model.

**P1.7** Derive an expression for the transresistance  $v_{out}/i_{in}$  for the circuit of Figure 1.7 using the following parameters:  $A_{i1} = 1$ ,  $G_{m2} = 10 \text{ mS}$ ,  $A_{v3} = 0.8$ ,  $R_{in1} = 50 \Omega$ ,  $R_{out1} = 500 \Omega$ ,  $R_{out2} = 1 \text{ k}\Omega$ , and  $R_{out3} = 100 \Omega$ . Using this result, lump the entire circuit into a single transresistance amplifier as shown in Figure 1.9(d). Draw the resulting model, including  $R_{in}$  and  $R_{out}$ .

**P1.8** Consider the amplifier circuit of Figure 1.13(a) with  $R_1 = 1/g_m = 1 \text{ k}\Omega$  and  $R_2 = 100 \text{ k}\Omega$ . Compute all component values for the bilateral two-port current amplifier model of Figure 1.13(b). Note that  $A_{if}$ ,  $R_{in}$ , and  $R_{out}$  can be described as explained in Section 1-3. Similar to  $A_{if}$ ,  $A_{ir}$  is found by short-circuiting the input port and by injecting a test current into the output port. Compare the relative magnitude of  $A_{if}$  and  $A_{ir}$ .

3. Problems

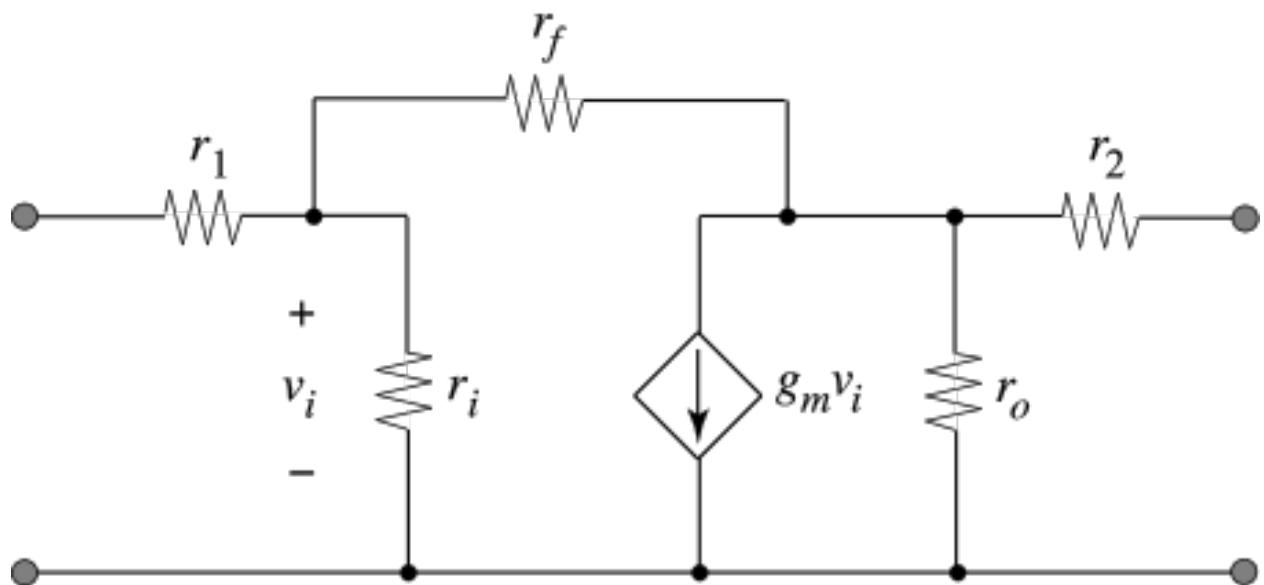


Figure 3.1.: Figure P1-5

# 4. Introduction

With the development of the integrated circuit, the semiconductor industry is undoubtedly the most influential industry to appear in our society. Its impact on almost every person in the world exceeds that of any other industry since the beginning of the Industrial Revolution. The reasons for its success are as follows:

## 💡 Chapter Objectives

- Review the MOSFET device structure and basic operation as described by the square-law model.
- Introduce large- and small-signal analysis techniques using the common-source voltage amplifier as a motivating example.
- Derive a small-signal model for the MOSFET device, consisting of a transconductance and output resistance element.
- Provide a feel for potential inaccuracies and range limitations of simple modeling expressions.

## 4.1. First-Order MOSFET Model

The device-level derivations of this section assume familiarity with basic solid-state physics and electrostatics. For a ground-up treatment from first principles, the reader is referred to introductory solid-state device material (see Reference 1).

### 4.1.1. Derivation of I-V Characteristics

The basic structure of an **enhancement mode n-channel** MOSFET is shown in Figure 4.1(a). It consists of a lightly doped p-substrate (**bulk**), two heavily doped n-type regions (**source** and **drain**) and a conductive gate electrode that is isolated from the substrate using a thin silicon dioxide layer of thickness  $t_{ox}$ . Other important geometry parameters of this device include the **channel length L** (distance between the source and drain) and the **channel width W**.

As we shall see, the name “n-channel” stems from the fact that this device conducts current by forming an n-type layer underneath the gate. A **p-channel** device can be constructed similarly using an n-type bulk and p-type source/drain regions. The differentiating details between n- and p-channel devices are summarized in Section 2-1-2. For the time being, we will use the n-channel device to discuss the basic principles.

In order to study the electrical behavior of a MOSFET, it is useful to define a schematic symbol and conventions for electrical variables as shown in Figure 4.1(b) . The variables  $V_{GS}$ ,  $V_{DS}$ , and  $V_{BS}$

#### 4. Introduction

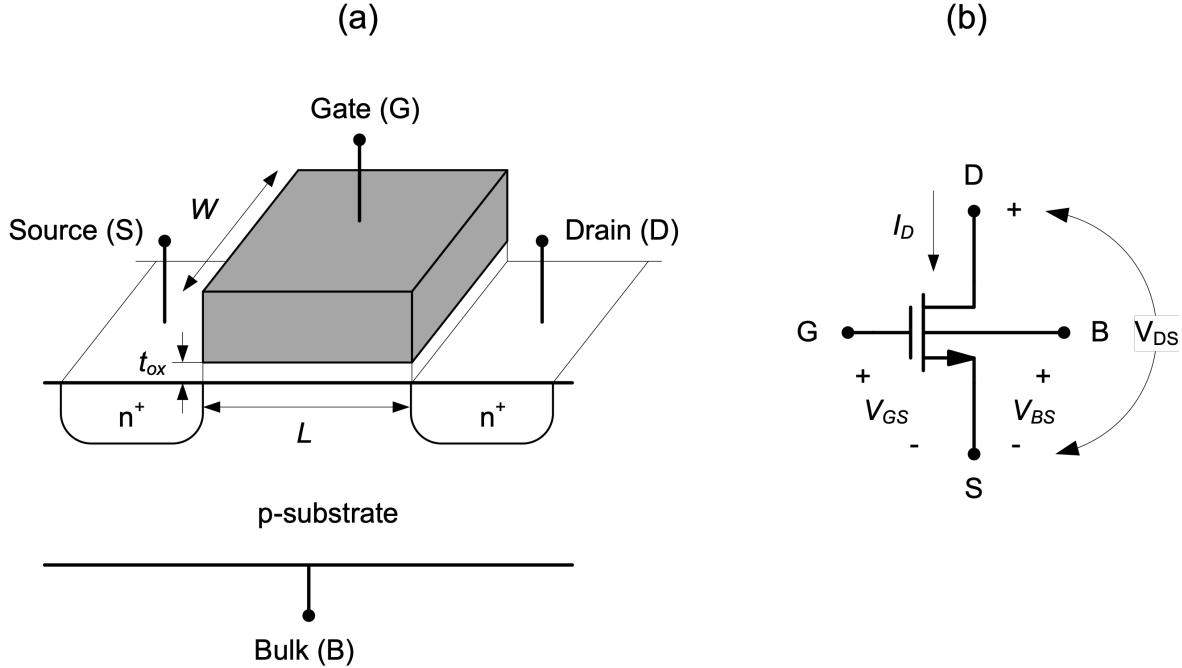


Figure 4.1.: (a) Cross-section of an n-channel MOSFET.

describe the voltages between the respective terminals using the commonly used ordered subscript convention  $V_{XY} = V_X - V_Y$ . The current flowing into the drain node is labeled  $I_D$ .

It is important to note that the MOSFET device considered here is perfectly symmetric; i.e., the drain and source terminal labels can be interchanged. It is a common convention to assign the source to the lower potential of these two terminals, since this terminal is the source of electrons that enable the flow of current. We will see later that this convention, together with the arrow that marks the source (and the direction of current flow), provides useful intuition when reading a larger circuit schematic.

We now begin our analysis of the MOSFET device by considering the condition shown in Figure 4.2(a), where the bulk and source are connected to a reference potential (GND),  $V_{GS} = 0$  V and  $V_{DS} = 0$  V. Under this condition, the drain and source terminals are isolated by two reverse-biased pn-junctions and their **depletion regions**, which prevent any significant flow of current. Applying a positive voltage at the drain ( $V_{DS} > 0$  V) increases the reverse-bias at the drain-bulk junction and will only increase the width of the depletion region at the drain, while  $I_D = 0$  is still maintained (to first-order).

Consider now  $V_{GS} = 0$  as shown in Figure 4.2(b). This positive voltage at the gate attracts electrons from the source. With increasing  $V_{GS}$ , a larger amount of electrons is supplied by the source, and ultimately, a so-called **inversion layer** forms underneath the gate. The voltage  $V_{GS}$  at which a significant number of mobile electrons underneath the gate become available is called the **threshold voltage** of the transistor, or  $V_t$ . In order to differentiate the threshold voltages and other device parameters of n-and p-channel devices, we will utilize the subscripts n and p throughout this module. E.g., we denote the threshold voltage for n-channels and p-channels as  $V_{Tn}$  and  $V_{Tp}$ , respectively.

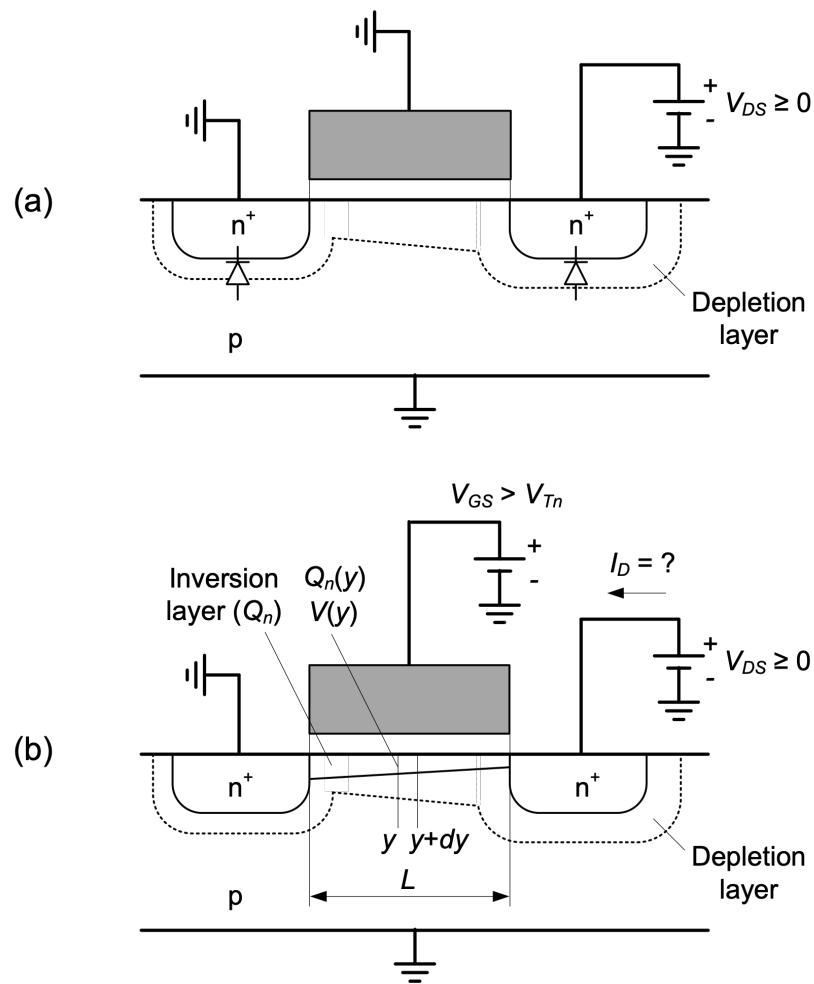


Figure 4.2.: (a) n-channel MOSFET with  $V_{GS} = 0$ , (b)  $V_{GS} > V_{Tn}$ ,

#### 4. Introduction

With the inversion layer under the gate, the drain and source regions are now “connected” through a conductive path and any voltage between these terminals ( $V_{GS} > 0$ ) will result in a flow of drain current. How can we calculate this current? In order to answer this question, the following approximations are useful:

1. The current primarily depends on the number of mobile electrons in the channel times their velocity.
2. The number of mobile electrons in the channel is set by the vertical electric field from the gate to the conductive channel (**gradual channel approximation**).
3. The threshold voltage is constant along the channel; this assumption neglects the so-called body effect.
4. The velocity of the electrons traveling from the source to the drain is proportional to the lateral electric field in the channel.

Figure 4.2(b) establishes relevant variables for further analysis. The auxiliary variable  $y$  ranges from 0 to  $L$  and is used to express electrical quantities as a function of the distance from the source. The inversion layer charge density (per unit area) and voltage at position  $y$  in the channel are denoted as  $Q_n(y)$  and  $V_y$ , respectively. With these conventions in place, we can translate the above-listed assumptions into the following equations:

$$I_D = -W \cdot Q_n \cdot v(y) \quad (4.1)$$

$$Q_n(y) = -C_{ox} \cdot (V_{GS} - V(y) - V_{Tn}) \quad (4.2)$$

$$v(y) = -\mu_n \cdot E_y \quad (4.3)$$

In these expressions,  $v$  is the velocity of the carriers,  $C_{ox}$  is the **gate capacitance** per unit area (between the gate electrode and the conductive channel). The term  $\mu_n$  is called **mobility**, and it relates the drift velocity of the carriers to the local electric field.

As indicated in Equation 4.2, the mobile charge density at coordinate  $y$  depends on the local potential, since the voltage across the oxide is given by  $V_{GS} - V(y)$ . An inversion layer is present at any location under the gate where this voltage difference is larger than the threshold ( $V_{Tn}$ ). Assuming that the inversion layer extends from source to drain as drawn in Figure 4.2(b), we have  $V(L) = V_{DS}$  and  $Q_n(L) = -C_{ox} (V_{GS} - V_{Tn} - V_{DS})$ . This implies that  $V_{DS}$  cannot exceed  $V_{GS} - V_{Tn}$  for an inversion layer that extends across the entire channel. For the time being, we will solve for the drain current for this condition and later extend the obtained result for the case of  $V_{DS} = V_{GS} - V_{Tn}$ .

Now, by combining Equation 4.1 through Equation 4.3 and noting that the electric field is given by  $E(y) = -dV(y)/dy$ , we can write

$$I_D(y) = \mu_n C_{ox} W \cdot (V_{GS} - V_y - V_{Tn}) \frac{dV_y}{dy} \quad (4.4)$$

#### 4.1. First-Order MOSFET Model

This result describes the current density profile along the channel. The terminal current,  $I_D$ , can be found by separating the variables and integrating along the direction of  $y$

$$\int_0^L I_D(y) dy = \mu_n C_{ox} W \int_0^{V_{DS}} (V_{GS} - V(y) - V_{Tn}) dV \quad (4.5)$$

which yields a closed-form solution for the drain current

$$I_D = \mu_n C_{ox} \frac{W}{L} \left( V_{GS} - V_{Tn} - \frac{V_{DS}}{2} \right) V_{DS} \quad (4.6)$$

Note that this expression is valid for  $V_{DS} < V_{GS} - V_{Tn}$ , as assumed above. In order to extend the obtained result for  $V_{DS} = V_{GS} - V_{Tn}$ , we continue by inspecting the shape of the inversion layer for various  $V_{DS}$  (see Figure 4.3). For  $V_{DS} = 0$  V [case (a)], no current flows and  $V(y) = 0$  for all  $y$ . Provided that  $V_{GS} > V_{Tn}$ , a uniform inversion layer exists underneath the gate. For small  $V_{DS} > 0$ , a current flows in the inversion layer, which causes increasing  $V(y)$  and decreasing inversion layer charge along the channel. As  $V_{DS}$  approaches  $V_{GS} - V_{Tn}$ ,  $Q_n(L)$  approaches zero with a point of diminishing charge at the drain. This effect is called **pinch-off**.

What happens when we increase  $V_{DS}$  beyond the point of pinch-off? Further analysis based on solving the two-dimensional **Poisson Equation** at the drain predicts that the pinch-off point will move from  $L$  to  $L - \Delta L$ , where  $\Delta L$  is small relative to  $L$ . Even though no inversion layer exists in the region from  $L - \Delta L$  to  $L$ , the device still conducts current. The charges arriving at  $y = L - \Delta L$  are being swept to the drain by the electric field present in the depletion region of the surrounding pn junction.

To first-order, and neglecting the small change in channel length  $\Delta L$ , the current becomes independent of  $V_{DS}$  and is approximately given by the current at the onset of pinch-off, i.e., at  $V_{DS} = V_{GS} - V_{Tn}$ . Substituting this condition into Equation 4.6, we obtain

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Tn})^2 \quad (4.7)$$

for  $V_{DS} > V_{GS} - V_{Tn}$ .

Equation 4.6 and Equation 4.7 are plotted in Figure 4.4 as a function of  $V_{DS}$  and some fixed  $V_{GS} > V_{Tn}$ . The operating region for  $V_{DS} < V_{GS} - V_{Tn}$  is commonly called the **triode region**. This name stems from the direct dependence of the drain current on the drain-source voltage, which is qualitatively similar to the behavior of vacuum tube “triodes.” The region  $V_{DS} > V_{GS} - V_{Tn}$  is called the **saturation region** due to the saturation in current at large  $V_{DS}$ . In this region, the device operates essentially like a current source; the current is (to first-order) independent of the applied  $V_{DS}$  and  $I_D = I_{Dsat} = \text{constant}$ . The quantity  $V_{GS} - V_{Tn}$  is often called **gate overdrive**.

The drain-source voltage at which the drain current saturates is called  $V_{DSat}$ . From the above first-order analysis, it is clear that  $V_{DSat} = V_{GS} - V_{Tn}$ . Nonetheless, it is useful to distinguish between these two quantities, because they may differ significantly when a more elaborate device model is used.  $V_{DSat}$  is generally not exactly equal to  $V_{GS} - V_{Tn}$  when second-order effects, for example related to small geometries and modern device structures, are considered.

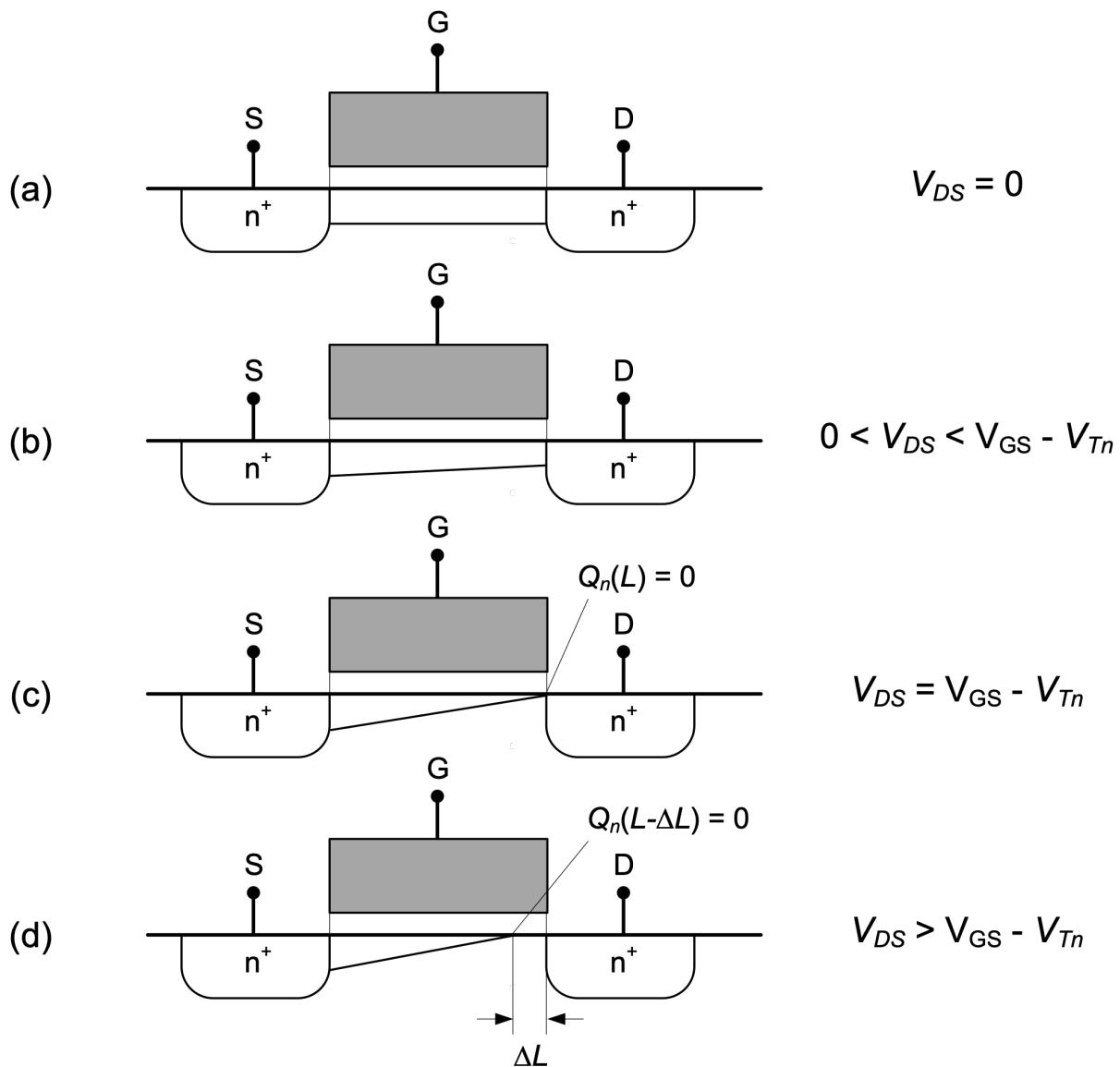


Figure 4.3.: Channel profile for varying  $V_{DS}$ .

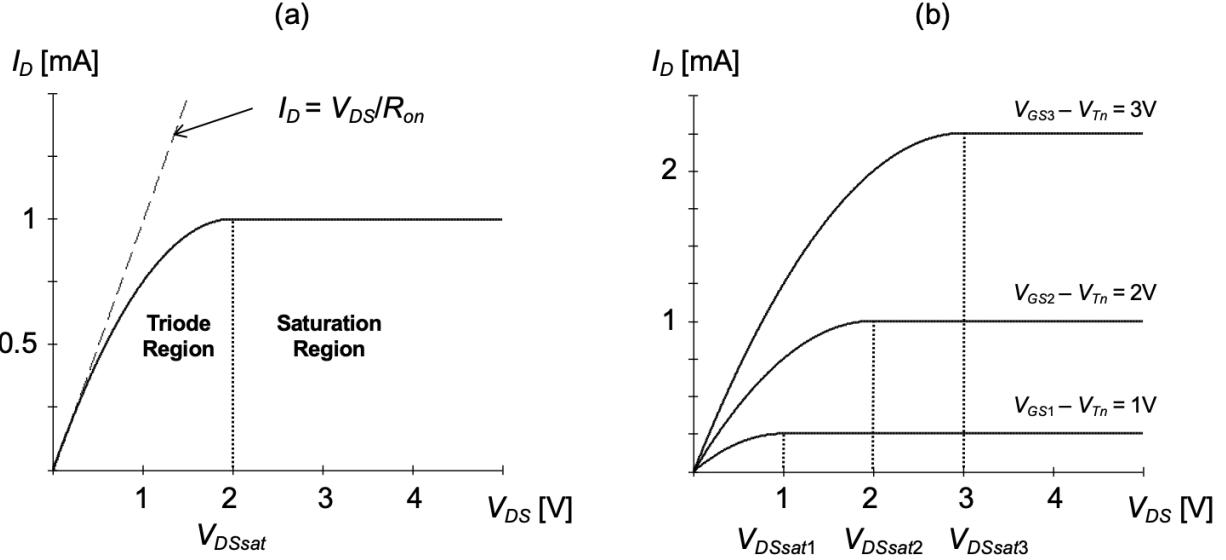


Figure 4.4.: (a) n-channel I-V characteristic for a fixed value of  $V_{GS} - V_{Tn} = 2V$ . (b) I-V plots with varying  $V_{GS} - V_{Tn}$  (drain characteristic). Parameters:  $\mu C_{ox} = 50 \mu A/V^2$  and  $W/L = 10$ .

From a circuit perspective, the device's behavior in the triode region is similar to a resistor: the current increases monotonically with increasing terminal voltage. Even though the dependence of  $I_D$  on  $V_{DS}$  is nonlinear (as seen from Equation 4.6), it is sometimes useful to approximate the characteristic using a linear I-V law, shown as a dashed line in Figure 4.4(a). For  $V_{DS} \ll V_{GS} - V_{Tn}$ , we can approximate Equation 4.6 as

$$I_D \equiv \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Tn}) V_{DS} \quad (4.8)$$

Under this approximation,  $I_D$  depends linearly on  $V_{DS}$ , and we can define the so-called **on-resistance** of the device as

$$R_{on} = \frac{V_{DS}}{I_D} \equiv \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Tn})} \quad (4.9)$$

It is interesting to interpret the dependencies in this expression using basic intuition. Increasing the aspect ratio  $W/L$  decreases  $R_{on}$  since the conductive path becomes shorter and/or wider; this is a basic property of any conductor. The on-resistance also decreases with increasing  $C_{ox}$  and  $V_{GS} - V_{Tn}$ ; this is because the inversion charge increases with these quantities ( $Q = CV$ ). Larger mobility ( $\mu_n$ ) means that the carriers travel faster for the same applied voltages (electric field). This increases the current (charge per unit of time) and therefore also results in smaller  $R_{on}$ .

As seen from Equation 4.7, the magnitude of the drain current in saturation depends on the square of the gate overdrive  $V_{GS} - V_{Tn}$ . This is further illustrated in Figure 4.4(b), which shows I-V plots for increasing multiples of  $V_{GS1} - V_{Tn} = 1V$ . Doubling and tripling the gate overdrive

#### 4. Introduction

increases the saturation current by factors of four and nine, respectively. Note that  $R_{on}$  is reduced only by factors of two and three in these cases, respectively.

The plot in Figure 4.4(b) is often called the **drain characteristic**, because the drain-source voltage (as opposed to the gate-source voltage, which is included as a parameter on the curves), is swept along the x-axis. Alternatively, the term **output characteristic** is sometimes used, primarily because  $V_{DS}$  can often be viewed as the output port voltage of the device; we will see this in the example discussed in Section 2-2.

Another commonly used characterization plot for MOSFETs is the so-called **transfer characteristic**, which shows the drain current as a function of  $V_{GS}$  for a fixed value of  $V_{DS}$ . If  $V_{DS}$  is chosen large enough such that the device operates in the saturation region for all applied  $V_{GS}$ ,  $I_D$  follows from Equation 4.7 and the plot is shaped like a parabola as drawn in Figure 4.5.

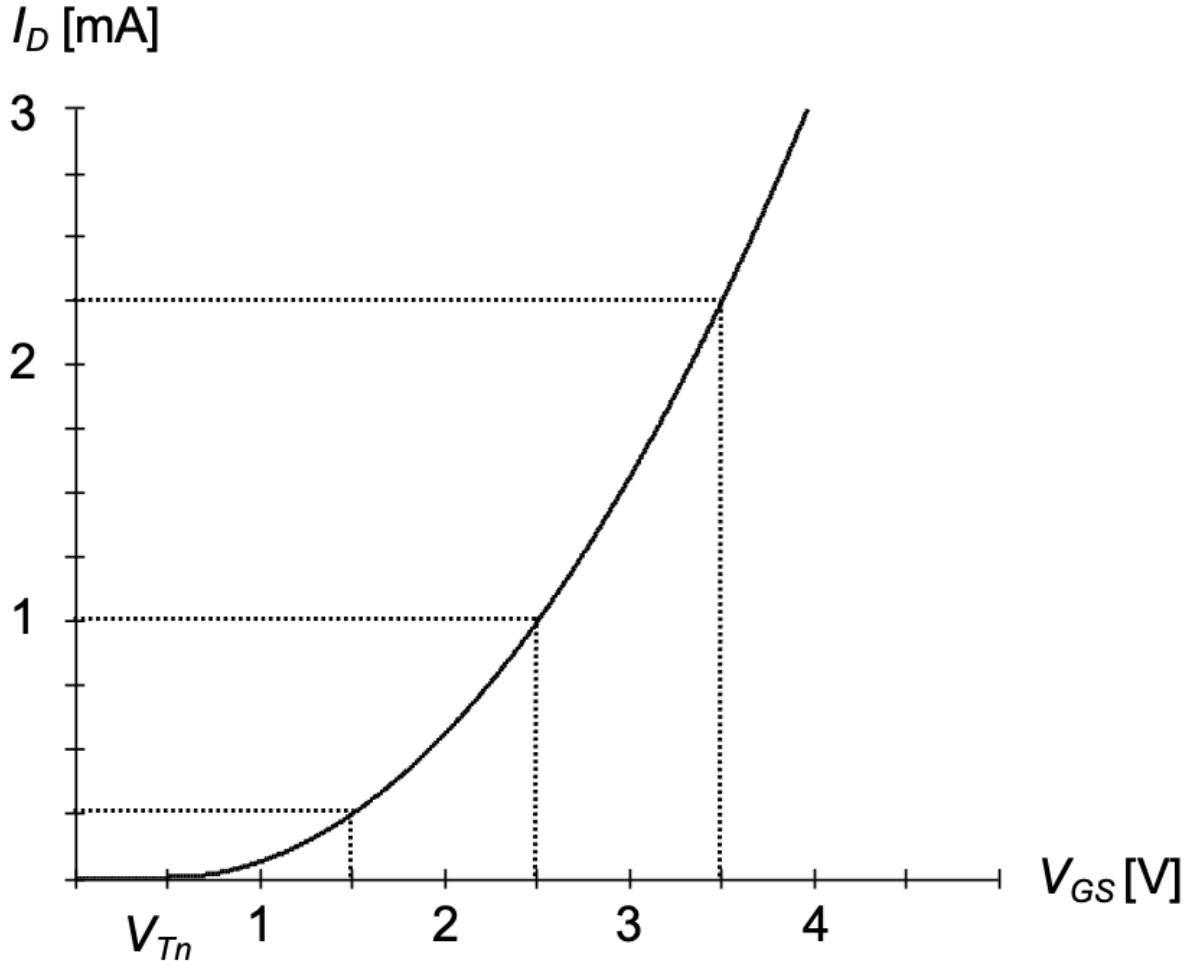


Figure 4.5.: Plot of n-channel drain current as a function of  $V_{GS}$  (transfer characteristic). Parameters:  $V_{DS} = 5$  V,  $\mu C_{ox} = 50$  A/V<sup>2</sup>,  $V_{Tn} = 0.5$  V, and  $W/L = 10$ .

Table 4.1 summarizes the first-order MOSFET I-V relationships that were discussed in this section. This set of equations (and extended versions thereof) is often called the **square-law model** since one of its primary features is the quadratic dependence of the saturation current on  $V_{GS} - V_{Tn}$ .

When working with this device model, it is important to remember that it predicts the behavior of real MOSFETs only with limited accuracy. This is primarily so because we have made several simplifications in the model's derivation. The most significant shortcomings that result from these assumptions can be summarized as follows:

1. In reality, the saturation current has a weak dependence on  $V_{DS}$ . This is primarily due to a shortening of the channel length ( $\Delta L$ ) with increasing  $V_{DS}$  and also due to the drain voltage dependence of the mobile charge in the channel. We will address this issue in Section 2-2.
2. For transistors built in modern technologies, several second-order effects related to small geometries and large electric fields become significant. This typically results in a saturation current law exponent that is less than two, and  $V_{DSat} < V_{GS} - V_{Tn}$ . In addition, the drain current does not scale strictly proportional to  $1/L$  and the threshold voltage is not constant, but a function of the drain voltage.
3. For  $V_{GS} < V_{Tn}$  the device is not completely off, but carries a small current that exponentially depends on  $V_{GS}$ . This operating region is called the **sub-threshold region**.
4. For small values of  $V_{GS} < V_{Tn}$ , on the order of a few tens of millivolts, the region underneath the gate is only moderately inverted, and the square law model tends to predict the drain current with poor accuracy.

Table 4.1.: First-order MOSFET model summary

	“ON” $V_{GS} \geq V_{Tn}$	“OFF” $V_{GS} < V_{Tn}$
$V_{DS} < V_{DSat}$	$I_D = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Tn} - \frac{V_{DS}}{2}) V_{DS}$	$I_D = 0$
$V_{DS} \geq V_{DSat}$	$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Tn})^2$	$I_D = 0$

Despite these shortcomings, the first-order MOSFET model possesses many of the critical features needed to study the fundamentals of analog circuit design. Many of the second-order effects not featured in the basic model can be treated using advanced device physics and often result in a high-complexity model that is unsuitable for hand-calculations and intuition building.

Within the range of circuits treated in this module, we typically begin by applying the first-order model. Then, only when the circuit appears to be sensitive to second-order dependencies not covered by this model, we will look for extensions. A treatment in this fashion has the advantage that the reader can develop a feel for where and when modeling extensions and parameter accuracy are critical.

In general, the tradeoff between modeling accuracy and complexity is a recurring theme at all levels of analog circuit design; the issue is not limited to the introductory material covered in this module. More accurate models can always be generated at the expense of complexity and time. An experienced analog designer will often use the simplest possible model that will predict the behavior of his or her circuit with sufficient (but not perfect) accuracy. This also implies that analog circuit designers must always be on the lookout for model inadequacies. We will encounter and discuss situations where either model expansions or critical insight on modeling accuracy are needed throughout this module.

## 4. Introduction

### 4.1.2. P-Channel MOSFET

The n-channel MOSFET discussed so far conducts current through an electron inversion layer in a p-type bulk. Similarly, we can construct a **p-channel** device that operates based on forming an inversion layer of holes in an n-type bulk. The structure of such a MOSFET, which consists of *p+* source and drain regions in an n-type bulk, is shown in Figure 4.6. In many process technologies, the n-type bulk region is formed by creating an n-type well (**n-well**) in the p-type substrate that is used to form n-channels. Such a technology is called an **n-well technology**. In general, a technology that offers both n- and p-channel devices is called **CMOS** technology, where CMOS stands for Complementary Metal-Oxide-Semiconductor.

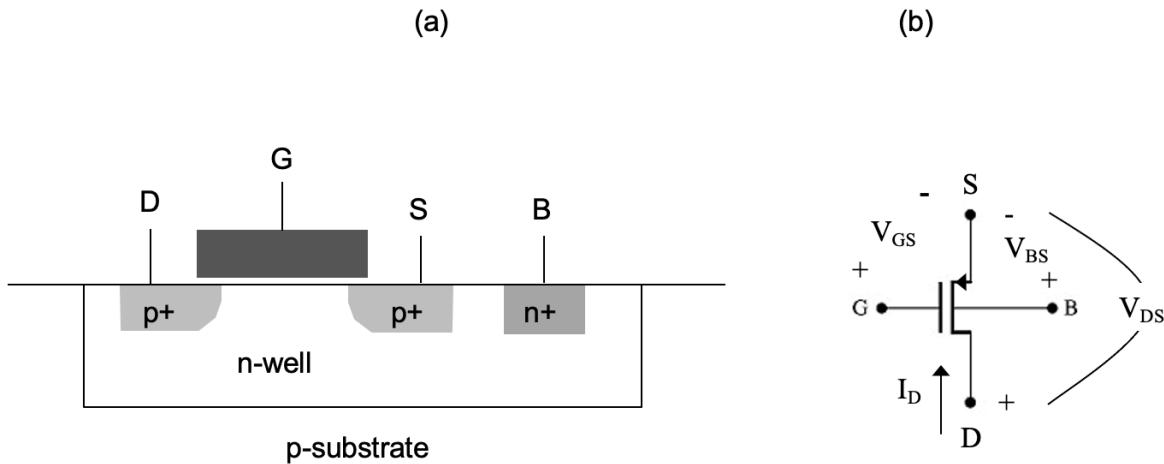


Figure 4.6.: (a) Cross-section of a p-channel MOSFET. (b) Schematic symbol.)

The drain current equations for a p-channel MOSFET can be derived using exactly the same approach as used for the n-channel device since the basic physics are the same. For a p-channel device, the gate must be made negative with respect to the p-type source in order to form an inversion layer of holes; the threshold voltage  $V_{Tp}$  is therefore typically negative. Since holes drift across the channel from the source to the drain in the p-channel MOSFET, the drain voltage must be negative with respect to the source, and the drain current (defined as flowing into the drain terminal) is negative. Therefore, in the on-state of the transistor,  $V_{GS}$  and  $V_{DS}$  are negative quantities, and the source lies at the highest potential among the four terminals. The drain current for a p-channel in saturation, i.e.,  $V_{GS} < V_{DS}$  and  $V_{DS} - V_{GS} - V_{Tp}$ , is given by

$$I_D = -\frac{1}{2}\mu_p C_{ox} \frac{W}{L} (V_{GS} - V_{Tp})^2 \quad (4.10)$$

A practical problem for the circuit designer is to keep track of the minus signs and negative quantities in the p-channel equations. A solution to this issue is to “think positive,” and work with the physically intuitive positive quantities  $V_{SG}$  (instead of  $V_{GS}$ ),  $V_{SD}$  (instead of  $V_{DS}$ ) in all hand calculations. Following this approach, we can rewrite Equation 4.10 as

$$-I_D = \frac{1}{2}\mu_p C_{ox} \frac{W}{L} (V_{GS} - V_{Tp})^2 \quad (4.11)$$

Note that the right-hand side of this equation yields a positive number. The minus sign included on the left-hand side remains necessary because  $I_D$ , as defined in Figure 4.6(b), is a negative quantity.

### 4.1.3. Standard Technology Parameters

For use throughout this module, it is convenient to define standard MOSFET parameter values as given in Table 4.2. The chosen values are representative of a CMOS technology with a minimum channel length, or **feature size** of 1  $\mu\text{m}$ . As we learn more about the behavior of MOSFETs in later sections, this list of parameters will grow and we will augment it as needed.

In the context of defining these parameters, it is important to make a clear distinction between **technology parameters** and **design parameters**. Technology parameters are typically fixed in the sense that a circuit designer cannot alter their values. For instance, the mobility in a MOSFET depends on how the transistor is made, and the underlying recipe remains unchanged and will be reused for an extended time to manufacture a large variety and quantity of integrated circuits. In most modern CMOS technologies, the width and length of a MOSFET remain as the only parameters that the circuit designer can choose (within appropriate limits) to alter the device's electrical behavior.

In determining the transistor geometries, the designer will usually work with electrical variables and parameters that describe the circuit and its functionality, for example in terms of currents and voltages. From these electrical descriptions and specifications, the widths and lengths of the transistors are then calculated, and sometimes adjusted via an iterative process. In this task, intermediate electrical parameters, as for instance the gate overdrive of a MOSFET, are also legitimately viewed as parameters that are under the control of the circuit designer.

#### Example 2-1: P-Channel Drain Current Calculation

A p-channel transistor is operated with the following terminal voltages relative to ground:  $V_G = 2.5 \text{ V}$ ,  $V_S = V_B = 5 \text{ V}$ ,  $V_D = 1 \text{ V}$ . Calculate the drain current  $I_D$  using the standard technology parameters given in Table 4.2 and assuming  $W/L = 5$ .

#### SOLUTION

From the given terminal voltages, we find  $V_{SG} = 5 \text{ V} - 2.5 \text{ V} = 2.5 \text{ V}$  and  $V_{SD} = 5 \text{ V} - 1 \text{ V} = 4 \text{ V}$ . Since  $V_{SG} > V_{Tp}$ , the transistor is on, and since  $V_{SD} > V_{SG} + V_{Tp} = 2.5 \text{ V} - 0.5 \text{ V} = 2 \text{ V}$ , it operates in saturation. Therefore, using Equation 4.11 we find

$$\begin{aligned} -I_D &= \frac{1}{2}\mu_p C_{ox} \frac{W}{L} (V_{GS} - V_{Tp})^2 \\ -I_D &= \frac{1}{2} \cdot 25 \frac{\mu\text{A}}{\text{V}^2} \cdot 5 \cdot (2.5\text{V} - 0.5\text{V})^2 = 250\mu\text{A} \\ -I_D &= -250\mu\text{A} \end{aligned}$$

#### 4. Introduction

Table 4.2.: Standard technology parameters for the first-order MOSFET model

Parameter	n-channel MOSFET	p-channel MOSFET
Threshold voltage	$V_{Tn} = 0.5V$	$V_{Tp} = -0.5V$
Transconductance parameter	$\mu_n C_{ox} = 50\mu A/V^2$	$\mu_p C_{ox} = 25\mu A/V^2$

## 4.2. Building a Common-Source Voltage Amplifier

We will now utilize our first-order understanding of MOSFETs to construct a basic voltage amplifier. We begin by noting that the drain current in all regions of operation can be controlled by varying the gate-source voltage. One way to utilize this effect to build a voltage amplifier is to apply the input such that it controls  $V_{GS}$ . An output voltage can then be generated by letting the drain current flow through a resistor, as shown in Figure 4.7(a). The top terminal of the resistor is connected to a **supply voltage**,  $V_{DD}$ . In this scheme, a larger  $V_{IN}$  causes the drain current to increase and  $V_{OUT}$  to decrease, since a larger  $V_{IN}$  makes the transistor a “better conductor” (more inversion charge), which forces the voltage at the output port closer to ground. This type of circuit is therefore categorized as an **inverting amplifier**. Furthermore, this transistor stage is called a **common-source amplifier**, since the source terminal of the MOSFET is common to the input and output ports of the circuit.

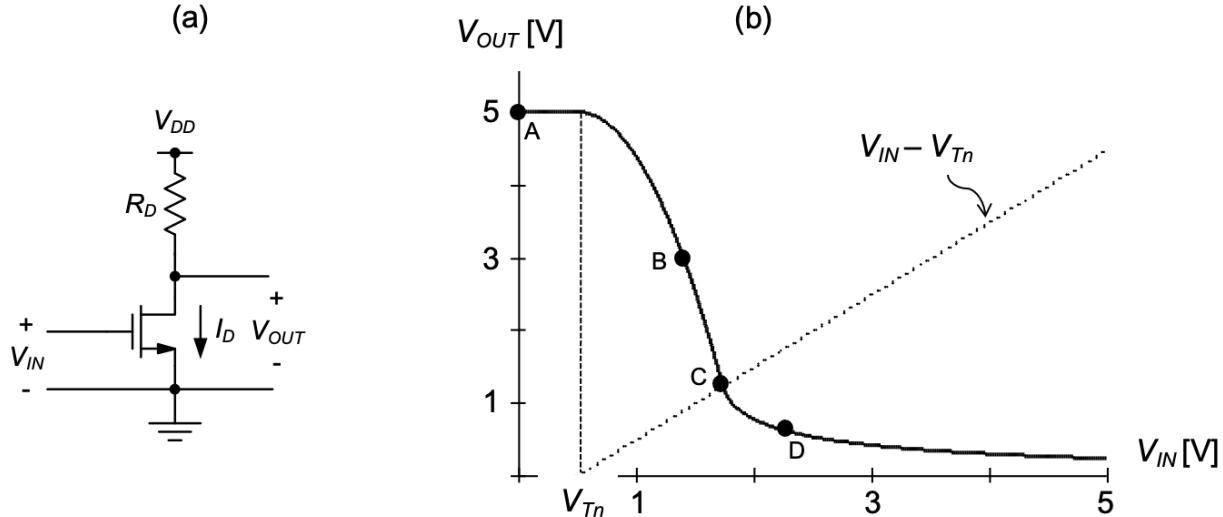


Figure 4.7.: (a) Basic common-source amplifier schematic. (b) Voltage transfer characteristic for  $V_{DD} = 5 V$ ,  $R_D = 5 k\Omega$ , and  $W/L = 20$ .

### 4.2.1. Voltage Transfer Characteristic

In order to derive the voltage transfer characteristic of the circuit ( $V_{OUT}$  as a function of  $V_{IN}$ ) we begin by applying Kirchhoff's laws at the output node. This yields

$$V_{OUT} = V_{DD} - I_D R_D \quad (4.12)$$

The drain current  $I_D$  in this expression depends on  $V_{GS}$  and  $V_{DS}$  of the transistor, as described in Table 4.1. Given the structure of the circuit in Figure 4.7(a), we note that  $V_{GS} = V_{IN}$  and  $V_{DS} = V_{OUT}$ . Using this information, we can construct a piecewise function that relates the input and output voltages of the circuit. For this derivation, imagine that we sweep  $V_{IN}$  from 0 V to the supply voltage,  $V_{DD}$ .

First, we note that for  $V_{IN} = V_{GS} < V_{Tn}$ , no current flows in the transistor; this implies  $V_{OUT} = V_{DD}$ . This behavior is shown in Figure 4.7(b) as a horizontal line for the input voltage range  $0 \leq V_{IN} < V_{Tn}$ , between points A and the vertical line at  $V_{Tn}$ . As  $V_{IN}$  increases to values greater than or equal to  $V_{Tn}$ , the transistor conducts current, and  $V_{OUT}$  must be less than  $V_{DD}$ . In order to calculate how  $V_{OUT}$  changes as a function of  $V_{IN}$ , we must first determine the transistor's region of operation. As we increase  $V_{IN}$  above  $V_{Tn}$ , does the MOSFET operate in saturation or in the triode region?

To answer this question, we must determine if  $V_{DS}$  is smaller or larger than  $V_{GS} - V_{Tn}$ . For  $V_{IN}$  just above  $V_{Tn}$ ,  $V_{GS} - V_{Tn}$  is smaller than  $V_{DS}$ , which is still close to  $V_{DD}$  at the onset of current conduction. Therefore, the device must initially operate in saturation as we transition from the "OFF" state of the transistor into the region where  $I_D > 0$ . Under this condition, the output voltage is given by

$$V_{OUT} = V_{DD} - R_D \cdot \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{IN} - V_{Tn})^2 \quad (4.13)$$

and the voltage transfer characteristic shows a drop that is quadratic in  $V_{IN}$  as seen in Figure 4.7(b).

As we continue to increase  $V_{IN}$ ,  $V_{GS} - V_{Tn}$  also increases while  $V_{OUT}$  continues to decrease. At a sufficiently large  $V_{IN}$ ,  $V_{DS}$  can approach  $V_{GS} - V_{Tn}$  and the condition for current saturation may no longer hold; the device then transitions into the triode region. The input voltage at which this transition occurs (point C in Figure 4.7(b)) can be computed by setting the right-hand side of Equation 4.13 equal to  $V_{IN} - V_{Tn}$ , and solving for  $V_{IN}$ . It is interesting to note that graphically, point C can be found through the intersection of the voltage transfer characteristic with the line  $V_{IN} - V_{Tn}$ . The intersect corresponds to the point where  $V_{OUT} = V_{DS} = V_{IN} - V_{Tn} = V_{GS} - V_{Tn}$ , i.e., the transition point between saturation and triode for the MOSFET.

For the region where the MOSFET operates in the triode region, we have

$$V_{OUT} = V_{DD} - R_D \cdot \mu_n C_{ox} \frac{W}{L} (V_{IN} - V_{Tn} - \frac{V_{OUT}}{2}) V_{OUT} \quad (4.14)$$

Unfortunately, solving this expression for  $V_{OUT}$  yields an unwieldy square-root expression that is best analyzed graphically. As we can see from the plot in Figure 4.7(b), the most important feature here is that the slope of the voltage transfer characteristic diminishes for large  $V_{IN}$ ; i.e., the slope of the curve at point D is smaller than the slope at point C. Qualitatively, this can be explained by viewing the MOSFET as a resistor, whose value continues to decrease with  $V_{IN}$ . For very large  $V_{IN}$ , the output voltage must asymptotically approach 0 V. This can be shown by approximating the MOSFET by its on-resistance for small  $V_{DS}$  as given by Equation 4.9. The output voltage in

#### 4. Introduction

the vicinity of point  $D$  can then be expressed by considering the resistive voltage divider formed by  $R_D$  and  $R_{on}$ .

$$V_{OUT} \approx \frac{V_{DD} \cdot R_{on}}{R_D + R_{on}} = \frac{V_{DD}}{1 + R_D \cdot \mu_n C_{ox} \frac{W}{L} (V_{IN} - V_{Tn})} \quad (4.15)$$

This result confirms that for large input voltages,  $V_{OUT}$  will asymptotically approach zero.

#### Example 2-2: Voltage Transfer Calculations for a Common-Source Amplifier

Consider the circuit of Figure 4.7(a) with the following parameters:  $V_{DD} = 5 \text{ V}$ ,  $R_D = 10 \text{ k}\Omega$ .

- Using the standard technology parameters of Table 4.2, calculate the required aspect ratio  $W/L$  such that  $V_{OUT} = 2.5 \text{ V}$  for  $V_{IN} = 1 \text{ V}$ .
- Assuming  $W/L = 10$ , calculate the input voltage  $V_{IN}$  that yields  $V_{OUT} = 2.5 \text{ V}$ .

#### SOLUTION

- As a first step, we can calculate the drain current that results in  $V_{OUT} = 2.5 \text{ V}$  using Equation 4.12.

$$V_{OUT} = V_{DD} - I_D R_D$$

$$2.5\text{V} = 5\text{V} - (I_D \cdot 10\text{k}\Omega)$$

$$I_D = 250\text{A}$$

Since  $V_{GS} - V_{Tn} = 0.5 \text{ V} < V_{DS} = 2.5 \text{ V}$ , we know that the device must operate in the saturation region. Therefore,

$$\begin{aligned} I_D &= \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Tn})^2 \\ 250\text{A} &= \frac{1}{2} \cdot 50 \frac{\text{A}}{\text{V}^2} \cdot \frac{W}{L} \cdot (1\text{V} - 0.5\text{V})^2 \end{aligned}$$

and solving for the aspect ratio yields  $W/L = 40$ . Note that this answer can also be found by direct evaluation of Equation 4.13, without computing  $I_D$  initially.

- since  $V_{IN}$  is unknown in this part of the problem, we cannot immediately determine the operating region of the MOSFET. In such a situation, it is necessary to guess the operating region, and later test whether the guess was correct. Let us begin by assuming that the device operates in saturation. We can then write

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Tn})^2$$

$$250A = \frac{1}{2} \cdot 50 \frac{A}{V^2} \cdot 10 \cdot (V_{GS} - 0.5V)^2$$

The two solutions to this equation are  $V_{GS1} = 1.5$  V, and  $V_{GS2} = -0.5$  V. Since we know that the device is off for  $V_{GS} < V_{Tn}$ , it is clear that  $V_{GS2}$  is a non-physical solution that must be discarded. For the obtained  $V_{GS1}$ , we must now verify that the device operates in saturation, as initially assumed. It is straightforward to see that this is indeed the case since  $V_{GS1} - V_{Tn} = 1$  V  $< V_{DS} = 2.5$  V. Therefore, the final answer to this problem is  $V_{IN} = 1.5$  V.

If we had initially guessed that the device operates in the triode region, we would write

$$I_D = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Tn} - \frac{V_{DS}}{2}) V_{DS}$$

$$250A = 50 \frac{A}{V^2} \cdot 10 \cdot (V_{GS} - 0.5V - \frac{2.5V}{2}) \cdot 2.5V$$

- The two solution to this equation is  $V_{GS} = 1.95$  V. Since  $V_{GS} - V_{Tn} = 1.45$  V  $< V_{DS} = 2.5$ , we see that the obtained result contradicts the assumed operation in triode. Therefore, the next logical step would be to evaluate the saturation equation, as already done above.

### 4.2.2. Load Line Analysis

A generally useful tool for graphical analysis in electronic circuits is the so-called **load line analysis**. The basis for such an analysis in the context of our circuit is the fact that the current flowing through the transistor ( $I_D$ ) is equal to the current flowing through the resistor (which is viewed in this context as the load of the circuit). Therefore, if we draw the I-V characteristics of the MOSFET and  $R_D$  in one diagram, valid output voltages lie at the intersection of the two curves (equal current). This is further illustrated in Figure 4.8. The load line equation in this plot follows from solving Equation 4.12 for  $I_D$  and is given by

$$I_D = \frac{V_{DD} - V_{OUT}}{R_D} \quad (4.16)$$

The points A, B, C, and D marked in Figure 4.8 correspond to the points shown with the same annotation in Figure 4.7(b). Since the transistor drain characteristics are overlaid in Figure 4.8, it is easy to identify the operating regions that correspond to each point. For example, we can immediately see that point B lies in saturation, since the intersect occurs in a region of constant drain current.

#### Example 2-3: Output Voltage Calculations for a Common-Source Voltage Amplifier

Construct a load line plot to verify the solution of Example 2-2(b) using  $V_{DD} = 5$  V,  $R_D = 10$  k $\Omega$ , and  $W/L = 10$ . Use  $V_{IN} = V_{GS} = 1$  V, 1.5 V, and 2 V for the drain characteristic plot.

#### SOLUTION

#### 4. Introduction

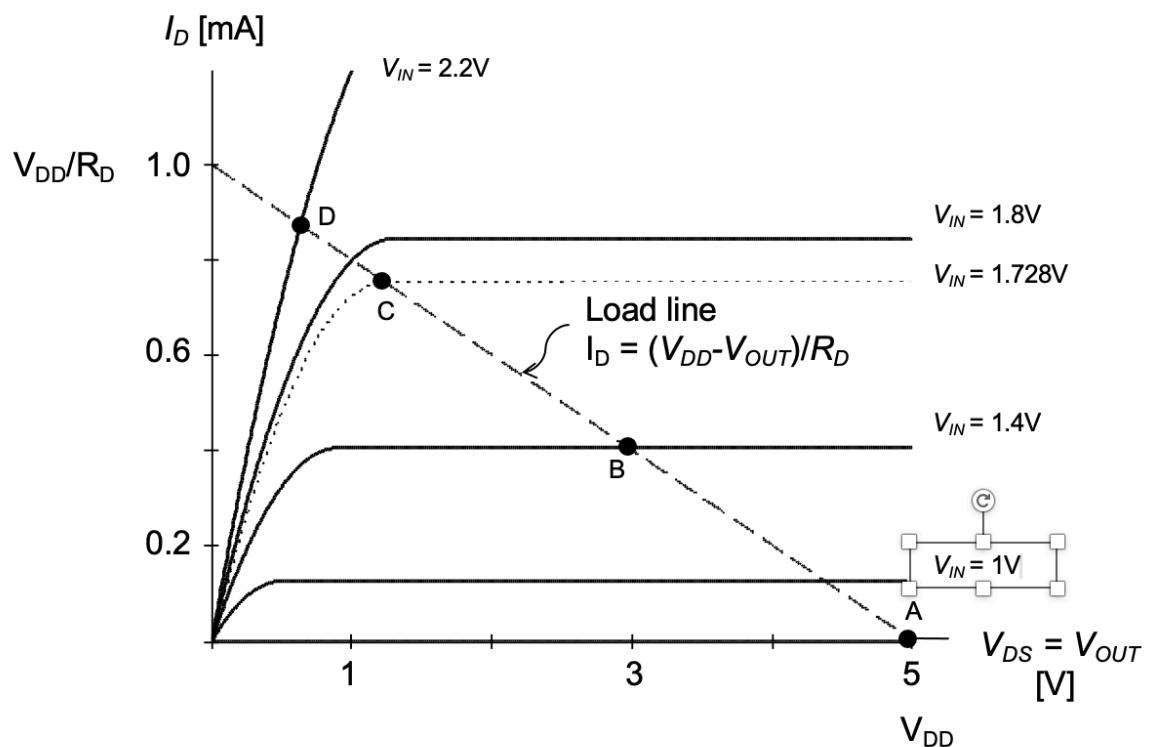


Figure 4.8.: Load line plot for the CS amplifier in Figure 4.7(a). Parameters:  $V_{DD} = 5$  V,  $R_D = 5$  k $\Omega$ , and  $W/L = 20$ .

## 4.2. Building a Common-Source Voltage Amplifier

The solution is shown in Figure 4.9. The load line is most easily drawn by connecting the points  $(0, V_{DD}/R_D = 0.5 \text{ mA})$  and  $(V_{DD} = 5 \text{ V}, 0)$ . The drain characteristics are drawn for the three given  $V_{GS}$  using the expressions of Table 4.1, by sweeping  $V_{DS} = V_{OUT}$  from 0 V to 5 V. The intersect of the load line with the drain characteristic for  $V_{IN} = 1.5 \text{ V}$  confirms the result already obtained in Example 2-2(b).

### 4.2.3. Biasing

After deriving the voltage transfer characteristic of our amplifier, we are now in a position to evaluate this circuit from an application standpoint. As we have discussed in Chapter 1, a common objective for a voltage amplifier is to create large output voltage excursions from small changes in the applied input voltage. With this objective in mind, it becomes clear that only a limited range of the transfer characteristic in Figure 4.7(b) is useful for amplification. For example, a change in the input voltage applied around point D in Figure 4.7(b) yields almost no change in the output voltage. In order to amplify small changes in  $V_{IN}$  into large changes in  $V_{OUT}$ , the transistor should be operated in the saturation region, i.e., in the vicinity of point B. The general concept of operating a circuit and its constituent transistor(s) around a useful operating point is called **biasing**.

Biasing generally necessitates the introduction of auxiliary voltages and/or currents that bring the circuit into the desired state. For the circuit considered in this section, proper biasing can be achieved by decomposing the input voltage into a constant component, and a component that represents the incremental voltage change to be amplified; this is illustrated in Figure 4.10(a). The incremental voltage component  $v_{in}$  could represent, for instance, the signal generated by a microphone or a similar transducer. The voltage  $V_{IN}$  is a constant voltage that defines the point on the overall transfer characteristic around which the incremental  $v_{in}$  is applied. We call  $V_{IN}$  the **input bias voltage** of the circuit.

Per IEEE convention, the total quantity in such a decomposition is denoted using a lowercase symbol and uppercase subscript, i.e.,  $v_{IN} = V_{IN} + v_{in}$  in our example. Similarly, the drain current is decomposed as  $i_d = I_D + i_d$ , where  $I_D$  is the current at the operating point, and  $i_d$  captures the current deviations due to the applied signal.

Figure 4.10(b) elucidates this setup further using the circuit's transfer characteristic. With  $v_{in} = 0$ , the output is equal to  $V_{OUT}$ , which is called the bias point or operating point of the output node. The bias point is sometimes also called the quiescent point (Q), since the corresponding voltage level corresponds to that of a “quiet” input. Note that  $V_{OUT}$  can be calculated by evaluating Equation 4.13, as done previously.

With some nonzero  $v_{in}$  applied, the output will now see an excursion away from the bias point. For example, applying a positive  $v_{in}$  will result in a negative incremental change  $v_{out}$  at the output. How can we compute  $v_{out}$  for a given  $v_{in}$ ? Since Equation 4.13 must hold for the total quantities  $v_{IN} = V_{IN} + v_{in}$  and  $v_{OUT} = V_{OUT} + v_{out}$  we can write

$$V_{OUT} = V_{DD} - R_D \cdot \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (v_{IN} - V_{Tn})^2 \quad (4.17)$$

or

$$V_{OUT} + v_{out} = V_{DD} - R_D \cdot \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{IN} + v_{in} - V_{Tn})^2 \quad (4.18)$$

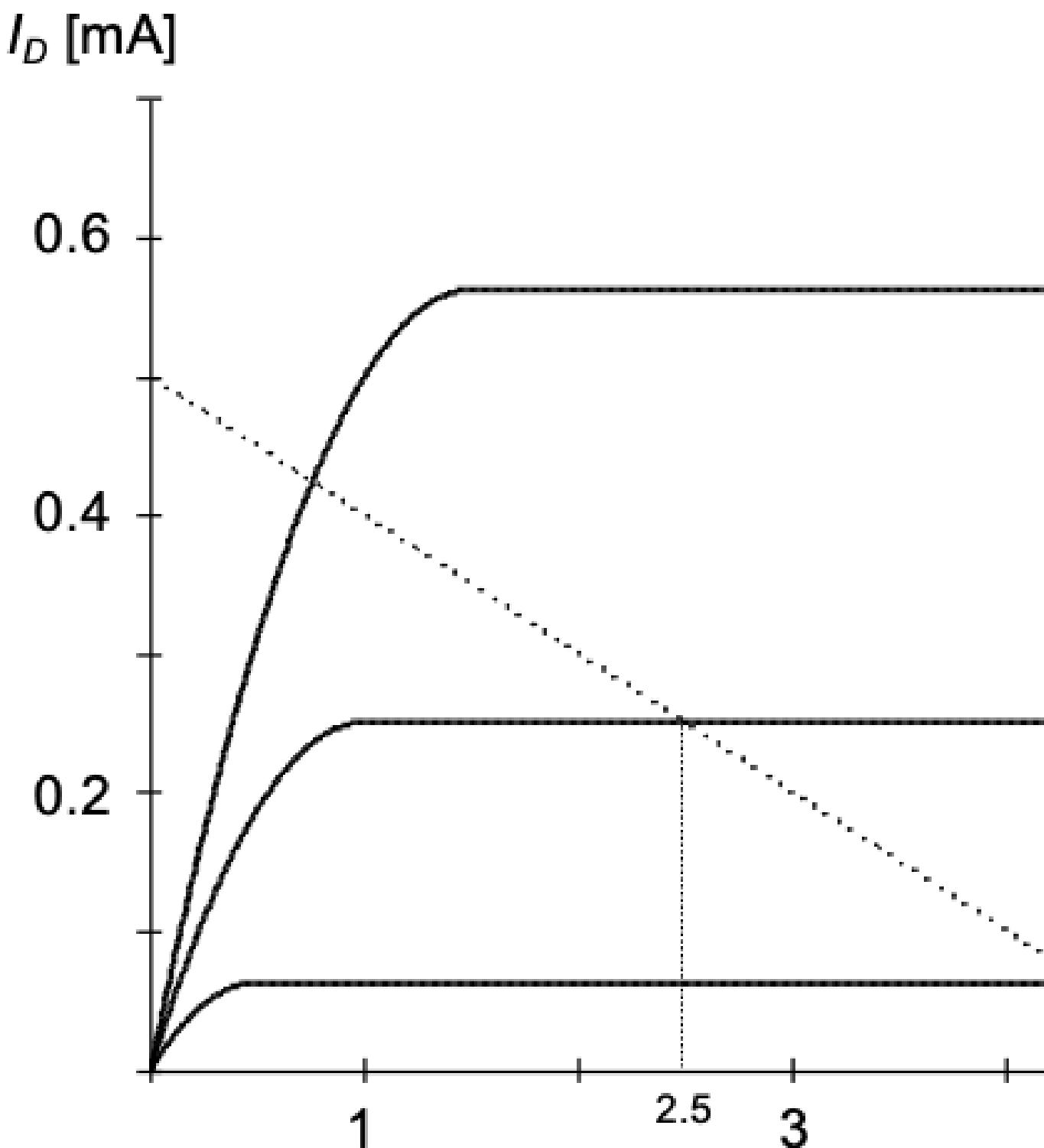


Figure 4.9.

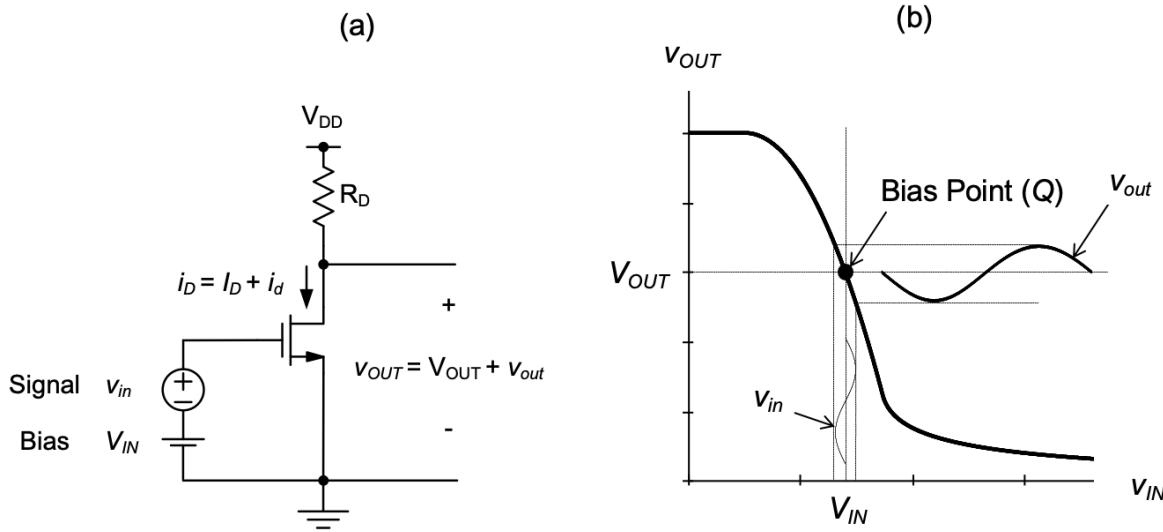


Figure 4.10.: (a) CS amplifier with input bias.(b) Transfer characteristic showing the bias point.

In order to simplify this expression, and since we are only interested in the change of  $v_{out}$  as a function of  $v_{in}$ , it is useful to eliminate the constant term from this expression, given by

$$V_{OUT} = V_{DD} - R_D \cdot \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{IN} - V_{Tn})^2 \quad (4.19)$$

After subtracting Equation 4.19 from Equation 4.18 and rearranging the terms, we obtain

$$v_{out} = -R_D \mu_n C_{ox} \frac{W}{L} (V_{IN} - V_{Tn}) \cdot v_{in} \left[ 1 + \frac{v_{in}}{2(V_{IN} - V_{Tn})} \right] \quad (4.20)$$

Using the drain current expression of Equation 4.7, and by defining

$$V_{OV} = (V_{GS} - V_{Tn})|_Q = V_{IN} - V_{Tn} \quad (4.21)$$

the result can be further simplified and rewritten as

$$v_{out} = -\frac{2I_D}{V_{OV}} \cdot R_D \cdot v_{in} \left( 1 + \frac{v_{in}}{2V_{OV}} \right) \quad (4.22)$$

where  $I_D$  is the transistor's drain current at the bias point, and  $V_{OV}$  is introduced as a symbol for the quiescent point gate overdrive voltage.

From the end result in Equation 4.22, we see that  $v_{out}$  is a nonlinear function of  $v_{in}$ . This is not surprising, since we are employing a transistor that exhibits a nonlinear I-V characteristic. While this derivation was relatively simple, the analysis of nonlinear circuits in general tends to be complex. Picture a circuit that contains several transistors, as for instance a cascade connection of several stages of the amplifier circuit considered here. Even with only a few nonlinear elements, most cases

#### 4. Introduction

involving practical circuits with just moderate complexity tends to yield unwieldy expressions. A widely used solution to this problem is to approximate the circuit behavior using a linear model around its operating point, which we will discuss next.

##### 4.2.4. The Small-Signal Approximation

Equation 4.22 is written in a format that suggests an opportunity for simplification. Provided that  $v_{in} \ll v_{OV}$ , the bracketed term is close to unity and we can write

$$v_{out} = -\frac{2I_D}{V_{OV}} \cdot R_D \cdot v_{in} = A_v \cdot v_{in} \quad (4.23)$$

where  $A_v$  is a constant voltage gain term that relates the incremental input and output voltages.

Interestingly, the term  $A_v$  can also be found using basic calculus. Assuming that the incremental voltages represent infinitesimally small deviations in the total signal, we can rewrite Equation 4.23 as

$$dv_{OUT} = A_v \cdot dv_{IN} \quad (4.24)$$

and therefore

$$A_v = \left. \frac{dv_{OUT}}{dv_{IN}} \right|_Q = \left. \frac{dv_{OUT}}{dv_{IN}} \right|_{v_{IN}=v_{IN}} \quad (4.25)$$

where the derivative is evaluated at the circuit's operating point  $Q$  that is fully defined by choice of the input bias voltage  $V_{IN}$ . By applying Equation 4.25 to Equation 4.17, we find

$$\begin{aligned} A_v &= \left. \frac{d}{dv_{IN}} \left[ V_{DD} - R_D - \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (v_{IN} - V_{Tn})^2 \right] \right|_{v_{IN}=v_{IN}} \\ &= -R_D \mu_n C_{ox} \left. \frac{W}{L} (v_{IN} - V_{Tn}) \right|_{v_{IN}=v_{IN}} \\ &= -R_D \mu_n C_{ox} \frac{W}{L} (V_{IN} - V_{Tn}) = -R_D \mu_n C_{ox} \frac{W}{L} V_{OV} \end{aligned} \quad (4.26)$$

Finally, using Equation 4.7, we find

$$A_v = -\frac{2I_D}{V_{OV}} \cdot R_D \quad (4.27)$$

which is the same result obtained previously. The voltage gain  $A_v$  can be interpreted graphically as shown in Figure 4.11. From Equation 4.25 and basic calculus we know that  $A_v$  is the slope of the tangent to the transfer characteristic at the point  $(V_{IN}, V_{OUT})$ , which is the operating point of the circuit.

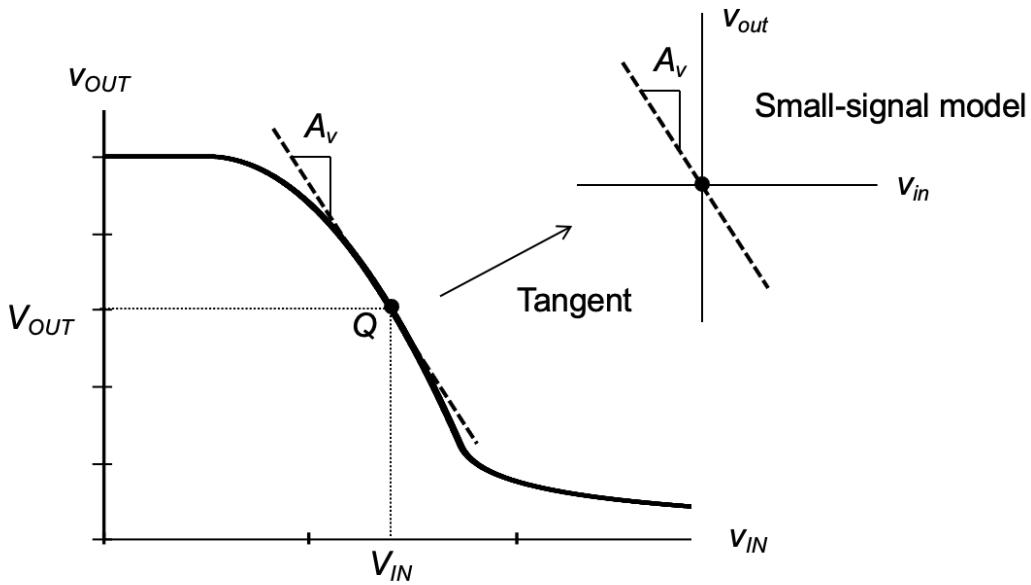


Figure 4.11.: Concept of small-signal voltage gain. In the small signal model, the input and output voltages are linearly related through  $A_v$ , the slope of the tangent at the operating point of the large-signal transfer characteristic.

In analog circuit nomenclature,  $A_v$  is called the **small-signal voltage gain** of the circuit; this emphasizes that this quantity is only suitable for calculations with “small” signals such that nonlinear effects are negligible. In the particular circuit considered here, “small” means  $v_{in} \ll V_{OV}$ , as seen from our analysis. The general concept of approximating circuit behavior by assuming small-signal excursions around an operating point is called **small-signal approximation**. In order to clearly distinguish a circuit transfer characteristic obtained through such an approximation from one that incorporates the nonlinear transistor behavior (e.g., Equation 4.17), the term **large-signal transfer characteristic** is typically used for the latter.

As we shall see in the remainder of this module, working with small-signal approximations greatly simplifies analog circuit analysis and design. The price paid for the approximation, however, is that the resulting equations by themselves cannot be used to reason about the circuit’s behavior for large signals, as for instance signals where  $v_{in}$  is comparable to, or even greater than,  $V_{OV}$ . As illustrated in Figure 4.11, the small-signal approximation essentially creates a new coordinate system that linearly relates the input and output voltages. In this model, the output voltage follows the input linearly, no matter how large the applied voltage is. In reality, considering the circuit’s large signal transfer characteristic, signal clipping and strong waveform distortion can occur for large excursions and poorly chosen bias points. Examples of such cases are illustrated in Figure 4.12.

#### Example 2-4 : Signal clipping

Consider the circuit of Figure 4.10, using the parameters from Example 2-2(b):  $V_{DD} = 5 V$ ,  $R_D = 10 k\Omega$ ,  $W/L = 10$ , and  $V_{IN}$  is adjusted to 1.5 V, so that  $V_{OUT} = 2.5 V$  at the circuit’s operating point. Calculate the most negative excursion that the incremental input voltage  $v_{in}$  can assume before the output is “clipped” to  $V_{DD}$  (as in Figure 4.12(a)).

#### 4. Introduction

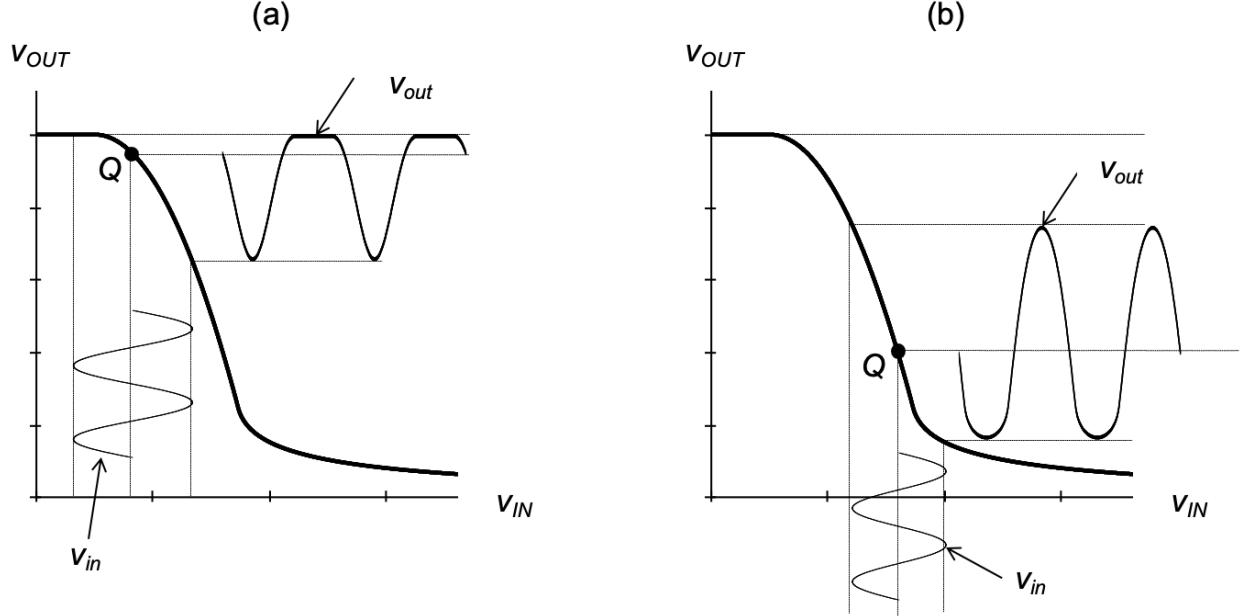


Figure 4.12.: Examples of signal clipping and distortion. (a) Output waveform is clipped due to supply voltage limit. (b) Output waveform drives the MOSFET into the triode region.

#### SOILUTION

The circuit's output voltage is given by

$$v_{OUT} = V_{DD} - R_D \cdot \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{IN} + v_{in} - V_{Tn})^2$$

Clipping  $v_{OUT}$  to the supply voltage implies  $v_{OUT} = V_{DD}$ . This requires

$$0 = V_{IN} + v_{in} - V_{Tn}$$

$$v_{in} = -(V_{IN} - V_{Tn}) = -(V_{OV})$$

$$v_{in} = -(1.5V - 0.5V) = -1V$$

In words, applying a negative signal ( $v_{in}$ ) at the input of magnitude larger than 1 V will cause the output to reach the supply voltage. Making  $v_i$  more negative will create a “plateau” in the output waveform as shown in Figure 4.12(a).

In a majority of analog circuits, it is sufficient to use the large-signal characteristic for bias-point and signal-range calculations. For all other purposes, as for instance voltage gain calculations, it is usually appropriate and justifiable to work with small-signal approximations. Without this clever split in the analysis, most analog circuits of only moderate complexity would not be amenable to

hand analysis, simply because the nonlinear nature of the transistors would create prohibitively complex systems of non-linear equations.

Circuits that are designed to amplify small signals from a transducer are classical examples where the small-signal approximation works. Consider, for instance, the above-discussed amplifier circuit fed with an input signal from a radio antenna, which is often on the order of several hundred microvolts. As long as  $V_{OV}$  is chosen larger than several hundred millivolts, the small signal approximation will hold with reasonable accuracy. Other examples (not covered in this module) include amplifiers that rely on electronic feedback, which tends to minimize the signal excursions around a circuit's bias point (see Reference 2).

As a final remark, it should be noted that even if the input to a circuit is “small,” the output will always show at least some amount of nonlinear distortion. In our basic amplifier, this distortion is caused by the bracketed term in Equation 4.22. In cases where even weak distortion is an issue, the designer often employs computer simulation tools to study the relevant behavior. From a design perspective, deviations from linearity can be minimized if needed. For the discussed common-source amplifier, this is seen from Equation 4.22: decreasing the ratio  $v_{in} / V_{OV}$ , either by reducing  $v_{in}$  or by increasing  $V_{OV}$  will result in improved linearity.

The exact analysis of nonlinear distortion is beyond the scope of this module, and is typically treated only in advanced integrated circuit texts, as for instance Reference 3. We will focus here primarily on studying the relevant behavior of analog circuits using a linear small-signal abstraction, aided by basic bias-point and signal-range calculations.

#### 4.2.5. Transconductance

The method of differentiating a circuit’s large-signal transfer characteristic to obtain a small-signal approximation was straightforward for the simple one-transistor circuit discussed so far. Unfortunately, for a larger circuit it is usually much more difficult and often tedious to derive a complete transfer characteristic in the form of Equation 4.17.

A clever workaround that is predominantly used in analog circuit analysis is based on linearizing the circuit element-by-element around the operating point. This method is applied in three steps: (1) Compute all node voltages and branch currents at the operating point using the devices’ large-signal model. (2) Substitute linear models for all nonlinear components and compute their parameters using the operating point information. (3) Compute the desired transfer function using the linear model obtained in step 2.

The biggest advantage of this method, called **small-signal analysis**, is that it avoids computing the large-signal transfer characteristic of the circuit, and instead defers the transfer function analysis until all elements have been approximated by linear models. The linearized models of nonlinear elements, such as MOSFETs, are typically called **small-signal models**.

We will now illustrate the small-signal analysis approach by applying it to the basic common-source amplifier example covered so far in this chapter. Consider first the MOSFET device in Figure 4.7(a). In general, once the operating point of the transistor is known, the small-signal model is obtained by differentiating the large signal I-V relationships at this point. This is further illustrated in Figure 4.13, assuming that the MOSFET is biased in the saturation region. The proportionality factor that links the incremental drain current ( $i_d$ ) and the gate-source voltage ( $v_{gs}$ ) is given by

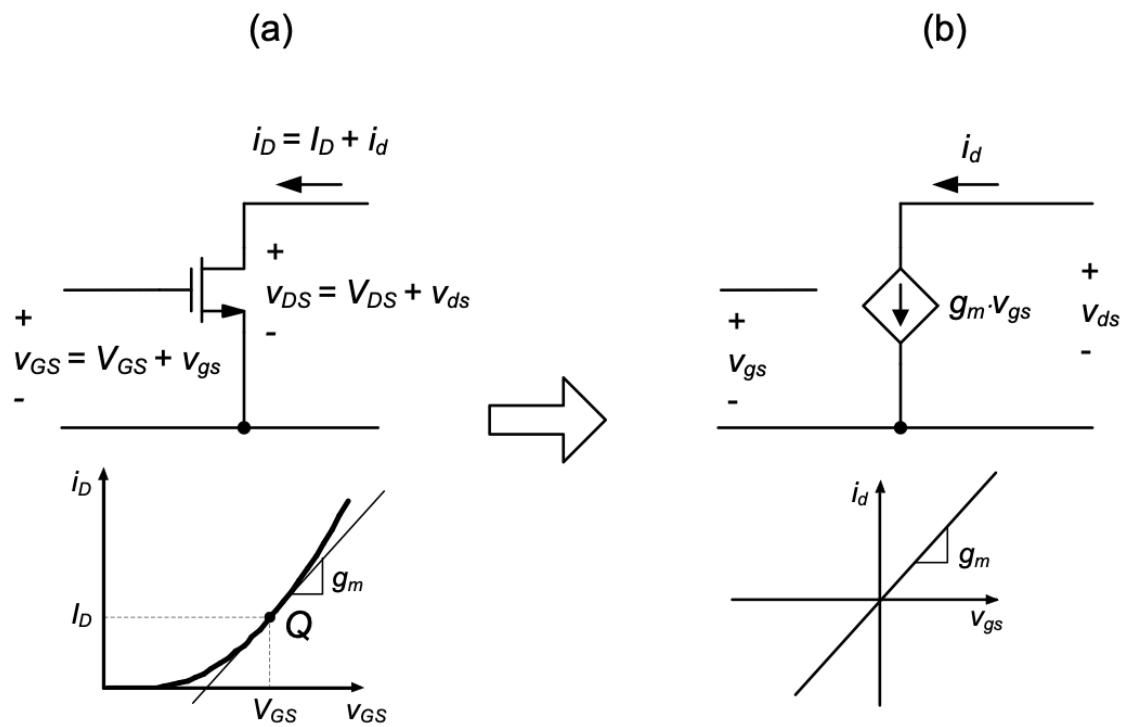


Figure 4.13.: (a) Large-signal transfer characteristic of an n-channel MOSFET in the saturation region. (b) Small-signal transconductance ( $g_m$ ) at the operating point.

## 4.2. Building a Common-Source Voltage Amplifier

the slope of the tangent to the large signal transfer characteristic at the bias point. This quantity is called **transconductance**, or  $g_m$ . Mathematically, we can write

$$g_m = \frac{i_d}{v_{gs}} = \left. \frac{di_D}{dv_{GS}} \right|_{v_{GS}=V_{GS}} \quad (4.28)$$

In order to find the transconductance for the saturation region of the device, we evaluate Equation 4.28 using Equation 4.7. This yields

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Tn}) = \mu_n C_{ox} \frac{W}{L} V_{OV} \quad (4.29)$$

Alternative forms of this expression are obtained by eliminating  $V_{OV}$  or  $\mu_n C_{ox} W/L$  using Equation 4.7, which gives

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \quad (4.30)$$

or

$$g_m = \frac{2I_D}{V_{OV}} \quad (4.31)$$

All of the above equations can be used to calculate  $g_m$ ; the choice of which equation is used depends on the given parameters. The physical unit for transconductance is  $A/V = \Omega^{-1}$ , or **Siemens (S)**.

Once the transconductance is determined, we can insert the model of Figure 4.13(b) into the original circuit (Figure 4.7(a)) for further analysis. The resulting small-signal circuit equivalent is shown in Figure 4.14. No modeling modification is needed for the resistor  $R_D$ , as it is already assumed in Figure 4.7(a) that it follows a linear  $I/V$  law ( $V = I \cdot R$ ). However, since the supply voltage is constant in the large-signal model, it must be replaced with 0 V or ground ( $GND$ ) in the small-signal model. This is because the differentiation of a constant quantity yields zero.

Using the model of Figure 4.14, we now apply Kirchhoff's laws at the output and find

$$v_{out} = -g_m \cdot v_{in} \cdot R_D \quad (4.32)$$

Finally, by substituting Equation 4.31 we obtain

$$v_{out} = -\frac{2I_D}{V_{OV}} \cdot R_D \cdot v_{in} = A_v \cdot v_{in} \quad (4.33)$$

As expected, this result is equivalent to what was obtained by applying the small-signal approximation to Equation 4.22, and also by differentiating Equation 4.17 at the operating point. However, as indicated previously, the big advantage of working with a small-signal model for individual transistors is that this simplifies the analysis of larger circuits.

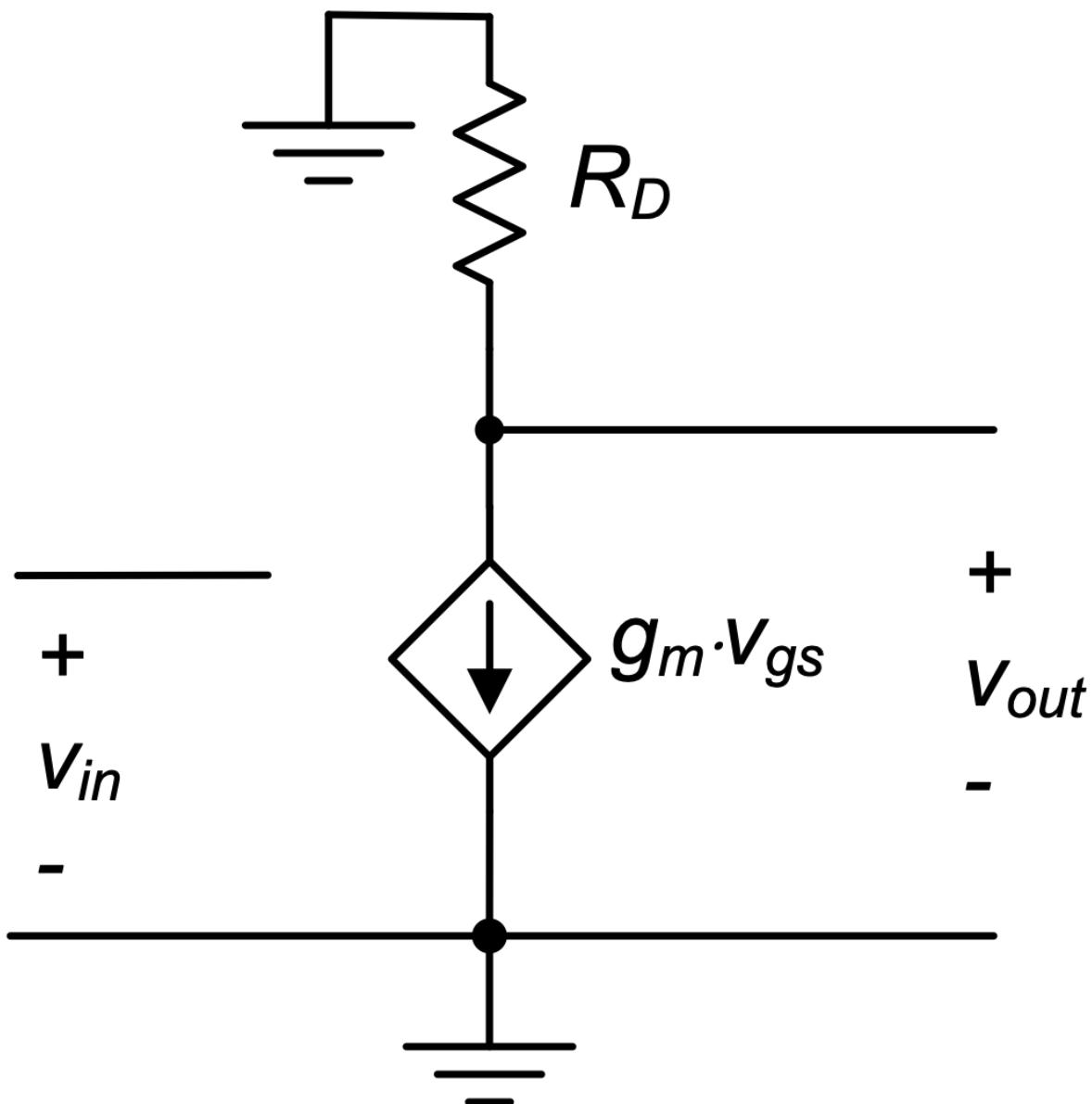


Figure 4.14.: Small-signal model of the circuit in Figure 4.7(a).

#### 4.2.6. P-Channel Common-Source Voltage Amplifier

As shown in Figure 4.15(a), we can also build a CS amplifier using a p-channel device. Similar to the n-channel case, we can derive a large-signal transfer characteristic using Equation 4.11 and by applying *KVL* at the output node. The resulting plot is shown in Figure 4.15(b). Compared to the n-channel case (Figure 4.7(b)), one can show that the characteristic is flipped sideways (since  $V_{SG} = V_{DD} - V_{IN}$ ) and upside down (because  $I_D$  is negative for a p-channel transistor). Therefore, for small  $V_{IN}$  near 0 V, the device operates in the triode region and the output voltage is close to  $V_{DD}$ . For  $V_{IN} = V_{DD}$ , the device is off and the output is at 0 V, since  $V_{SG} = 0$  and no current flows in the device.

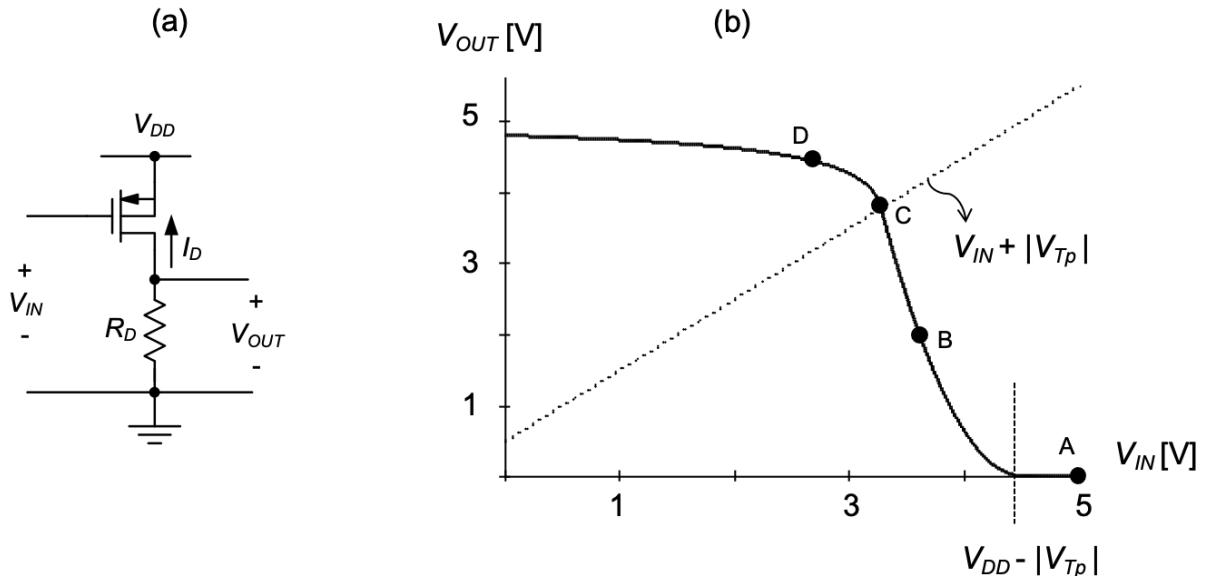


Figure 4.15.: (a) P-channel common-source amplifier schematic. (b) Voltage transfer characteristic for  $V_{DD} = 5$  V,  $R_D = 5$  k $\Omega$ , and  $W/L = 40$ .

In terms of its small-signal model, it follows that the p-channel CS amplifier is identical to the n-channel version. This can be seen intuitively by comparing Figure 4.7(b) and Figure 4.15(b): in the region around point *B*, both transfer characteristics exhibit a negative slope and therefore will behave alike for small perturbations. We will show this formally in the following discussion.

We begin by inserting a small-signal model for the transistor as shown in Figure 4.16(a). Based on the positive variable convention of Equation 4.11, we define the transconductance for the p-channel transistor as

$$g_m = \frac{d}{dv_{SG}}((-i_D)) \Big|_Q = \mu_p C_{ox} \frac{W}{L} (V_{SG} + V_{Tp}) \quad (4.34)$$

#### 4. Introduction

$$= \frac{2(-I_D)}{V_{SG} + V_{Tp}} = \frac{2(-I_D)}{V_{OV}}$$

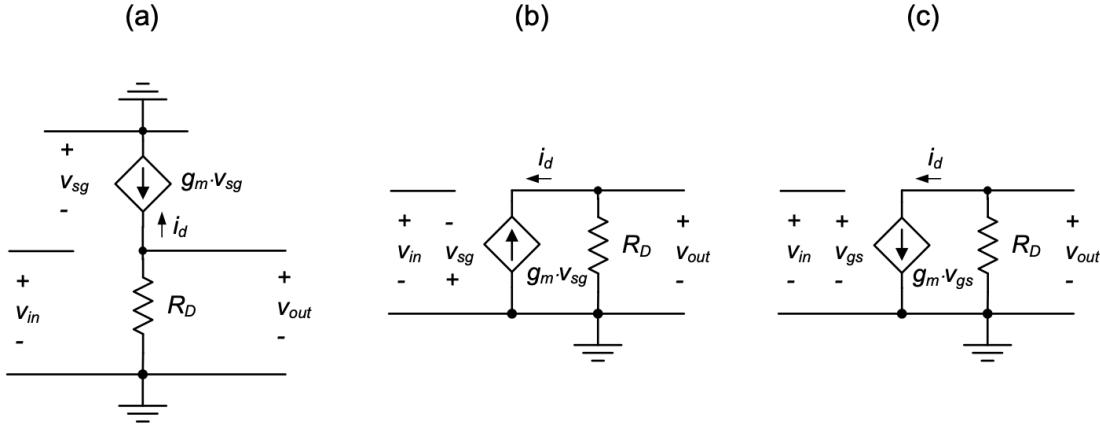


Figure 4.16.: Small-signal model of the p-channel common-source amplifier: (a) using the p-channel model directly, (b) a flipped version of (a), and (c) with sign changes applied to show equivalence with the n-channel model.

Note that through this expression, we have defined  $V_{OV}$  for the p-channel case as  $V_{SG} + V_{Tp}$ , which is a positive quantity for a p-channel device in the “ON” state.

Although we could solve for the small-signal voltage gain directly with the circuit shown in Figure 4.16(a) it is easier to flip the transistor 180° (Figure 2-15(b)) so that the circuit appears similar to the n-channel version. Since  $v_{sg} = -v_{gs}$  we can change signs at the input and the dependent current source and find that the p-channel common-source amplifier small-signal model is identical to the n-channel version as shown in Figure 4.16(c).

This result applies more generally to all the transistor configurations and model extensions that we will study in this module. Once the operating point parameters of a p-channel device have been determined (e.g., a calculation of  $g_m$  using Equation 4.34), it is perfectly valid to replace it with an n-channel equivalent. This is a very powerful and convenient result, since it allows us to focus on n-channel only configurations in small-signal analyses, without having to worry about the specific sign conventions of p-channels.

#### 4.2.7. Modeling Bounds for the Gate Overdrive Voltage

According to Equation 4.31,  $g_m/I_D = 2/V_{OV}$  tends to infinity as the gate overdrive voltage  $V_{OV}$  approaches zero. This implies that for a transistor that is “barely on,” we can extract very large transconductance values for only small bias currents. Unfortunately, this behavior is incorrect, and stems from limitations of the device model discussed in Section 2-1. As  $V_{OV}$  approaches zero, a more complex analysis is needed to predict the drain current and its derivative with respect to gate voltage see Reference 4.

Figure 4.17 plots the  $g_m/I_D$  characteristic of a MOSFET, and the expected behavior based on Equation 4.31. As we can see, for  $V_{OV} < 150mV$ , a large discrepancy exists between a physical

## 4.2. Building a Common-Source Voltage Amplifier

device and the prediction based on the simple square-law model used in this treatment. In order to avoid unrealistic design outcomes due to this modeling limitation, we define a bound for the minimum allowed gate overdrive voltage for all circuits covered in this module

$$V_{OV} \geq V_{OVmin} = 150mV \quad (4.35)$$

Designing with a smaller  $V_{OV}$  would require a more elaborate model for hand calculations, which is beyond the scope of this module. The interested reader is referred to advanced material on this topic, available for example in References 4 and 5.

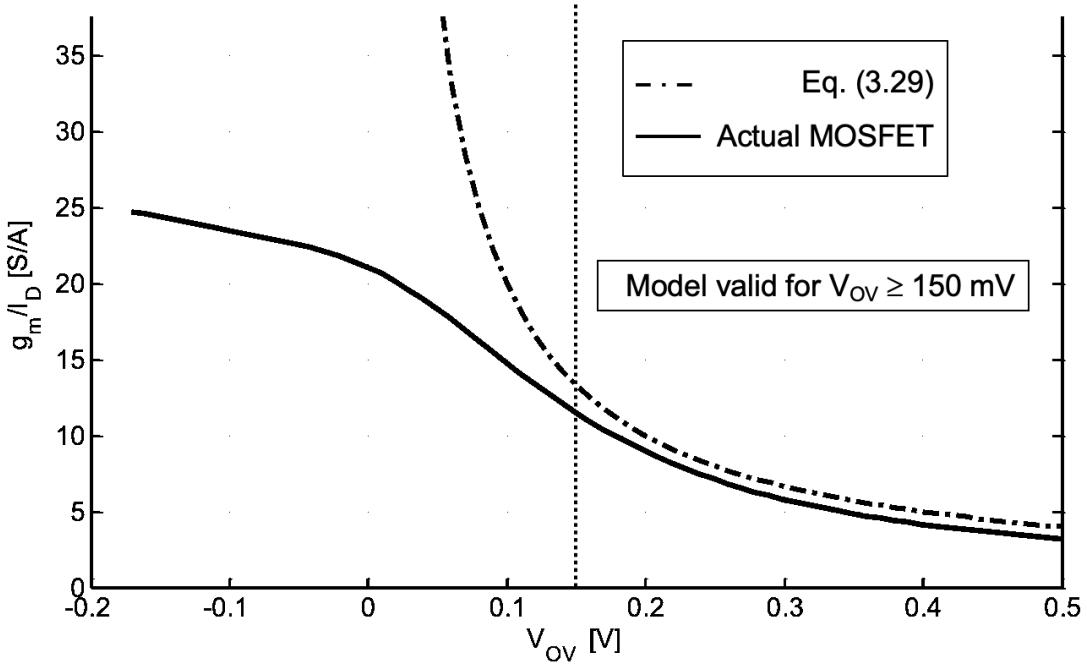


Figure 4.17.: Transconductance to current ratio predicted by Equation 4.31 and the behavior of an actual MOSFET.

### 4.2.8. Voltage Gain and Drain Biasing Considerations

In the basic common-source amplifier discussed so far, the drain resistor  $R_D$  serves a dual purpose: (1) it translates the device's incremental drain current ( $i_d$ ) into a voltage ( $V_{out}$ ), and (2) it supplies the quiescent point drain current ( $I_D$ ) for the MOSFET. As we shall show next, this creates an undesired link between the bias point constraints of the circuit and the achievable small-signal voltage gain of the amplifier. To see this, we rewrite Equation 4.36 as shown below

$$A_v = -\frac{2I_D}{V_{OV}} \cdot R_D = -2\frac{V_R}{V_{OV}} \quad (4.36)$$

where  $V_R = V_{DD} - V_{OUT}$  is the voltage drop across  $R_D$  at the operating point. This result leads to several interesting conclusions. First, note that the voltage gain of the amplifier is fully determined

#### 4. Introduction

once  $V_{OV}$  and voltage drop across  $R_D$  are known. For example, if the circuit is biased such that  $V_{OV} = 0.2$  V and  $V_R = 2$  V, we have  $A_v = -20$ ; regardless of the particular W, L or  $\mu_n C_{ox}$  of the employed MOSFET. Second, since the possible values for  $V_{OV}$  are lower-bounded (Equation 4.35) and  $V_R$  is upper-bounded (finite  $V_{DD}$ ), there exists a maximum possible  $A_v$  that can be obtained

$$|A_{vmax}| = 2 \frac{V_{Rmax}}{V_{OVmin}} = 2 \frac{V_{DD} - V_{OVmin}}{V_{OVmin}} \cong 2 \frac{V_{DD}}{V_{OVmin}} \quad (4.37)$$

In this result, it was assumed the transistor is biased at the edge of the triode region, a somewhat impractical, but appropriate limit case to consider. Evaluating the above expression for  $V_{DD} = 5$  V and  $V_{OVmin} = 150$  mV yields  $|A_{vmax}| \approx 67$ . Can we overcome this limit and change our amplifier such that it can achieve voltage gains beyond this value?

In order to investigate this, consider the load line illustrations shown in Figure 4.18. As explained in Section 2-2-2, the load line for our circuit is defined by the points  $(0, V_{DD}/R_D)$  and  $(V_{DD}, 0)$ . From the location of these points, we see that the x-axis intercept of the load line is fixed, while the y-intercept moves lower with larger values of  $R_D$ . This reduces the slope of the load line, resulting in a larger small-signal voltage gain of the circuit. Furthermore, note that for a fixed quiescent point drain current  $I_D$ , larger  $R_D$  shifts the output bias point  $V_{OUT}$  to smaller values, i.e., closer to the edge of the MOSFET's triode region. This observation captures the result of Equation 4.37 in a graphical way: we cannot increase the small-signal voltage gain beyond a certain limit due the link between  $V_{OUT}$  and the chosen  $R_D$ .

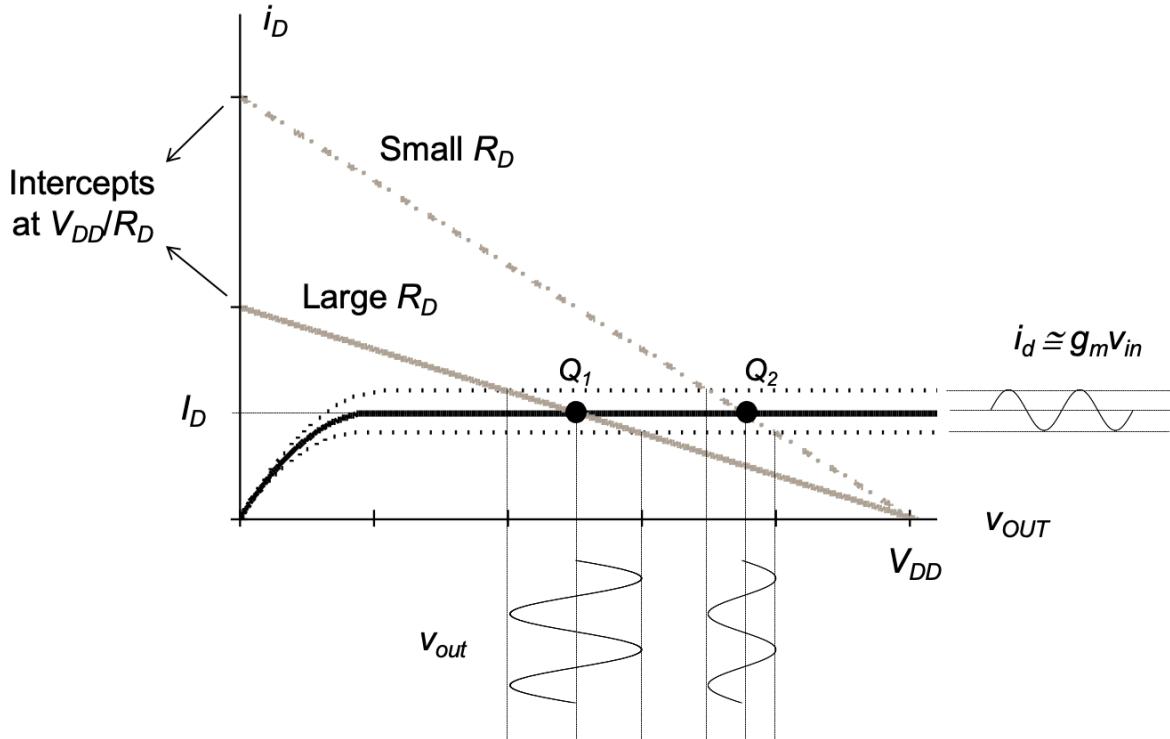


Figure 4.18.: Amplifier load lines for large and small values of  $R_D$ .

A more ideal situation is depicted in Figure 4.19. If we could somehow create a load line that “rotates” about the desired operating point (as a function of  $R_D$ ), the voltage gain could be set

independently of  $V_{OUT}$ . A modified drain network that lets us achieve this behavior is shown in Figure 4.20(a). In this circuit,  $R_D$  is now connected to a voltage  $V_B$  (instead of the supply voltage  $V_{DD}$ ) and an ideal current source  $I_B$  is used to provide a fixed current. In a realistic implementation circuit,  $I_B$  can be built, for example, using a p-channel MOSFET that operates in saturation. For the time being, we will neglect such implementation details, and postpone the discussion of current sources to Chapter 5.

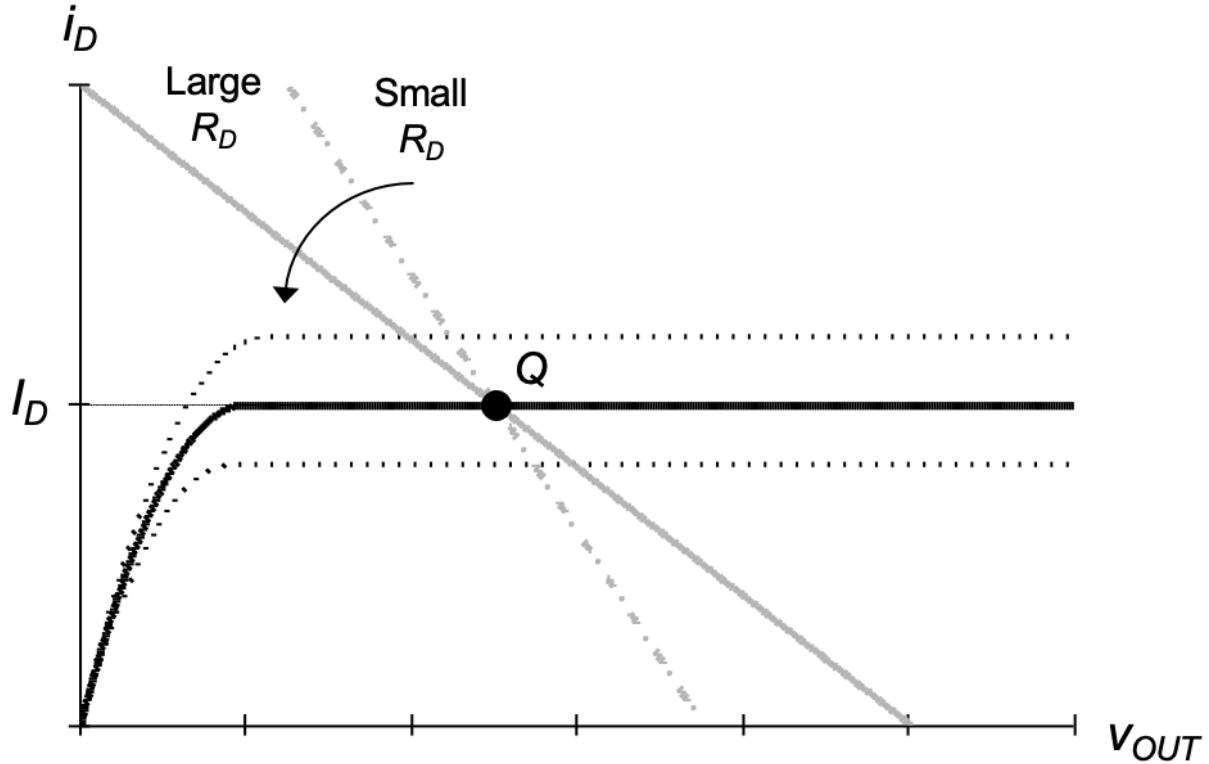


Figure 4.19.: Desired load line behavior.

With this new configuration, the relationship between  $i_D$  and  $v_{OUT}$  becomes

$$i_D = I_B = \frac{V_B - v_{OUT}}{R_D} \quad (4.38)$$

or

$$v_{OUT} = V_B + (I_B - i_D)R_D \quad (4.39)$$

As we can see from these equations (also graphically shown in Figure 4.20(b)), at the point  $v_{OUT} = V_B$ , we have  $i_D = I_B$ , regardless of the value of  $R_D$ . Therefore, utilizing this point as the operating point of our amplifier precisely achieves the goal we have in mind. In particular, we wish to set  $I_B = I_D$ , the desired quiescent point drain current of the MOSFET, and  $V_B = V_{OUT}$ , the desired output operating point. With this choice, the role of the current source is to provide the MOSFET's bias current, while the resistor  $R_D$  is responsible only for converting the incremental drain current into an incremental output voltage; no DC bias current flows in this element.

#### 4. Introduction

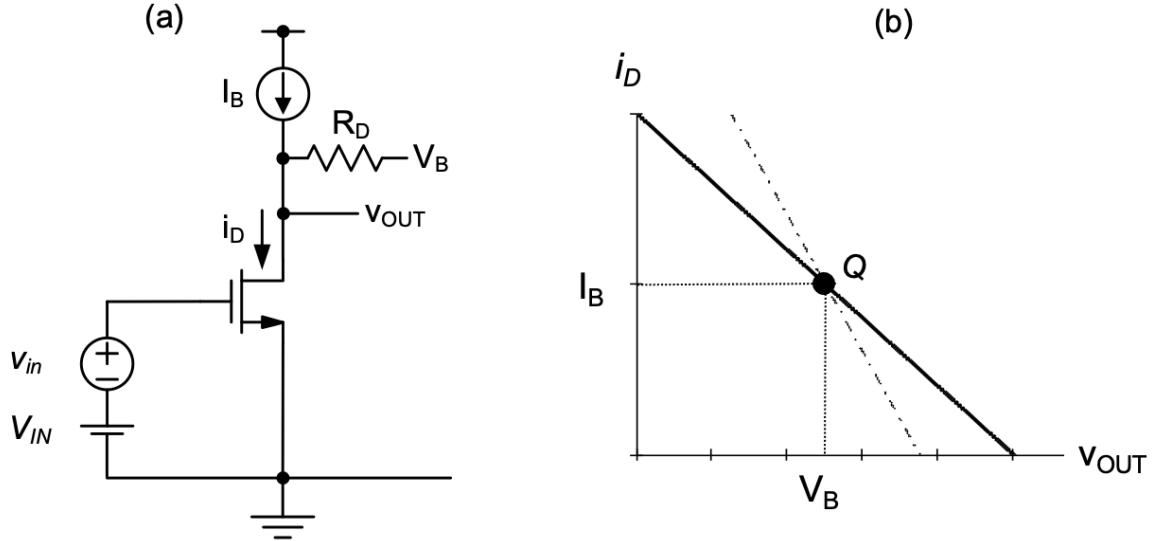


Figure 4.20.: (a) CS amplifier with modified drain biasing scheme. (b) Load line characteristic.

Since the voltage source  $V_B$  and the current source  $I_B$  aid in maintaining the circuit's bias point, we generally classify these elements as biasing sources. However, it is important to distinguish their function from the input bias voltage  $V_{IN}$ .  $V_{IN}$  directly sets the quiescent point gate-source voltage of the transistor and therefore fully defines the operating point on the MOSFET's I-V characteristic and the corresponding drain current. In the above-described scenario,  $I_B$  is adjusted to supply this same drain current, but does not define it. We therefore categorize  $I_B$  an **auxiliary bias** current that helps sustain, but does not set the quiescent point of the transistor. Since  $V_B$  defines the quiescent point output voltage of the circuit, we refer to this element as the **output bias voltage**.

Lastly, it is important to note that for the modified circuit in Figure 4.20(a), the previously derived small-signal model shown in Figure 4.14 still applies. This can be understood by differentiating Equation 4.39 at the operating point to find the small-signal equivalent of the network placed at the drain of the amplifier

$$\left. \frac{dv_{out}}{di_D} \right|_Q = \frac{d}{di_D} (V_B + (I_B - i_D)R_D) = -R_D \quad (4.40)$$

As this result indicates, and as we have seen previously, any constant sources, such as  $V_B$ ,  $I_B$ , etc., drop out of the small signal model, which captures only components that affect the incremental changes in currents and voltages around the circuit's operating point.

For the circuit in Figure 4.20(a), one might now be tempted to think that we can obtain an arbitrarily large voltage gain, as long as  $R_D$  is made very large. Unfortunately this is not the case for several reasons, the first of which stems from physical effects that we have not yet included in the MOSFET model. This aspect is further discussed in Section 2-3. In addition, there are practical limitations to the attainable voltage gain, discussed next.

#### 4.2.9. Sensitivity of the Bias Point to Component Mismatch\*

Consider a CS amplifier biased at the gate as done previously with a bias voltage  $V_{IN}$ , directly setting up the quiescent point drain current  $I_D$  (depending on  $W/L$  and other relevant device parameters). Our goal in using the drain bias network of Figure 4.20(a) is then to set  $I_B = I_D$  and chose  $V_B$  such the output is biased at a reasonable, desired  $V_{OUT}$ . Unfortunately, in practice, we can never achieve  $I_B = I_D$  exactly; there will always be a non-zero  $\Delta I = I_B - I_D$ . This case is shown in Figure 4.21. As illustrated, the finite  $\Delta I$  leads to a shift  $\Delta V$  away from the desired output operating point  $V_B$ . This shift is proportional to  $R_D$ , since the current difference  $\Delta I$  flows into  $R_D$ , creating the undesired  $\Delta V$ .

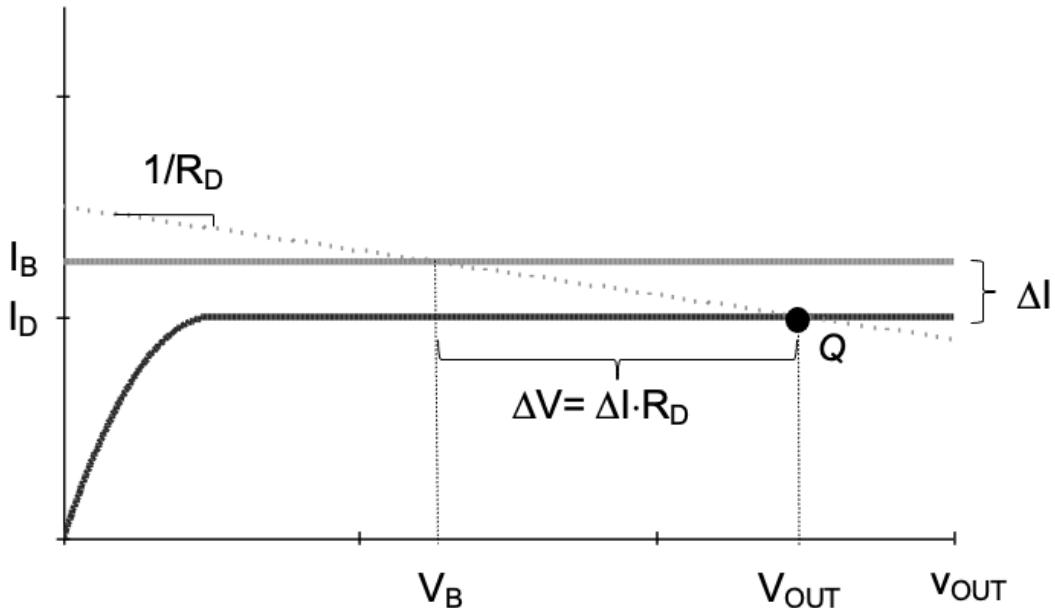


Figure 4.21.: Bias point shift due to mismatch in  $I_B$  and  $I_D$ .

#### Example 2-5: Output Bias Voltage Shift due to Current Mismatch

Consider the CS amplifier of Figure 4.20(a), biased at the gate such that  $V_{OV} = 500$  mV. Assume  $I_D = 200 \mu A$ , and that  $R_D$  is chosen such that the amplifier achieves  $A_v = -400$ . Considering Figure 4.21, how much mismatch between  $I_B$  and  $I_D$  (in  $\mu A$ ) can be tolerated such that  $V_{OUT}$  deviates from the intended bias point ( $V_B$ ) by no more than  $\Delta V = 500$  mV? Repeat this calculation for  $A_v = -40$  and  $-4$ .

#### SOLUTION

We begin by computing the transconductance of the MOSFET

$$g_m = \frac{2I_D}{V_{OV}} = \frac{2 \cdot 200\mu A}{0.5V} = 800S$$

#### 4. Introduction

In order to achieve  $A_v = -400$ , we require  $R_D = 400/800 \mu S = 500k\Omega$ . Therefore,

$$\frac{\Delta I}{I_D} = \frac{\Delta V}{I_D R_D} < \frac{500mV}{200\mu A \cdot 500k\Omega} = 0.5\%$$

For  $A_v = -40$  and  $A_v = -4$ , the result modifies to 5%, and 50%, respectively.

As expected, this result confirms that for larger  $|A_v|$ , the auxiliary bias current  $I_B$  must match the MOSFETs drain current more accurately. How precisely can we match these two currents? Unfortunately, answering this question in detail is beyond the scope of this module, and is the subject of advanced research papers such as Reference 6. Nonetheless, it can be said in general that matching currents, voltages, or any other electrical quantities in today's integrated circuits to better than 1% requires special care and understanding. In some cases, even 10% matching can be hard to guarantee. With this guideline in mind, it becomes clear that the circuit of Figure 4.20(a) may become impractical if we aim for too much voltage gain.

The general issue of properly dealing with variability in integrated circuit components is a complex topic that is still being actively researched. At the introductory level of this module, the main point that the reader should retain is that any circuit whose bias point relies on precisely matched components or high absolute accuracy in any electrical parameter may not be robust in the presence of component variability. In general, experienced circuit designers avoid situations that resemble the “balancing of a marble on the tip of a cone,” i.e., circuits that will be overly sensitive to variations in component parameters. We will take up this point once more when discussing practical biasing circuits in Chapter 5.

As a final note concerning the issue of variability, it is worth mentioning that electronic feedback can help alleviate problems as the one analyzed in Example 2-5. Picture for example adding an auxiliary circuit to Figure 4.20(a) that somehow measures  $V_{OUT}$ , and adjusts  $V_{IN}$  (and therefore  $I_D$ ) until the desired output operating voltage is set. In such schemes, relatively large variations in  $I_B$  can be absorbed. Feedback circuits are not covered in this module, but are the subject of advanced texts such as Reference 2.

### 4.3. Channel Length Modulation

The MOSFET model used so far assumes that the drain current in the saturation region is independent of the drain-source voltage. This behavior corresponds to that of an ideal current source, which is generally non-physical. A more realistic output characteristic observed in real MOSFETs is shown in Figure 4.22. For a physical MOSFET,  $I_D$  tends to increase with  $V_{DS}$ ; an effect that can be explained (to first-order) as a voltage dependent modulation of the channel length (see Section 2-3-1).

When inserted into the circuit of Figure 4.20(a), the dependence of drain current on  $v_{DS}$  ( $v_{OUT}$ ), will have an impact on the overall transfer characteristic of the amplifier, which we will thus consider in this section. For simplicity, let us first investigate the case of  $R_D \rightarrow \infty$ , i.e., no explicit drain resistance, and using only an ideal current source in the drain biasing network (see Figure 4.23(a)). In this case, the load line is horizontal at  $I_B = I_D$ , as shown in Figure 4.23(b). As before, the operating point  $Q$  is established at the point where the load line and the device's drain characteristic for the applied quiescent point input voltage ( $V_{IN}$ ) meet.

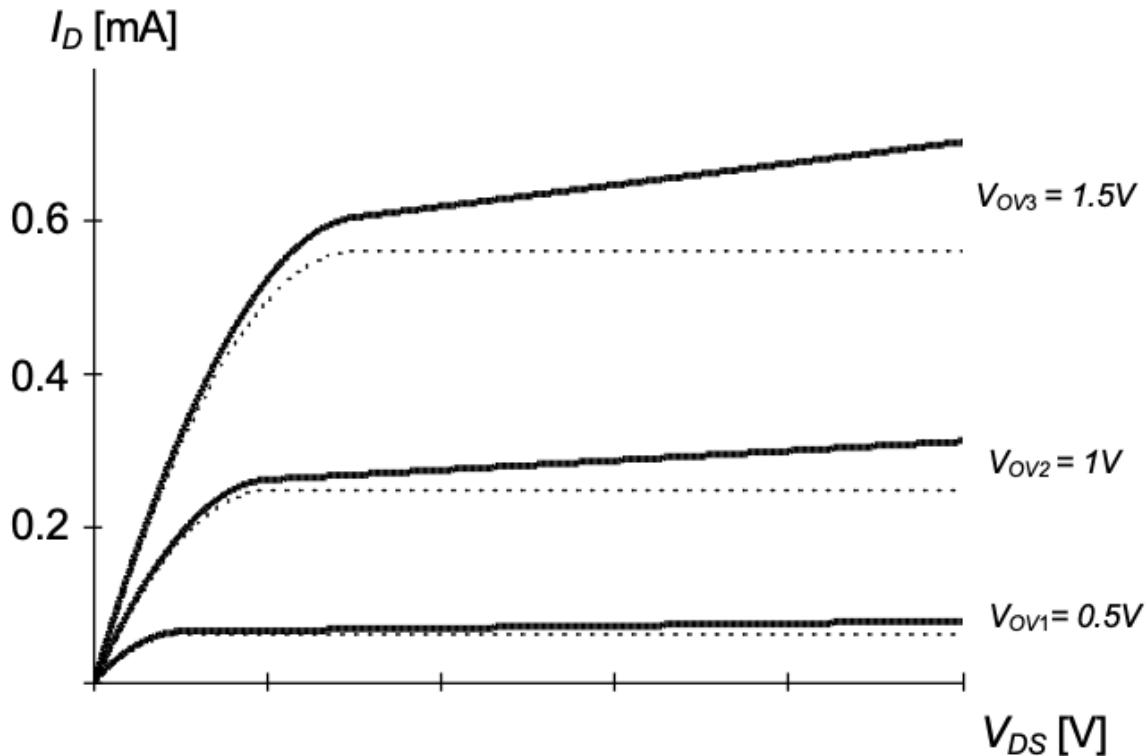


Figure 4.22.: Realistic n-channel I-V plots, incorporating the dependence of saturation drain current on  $V_{DS}$ . (solid lines), along with the first-order model assumed previously (dotted lines). Parameters:  $W = 20 \mu m$ ,  $L = 2 \mu m$ .

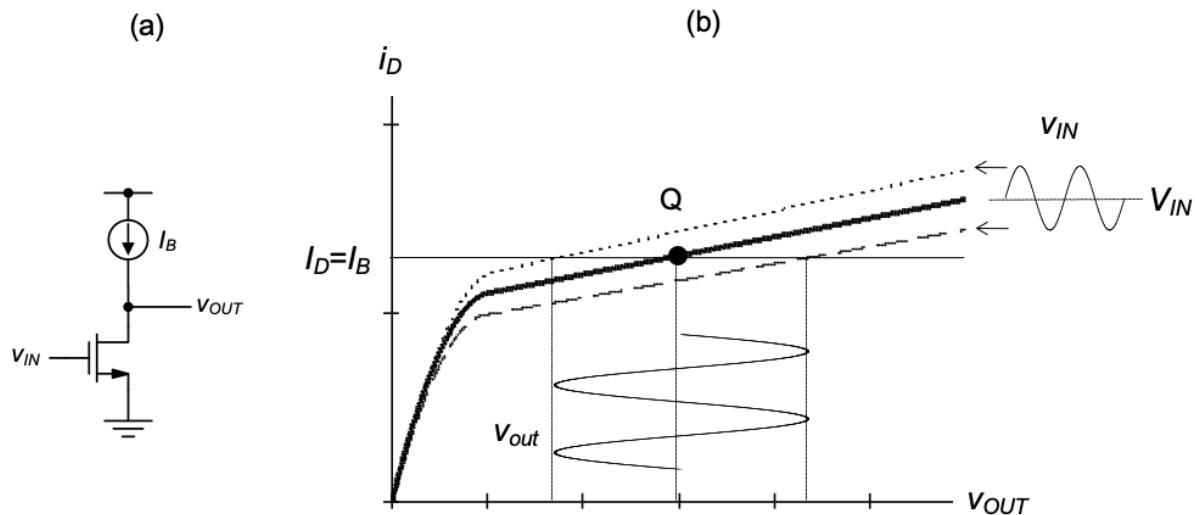


Figure 4.23.: (a) Intrinsic voltage gain stage. (b) Load line plot.

## 4. Introduction

Note that similar to the case considered in the previous section, the output operating point voltage in this circuit will shift by large amounts for relatively small changes in  $I_B$  (or MOSFET parameters). This issue must be addressed when this circuit is used in practice, for example by providing a feedback mechanism that adjusts  $I_B$  such that the desired  $V_{OUT}$  is maintained in the presence of component variations.

Assuming that a well-defined operating point has been established by some means, incremental changes in  $v_{IN}$  applied around the bias point  $Q$  will force the intersection of the horizontal load line with the MOSFET's drain characteristics to move sideways (since the drain current cannot change), creating a finite output voltage excursion  $v_{OUT}$ . The magnitude of this voltage excursion, and thus the voltage gain of the circuit, depends on the slope of the MOSFET's drain characteristic in saturation. The voltage gain achieved in this configuration is commonly called the **intrinsic voltage gain** of the MOSFET, as it represents the voltage gain of the transistor by itself, without any added resistances in the drain bias network. By the same reasoning, the circuit of Figure 4.23(a) is often called the **intrinsic voltage gain stage**. The voltage gain and other parameters of more complex amplifier circuits are often directly related to the intrinsic voltage gain of their constituent transistors, giving this parameter a fundamental significance in circuit design.

### 4.3.1. The -Model

Unfortunately, the intrinsic voltage gain of a MOSFET cannot be predicted using the MOSFET model established so far. We will therefore extend the first-order MOSFET model to incorporate the dependence of the saturation current on the drain-source voltage. As a first step, we will describe the effect in terms of large-signal equations. Next, we will apply a small-signal approximation that makes it possible to capture the  $I_{Dsat}-V_{DS}$  dependence through a single resistor added to the MOSFET's small-signal model.

We begin by revisiting an approximation that was made in Section 2-1. In order to arrive at the constant drain current expression in saturation (Equation 4.7), it was assumed that  $\Delta L$ , the distance from the pinch-off point to the drain, is negligible relative to the channel length  $L$ . In reality, this approximation is fine only as long we do not care about the  $I_D-V_{DS}$  dependence seen in Figure 4.22. Therefore, in order to get a quantitative handle on the MOSFET's intrinsic voltage gain, we must further investigate the impact of the physics at the drain side.

The simplest possible way to proceed is to factor  $\Delta L$  into the existing derivation of Section 2-1. Instead of integrating Equation 4.5 over the length  $L$ , we use  $L-\Delta L$  as the upper limit of the integral. Recall that  $L-\Delta L$  is the actual location where the mobile charge vanishes, i.e.,  $Q_n(y) = 0$ . With this change we obtain the following expression for the saturation region.

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L - \Delta L} (V_{GS} - V_{Tn})^2 \quad (4.41)$$

Now, provided that  $\Delta L$  is still small (but not negligible) relative to  $L$ , we can apply the following first-order approximation:

$$\frac{1}{L - \Delta L} \approx \frac{1}{L} \left(1 + \frac{\Delta L}{L}\right) \quad (4.42)$$

### 4.3. Channel Length Modulation

Next, note that  $\Delta L$  must be a function of the drain voltage, since the depletion region widens with increasing reverse bias. This effect is commonly called **channel length modulation**. Unfortunately, an exact calculation of  $\Delta L$  as a function of the terminal voltages involves solving the two-dimensional Poisson equation and leads to complex expressions. For simplicity, we assume that the fractional change in channel length is proportional to the drain voltage

$$\frac{\Delta L}{L} = \lambda_n V_{DS} \quad (4.43)$$

where  $\lambda_n$  is the channel length modulation parameter. Device measurements and simulations indicate that  $\lambda_n$  approximately varies with the inverse of the channel length. For the MOSFETs in this module, we will use

$$\lambda_n = \frac{0.1\mu mV^{(-1)}}{L} \quad (4.44)$$

where  $L$  is in  $\mu m$ . Finally, we substitute Equation 4.44 and Equation 4.43 into Equation 4.41 and find a very useful approximation to the drain current in saturation, often called the  **$\lambda$ -model**:

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Tn})^2 (1 + \lambda_n V_{DS}) \quad (4.45)$$

where  $V_{DS} - V_{DSsat} = V_{GS} - V_{Tn}$ . This model has proven useful and sufficiently accurate for basic hand calculations, even though the physics related to the  $I_{DSsat}$ - $V_{DS}$  dependence are in reality much more complex than discussed above. As long as  $\lambda_n$  is determined from measurements or accurate physical analysis, the model properly approximates a typical MOSFET's I-V characteristic to first-order. Higher-order models are typically not used in hand analysis, but find their use in advanced computer simulation models.

We now wish to incorporate the channel length modulation effect into the small-signal model of the MOSFET. An important new feature that must be considered in this task is that the drain current of Equation 4.45 now depends on two voltages, namely  $V_{DS}$  and  $V_{GS}$ . A common and appropriate way of handling this situation for small-signal modeling is to approximate the incremental drain current around the operating point as the total differential (as frequently used in error analysis) due to both variables, i.e.

$$i_d = \left. \frac{\partial i_D}{\partial V_{GS}} \right|_Q \cdot v_{gs} + \left. \frac{\partial i_D}{\partial V_{DS}} \right|_Q \cdot v_{ds} \quad (4.46)$$

The above expression essentially treats  $v_{DS}$  as a constant when evaluating the derivative of  $i_D$  with respect to  $v_{GS}$ . Similarly,  $v_{GS}$  is assumed constant in the differentiation with respect to  $v_{DS}$ . This use of partial differentiation is justified and reasonably accurate as long as at least one of the following two conditions is met:

1. The excursion in the variable that is treated as a constant can be approximated as infinitesimally small and therefore negligible.
2. The excursion in the variable that is approximated as a constant is considerable, but nonetheless does not affect the derivative with respect to the second variable.

#### 4. Introduction

In the context of a common-source amplifier, for instance, the first condition applies to  $v_{GS}$ . Just as in the derivation of the simple small-signal model without  $V_{DS}$  dependence, we can argue that changes in  $v_{GS}$  are suitably modeled as “small” (relative to  $V_{OV}$ ). The same condition cannot be applied to  $v_{DS}$  in general. Often times the output voltage, and therefore  $v_{DS}$ , see large excursions in amplifier circuits. In order for Equation 4.46 to be reasonably accurate, we must require the second condition, i.e., the derivative of  $i_D$  w.r.t.  $v_{GS}$  must not strongly depend on drain-source voltage. By inspection of Equation 4.45, we see that this condition is met as long as  $\lambda_n$  is small, which is typically the case for MOSFETs intended for use in amplifier stages.

To continue with our analysis, we rewrite Equation 4.46 as

$$i_d = g_m v_{gs} + g_o v_{ds} \quad (4.47)$$

where

$$g_m = \left. \frac{\partial i_D}{\partial V_{GS}} \right|_Q = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Tn})(1 + \lambda_n V_{DS}) = \frac{2I_D}{V_{GS} - V_{Tn}} = \frac{2I_D}{V_{OV}} \quad (4.48)$$

and

$$g_o = \left. \frac{\partial i_D}{\partial V_{GS}} \right|_Q = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Tn})^2 \lambda_n = \frac{2I_D}{V_{GS} - V_{Tn}} = \frac{2I_D}{V_{OV}} \quad (4.49)$$

where the approximate end result assumes  $\lambda_n V_{DS} \ll 1$ , a condition that is often satisfied for long channels and moderate  $V_{DS}$ . For instance, assuming  $L = 2 \mu\text{m}$  and  $V_{DS} = 2 \text{ V}$  gives  $\lambda_n V_{DS} = 0.1$  which is much less than one.

In the above expressions,  $g_m$  is the transconductance of the MOSFET (as defined previously) and  $g_o$  is called the output conductance. The inverse of  $g_o$  is called the output resistance,  $r_o = g_o^{-1}$ . Graphically, the output conductance corresponds to the slope of the transistor’s drain characteristic at the operating point, which is the derivative of  $i_D$  with respect to  $v_{DS}$ , while keeping the gate-source voltage constant (see Figure 4.24(a)). In the small-signal model of the MOSFET, the output conductance can be included as shown in Figure 4.24(b). This representation follows directly from Equation 4.47, which represents Kirchhoff’s Current Law equation for the drain node of the transistor.

Just as with the simple  $g_m$ -only small-signal model of Figure 4.13, the main idea for the usage of the extended model with  $g_o$  is to use the small-signal equivalent circuit of Figure 4.24(b) in a larger circuit. We will illustrate this using two examples of interest: the intrinsic voltage gain stage of Figure 4.23(a) and the common-source amplifier of Figure 4.20(a).

#### 4.3.2. Common-Source Voltage Amplifier Analysis Using the $\lambda$ -Model

For the intrinsic voltage gain stage, the small-signal model of Figure 4.24(b) corresponds directly to the small-signal model for the entire circuit with  $v_{in} = v_{gs}$  and  $v_{out} = v_{ds}$ . Therefore, the voltage gain of the intrinsic gain stage is given by

$$A_v = -\frac{g_m}{g_o} = -g_m r_o \cong -\frac{2I_D}{V_{OV}} \cdot \frac{1}{\lambda_n I_D} = -\frac{2}{\lambda_n V_{OV}} \quad (4.50)$$

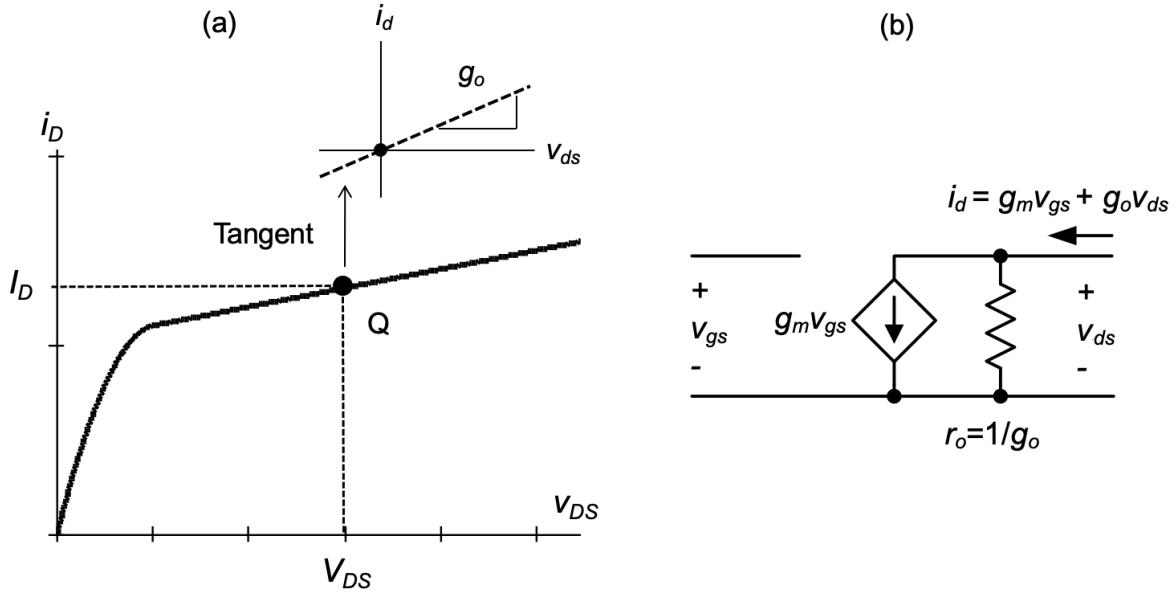


Figure 4.24.: (a) Graphical interpretation of  $g_o$ . (b) MOSFET small-signal model for the saturation region with output conductance ( $g_o$ ).

From this expression, we can see that the voltage gain can be increased by increasing  $L$ , which will decrease  $\lambda$ . Alternatively, the voltage gain can be increased by reducing  $V_{OV}$ , which corresponds to reducing the drain current  $I_D$  for a fixed aspect ratio  $W/L$ . In this context, note that for  $V_{OV} \rightarrow 0$ , Equation 4.50 predicts infinite voltage gain. This non-physical outcome stems from the same issue already discussed in Section 2-2-7: for  $V_{OV} \rightarrow 0$ ,  $g_m$  approaches infinity for a fixed current in our simplistic square-law I-V model. As argued before, the usable range for  $V_{OV}$  must therefore be lower-bounded as specified in Equation 4.35. Assuming  $V_{OV} = V_{OV\min} = 150 \text{ mV}$  and  $L = 1 \mu\text{m}$ , the intrinsic voltage gain of a MOSFET described by the parameters used in this module is approximately  $2/(0.1 \cdot 0.15) = 133$ .

Let us now consider the common-source amplifier of Figure 4.20(a). Including the finite output conductance from the  $\lambda$ -model, the small-signal model is modified as shown in Figure 4.25 and the voltage gain expression becomes

$$A_v = -g_m \left( \frac{1}{r_o} + \frac{1}{R_D} \right)^{-1} = -g_m R_{out} \quad (4.51)$$

For  $R_D \rightarrow \infty$ , the small signal voltage gain approaches the intrinsic voltage gain as given by Equation 4.50. For  $R_D \ll r_o$ , we can approximate  $A_v \approx -g_m R_D$ . More generally, without even knowing the exact values of  $r_o$  and  $R_D$ , we can argue that as long as the desired gain is much less (in magnitude) than the intrinsic voltage gain,  $r_o$  can be neglected in the voltage gain calculation. To see this, we can rewrite Equation 4.51 as

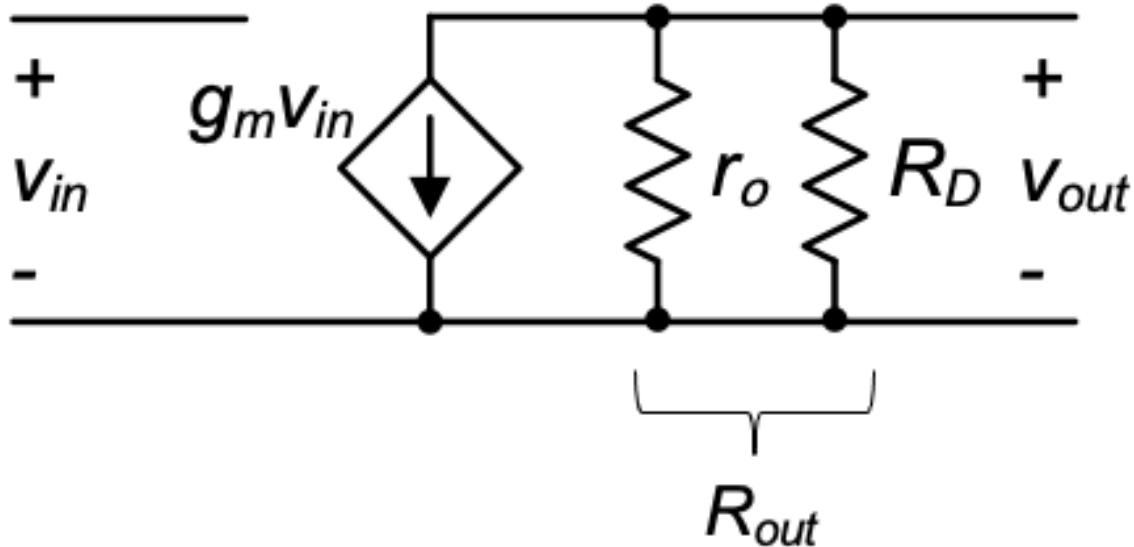


Figure 4.25.: Small-signal model for the circuit of Figure 4.20(a), with finite output conductance.

$$\frac{1}{|A_v|} = \frac{1}{g_m r_o} + \frac{1}{g_m R_D}$$

$$g_m R_D = \frac{|A_v|}{1 - \frac{|A_v|}{g_m r_o}} \cong |A_v| \quad \text{for } |A_v| \ll g_m r_o \quad (4.52)$$

#### Example 2-6: Analysis of a CS Amplifier Using the $\lambda$ -Model

Consider the CS voltage amplifier of Figure 4.20(a) with  $W = 80 \mu m$ ,  $L = 2 \mu m$  and  $R_D = 50 k\Omega$ . The gate is biased such that  $V_{OV} = 500mV$  and  $V_B$  is set to 2 V, which is also the desired output operating point  $V_{OUT}$ . Compute the required bias current  $I_B$  and the small-signal voltage gain of the circuit using the  $\lambda$ -model. Repeat the small-signal voltage gain calculation for  $R_D = 5 k\Omega$ .

#### SOLUTION

The bias current is found using

$$I_B = I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Tn})^2 (1 + \lambda_n V_{DS})$$

$$\frac{1}{2} \cdot 50 \frac{\mu A}{V^2} \cdot \frac{80}{2} (0.5V)^2 (1 + 0.05 \cdot 2)$$

$$= 275 \mu A$$

The corresponding transconductance and output resistance at the operating point are

$$g_m = \frac{2I_D}{V_{OV}} = \frac{2 \cdot 275\mu A}{0.5V} = 1.1mS$$

$$r_o = \frac{1 + \lambda_n V_{DS}}{\lambda_n I_D} = \frac{1 + 0.05 \cdot 2}{0.5V^{-1} \cdot 275\mu A} = 80k\Omega$$

According to Equation 4.51, the small signal voltage gain for  $R_D = 50 k\Omega$  is given by

$$A_v = -1.1mS \left( \frac{1}{80k\Omega} + \frac{1}{50k\Omega} \right)^{-1} = -33.9$$

for  $R_D = 5 k\Omega$  we find

$$A_v = -1.1mS \left( \frac{1}{80k\Omega} + \frac{1}{5k\Omega} \right)^{-1} = -5.18$$

Since the voltage gain for  $R_D = 5 k\Omega$  is much less than the intrinsic voltage gain of the transistor ( $g_m r_o = 88$ ), it is appropriate to neglect  $r_o$  in this calculation. We can simply compute

$$A_v = -1.1mS \cdot 5k\Omega = -5.5$$

This result differs only by about 5.9% from the accurate calculation.

Another opportunity for useful engineering approximations in the application of the  $\lambda$ -model lies in the operating point calculation. We will illustrate this point through the example below.

### Example 2-7: Approximate Operating Point Calculations

Recalculate  $I_D$ ,  $g_m$  and  $r_o$  by approximating  $\lambda V_{DS} \approx 0$  in the large-signal bias point calculations. Also recalculate  $A_v$  for  $R_D = 50 k\Omega$  using this approximation. Compare the results to the values obtained in Example 2-6.

#### SOLUTION

For  $\lambda V_{DS} = 0$ , the bias current is estimated as

$$\begin{aligned} I_B &= I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Tn})^2 \\ &= \frac{1}{2} \cdot 50 \frac{\mu A}{V^2} \cdot \frac{80}{2} (0.5V)^2 \\ &= 250\mu A \end{aligned}$$

The corresponding transconductance and output resistance at the operating point are

$$g_m = \frac{2I_D}{V_{OV}} = \frac{2 \cdot 250\mu A}{0.5V} = 1mS$$

#### 4. Introduction

$$r_o = \frac{1}{\lambda_n I_D} = \frac{1}{0.5V^{-1} \cdot 250\mu A} = 80k\Omega$$

and the voltage gain becomes

$$A_v = -1mS \left( \frac{1}{80k\Omega} + \frac{1}{50k\Omega} \right)^{-1} = -30.8$$

Relative to the accurate calculation from Example 2-6 ( $A_v = -33.9$ ), this result is in error by only about 9.1%.

There are several reasons why it is commonly acceptable to neglect the  $\lambda V_{DS}$  term in bias point hand calculations. First, without this approximation, the calculations can become cumbersome and lead to transcendental equations that are tedious and undesirable to solve in light of only a moderate percent-improvement in the obtained accuracy. If a more accurate result is desired, it can often be obtained more easily from computer simulations, which often follow a hand calculation in practice anyway. Last, one can argue that any circuit in which the operating point parameters strongly depend on  $\lambda$  may be impractical in the first place. The accuracy of the  $\lambda$ -model as far as absolute I-V values are concerned can only be approximate due to its empirical nature. For high accuracy analysis, much more complex models (such as the one described in Reference 7) must be used, carefully calibrated with physical measurements and subsequently evaluated in computer simulations. For the purpose of developing an introductory feel for circuits, however, the  $\lambda$ -model is still the most appropriate, mainly due its simplicity.

Table 2-3 summarizes the technology parameters introduced in this chapter.

Table 4.3.: Standard technology parameters for the  $\lambda$ -model.

Parameter	n-channel MOSFET	p-channel MOSFET
Threshold voltage	$V_{Tn} = 0.5V$	$V_{Tp} = -0.5V$
Transconductance parameter	$\mu_n C_{ox} = 50\mu A/V^2$	$\mu_p C_{ox} = 25\mu A/V^2$
Channel length modulation parameter	$\lambda_n = 0.1V^{-1}/L$ (L in $\mu m$ )	$\lambda_p = 0.1V^{-1}/L$ (L in $\mu m$ )

## 4.4. Two-Port Model for the Common-Source Voltage Amplifier

The circuit shown in Figure 4.25 corresponds to a transconductance amplifier model (with voltage output) since we modeled the MOSFET as a voltage controlled current source, which is in line with its physical behavior in the saturation region. Alternatively, and since the circuit is meant to function as a voltage amplifier, we can equivalently model it using a native voltage amplifier two-port as shown in Figure 4.26. The reader can prove that for this model the open-circuit voltage gain is given by  $A_v = -g_m R_{out}$ , where  $R_{out}$  corresponds to the parallel connection of  $R_D$  and  $r_o$ . The native voltage amplifier model is sometimes preferred since it more directly expresses the intended function we assumed in this chapter. However, as we shall see in Chapter 3, the voltage amplifier two-port is no longer a convenient representation for the CS voltage amplifier when device capacitances are included.

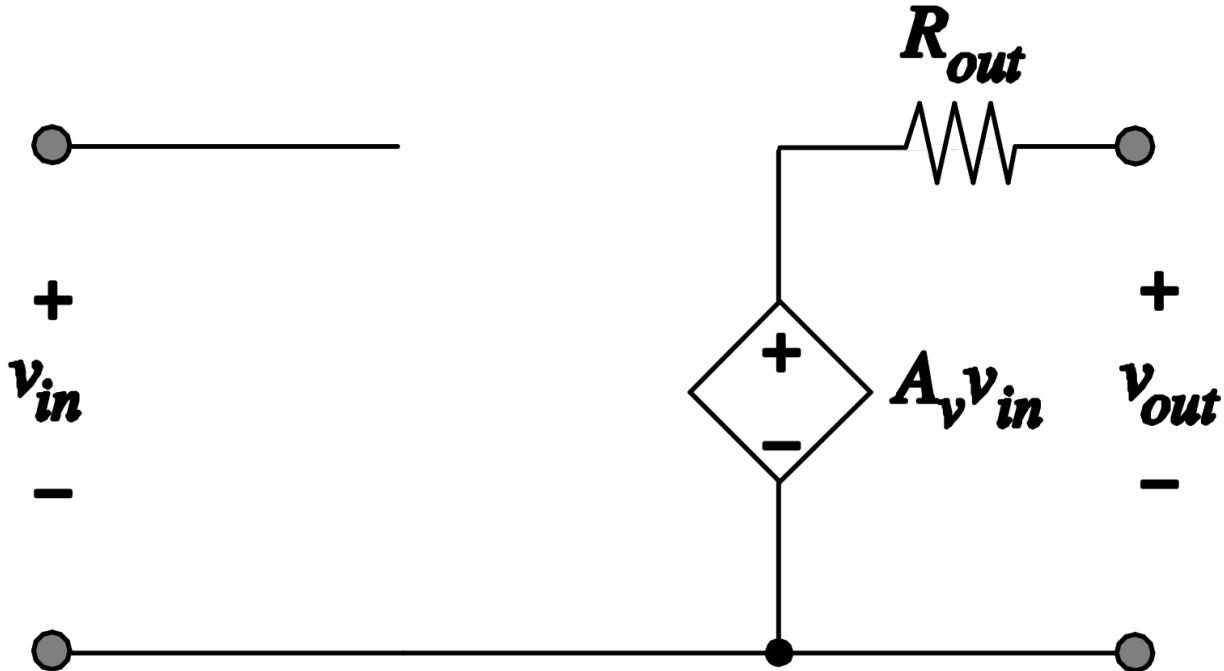


Figure 4.26.: Equivalent voltage amplifier-based model for the common-source amplifier circuit Figure 4.25.

Figure 4.27 shows the small-signal commonsource voltage amplifier model together with an input transducer and load resistance. Since the input resistance of the CS amplifier is infinite, no resistive division takes place at the input port and  $v_{in} = v_s$ . Thus, the overall voltage gain is computed as

$$A'_v = \frac{v_{out}}{v_s} = A_v \cdot \left( \frac{R_L}{R_L + R_{out}} \right) \quad (4.53)$$

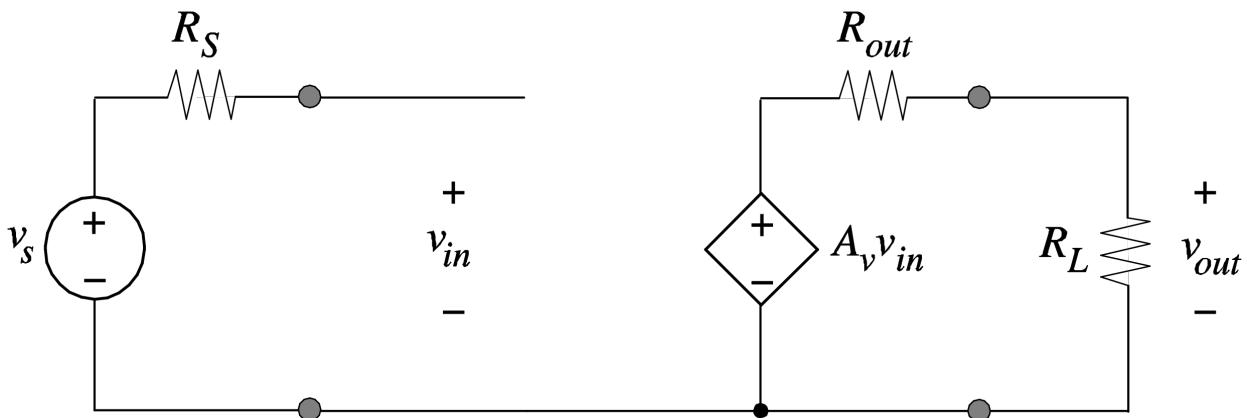


Figure 4.27.: Common-source amplifier model with transducer and load resistance.

The same expression can be found from the circuit of Figure 4.25 with  $R_L$  included across the output port. The reader is invited to prove this.

#### 4. Introduction

As a final note, we should emphasize that adding a load resistance may have implications on the bias point of the circuit. For example, if the load resistor carries a DC current, this current will affect the quiescent point output voltage of the amplifier. In this case, the load resistance must also be connected to the circuit in the operating point analysis where the small-signal parameters such as  $r_o$  are computed. Problem 2-17 looks at an example.

### 4.5. Summary

In this chapter we reviewed the basic I-V characteristics of a MOSFET and employed this device to construct examples of common-source voltage amplifiers. In deriving a model for the MOSFET, we concentrated on first-order effects that define the transistor's operation. The nonlinear nature of even the simplest device model dictates the use of small-signal approximations to enable analyses with manageable complexity. The presented methodology begins by finding the operating point of the transistor. Next, the small-signal equivalent is used to construct a linear small-signal model for further analysis.

We studied the basic common-source voltage amplifier with drain resistance and found that the voltage gain in this circuit is directly proportional to the voltage drop across the resistor, which imposes practical limits on the achievable voltage gain. A modified circuit based on an auxiliary bias current source was then analyzed as an alternative and used as a motivation to incorporate the effect of channel length modulation using the  $\lambda$ -model.

The most important concepts that you should have mastered are:

- Determining MOSFET drain currents in all regions of operation; determining the regions of operation based on the transistor's terminal voltages.
- Constructing transfer characteristics and load line plots for common-source stages for various drain bias configurations.
- Calculating the operating point of a CS stage and the MOSFET's small-signal parameters  $g_m$  and  $r_o$ .
- Drawing the small-signal model of a CS stage and calculating its voltage gain.

### 4.6. References

1. R. F. Pierret, *Semiconductor Device Fundamentals*, Prentice Hall, 1995.
2. P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th Edition, Wiley, 2008.
3. D. O. Pederson and K. Mayaram, *Analog Integrated Circuits for Communication: Principles, Simulation and Design*, 2nd Edition, Springer,
- 4.
5. Y. Tsividis, *Operation and Modeling of the MOS Transistor*, 2nd Edition, McGraw-Hill, New York, 1999.

6. P. G. A. Jespers, *The  $g_m/I_D$  Methodology, a Sizing Tool for Low-Voltage Analog CMOS Circuits*, Springer, 2010.
7. M. J. M. Pelgrom, et al., "Matching properties of MOS transistors," IEEE J. of Solid-State Circuits, pp. 1433-1439, May 1989.
8. G. Gildenblat, et al., "PSP: An Advanced Surface-Potential-Based MOSFET Model for Circuit Simulation," *IEEE Trans. Electron Devices*, pp. 1979-1993, Sept. 2006.

## 4.7. Problems

Unless otherwise stated, use the standard model parameters specified in Table 4.3 for the problems given below. Consider only first-order MOSFET behavior and include channel length modulation (as well as any other second-order effects) only where explicitly stated.

**P2.1** An n-channel transistor biased in saturation with  $W/L = 10$  carries a drain current of 200  $\mu\text{A}$  when  $V_{GS} = 1.5 \text{ V}$  is applied. With  $V_{GS} = 1 \text{ V}$ , the current drops to 50  $\mu\text{A}$ . Determine  $V_{Tn}$  and  $\mu C_{ox}$  of this transistor.

**P2.2** Show that two MOS transistors in series with channel lengths  $L_1$  and  $L_2$  and identical channel widths can be modeled as one equivalent MOS transistor with length  $L_1 + L_2$  (see Figure 4.28). Assume that  $M_1$  and  $M_2$  have identical parameters except for their channel lengths. Hint: there are (at least) two ways to solve this problem. One is through extensive algebra; the other is through physical insight and arguments based on the MOSFET cross-section.

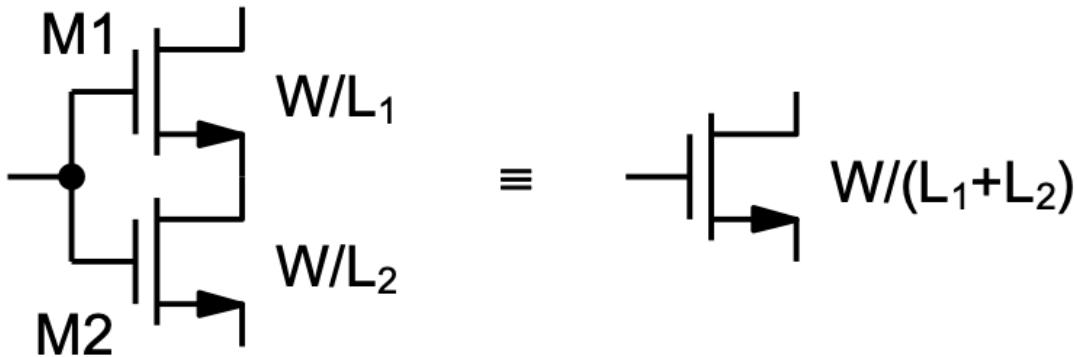


Figure 4.28.

**P2.3** Derive an analytical expression for the input voltage that corresponds to the transition point (point C) between the saturation and triode regions in Figure 4.7(b).

**P2.4** In Example 2-4, we calculated the most negative input excursion that the circuit in Figure 4.10 can handle before the output is clipped to the supply voltage. In this problem, calculate the most positive input excursion that can be applied before the MOSFET enters the triode region. Assume

#### 4. Introduction

the same parameters as in Example 2-4:  $V_{DD} = 5 \text{ V}$ ,  $R_D = 10 \text{ k}\Omega$ ,  $W/L = 10$ , and  $V_{IN}$  is adjusted to  $1.5 \text{ V}$ , so that  $V_{OUT} = 2.5 \text{ V}$  at the circuit's operating point.

**P2.5** For the circuit shown in Figure 4.29, sketch  $v_{OUT}$  as a function of  $v_{IN}$ . Assume that  $v_{IN}$  varies from 0 to 5 V. There is no need to carry out any detailed calculations; simply draw a qualitative graph and mark pertinent asymptotes and breakpoints (such as changes in the MOSFETs region of operation).

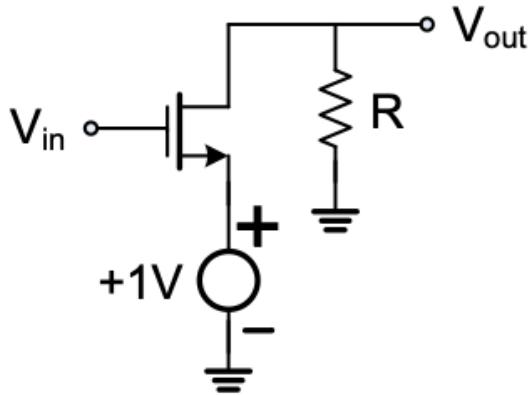


Figure 4.29.

**P2.6** Derive the small-signal voltage gain given by Equation 4.27 through direct differentiation of Equation 4.17, i.e., apply 4.25.

**P2.7** A field effect transistor built using a new (fictitious) material behaves “almost” exactly like a conventional MOSFET in silicon technology. The large signal I-V characteristic (in the saturation region) is given by

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Tn})^{2.5}$$

Assuming that  $\mu C_{ox} W/L = 100 \mu\text{A}/\text{V}^{2.5}$  and  $I_D = 1 \mu\text{A}$ ,

compute the transconductance of the device.

**P2.8** The ratio of the small-signal drain current excursion and quiescent point drain current ( $i_d/I_D$ ) is sometimes called the drain modulation index. Show that for a MOSFET,  $i_d/I_D$  is twice as large as the relative excursion in the gate-source voltage,  $v_{gs}/V_{OV}$ .

**P2.9** Consider the CS amplifier shown Figure 4.10(a). Calculate the small-signal voltage gain assuming  $V_{IN} = 1.5 \text{ V}$ ,  $W/L = 20$ ,  $R_D = 5 \text{ k}\Omega$ , and  $V_{DD} = 5 \text{ V}$ . Be sure to check the device's region of operation.

**P2.10** Consider the p-channel CS amplifier shown in Figure 4.15(a). Assuming  $W/L = 20$ ,  $R_D = 5 \text{ k}\Omega$ , and  $V_{DD} = 5 \text{ V}$ , calculate the required quiescent point input voltage so that  $V_{OUT} = 2.5 \text{ V}$ . What is the small-signal gain of the circuit?

**P2.11** Repeat Problem 2.9 with  $R_D = 10 \text{ k}\Omega$ . With this value, the MOSFET operates in the triode region. Compute the small-signal voltage gain by writing the large-signal relationship between the input and output for the triode region and subsequent differentiation at the operating point.

**P2.12** Consider the cascade connection of two CS amplifiers as shown in Figure 4.30.

- (a) Draw the small-signal equivalent model for this circuit.
- (b) Calculate the small-signal voltage gains  $v_{out1}/v_{in}$  and  $v_{out2}/v_{in}$ . Assume that  $V_{IN} = V_{DD}/2$  and that the device sizes are chosen such that the bias points of nodes  $v_{out1}$  and  $v_{out2}$  are also exactly at  $V_{DD}/2$ .

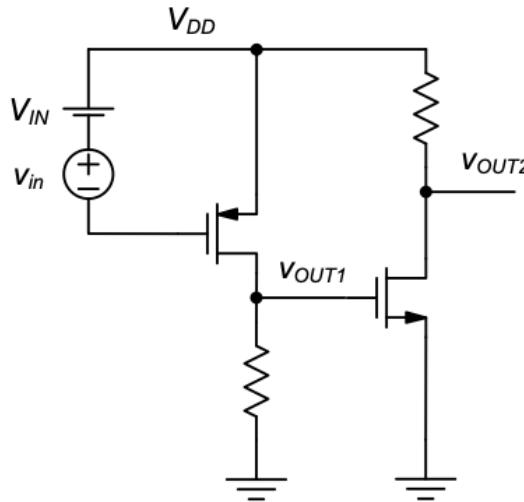


Figure 4.30.

**P2.13** Repeat Problem 2.9 and include the effect of channel length modulation in the small-signal voltage gain calculation. Neglect channel length modulation in the bias point calculation. Quantify the percent difference in the calculated small-signal voltage gain compared to Problem 2.9. Assume that the channel length of the MOSFET is  $2 \mu\text{m}$ .

**P2.14** For the p-channel common-source amplifier shown in Figure 4.15(a)

- (a) Given  $W/L = 12 \mu\text{m}/2 \mu\text{m}$  and  $R_D = 10 \text{ k}\Omega$ , calculate  $V_{IN}$  such that  $V_{OUT}$  is  $2.5 \text{ V}$ .  $V_{DD} = 5 \text{ V}$ . Neglect channel length modulation in this calculation.
- (b) What is the small-signal voltage gain,  $A_v = v_{out}/v_{in}$ ? Include the effect of channel-length modulation in your calculation.
- (c) To increase the voltage gain, you increase  $R_D$  to  $100 \text{ k}\Omega$ . Calculate the new small-signal voltage gain,  $A_v$ . You must re-bias the circuit so that  $V_{OUT} = 2.5 \text{ V}$ .
- (d) We could also try to increase the voltage gain of the initial circuit by increasing  $W/L$  rather than  $R_D$ . Calculate the new  $A_v$  if  $W/L = 120 \mu\text{m}/2 \mu\text{m}$  and  $R_D = 10 \text{ k}\Omega$ . Be sure to re-bias the circuit so that  $V_{OUT} = 2.5 \text{ V}$ .

#### 4. Introduction

**P2.15** Calculate the small-signal gain of the intrinsic gain stage shown in Figure 4.23(a), assuming  $W = 10 \mu\text{m}$  and using the parameters given below. In each case, explicitly calculate the gate overdrive voltage ( $V_{OV}$ ), the transconductance ( $g_m$ ) and the output resistance ( $r_o$ ). Assume that the circuit is biased such that the MOSFET operates in the saturation region. Neglect  $V_{DS}$  dependence in the calculation of  $r_o$ .

- (a)  $I_D = 100 \mu\text{A}$ ,  $L = 2 \mu\text{m}$
- (b)  $I_D = 50 \mu\text{A}$ ,  $L = 2 \mu\text{m}$
- (c)  $I_D = 100 \mu\text{A}$ ,  $L = 4 \mu\text{m}$

**P2.16** Consider the CS amplifier of Figure 4.20(a) with the following parameters:  $V_B = 2.5 \text{ V}$ ,  $I_B = 500 \mu\text{A}$ ,  $W = 20 \mu\text{m}$ ,  $L = 1 \mu\text{m}$ , and  $R_D = 5 \text{ k}\Omega$ .

- (a) Calculate the exact value of  $V_{IN}$  required such that  $I_D = I_B$ , and  $V_{OUT} = V_B$ . Include the effect of channel length modulation in your calculation.
- (b) Using the value of  $V_{IN}$  found in part (a), re-compute  $V_{OUT}$  for the two cases when  $\lambda$  changes by +50% and -50%, respectively. Such discrepancies may be due to variations in the semiconductor process or simply due to uncertainty in the simplistic  $\lambda$ -model.

**P2.17** Consider the CS amplifier shown in Figure 4.31 with the following parameters:  $V_{DD} = 5 \text{ V}$ ,  $V_{IN} = 1.8 \text{ V}$ ,  $W = 15 \mu\text{m}$ ,  $L = 1 \mu\text{m}$ ,  $R_D = 5 \text{ k}\Omega$ , and  $R_L = 10 \text{ k}\Omega$ .

- (a) Calculate the output quiescent point voltage and drain current of the circuit, taking the connected load resistance  $R_L$  into account. Ignore channel-length modulation in this calculation.
- (b) Calculate  $g_m$  and  $r_o$  using the parameters from part (a). Take  $V_{DS}$  dependence into account.
- (c) Draw a two-port voltage amplifier model for the circuit and calculate the open-circuit voltage gain ( $A_v$ ) and overall voltage gain ( $A'_v$ ) with the load resistor connected.
- (d) Repeat parts (a) and (b) without considering the connected  $R_L$  and recompute the two-port parameters of part (c). Summarize the observed differences.

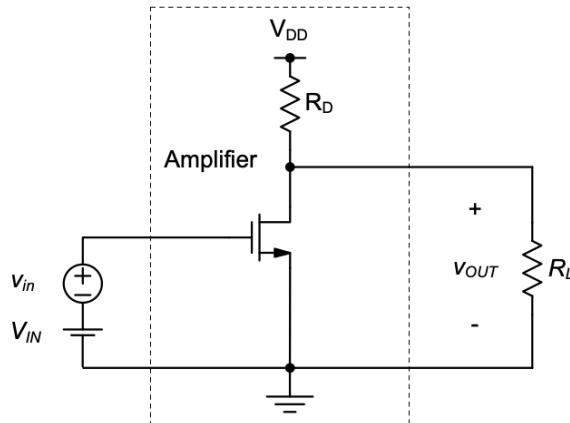


Figure 4.31.

## **Part II.**

# **Learn to Walk — Real Transistors, Noise, Mismatch, and Distortion**



## **5. Introduction**

TBD.



## **Part III.**

# **Dare to Run — Knowledge Base for State-of-the-Art Circuits**



## **6. Introduction**

TBD.



**Part IV.**

**References**



# References

- Gray, Paul R, Paul J Hurst, Stephen H Lewis, and Robert G Meyer. 2009. *Analysis and Design of Analog Integrated Circuits*. John Wiley & Sons.
- Robert, F. 2003. “Pierret: Semiconductor Device Fundamentals.” Reading, MA: Addison-Wesley.
- Staszewski, Robert Bogdan, Dirk Leipold, O Eliezer, Mitch Entezari, Khurram Muhammad, Imran Bashir, C-M Hung, et al. 2008. “A 24mm 2 Quad-Band Single-Chip GSM Radio with Transmitter Calibration in 90nm Digital CMOS.” In *2008 IEEE International Solid-State Circuits Conference-Digest of Technical Papers*, 208–607. IEEE.
- Ulaby, Fawwaz Tayssir, and Michel M Maharbiz. 2013. *Circuit Analysis and Design*. 2nd Edition. NTS Press.

