Microprocessor & Microcontroller Systems (1333202) - Summer 2024 Solution

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Question 1(a) [3 marks]

List common features of 8051 microcontroller.

Solution

The 8051 is a popular 8-bit microcontroller with the following key features:

Table 1. Common Features of 8051

Feature	Description
On-chip Oscillator	Built-in clock generator circuit (typically 12MHz)
Program Memory	4KB internal ROM for code storage
Data Memory	128 bytes internal RAM for variables
I/O Ports	4 bidirectional 8-bit ports (P0, P1, P2, P3)
Timers/Counters	Two 16-bit Timer/Counter units (Timer 0, Timer 1)
Serial Port	One Full duplex UART channel for communication
Interrupts	5 interrupt sources (2 external, 2 timer, 1 serial) with priority levels
SFRs	Special Function Registers for system control

Mnemonic

"On Program Data I/O Timers Serial Interrupts SFRs"

Question 1(b) [4 marks]

Define T-State, Machine Cycle, Instruction Cycle and Opcode.

Solution

These terms define the timing and operation of a microprocessor:

Table 2. Microprocessor Timing Definitions

Term	Definition	Duration/-Size
T-State	One subdivision of the operation performed in one clock period. It is the basic unit of time.	$1/f_{clk}$
Machine Cycle	Time required to complete one memory access (read/write) or I/O operation.	3-6 T-states (8085)
Instruction Cycle	Time required to fetch, decode, and execute a complete instruction.	1-5 Machine cycles
Opcode	Operation Code: The part of the instruction that specifies the operation to be performed.	1 byte

- **T-State**: Smallest unit of processing time.
- **Machine Cycle**: Basic CPU operation (Fetch, Read, Write).
- **Instruction Cycle**: Cycle = Fetch + Decode + Execute.

Mnemonic

"Time Machine Instruction Operation"

Question 1(c) [7 marks]

Compare Von-Neumann and Harvard Architecture.

Solution

Here is the comparison between the two major computer architectures:

Table 3. Von-Neumann vs Harvard Architecture

Parameter	Von-Neumann	Harvard
Memory Organization	Single shared memory for both Code and Data.	Separate physical memory for Program Code and Data.
Bus Structure	Single bus for fetching instruction and data.	Separate buses for instruction and data.
Speed	Slower execution due to serial fetching (bottleneck).	Faster execution as instruction and data can be fetched simultaneously.
Cost	Simpler hardware, lower cost.	More buses, bigger control unit, higher cost.
Flexibility	Efficient use of memory (code/data boundary is flexible).	Fixed amount of memory for code and data.
Examples	8085, x86 PCs.	8051, DSP chips.

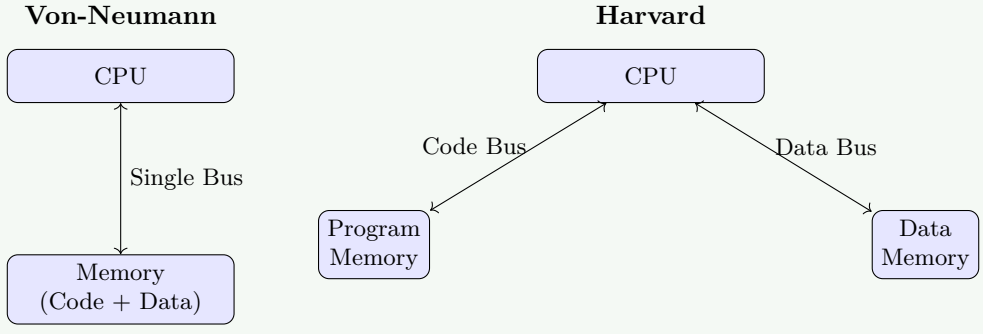


Figure 1. Architecture Comparison

Mnemonic

"Von-Single Harvard-Dual"

Question 1(c) OR [7 marks]

Explain Microcomputer System with block diagram.

Solution

A microcomputer system consists of a CPU, memory, I/O devices, and a system bus interconnecting them.

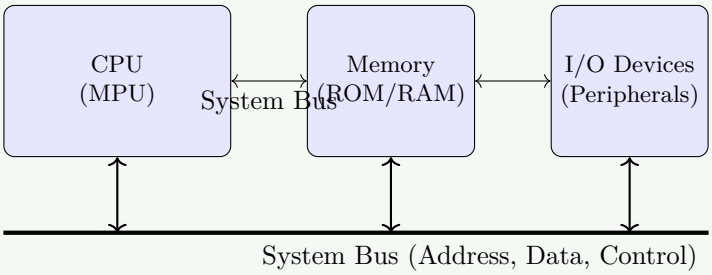


Figure 2. Microcomputer System Block Diagram

Table 4. System Components

Component	Function	Example
CPU	The "Brain". Fetches and executes instructions, reads/writes data. Control center.	8085, 8086
Memory	Stores instructions (ROM) and temporary data/variables (RAM).	EPROM, SRAM
I/O Unit	Interface to the outside world (Keyboard, Display, Sensors).	8255 PPI
System Bus	Set of wires to transfer Information. Includes Address, Data, and Control buses.	Ribbon Cable

Question 2(a) [3 marks]

Draw Bus organization in 8085 Microprocessor.

Solution

The 8085 has three sets of buses:

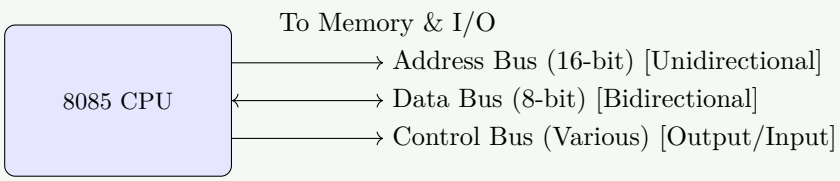


Figure 3. 8085 Bus Organization

Question 2(b) [4 marks]

List Flags used in 8085 and Explain working of each flags.

Solution

The 8085 has a 5-bit Flag Register containing status flags that are set/reset by ALU operations.

D7	D6	D5	D4	D3	D2	D1	D0	
S	**Z**	**x**	**AC**	**x**	**P**	**x**	**CY**	x = Undefined

Figure 4. Flag Register Format

Table 5. 8085 Flags

Flag	Bit	Function
S (Sign)	D7	Set to 1 if MSB of result is 1 (Negative), else 0.
Z (Zero)	D6	Set to 1 if result is Zero, else 0.
AC (Aux Carry)	D4	Set to 1 if carry generated from D3 to D4 (Lower nibble to Upper nibble). Used in BCD.
P (Parity)	D2	Set to 1 if result has even number of 1s (Even Parity), else 0.
CY (Carry)	D0	Set to 1 if operation generates a carry/borrow out of MSB.

Question 2(c) [7 marks]

Draw and Explain Block Diagram of 8085.

Solution

The 8085 architecture consists of the ALU, Timing & Control Unit, Registers, and Interrupt control.

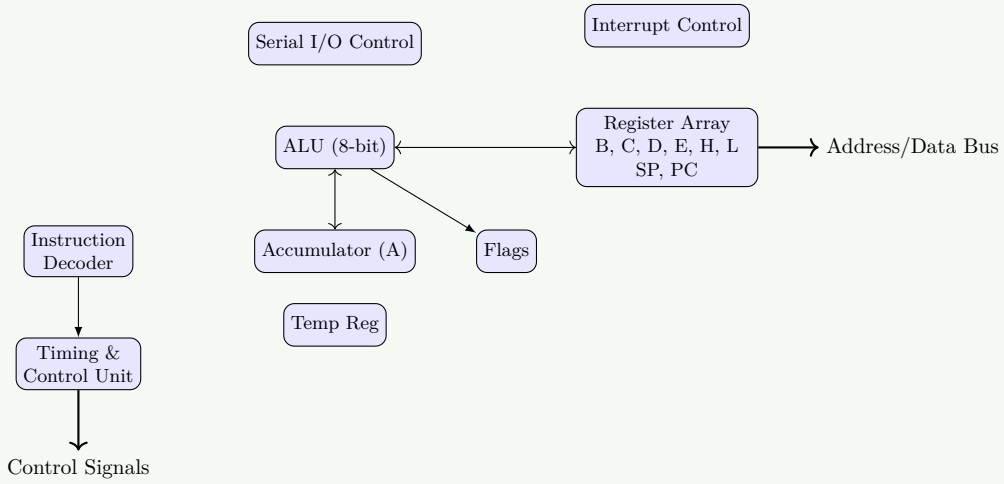


Figure 5. 8085 Architecture Block Diagram

Table 6. Functional Blocks

Block	Function
ALU	Performs arithmetic (+, -) and logical (AND, OR) operations.
Registers	General purpose (B-C, D-E, H-L) and Special (SP, PC, A).
Accumulator	8-bit register connected to ALU, stores result of operations.
Program Counter (PC)	16-bit register holding address of next instruction to fetch.
Stack Pointer (SP)	16-bit register holding address of top of stack RAM.
Timing & Control	Generates control signals (RD, WR, ALE) to coordinate operations.

Question 2(a) OR [3 marks]

Explain Instruction Fetching, Decoding and Execution Operation in microprocessor.

Solution

The instruction cycle consists of three phases:

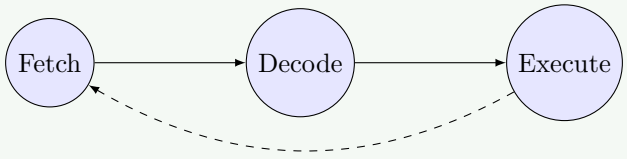


Figure 6. Instruction Cycle

- **Fetch**: The CPU places the PC address on the address bus. Memory sends the instruction opcode via data bus to the Instruction Register.
- **Decode**: The decoder interprets the opcode to determine what action is required (e.g., ADD, MOV).
- **Execute**: The Control Unit generates signals to perform the action (e.g., read data, perform ALU op).

Question 2(b) OR [4 marks]

What is Demultiplexing of Lower order Address and Data lines in 8085? Explain using neat sketch.

Solution

Address/Data lines AD0-AD7 are multiplexed to save pins. Software must separation them using the `ALE` signal and an external latch.

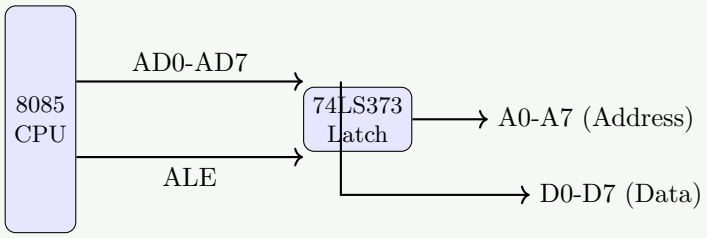


Figure 7. Demultiplexing Circuit

- **ALE = 1**: The bus AD0-AD7 carries Address. The Latch is enabled and captures the address.
- **ALE = 0**: The bus AD0-AD7 carries Data. The Latch holds the previous address constant on its output.
- Even when AD lines change to Data, memory still sees the Address from the Latch.

Question 2(c) OR [7 marks]

Draw and Explain Pin Diagram of 8085.

Solution

The 8085 is a 40-pin DIP IC.

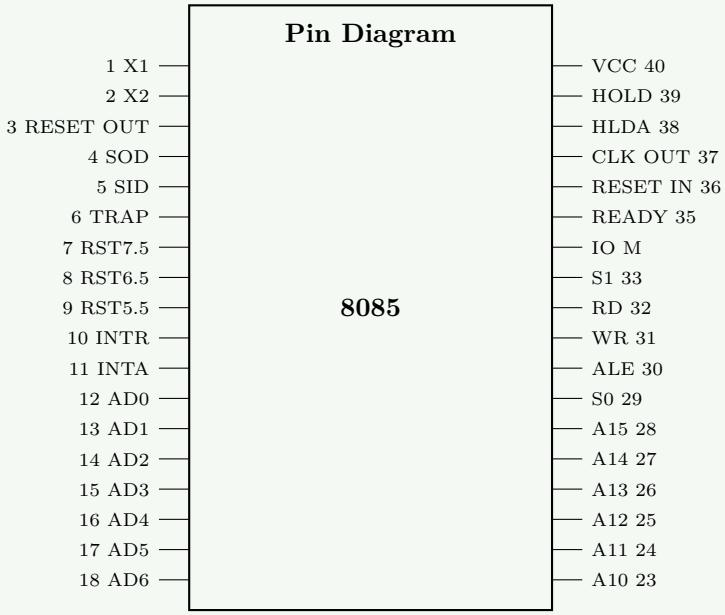


Figure 8. 8085 Pin Detail

Table 7. Pin Description

Pin Group	Function
High Address (A8-A15)	Carries most significant byte of address.
Multiplexed (AD0-AD7)	Carries lower address byte (T1) and Data (T2, T3).
Control (RD, WR, ALE)	READ, WRITE control and Address Latch Enable.
Status (IO/M, S0, S1)	Indicates type of machine cycle (Memory vs I/O, Read vs Write).
Interrupts	TRAP (Non-maskable), RST7.5, 6.5, 5.5, INTR.
Serial I/O	SID (Input), SOD (Output) for serial data.

Question 3(a) [3 marks]

Draw IP SFR of 8051 and Explain function of each bit.

Solution

The Interrupt Priority (IP) register (Address B8H) determines priority levels (High/Low).

D7							D0
-	-	**PT2**	**PS**	**PT1**	**PX1**	**PT0**	**PX0**

Figure 9. IP Register

- **1 = High Priority**, **0 = Low Priority**.
- **PS**: Serial Port Priority.

- **PTx**: Timer x Priority.
- **PXx**: External Interrupt x Priority.

Question 3(b) [4 marks]

Draw and explain Timer/Counter Logic diagram for 8051.

Solution

Timers count cycles from oscillator (Timer mode) or external pin events (Counter mode).

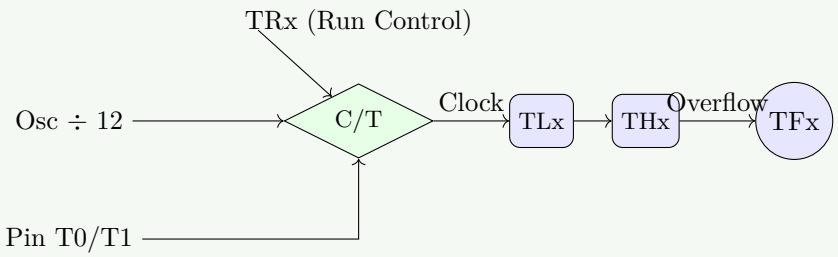


Figure 10. Timer Logic Block Diagram

Question 3(c) [7 marks]

Draw and Explain Block Diagram of 8051.

Solution

The 8051 is a comprehensive microcontroller with built-in memory and I/O.

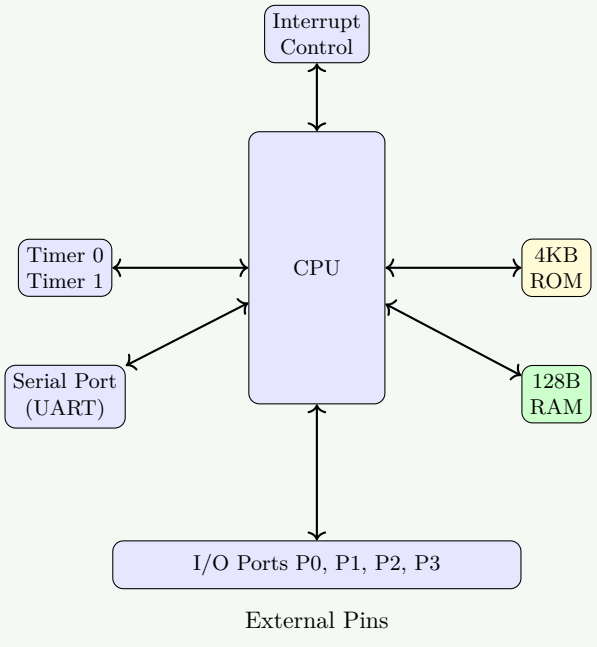


Figure 11. 8051 Architecture

- **CPU**: 8-bit central processor.
- **Memory**: Harvard architecture. 4KB On-chip Code ROM, 128 Bytes On-chip Data RAM.

- **I/O Ports**: 4 ports (P0-P3), each 8-bit. Total 32 pins.
- **Timers**: Two 16-bit timers (T0/T1) for delays or counting.
- **Serial Port**: Full-duplex UART (TXD, RXD).

Question 3(a) OR [3 marks]

Draw PCON SFR of 8051 and Explain function of each bit.

Solution

PCON (Power Control) at 87H controls power modes and baud rate doubling.

SMOD	-	-	-	GF1	GF0	PD	IDL

Figure 12. PCON Register

- **SMOD**: Double Baud Rate. 1 = Doubles baud rate for Timer 1.
- **GF1/GF0**: General purpose flags.
- **PD**: Power Down mode. Oscillator stops.
- **IDL**: Idle mode. Clock to CPU stops, but Interrupts/Timers run.

Question 3(b) OR [4 marks]

In 8051 Serial communication Mode 1, For XTAL=11.0592 MHz, find TH1 value needed to have for 9600 and 4800 baud rate.

Solution

Formula:

$$\text{Baud Rate} = \frac{2^{SMOD}}{32} \times \frac{XTAL}{12 \times (256 - TH1)}$$

Assuming SMOD=0 (Normal speed) and XTAL = 11.0592 MHz.

1. For 9600 Baud:

$$9600 = \frac{11059200}{32 \times 12 \times (256 - TH1)}$$

$$9600 = \frac{28800}{256 - TH1}$$

$$256 - TH1 = \frac{28800}{9600} = 3$$

$$TH1 = 256 - 3 = 253 = \textbf{FD H}$$

2. For 4800 Baud:

$$256 - TH1 = \frac{28800}{4800} = 6$$

$$TH1 = 256 - 6 = 250 = \textbf{FA H}$$

Question 4(a) [3 marks]

What are the differences in LCALL and LJMP instructions in 8051?

Solution

Table 8. LCALL vs LJMP

Feature	LCALL (Long Call)	LJMP (Long Jump)
Action	Calls a subroutine.	Jumps to an address.
Stack	Pushes PC (return address) to Stack.	Does NOT affect Stack.
Return	Requires `RET` at end of subroutine.	No return; one-way transfer.
Address	16-bit destination (64KB range).	16-bit destination (64KB range).

Question 4(b) [4 marks]

Write 8051 Assembly Language Program to generate square wave on port 1.0 using Timer0.

Solution

Listing 1. Square Wave Generation

```
    ORG 0000H
    LJMP MAIN

    ORG 0030H
MAIN:
    MOV TMOD, #01H      ; Timer 0, Mode 1 (16-bit)
LOOP:
    MOV TH0, #0FFH      ; Load high byte (Example value)
    MOV TL0, #000H      ; Load low byte
    SETB TR0            ; Start Timer
WAIT:
    JNB TF0, WAIT       ; Wait for Overflow Flag
    CLR TR0             ; Stop Timer
    CLR TF0             ; Clear Flag
    CPL P1.0            ; Complement P1.0 (Toggle)
    SJMP LOOP           ; Repeat
    END
```

Question 4(c) [7 marks]

Explain any three Logical and any four Data Transfer Instruction of 8051 with example.

Solution

Logical Instructions:

- `ANL A, Rn`: Logical AND Register Rn with Accumulator. Result in A.
  Ex: `ANL A, R2`
- `ORL A, #data`: Logical OR immediate data with A.
  Ex: `ORL A, #30H`
- `XRL A, direct`: Logical XOR memory content with A.
  Ex: `XRL A, 40H`

Data Transfer Instructions:

- `MOV A, Rn`: Move content of Register to Accumulator.
  Ex: `MOV A, R5`
- `MOVX A, @DPTR`: Move External RAM data pointed by DPTR to A.
  Ex: `MOVX A, @DPTR`

- `PUSH direct`: Push content of memory address onto Stack.
  Ex: `PUSH 0E0H` (Push A)
- `MOVC A, @A+DPTR`: Move Code Byte from ROM relative to DPTR.
  Ex: `MOVC A, @A+DPTR`

Question 4(a) OR [3 marks]

Explain Instructions: (i) RRC A (ii) POP (iii) CLR PSW.7

Solution

1. **RRC A**: Rotate Accumulator Right through Carry. MSB takes Carry value, Carry takes LSB.
2. **POP direct**: Pop byte from Stack into destination address. SP is decremented.
3. **CLR PSW.7**: Clears the Carry Flag (CY). PSW.7 corresponds to the Carry bit.

Question 4(b) OR [4 marks]

Write 8051 Assembly Language Program to Divide data stored in location 30H by data stored in location 31H and store remainder in 40h and quotient in 41h memory location.

Solution

Listing 2. Division Program

```
    ORG 0000H
    MOV A, 30H      ; Dividend (Numerator)
    MOV B, 31H      ; Divisor (Denominator)
    DIV AB          ; Divide A by B
    ; Result: A = Quotient, B = Remainder
    MOV 41H, A      ; Store Quotient
    MOV 40H, B      ; Store Remainder
    END
```

Question 4(c) OR [7 marks]

List Addressing Modes of 8051 Microcontroller and Explain each with Example.

Solution

Table 9. 8051 Addressing Modes

Mode	Explanation	Example
Immediate	Operand is provided in the instruction itself (#).	`MOV A, #25H`
Register	Operand is in one of the registers R0-R7.	`MOV A, R0`
Direct	Direct memory address is specified.	`MOV A, 30H`
Register Indirect	Address is held in R0 or R1 (@).	`MOV A, @R0`
Indexed	Base address + Accumulator offset. Used for ROM lookups.	`MOVC A, @A+DPTR`

Question 5(a) [3 marks]

Draw Interfacing of Relay with 8051 microcontroller.

Solution

A relay requires a driver transistor as it uses high current.

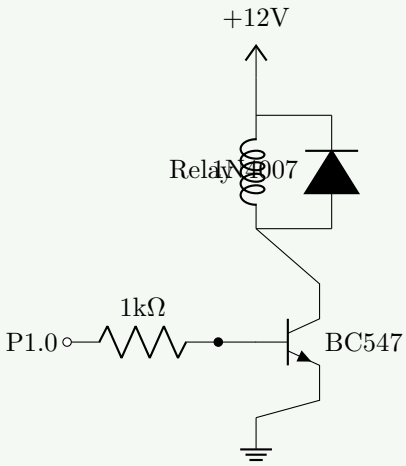


Figure 13. Relay Interfacing

Question 5(b) [4 marks]

Interface 7 Segment display with 8051 microcontroller and write a program to print "1" on it.

Solution

Assuming Common Cathode display on Port 1.

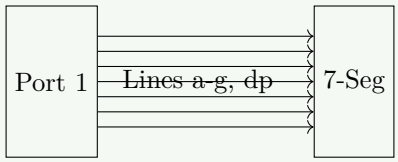


Figure 14. 7-Segment Interface

Listing 3. Display Digit 1

```
    ; For Common Cathode, segments B, C must be 1.
    ; Pattern: dp g f e d c b a
    ; "1" -> 0 0 0 0 0 1 1 0 = 06H
    MOV P1, #06H
    END
```

Question 5(c) [7 marks]

Interface DAC 0808 with 8051 microcontroller and write a program to generate Square wave.

Solution

DAC 0808 is an 8-bit DAC. Port 2 connects to D0-D7.

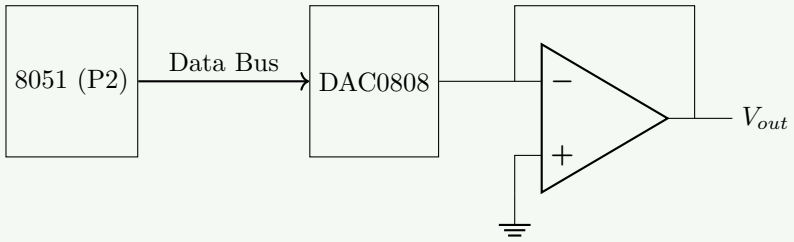


Figure 15. DAC Interfacing

Listing 4. Square Wave via DAC

```
LOOP:
    MOV P2, #00H      ; Min Voltage (0V)
    ACALL DELAY       ; Wait
    MOV P2, #0FFH     ; Max Voltage (5V)
    ACALL DELAY       ; Wait
    SJMP LOOP
DELAY:
    MOV R0, #255
DL: DJNZ R0, DL
    RET
```

Question 5(a) OR [3 marks]

Interface of Push button Switch with 8051 microcontroller.

Solution

A push button connects a pin to Ground. A pull-up resistor ensures High logic when open.

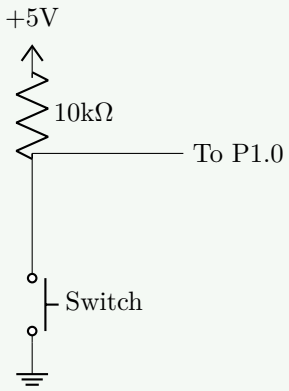


Figure 16. Switch Interface

Question 5(b) OR [4 marks]

Interface DC Motor with 8051 microcontroller.

Solution

Use a Darlington Transistor (like TIP122) or MOSFET to drive the motor current.

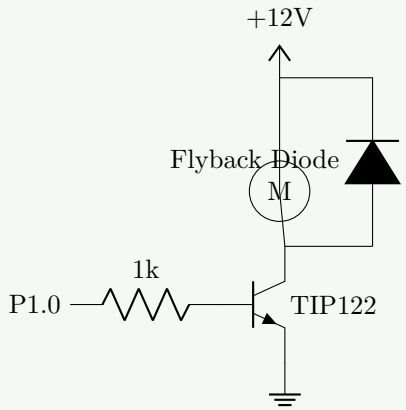


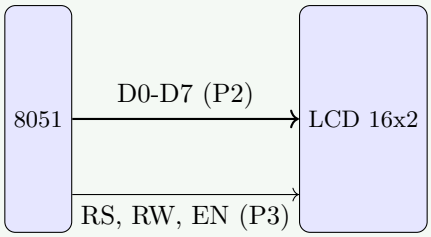
Figure 17. DC Motor Driver

Question 5(c) OR [7 marks]

Interface LCD with 8051 microcontroller and write a program to display ”Hello”.

Solution

LCD 16x2 works in 8-bit mode. Data lines to P2, Control to P3.



Listing 5. LCD ”HELLO”

```
    MOV A, #38H     ; Init 2 lines, 5x7 matrix
    ACALL CMD
    MOV A, #0EH     ; Display ON, Cursor ON
    ACALL CMD
    MOV A, #'H'     ; Data H
    ACALL DAT
    MOV A, #'E'
    ACALL DAT
    ; ... (L, L, O)
    SJMP $
CMD:
    MOV P2, A
    CLR P3.0        ; RS=0 (Command)
    SETB P3.1       ; EN=1
    CLR P3.1        ; EN=0 (Latch)
    ACALL DELAY
    RET
DAT:
    MOV P2, A
    SETB P3.0       ; RS=1 (Data)
```

```
    SETB P3.1
    CLR P3.1
    ACALL DELAY
    RET
```