

# Subject Name Solutions

1323202 – Summer 2024

Semester 1 Study Material

*Detailed Solutions and Explanations*

## Question 1(a) [3 marks]

What is heat sink. lists its types

### Solution

A heat sink is a passive device that absorbs and dissipates heat from electronic components to prevent overheating.

Table 1: Types of Heat Sinks

Type	Description
<b>Passive</b>	Uses natural convection without external power
<b>Active</b>	Incorporates fans or liquid cooling
<b>Radial</b>	Fins arranged in radial pattern from center
<b>Pin-fin</b>	Uses pins or rods for increased surface area
<b>Extruded</b>	Made by forcing aluminum through shaped die

### Mnemonic

“PAPER” (Passive, Active, Pin-fin, Extruded, Radial)

## Question 1(b) [4 marks]

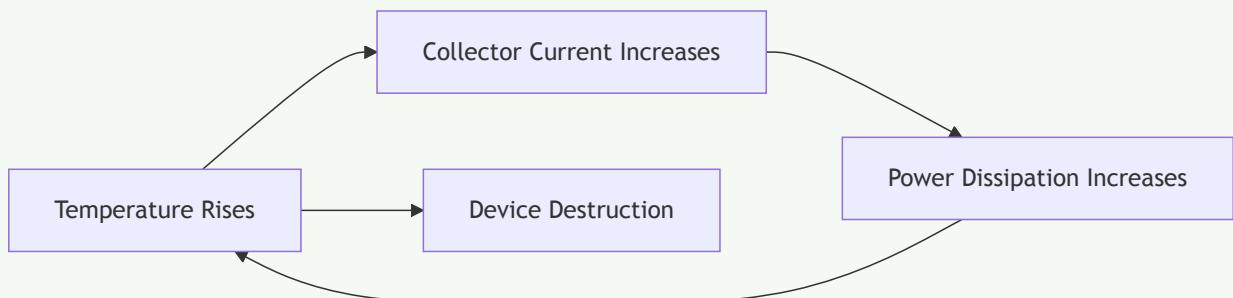
Define the Following: 1. Thermal Runaway 2. Thermal Stability

### Solution

**Thermal Runaway:** The self-accelerating destructive process where increased temperature causes increased current flow, which further increases temperature, potentially destroying the transistor.

**Thermal Stability:** The ability of a transistor circuit to maintain stable operation despite temperature changes, preventing thermal runaway.

### Diagram: Thermal Runaway Process



### Mnemonic

“RISE” (Runaway Is Self-Escalating)

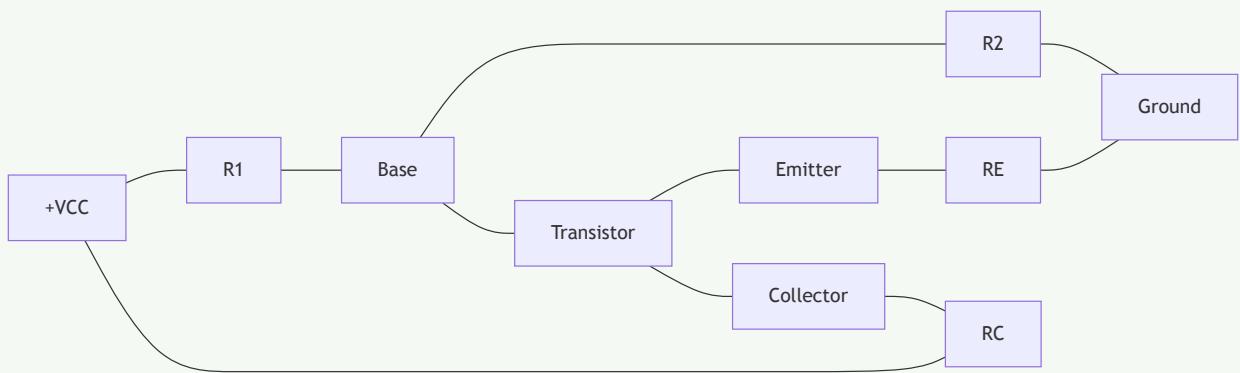
## Question 1(c) [7 marks]

Explain voltage divider bias in details.

## Solution

Voltage divider bias is a common transistor biasing technique that provides stable operation.

**Circuit Diagram:**



- **Voltage divider network:** R1 and R2 establish a fixed base voltage
- **Stable Q-point:** Maintains operating point despite temperature variations
- **Better stability:** Higher stability factor compared to fixed bias
- **Self-adjusting:** Base current automatically adjusts to counter temperature changes

## Mnemonic

“VSST” (Voltage divider, Stable, Self-adjusting, Temperature resistant)

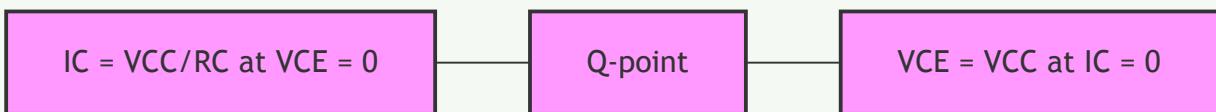
## Question 1(c) OR [7 marks]

Explain D.C. Load Line in details.

## Solution

DC Load Line is a graphical method for analyzing transistor bias conditions.

**Diagram: DC Load Line on Transistor Characteristic Curves**



- **Definition:** Graphical line showing all possible operating points for a given circuit
- **Endpoints:** (0, VCC/RC) and (VCC, 0) on IC-VCE plane
- **Q-point:** Intersection of load line with transistor characteristic curve
- **Equation:**  $IC = (VCC - VCE)/RC$

## Mnemonic

“QECC” (Q-point Exists where Collector Current meets characteristics)

## Question 2(a) [3 marks]

Explain how transistor works as a switch.

## Solution

A transistor switch operates in either saturation (ON) or cutoff (OFF) regions.

Table 2: Transistor Switch Operation

State	Region	Base Current	Collector Current	VCE
OFF	Cutoff	$IB \approx 0$	$IC \approx 0$	$VCE \approx VCC$
ON	Saturation	$IB > IB(\text{sat})$	$IC \approx IC(\text{sat})$	$VCE \approx 0.2V$

## Mnemonic

“COS” (Cutoff Off, Saturation on)

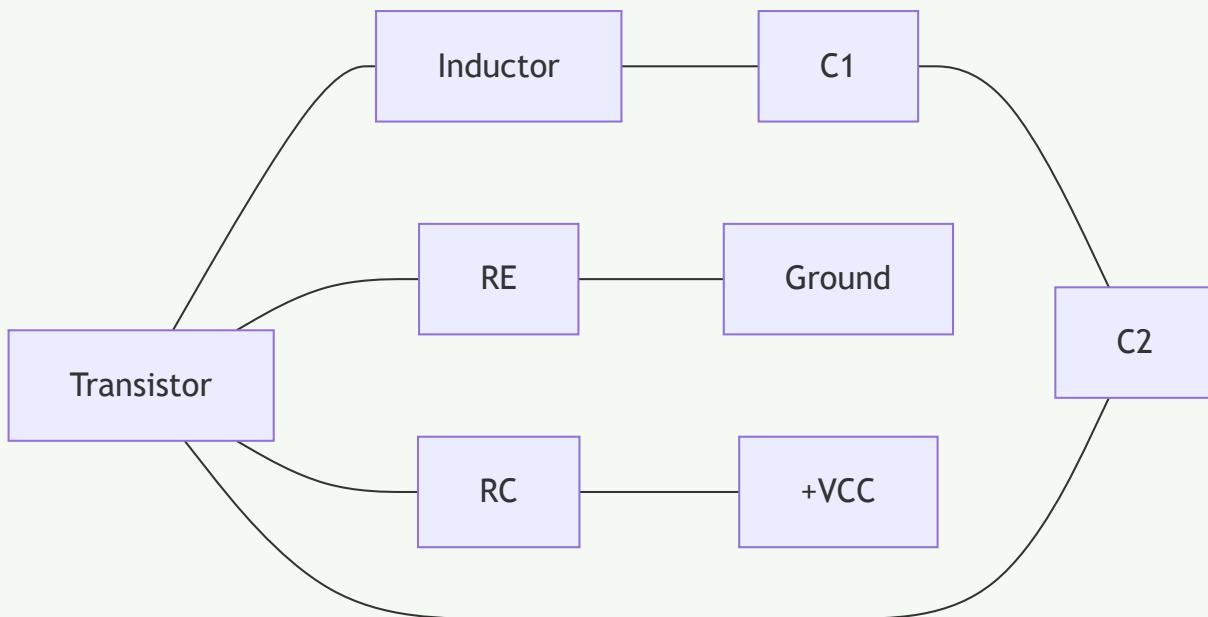
## Question 2(b) [4 marks]

Draw and explain colpitt oscillator.

### Solution

Colpitt oscillator is an LC oscillator using a capacitive voltage divider for feedback.

**Circuit Diagram:**



- **Feedback:** Provided by capacitive voltage divider ( $C_1, C_2$ )
- **Resonant frequency:**  $f = 1/(2 \sqrt{L})$ , where  $C = (C_{12})/(C_1 + C_2)$
- **Oscillation:** Maintains through regenerative feedback
- **Phase shift:**  $360^\circ$  around the loop

## Mnemonic

“CFPO” (Capacitive Feedback Produces Oscillations)

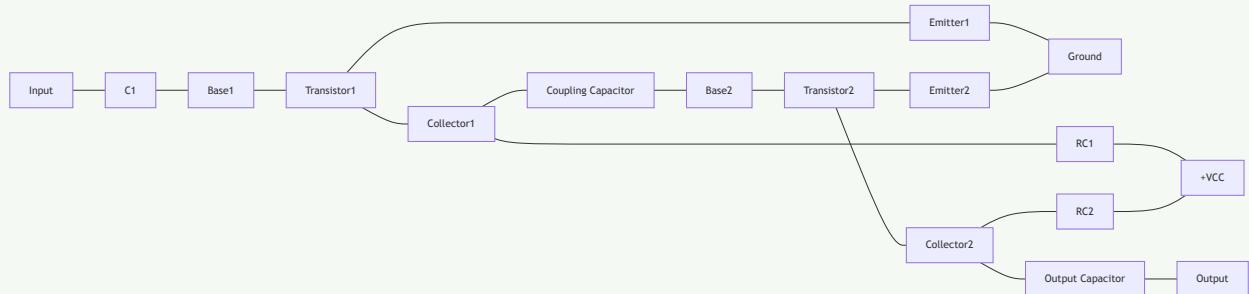
## Question 2(c) [7 marks]

Explain Frequency Response Two Stage RC Coupled Amplifier with circuit diagram.

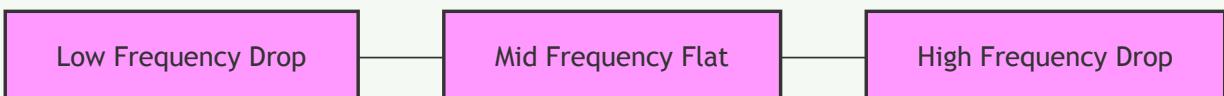
### Solution

Two-stage RC coupled amplifier combines two amplifier stages with RC coupling.

**Circuit Diagram:**



## Frequency Response:



- **Low frequency:** Gain drops due to coupling capacitor impedance
  - **Mid frequency:** Maximum flat gain region (bandwidth)
  - **High frequency:** Gain drops due to transistor capacitance effects
  - **Overall gain:** Product of individual stage gains

## Mnemonic

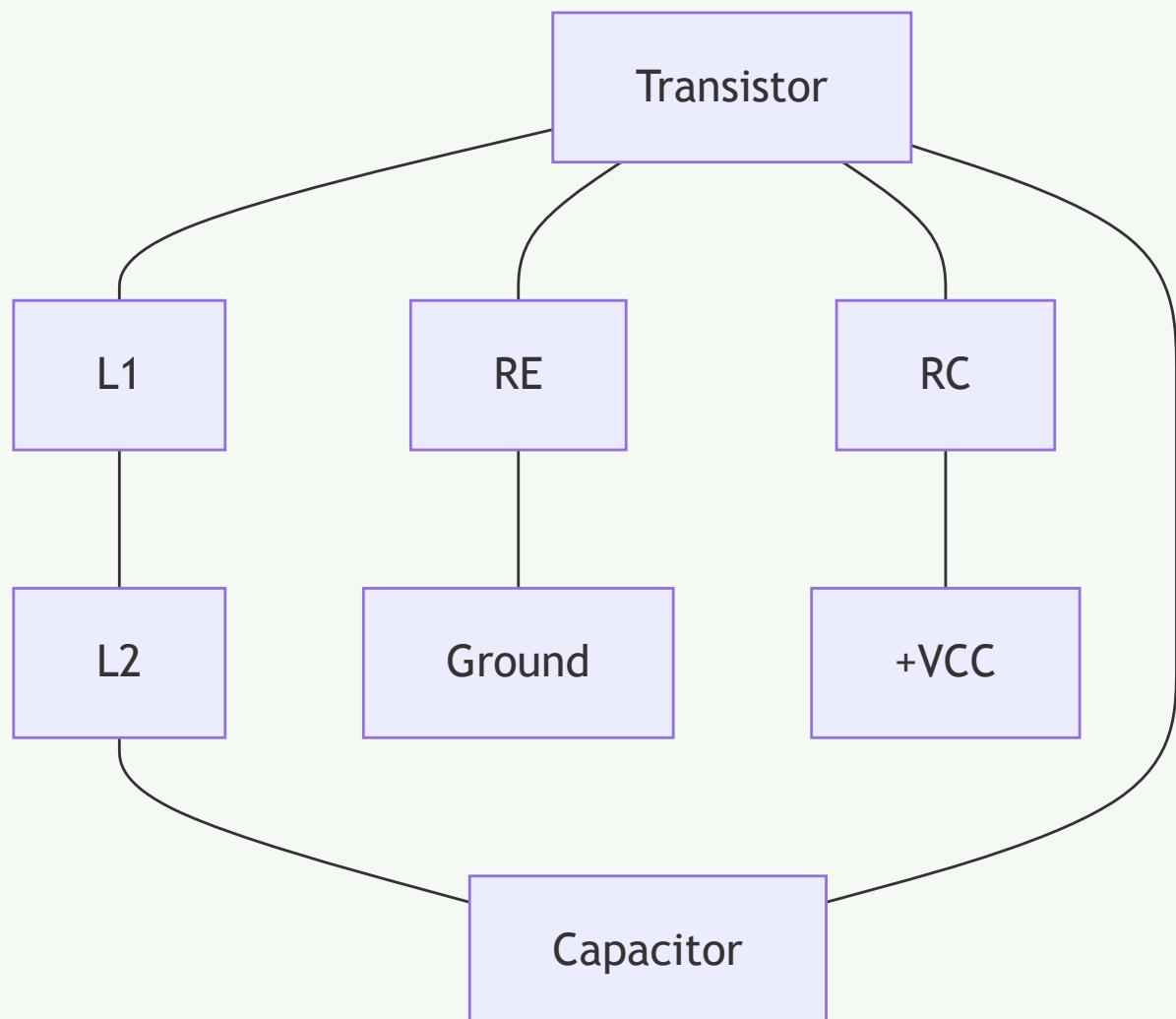
“LMH” (Low drops, Mid flat, High drops)

### Question 2(a) OR [3 marks]

**Draw circuit diagram of Hartley oscillator.**

## Solution

### Circuit Diagram of Hartley Oscillator:



## Mnemonic

“ITLC” (Inductor Tapped for LC Circuit)

## Question 2(b) OR [4 marks]

List different types of negative feedback.

### Solution

Table 3: Types of Negative Feedback

Type	Configuration	Effect on Parameters
Voltage Series	Output voltage fed to input in series	Increases input impedance, reduces distortion
Voltage Shunt	Output voltage fed to input in parallel	Decreases input impedance, increases bandwidth
Current Series	Output current fed to input in series	Increases output impedance, stabilizes current gain
Current Shunt	Output current fed to input in parallel	Decreases output impedance, stabilizes voltage gain

## Mnemonic

“VSCS” (Voltage Series, Current Shunt)

## Question 2(c) OR [7 marks]

List advantages of Negative feedback amplifier and Explain voltage series negative feedback in details.

### Solution

#### Advantages of Negative Feedback:

- Stabilizes gain against component variations
- Reduces distortion and noise
- Increases bandwidth
- Modifies input/output impedance
- Improves linearity

#### Voltage Series Negative Feedback:



- **Configuration:** Output voltage sampled, fed back in series with input
- **Closed-loop gain:**  $A_{CL} = A/(1+A)$ , where  $A$  is open-loop gain and  $A_{FB}$  is feedback fraction
- **Input impedance:** Increases by factor  $(1+A)$
- **Output impedance:** Decreases by factor  $(1+A)$

## Mnemonic

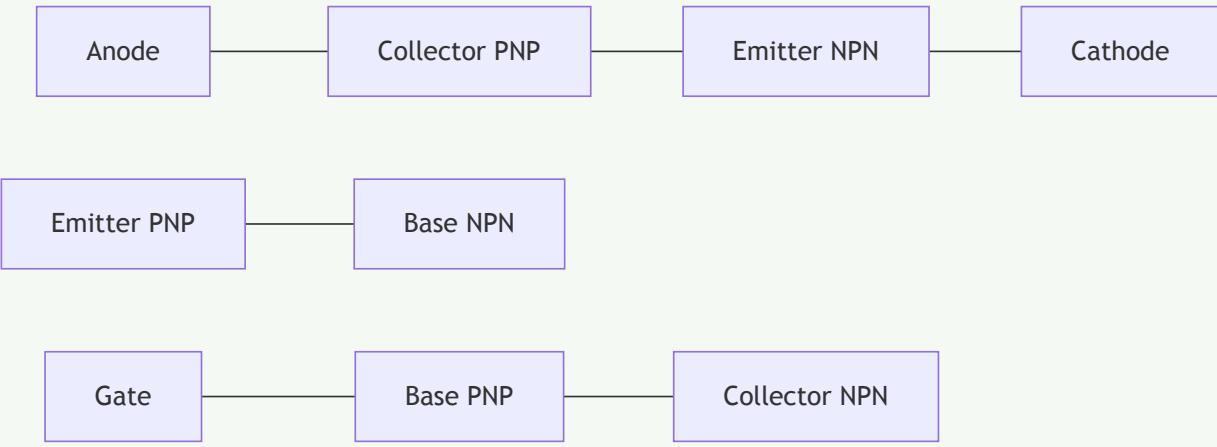
“SIGO” (Stable gain, Increased input impedance, Gain reduction, Output impedance reduction)

## Question 3(a) [3 marks]

Draw circuit of SCR using two transistor analogy.

## Solution

Two Transistor Analogy of SCR:



## Mnemonic

“PNPNPN” (PNP and NPN structure)

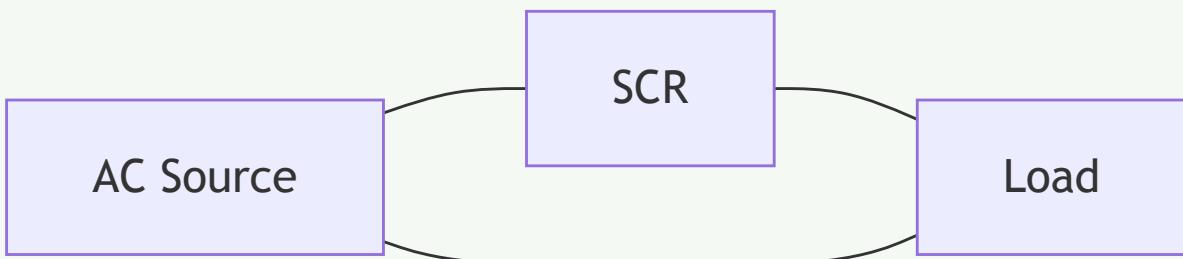
## Question 3(b) [4 marks]

Draw and explain Natural Commutation of SCR.

## Solution

Natural commutation occurs when the SCR current naturally falls below the holding current.

Circuit Diagram:



Current Waveform:

1  
2  
3  
4 SCR OFF     SCR OFF  
5        SCR ON     SCR ON

- **Definition:** SCR turns off automatically when current falls below holding current
- **AC circuit:** Occurs naturally at end of each positive half-cycle
- **Zero crossing:** SCR turns off when AC voltage crosses zero
- **No external circuit:** No additional components needed for turn-off

## Mnemonic

“NAZC” (Natural At Zero Crossing)

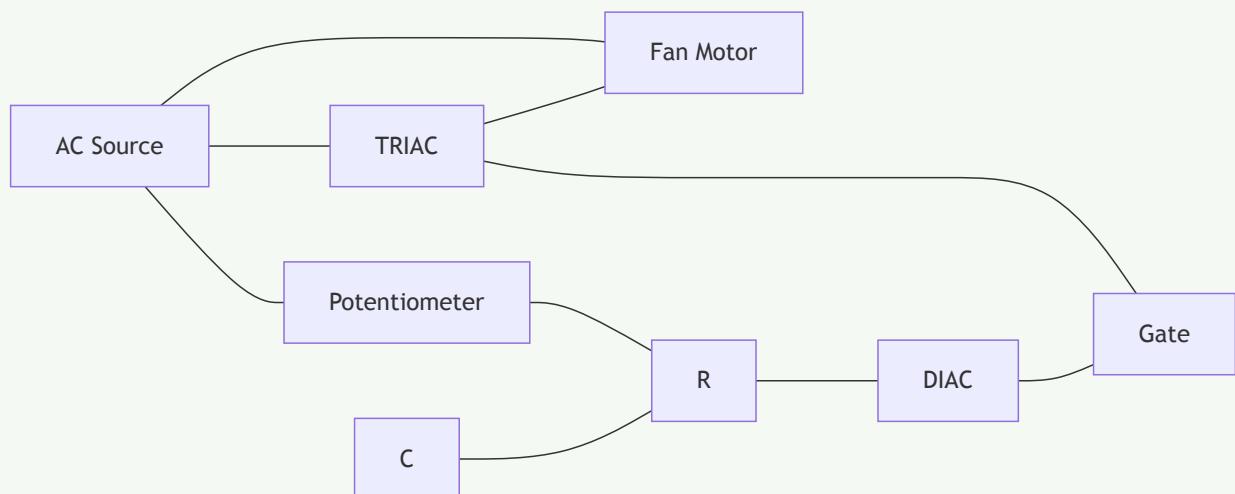
## Question 3(c) [7 marks]

Explain how TRIAC can be used as fan regulator and on-off control for ac power.

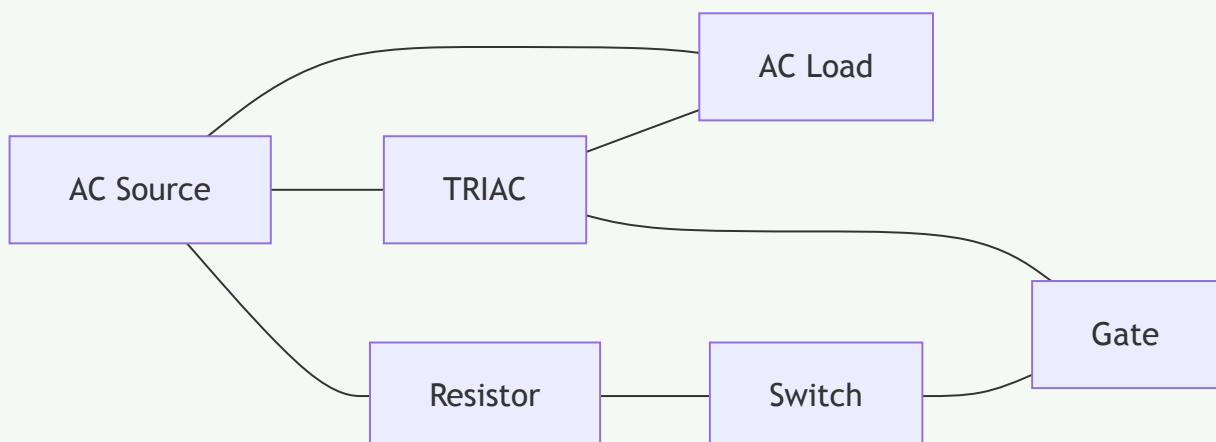
## Solution

TRIAC is a bidirectional device ideal for AC power control applications.

### TRIAC Fan Regulator Circuit:



### TRIAC On-Off Control:



- **Fan Regulation:** Phase control technique varies power to fan
- **Potentiometer:** Adjusts firing angle of TRIAC
- **On-Off Control:** Simple switch triggers TRIAC gate
- **Bidirectional:** Controls current in both half-cycles

## Mnemonic

“FPOB” (Fan Power is controlled by Phase angle in both directions)

## Question 3(a) OR [3 marks]

Draw symbol of SCR, DIAC and TRIAC.

## Solution

### Symbols of Thyristors:

1	SCR	DIAC	TRIAC
2			
3	A		
4			
5			
6			
7			
8			



### Mnemonic

“SDT” (SCR has gate on one side, DIAC has none, TRIAC has gate in middle)

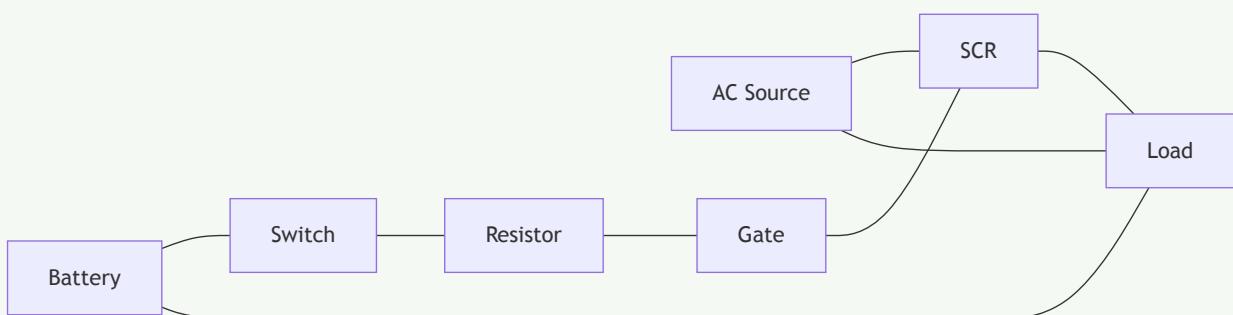
### Question 3(b) OR [4 marks]

Draw and explain Gate triggering of SCR.

#### Solution

Gate triggering is the most common method to turn on an SCR.

**Circuit Diagram:**



- **Principle:** Applying positive voltage between gate and cathode
- **Current requirement:** Small gate current triggers much larger anode current
- **Latching:** Once triggered, SCR remains ON even if gate signal is removed
- **Turn-off:** Requires reducing anode current below holding current

### Mnemonic

“GPLT” (Gate Pulse Latches Thyristor)

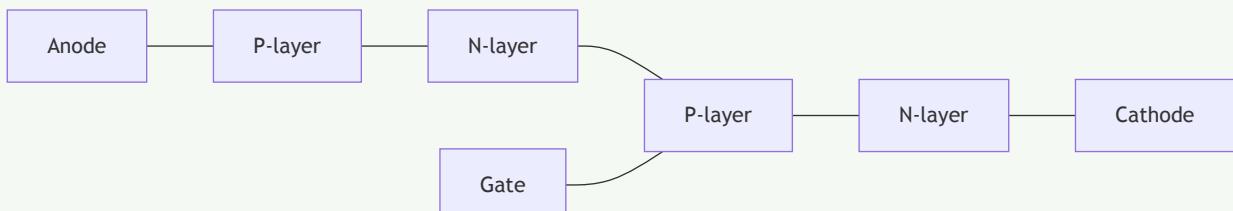
### Question 3(c) OR [7 marks]

Draw Construction and Voltage Vs Current characteristic of SCR and explain V-I characteristic.

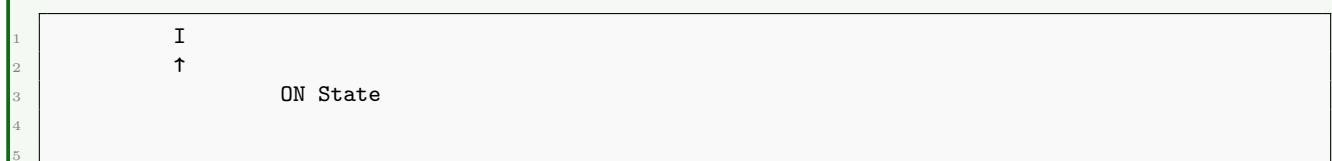
#### Solution

SCR (Silicon Controlled Rectifier) is a four-layer PNPN semiconductor device.

**SCR Construction:**



**V-I Characteristic:**



```

6 Holding
7 current
8
9
0 Forward
1 breakover
2 voltage
3
4 \rightarrow V
5 Reverse
6 breakdown
7 voltage

```

- **Forward blocking region:** SCR conducts minimal current until breakdown voltage
- **Forward conduction region:** Low resistance state after triggering
- **Reverse blocking region:** Blocks current in reverse direction
- **Gate triggering:** Reduces breakdown voltage, facilitating turn-on

### Mnemonic

“FBRH” (Forward Blocking, Reverse blocking, Holding current)

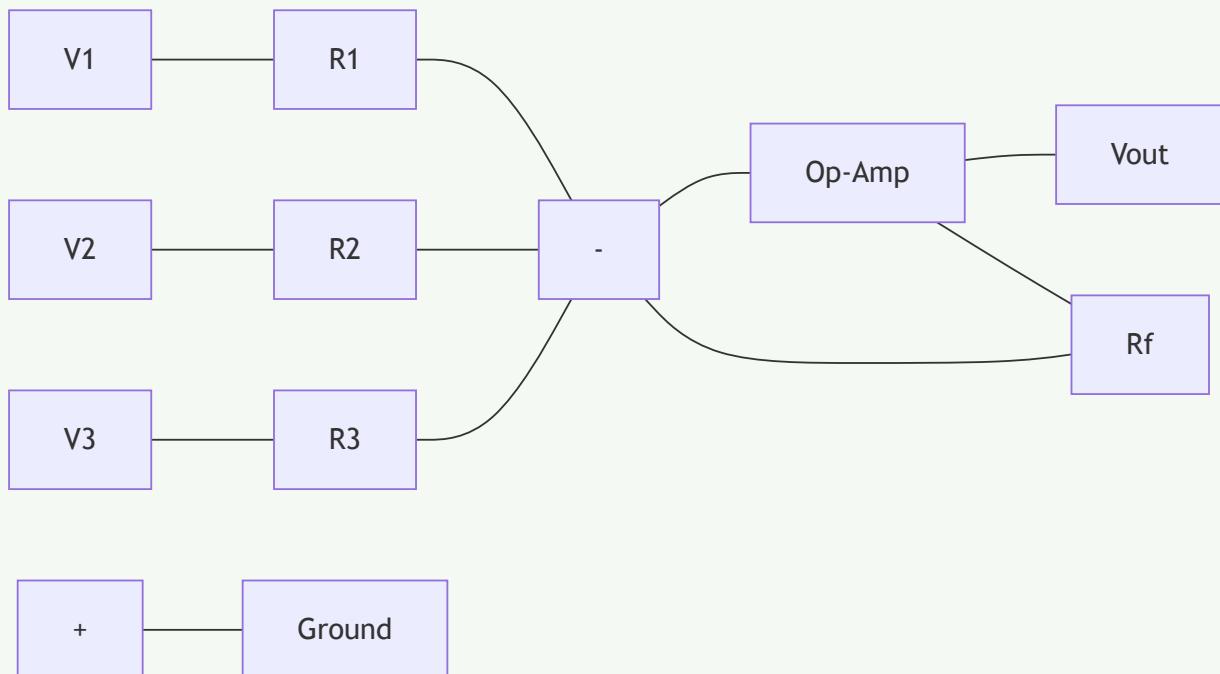
### Question 4(a) [3 marks]

Explain OP-AMP as a summing amplifier.

### Solution

Summing amplifier adds multiple input signals with weighted gains.

**Circuit Diagram:**



- **Function:** Outputs weighted sum of input voltages
- **Output equation:**  $V_{out} = -(V_1/R_1 + V_2/R_2 + V_3/R_3)$
- **Equal weights:** When  $R_1 = R_2 = R_3$ , output is simple sum multiplied by  $-R_f/R$
- **Virtual ground:** Inverting input maintains 0V potential

### Mnemonic

“SWAP” (Sum Weighted And Proportional)

## Question 4(b) [4 marks]

Define the following OP-AMP parameters: 1. input bias current 2. CMRR

### Solution

**Input Bias Current:** The average of the currents flowing into the two input terminals of an op-amp when the output is at zero.

**CMRR (Common Mode Rejection Ratio):** The ratio of differential gain to common-mode gain, indicating how well an op-amp rejects signals common to both inputs.

Table 4: Op-Amp Parameters

Parameter	Typical Value	Importance
Input Bias Current	20-200 nA	Lower is better for high impedance circuits
CMRR	80-120 dB	Higher is better for noise rejection

### Mnemonic

“BIC-CMR” (Bias Is Current, Common Mode Rejection)

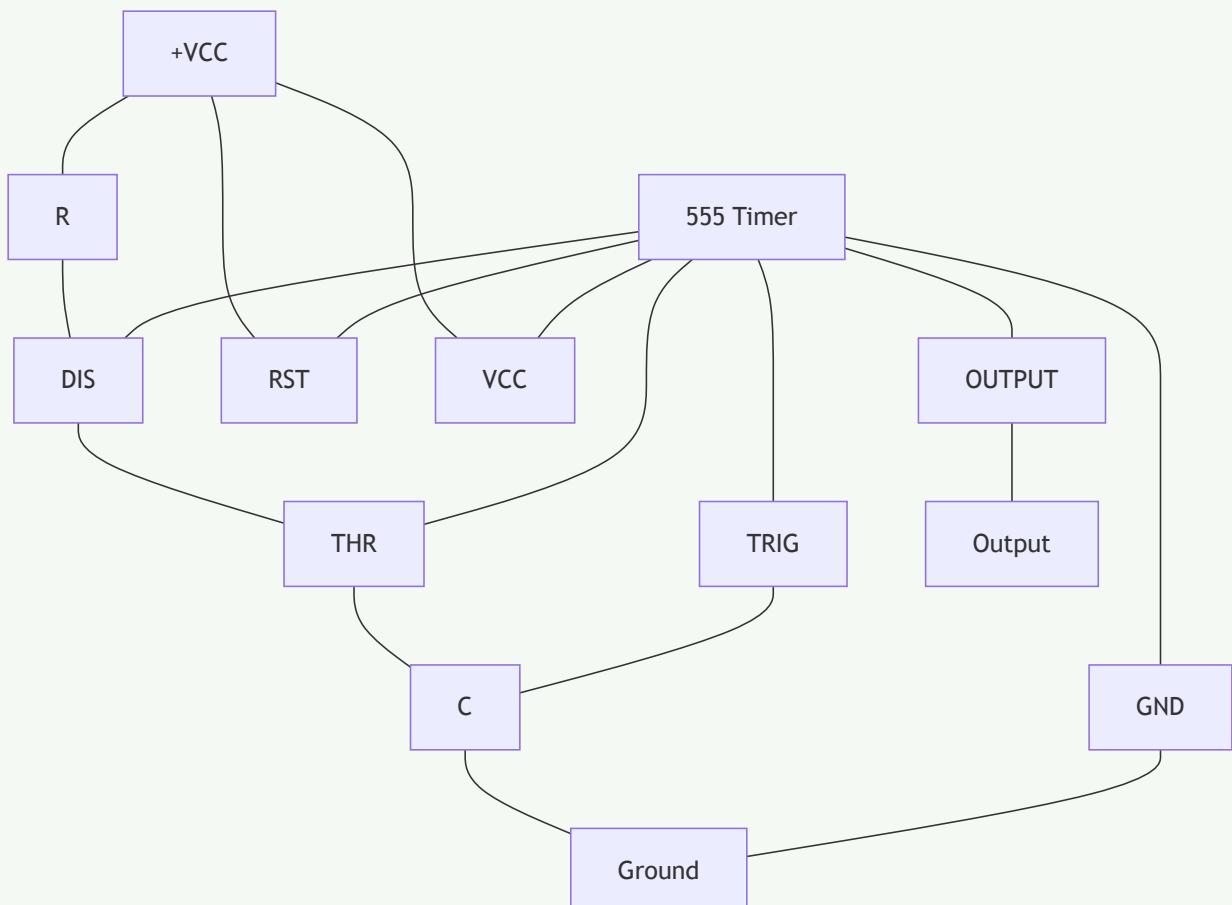
## Question 4(c) [7 marks]

Draw and explain monostable multivibrator using 555 Timer.

### Solution

Monostable multivibrator generates a single pulse of predetermined duration when triggered.

**Circuit Diagram:**



**Output Waveform:**

```

1 Trigger   -----
2           -----
3
4 Output    -----
5
6          T = 1.1RC

```

- **Operation:** Single stable state (output LOW), temporarily HIGH when triggered
- **Pulse width:**  $T = 1.1 \times R \times C$  (seconds)
- **Triggering:** Falling edge on TRIG pin (pin 2)
- **Timing components:** R and C determine pulse duration

### Mnemonic

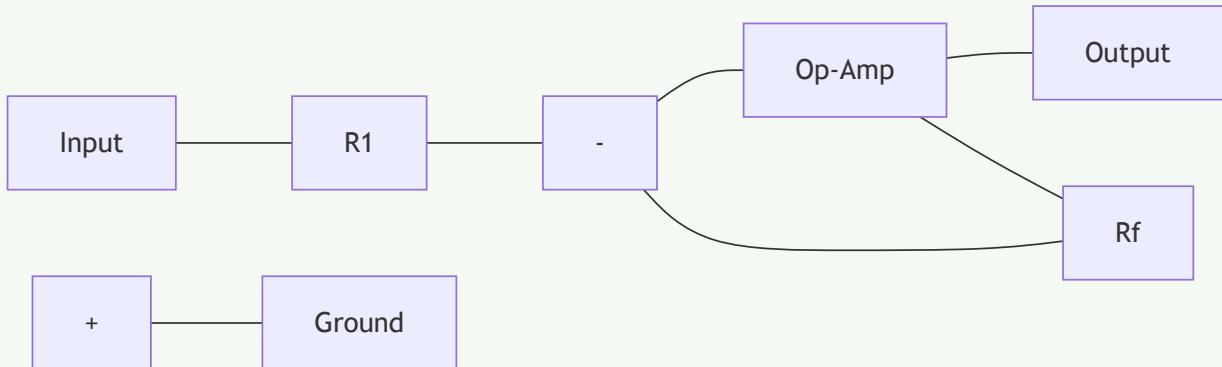
“POST” (Pulse Output, Single Trigger)

## Question 4(a) OR [3 marks]

Draw the circuit diagram of OP-AMP as a inverting amplifier.

### Solution

#### Inverting Amplifier Circuit:



### Mnemonic

“IRON” (Inverting Requires One Negative input)

## Question 4(b) OR [4 marks]

Define the following OP-AMP parameters: 1. input offset current 2. slew rate

### Solution

**Input Offset Current:** The difference between the currents flowing into the two input terminals of an op-amp.

**Slew Rate:** The maximum rate of change of output voltage per unit of time, typically measured in V/ s.

Table 5: Op-Amp Parameters

Parameter	Typical Value	Importance
Input Offset Current	2-50 nA	Lower is better for precision applications
Slew Rate	0.5-20 V/ s	Higher is better for high-frequency operation

### Mnemonic

“IOSR” (Input Offset and Slew Rate)

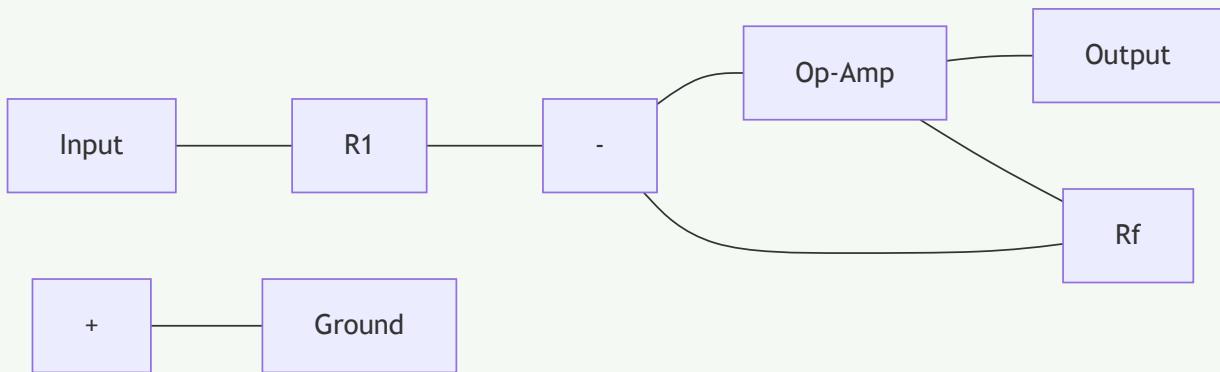
### Question 4(c) OR [7 marks]

Explain op-amp as Inverting amplifier and obtain equation of its Voltage gain.

#### Solution

Inverting amplifier produces an output signal that is inverted and amplified.

Circuit Diagram:



#### Voltage Gain Derivation:

```
1 At node N (inverting input):  
2 I1 + If = 0 (By Kirchhoff's Current Law)  
3 (Vin - VN)/R1 + (Vout - VN)/Rf = 0  
4  
5 Since VN \approx 0 (virtual ground):  
6 Vin/R1 + Vout/Rf = 0  
7 Vout/Vin = -Rf/R1
```

- **Gain equation:**  $V_{out}/V_{in} = -R_f/R_1$
- **Virtual ground:** Inverting terminal maintained at 0V
- **Input impedance:** Equal to  $R_1$
- **Negative feedback:** Provides stability and linearity

#### Mnemonic

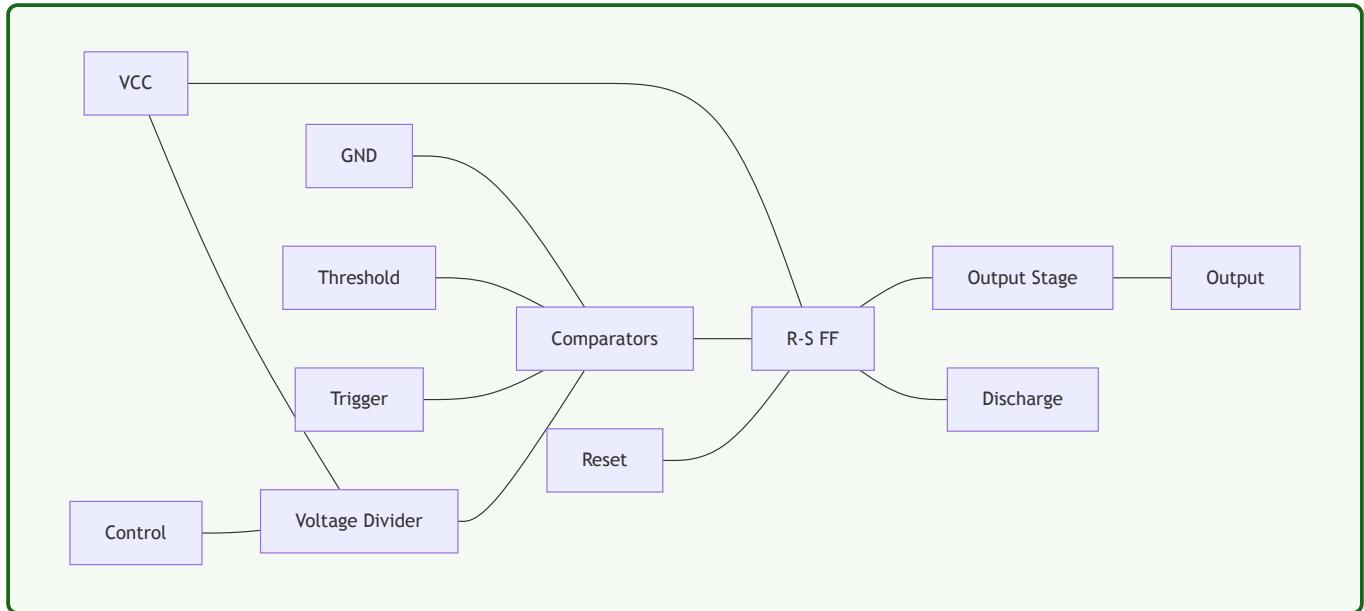
“GIVN” (Gain Is Negative, Virtual ground)

### Question 5(a) [3 marks]

Draw the block diagram of IC 555.

#### Solution

Block Diagram of IC 555:



### Mnemonic

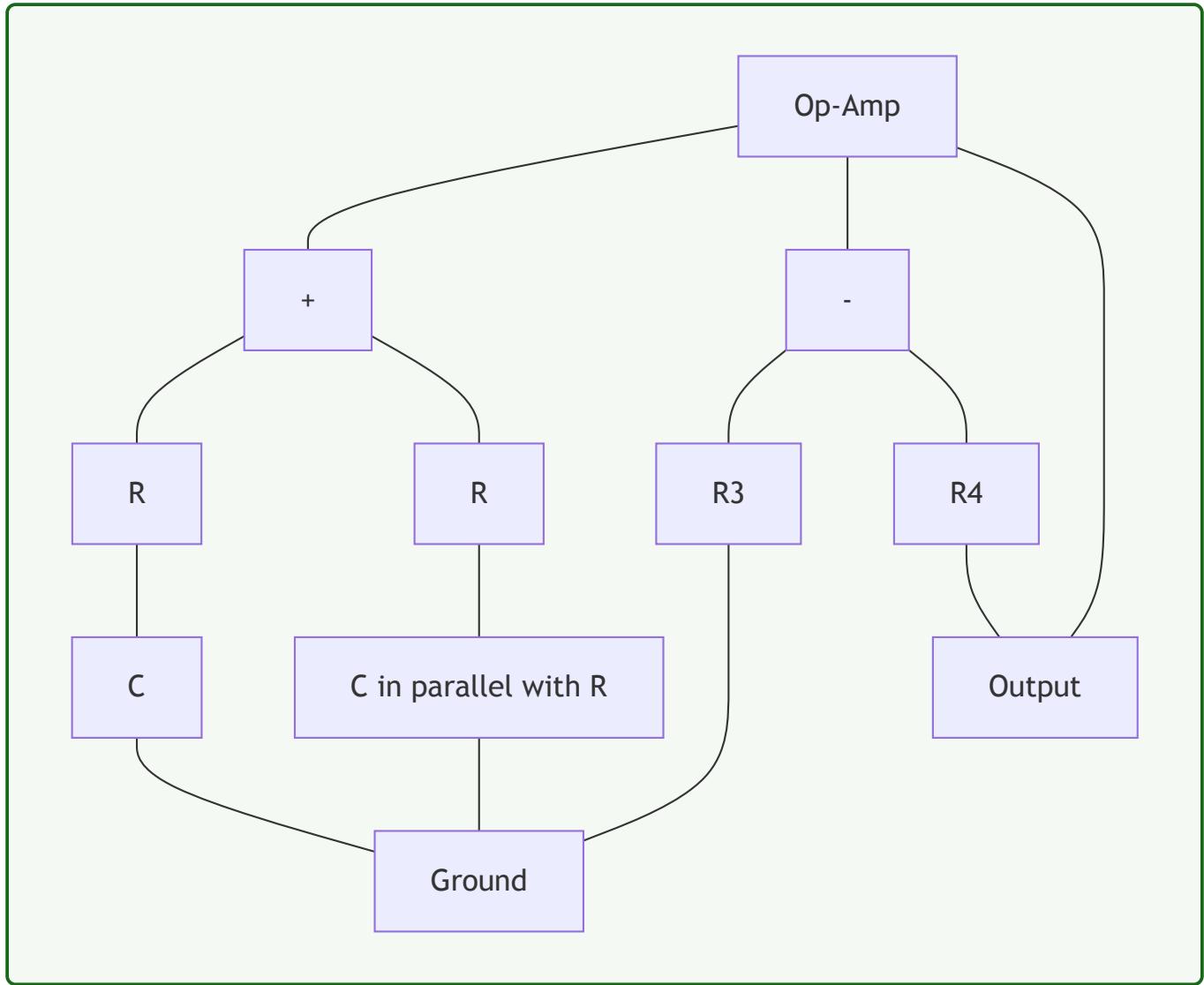
“CVOT” (Comparators, Voltage divider, Output stage, Timer)

### Question 5(b) [4 marks]

Draw the circuit diagram of OP-AMP as a wein bridge oscillator.

### Solution

Wein Bridge Oscillator Circuit:



### Mnemonic

“WPRC” (Wein Produces Resonant Circuit)

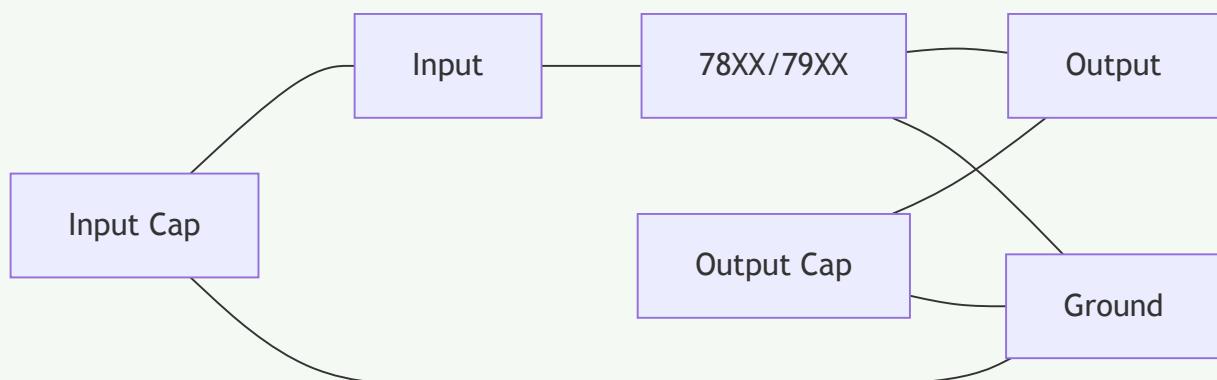
### Question 5(c) [7 marks]

Explain working of different types of Fixed and variable voltage regulator IC.

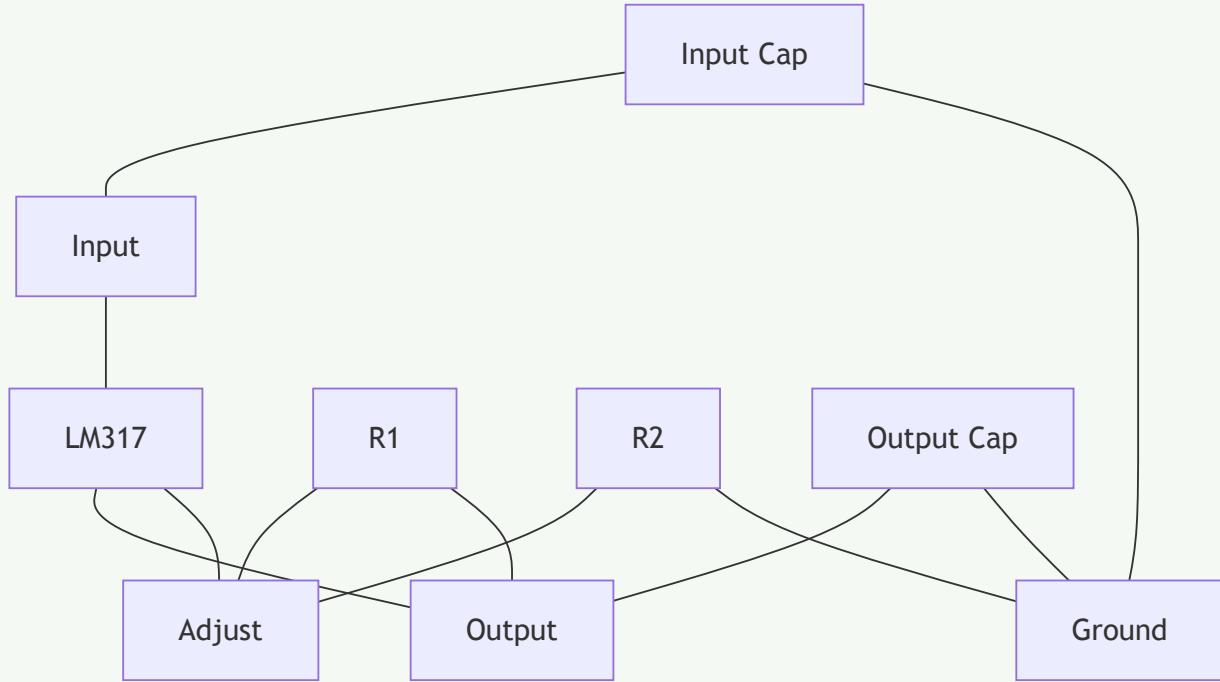
### Solution

Voltage regulator ICs maintain stable output voltage despite input or load variations.

#### Fixed Voltage Regulators:



### Variable Voltage Regulator:



- **Fixed regulators:** 78XX (positive) and 79XX (negative) series provide specific voltages
- **Variable regulators:** LM317 (positive) and LM337 (negative) allow adjustable output
- **Three-terminal design:** Input, output, and ground/adjust terminals
- **Output equation for LM317:**  $V_{out} = 1.25V \times (1 + R_2/R_1)$
- **Protection features:** Short circuit, thermal overload, and safe area protection

### Mnemonic

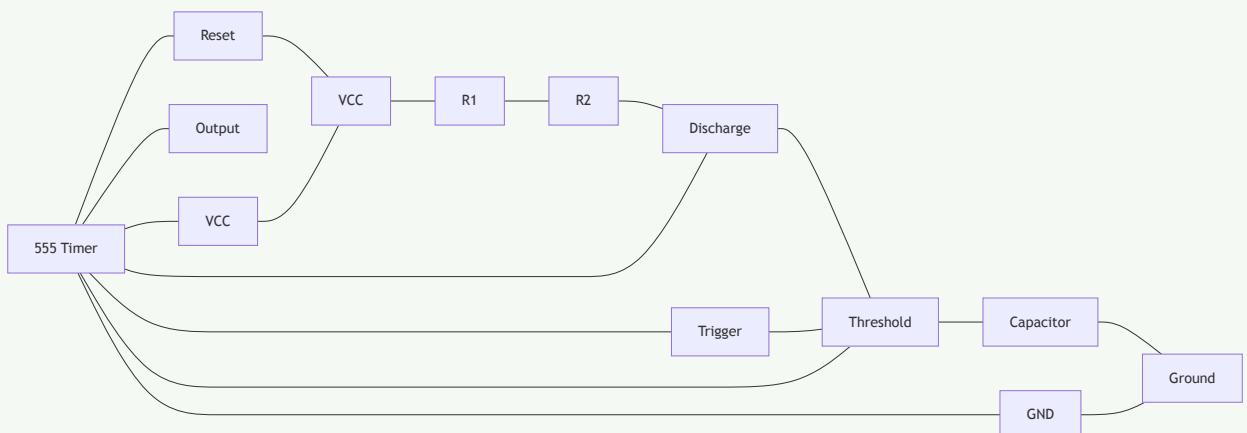
“FAVOR” (Fixed And Variable Output Regulators)

### Question 5(a) OR [3 marks]

Draw the block diagram of astable multivibrator using 555 timer.

### Solution

#### Astable Multivibrator Block Diagram:



### Mnemonic

“FOFT” (Free-running Oscillator From Timer)

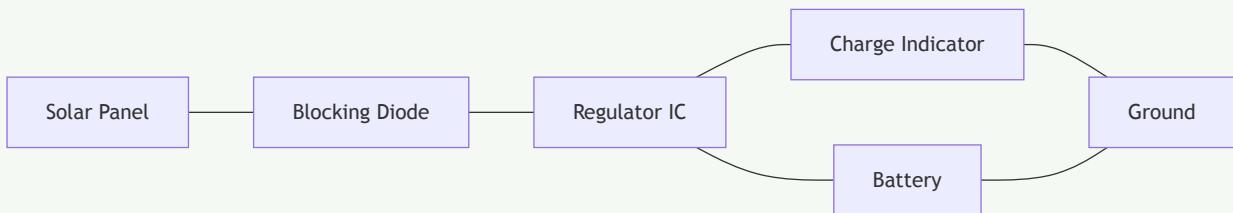
### Question 5(b) OR [4 marks]

Draw and explain solar based battery charger circuits.

#### Solution

Solar battery charger converts solar energy to charge batteries.

Circuit Diagram:



- **Solar panel:** Converts sunlight to DC electricity
- **Blocking diode:** Prevents battery discharge through panel at night
- **Regulator IC:** Controls charging voltage and current
- **Charge indicator:** Shows charging status
- **Protection:** Overcharge and reverse polarity protection

#### Mnemonic

“SBRCP” (Solar, Blocking diode, Regulator, Charging, Protection)

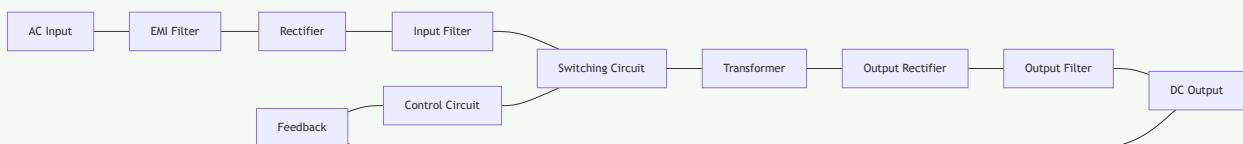
### Question 5(c) OR [7 marks]

Draw and explain the block diagram of SMPS.

#### Solution

SMPS (Switch Mode Power Supply) converts electrical power efficiently using switching regulators.

Block Diagram:



- **EMI filter:** Removes noise from AC input
- **Rectifier:** Converts AC to unregulated DC
- **Switching circuit:** Chops DC at high frequency (20-100 kHz)
- **Transformer:** Provides isolation and voltage conversion
- **Output rectifier:** Converts high-frequency AC back to DC
- **Output filter:** Smooths DC output
- **Feedback circuit:** Monitors output for regulation
- **Control circuit:** Adjusts switching based on feedback

#### Mnemonic

“ERST-FOFC” (EMI filter, Rectifier, Switching, Transformer, Feedback, Output rectifier, Filter, Control)