

# Microprocessor & Microcontroller Systems (1333202) - Winter 2024 Solution

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## Question 1(a) [3 marks]

List the features of 8051 Microcontroller.

### Solution

The 8051 microcontroller has several important features:

**Table 1.** Features of 8051

Feature	Description
<b>CPU</b>	8-bit CPU optimized for control applications
<b>Memory</b>	4KB internal ROM, 128 bytes internal RAM
<b>I/O Ports</b>	4 bidirectional 8-bit I/O ports (P0-P3)
<b>Timers</b>	Two 16-bit timer/counters (Timer 0 & Timer 1)
<b>Interrupts</b>	5 interrupt sources with 2 priority levels
<b>Serial Port</b>	Full duplex UART for serial communication

### Mnemonic

“CPU Memory Input-Output Timers Interrupts Serial (C-MIT-IS)”

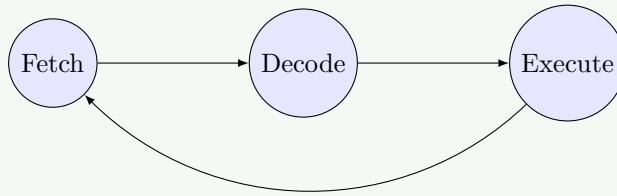
## Question 1(b) [4 marks]

Define: Opcode, Operand, Instruction cycle, Machine cycle

### Solution

**Table 2.** Definitions

Term	Definition
<b>Opcode</b>	Operation code that specifies the operation to be performed
<b>Operand</b>	Data or address on which the operation is performed
<b>Instruction Cycle</b>	Complete process of fetching, decoding and executing an instruction
<b>Machine Cycle</b>	Time required to access memory or I/O device

**Figure 1.** Instruction Cycle**Mnemonic**

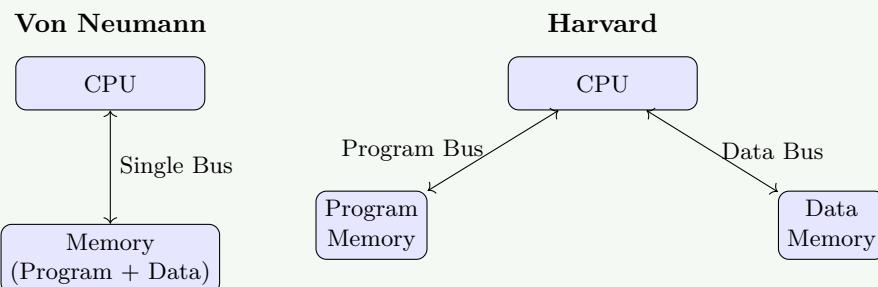
“Opcode Operand Instruction-cycle Data-cycle (OIDO)”

**Question 1(c) [7 marks]**

Compare Von Neumann and Harvard Architecture.

**Solution****Table 3.** Von Neumann vs Harvard

Parameter	Von Neumann	Harvard
<b>Memory Structure</b>	Single memory for program and data	Separate memory for program and data
<b>Bus System</b>	Single bus system	Separate bus for program and data
<b>Speed</b>	Slower due to bus conflicts	Faster simultaneous access
<b>Cost</b>	Lower cost	Higher cost
<b>Complexity</b>	Simple design	Complex design
<b>Examples</b>	8085, x86 processors	8051, DSP processors

**Figure 2.** Architecture Comparison**Mnemonic**

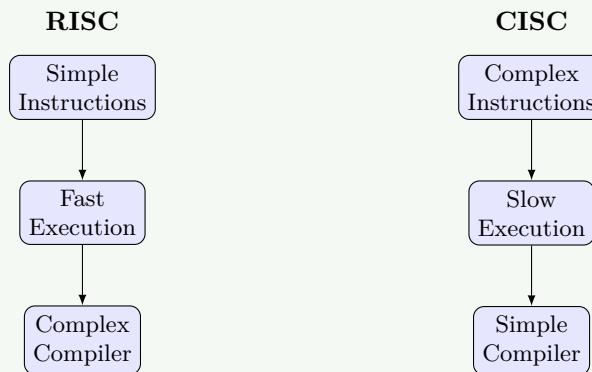
“Von-Single-Bus-Simple-Cheap vs Harvard-Separate-Dual-Fast-Complex (VSBSC vs HSDFC)”

**Question 1(c) OR [7 marks]**

Compare RISC and CISC.

**Solution****Table 4.** RISC vs CISC

Parameter	RISC	CISC
<b>Instruction Set</b>	Reduced, simple instructions	Complex instruction set
<b>Instruction Size</b>	Fixed size instructions	Variable size instructions
<b>Execution Time</b>	Single clock cycle per instruction	Multiple clock cycles
<b>Memory Access</b>	Load/Store architecture	Memory-to-memory operations
<b>Compiler</b>	Complex compiler required	Simple compiler
<b>Examples</b>	ARM, MIPS	8085, x86

**Figure 3.** RISC vs CISC Concepts**Mnemonic**

“Simple-Fast-Complex vs Complex-Slow-Simple (RISC-SFS vs CISC-CSS)”

**Question 2(a) [3 marks]**

List the 16-bit Registers available in 8085 and Explain its Function.

**Solution****Table 5.** 16-bit Registers of 8085

Register	Function
<b>PC (Program Counter)</b>	Points to next instruction address. Automatically increments after each instruction fetch.
<b>SP (Stack Pointer)</b>	Points to top of stack in memory. Decrements during PUSH, increments during POP operations.
<b>BC, DE, HL</b>	General purpose register pairs for 16-bit data storage or addresses.

**Mnemonic**

“Program-Counter Stack-Pointer BC-DE-HL (PC SP BDH)”

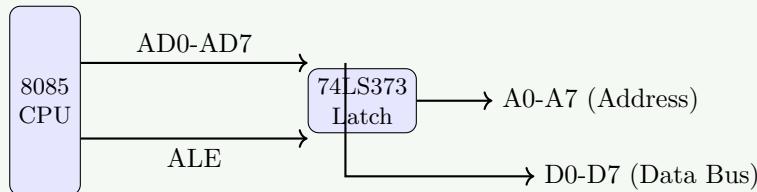
**Question 2(b) [4 marks]**

Explain Address and Data Bus De-multiplexing in 8085.

### Solution

De-multiplexing separates address and data signals from AD0-AD7 pins using ALE signal.

- **ALE:** Address Latch Enable signal controls the process.
- **T1 state:** AD0-AD7 contains lower 8-bit address. ALE goes HIGH.
- **Latch:** Address is latched in external latch (74LS373) when ALE is High.
- **T2-T3 states:** AD0-AD7 becomes data bus.



**Figure 4.** Address/Data Demultiplexing

### Mnemonic

“ALE Latches Address Low”

## Question 2(c) [7 marks]

Explain Pin Diagram of 8085 with neat sketch.

### Solution

The 8085 is a 40-pin microprocessor.

**Table 6.** Pin Functions

Pin Group	Function
<b>AD0-AD7</b>	Multiplexed Address/Data bus (Lower 8-bit)
<b>A8-A15</b>	Higher order Address bus
<b>ALE</b>	Address Latch Enable signal
<b>RD, WR</b>	Read and Write control signals
<b>IO/M</b>	I/O or Memory operation indicator
<b>S0, S1</b>	Status signals

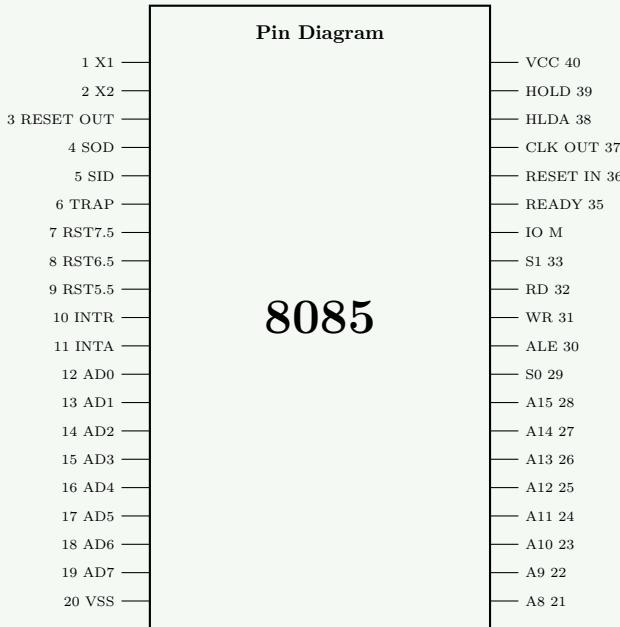


Figure 5. 8085 Pin Diagram

**Mnemonic**

“Address Data Control Power Interrupt (ADCPI)”

**Question 2(a) OR [3 marks]**

Explain Instruction Fetching Operation in 8085.

**Solution**

Instruction fetching is the first step in instruction cycle:

- **PC contents** placed on address bus (A0-A15).
- **ALE signal** goes high to latch address.
- **RD signal** goes low to read memory.
- **Instruction** fetched from memory to data bus.
- **PC incremented** to point to next instruction.

This occurs during **T1 and T2** states and takes **4 clock cycles** for simple instructions.

**Mnemonic**

“PC ALE RD Fetch Increment (PARFI)”

**Question 2(b) OR [4 marks]**

Explain Flag Register of 8085.

**Solution**

The Flag Register stores status information after arithmetic/logical operations.

Table 7. 8085 Flags

Bit	Flag	Function
D7	S (Sign)	Set if result is negative
D6	Z (Zero)	Set if result is zero
D4	AC (Aux Carry)	Set if carry from bit 3 to 4
D2	P (Parity)	Set if result has even parity
D0	CY (Carry)	Set if carry/borrow generated

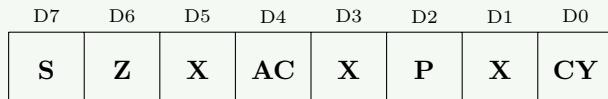


Figure 6. Flag Register Format

**Mnemonic**

“S-Z-X-AC-X-P-X-CY”

**Question 2(c) OR [7 marks]**

Explain Architecture of 8085 with neat sketch.

**Solution**

The 8085 architecture consists of ALU, Registers, Control Unit, and Buses.

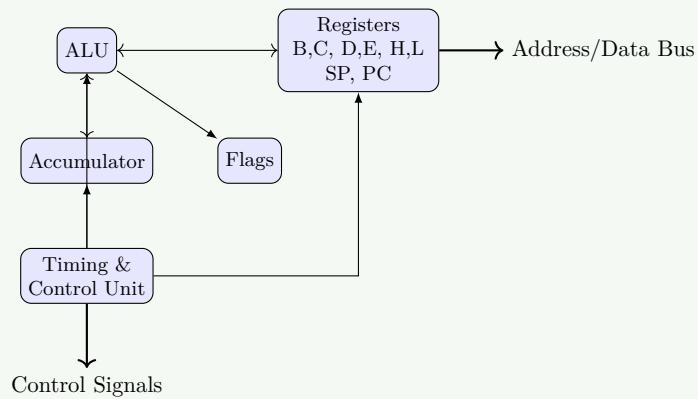


Figure 7. 8085 Architecture

- **ALU:** Performs arithmetic and logical operations.
- **Registers:** Store data (A, B, C...) and addresses (PC, SP) temporarily.
- **Control Unit:** Generates signals (RD, WR, ALE) for operation.
- **Buses:** Address (16-bit) and Data (8-bit) buses for communication.

**Mnemonic**

“ALU Registers Control Address Data (ARCAD)”

**Question 3(a) [3 marks]**

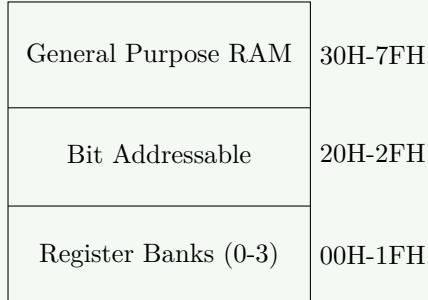
Explain Internal RAM Organization of 8051 Microcontroller.

### Solution

The 8051 has 128 bytes of internal RAM organized as:

**Table 8.** RAM Organization

Address	Purpose
<b>00H-1FH</b>	Register Banks (4 banks of 8 registers each)
<b>20H-2FH</b>	Bit Addressable Area (16 bytes)
<b>30H-7FH</b>	General Purpose RAM (80 bytes)



**Figure 8.** Internal RAM Map

### Mnemonic

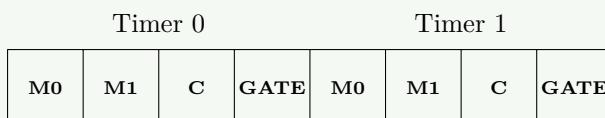
“Register Bit General (RBG)”

## Question 3(b) [4 marks]

Explain Function of Each bit of TMOD SFR of 8051 Microcontroller.

### Solution

TMOD (Timer Mode) register controls Timer 0 and Timer 1.



**Figure 9.** TMOD Register

- **GATE:** 1 = External gate control (INTx pin), 0 = Internal control.
- **C/T:** 1 = Counter mode, 0 = Timer mode.
- **M1, M0:** Mode selection (00: 13-bit, 01: 16-bit, 10: 8-bit auto-reload, 11: Split).

### Mnemonic

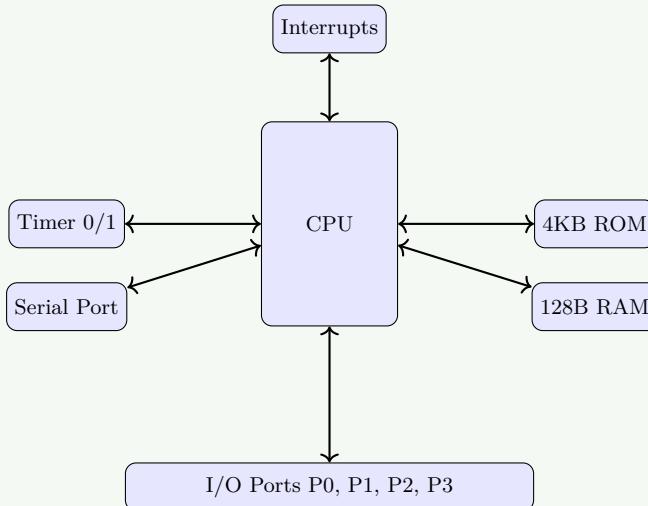
“GATE C/T Mode1 Mode0”

## Question 3(c) [7 marks]

Explain Architecture of 8051 with neat sketch.

### Solution

The 8051 has Harvard architecture with separate program and data memory.



**Figure 10.** 8051 Architecture

- **Memory:** 4KB ROM (Program), 128B RAM (Data).
- **Peripherals:** 4 I/O Ports, 2 Timers, 1 Serial Port.
- **Interrupts:** 5 Sources (External, Timer, Serial).

### Mnemonic

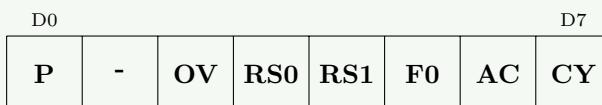
“CPU ROM RAM Ports Timers Serial Interrupts (CRRRPTI)”

## Question 3(a) OR [3 marks]

Explain PSW SFR of 8051 Microcontroller.

### Solution

PSW (Program Status Word) contains status flags.



**Figure 11.** PSW Register

- CY: Carry Flag. AC: Aux Carry.
- RS1, RS0: Register Bank Select (00-Bank0, 01-Bank1, 10-Bank2, 11-Bank3).
- OV: Overflow Flag. P: Parity Flag.

### Mnemonic

“CY AC F0 RS1 RS0 OV - P”

## Question 3(b) OR [4 marks]

Explain Function of Each bit of SCON SFR of 8051 Microcontroller.

### Solution

SCON controls serial communication.

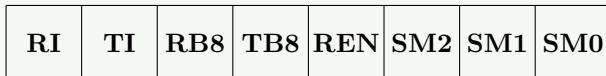


Figure 12. SCON Register

- **SM0, SM1:** Mode selection (0-Shi.Reg, 1-8bit UART, 2-9bit Fixed, 3-9bit Var).
- **REN:** Receive Enable.
- **TB8/RB8:** 9th bit for transmit/receive.
- **TI/RI:** Transmit/Receive Interrupt flags.

### Mnemonic

“SM0 SM1 SM2 REN TB8 RB8 TI RI”

## Question 3(c) OR [7 marks]

Explain Pin Diagram of 8051 with neat sketch.

### Solution

The 8051 is a 40-pin DIP package.

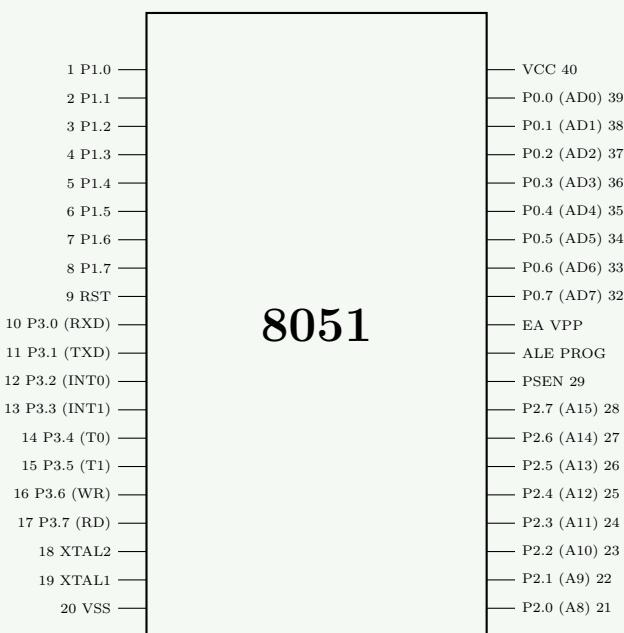


Figure 13. 8051 Pin Diagram

- **Port 0:** Multiplexed AD0-AD7. **Port 2:** High Address A8-A15.
- **Port 1:** I/O only. **Port 3:** Special functions (RX, TX, INT, T0, T1, WR, RD).
- **Control:** RST, ALE, PSEN, EA.

### Mnemonic

“Port Power Crystal Control (PPCC)”

## Question 4(a) [3 marks]

Write and Explain any Three Data Transfer Instructions of 8051 Microcontroller.

### Solution

**Table 9.** Data Transfer Instructions

Instruction	Function
MOV A, R0	Move contents of R0 to Accumulator.
MOV R1, #50H	Move immediate data 50H to R1.
MOV 30H, A	Move Accumulator contents to direct address 30H.

**Listing 1.** Data Transfer Examples

```

1 MOV A, R0      ; A = R0
2 MOV R1, #50H    ; R1 = 50H
3 MOV 30H, A      ; [30H] = A

```

### Mnemonic

“MOV Between Register Immediate Direct”

## Question 4(b) [4 marks]

Write 8051 Assembly Language Program to Multiply Content of R0 and R1 and Store Result in R5 (Lower Byte) and R6 (Higher Byte).

### Solution

**Listing 2.** Multiplication Program

```

1 ORG 0000H
2
3 MOV A, R0      ; Load Multiplicand
4 MOV B, R1      ; Load Multiplier
5 MUL AB        ; Multiply A * B
6             ; Result: B(High) A(Low)
7
8 MOV R5, A      ; Store Lower Byte
9 MOV R6, B      ; Store Higher Byte
10
11 SJMP $         ; Stop
12 END

```

## Question 4(c) [7 marks]

List Addressing Modes of 8051 Microcontroller and Explain each with Example.

**Solution****Table 10.** Addressing Modes

Mode	Description	Example
<b>Immediate</b>	Data directly in instruction (#).	MOV A, #50H
<b>Register</b>	Data in register (Rn).	MOV A, R0
<b>Direct</b>	Data at direct memory address.	MOV A, 30H
<b>Indirect</b>	Address in register (@Ri).	MOV A, @R0
<b>Indexed</b>	Base + Offset (usually for ROM).	MOVC A, @A+DPTR
<b>Relative</b>	Offset added to PC (Jumps).	SJMP LABEL
<b>Bit</b>	Direct bit address.	SETB P1.0

**Mnemonic**

“Immediate Register Direct Indirect Indexed Relative Bit (I-R-D-I-I-R-B)”

**Question 4(a) OR [3 marks]**

Write and Explain any Three Logical Instructions 8051 Microcontroller.

**Solution****Table 11.** Logical Instructions

Instruction	Function
ANL A, R0	AND Accumulator with R0. Masking bits.
ORL A, #0FH	OR Accumulator with immediate OFH. Setting bits.
XRL A, 30H	XOR Accumulator with memory. Toggling bits.

**Listing 3.** Logical Examples

```

1 ANL A, R0      ; A = A AND R0
2 ORL A, #0FH    ; A = A OR OFH
3 XRL A, 30H     ; A = A XOR [30H]

```

**Question 4(b) OR [4 marks]**

Write 8051 Assembly Language Program to Subtract Number Stored in 2000h from 2001h and Store result in 2002h. (External Memory).

**Solution****Listing 4.** Subtraction Program

```

1 ORG 0000H
2
3 MOV DPTR, #2001H    ; Point to Minuend
4 MOVX A, @DPTR       ; Load Minuend
5 MOV R0, A            ; Save in R0
6

```

```

7   MOV DPTR, #2000H ; Point to Subtrahend
8   MOVX A, @DPTR    ; Load Subtrahend
9   MOV R1, A         ; Save in R1
10
11  MOV A, R0         ; Restore Minuend
12  CLR C            ; Clear Carry for SUBB
13  SUBB A, R1       ; A = Minuend - Subtrahend
14
15  MOV DPTR, #2002H ; Point to Result
16  MOVX @DPTR, A    ; Store Result
17
18  SJMP $
19  END

```

## Question 4(c) OR [7 marks]

Explain Instructions: RET, PUSH, CLR PSW.0, RLC A, CJNE, NOP, ANL.

### Solution

**Table 12.** Instruction Explanation

Instruction	Function
RET	Return from subroutine. Pops PC from stack.
PUSH 30H	Pushes contents of address 30H onto Stack.
CLR PSW.0	Clears Carry Flag (Bit 0 of PSW).
RLC A	Rotate A Left through Carry Flag.
CJNE A, #dat, L	Compare A with data, Jump to Label if Not Equal.
NOP	No Operation. Consumes time/space only.
ANL A, #data	Logical AND Accumulator with immediate data.

### Mnemonic

“Return Push Clear Rotate Compare No-op AND”

## Question 5(a) [3 marks]

List the application of Microcontroller in various fields.

### Solution

**Table 13.** Applications

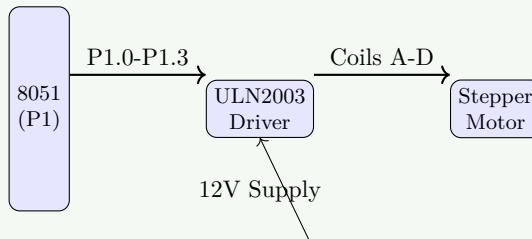
Field	Applications
Consumer	TV Remotes, Washing Machines, Microwaves
Automotive	ABS, Engine Control, Airbags
Industrial	Robotics, Process Control, Automation
Medical	Pacemakers, Glucose Meters
Communication	Mobile Phones, Modems
Home	Smart Thermostats, Security Systems

## Question 5(b) [4 marks]

Interface Stepper Motor with 8051 Microcontroller and Explain in brief.

### Solution

Stepper motor requires a driver like ULN2003 for current amplification.



**Figure 14.** Stepper Motor Interface

**Table 14.** Half-Step Sequence

Step	P1.3	P1.2	P1.1	P1.0	Hex
1	0	0	0	1	01H
2	0	0	1	1	03H
3	0	0	1	0	02H
4	0	1	1	0	06H

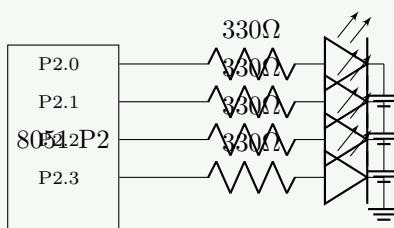
### Mnemonic

“Step Sequence Driver Protection (SSDP)”

## Question 5(c) [7 marks]

Draw interfacing circuit to interface 4 LED at port 2.0 to 2.3 of microcontroller 8051 and write assembly language program to flash it.

### Solution



**Figure 15.** 4 LED Interface

**Listing 5.** LED Flashing Program

```

1   ORG 0000H
2   MAIN:
3     MOV P2, #0FH      ; Turn ON LEDs (P2.0-P2.3 = 1)
4     ACALL DELAY
5     MOV P2, #00H      ; Turn OFF LEDs
6     ACALL DELAY
7     SJMP MAIN
  
```

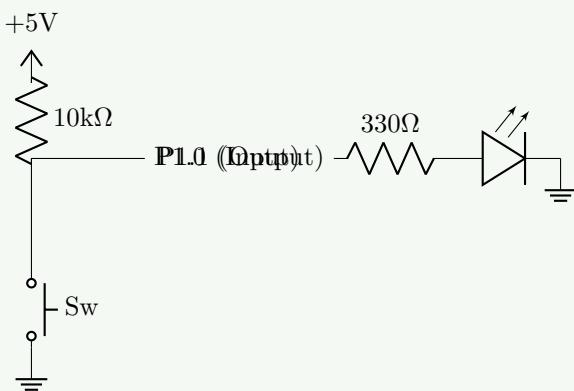
```

8   DELAY:
9     MOV R0, #255
10    L1: MOV R1, #255
11    L2: DJNZ R1, L2
12    DJNZ R0, L1
13    RET
14
15   END

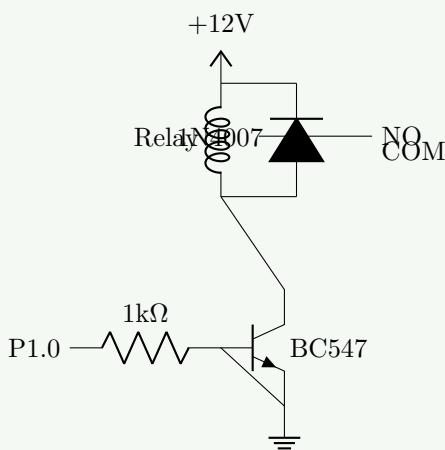
```

**Mnemonic****“Resistor LED Ground Program (RLGP)”****Question 5(a) OR [3 marks]****Draw Interfacing of Push button switch and LED with 8051 Microcontroller.****Solution**

Switch at P1.0 (Input), LED at P1.1 (Output).

**Figure 16.** Switch and LED Interface**Mnemonic****“Pull-up Switch LED Current-limit (PSLC)”****Question 5(b) OR [4 marks]****Interface Relay with 8051 Microcontroller and Explain in brief.****Solution**

Relay is an electromechanical switch. It isolates high voltage load from microcontroller.

**Figure 17.** Relay Driver Circuit

- **Transistor:** Acts as switch.  $P1.0=1 \rightarrow$  Transistor ON  $\rightarrow$  Relay ON.
- **Flyback Diode:** Protects transistor from back EMF.
- **Isolation:** High voltage AC load is isolated from 5V logic.

**Mnemonic**

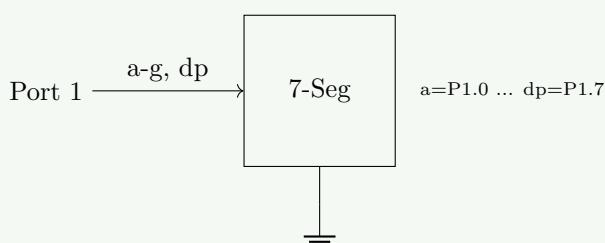
“Transistor Resistor Diode Relay (TRDR)”

**Question 5(c) OR [7 marks]**

Interface 7 segment LED with 8051 Microcontroller and write assembly language program to print 0 on it.

**Solution**

Common Cathode display connected to Port 1.

**Figure 18.** 7-Segment Connection**Table 15.** Digit 0 Code

Digit	Segments (gfedcba)	Hex
0	0 1 1 1 1 1 1	3FH

**Listing 6.** Display 0

```

1  ORG 0000H
2  MAIN:
3      MOV P1, #3FH          ; Pattern for '0'
4      SJMP MAIN            ; Loop
5      END

```

**Mnemonic**

“Seven Segments Common Cathode Current-limit (SSCCC)”