

Subject Name Solutions

4311102 – Winter 2023

Semester 1 Study Material

Detailed Solutions and Explanations

Question 1(a) [3 marks]

Define Forward and reverse bias of diode.

Solution

Forward Bias of Diode:

- **Connection Method:** P-type connected to positive terminal and N-type connected to negative terminal of battery
- **Barrier Width:** Barrier width decreases
- **Resistance:** Low resistance (typically 100-1000Ω)
- **Current Flow:** Allows current to flow easily through the diode

Reverse Bias of Diode:

- **Connection Method:** P-type connected to negative terminal and N-type connected to positive terminal
- **Barrier Width:** Barrier width increases
- **Resistance:** Very high resistance (typically several MΩ)
- **Current Flow:** Blocks current flow (only small leakage current flows)

Diagram:

Mermaid Diagram (Code)

```
{Shaded}  
{Highlighting} []  
graph TD  
    A[Forward Bias] --> B[P connected to +ve]  
    B --> C[Current flows easily]  
    D[Reverse Bias] --> E[P connected to -ve]  
    E --> F[Current blocked]  
{Highlighting}  
{Shaded}
```

Mnemonic

“PFNR” - “Positive to P Forward, Negative to P Reverse”

Question 1(b) [4 marks]

Explain construction and working of LDR.

Solution

Construction of LDR:

- **Material:** Made of semiconductor material (Cadmium Sulfide)
- **Pattern:** Zigzag pattern of photosensitive material on ceramic base
- **Electrodes:** Metal electrodes at both ends
- **Package:** Encapsulated in transparent plastic or glass case

Working Principle:

- **Photoconductivity:** Based on photoconductivity principle
- **Dark Resistance:** High resistance (MΩ range) in dark conditions
- **Light Exposure:** When exposed to light, photons release electrons
- **Resistance Drop:** Resistance decreases (kΩ range) in bright light

Diagram:

+---{-}---{-}---{-}+
| | Zigzag pattern of

```
| +{ -/{ -}+ { -} semiconductor material}
| | |
| +{ -/{ -}+}
| | |
+{ -{-}{ -}{ -}{ -}{ -}{ -}+}
| | |
| | |
L D { { -} Leads}
```

Mnemonic

“MILD” - “More Illumination, Less Dark-resistance”

Question 1(c) [7 marks]

Explain the color band coding method of Resistor. Write color band of $47\text{k}\Omega \pm 5\%$ resistance.

Solution

Color Band Coding Method:

Color	Value	Multiplier	Tolerance
Black	0	10^0	-
Brown	1	10^1	$\pm 1\%$
Red	2	10^2	$\pm 2\%$
Orange	3	10^3	-
Yellow	4	10^4	-
Green	5	10^5	$\pm 0.5\%$
Blue	6	10^6	$\pm 0.25\%$
Violet	7	10^7	$\pm 0.1\%$
Grey	8	10^8	$\pm 0.05\%$
White	9	10^9	-
Gold	-	10^{-1}	$\pm 5\%$
Silver	-	10^{-2}	$\pm 10\%$
Colorless	-	-	$\pm 20\%$

4-Band Resistor Color Code:

- First Band: First significant digit
 - Second Band: Second significant digit
 - Third Band: Multiplier
 - Fourth Band: Tolerance

For $47k\Omega \pm 5\%$:

- First digit: 4 = Yellow
 - Second digit: 7 = Violet
 - Multiplier: 10^3 = Orange(fork)
 - Tolerance: $\pm 5\%$ = Gold

Color bands for $47\text{k}\Omega \pm 5\%$: Yellow – Violet – Orange – Gold

Diagram:

Mnemonic

“BAND” - “Beginning digits, Amplify with Multiplier, Note tolerance with last band, Decode carefully”

Question 1(c) [7 marks] (OR)

Explain Aluminum Electrolytic wet type capacitor.

Solution

Aluminum Electrolytic Wet Type Capacitor:

Construction:

- Plates: Two aluminum foils (anode and cathode)
 - Dielectric: Aluminum oxide layer on anode foil
 - Electrolyte: Liquid electrolyte (boric acid, sodium borate, etc.)
 - Separator: Paper separator soaked in electrolyte
 - Enclosure: Aluminum can with rubber seal

Working Principle:

- Oxide Layer: Thin aluminum oxide layer acts as dielectric
 - Electrolyte: Acts as cathode connection to second plate
 - Polarization: Has defined polarity (+ and -) terminals

Characteristics:

- Capacitance Range: 1 F to 47,000 F
 - Voltage Rating: 6.3V to 450V
 - Polarity: Polarized (must connect correctly)
 - Leakage Current: Higher than other capacitor types
 - ESR: Higher equivalent series resistance

Diagram:

Mermaid Diagram (Code)

```
{Shaded}  
{Highlighting}[]  
graph TD  
    A[Aluminum Electrolytic Capacitor] --- B[Aluminum Can]  
    A --- C[Anode Foil]  
    A --- D[Cathode Foil]  
    A --- E[Electrolyte]  
    A --- F[Separator]  
    A --- G[Aluminum Oxide Layer]  
    A --- H[Terminal Posts]  
{Highlighting}  
{Shaded}
```

Mnemonic

“POLE” - “Polarized, Oxide layer, Liquid electrolyte, Enormous capacitance”

Question 2(a) [3 marks]

Draw the symbol of Schottkey diode, LED and Photo-diode.

Solution

Symbols:

Key Features:

- **Schottky Diode:** Standard diode symbol with curved bar (represents metal-semiconductor junction)
- **LED:** Standard diode symbol with two arrows pointing away (represents light emission)
- **Photo-diode:** Standard diode symbol with two arrows pointing toward diode (represents light detection)

Mnemonic

“SLP” - “Schottky has curve, LED emits, Photo-diode absorbs”

Question 2(b) [4 marks]

Define Active and Passive Components with example.

Solution**Passive Components:**

Characteristic	Description	Examples
Power	Cannot generate power	Resistors, Capacitors, Inductors
Signal	Cannot amplify signals	Transformers, Diodes
Control	No control over current flow	Connectors, Switches
Energy	Store or dissipate energy	Fuses, Filters

Active Components:

Characteristic	Description	Examples
Power	Can generate power	Transistors, ICs
Signal	Can amplify signals	Op-amps, Amplifiers
Control	Control current flow	SCRs, MOSFETs
Dependency	Require external power	Voltage regulators, Microcontrollers

Diagram:

```
graph TB
    A[Electronic Components] --> B[Active Components]
    A --> C[Passive Components]
    B --> D[Transistors]
    B --> E[ICs]
    B --> F[Amplifiers]
    C --> G[Resistors]
    C --> H[Capacitors]
    C --> I[Inductors]
```

Mnemonic

“PASS-ACT” - “Passive stores or dissipates, Active controls or amplifies”

Question 2(c) [7 marks]

Explain working of full wave bridge rectifier.

Solution

Full Wave Bridge Rectifier:

Circuit Construction:

- Diodes: Four diodes arranged in bridge configuration
- Input: AC supply from transformer secondary
- Output: Pulsating DC across load resistor with filter capacitor

Working Principle:

- Positive Half Cycle: D1 and D3 conduct, D2 and D4 block
- Negative Half Cycle: D2 and D4 conduct, D1 and D3 block
- Current Flow: Always flows through load in same direction

Performance Parameters:

- Ripple Frequency: $2 \times \text{input frequency}$ (100Hz for 50Hz input)
- Efficiency: 81.2%
- PIV: $V_0(\text{max})$ per diode
- TUF: 0.812 (Transformer Utilization Factor)

Diagram:

Mermaid Diagram (Code)

```
{Shaded}  
{Highlighting} []  
graph LR  
    A[AC Input] --> B[Bridge Rectifier]  
    B --> C[D1]  
    B --> D[D2]  
    B --> E[D3]  
    B --> F[D4]  
    C --> G[Load]  
    D --> G  
    E --> G  
    F --> G  
    G --> H[Pulsating DC Output]  
    H --> I[Filter Capacitor]  
    I --> J[Smooth DC Output]  
{Highlighting}  
{Shaded}
```

Mnemonic

“BRIDGE” - “Better Rectification with Improved Diode Geometry Efficiency”

Question 2(a) [3 marks] (OR)

Explain construction and working of LED.

Solution

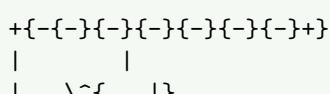
Construction of LED:

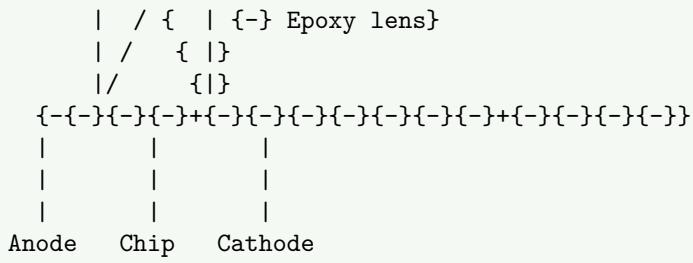
- Material: Semiconductor (GaAs, GaP, AlGaInP, etc.)
- Junction: P-N junction with heavily doped semiconductors
- Package: Encased in transparent or colored epoxy lens
- Cathode: Identified by flat side on package or shorter lead

Working Principle:

- Forward Bias: Applied to P-N junction
- Recombination: Electrons and holes recombine at junction
- Energy Release: Energy released as photons (light)
- Wavelength: Determined by band gap of semiconductor material

Diagram:





Mnemonic

“LEDS” - “Light Emits During electron-hole recombination in Semiconductor”

Question 2(b) [4 marks] (OR)

Explain composition type resistors.

Solution

Composition Resistors:

Construction:

- Core Material: Carbon particles mixed with insulating material (clay/ceramic)
- Binding: Resin binder forms solid cylindrical shape
- Terminals: Metal caps with leads attached to ends
- Protection: Coated with insulating paint or plastic

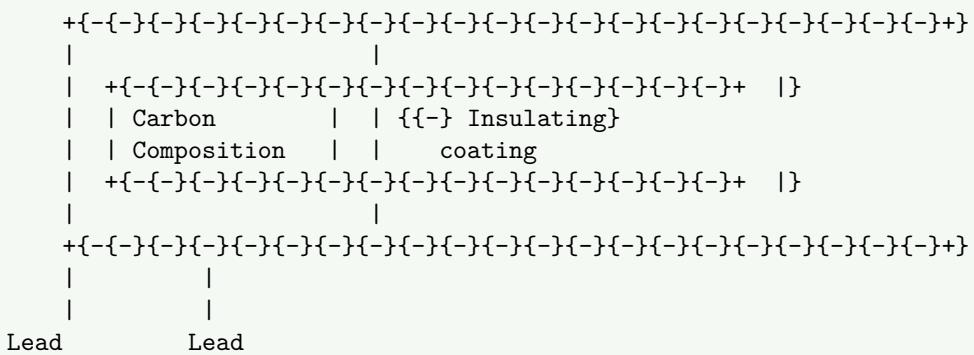
Characteristics:

- Resistance Range: 1Ω to $22M\Omega$
- Power Rating: $1/8W$ to $2W$
- Tolerance: $\pm 5\%$ to $\pm 20\%$
- Temperature Coefficient: -500 to $+500 \text{ ppm}/^\circ\text{C}$

Advantages & Limitations:

- Cost: Low cost
- Noise: Higher noise level
- Stability: Less stable with temperature
- Applications: General purpose, non-critical applications

Diagram:



Mnemonic

“CCRI” - “Carbon Composition Resistors are Inexpensive”

Question 2(c) [7 marks] (OR)

Explain working of full wave rectifier with two diodes.

Solution

Full Wave Rectifier with Two Diodes (Center-tap):

Circuit Construction:

- Transformer: Center-tapped transformer secondary
- Diodes: Two diodes connected to opposite ends of secondary
- Output: Taken between center tap and diode junction

Working Principle:

- Positive Half Cycle: Upper half of secondary positive, D1 conducts, D2 blocks
- Negative Half Cycle: Lower half of secondary positive, D2 conducts, D1 blocks
- Current Flow: Always flows through load in same direction

Performance Parameters:

- Ripple Frequency: $2 \times \text{input frequency}$ (100Hz for 50Hz input)
- Efficiency: 81.2%
- PIV: $2V_0(\text{max})$ per diode (twice the center-tap rectifier)
- TUF: 0.693 (Transformer Utilization Factor)

Diagram:

Mermaid Diagram (Code)

```
{Shaded}  
{Highlighting} []  
graph LR  
    A[AC Input] --> B[Center-Tapped Transformer]  
    B --> C[D1]  
    B --> D[D2]  
    B --> E[Ground]  
    C --> F[Load]  
    D --> F  
    F --> G[Pulsating DC Output]  
    G --> H[Filter]  
    H --> I[Smooth DC Output]  
{Highlighting}  
{Shaded}
```

Mnemonic

“CTFWR” - “Center Tap Facilitates Whole-cycle Rectification”

Question 3(a) [3 marks]

Explain working of schhotkey diode.

Solution

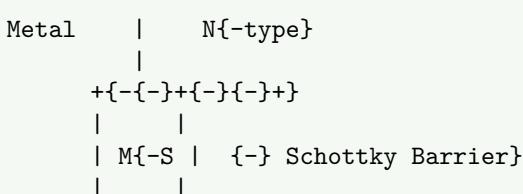
Working of Schottky Diode:

- Junction Type: Metal-Semiconductor (M-S) junction instead of P-N
- Charge Carriers: Majority carrier device (electrons in N-type)
- Barrier: Schottky barrier formed at metal-semiconductor interface
- Forward Voltage: Lower forward voltage drop (0.2-0.4V vs 0.7V for Si diode)

Key Characteristics:

- Switching Speed: Very fast switching (no minority carrier storage)
- Applications: High-frequency circuits, power supplies
- Recovery Time: Negligible reverse recovery time

Diagram:



+{-{-}{}{-}{}{-}{}{-}+}

Mnemonic

“SFAM” - “Schottky’s Fast And Metal-based”

Question 3(b) [4 marks]

Explain N type semiconductor.

Solution

N-type Semiconductor:

Formation:

- Base Material: Intrinsic semiconductor (Silicon or Germanium)
- Doping Element: Pentavalent impurity (P, As, Sb)
- Doping Process: Thermal diffusion or ion implantation
- Concentration: Typically 1 part impurity to 10^8 parts silicon

Characteristics:

- Majority Carriers: Electrons (negative charge carriers)
- Minority Carriers: Holes
- Conductivity: Higher than intrinsic semiconductor
- Fermi Level: Closer to conduction band

Diagram:

Mermaid Diagram (Code)

```
{Shaded}  
{Highlighting} []  
graph TD  
    A[N{-type Semiconductor}] --- B[Silicon Atom]  
    A --- C[Pentavalent Impurity Atom]  
    C --- D[Extra Free Electron]  
    A --- E[Majority Carriers: Electrons]  
    A --- F[Minority Carriers: Holes]  
{Highlighting}  
{Shaded}
```

Mnemonic

“PENT” - “Pentavalent Element makes N-Type with free electrons”

Question 3(c) [7 marks]

Explain construction and working of PN Junction Diode.

Solution

Construction of PN Junction Diode:

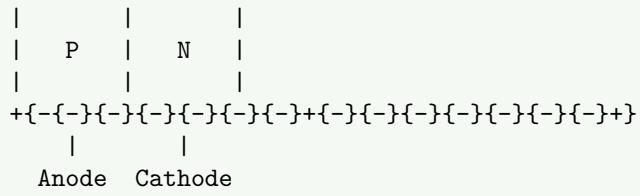
- Materials: P-type and N-type semiconductor regions
- Junction: Formed by diffusion or epitaxial growth
- Depletion Region: Forms at junction interface
- Contacts: Metal contacts attached to both regions
- Packaging: Sealed in glass, plastic, or metal case

Working Principle:

- Depletion Region: Forms due to diffusion of carriers
- Barrier Potential: Created across junction (0.7V for Si, 0.3V for Ge)
- Forward Bias: Current flows when forward voltage > barrier potential
- Reverse Bias: Only small leakage current flows until breakdown

Diagram:

+{-{-}{}{-}{}{-}{}{-}+{-}{}{-}{}{-}{}{-}+{-}+}



Depletion region at junction

Mnemonic

“BIRD” - “Barrier forms at Interface, Rectifies Direct current”

Question 3(a) [3 marks] (OR)

Explain working of photo-diode.

Solution

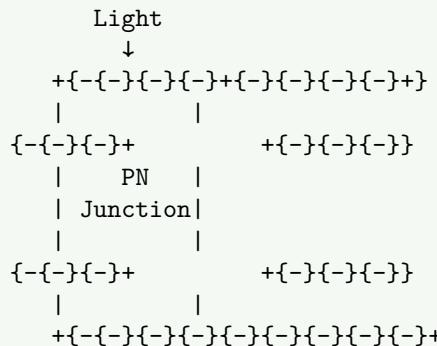
Working of Photo-diode:

- Operation Mode: Reverse biased P-N junction
- Light Absorption: Photons create electron-hole pairs in depletion region
- Carrier Generation: Light energy > band gap energy creates free carriers
- Current Flow: Photocurrent proportional to light intensity

Key Characteristics:

- Sensitivity: Depends on semiconductor material and wavelength
- Response Time: Very fast (ns range)
- Operating Modes: Photovoltaic mode or photoconductive mode
- Applications: Light sensors, optical communication

Diagram:



Mnemonic

“PLIP” - “Photons Lead to Increased Photocurrent”

Question 3(b) [4 marks] (OR)

Explain P type Semiconductor.

Solution

P-type Semiconductor:

Formation:

- Base Material: Intrinsic semiconductor (Silicon or Germanium)
- Doping Element: Trivalent impurity (B, Al, Ga)
- Doping Process: Thermal diffusion or ion implantation
- Concentration: Typically 1 part impurity to 10^8 parts silicon

Characteristics:

- Majority Carriers: Holes (positive charge carriers)

- Minority Carriers: Electrons
- Conductivity: Higher than intrinsic semiconductor
- Fermi Level: Closer to valence band

Diagram:

Mermaid Diagram (Code)

```
{Shaded}
{Highlighting} []
graph TD
    A[P{-type Semiconductor}] --> B[Silicon Atom]
    A --> C[Trivalent Impurity Atom]
    C --> D[Hole Formation]
    A --> E[Majority Carriers: Holes]
    A --> F[Minority Carriers: Electrons]
{Highlighting}
{Shaded}
```

Mnemonic

“TRIP” - “TRIvalent impurity Produces holes in P-type”

Question 3(c) [7 marks] (OR)

Compare half wave and full wave rectifier.

Solution

Comparison between Half Wave and Full Wave Rectifier:

Parameter	Half Wave Rectifier	Full Wave Rectifier
Circuit Complexity	Simple, uses 1 diode	Complex, uses 2 or 4 diodes
Output Waveform	Pulsating DC for half cycle	Pulsating DC for full cycle
Efficiency	40.6%	81.2%
Ripple Factor	1.21	0.48
Ripple Frequency	Same as input (50 Hz)	Twice the input (100 Hz)
PIV of Diode	V_m	$2V_m$ (center-tap), V_m (bridge)
TUF	0.287	0.693 (center-tap), 0.812 (bridge)
DC Output Voltage	$0.318V_m$	$0.636V_m$
Form Factor	1.57	1.11
Applications	Low power applications	Power supplies, battery chargers

Diagram:

Mermaid Diagram (Code)

```
{Shaded}  
{Highlighting} []  
graph TD  
    A[Rectifiers] --> B[Half Wave]  
    A --> C[Full Wave]  
    C --> D[Center-Tapped]  
    C --> E[Bridge]  
    B --> F[Uses 1 diode]  
    B --> G[Lower efficiency]  
    D --> H[Uses 2 diodes]  
    E --> I[Uses 4 diodes]  
    C --> J[Higher efficiency]  
{Highlighting}  
{Shaded}
```

Mnemonic

“HERO” - “Half wave: Efficiency Reduced, One-half cycle only”

Question 4(a) [3 marks]

Draw the symbol and construction of PNP and NPN transistor with proper notation.

Solution

Transistor Symbols and Construction:

NPN Symbol	PNP Symbol
C	C
-	-
/	/
{	}
{	}
{	/ }
/	
/	
-	-
B	B
-	-
E	E

Construction:

NPN Construction	PNP Construction
+{--}{-}{-}{-}{-}{-}{-}+	+{--}{-}{-}{-}{-}{-}{-}+
N	P {{-} Collector}
+{--}{-}{-}{-}{-}{-}{-}+	+{--}{-}{-}{-}{-}{-}{-}+
P	N {{-} Base}
+{--}{-}{-}{-}{-}{-}{-}+	+{--}{-}{-}{-}{-}{-}{-}+
N	P {{-} Emitter}

+{--}{-}{-}{-}{-}{-}{-}+

+{--}{-}{-}{-}{-}{-}{-}+

Mnemonic

“NIN-PIP” - “N-P-N layers for NPN, P-N-P layers for PNP”

Question 4(b) [4 marks]

Explain working of Transistor amplifier.

Solution

Working of Transistor Amplifier:

Circuit Configuration:

- Common Emitter: Most commonly used
- Biasing: Proper DC bias provided to operate in active region
- Coupling: Input/output coupling through capacitors
- Load: Collector resistor as load

Working Principle:

- Input Signal: Applied to base-emitter junction
- Base Current: Small base current controls larger collector current
- Amplification: Small input voltage variations cause larger output voltage variations
- Phase Shift: 180° phase shift between input and output

Key Parameters:

- Voltage Gain: $A_v = V_{out}/V_{in}$
- Current Gain: $= I_c/I_b$
- Input Impedance: Typically $1-2\text{k}\Omega$ in CE configuration

Diagram:

Mermaid Diagram (Code)

```
{Shaded}
{Highlighting} []
graph LR
    A[Input Signal] --> B[Base Current]
    B --> C[Controls Collector Current]
    C --> D[Voltage Drop Across R<sub>C</sub>]
    D --> E[Amplified Output Signal]
{Highlighting}
{Shaded}
```

Mnemonic

“ABCD” - “Amplification through Base Controlled collector Current Dynamics”

Question 4(c) [7 marks]

Explain working of Zener diode.

Solution

Working of Zener Diode:

Basic Structure:

- Junction: Heavily doped P-N junction
- Construction: Similar to normal diode but optimized for breakdown
- Breakdown: Designed to operate in reverse breakdown region

Working Principle:

- Forward Bias: Acts like normal diode
- Reverse Bias:
 - Below breakdown: Small leakage current
 - At breakdown: Sharp increase in current at Zener voltage

- Beyond breakdown: Maintains constant voltage

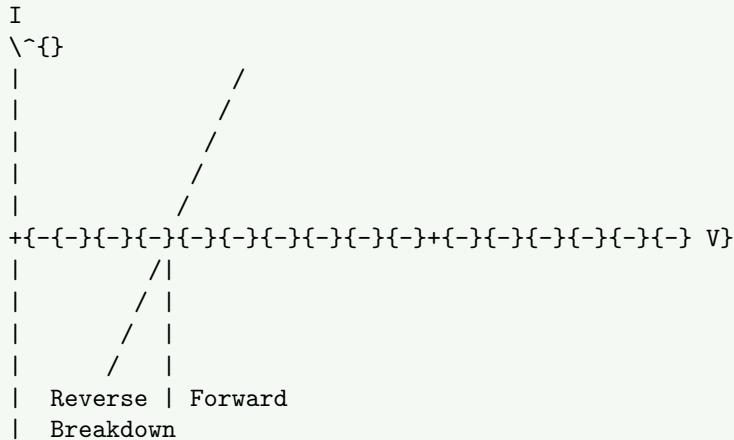
Breakdown Mechanisms:

- Zener Effect: Dominant below 5V (direct tunneling)
- Avalanche Effect: Dominant above 5V (impact ionization)

Applications:

- Voltage Regulation: Maintains constant output voltage
- Reference Voltage: Precise voltage reference
- Overvoltage Protection: Protects sensitive components

Diagram:



Mnemonic

“ZEBRA” - “Zener Effect Breaks at Regulated Avalanche voltage”

Question 4(a) [3 marks] (OR)

Explain transistor as a switch.

Solution

Transistor as a Switch:

Operating Regions:

- Cutoff Region: Transistor OFF ($IB = 0, IC \approx 0$)
- Saturation Region: Transistor ON ($IB > IC/ , VCE \approx 0.2V$)

Switching Operation:

- OFF State: No base current, high VCE, acts as open switch
- ON State: Sufficient base current, low VCE, acts as closed switch

Switching Characteristics:

- Turn-ON Time: Time to go from cutoff to saturation
- Turn-OFF Time: Time to go from saturation to cutoff

Diagram:

Mermaid Diagram (Code)

```
{Shaded}
{Highlighting} []
graph TD
    A[Transistor Switch] --> B[OFF State: Cutoff Region]
    A --> C[ON State: Saturation Region]
    B --> D[I<sub>B</sub>/sub<sub>C</sub></sub> = 0, I<sub>C</sub>/sub<sub>C</sub> 0]
    B --> E[V<sub>CE</sub>/sub<sub>C</sub> V<sub>CC</sub>/sub<sub>C</sub>]
    C --> F[I<sub>B</sub>/sub<sub>C</sub> I<sub>C</sub>/sub<sub>C</sub>]
    C --> G[V<sub>CE</sub>/sub<sub>C</sub> 0.2V]
```

Mnemonic

“COST” - “Cutoff Off, Saturation Turns-on”

Question 4(b) [4 marks] (OR)

Draw and Explain characteristics of CE amplifier.

Solution

CE Amplifier Characteristics:

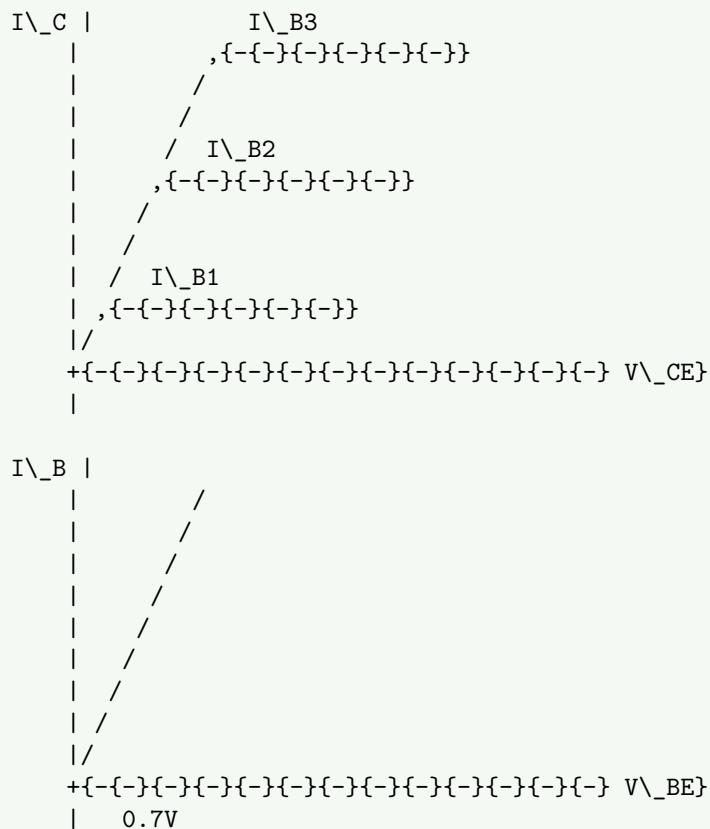
Input Characteristics:

- Plot: I_B vs V_{BE} at constant V_{CE}
- Behavior: Resembles forward-biased diode curve
- Knee Voltage: Approximately 0.7V for silicon
- Input Resistance: Slope of curve ($\Delta V_{BE}/\Delta I_B$)

Output Characteristics:

- Plot: I_C vs V_{CE} at constant I_B
- Regions:
 - Saturation ($V_{CE} < 0.2V$)
 - Active ($V_{CE} > 0.2V$)
 - Cutoff ($I_B = 0$)
- Early Effect: Slight increase in I_C with increasing V_{CE}

Diagram:



Mnemonic

“IAOC” - “Input curves At Origin, Output curves show Current gain”

Question 4(c) [7 marks] (OR)

Explain working of Varactor diode.

Solution

Working of Varactor Diode:

Basic Structure:

- Junction: Special P-N junction diode
- Operation: Always operated in reverse bias
- Property: Junction capacitance varies with reverse voltage

Working Principle:

- Depletion Layer: Widens with increasing reverse voltage
- Capacitance Effect: Depletion region acts as dielectric between P and N regions
- Capacitance Formula: $C \propto 1/d$
- Tuning Range: Typically 4:1 to 10:1 capacitance

Applications:

- Voltage-Controlled Capacitor: In electronic tuning circuits
- Frequency Modulation: In voltage-controlled oscillators (VCOs)
- Automatic Frequency Control: In receivers
- Parametric Amplification: In microwave circuits

Diagram:

Mermaid Diagram (Code)

```
{Shaded}  
{Highlighting} []  
graph LR  
    A[Varactor Diode] --> B[Reverse Bias Operation]  
    B --> C[Depletion Region Width]  
    C --> D[Junction Capacitance]  
    D --> E[Changes with Applied Voltage]  
    E --> F[Electronic Tuning]  
{Highlighting}  
{Shaded}
```

Mnemonic

“VCAP” - “Voltage Controls cAPacitance”

Question 5(a) [3 marks]

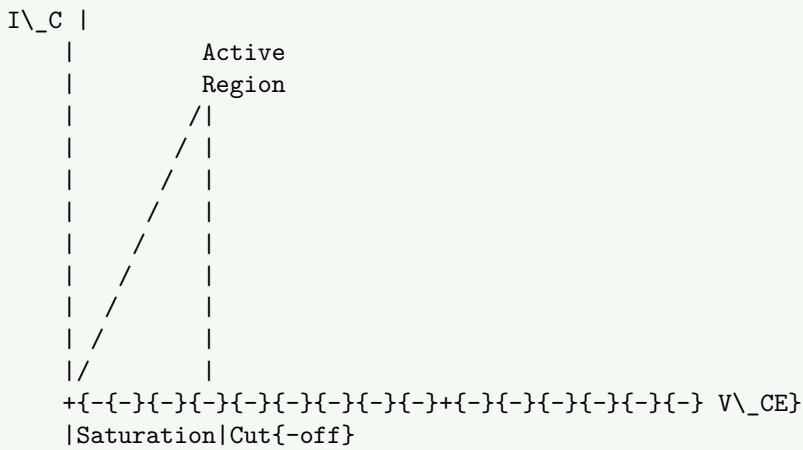
Define Active, Saturation and Cut-off region for transistor amplifier.

Solution

Transistor Regions of Operation:

Region	Definition	Biasing Condition	Application
Active Region	Both junctions are properly biased (BE forward, BC reverse)	$IB > 0, VCE > VCE(sat)$	Amplification
Saturation Region	Both junctions forward biased	$IB > IC, VCE \approx 0.2V$	Switching (ON state)
Cut-off Region	Both junctions reverse biased	$IB = 0, IC \approx 0, VCE \approx VCC$	Switching (OFF state)

Diagram:



Mnemonic

“ASC” - “Active for Signals, Saturation & Cutoff for switches”

Question 5(b) [4 marks]

If the value of $I_C = 10\text{mA}$ and $I_B = 100 \text{ A} = 0.1 \text{ mA}$ then find the value of current gains α and β .

Solution

Given:

- Collector current (I_C) = 10 mA
- Base current (I_B) = $100 \text{ A} = 0.1 \text{ mA}$

Calculate (Common Emitter Current Gain):

- $\alpha = I_C / I_B$
- $= 10 \text{ mA} / 0.1 \text{ mA}$
- $= 100$

Calculate (Common Base Current Gain):

- $I_E = I_C + I_B = 10 \text{ mA} + 0.1 \text{ mA} = 10.1 \text{ mA}$
- $\beta = I_C / I_E$
- $= 10 \text{ mA} / 10.1 \text{ mA}$
- $= 0.990 \text{ or } 0.99$

Relation between α and β :

- $\alpha = \beta / (\beta + 1)$
- $= 100 / (100 + 1) = 100 / 101 = 0.990$
- $= \beta / (1 - \beta)$
- $= 0.99 / (1 - 0.99) = 0.99 / 0.01 = 99 \approx 100$

Mnemonic

“ABC” - “Alpha equals Beta divided by (Beta plus one) for Current gains”

Question 5(c) [7 marks]

Discuss Strategies of electronic waste management in the small electronics Industries.

Solution

E-Waste Management Strategies for Small Electronics Industries:

Strategy	Description	Implementation
Segregation	Separate e-waste from general waste	Dedicated collection bins for different components

Reduce	Minimize waste generation	Efficient design, extended product life, repair services
Reuse	Use components again	Refurbish, repurpose working parts
Recycle	Process for material recovery	Partner with authorized recyclers, follow guidelines

Training	Educate employees	Regular workshops on proper handling procedures
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Key Implementation Steps:

- **Inventory Management:** Track electronic components throughout lifecycle
- **Authorized Partnerships:** Work only with certified e-waste handlers
- **Documentation:** Maintain records of waste disposal for compliance
- **Green Design:** Design products for easy disassembly and recycling

Regulatory Compliance:

- **Registration:** Register with pollution control board
- **Authorization:** Obtain necessary permits
- **Annual Returns:** Submit regular compliance reports

Diagram:

Mermaid Diagram (Code)

```
{Shaded}
{Highlighting} []
graph TD
    A[E{-Waste Management}] --> B[Collection \& Segregation]
    A --> C[Storage]
    A --> D[Transportation]
    A --> E[Processing]
    B --> F[Separate bins for different components]
    C --> G[Safe storage in designated areas]
    D --> H[Authorized carriers only]
    E --> I[Authorized recyclers]
    E --> J[Material recovery]
    E --> K[Safe disposal of residues]
{Highlighting}
{Shaded}
```

Mnemonic

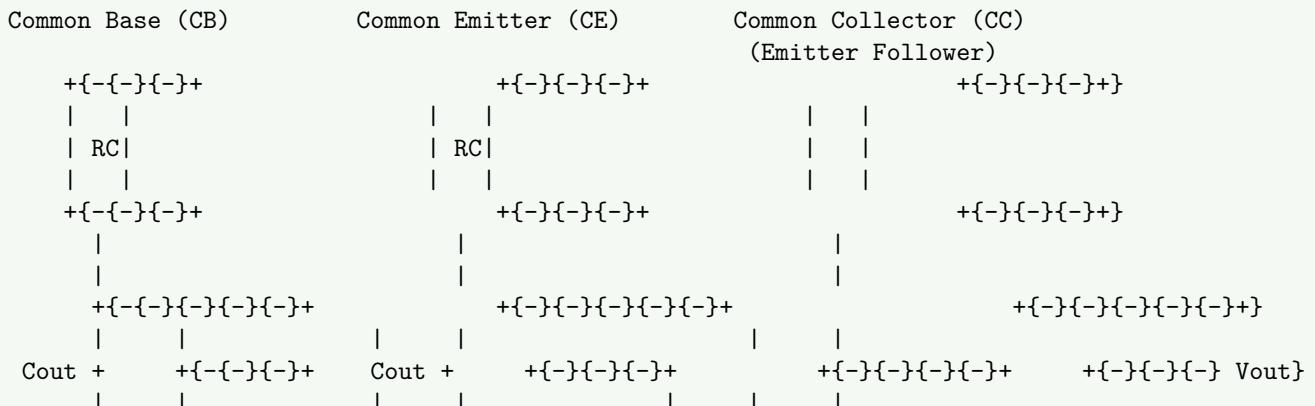
“SRRTA” - “Segregate, Reduce, Reuse, Train, Authorize”

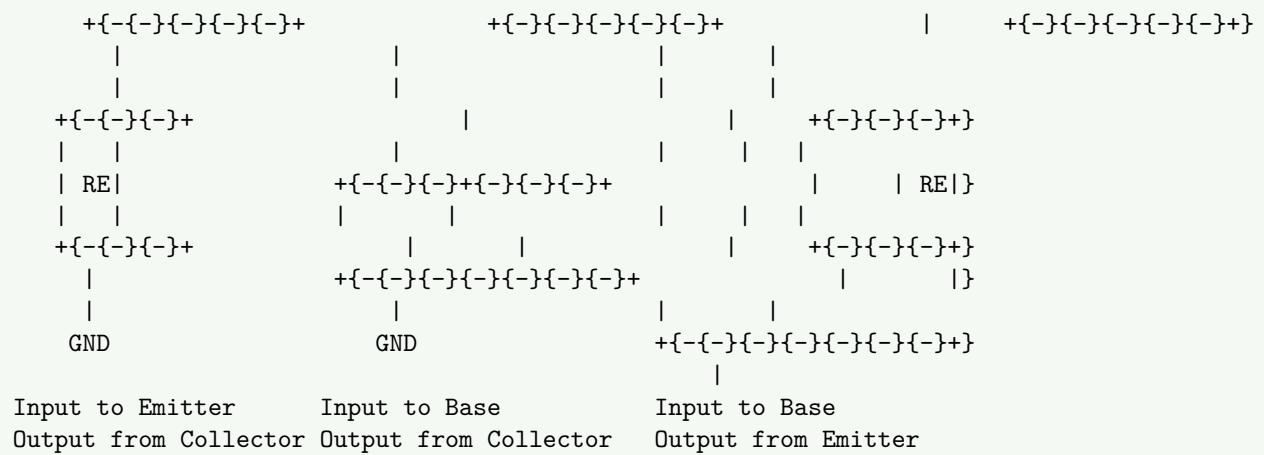
Question 5(a) [3 marks] (OR)

Draw CB, CE and CC transistor configuration circuits.

Solution

Transistor Configuration Circuits:





Key Characteristics:

- CB: High stability, low input impedance, high output impedance
- CE: Medium stability, medium input impedance, medium output impedance
- CC: Low stability, high input impedance, low output impedance

Mnemonic

“EBC” - “Emitter input for CB, Base input for CE/CC, Collector output for CB/CE”

Question 5(b) [4 marks] (OR)

Derive relation between current gains α and β .

Solution

Relation Between Current Gains α and β :

Given definitions:

- $\alpha = IC/IE$ (Common Base current gain)
- $\beta = IC/IB$ (Common Emitter current gain)

Step 1: Use current relation in transistor

- $IE = IC + IB$

Step 2: Express β in terms of

- $\beta = IC/IE$
- $\beta = IC/(IC + IB)$

Step 3: Substitute $IB = IC/\alpha$

- $\beta = IC/(IC + IC/\alpha)$
- $\beta = IC/(IC(1 + 1/\alpha))$
- $\beta = IC/(IC(\alpha + 1)/\alpha)$
- $\beta = \alpha/(\alpha + 1)$

Step 4: Express α in terms of

- $\alpha = \beta/(1 - \beta)$

Diagram:

$$\begin{array}{ccc}
 & I_C & \\
 / & & \{\} \\
 / & & \{\} \\
 I_B & & I_E \\
 & = I_C/I_E & \\
 & = I_C/I_B & \\
 I_E & = I_C + I_B &
 \end{array}$$

Mnemonic

“ABR” - “Alpha = Beta divided by (Beta plus one) Reciprocally”

Question 5(c) [7 marks] (OR)

Define E-Waste and Explain disposal of electronic waste.

Solution

E-Waste Definition: Electronic waste (e-waste) refers to discarded electrical or electronic devices that have reached end-of-life or become obsolete, including computers, televisions, mobile phones, printers, and other electronic equipment containing hazardous components like lead, mercury, cadmium, PCBs, and brominated flame retardants.

Disposal Methods of E-Waste:

Method	Description	Environmental Impact
Collection & Segregation	Gathering and separating by type	Reduces contamination
Dismantling	Manual disassembly of components	Enables targeted recycling
Material Recovery	Extracting valuable materials	Conserves natural resources
Refurbishment	Repairing for reuse	Extends product lifecycle
Authorized Recycling	Processing by certified facilities	Ensures proper handling

Disposal Process Flow:

- Initial Assessment: Determine if device can be repaired/reused
- Data Sanitization: Secure erasure of personal/business data
- Disassembly: Separation into component categories
- Resource Recovery: Extraction of valuable materials
- Hazardous Waste: Special handling of toxic components

Diagram:

Mermaid Diagram (Code)

```
{Shaded}
{Highlighting} []
graph TD
    A[E{-Waste Disposal}] --> B[Collection]
    B --> C[Sorting \& Segregation]
    C --> D[Recycling]
    C --> E[Recovery]
    C --> F[Safe Disposal]
    D --> G[Disassembly]
    G --> H[Material Sorting]
    H --> I[Crushing \& Shredding]
    I --> J[Material Separation]
    J --> K[Refinement]
    K --> L[New Products]
    F --> M[Landfill for Inert Material]
    F --> N[Incineration with Pollution Control]
{Highlighting}
{Shaded}
```

Mnemonic

“CRESD” - “Collect, Recycle, Extract, Separate, Dispose”