

# Microprocessor and Microcontroller (4341101) - Winter 2023 Solution

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## Question 1 [a marks]

3 Compare RISC and CISC.

### Solution

Answer:

Table 1. RISC vs CISC

Feature	RISC	CISC
Instructions	Simple, fixed-length	Complex, variable-length
Execution	Single cycle	Multiple cycles
Addressing modes	Few	Many
Registers	Many	Few
Design focus	Hardware simplicity	Code density

### Mnemonic

“RISCs Complete Instructions Simply”

## Question 1 [b marks]

4 Compare Von-Neumann and Harvard architecture.

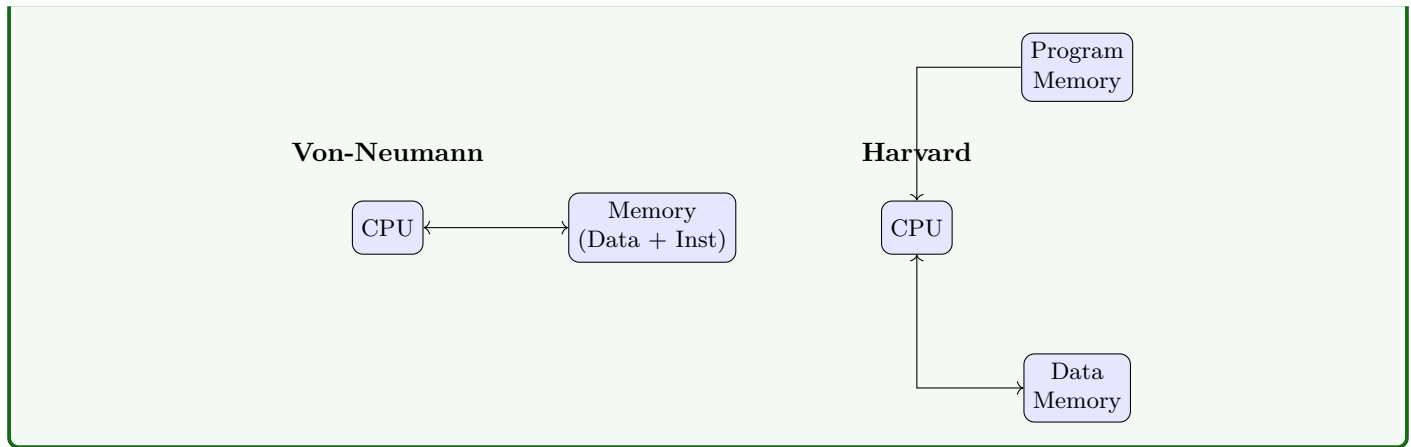
### Solution

Answer:

Table 2. Von-Neumann vs Harvard

Feature	Von-Neumann	Harvard
Memory	Single shared memory	Separate program & data memory
Bus	Single bus for data & instructions	Separate buses
Speed	Slower (memory bottleneck)	Faster (parallel access)
Complexity	Simpler design	More complex
Applications	General computing	Real-time systems

Diagram:



### Mnemonic

“Harvard Has Separate Spaces”

## Question 1 [c marks]

7 Explain: 8085 Instruction Format, Control Unit, Machine Cycle, ALU

### Solution

Answer:

#### 1. Instruction Format:

Opcode	Operand 1	Operand 2
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1-3 Bytes Total Length

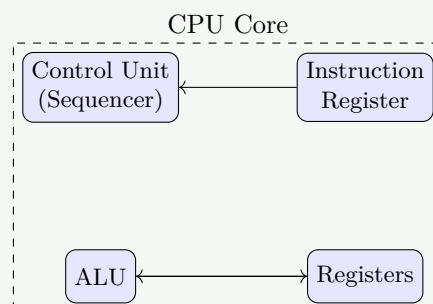
Contains opcode (3-8 bits) and 0-2 operands.

#### 2. Explanations:

Table 3. Components

Component	Function
<b>Instruction Format</b>	1-3 byte structure with opcode and operands
<b>Control Unit</b>	Fetches, decodes instructions; generates signals
<b>Machine Cycle</b>	Basic operation cycle (T-states)
<b>ALU</b>	Performs arithmetic and logical operations

#### 3. Diagram:



**Mnemonic**

“CIMA: Control Interprets, Machine Acts”

OR

## Question 1 [c marks]

7 Compare Microprocessor and Microcontroller.

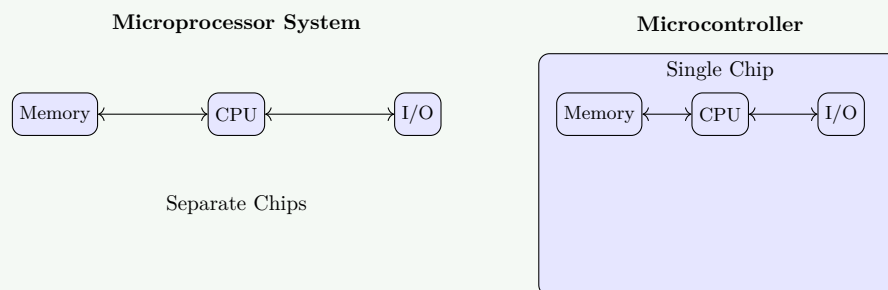
**Solution**

Answer:

**Table 4.** Microprocessor vs Microcontroller

Feature	Microprocessor	Microcontroller
Design	CPU only	CPU + peripherals
Memory	External	Internal (RAM/ROM)
I/O ports	Limited	Many built-in
Cost	Higher	Lower
Applications	General computing	Embedded systems
Power	Higher	Lower
Example	Intel 8085/8086	Intel 8051

Diagram:

**Mnemonic**

“Micro-P Processes, Micro-C Controls”

## Question 2 [a marks]

3 Explain Instruction Fetching, Decoding and Execution Operation in microprocessor.

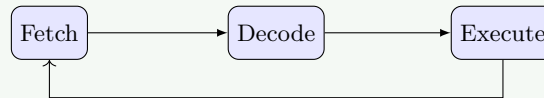
**Solution**

Answer:

**Table 5.** Operation Phases

Phase	Operation
<b>Fetching</b>	CPU gets instruction from memory using PC
<b>Decoding</b>	Determines operation type and operands
<b>Execution</b>	Performs the actual operation

Diagram:



**Mnemonic**

“FDE: First Get, Then Understand, Finally Do”

## Question 2 [b marks]

4 Explain Bus Organization of 8085 microprocessor.

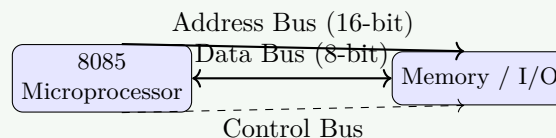
**Solution**

Answer:

**Table 6. 8085 Buses**

Bus Type	Width	Function
<b>Address Bus</b>	16-bit	Carries memory addresses (A0-A15)
<b>Data Bus</b>	8-bit	Transfers data (D0-D7)
<b>Control Bus</b>	Various	Manages data flow (RD, WR, IO/M)
<b>Multiplexed</b>	AD0-AD7	Lower address bits + data bits

Diagram:



**Mnemonic**

“ADC: Address points, Data flows, Control directs”

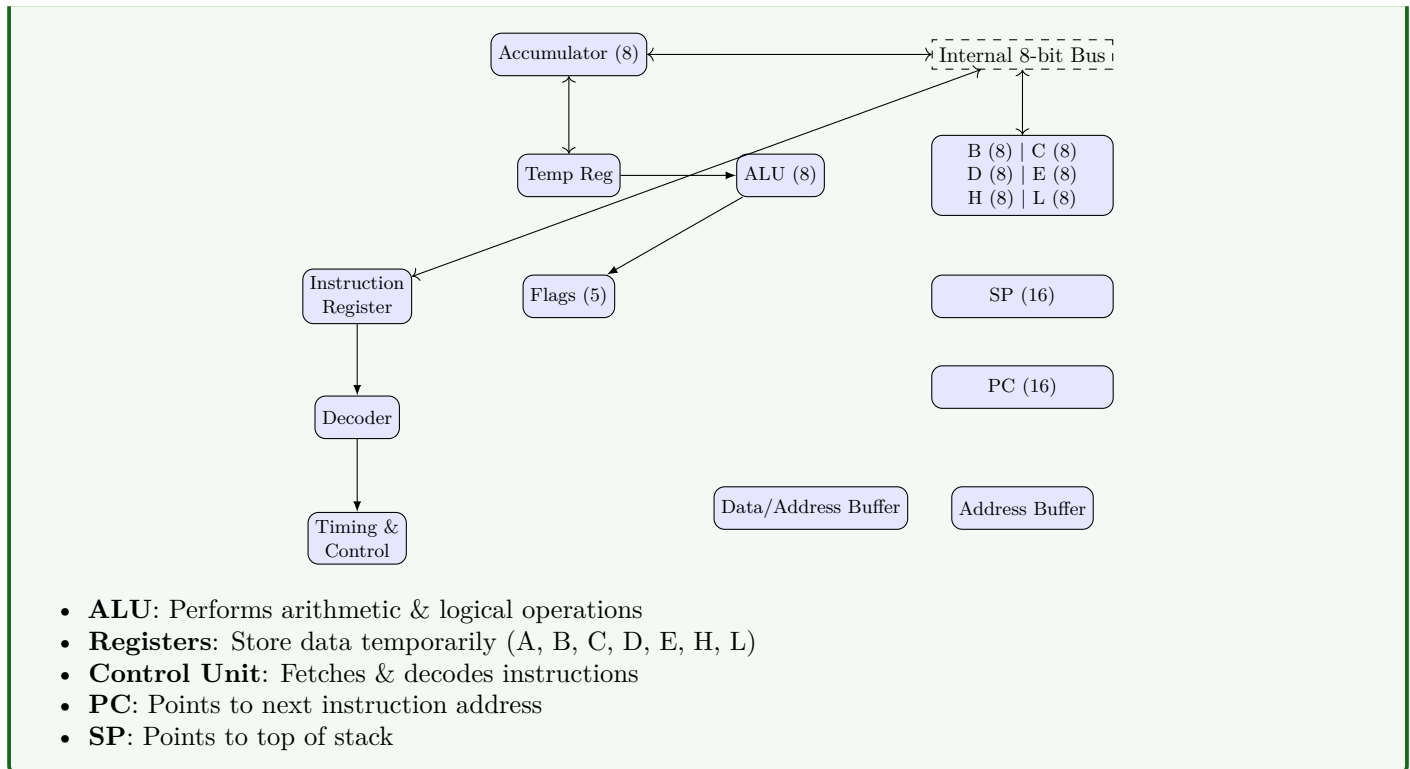
## Question 2 [c marks]

7 Describe architecture of 8085 microprocessor with the help of neat diagram.

**Solution**

Answer:

Diagram:



### Mnemonic

“AR CBD: Architecture Registers Control Buses Data”

OR

## Question 2 [a marks]

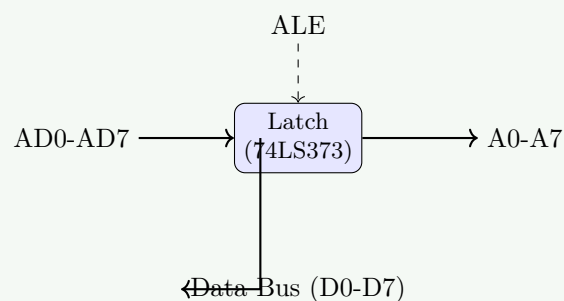
3 Explain De-multiplexing of Address and Data buses for 8085 Microprocessor.

### Solution

#### Answer:

1. **ALE High:** Lower address (A0-A7) appears on AD0-AD7 lines. Latch captures it.
2. **ALE Low:** AD0-AD7 lines are used for Data (D0-D7).

#### Diagram:



### Mnemonic

“ALAD: ALE Latches Address before Data”

OR

## Question 2 [b marks]

4 Draw Flag Register of 8085 microprocessor & explain it.

### Solution

Answer:

Flag Register (8-bit):

D7	D6	D5	D4	D3	D2	D1	D0
S	Z	X	AC	X	P	1	CY

- **S (Sign):** Set if D7 is 1 (Negative result)
- **Z (Zero):** Set if result is zero
- **AC (Auxiliary Carry):** Carry from D3 to D4
- **P (Parity):** Set if result has even number of 1s
- **CY (Carry):** Carry out from D7

### Mnemonic

“SuZie AC’s Perfect CarrY”

OR

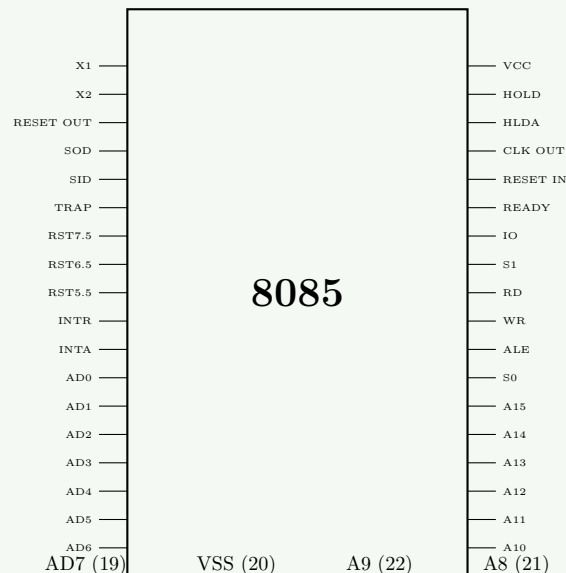
## Question 2 [c marks]

7 Describe Pin diagram of 8085 microprocessor with the help of neat diagram.

### Solution

Answer:

Pin Diagram:



- **Address/Data:** Multiplexed AD0-AD7, A8-A15
- **Control:** RD, WR, IO/M, ALE
- **Interrupts:** TRAP, RST 7.5/6.5/5.5, INTR
- **Power:** VCC (+5V), VSS (GND)

**Mnemonic**

“ACID-PS: Address-Control-Interrupt-DMA-Power-Serial”

**Question 3 [a marks]**

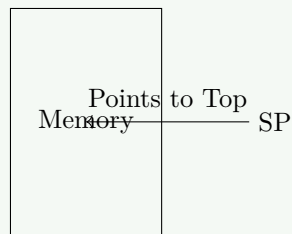
3 Explain Stack, Stack Pointer and Stack operation.

**Solution**

**Answer:**

- **Stack:** Reserved area of RAM used for temporary storage (LIFO).
- **Stack Pointer (SP):** 16-bit register holding address of top of stack.
- **PUSH:** Decrement SP, Store data.
- **POP:** Retrieve data, Increment SP.

**Diagram:**



LIFO: Last In First Out

**Mnemonic**

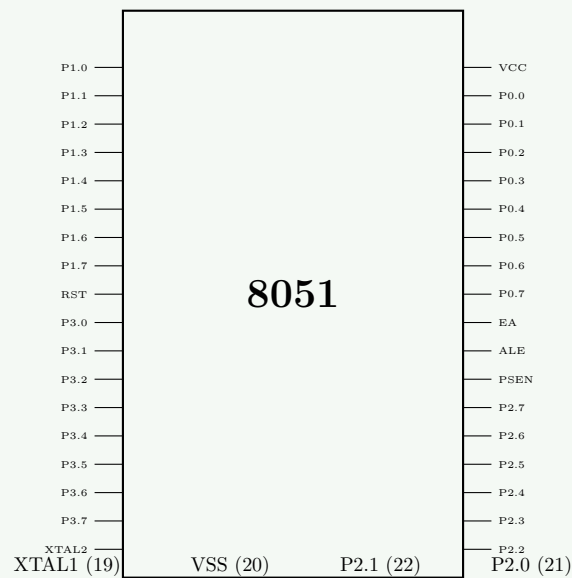
“SP Points to LIFO Lane”

**Question 3 [b marks]**

4 Draw Pin diagram of 8051 microcontroller.

**Solution**

**Answer:**



- **P0:** Multiplexed Address/Data
- **P1:** General I/O
- **P2:** High Order Address
- **P3:** Special Functions (Serial, Int, Timer)

#### Mnemonic

“PORT 0123: Data-General-Address-Special”

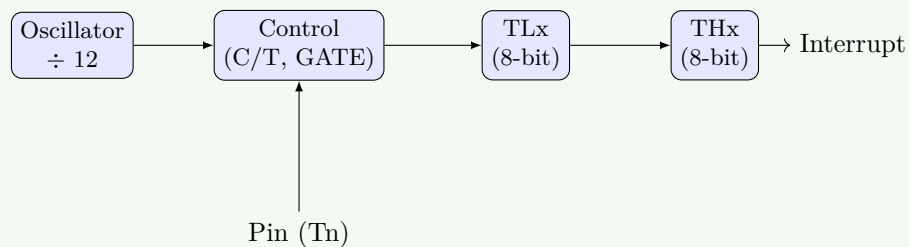
### Question 3 [c marks]

7 Draw Timers/Counters logic diagram of 8051 microcontroller and explain its operation in various modes.

#### Solution

Answer:

Logic Diagram:



Modes:

- **Mode 0:** 13-bit timer mode.
- **Mode 1:** 16-bit timer mode.
- **Mode 2:** 8-bit auto-reload mode.
- **Mode 3:** Split timer mode.

#### Mnemonic

“MARC: Mode Auto-Reload Count”



OR

## Question 3 [a marks]

3 List Common features of Microcontrollers.

## Solution

Answer:

Table 7. MCU Features

Feature	Purpose
<b>CPU Core</b>	Process instructions
<b>Memory</b>	Store program (ROM) and data (RAM)
<b>I/O Ports</b>	Interface with external devices
<b>Timers</b>	Measure time intervals
<b>Interrupts</b>	Handle asynchronous events
<b>Serial Comm</b>	Transfer data with other devices

## Mnemonic

“CRITICS: CPU ROM I/O Timers Interrupts Comm Serial”

OR

## Question 3 [b marks]

4 Explain Internal RAM Organization of 8051 microcontroller.

## Solution

Answer:

	Lower 128 Bytes
Bank 0 (00H-07H)	
Bank 1 (08H-0FH)	
Bank 2 (10H-17H)	
Bank 3 (18H-1FH)	
Bit Addressable (20H-2FH)	
Scratch Pad (30H-7FH)	

- **Register Banks (00H-1FH):** 4 banks of 8 registers (R0-R7).
- **Bit Addressable (20H-2FH):** 16 bytes where each bit can be accessed.
- **Scratch Pad (30H-7FH):** General purpose RAM.
- **SFRs (80H-FFH):** Special Function Registers (upper 128 bytes).

**Mnemonic**

“RBBS: Registers Bits Buffer Scratch”

OR

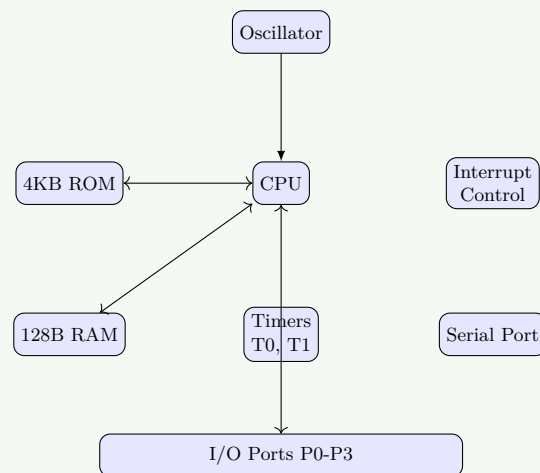
### Question 3 [c marks]

7 Explain architecture of 8051 microcontroller with the help of neat diagram.

**Solution**

**Answer:**

**Diagram:**



- **CPU:** 8-bit central processor.
- **Memory:** 4KB ROM (Code), 128B RAM (Data).
- **I/O:** 4 Ports (P0-P3).
- **Timers:** 2 16-bit timers.
- **Serial:** 1 UART channel.
- **Interrupts:** 5 sources.

**Mnemonic**

“CAPITALS: CPU Architecture Ports I/O Timer ALU LS-Interface Serial”

### Question 4 [a marks]

3 Write an 8051 Assembly Language Program to Copy the data from external RAM Location 0123h to TL0 and Data from external RAM location 0234h to TH0.

**Solution**

**Answer:**

```

1  MOV  DPTR, #0123H    ; Load DPTR with source address 0123H
2  MOVX  A, @DPTR       ; Read data from external RAM
3  MOV  TL0, A          ; Copy to Timer 0 low byte
4
5  MOV  DPTR, #0234H    ; Load DPTR with source address 0234H
  
```

```

6 MOVX A, @DPTR      ; Read data from external RAM
7 MOV TH0, A         ; Copy to Timer 0 high byte

```

### Mnemonic

“DRAM: DPTR Read Address Move”

## Question 4 [b marks]

4 Write an 8051 Assembly Language Program to blink LED interfaced at port P1.3 at time interval of 1ms.

### Solution

#### Answer:

```

1 AGAIN: SETB P1.3      ; Turn ON LED at P1.3
2          ACALL DELAY   ; Call delay subroutine
3          CLR P1.3      ; Turn OFF LED at P1.3
4          ACALL DELAY   ; Call delay subroutine
5          SJMP AGAIN    ; Repeat forever
6
7 DELAY:  MOV R7, #250    ; Load R7 for outer loop
8 OUTER:  MOV R6, #1      ; Load R6 for inner loop
9 INNER:  DJNZ R6, INNER  ; Decrement R6 until zero
10        DJNZ R7, OUTER  ; Decrement R7 until zero
11        RET            ; Return from subroutine

```

### Mnemonic

“STACI: Set-Timer-And-Clear-Infinitely”

## Question 4 [c marks]

7 List Addressing Modes of 8051 Microcontroller and explain all of them with the help of example.

### Solution

#### Answer:

Table 8. Addressing Modes

Addressing Mode	Example	Description
Immediate	MOV A, #25H	Data is in instruction
Register	MOV A, R0	Data is in register
Direct	MOV A, 30H	Data is at RAM address
Indirect	MOV A, @R0	R0/R1 contains address
Indexed	MOVC A, @A+DPTR	Access program memory
Bit	SETB P1.3	Access individual bits
Relative	SJMP LABEL	Jumps with 8-bit offset

**Mnemonic**

“IM DIRBI: Immediate Register Direct Bit Indexed”

OR

## Question 4 [a marks]

3 Write an 8051 Assembly Language Program to Subtract the content of RAM location 11h from RAM location 14h; put result in RAM location 3Ch.

**Solution****Answer:**

```

1  MOV  A, 14H      ; Load content of RAM location 14H to A
2  CLR  C           ; Clear carry flag
3  SUBB A, 11H      ; Subtract content of 11H with borrow
4  MOV  3CH, A      ; Store result in RAM location 3CH

```

**Mnemonic**

“LCSS: Load-Clear-Subtract-Store”

OR

## Question 4 [b marks]

4 Write an 8051 Assembly Language Program to generate a square wave of 50% duty cycle on bit 3 of Port 1 using Timer 0 in Mode 1.

**Solution****Answer:**

```

1      MOV  TMOD, #01H ; Timer 0, Mode 1 (16-bit)
2  AGAIN: MOV  TH0, #0FCH ; Load high byte
3      MOV  TL0, #18H  ; Load low byte (-1000 in 16-bit)
4      SETB TR0        ; Start timer
5      JNB  TF0, $      ; Wait for overflow
6      CLR  TR0        ; Stop timer
7      CLR  TF0        ; Clear timer flag
8      CPL  P1.3        ; Toggle P1.3
9      SJMP AGAIN      ; Repeat

```

**Mnemonic**

“MSTCCS: Mode-Set-Timer-Check-Clear-Switch”

OR

## Question 4 [c marks]

7 Explain any seven Logical Instructions with example for 8051 Microcontroller.

**Solution****Answer:****Table 9.** Logical Instructions

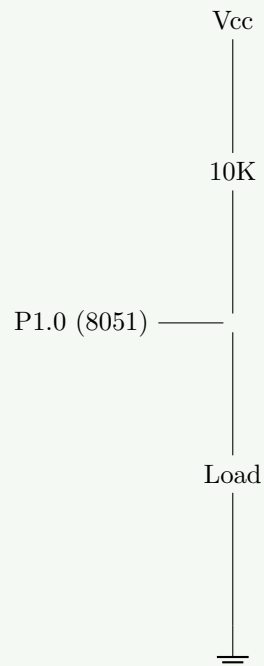
Instruction	Example	Operation
<b>ANL</b>	ANL A, #3FH	Logical AND
<b>ORL</b>	ORL P1, #80H	Logical OR
<b>XRL</b>	XRL A, R0	Logical XOR
<b>CLR</b>	CLR A	Clear (set to 0)
<b>CPL</b>	CPL P1.0	Complement (invert)
<b>RL</b>	RL A	Rotate left
<b>RR</b>	RR A	Rotate right

**Mnemonic**

“A-OX-CCR: AND OR XOR Clear Complement Rotate”

**Question 5 [a marks]**

3 Draw Interfacing of Push button Switch with 8051 microcontroller.

**Solution****Answer:****Diagram:**

- **Pull-up Resistor:** Keeps pin HIGH when button is open.
- **Button Press:** Pulls pin LOW.

**Mnemonic**

“PIP: Pull-up-Input-Press”

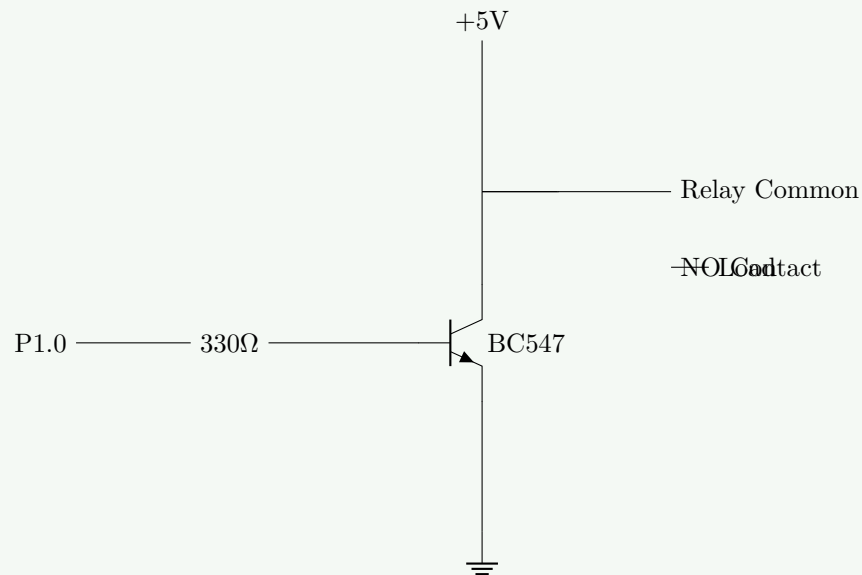
**Question 5 [b marks]**

4 Interface Relay with 8051 microcontroller.

**Solution**

Answer:

Diagram:

**Mnemonic**

“TRIP: Transistor-Relay-Interface-Protection”

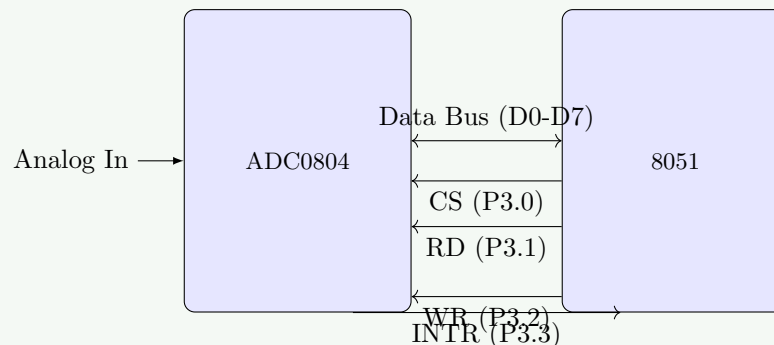
**Question 5 [c marks]**

7 Interface ADC0804 with 8051 microcontroller.

**Solution**

Answer:

Diagram:



- **Data Bus:** P1.0-P1.7 connected to D0-D7.
- **Control:** RD, WR, INTR for handshaking.

**Mnemonic**

“CRIW: Control-Read-Interrupt-Write”

OR

## Question 5 [a marks]

3 List Applications of microcontroller in various fields.

**Solution**

Answer:

Table 10. Applications

Field	Applications
<b>Industrial</b>	Motor control, automation, PLCs
<b>Medical</b>	Patient monitoring, diagnostic equipment
<b>Consumer</b>	Washing machines, microwaves, toys
<b>Automotive</b>	Engine control, ABS, airbag systems
<b>Communication</b>	Mobile phones, modems, routers
<b>Security</b>	Access control, alarm systems

**Mnemonic**

“I-MACS: Industrial-Medical-Automotive-Consumer-Security”

OR

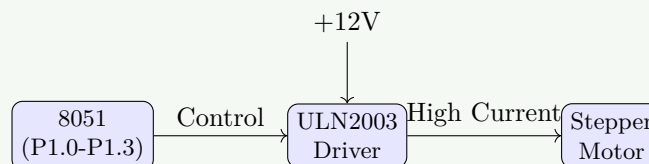
## Question 5 [b marks]

4 Interface Stepper motor with 8051 microcontroller.

**Solution**

Answer:

Diagram:



Sequence (Clockwise): 0x08, 0x0C, 0x04, 0x06.

**Mnemonic**

“PDCS: Port-Driver-Current-Sequence”

OR

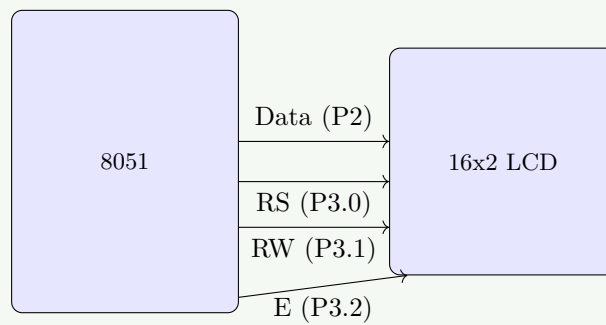
## Question 5 [c marks]

7 Interface LCD with 8051 microcontroller.

### Solution

Answer:

Diagram:



- **Data:** Port 2 sends ASCII data/commands.
- **RS:** 0 for Command, 1 for Data.
- **E:** Enable Pulse to latch data.

### Mnemonic

“DICE: Data-Instruction-Control-Enable”