Microprocessor & Microcontroller Systems (1333202) - Winter 2024 Solution

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Question 1(a) [3 marks]

List the features of 8051 Microcontroller.

Solution

The 8051 microcontroller has several important features:

Table 1. Features of 8051

Feature	Description
CPU	8-bit CPU optimized for control applications
Memory	4KB internal ROM, 128 bytes internal RAM
I/O Ports	4 bidirectional 8-bit I/O ports (P0-P3)
Timers	Two 16-bit timer/counters (Timer 0 & Timer 1)
Interrupts	5 interrupt sources with 2 priority levels
Serial Port	Full duplex UART for serial communication

Mnemonic

"CPU Memory Input-Output Timers Interrupts Serial (C-MIT-IS)"

Question 1(b) [4 marks]

Define: Opcode, Operand, Instruction cycle, Machine cycle

Solution

Table 2. Definitions

Term	Definition
Opcode	Operation code that specifies the operation to be performed
Operand	Data or address on which the operation is performed
Instruction Cycle	Complete process of fetching, decoding and executing an instruction
Machine Cycle	Time required to access memory or I/O device

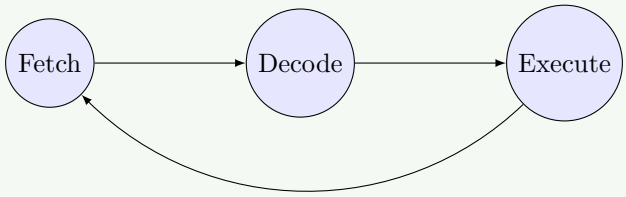

Figure 1. Instruction Cycle

Mnemonic

"Opcode Operand Instruction-cycle Data-cycle (OOID)"

Question 1(c) [7 marks]

Compare Von Neumann and Harvard Architecture.

Solution

Table 3. Von Neumann vs Harvard

Parameter	Von Neumann	Harvard
Memory Structure	Single memory for program and data	Separate memory for program and data
Bus System	Single bus system	Separate bus for program and data
Speed	Slower due to bus conflicts	Faster simultaneous access
Cost	Lower cost	Higher cost
Complexity	Simple design	Complex design
Examples	8085, x86 processors	8051, DSP processors

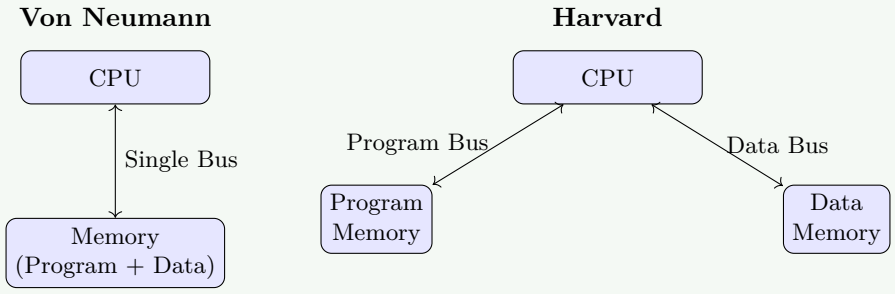

Figure 2. Architecture Comparison

Mnemonic

"Von-Single-Bus-Simple-Cheap vs Harvard-Separate-Dual-Fast-Complex (VSBSC vs HSDFC)"

Question 1(c) OR [7 marks]

Compare RISC and CISC.

Solution

Table 4. RISC vs CISC

Parameter	RISC	CISC
Instruction Set	Reduced, simple instructions	Complex instruction set
Instruction Size	Fixed size instructions	Variable size instructions
Execution Time	Single clock cycle per instruction	Multiple clock cycles
Memory Access	Load/Store architecture	Memory-to-memory operations
Compiler	Complex compiler required	Simple compiler
Examples	ARM, MIPS	8085, x86

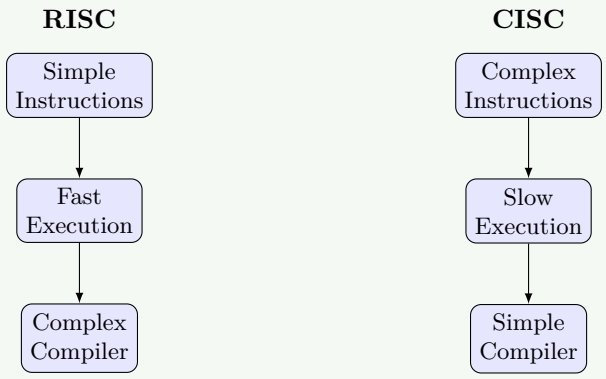

Figure 3. RISC vs CISC Concepts

Mnemonic

"Simple-Fast-Complex vs Complex-Slow-Simple (RISC-SFS vs CISC-CSS)"

Question 2(a) [3 marks]

List the 16-bit Registers available in 8085 and Explain its Function.

Solution

Table 5. 16-bit Registers of 8085

Register	Function
PC (Program Counter)	Points to next instruction address. Automatically increments after each instruction fetch.
SP (Stack Pointer)	Points to top of stack in memory. Decrements during PUSH, increments during POP operations.
BC, DE, HL	General purpose register pairs for 16-bit data storage or addresses.

Mnemonic

"Program-Counter Stack-Pointer BC-DE-HL (PC SP BDH)"

Question 2(b) [4 marks]

Explain Address and Data Bus De-multiplexing in 8085.

Solution

De-multiplexing separates address and data signals from AD0-AD7 pins using ALE signal.

- **ALE**: Address Latch Enable signal controls the process.
- **T1 state**: AD0-AD7 contains lower 8-bit address. ALE goes HIGH.
- **Latch**: Address is latched in external latch (74LS373) when ALE is High.
- **T2-T3 states**: AD0-AD7 becomes data bus.

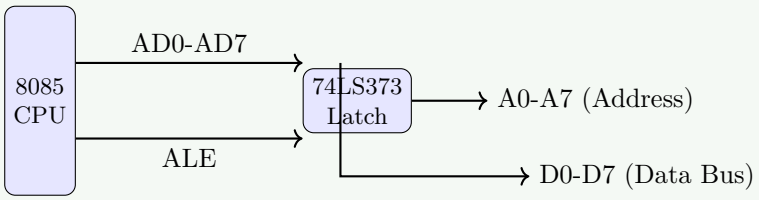

Figure 4. Address/Data Demultiplexing

Mnemonic

"ALE Latches Address Low"

Question 2(c) [7 marks]

Explain Pin Diagram of 8085 with neat sketch.

Solution

The 8085 is a 40-pin microprocessor.

Table 6. Pin Functions

Pin Group	Function
AD0-AD7	Multiplexed Address/Data bus (Lower 8-bit)
A8-A15	Higher order Address bus
ALE	Address Latch Enable signal
RD, WR	Read and Write control signals
IO/M	I/O or Memory operation indicator
S0, S1	Status signals

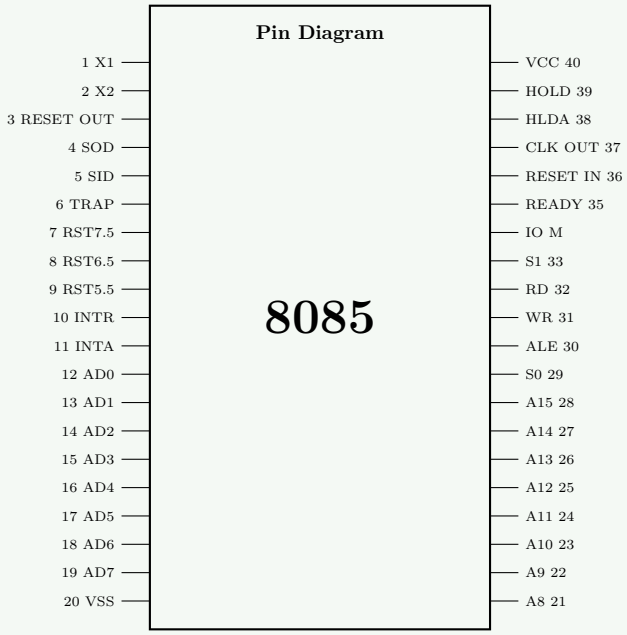

Figure 5. 8085 Pin Diagram

Mnemonic

"Address Data Control Power Interrupt (ADCPI)"

Question 2(a) OR [3 marks]

Explain Instruction Fetching Operation in 8085.

Solution

Instruction fetching is the first step in instruction cycle:

- **PC contents** placed on address bus (A0-A15).
- **ALE signal** goes high to latch address.
- **RD signal** goes low to read memory.
- **Instruction** fetched from memory to data bus.
- **PC incremented** to point to next instruction.

This occurs during **T1 and T2** states and takes **4 clock cycles** for simple instructions.

Mnemonic

"PC ALE RD Fetch Increment (PARFI)"

Question 2(b) OR [4 marks]

Explain Flag Register of 8085.

Solution

The Flag Register stores status information after arithmetic/logical operations.

Table 7. 8085 Flags

Bit	Flag	Function
D7	**S (Sign)**	Set if result is negative
D6	**Z (Zero)**	Set if result is zero
D4	**AC (Aux Carry)**	Set if carry from bit 3 to 4
D2	**P (Parity)**	Set if result has even parity
D0	**CY (Carry)**	Set if carry/borrow generated

D7	D6	D5	D4	D3	D2	D1	D0
S	**Z**	**X**	**AC**	**X**	**P**	**X**	**CY**

Figure 6. Flag Register Format

Mnemonic

"S-Z-X-AC-X-P-X-CY"

Question 2(c) OR [7 marks]

Explain Architecture of 8085 with neat sketch.

Solution

The 8085 architecture consists of ALU, Registers, Control Unit, and Buses.

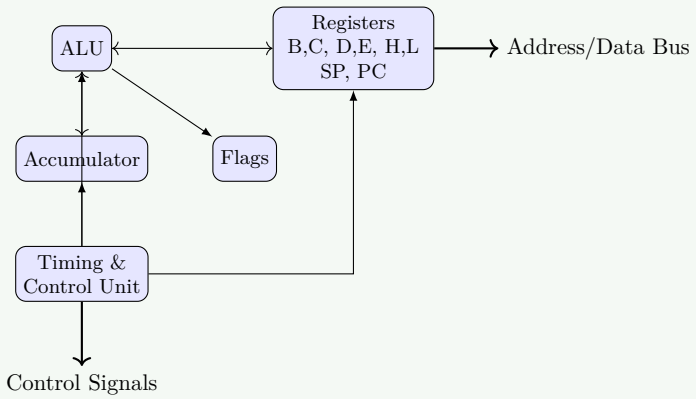

Figure 7. 8085 Architecture

- **ALU**: Performs arithmetic and logical operations.
- **Registers**: Store data (A, B, C...) and addresses (PC, SP) temporarily.
- **Control Unit**: Generates signals (RD, WR, ALE) for operation.
- **Buses**: Address (16-bit) and Data (8-bit) buses for communication.

Mnemonic

"ALU Registers Control Address Data (ARCAD)"

Question 3(a) [3 marks]

Explain Internal RAM Organization of 8051 Microcontroller.

Solution

The 8051 has 128 bytes of internal RAM organized as:

Table 8. RAM Organization

Address	Purpose
00H-1FH	Register Banks (4 banks of 8 registers each)
20H-2FH	Bit Addressable Area (16 bytes)
30H-7FH	General Purpose RAM (80 bytes)

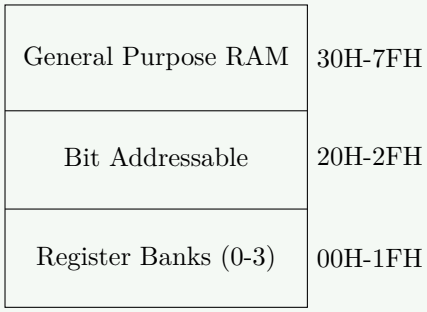

Figure 8. Internal RAM Map

Mnemonic

"Register Bit General (RBG)"

Question 3(b) [4 marks]

Explain Function of Each bit of TMOD SFR of 8051 Microcontroller.

Solution

TMOD (Timer Mode) register controls Timer 0 and Timer 1.

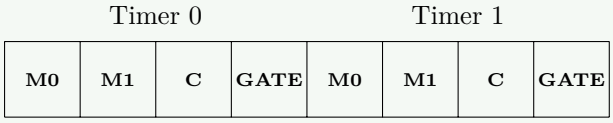

Figure 9. TMOD Register

- **GATE**: 1 = External gate control (INTx pin), 0 = Internal control.
- **C/T**: 1 = Counter mode, 0 = Timer mode.
- **M1, M0**: Mode selection (00: 13-bit, 01: 16-bit, 10: 8-bit auto-reload, 11: Split).

Mnemonic

"GATE C/T Mode1 Mode0"

Question 3(c) [7 marks]

Explain Architecture of 8051 with neat sketch.

Solution

The 8051 has Harvard architecture with separate program and data memory.

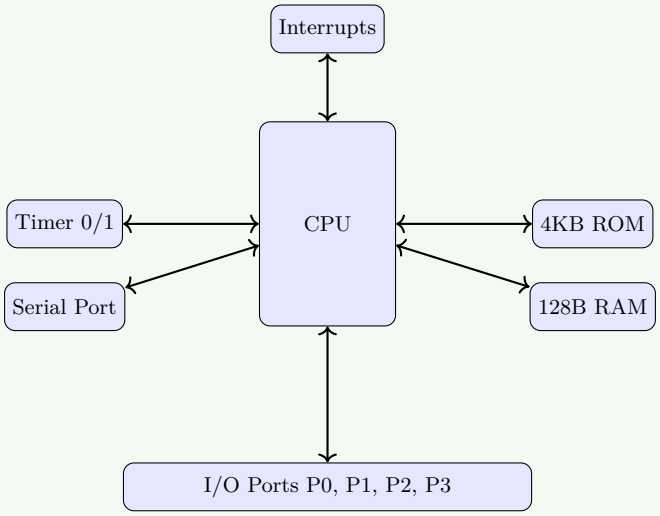

Figure 10. 8051 Architecture

- **Memory**: 4KB ROM (Program), 128B RAM (Data).
- **Peripherals**: 4 I/O Ports, 2 Timers, 1 Serial Port.
- **Interrupts**: 5 Sources (External, Timer, Serial).

Mnemonic

"CPU ROM RAM Ports Timers Serial Interrupts (CRRRPTI)"

Question 3(a) OR [3 marks]

Explain PSW SFR of 8051 Microcontroller.

Solution

PSW (Program Status Word) contains status flags.

D0							D7
P	**-**	**OV**	**RS0**	**RS1**	**F0**	**AC**	**CY**

Figure 11. PSW Register

- **CY**: Carry Flag. **AC**: Aux Carry.
- **RS1, RS0**: Register Bank Select (00-Bank0, 01-Bank1, 10-Bank2, 11-Bank3).
- **OV**: Overflow Flag. **P**: Parity Flag.

Mnemonic

"CY AC F0 RS1 RS0 OV - P"

Question 3(b) OR [4 marks]

Explain Function of Each bit of SCON SFR of 8051 Microcontroller.

Solution

SCON controls serial communication.

RI	TI	RB8	TB8	REN	SM2	SM1	SM0

Figure 12. SCON Register

- **SM0, SM1**: Mode selection (0-Shi.Reg, 1-8bit UART, 2-9bit Fixed, 3-9bit Var).
- **REN**: Receive Enable.
- **TB8/RB8**: 9th bit for transmit/receive.
- **TI/RI**: Transmit/Receive Interrupt flags.

Mnemonic

"SM0 SM1 SM2 REN TB8 RB8 TI RI"

Question 3(c) OR [7 marks]

Explain Pin Diagram of 8051 with neat sketch.

Solution

The 8051 is a 40-pin DIP package.

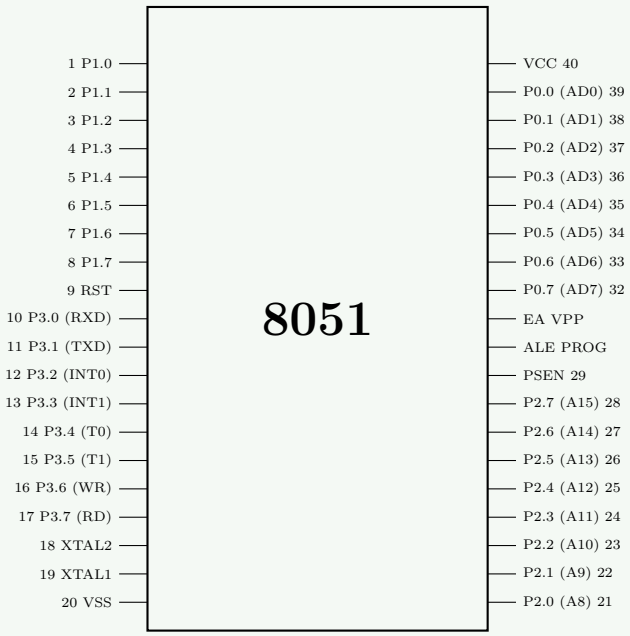

Figure 13. 8051 Pin Diagram

- **Port 0**: Multiplexed AD0-AD7. **Port 2**: High Address A8-A15.
- **Port 1**: I/O only. **Port 3**: Special functions (RX, TX, INT, T0, T1, WR, RD).
- **Control**: RST, ALE, PSEN, EA.

Mnemonic

"Port Power Crystal Control (PPCC)"

Question 4(a) [3 marks]

Write and Explain any Three Data Transfer Instructions of 8051 Microcontroller.

Solution

Table 9. Data Transfer Instructions

Instruction	Function
MOV A, R0	Move contents of R0 to Accumulator.
MOV R1, #50H	Move immediate data 50H to R1.
MOV 30H, A	Move Accumulator contents to direct address 30H.

Listing 1. Data Transfer Examples

```
MOV A, R0       ; A = R0
MOV R1, #50H    ; R1 = 50H
MOV 30H, A      ; [30H] = A
```

Mnemonic

"MOV Between Register Immediate Direct"

Question 4(b) [4 marks]

Write 8051 Assembly Language Program to Multiply Content of R0 and R1 and Store Result in R5 (Lower Byte) and R6 (Higher Byte).

Solution

Listing 2. Multiplication Program

```
    ORG 0000H

    MOV A, R0       ; Load Multiplicand
    MOV B, R1       ; Load Multiplier
    MUL AB          ; Multiply A * B
                    ; Result: B(High) A(Low)

    MOV R5, A       ; Store Lower Byte
    MOV R6, B       ; Store Higher Byte

    SJMP $          ; Stop
    END
```

Question 4(c) [7 marks]

List Addressing Modes of 8051 Microcontroller and Explain each with Example.

Solution

Table 10. Addressing Modes

Mode	Description	Example
Immediate	Data directly in instruction (#).	`MOV A, #50H`
Register	Data in register (Rn).	`MOV A, R0`
Direct	Data at direct memory address.	`MOV A, 30H`
Indirect	Address in register (@Ri).	`MOV A, @R0`
Indexed	Base + Offset (usually for ROM).	`MOVC A, @A+DPTR`
Relative	Offset added to PC (Jumps).	`SJMP LABEL`
Bit	Direct bit address.	`SETB P1.0`

Mnemonic

"Immediate Register Direct Indirect Indexed Relative Bit (I-R-D-I-I-R-B)"

Question 4(a) OR [3 marks]

Write and Explain any Three Logical Instructions 8051 Microcontroller.

Solution

Table 11. Logical Instructions

Instruction	Function
`ANL A, R0`	AND Accumulator with R0. Masking bits.
`ORL A, #0FH`	OR Accumulator with immediate 0FH. Setting bits.
`XRL A, 30H`	XOR Accumulator with memory. Toggling bits.

Listing 3. Logical Examples

```
ANL A, R0       ; A = A AND R0
ORL A, #0FH     ; A = A OR 0FH
XRL A, 30H      ; A = A XOR [30H]
```

Question 4(b) OR [4 marks]

Write 8051 Assembly Language Program to Subtract Number Stored in 2000h from 2001h and Store result in 2002h. (External Memory).

Solution

Listing 4. Subtraction Program

```
    ORG 0000H

    MOV DPTR, #2001H    ; Point to Minuend
    MOVX A, @DPTR       ; Load Minuend
    MOV R0, A           ; Save in R0

```

```
    MOV DPTR, #2000H    ; Point to Subtrahend
    MOVX A, @DPTR       ; Load Subtrahend
    MOV R1, A           ; Save in R1

    MOV A, R0           ; Restore Minuend
    CLR C               ; Clear Carry for SUBB
    SUBB A, R1          ; A = Minuend - Subtrahend

    MOV DPTR, #2002H    ; Point to Result
    MOVX @DPTR, A       ; Store Result

    SJMP $
    END
```

Question 4(c) OR [7 marks]

Explain Instructions: RET, PUSH, CLR PSW.0, RLC A, CJNE, NOP, ANL.

Solution

Table 12. Instruction Explanation

Instruction	Function
`RET`	Return from subroutine. Pops PC from stack.
`PUSH 30H`	Pushes contents of address 30H onto Stack.
`CLR PSW.0`	Clears Carry Flag (Bit 0 of PSW).
`RLC A`	Rotate A Left through Carry Flag.
`CJNE A, #dat, L`	Compare A with data, Jump to Label if Not Equal.
`NOP`	No Operation. Consumes time/space only.
`ANL A, #data`	Logical AND Accumulator with immediate data.

Mnemonic

"Return Push Clear Rotate Compare No-op AND"

Question 5(a) [3 marks]

List the application of Microcontroller in various fields.

Solution

Table 13. Applications

Field	Applications
Consumer	TV Remotes, Washing Machines, Microwaves
Automotive	ABS, Engine Control, Airbags
Industrial	Robotics, Process Control, Automation
Medical	Pacemakers, Glucose Meters
Communication	Mobile Phones, Modems
Home	Smart Thermostats, Security Systems

Question 5(b) [4 marks]

Interface Stepper Motor with 8051 Microcontroller and Explain in brief.

Solution

Stepper motor requires a driver like ULN2003 for current amplification.

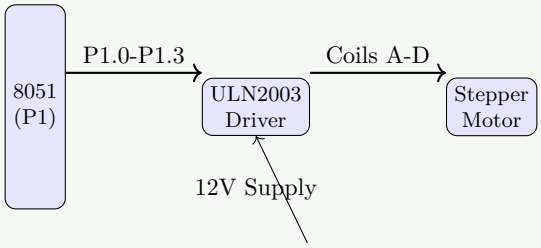

Figure 14. Stepper Motor Interface

Table 14. Half-Step Sequence

Step	P1.3	P1.2	P1.1	P1.0	Hex
1	0	0	0	1	01H
2	0	0	1	1	03H
3	0	0	1	0	02H
4	0	1	1	0	06H

Mnemonic

"Step Sequence Driver Protection (SSDP)"

Question 5(c) [7 marks]

Draw interfacing circuit to interface 4 LED at port 2.0 to 2.3 of microcontroller 8051 and write assembly language program to flash it.

Solution

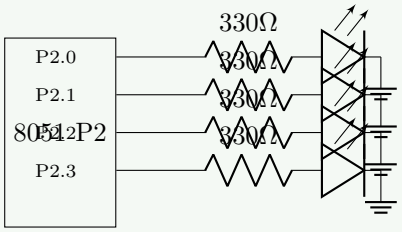

Figure 15. 4 LED Interface

Listing 5. LED Flashing Program

```
    ORG 0000H
MAIN:
    MOV P2, #0FH        ; Turn ON LEDs (P2.0-P2.3 = 1)
    ACALL DELAY
    MOV P2, #00H        ; Turn OFF LEDs
    ACALL DELAY
    SJMP MAIN
```

```
8
9   DELAY:
10      MOV R0, #255
11  L1: MOV R1, #255
12  L2: DJNZ R1, L2
13      DJNZ R0, L1
14      RET
15      END
```

Mnemonic

"Resistor LED Ground Program (RLGP)"

Question 5(a) OR [3 marks]

Draw Interfacing of Push button switch and LED with 8051 Microcontroller.

Solution

Switch at P1.0 (Input), LED at P1.1 (Output).

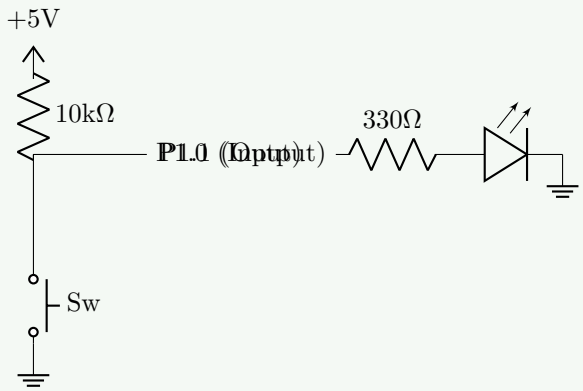

Figure 16. Switch and LED Interface

Mnemonic

"Pull-up Switch LED Current-limit (PSLC)"

Question 5(b) OR [4 marks]

Interface Relay with 8051 Microcontroller and Explain in brief.

Solution

Relay is an electromechanical switch. It isolates high voltage load from microcontroller.

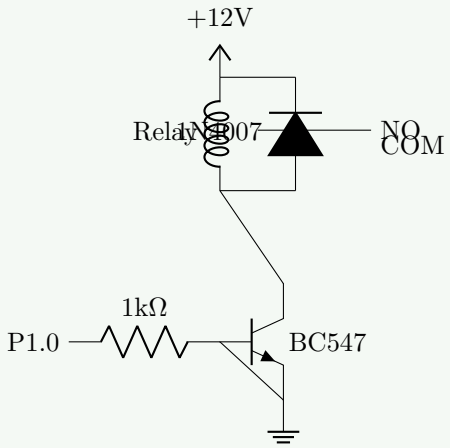

Figure 17. Relay Driver Circuit

- **Transistor**: Acts as switch. P1.0=1 → Transistor ON → Relay ON.
- **Flyback Diode**: Protects transistor from back EMF.
- **Isolation**: High voltage AC load is isolated from 5V logic.

Mnemonic

"Transistor Resistor Diode Relay (TRDR)"

Question 5(c) OR [7 marks]

Interface 7 segment LED with 8051 Microcontroller and write assembly language program to print 0 on it.

Solution

Common Cathode display connected to Port 1.

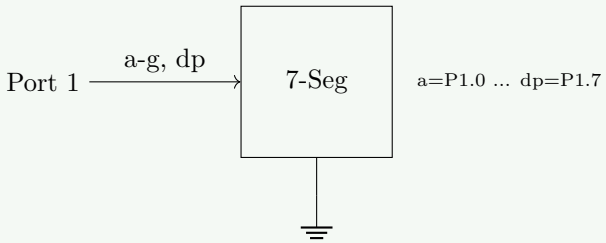

Figure 18. 7-Segment Connection

Table 15. Digit 0 Code

Digit	Segments (gfedcba)	Hex
0	0 1 1 1 1 1 1	3FH

Listing 6. Display 0

```
    ORG 0000H
MAIN:
    MOV P1, #3FH        ; Pattern for '0'
    SJMP MAIN           ; Loop
    END
```

Mnemonic

"Seven Segments Common Cathode Current-limit (SSCCC)"