Microprocessor and Microcontroller (4341101) - Winter 2023 Solution

Milav Dabgar

December 15, 2023

Question 1 [a marks]

3 Compare RISC and CISC.

Solution

Answer:

Table 1. RISC vs CISC

Feature	**RISC**	**CISC**
Instructions	Simple, fixed-length	Complex, variable-length
Execution	Single cycle	Multiple cycles
Addressing modes	Few	Many
Registers	Many	Few
Design focus	Hardware simplicity	Code density

Mnemonic

“RISCs Complete Instructions Simply”

Question 1 [b marks]

4 Compare Von-Neumann and Harvard architecture.

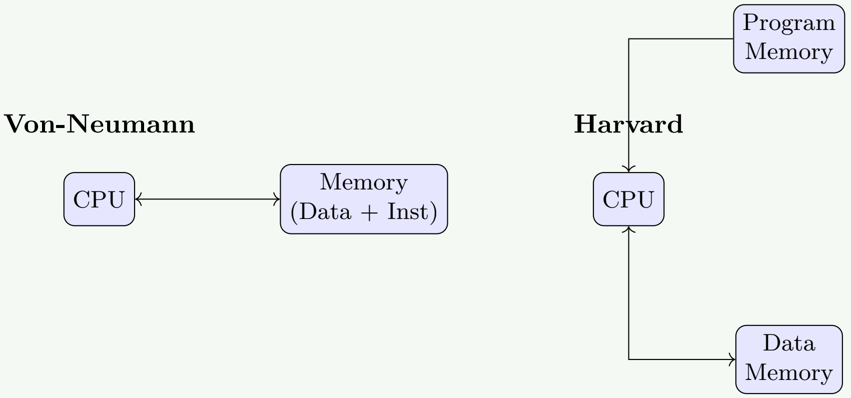
Solution

Answer:

Table 2. Von-Neumann vs Harvard

Feature	**Von-Neumann**	**Harvard**
Memory	Single shared memory	Separate program & data memory
Bus	Single bus for data & instructions	Separate buses
Speed	Slower (memory bottleneck)	Faster (parallel access)
Complexity	Simpler design	More complex
Applications	General computing	Real-time systems

Diagram:



Mnemonic

"Harvard Has Separate Spaces"

Question 1 [c marks]

7 Explain: 8085 Instruction Format, Control Unit, Machine Cycle, ALU

Solution

Answer:

1. Instruction Format:

Opcode	Operand 1	Operand 2

1-3 Bytes Total Length

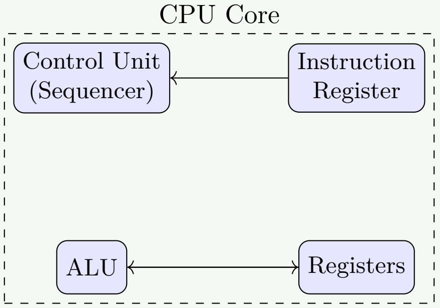
Contains opcode (3-8 bits) and 0-2 operands.

2. Explanations:

Table 3. Components

Component	**Function**
Instruction Format	1-3 byte structure with opcode and operands
Control Unit	Fetches, decodes instructions; generates signals
Machine Cycle	Basic operation cycle (T-states)
ALU	Performs arithmetic and logical operations

3. Diagram:



Mnemonic

"CIMA: Control Interprets, Machine Acts"

OR

Question 1 [c marks]

7 Compare Microprocessor and Microcontroller.

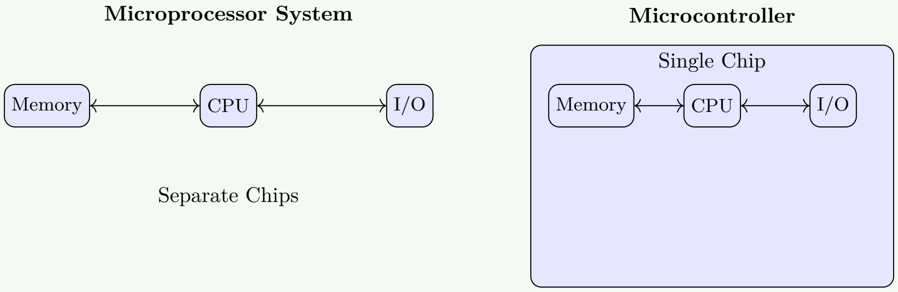
Solution

Answer:

Table 4. Microprocessor vs Microcontroller

Feature	**Microprocessor**	**Microcontroller**
Design	CPU only	CPU + peripherals
Memory	External	Internal (RAM/ROM)
I/O ports	Limited	Many built-in
Cost	Higher	Lower
Applications	General computing	Embedded systems
Power	Higher	Lower
Example	Intel 8085/8086	Intel 8051

Diagram:



Mnemonic

"Micro-P Processes, Micro-C Controls"

Question 2 [a marks]

3 Explain Instruction Fetching, Decoding and Execution Operation in microprocessor.

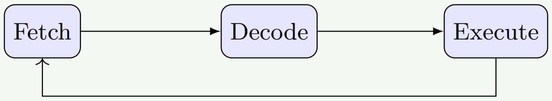
Solution

Answer:

Table 5. Operation Phases

Phase	Operation
Fetching	CPU gets instruction from memory using PC
Decoding	Determines operation type and operands
Execution	Performs the actual operation

Diagram:



Mnemonic

"FDE: First Get, Then Understand, Finally Do"

Question 2 [b marks]

4 Explain Bus Organization of 8085 microprocessor.

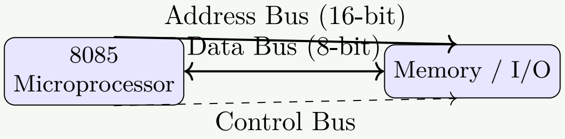
Solution

Answer:

Table 6. 8085 Buses

Bus Type	Width	Function
Address Bus	16-bit	Carries memory addresses (A0-A15)
Data Bus	8-bit	Transfers data (D0-D7)
Control Bus	Various	Manages data flow (RD, WR, IO/M)
Multiplexed	AD0-AD7	Lower address bits + data bits

Diagram:



Mnemonic

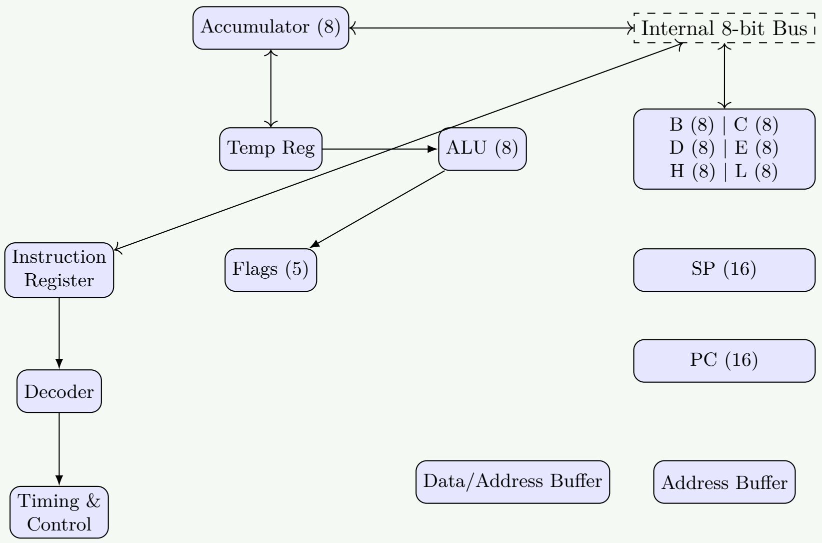
"ADC: Address points, Data flows, Control directs"

Question 2 [c marks]

7 Describe architecture of 8085 microprocessor with the help of neat diagram.

Solution

Answer:
Diagram:



- **ALU**: Performs arithmetic & logical operations
- **Registers**: Store data temporarily (A, B, C, D, E, H, L)
- **Control Unit**: Fetches & decodes instructions
- **PC**: Points to next instruction address
- **SP**: Points to top of stack

Mnemonic

"ARCBD: Architecture Registers Control Buses Data"

OR

Question 2 [a marks]

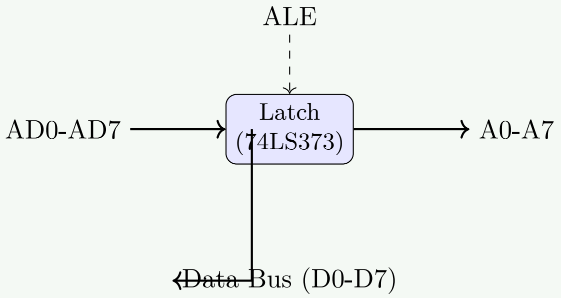
3 Explain De-multiplexing of Address and Data buses for 8085 Microprocessor.

Solution

Answer:

1. **ALE High**: Lower address (A0-A7) appears on AD0-AD7 lines. Latch captures it.
2. **ALE Low**: AD0-AD7 lines are used for Data (D0-D7).

Diagram:



Mnemonic

"ALAD: ALE Latches Address before Data"

OR

Question 2 [b marks]

4 Draw Flag Register of 8085 microprocessor & explain it.

Solution

Answer:
Flag Register (8-bit):

D7	D6	D5	D4	D3	D2	D1	D0
S	Z	X	AC	X	P	1	CY

- **S (Sign)**: Set if D7 is 1 (Negative result)
- **Z (Zero)**: Set if result is zero
- **AC (Auxiliary Carry)**: Carry from D3 to D4
- **P (Parity)**: Set if result has even number of 1s
- **CY (Carry)**: Carry out from D7

Mnemonic

"SuZie AC's Perfect CarrY"

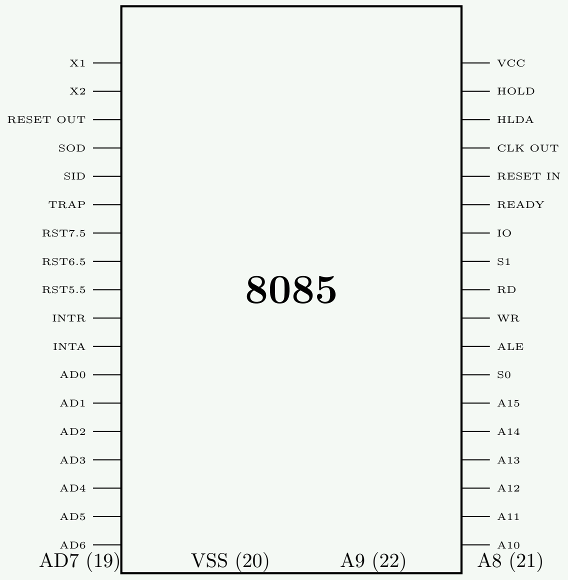
OR

Question 2 [c marks]

7 Describe Pin diagram of 8085 microprocessor with the help of neat diagram.

Solution

Answer:
Pin Diagram:



- **Address/Data**: Multiplexed AD0-AD7, A8-A15
- **Control**: RD, WR, IO/M, ALE
- **Interrupts**: TRAP, RST 7.5/6.5/5.5, INTR
- **Power**: VCC (+5V), VSS (GND)

Mnemonic

"ACID-PS: Address-Control-Interrupt-DMA-Power-Serial"

Question 3 [a marks]

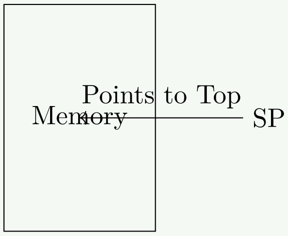
3 Explain Stack, Stack Pointer and Stack operation.

Solution

Answer:

- **Stack**: Reserved area of RAM used for temporary storage (LIFO).
- **Stack Pointer (SP)**: 16-bit register holding address of top of stack.
- **PUSH**: Decrement SP, Store data.
- **POP**: Retrieve data, Increment SP.

Diagram:



LIFO: Last In First Out

Mnemonic

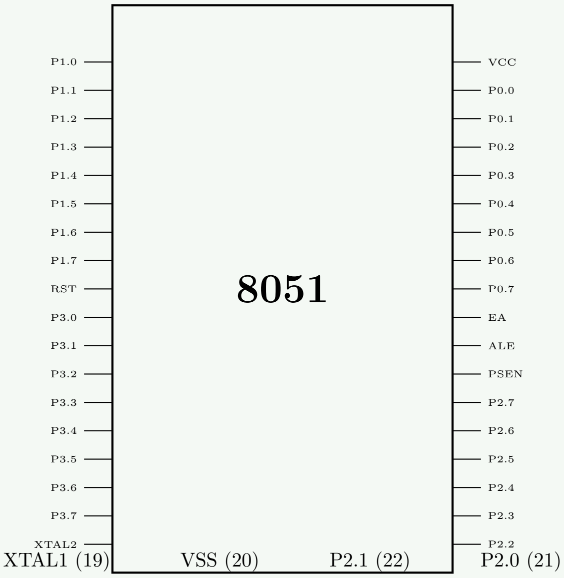
"SP Points to LIFO Lane"

Question 3 [b marks]

4 Draw Pin diagram of 8051 microcontroller.

Solution

Answer:



- **P0**: Multiplexed Address/Data
- **P1**: General I/O
- **P2**: High Order Address
- **P3**: Special Functions (Serial, Int, Timer)

Mnemonic

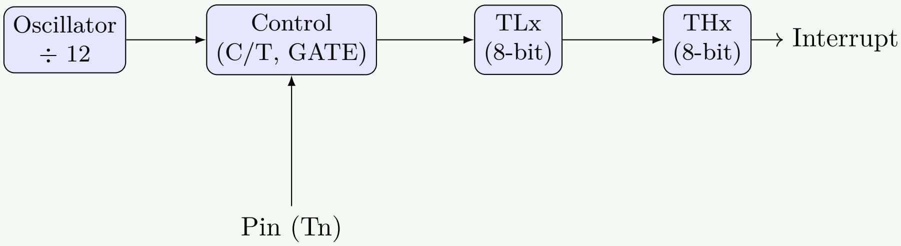
"PORT 0123: Data-General-Address-Special"

Question 3 [c marks]

7 Draw Timers/Counters logic diagram of 8051 microcontroller and explain its operation in various modes.

Solution

Answer:
Logic Diagram:



Modes:

- **Mode 0**: 13-bit timer mode.
- **Mode 1**: 16-bit timer mode.
- **Mode 2**: 8-bit auto-reload mode.
- **Mode 3**: Split timer mode.

Mnemonic

"MARC: Mode Auto-Reload Count"

OR

Question 3 [a marks]

3 List Common features of Microcontrollers.

Solution

Answer:

Table 7. MCU Features

Feature	**Purpose**
CPU Core	Process instructions
Memory	Store program (ROM) and data (RAM)
I/O Ports	Interface with external devices
Timers	Measure time intervals
Interrupts	Handle asynchronous events
Serial Comm	Transfer data with other devices

Mnemonic

"CRITICS: CPU ROM I/O Timers Interrupts Comm Serial"

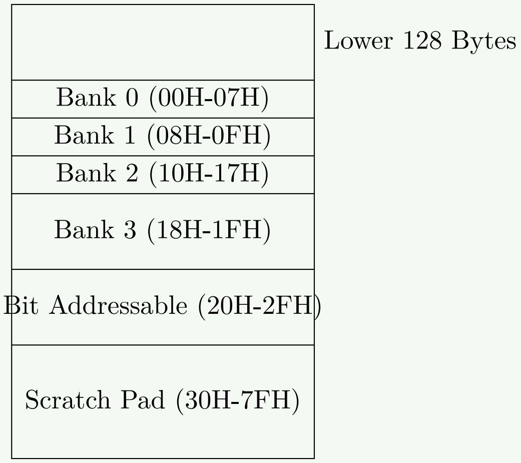
OR

Question 3 [b marks]

4 Explain Internal RAM Organization of 8051 microcontroller.

Solution

Answer:



- **Register Banks (00H-1FH)**: 4 banks of 8 registers (R0-R7).
- **Bit Addressable (20H-2FH)**: 16 bytes where each bit can be accessed.
- **Scratch Pad (30H-7FH)**: General purpose RAM.
- **SFRs (80H-FFH)**: Special Function Registers (upper 128 bytes).

Mnemonic

"RBBS: Registers Bits Buffer Scratch"

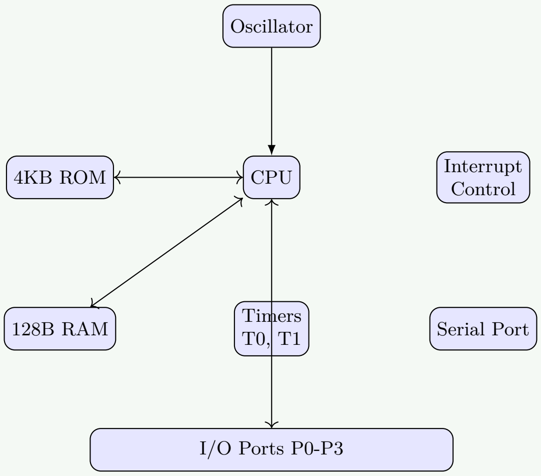
OR

Question 3 [c marks]

7 Explain architecture of 8051 microcontroller with the help of neat diagram.

Solution

Answer:
Diagram:



- **CPU**: 8-bit central processor.
- **Memory**: 4KB ROM (Code), 128B RAM (Data).
- **I/O**: 4 Ports (P0-P3).
- **Timers**: 2 16-bit timers.
- **Serial**: 1 UART channel.
- **Interrupts**: 5 sources.

Mnemonic

"CAPITALS: CPU Architecture Ports I/O Timer ALU LS-Interface Serial"

Question 4 [a marks]

3 Write an 8051 Assembly Language Program to Copy the data from external RAM Location 0123h to TL0 and Data from external RAM location 0234h to TH0.

Solution

Answer:

```
MOV  DPTR, #0123H   ; Load DPTR with source address 0123H
MOVX A, @DPTR       ; Read data from external RAM
MOV  TL0, A         ; Copy to Timer 0 low byte

MOV  DPTR, #0234H   ; Load DPTR with source address 0234H
```

```
MOVX A, @DPTR       ; Read data from external RAM
MOV  TH0, A         ; Copy to Timer 0 high byte
```

Mnemonic

"DRAM: DPTR Read Address Move"

Question 4 [b marks]

4 Write an 8051 Assembly Language Program to blink LED interfaced at port P1.3 at time interval of 1ms.

Solution

Answer:

```
AGAIN:  SETB P1.3         ; Turn ON LED at P1.3
        ACALL DELAY       ; Call delay subroutine
        CLR  P1.3         ; Turn OFF LED at P1.3
        ACALL DELAY       ; Call delay subroutine
        SJMP AGAIN        ; Repeat forever

DELAY:  MOV  R7, #250     ; Load R7 for outer loop
OUTER:  MOV  R6, #1       ; Load R6 for inner loop
INNER:  DJNZ R6, INNER    ; Decrement R6 until zero
        DJNZ R7, OUTER    ; Decrement R7 until zero
        RET               ; Return from subroutine
```

Mnemonic

"STACI: Set-Timer-And-Clear-Infinitely"

Question 4 [c marks]

7 List Addressing Modes of 8051 Microcontroller and explain all of them with the help of example.

Solution

Answer:

Table 8. Addressing Modes

Addressing Mode	Example	Description
Immediate	`MOV A, #25H`	Data is in instruction
Register	`MOV A, R0`	Data is in register
Direct	`MOV A, 30H`	Data is at RAM address
Indirect	`MOV A, @R0`	R0/R1 contains address
Indexed	`MOVC A, @A+DPTR`	Access program memory
Bit	`SETB P1.3`	Access individual bits
Relative	`SJMP LABEL`	Jumps with 8-bit offset

Mnemonic

"I'M DIRBI: Immediate Register Direct Bit Indexed"

OR

Question 4 [a marks]

3 Write an 8051 Assembly Language Program to Subtract the content of RAM location 11h from RAM location 14h; put result in RAM location 3Ch.

Solution

Answer:

```
MOV  A, 14H       ; Load content of RAM location 14H to A
CLR  C            ; Clear carry flag
SUBB A, 11H       ; Subtract content of 11H with borrow
MOV  3CH, A       ; Store result in RAM location 3CH
```

Mnemonic

"LCSS: Load-Clear-Subtract-Store"

OR

Question 4 [b marks]

4 Write an 8051 Assembly Language Program to generate a square wave of 50% duty cycle on bit 3 of Port 1 using Timer 0 in Mode 1.

Solution

Answer:

```
      MOV  TMOD, #01H   ; Timer 0, Mode 1 (16-bit)
AGAIN: MOV  TH0, #0FCH   ; Load high byte
      MOV  TL0, #18H    ; Load low byte (-1000 in 16-bit)
      SETB TR0          ; Start timer
      JNB  TF0, $       ; Wait for overflow
      CLR  TR0          ; Stop timer
      CLR  TF0          ; Clear timer flag
      CPL  P1.3         ; Toggle P1.3
      SJMP AGAIN        ; Repeat
```

Mnemonic

"MSTCCS: Mode-Set-Timer-Check-Clear-Switch"

OR

Question 4 [c marks]

7 Explain any seven Logical Instructions with example for 8051 Microcontroller.

Solution

Answer:

Table 9. Logical Instructions

Instruction	**Example**	**Operation**
ANL	`ANL A, #3FH`	Logical AND
ORL	`ORL P1, #80H`	Logical OR
XRL	`XRL A, R0`	Logical XOR
CLR	`CLR A`	Clear (set to 0)
CPL	`CPL P1.0`	Complement (invert)
RL	`RL A`	Rotate left
RR	`RR A`	Rotate right

Mnemonic

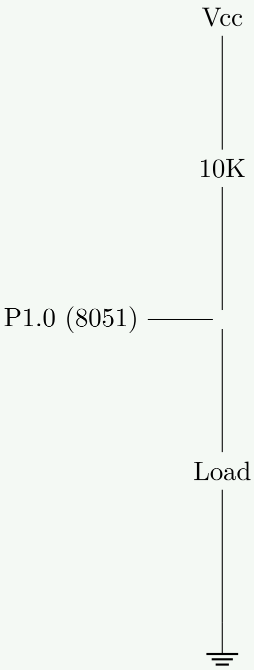
"A-OX-CCR: AND OR XOR Clear Complement Rotate"

Question 5 [a marks]

3 Draw Interfacing of Push button Switch with 8051 microcontroller.

Solution

Answer:
Diagram:



- **Pull-up Resistor**: Keeps pin HIGH when button is open.
- **Button Press**: Pulls pin LOW.

Mnemonic

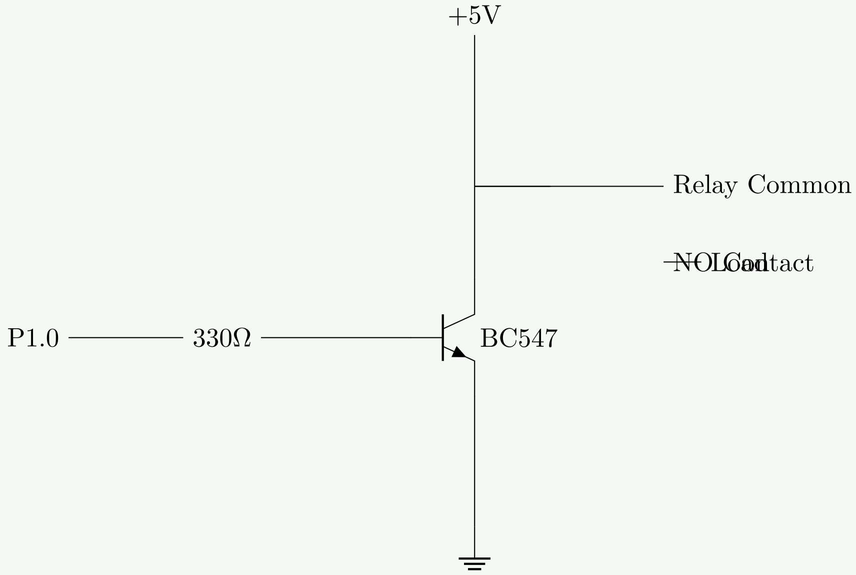
"PIP: Pull-up-Input-Press"

Question 5 [b marks]

4 Interface Relay with 8051 microcontroller.

Solution

Answer:
Diagram:



Mnemonic

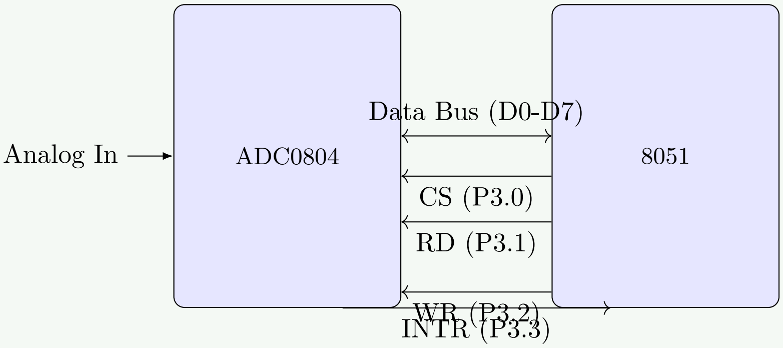
"TRIP: Transistor-Relay-Interface-Protection"

Question 5 [c marks]

7 Interface ADC0804 with 8051 microcontroller.

Solution

Answer:
Diagram:



- **Data Bus**: P1.0-P1.7 connected to D0-D7.
- **Control**: RD, WR, INTR for handshaking.

Mnemonic

"CRIW: Control-Read-Interrupt-Write"

OR

Question 5 [a marks]

3 List Applications of microcontroller in various fields.

Solution

Answer:

Table 10. Applications

Field	Applications
Industrial	Motor control, automation, PLCs
Medical	Patient monitoring, diagnostic equipment
Consumer	Washing machines, microwaves, toys
Automotive	Engine control, ABS, airbag systems
Communication	Mobile phones, modems, routers
Security	Access control, alarm systems

Mnemonic

"I-MACS: Industrial-Medical-Automotive-Consumer-Security"

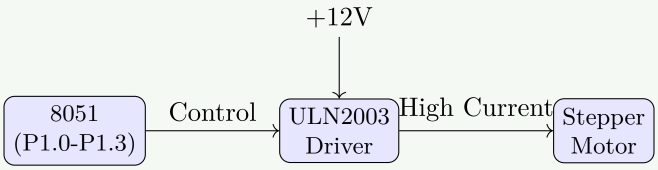
OR

Question 5 [b marks]

4 Interface Stepper motor with 8051 microcontroller.

Solution

Answer:
Diagram:



Sequence (Clockwise): 0x08, 0x0C, 0x04, 0x06.

Mnemonic

"PDCS: Port-Driver-Current-Sequence"

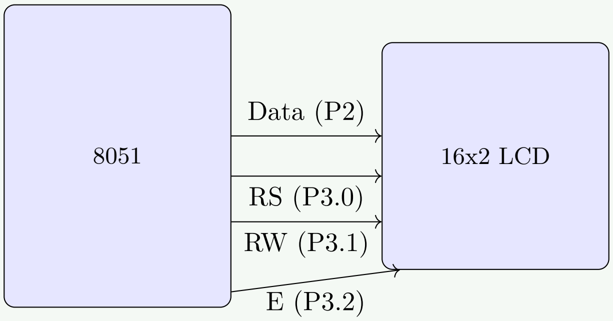
OR

Question 5 [c marks]

7 Interface LCD with 8051 microcontroller.

Solution

Answer:
Diagram:



- **Data**: Port 2 sends ASCII data/commands.
- **RS**: 0 for Command, 1 for Data.
- **E**: Enable Pulse to latch data.

Mnemonic

"DICE: Data-Instruction-Control-Enable"