CS466 Midterm Review Topics

- Microprocessor layout and identification of major components;
  - Devices RAM/ROM/etc..
  - I/O or Memory Mapped
- Wait States
- DMA
- Watchdog
- Scheduling, Round-Robin, etc (Chapter 5)
- Power-On to Main processing
- RTOS/Tasks and the Scheduler
- When does Scheduler run
- Task States
- Task Context
- Volatile
- Data-Sharing Issues (inter-task and isr-task)
- Interrupts;
  - Latency calculations
  - Priority Schemes
  - Signal Detection to ISR execute steps.
  - Shared Data
- Semaphores
  - Priority Inversion Scenario
  - Deadly Embrace Scenario
  - Avoidance Rules, Rules of thumb
- Register Access Macro
- Reentrancy vs. Threadsafe
- RTOS Characteristics
  - Tasks/Threads
  - Semaphores
  - Queues
  - Scheduler
  - Making sure low-priority task runs.
- Lab Lessons
  - Board Setup
  - Digital Input and Output Setup
  - ~~LED and Button Schematics~~
  - Lab Edit/Build/Make cycle
  - ~~When Pull-Up is required and not~~
  - Register Information and address lookup
  - TivaDriver Library
  - Tiva Board Characteristics, RAM/ROM/ASIC Blocks
  - File use? (Program, linker, startup, Makefile, etc)
- Moon Video