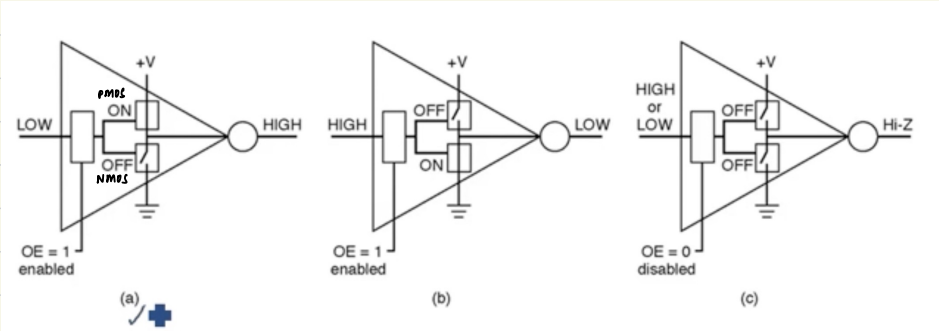
Tristate Outputs

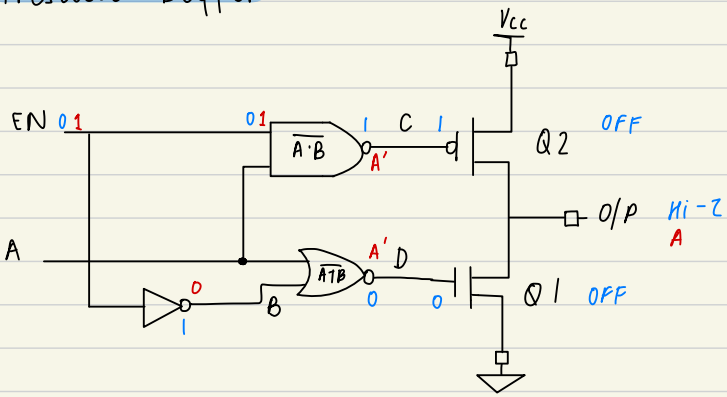
all 3 are valid

- logic 0, logic 1, high impedence (Hi-Z)
  - neither 1 or 0, acts like an open circuit (when both transistors are off)
- when a device is enabled, O/P is logic 0 or 1
- when disabled, O/P is Hi-Z
- eg. tristate buffer, tristate inverter

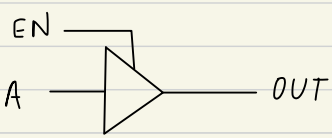
Tristate Inverter



Tristate Buffer



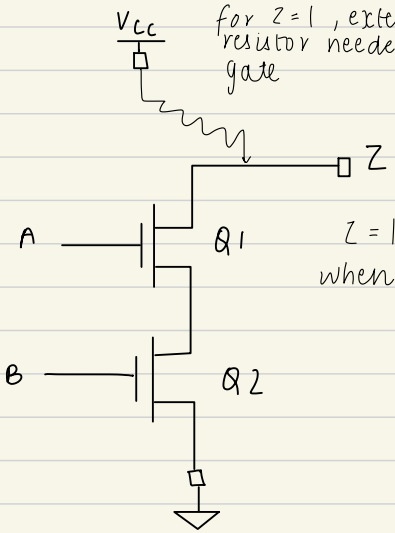
EN	A	B	C	D	Q1	Q2	OUT
L	L	H	H	L	OFF	OFF	Hi-Z
L	H	H	H	L	OFF	OFF	Hi-Z
H	L	L	H	H	ON	OFF	L
H	H	L	L	L	OFF	ON	H



Advantages of logic devices with tristate outputs

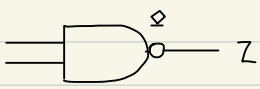
- 2/+ o/p can be connected together BUT only 1 can be enabled
- else bus contention takes place which results in a wrong o/p
- when o/ps are connected together, they share the same data bus
- non tristate output is essentially enabled and cannot be connected to a tristate output

Open-collector / drain output

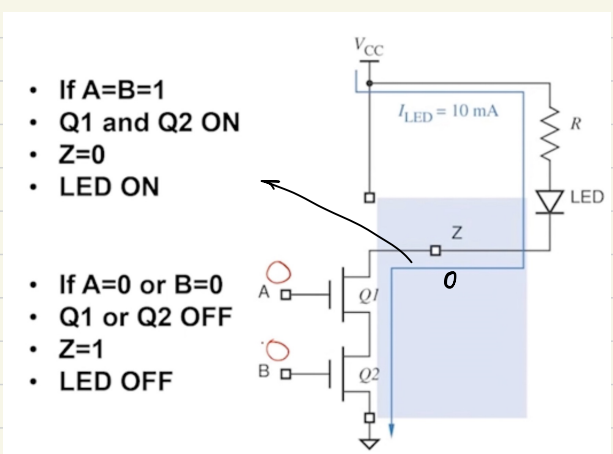


A	B	Q1	Q2	Z
L	L	OFF	OFF	open
L	H	OFF	ON	open
H	L	ON	OFF	open
H	H	ON	ON	L

open-drain symbol



- open-drain can drive LED
- ↑ can be tied together
  ↑
  ≡ to a AND gate



L11 practice problems

1. Two different logic circuits have the characteristics shown below.

   (a) Which circuit has better DC noise margin?

   (b) Which circuit has better DC fan-out?

   (c) Which circuit can operate at a higher frequency?

   (d) Are the two circuits able to drive each other?

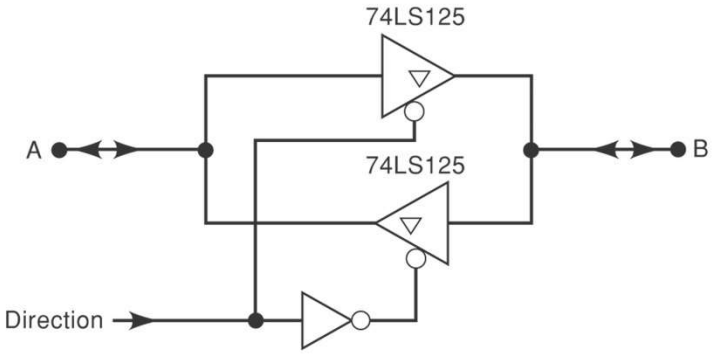
	Circuit A	Circuit B
Vcc (V)	5	5
VIH(min) (V)	1.6	1.8
VIL(max) (V)	0.9	0.7
VOH(min) (V)	2.2	2.5
VOL(max) (V)	0.4	0.3
IIH(max) (mA)	1.0	1.5
IIL(max) (mA)	1.0	1.5
IOH(max) (mA)	20	27
IOL(max) (mA)	25	30
tPLH (ns)	10	18
tPHL (ns)	8	14
PD (mW)	16	10

fan-out

fanout

(Adapted from Tocci, Widmer and Moss, ed. 10)

2. The figure below shows how two tristate buffers can be used to construct a bidirectional transceiver that allows digital data to be transmitted from A to B, or from B to A. Describe the circuit operation.
(Tocci, Widmer & Moss, ed. 10)



3. Describe the operation and hence obtain the Boolean expression for this CMOS circuit.
(Wakerly Ex. 3.59)