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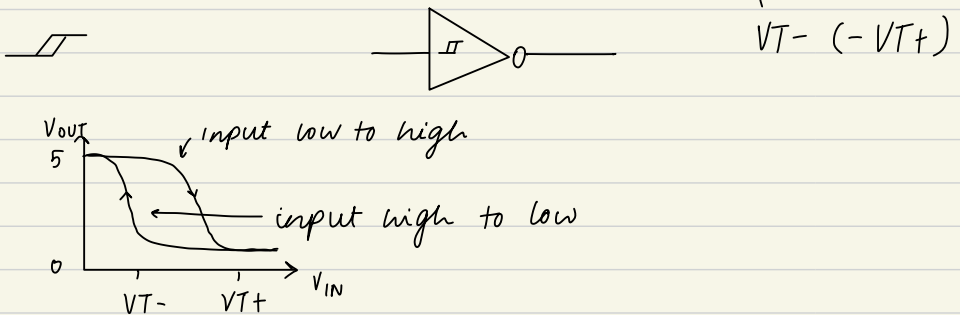
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## Inverter

### Schmitt-Trigger Inputs

- 2 threshold voltages  $V_{T-}$  and  $V_{T+}$
- when  $V_{IN} > V_{T+}$ ,  $V_{OUT}$  switches to low
- when  $V_{IN} < V_{T-}$ ,  $V_{OUT}$  switches to high
- the non-symmetric is called **hysteresis**



- this one is more stable than a standard inverter when  $V_{IN}$  rises slowly / fluctuates around  $V_T$

## Combinational PLA

- PLD : programmable logic devices
  - PLA, PAL, CPLD, FPGA ← examples
  - PLA : prog. logic array
  - PAL : prog. array logic
  - CPLD : complex PLD
  - FPGA : field programmable gate array
  - SoM / SOP can be implemented on PLA
  - $\langle \text{no of input} \rangle \times \langle \text{no of output} \rangle$  PLA
- } simple
- } complex

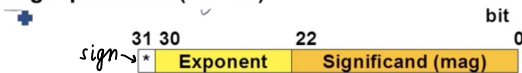
## Fixed-point Numbers

- radix point has a fixed position among int and frac
- int only (usually)
- dis. advantages
  - relatively small range of numbers that can be represented
  - possible loss of significant digits during computation

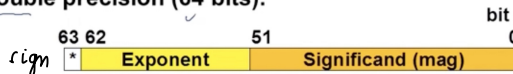
## Floating-point number

- $S X R^E$  ← exponent : signed fixed point int  
    ↑    ↑ radix : base (2 binary, 8 octal etc)  
significand : signed fractional fixed point no

### Single precision (32 bits):



### Double precision (64 bits):

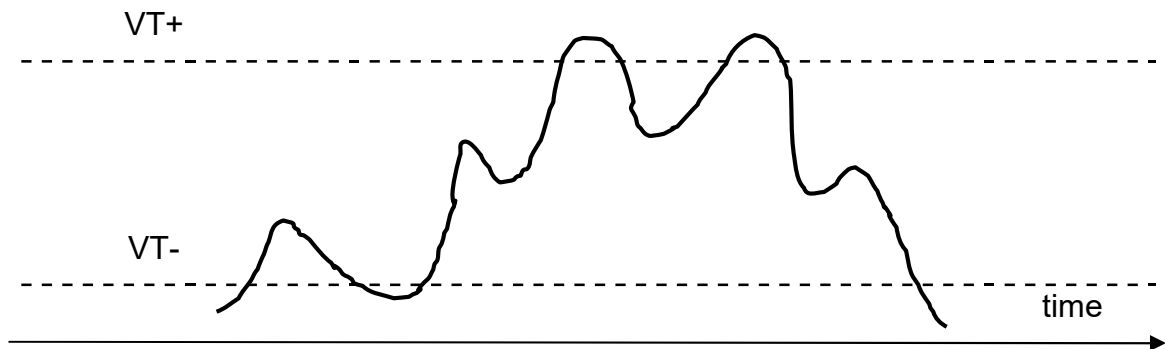


- \* is the sign bit of significand
- radix is 2
- significand is in sign-magnitude notation
- exponent is in 2's complement notation

**L12 practice problems**

1. Given the following input waveform and threshold voltages  $V_{T+}$  and  $V_{T-}$ , sketch the output waveforms for each Schmitt-Trigger device below:

- (a) buffer  
(b) inverter



2. Implement the given truth table using the following programmable logic device. Indicate the inputs, outputs and programmed connections clearly on the PLA diagram.

(Hint: use Karnaugh map to first obtain a minimum-cost SOP Boolean expression for x and for y)

Inputs				Outputs	
a	b	c	d	x	y
0	0	0	0	1	1
0	0	0	1	1	0
0	0	1	0	1	1
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	1	0
0	1	1	0	0	1
0	1	1	1	0	1
1	0	0	0	1	1
1	0	0	1	0	1
1	0	1	0	1	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	1	0	1
1	1	1	0	1	0
1	1	1	1	1	0

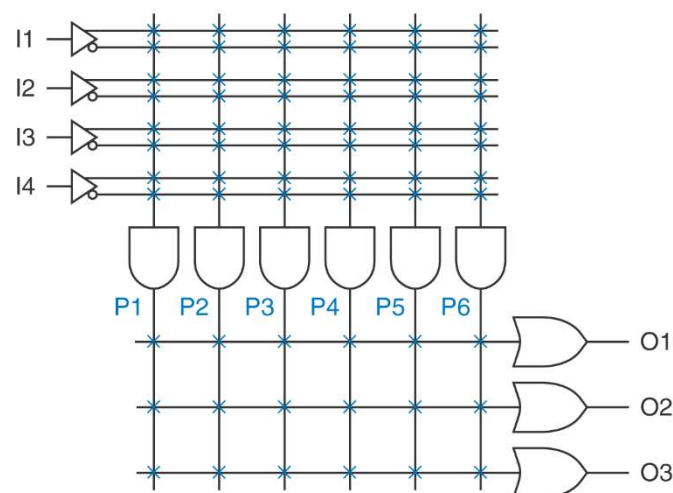


Figure 6-22

Compact representation of a  $4 \times 3$  PLA with six product terms.

3. A digital system uses a 16-bit fixed point representation for unsigned numbers, with 8 bits allocated to the integer portion and 8 bits allocated to the fractional portion.

The 16-bit data format (in 4-bit groups for easy reading) is:

xxxx xxxx yyyy yyyy

where xxxx xxxx is the 8-bit integer portion, and yyyy yyyy is the 8-bit fractional portion.

- (a) What is the smallest non-zero binary value that can be represented in this system? What is this value in decimal?
- (b) What is the largest binary value that can be represented in this system? What is this value in decimal?
- (c) What is the 16-bit representation of the decimal value 8.7? Is this an exact representation?