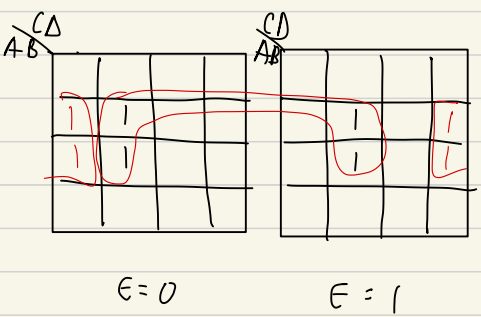
- adjacent differ by 1 bit
- SOP : OR O/P 1 $XY + XY' = X$
- POS : AND O/P 0 $(X+Y)(X+Y') = X$
- grouping and then eliminating all varying values
  - 2 ~ 1
  - 4 ~ 2
  - 8 ~ 3

→ overlap is allowed
→ biggest and fewest loops
→ loop one and use minterm notation
→ loop zeros and use maxterm notation

5 input is 3D



E = 0 E = 1

- DONT CARE

O/Ps for inputs that don't matter

eg. I/P : BCD digit
O/P : high ($x \in [0,5]$)
low ($x \in [6,9]$)

BCD has a limit of 9

	A	B	C	D	O/P
0	0	0	0	0	1
	⋮				⋮
5	0	1	0	1	1
6	0	1	1	0	0
	⋮				⋮
9	1	0	0	1	0
	⋮				X
					X
15	1	1	1	1	X

} don't care

in a K-Map 'don't cares' can be used as a joker card. can be taken as 1 or 0 in loops to make bigger loops. and those that aren't looped can be treated as the opposite

and give more simplified SOPs/POSs

L8 practice problems

1. Design a combinational logic circuit that converts a 4-bit Excess-3 code into a BCD code. Your design needs to accept only those inputs that produce valid BCD codes. Use K-map method for simplification and make use of any don't care conditions.

AB \ CD	00	01	11	10
00	0	0	1	0
01	1	1	1	1
11	X	X	X	X
10	1	1	X	X

Hint: this circuit has 4 inputs and 4 outputs. To fulfill the design, a Boolean expression must be obtained for each output.

An excess-3 code is obtained by adding the decimal value 3 to a BCD code. For example, decimal 0 is 0000 in BCD, which is 0011 in excess-3. See partial truth table below.

Partial truth table:

Input				Output			
Excess-3 code				BCD code			
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
1	1	0	0	1	0	0	1

3 2 1 0 ← 4 KMAPS

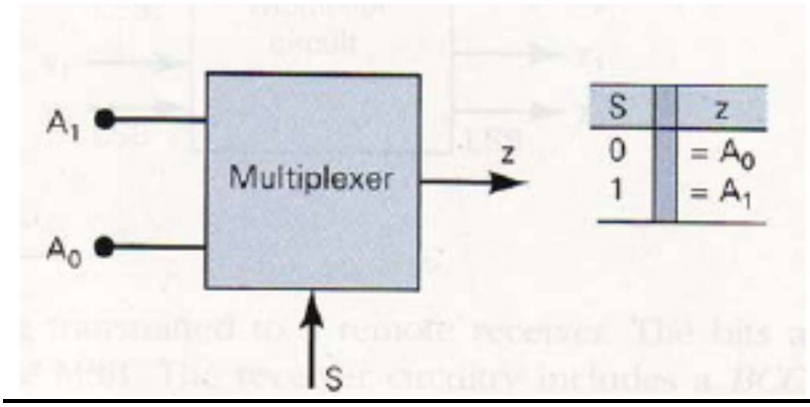
2. Problem 4.7 from Tocci 9th Ed.
A 4-bit binary number is represented as A3, A2, A1, A0 where A0 is the LSB. Design a logic circuit that will produce a High output whenever the binary number is greater than 0010 and less than 1000.

Note: otherwise the circuit produces a LOW output.

Design typically means a Boolean expression must be obtained for the circuit output. With the expression, a logic circuit diagram may be drawn if needed.

3. Problem 4-35 from Tocci 9th Ed.
Design a logic circuit that has two signal inputs A1 and A0 and a control input S so that it functions according to the requirements given in the figure below. This circuit is a multiplexer which will be covered in the MSI syllabus.

Original_Z =
$S \cdot A_1 + A_0 S'$



4. Modify the circuit obtained in Question 3 such that it now has an active-high enable input EN whose effect is shown in the new truth table:

Inputs		Output
EN	S	Z
0	X	0
1	0	A0
1	1	A1

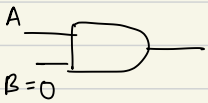
X = “don’t care”, i.e. 0 or 1

You may describe the modification with words or sketch a diagram to illustrate

mod = EN • (Original_Z)

ENABLE / DISABLE ← design feature

- enabled : if O/P can change w/ change in I/P
- disabled / inhibited : O/P is fixed (0 or 1)

eg. 

$X = A \cdot 0 = 0$ regardless of A
∴ disabled.