

a good logie circuit diagram

pin numbers, IC numbers, component values, signal names and power supply voltages clearly indicated bubble to bubble design

 $V_{\mathrm{DD}} = +5.0 \ \mathrm{V}$

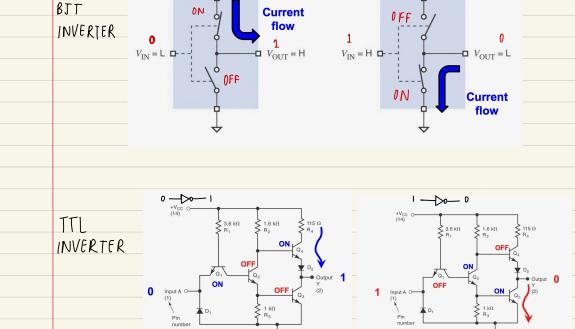
active levels

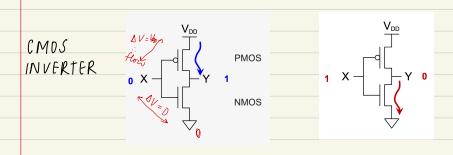
(a)

 $V_{\rm DD} = +5.0 \text{ V}$

all indicated

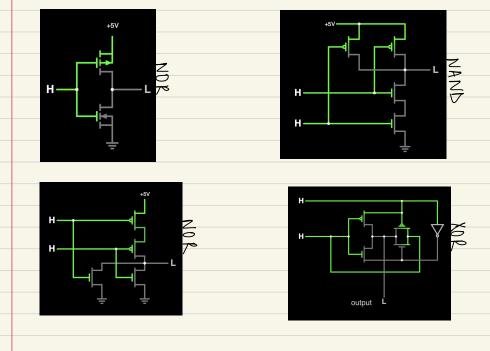
back to transistors as a switch





CMOS LOGIC URULITS

· series: all must nork · parallel: at least one must work



L10 practice problems

CMOS Logic

Determine the truth tables for the following CMOS logic circuits.

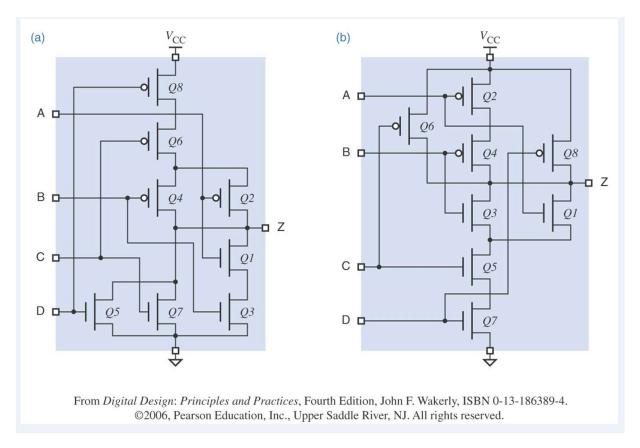


Fig. X3.11

Hint:

From the circuit diagram

Step 1: identify the inputs (e.g. A, B, C, D)

<u>Step 2</u>: identify the pair of transistors directly controlled by each input (e.g. input A controls Q1 and Q2)

<u>Step 3</u>: identify all the possible current paths (series as well as parallel) from Vcc to output so as to make output = 1.

For each possible path, identify the correct input values, and fill up the corresponding rows in the truth table with output=1

<u>Step 4</u>: identify all the possible current paths (series as well as parallel) from output to GND so as to make output = 0.

For each possible path, identify the correct input values, and fill up the corresponding rows in the truth table with output=0

Page 1 ©2021 NTU

