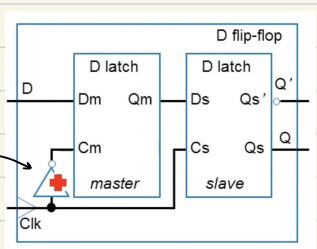
Limitations of D latches

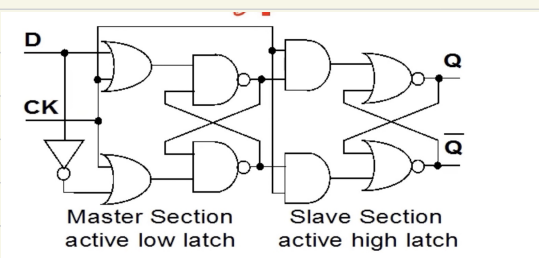
propagation of a value through the latch is dependent on the time period of the clock and is hence hard to predict.

soln. edge triggered flip-flops

- logic: at each clock rising edge, each flip flop takes D input and gives Q output
- implemented: 2 step process using 2 oppositely enabled latches (master-slave)

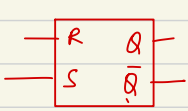


has a delay

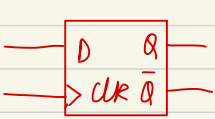


soln: use an active low version of the latch ↑

note: latch ≡ level-sensitive (O/P changes when enable is ↑)
flip-flop ≡ edge-triggered (+ve (0→1) or -ve (1→0))
↑ assumed to be



latch



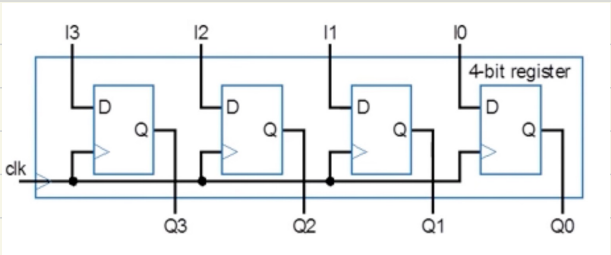
flip-flop

→ symbol: ▷ on control input

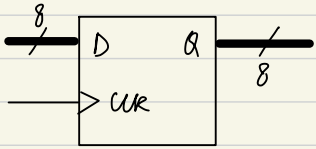
- D flip flop : $Q = D$ at rising edge of C
- J-K flip flop : $Q = 1$ if j is asserted
  $Q = 0$ if k is asserted
  Q toggles is J & K are asserted
  } at r.e of C
- T flip-flop : Q toggles if $T = 1$ at r.e of C

Registers = multiple D flip-flops

- stores multibit signals



- "fundamental sequential component"
- symbol :



- timing diagram :