

Digital circuits integrated digital circuits · resistors, diodes and transitors on a single piece of semiconductor material called substrate / die / chip resistor · diodes (current flows only in 2 way) translators (act as a switch) (most imp) < 3 pins Resistor LED (diode) 5 V * transistor

Scale of Integration (SI)

complexity of a circuit of no of gates

Small-scale

medium - Scale

large

VLSI

utra LSI

Scale of Integration (SI)

no of gates

12

12-99

100-9999

100-9999

100-99999

> 1000000

74LS283

eg of SSI

simple scale
of integration

open circuit causes at least a part of the circuit to not work due to no current flow through it

short circuit causes a large amount of current to gush through a part of the circuit

transistors used to make logic switch between High and Low

conductor transistor-transitor logic complimentary metal-oxide semi (MOS circuits TTL circuits → unipolar field-effect → bipolar junction translators BJT MOSFET (MOS field-effect trans) → base, emitter, collector → gate, drain, source

→ w/ correct voltage at G, → w/ correct voltage at B, current will flow between when will flow between C and E S and D

NMOS from PMOS S,D made derection S,D made

from n-type from p-type

TTL Family

different profixes

differ in electrical characteristics such as power dissipation, delay time, switching speed

· same pur layout and logic function

| TTL series | Prefix | E.g. |
|-----------------------------------|--------|---------|
| Standard | 74 | 7404 |
| High-speed | 74H | 74H04 |
| Low-power | 74L | 74L04 |
| Advanced low-power Schottky | 74ALS | 74ALS04 |

CMOS Family

· old series not compatible with TTL

HC series pin-compatible with TTL (they share the same pin layout)

· ACT series is electrically-compatible with TTL (have similar voltage and current requirements and can be connected together)

L, (MOS O/P → TTL I/P or vice-versa is cool

| CMOS | Prefix | E.g. |
|-------------|--------|---------|
| series | | |
| old | 40/140 | 4001 |
| | | 14001 |
| metal gate | 74C / | 74C02 |
| high speed/ | 74HC | 74HC02 |
| elec. comp | 74HCT | 74HCT02 |
| with TTL • | / | |
| | | |

CMDS > TIL

transistor as the only circuit element greater packing density simpler fabrication process were power dissipation greater fan-out

logic-level voltage ranges

TTL: Vcc nominally +5V

common collector voltage

(MOS:

→ VDD ranges from +3 to +18 V

voltage drain drain w when CMOS and TTLIG are used together, 5V is used.

Incompatible voltage ranges

Logic 1 0/Pon to I/Pomos is indeterminate logic 0 ope cmos to IP TTL Logic 0

aka floating inputs

what if pins are left unconnected in circuit

noise pick up - connect unused inputs to vice or gnd

→ picks up noise and may allow a huge amount of current to flow through IC

→ †damages IC

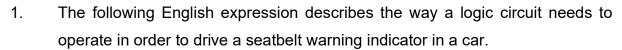
→ accuraised pins MUST be connucted. TO VCC or gnd.

active levels
a signal is called when it
outive high: gives named result when it is logic

· active low : gives named result when its logic 0

active low: <NAME>* if a <NAME>* signal exists, do not high: <NAME> assume existence of <NAME> _ · when a signal gives the result, its said to be asserted else its regated

L9 practice problems



If the driver is present and the driver is not buckled up and the ignition switch is on, then turn on the warning light.

AND connector

Using active high inputs driver present, buckled up and ignition on, design a circuit to produce the active high output warning_light. = $(dnvr_prosent)$ (a) Construct the truth table. $(bulled_up)^7$ $(ignitim_m)$

- (b) Write the Boolean expression for warning light.

TT row 6

(Question from Tocci, Widmer and Moss, 10th ed. Example 3-24)

Repeat Question 1. But this time with active low inputs driver present*, OR buckled_up*, ignition_on* and <u>active low</u> output_warning_light*.

> Note the meaning of active low. E.g. driver present*=0 when the driver is present.

- 3. Repeat Question 1. But this time with active low inputs driver_present*, buckled_up*, active high input ignition_on and active high output warning_light.
- A logic circuit has four inputs A, B, C*, D* and one output F. 4. HHLL * denotes active low signals.

The output F is only asserted when either A or C* is asserted (but not both), and either B or D* is negated (but not both).

Construct the truth table for F and obtain its canonical sum-of-minterm expression.

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