

	1.	Char	acterust	iU	of Instr	uctions	
instructions	are	als o	stored	in	binary	patterns	called

for us, they are represented as mneumohics

machine code

•	ARM (32-bit CPU)eg.	
	()	
	0x00)	

OXOI > -> MOV RI, RO
OXAO

add

instructions must be saved sequentially Von neumann executive model

instructions or

Turing machine memony is partitioned into separate code and data segments

011 A								
11/100 G								
C 2. ARM Instruction Format								
the in an a	excapable that							
W W W	example study	-						
MoV = move	instruction							
V								
takes 2 operand; copies source to destination								
: MOV R1, RD		RO	0x1234	, RO 0×123				
1. MUV R1, RU		RI	0x 000	$\rightarrow R_1 0 \times 123$				
dest so				1 (2 - 2 - 2				
here, both a	perands are	registe	UKC					
,		97 -01	- ' '					
3. 1	Instruction orga	anisatio	m in me	mory				
				V				
	machine code is executable, unlike data							
	utnuctions int	t mau	rune cod	e is colle				
encoding	the encoded	in 1+m ct	י אחי					
CIW / Chuz	wa entonata	JAITUU	LUIL					
instructions	Op-code	0	perands					
format	1		1					
	code that	info	about	data.				
defines what which to use and								
	operation to do) when	e to stor	e result				
			000	C (1				
some operation	ons simply the	ange 1	orogram	tow of the				
IZVOVYVY KIWIVI		M						
0.000	sol oriode proc	00		C / Certin				
0.1.00.000	so, whose proc		300 3 3 0					

4.0 pcode · n instructions need logzn bits to encode it

· more the variety of instructions, longer is the length of each instruction

its a tradeoff bird software and hardware = a multiplier will take up a lot of hardware the method by which an operand is specified is called addressing mode encoding the operand. addressing mode

, a lot of ways

RO-R12 are general purpose

R13 R14 is R15 is

RIA is

R15 is R14 IS

is the link

R11 > FP R13 → SP

R14 -> LR R15 → PC

Program Counter

RIS Keeps it

A Simple Processor

Basic components of a simple processor (CPU) and its interface signals to external main memory.

